MAGNETIC TAPE CONTROLLER

TRAINING MANUAL

FIRST EDITION

CONTROL DATA
CORPORATION

MAGNETIC TAPE CONTROLLER T.M.

FIRST EDITION

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Address comments concerning this manual to:

CONTROL DATA EDUCATION INSTITUTES
4530 West 77th Street
Minneapolis, Minnesota 55435

ATTN: MGR of CURRICULUM
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FOREWORD

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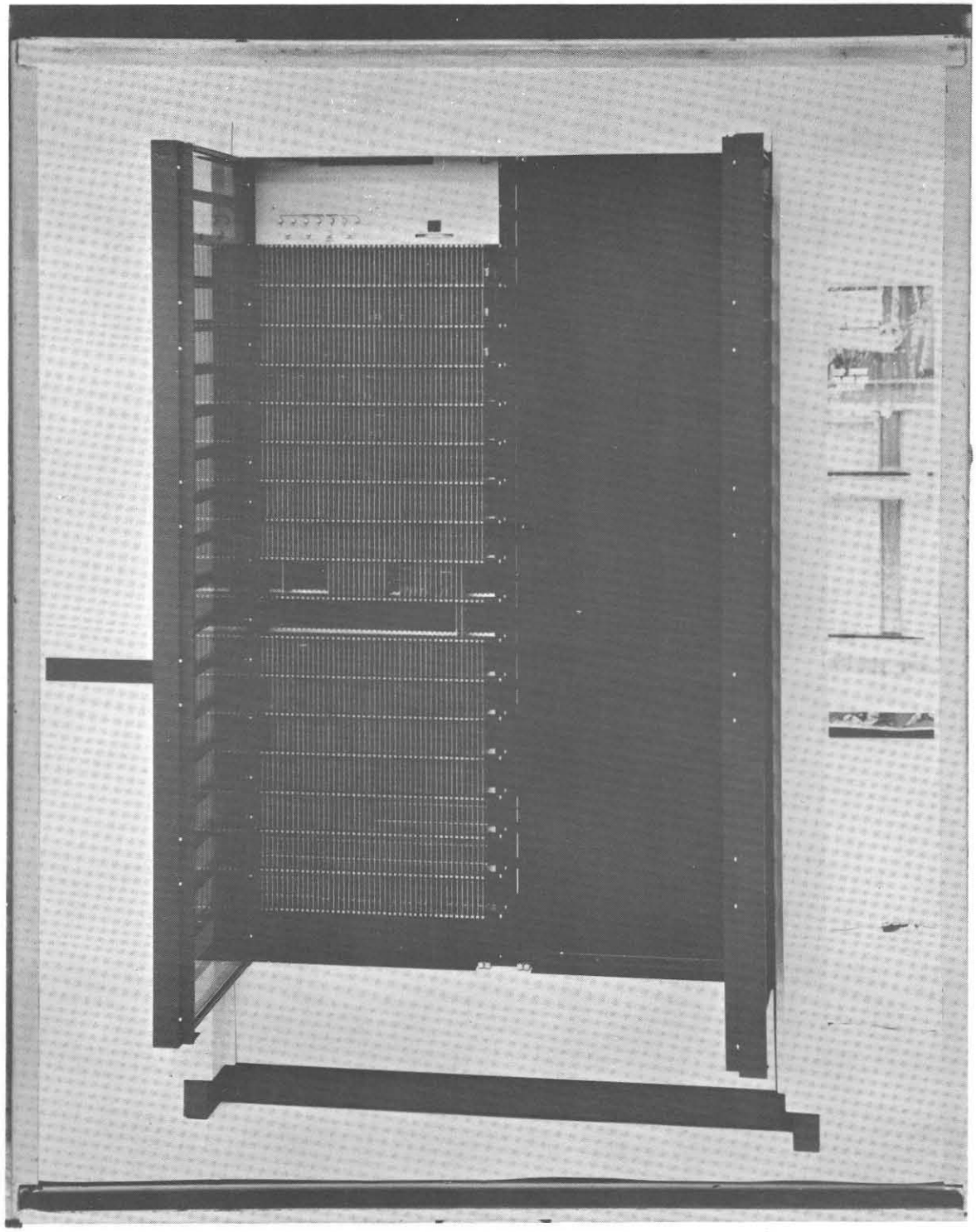
GENERAL DESCRIPTION



3228/3229 Magnetic Tape Controller

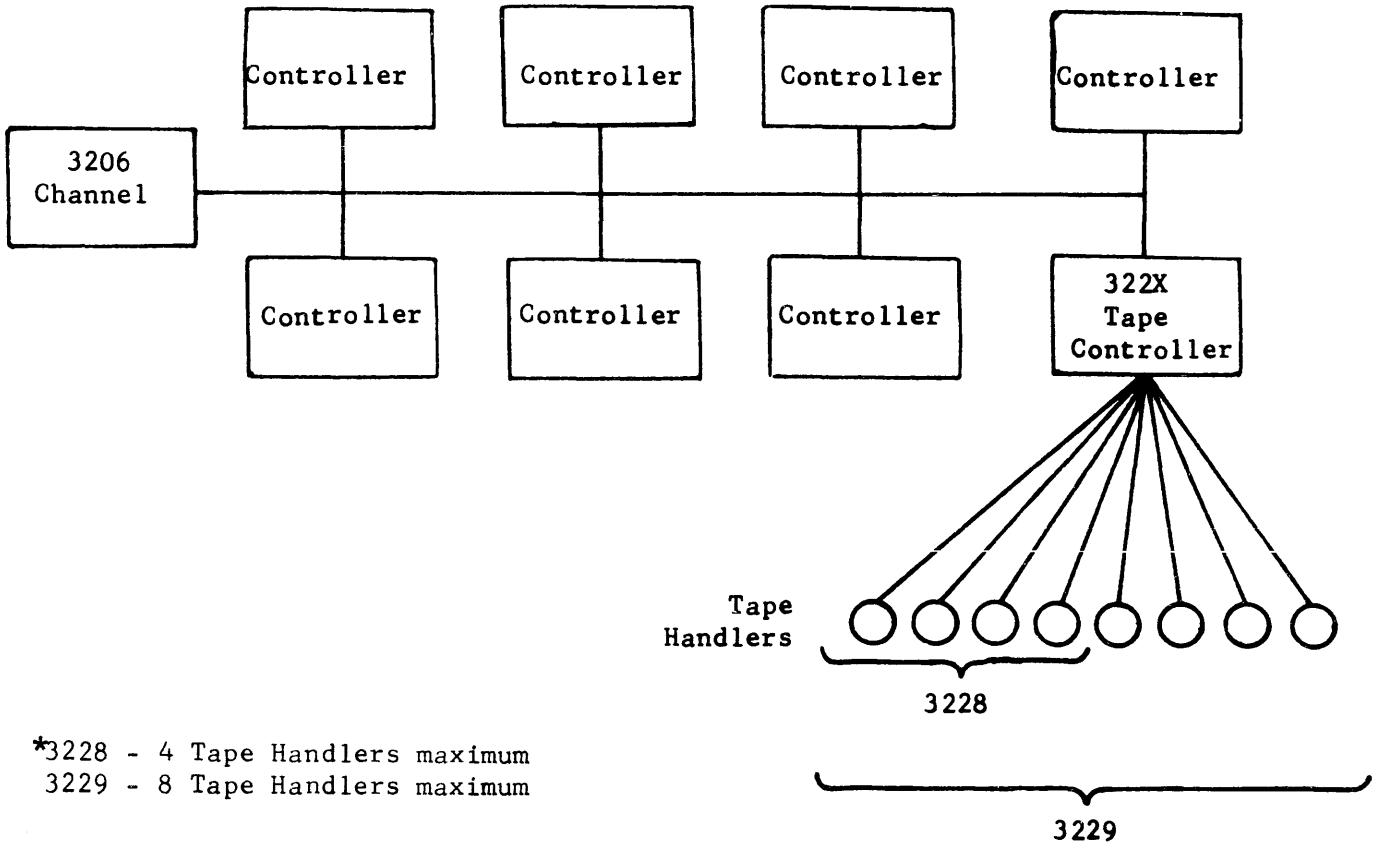
CHAPTER I

GENERAL DESCRIPTION

INTRODUCTION

The Control Data 3228 or 3229 Magnetic Tape Controller* are Input/Output devices for a 3000 series computer system. The controller can be cabled as one of the eight possible controllers on one Data Channel (see figure 3-1-1). The scheme of selection and operation of this or any controller on the channel follows a method inherent in all of the 3000 series peripheral equipment.

The controller allows the data channel to select a particular tape handler and modifies and synchronizes data flow. The controller is used with any of the 60X Tape Handlers. The 3228 may use up to four tape handlers; the 3229 up to eight. The tape handlers are selected and operated by the exchange of requests and replies typical to the 60X tape system. The controller can read or write on one tape handler at a time. Search, Rewind, and other indexing functions of the tape handler, once initiated, frees the controller on the data channel for other operations.



*3228 - 4 Tape Handlers maximum
3229 - 8 Tape Handlers maximum

Figure 1-1

SWITCHES AND INDICATORS

EQUIPMENT SELECTION SWITCH

An Equipment Selection switch is associated with each channel. The setting of this switch designates the controller as equipment number. Any interrupts coming from the controller will be transmitted on one of the eight interrupt lines corresponding to the setting of the Equipment Selection switch.

When a controller is connected to a tape handler, a white indicator in the Equipment Selection switch is illuminated. When a tape handler is in use, the Equipment Select switch on the tape handler lights.

If a transmission parity error occurs during a Function, Read, or Write operation, a red indicator in the Controller Equipment Selection switch lights.

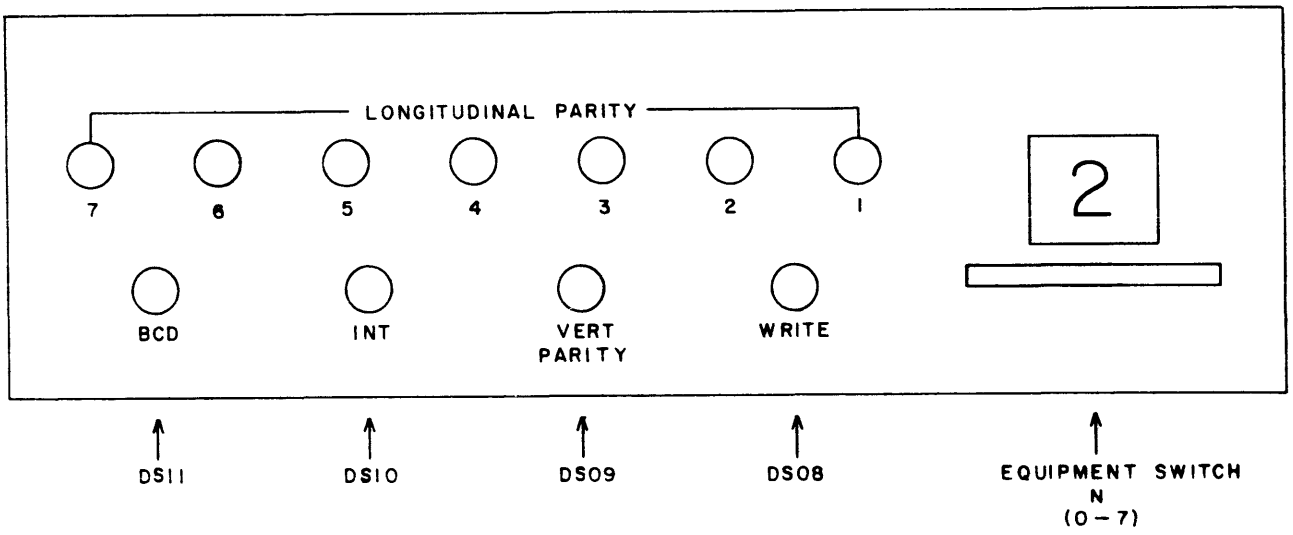


Figure 1-2 3228/3229 Control Panel

LONGITUDINAL PARITY

At the end of an operation involving longitudinal parity checking, none of the Longitudinal Parity indicators should be on. If one or more are on, it indicates a longitudinal parity error has occurred.

INTERRUPT (INT)

This indicators lights when an Interrupt occurs. This light is on until the Interrupt signal drops.

BCD

This indicator lights when BCD mode is selected or an End of File Mark is written on tape.

WRITE

The Write indicator is illuminated during Write and Write End of File Mark operations. The Write indicator remains on until the Write operation terminates.

VERTICAL PARITY

The Vertical Parity Error indicator lights if a vertical parity error occurs during an operation. This light is lit until a new record is begun.

LOGIC CABLING

Cables are attached to a cable connector panel located at the bottom rear of the 322X chassis. The panel is arranged as shown in Figure 1-3.

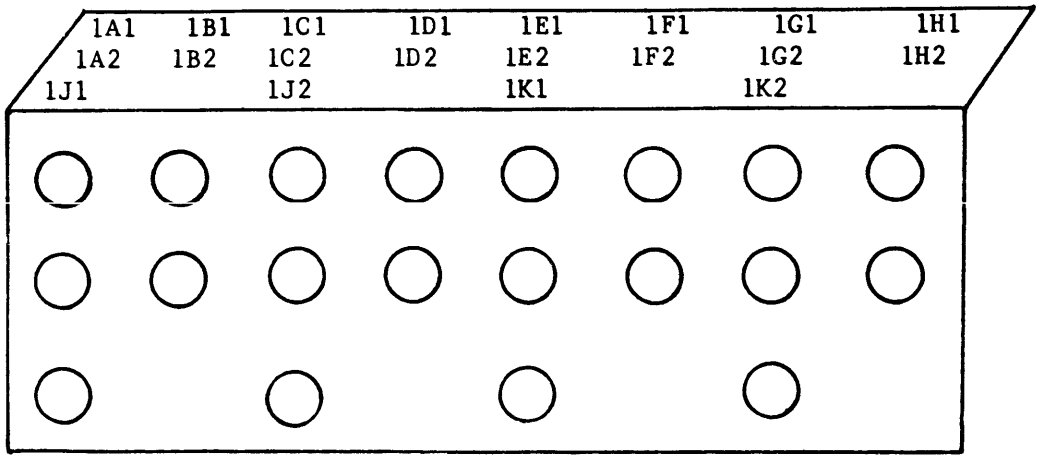
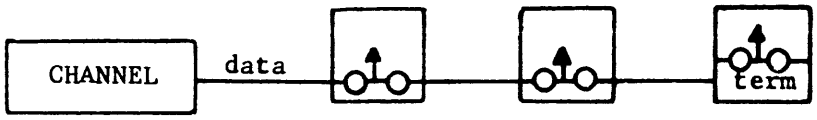


Figure 1-3

The bottom four connectors 1J1, 1J2, 1K1, and 1K2 are associated with the Data Channel. The cable carrying data and control signals are wired in parallel. Accordingly, a signal on any individual line within a cable is felt at all controllers cabled to the channel.

Data is brought into the controller through connector 1J1. Data continues to the next controller from connector 1J2. If this is the last controller on the channel a terminator must be attached to 1J2.



Control signals enter the controller through connector 1K1 and continue to the next controller or are terminated at connector 1K2.

The specific signal on the individual lines of the two cables are listed in table 1-1 for the Data I/O Cable and table 1-2 for the Control Cable.

An explanation of each signal in the Data I/O Cables is contained in table 1-3.

The top sixteen connectors are pairs, each pair being associated with one of the eight tape handlers possible to be cabled to the controller. Each transport has two cables, one attached to J208, the other attached to J209. Both connectors located on the right side of the logic chassis in the back of the handler. The two cables are specified: one as the Input Cable to the handler, the other as the Output Cable from the handler, though, in fact, signals travel in both directions in both cables.

The Output Cable from J208 on the transport is connected to the 1A1, 1B1, 1C1, etc. connector on the controller. See table 1-3.

The Input Cable from J209 on the transport is connected to the 1A2, 1B2, 1C2, etc. connector on the controller.

The specific signal on the individual lines of the two cables are listed in table 1-4 for the Output Cable and in table 1-5 for the Input Cable.

An explanation of each signal on these cables is contained in table 1-6.

TABLE 1-1. SIGNAL AND PIN ASSIGNMENTS

Data I/O Cable

(Mates a 322X Control and a 3206 or a 3681 Converter)

Pin (two used)	Signal
A1-2	Data Bit 00
A3-4	Data Bit 01
A5-6	Data Bit 02
A7-8	Data Bit 03
A9-10	Data Bit 04
B1-2	Data Bit 05
B3-4	Data Bit 06
B5-6	Data Bit 07
B7-8	Data Bit 08
B9-10	Data Bit 09
C1-2	Data Bit 10
C3-4	Data Bit 11
C5-6	Parity Bit
C7-8	Channel Busy
C9-10	Reverse Assembly
D1-2	Read
D3-4	Write
D5-6	Connect
D7-8	Function
D9-10	Data Signal
E1-2	Reply
E3-4	Reject
E5-6	End of Record
E7-8	Parity Error
E9-10	(Unused)
F1-2	
F3-4	Master Clear
F5-6	(Used Internally)
F7-8	(Used Internally)
F9-10	Termination Power
(Not in cable. See note).	

TABLE 1-2. SIGNAL AND PIN ASSIGNMENTS

Control I/O Cable

(Mates a 322X Control and a 3206)

Pin (two used)	Signal
A1-2	Status Bit 00 Ready
A3-4	Status Bit 01 R/W Control (and/or) Bus
A5-6	Status Bit 02 Density (1 = 556 BPI)
A7-8	Status Bit 03 File Mark
A9-10	Status Bit 04 Load Point
B1-2	Status Bit 05 End of Tape
B3-4	Status Bit 06 Write Enable
B5-6	Status Bit 07 Density (1 = 800 BPI)
B7-8	Status Bit 08 Lost Data
B9-10	Status Bit 09 Longitudinal Parity Error
C1-2	Status Bit 10 Vertical Parity Error
C3-4	Status Bit 11 Tape Handler Reserved for Other Control (Unused)
C5-6	Computer Running (Unused)
C7-8	Negate BCD Conversion (1604 Mode)
C9-10	Suppress Assembly/Disassembly
D1-2	Interrupt Line 0
D3-4	Interrupt Line 1
D5-6	Interrupt Line 2
D7-8	Interrupt Line 3
D9-10	Interrupt Line 4
E1-2	Interrupt Line 5
E3-4	Interrupt Line 6
E5-6	Interrupt Line 7
E7-8	(Unused)
E9-10	(Unused)
F1-2	(Unused)
F3-4	(Unused)
F5-6	(Unused)
F7-8	(Unused)
F9-10	Termination Power
(Not in cable. See note).	

NOTE: The 29-pair cables terminate in 61-pin connectors. Pins F9-10 of each connector are used to provide power to the terminal assembly and do not connect to lines in the I/O cable.

TABLE 1-3. DATA CHANNEL SIGNALS

**Data Signal	Static 1 signal received by the 322X during both Read and Write operations. Signal drops when 322X returns a Reply to the 3206. 1) In a Read operation, Data Signal indicates that 322X may begin reading information and transmitting it to the data channel. 2) In a Write operation, Data Signal indicates that information is available on the data lines and the Write operation may begin.
***Reply	Static 1 signal produced by the 322X in response to a Connect, Function, or Data Signal. Signal drops when Connect, Function, or Data Signal drops. 1) If connection can be made when Connect signal is received, the 322X connects the desired tape unit and returns a Reply. 2) If a specified function can be performed when the Function signal is received, the 322X executes the function and returns a Reply. 3) In a Read operation, the 322X sends a Reply as soon as it has placed a 12-bit word on the data lines in response to the Data Signal. In a Write operation, the 322X sends a Reply as soon as it samples the data lines in response to the Data Signal.
***Reject	Static 1 signal produced by the 322X in response to a Connect or Function signal, if the connection cannot be made or the Function cannot be performed at the time that the 322X receives the respective signal.
***End of Record	Static 1 signal produced by the 322X during a Read operation. This signal is produced in response to the Data Signal, if the end of the specified block of data has been reached.
*Data Bits	The 12 lines which carry data are bidirectional, and perform as follows: 1) In a Read (input) operation, data is read from tape in 6-bit frames, and assembled into 12-bit bytes. These 12-bit bytes are sent to the 3206 data channel. 2) In a Write (output operation) data is received from

TABLE 1-3. DATA CHANNEL SIGNALS (Cont'd)

	the 3206 in 12-bit bytes. The 322X disassembles these 12-bit bytes into 6-bit frames and writes them on tape. 3) The Connect code and Function code are received by the 322X via the 12 data lines.
**Channel Busy	Static 1 signal which indicates the data channel is performing a Read/Write operation.
*Parity Bit	A parity bit accompanies each 12 bits of data transmitted between the 322X and the 3206 data channel. Odd parity is used, so the total number of 1s transmitted is always an odd number.
**Read	Static 1 signal received by the 322X from the 3206 during a Read operation.
**Write	Static 1 signal received by the 322X from the 3206 during a Write operation.
**Connect	Static 1 signal received by the 322X when a 12-bit Connect code is available on data lines. The signal drops when the 322X returns a Reply or Reject.
**Function	Static 1 signal received by 322X when a 12-bit Function code is available on data lines. The signal drops when the 322X returns a Reply or Reject.
***Parity Error	Static 1 signal produced if the total number of 1s in the 12 data bits plus the parity bit is not an odd number. This signal will be returned to the 3206 only if the 322X is connected to some tape handler.
**Master Clear	A 1 signal from the computer which returns channel and 322X to zero initial conditions and clears all connections to tape handlers.
***Reverse Assembly	This signal directs the data channel to reverse the byte positions while receiving a computer word from the 322X.
***Status Bits	The 322X uses eleven status lines to indicate its condition.
***Negate BCD Conversion	Static 1 received by the 322X. This signal disables the automatic internal-to-external BCD conversion during a Write operation in BCD mode. It also disables the automatic external-to-internal BCD conversion during a Read operation in BCD mose. (Used only when the 322X is used by a 3400 or 3600 computer.)

TABLE 1-3. DATA CHANNEL SIGNALS (Cont'd)

**Suppress Assembly/ Disassembly	Static 1 signal received by the 322X. This signal disables the assembly/disassembly in the 322X. Each word received by the 322X from the data channel writes one 6-bit frame on the tape (lower 6 bits of the data channel word). During Read, the upper 6 bits of the data channel word are all zeros.
***Interrupt Lines	A 1 signal on an Interrupt line indicates a tape handler connected to the 322X has reached a predetermined condition. Each 322X has an Interrupt line corresponding to the setting of the Equipment Number switch.

*Bidirectional signal flow
**Signal flow from the 3206 to the 322X
***Signal flow from the 322X to the 3206

TABLE 1-4. OUTPUT CABLE FROM 322X TO 60X

(Between J208 on transport and 1A1, 1B1, 1C1, etc. on the controller)

NOTE

Terms in parentheses give signal nomenclature used in 60X manuals and specifications.

Pin	Signal
*A	2^0 Write
*B	2^1 Write
*C	2^2 Write
*D	2^3 Write
*E	2^4 Write
*F	2^5 Write
*H	Parity Write
*J	Write Sprocket
**K	Address 6
**L	Address 7
*M	Forward
*N	Reverse
*P	Search End of File (Stop On File Mark)
*R	Set 556 BPI Density (Select Hi Density)
*S	Set 200 BPI Density (Select Lo Density)
*T	Write (Write Select)
*U	Read (Read Start)
*V	MC (Master Clear)
*W	Rewind Unload
*X	Rewind
**Y	Address 5
*Z	Turn On Connect Light (Unit Select Light #1)
*a	Turn On Reserve Light (Unit Select Light #2)
b	Ground

*From 322X to 60X
**From 60X to 322X

TABLE 1-5. INPUT CABLE TO 322X FROM 60X

(Between J209 on transport and 1A2, 1B2, 1C2, etc. on the controller)

NOTE

Terms in parentheses give signal nomenclature used in 60X manuals and specifications.

Pin	Signal
**A	2^0 Read
**B	2^1 Read
**C	2^2 Read
**D	2^3 Read
**E	2^4 Read
**F	2^5 Read
**H	Parity Read
**J	Read Sprocket
**K	Write Enable (Write Ready)
**L	Address 4
**M	End of Record (End of Operation)
**N	File Mark
**P	Address 0
**R	Address 1
**S	Address 2
**T	Address 3
**U	Busy
**V	Density (1 = 556 BPI)
**W	Load Point
**X	End of Tape
**Y	Ready
Z	Density (1 = 800 BPI)
a	Not Used
b	Ground

*From 322X to 60X
**From 60X to 322X

TABLE 1-6. SIGNAL DEFINITIONS

Signal Definitions:	Output cable from 322X to 60X
7 Write Information	These seven lines carry information from the Write register in the 322X control. Six lines carry data, one line carries a parity bit.
Write Sprocket	A 4 (6) usec pulse which gates the information on the seven data lines into the 60X Write circuitry.
Address 5, 6, and 7	These three address lines (eight total) correspond to a setting on the 60X Unit Select switch. A static 1 signal appears on the address line corresponding to the Unit Select setting. When the switch is rotated, all address lines have a momentary 0 output.
Forward	A 1 signal which initiates forward tape motion at 150/75 ips.
Reverse	A 1 signal which initiates reverse tape motion at 150/75 ips.
Search End of File	A 1 signal which inhibits stop circuits until an End of File character is detected.
Set 556 BPI Density	A 1 signal which selects 556 BPI density Operating mode (556 bits per inch).
Set 200 BPI Density	A 1 signal which selects 200 BPI density Operating mode (200 bits per inch).
Write	A 1 signal which enables Write and Read verify operations.
Read	A 1 signal which enables a Read operation.
MC	A 1 signal which establishes initial operating conditions by clearing all Select conditions. Immediately stops tape motion.
Rewind Unload	A 1 signal which intiiates tape motion in a reverse direction at 350 ips to a Tape Unload condition (all tape on supply reel) and Stop.
Rewind	A 1 signal which initiates tape motion at 350 ips to the nearest Load Point marker.

TABLE 1-6. SIGNAL DEFINITIONS

Signal Definitions: Output cable to 322X from 60X	
Turn On Connect Light	A 1 signal which turns on Unit Select light #1. This light indicates a particular tape handler is connected to a data channel.
Turn On Reserve Light	A 1 signal which turns on Unit Select light #2. This light indicates a particular tape handler is reserved by a data channel. (Not used when connected to 3206.)
Ground	
7 Read Information	These seven lines carry information from the 60X to the 322X. Six lines carry data, one line carries a parity bit.
Read Sprocket	A 1 pulse which signals the 322X to sample the 7 bits of Read information from the 60X.
Write Enable	A 1 signal which indicates that the file protection ring is in and tape has been loaded. Write and Read Verify operations may now be performed.
Address 0,1,2,3,4	See Address 5, 6, and 7.
End of Record	A 1 signal which indicates an End of Record check character, File Mark, or Load Point has been detected.
File Mark	A 1 signal which indicates a File Mark has been detected.
Busy	A 1 signal which indicates that tape is in motion. Signal drops 5 ms after tape motion stops.
Density (556 BPI)	A 1 signal which indicates that 556 BPI density is selected. If this signal is absent, 200 or 800 BPI density is selected.
Load Point	A 1 signal which indicates tape is at Load Point.
End of Tape	A 1 signal which indicates the End of Tape marker has been sensed.
Ready	A 1 signal which indicates the 60X is under 322X control and is prepared for the next operation. The tape handler is always ready when its Ready indicator is illuminated. The tape handler is Not Ready when power is off or when the tape handler is being manipulated from its control panel.
Density (800 BPI)	A 1 signal which indicates 800 BPI density is selected. If this signal is absent, 200 BPI or 556 BPI density is selected.
Ground	

CHAPTER II

FUNCTIONAL DESCRIPTION

CHAPTER II

FUNCTIONAL DESCRIPTION

CLEAR CONTROLLER

Prior to initial use of the tape controller, the system should be cleared. There are five possible ways of clearing the controller:

1. Clear Channel (100 usec) 77.51 IOCL

   This instruction clears all activity in the data channel and clears the tape handler connection.

2. Clear (2 usec) Function 0005

   This instruction clears the tape handler connection, but the controller remains "connected" in the sense that Status signals are still available for the data channel.

3. Release Function 0000

   This instruction clears only the connection for a connected tape handler (not relevant in a 3228/3229 - used for compatibility).

NOTE

> The latter two Function instructions (Clear and Release) can only be used after the controller is connected to a tape handler.

4. Power On MC

   When power is applied to the 3228/29, all tape handlers connected are cleared. Logic in the controller is also cleared, and no Status signals are available to the data channel.

5. External MC (from Console)

   This clears all tape handlers connected and clears the logic in the controller. No Status signals are available to the data channel after executing this operation.

NOTE

> Both Master Clear operations place the 3228/29 in binary format.

COMPUTER-TAPE OPERATIONS

Computer-Tape handler operations are selected by computer External Function (EF) signals. These control the following functions:

1. Connect (code and signal)
   - Data Channel
   - Controller
   - Tape Handler

2. Status (on status lines after connect)

3. Function-Format (code and signal)
   - Format
     - Release
     - Parity Mode
     - Density
     - Clear
     - Reverse Read - Release Same (604/607 only)
   - Motion Directives
     - Rewind
     - Rewind Unload
     - Backspace
     - Search Forward to File Mark
     - Search Backward to File Mark
     - Write File Mark
     - Skip Bad Spot
   - Interrupt
     - Ready and Not Busy - Release Same
     - End of Operation - Release Same
     - Abnormal End of Operation - Release Same

4. Information Transfer
   - Write (signals)
   - Read (signals)

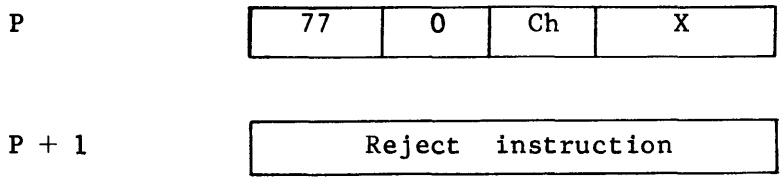
5. Assembly/Disassembly or Character (signal)

CONNECT

The computer sends a 12-bit Connect code over the data channel to the tape controller. A manual Equipment Selection switch on the tape controller locks out all Connect codes except the ones having the correct bit combinations in bits 9, 10, and 11. These bits must match the switch setting on the 3228/29 or the processor will not make the connection. Bits 0, 1, and 2 may have octal values of 0 - 7. These bits determine with which tape handlers the 3228/29 will communicate. Bits 3, 4, 5, 6, 7, and 8 are not used. If none of the controllers or any other equipments physically connected to the processor via data channels have the proper switch setting,

or a parity error occurs in the Connect code, an Internal Reject is generated by the computer.

PROGRAM CONSIDERATIONS



Ch is a number 0-7 for 3200
X is the 12-bit Connect Code

Bits 9, 10 and 11 designate one of eight possible controllers which could be attached to the designate channel.

Bits 3 through 8 are not used.

Bits 0, 1 and 2 designate one of eight possible tape transports which could be attached to the controller.

The Function Code 77.0 places a Connect Signal, the 12-bit Connect Code, and a Transmission Parity Bit on the designated channel. The Connect signal and the code is felt by all controllers on the channel. It will cause the desired equipment to connect for further operation and all others to disconnect.

NOTE 1

If the Channel is Busy from a previously initiated operation, the next instruction will be read at P + 1. (the reject instruction)

If a Reply is returned, the next instruction will be read at P +2.

If a Reject is returned, the next instruction will be read at P + 1.

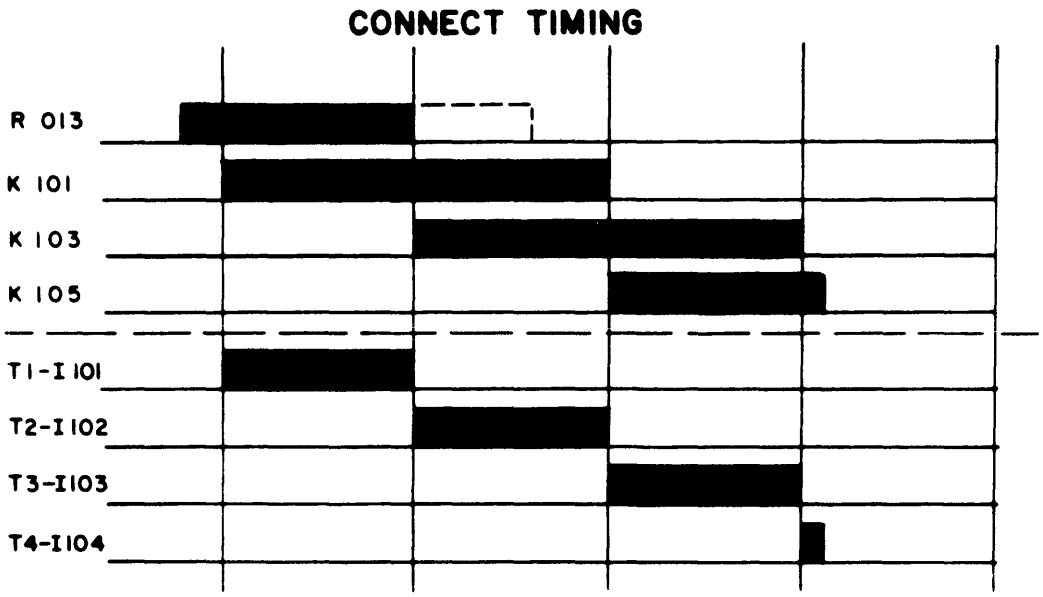
If neither a Reply nor Reject is returned within 100 usec, the next instruction will be read at P + 1 as the result of an internally generated Reject.

NOTE 2

The following text page references are to the 3228/3229 Magnetic Tape Controller diagrams. Use the Connect Operation Flow Diagram (Figure 22-1) when reading this topic..

INITIATE TIMING CHAIN

The Connect Signal arrives at R013 (page 3-1) and initiates the Connect Timing Chain (page 2). The progress of the Timing Chain is translated into 4 times to clock the Connect operation.



CHECK TRANSMISSION PARITY

Upon receipt of the Connect Signal, the controller checks the 12-bit Connect Code and associated parity bit within the Parity Checker logic (page 3-1) for possible transmission parity errors.

1. Parity Strobe will occur for every transmission on the Data Lines. In this case, the Strobe occurs as a result of the Connect Signal.

2. Check parity of data bits. If the data bits total an even number of bits through the Parity Checker the term P076 goes to a logical "1".

(p.3-1)

3. Parity Errors
   a. An even number of data bits and no parity bit.

      P076 · A012 · P079

   b. An odd number of data bits and a parity bit.

      P076 to P077 · R012 · P079

   c. If a parity error exists, set K116/117, XMSN Parity Error FF. (page 3-1) Parity Error is not sent to the channel since the Controller is not yet connected; however, the equipment number switch will be illuminated by a red lamp through D081, indicating a Parity Error.

CHECK EQUIPMENT NUMBER

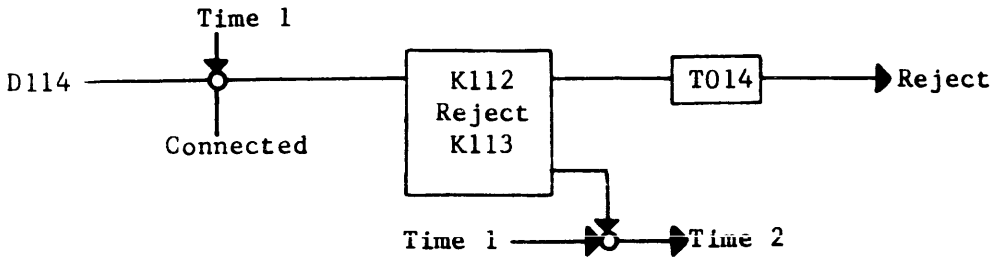
Bits 9, 10 and 11 of the Connect Code designate the specific equipment on the channel with which further operation is required. These bits are fed through the contacts of the Equipment Number Switch.

1. Switch and Code agree - No Parity Error
   All zeros fed into I110 to "1" (p.3-3)
2. Switch and Code do not agree or Parity Error or both
   At least one "1" into I110 to I111 to "1"
   At time 1 the Controller Connect FF K110/111 (page 3-3) will be cleared and the timing chain will be disabled preventing time 2 from occurring. No Reject or other reply occurs and 100 usec later an Internal Reject causes the Connect Signal and Code to be removed from the lines.

READ/WRITE CONTROL ACTIVE OR TAPE MOVING

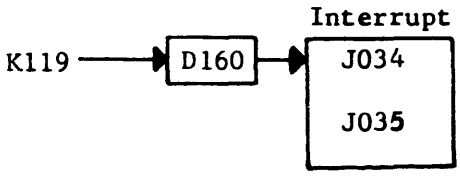
An attempt to connect during the time a previously initiated Read, Write or Function is in progress could destroy a desired action since signal interchange between transport and channel would be eliminated or interrupted.

If such action is in progress the term D114 is a logical "1" enabling the AND gate into K112/113 Reject FF (page 3-3). The result is that time 2 on the Timing Chain cannot occur and the Reject Signal is returned to the channel.

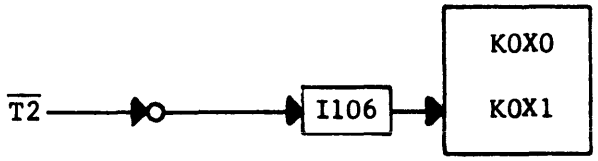


The Reject Signal returned to the channel causes the Connect Signal and Code to drop.

The Connect FF, K118/119, is also set at time 1 to disable the possibility of an Abnormal End of Operation Interrupt during the connect. This could be due to the loss of the Ready Signal returned from the transport.



At time 2, the controller Connect FF, K110/111, will set which provides the enable needed to choose the appropriate Unit Select FF (1 of 8, Page 3-5). In anticipation of the selection, all eight of the Unit Select FFs are cleared.

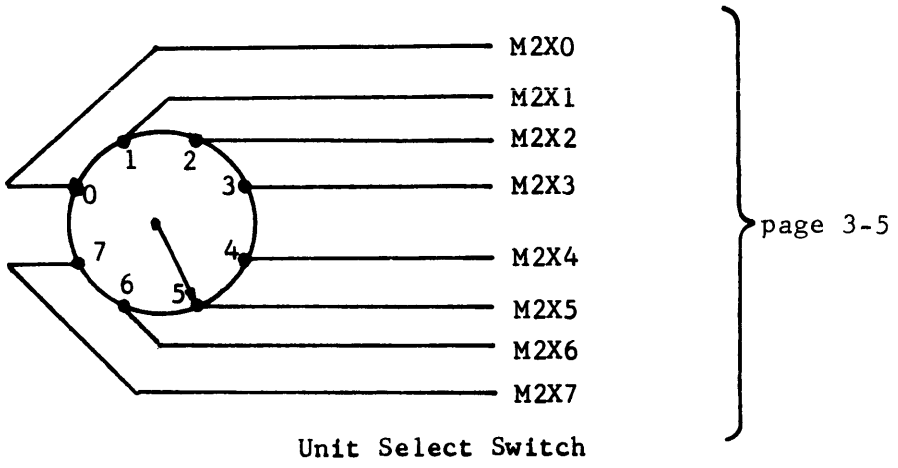


(p.3-5)

As the controller Connect FF sets, the Equipment Number Switch is illuminated by a white lamp through D080, indicating controller connected.

CODE AND TRANSPORT UNIT SELECT SWITCH COMPARISON

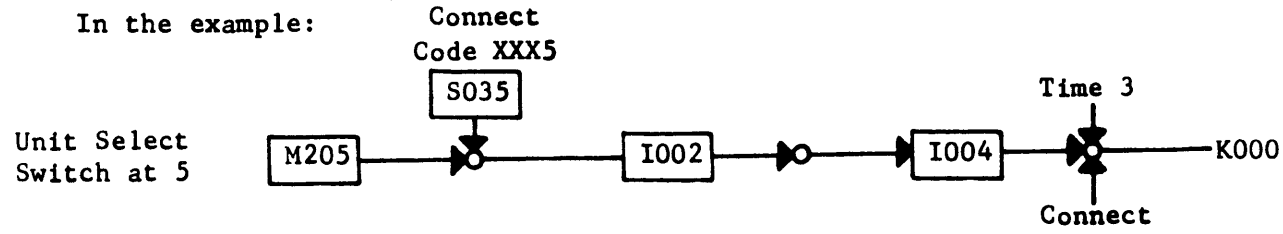
Each of the eight transports cabled to the controller is returning an indication of the position of its 8-position Unit Selector Switch. For example, a transport cabled to Connector A of the controller has the switch displaying a 5; then, M205 (page 3-5) outputs a logical "1". Seven other M2XX terms, each associated with a different transport, should be outputting a logical "1". Ideally, no other M2X5 term should be a one, and no two transports should display the same number.



The lower 3 bits--bits 0, 1, and 2--from the Connect Code have been translated through the Tape Unit Select Inverter (page 3-3) one of which will have a logical "1" output. In the preceding example, for a correct comparison, S035 should be a "1" and be fed to eight AND gates, one at the output of every M2X5 card (page 3-5) where the actual comparison should occur.

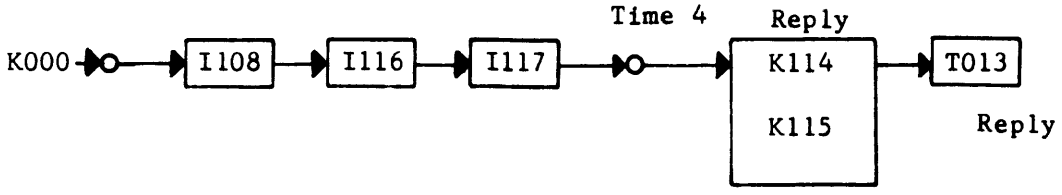
Code and Unit Select Switch Agree

Set the Unit Select FF to connect the transport at time 3.



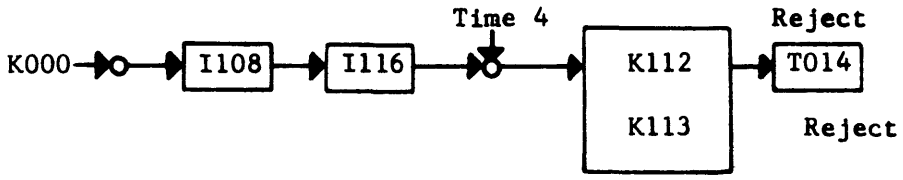
Set K114/115 (Reply FF) and return a Reply Signal to the channel.

Set K114/115 Reply FF and return a Reply Signal to the channel.



Code and Unit Select Switch do not Agree

If for some reason no transport is returning a signal which will compare, no Unit Select FF will be set. All AND gates into terms I109 and I108 will be made. Inverter I116 outputs a logical "1", the Reject FF is set at time 4, and the Reject Signal will be sent to the channel.



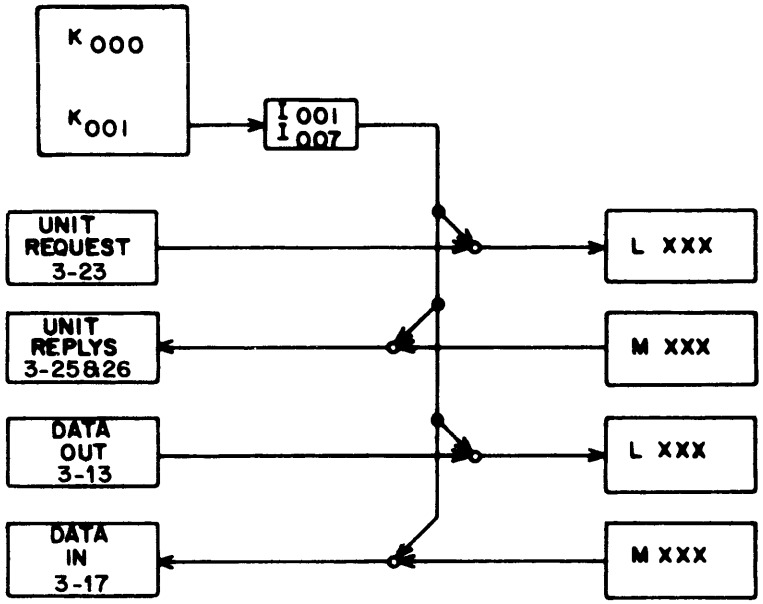
At time 4, K118/119 (Connect FF, p. 3-3) is cleared. The conditions for an Abnormal End of Operation Interrupt no longer exist.

COMPLETION

A Reply or Reject Signal returned to the channel causes the Connect Signal to drop which clears either the Reply or Reject FF and drops the Reject or Reply Signal.

(p. 3-1)

Following a Reply, at this time, the controller Connect FF (K110/111 page 3-3) is set. The Slave Inverters fed by the clear output provide enables for Read, Write, and Function operations. One of the Unit Select FFs (page 3-5) is set through its slave inverters, enables the flow of data and signals between the channel and the connected tape transport.



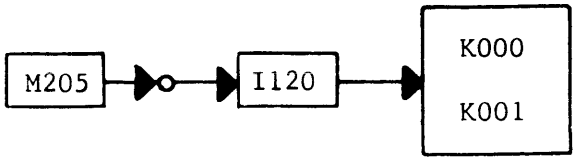
The Status lines (p. 3-1) are also enabled back to the channel permitting a sense or Copy Status instruction to be executed.

Once the connect is complete, the Unit Select FF will remain set until a Function, another Connect, or an Accident clears the FF.

Function - Clear (0005) or Release
Connected Unit (0000) will clear all Unit Select FFs through I106 (page 3-3).

Connect - Unit Select FFs cleared through I106 at T2 during a connect.

Accident - Moving the Unit Select Switch on the connected tape transport will cause all inputs to the I12X terms to Output zeros for an instant, clearing the Unit Select FF.



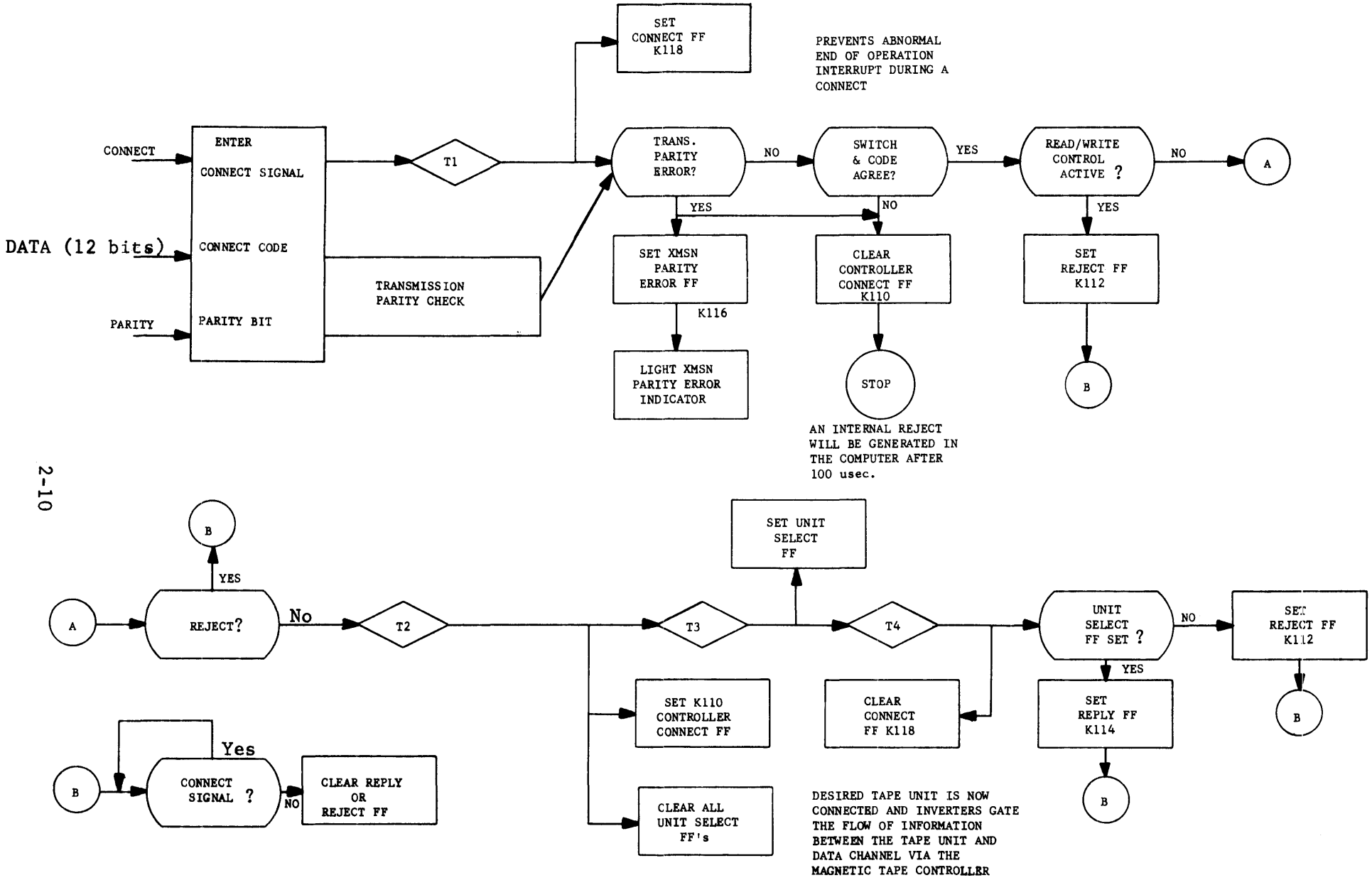


Figure 2-1. Connect Operation

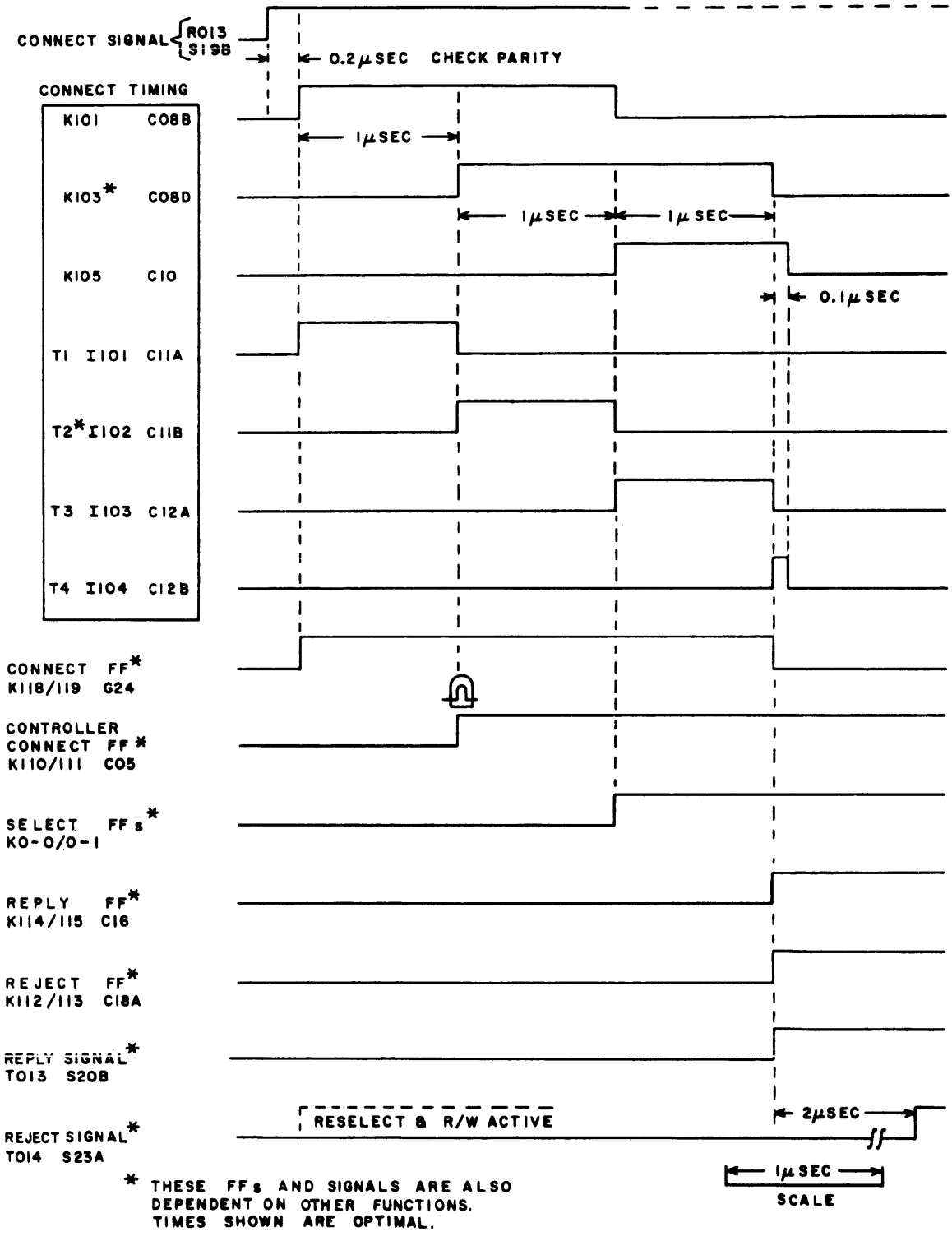


Figure 2-2. Connect Operation Timing

STATUS

After the desired tape handler has been connected it is usually necessary to check status before attempting further operations. The status is on line at all times while connected. Each controller has a distinctive meaning for each bit of the Status response. The meaning of the bits returned from the tape system are:

TABLE 2-1 - STATUS RESPONSE

XXX1	Ready	X1XX	Density (1 in bit 6 indicates 556 BPI) (0 in bit 6 and bit 7 indicates 200 BPI)
XXX2	Read/Write Control and/or Busy	X2XX	Density (800 BPI) 1 in bit 7
XXX4	Write Enable	X4XX	Lost Data
XX1X	File Mark	1XXX	End of Operation
XX2X	Load Point	2XXX	Transverse or Longitudinal Parity Error
XX4X	End of Tape		

A detailed explanation of the meaning of each response is as follows:

READY (XXX1)

A Ready indicator on the tape handler lights when it is in a Ready condition; i.e., power has been applied and the tape handler is in automatic mode. When in Automatic mode, the tape handler is controlled by the tape controller.

The Ready signal is not present when the tape handler is manually operated from its control panel.

READ/WRITE CONTROL (AND/OR) BUSY (XXX2)

This signal is present:

1. If the tape handler is Ready.
2. During and for 5 ms after any operation requiring tape motion (Read, Write, etc.).
3. Whenever the data channel begins executing or is executing a Read/Write instruction.

This signal will not be present if:

1. The tape handler is not Ready.
2. The channel begins executing or is executing a Read/Write instruction and:
   a. Lost Data has occurred in a previous operation and/or.
   b. Interrupt On Abnormal End of Operation has occurred in a previous operation and the Interrupt signal is still present.

WRITE ENABLE (XXX4)

This signal is present only when the file protection ring is on the tape reel. When this signal is absent, it is impossible to write on tape, although information may be read from the tape.

FILE MARK (XX1X)

This signal is present when the tape handler has searched for and located an End of File Mark. It is also present immediately after writing an End of File Mark. This signal drops when: (1) reading or writing begins on a new record or (2) a Backspace Search End of File Mark Forward. or Search End of File Mark Backward operation is initiated.

LOAD POINT (XX2X)

This signal is present when the tape is at Load Point. The signal drops when tape motion begins.

END OF TAPE (XX4X)

This signal is present when the End of Tape marker is detected. The signal drops when tape has been rewound past the End of Tape marker.

DENSITY (X1XX)

See table 2-1

DENSITY (X2XX)

See table 2-1

LOST DATA (X4XX)

This signal appears during a Write operation (Write signal present) if the tape controller is ready to accept information but the Data signal from the data channel is absent.

When the Lost Data signal appears during a Write operation, tape motion stops. Further Write operations are impossible until the Lost Data signal is cleared with a new Function or Connect code.

The Lost Data signal also appears during a Read operation (Read signal present) when the tape controller has data ready for output, but the Data signal from the Data channel is absent

If the Lost Data signal appears during a Read operation, reading continues until the end of the record. Further Read operations are impossible until the Lost Data signal is cleared with a new Function or Connect code. (Any legal Function code listed in the table will clear the Lost Data signal.)

The Lost Data signal is meaningless when the tape controller is attached to a 160/160-A via a 3681 adapter. However, this signal must be cleared if Read/Write operations are to continue.

END OF OPERATION (1XXX)

This signal indicates that an operation is completely finished.

PARITY ERROR (2XXX)

This signal indicates that a parity error has occurred during a Read/Write operation. This signal drops when reading begins on a new record. A Clear Channel instructiom External Master Clear, or a Power On Master Clear causes this signal to drop. The Parity Error signal may also appear when an End of File Mark is written or is read in Binary mode.

Any number of these responses may be active at the same time.

A program for status check could be:

```
1.  77 2 10100   EXS     Sense Status (Is Density 556?)
2.  01 0 00005   UJP     Yes - Jump to Address 5
3.  77 2 10000   COPY    No - Copy Status in A Register
4.  77 7 70000   UCS     Stop - on GO read Address 5
5.  Start next operation
```

In this program, as address 1 is read, bit 6 from the status line is being checked.

a. If the connected transport is in 556 BPI density, bit 6 will be on the status line, comparison occurs and the next instruction is read from address 2 which in turn, jumps to address 5 and a new operation can start.

b. If the controller is in a density other than 556 BPI-- for instance, 200 BPI-- bit 6 is a zero, comparison does not occur, and the

instruction from address 3 is read. Address 3 instruction causes the contents of the status lines to be placed into the lower 12 bits of the A register. Next, address 4 is read, which causes the machine to stop and display the status.

The density switch on the transport could now be conditioned manually.

FUNCTION

The computer sends a 12-bit Function Code, accompanied by a Function Signal. over the Data Channel. Only a controller which was previously connected will respond to the signal.

The Function Code in the form XXCD conditions the controller or transport for an operation.

C = 0 or 4---selects tape format for a read or write operation
C = 1 --------causes tape motion or index positioning
C = 2 --------requests Interrupts when specified conditions occur

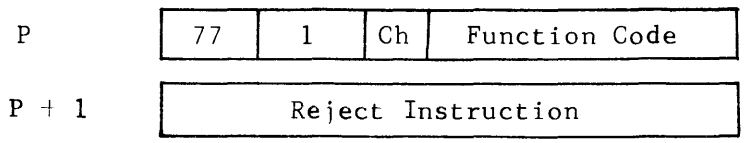
Those functions which select format are:

FORMAT

Release	0000	Clear	0005
Binary	0001	Density (800 BPI)	0006
Coded	0002	Set Reverse Read	0041
Density (556 BPI)	0003	Clear Reverse Read	0040
Density (200 BPI)	0004		

and will be used to prepare the system for the operation to be performed next.

PROGRAM CONSIDERATION



Ch is a channel designation and will be a digit between 0 and 7 for 3200 or 0 and 3 for 3100 computers.

Function Codes are four digits which indicate: 1) the desire to clear the controller 2) the density at which to read or write or 3) the parity of the frame to be read or written.

The Code 77.1 causes a Function Signal to be placed on the channel along with the 12-bit Function Code and a Transmission Parity Bit. The parity bit is such as to cause the total to be an odd number of "1" bits.

If a Reply is received within 100 usec, the next computer instruction will be read from location P+2.

If no Reply is received within this time a Reject occurs and the next instruction is from location P+1.

Internal Rejects occur at the end of 100 usec for the following reasons:

1. No Connect on the channel,
2. Equipment not ready, or busy in another operation.

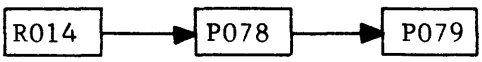
The instruction at P+1 will be read immediately if the instruction read at P calls for action on a busy channel, or is an Illegal Code (such as 3X).

NOTE

The following text page references are to the 3228/3229 Magnetic Tape Controller diagrams. Use the Function Flow Diagrams when reading this topic.

The Function signal (R014, (page 3-1) the Function Code (R001-R011, page 3-1) and the Parity bit (R012) enter the controller from the Data Channel. A Transmission Parity Check is made on the Function Code causing the XMSN Parity Error FF (K116/117) to set if Transmission Parity is in error.

The Function signal generates the Parity Strobe.



A transmission Parity Error indication will be returned for the connected equipment through T017 and the equipment number switch will turn red via D081, if the XMSN Parity Error FF sets.

CONTROLLER CONNECTED (K011)

The Function Signal (R014) occurs in each controller on the channel. In the 322X, the check is made at the AND gate into the 0.2 usec delay, Y050 (page 3-7).

If this AND gate is broken the Function cannot proceed. If no other controller can accept the signal, an internal reject occurs in 100 usec.

If the controller is connected, the AND gate will be made and the signal, delayed, 0.2 usec, will proceed.

TRANSMISSION PARITY ERROR (K117)

A Transmission Parity Error indicates that the entering Function Code is invalid. The presence of such an error is detected as an OR input to inverter I131 (page 3-7).

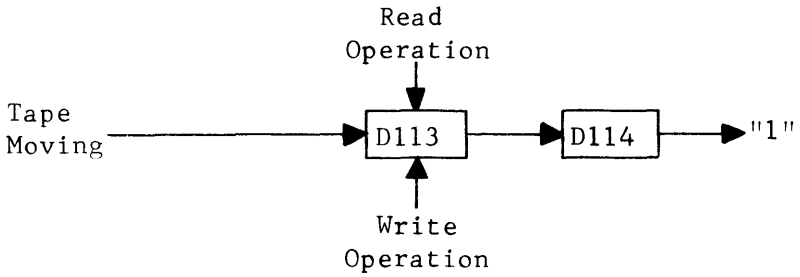
The set output of the XMSN Parity Error FF, if a logical "1", indicates the error exists and will stop the Function from proceeding. Since no Reply returns within 100 usec, an Internal Reject occurs.

If such an error does not exist, the signal proceeds.

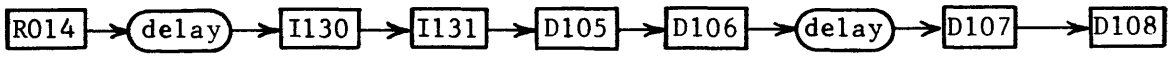
READ/WRITE CONTROL ACTIVE (D114)

Clearing, changing parity or density, etc., when some previously initiated operation is in progress, will negate or destroy a desirable operation and such a Function operation must not be permitted.

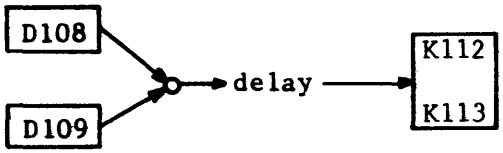
If a Read or Write operation is in progress, D114 (page 3-7) will be a logical "1", preventing the selection of any 1X flip-flop and the translation of 0X and 4X codes. This holds D109's output at a logical "1". D109 will also be a logical "1" if, during a 1X instruction, the tape handler is busy or not ready.



The Function signal will proceed on this path:



As the term, D108, outputs a logical "1", a Reject signal will occur if it ANDs with D109.

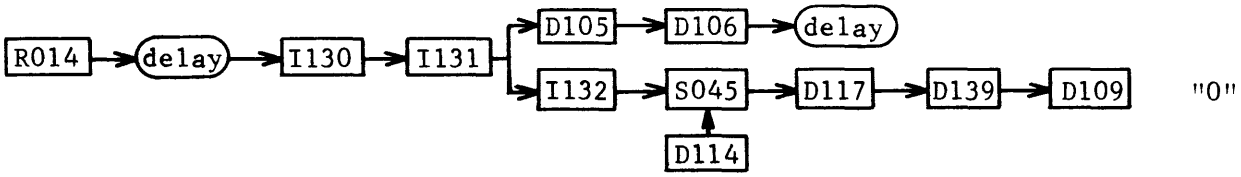


Reject (page 3-3)

Illegal Codes, such as 3X or 5X, also cause a reject, since they cannot be translated and D109 is held at a logical "1".

TRANSLATE FUNCTION CODE

If Read/Write Active D114 is a "0" indicating no operation in progress, this allow a translation of Function Code causing D109 to be a zero when D108 became a logical "1".



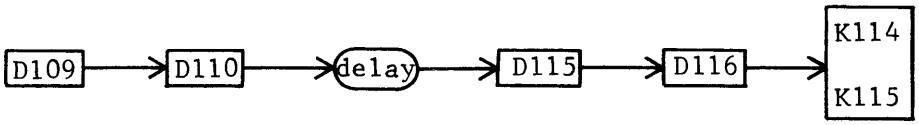
For the Format Functions 01 or 02 S045 and S040, translate bits 3, 4, and 5 only. Bits 0, 1 and 2 are translated by S010 thru S016 (page 3-3).

CONDITION THE FUNCTION SELECT FF

The combination of translator inverters, will set or clear the Function Select FF where the AND gate input is made.

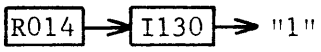
REPLY FOR FUNCTION SATISFIED WITHIN THE CONTROLLER

The Select Function FF is conditioned as the translation of the code occurs. Reject was denied when D109 went to zero before D108 became a "1". This is the path for a Reply to be returned to the channel.

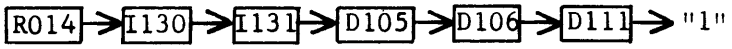


As K114/115 Reply FF sets, the transmitter, T013 (p. 3-1), sends a Reply Signal to the Channel.

The Reply or the Reject signal causes the function code and the function signal to drop, clearing either the Reply or Reject FF, as required.



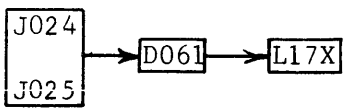
All functions are cleared and held clear by the absence of the Function signal,



with the exception of Format (J020/021) and Backward (J038/039) which retain a condition for the controller.

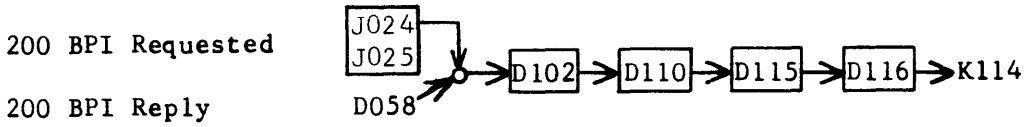
REPLY FOR DENSITY SELECTION FUNCTIONS - SATISFIED IN THE TRANSPORT

As in the case of functions satisfied within the controller, D109 goes to zero, before D108 becomes "1" to prevent Reject. In the previous case D109 going to zero passed straight through to produce the Reply. In this case D102 is "1" stopping the progress until a reply returns. Normally D102 is zero because both J022 and J024 Density Select FFs are clear. With one or both Density Select FFs set this AND gate into D102 is broken, as are all others. The Density FF being set places a Density Change Request Signal (p. 3-23) on-line to the transport.



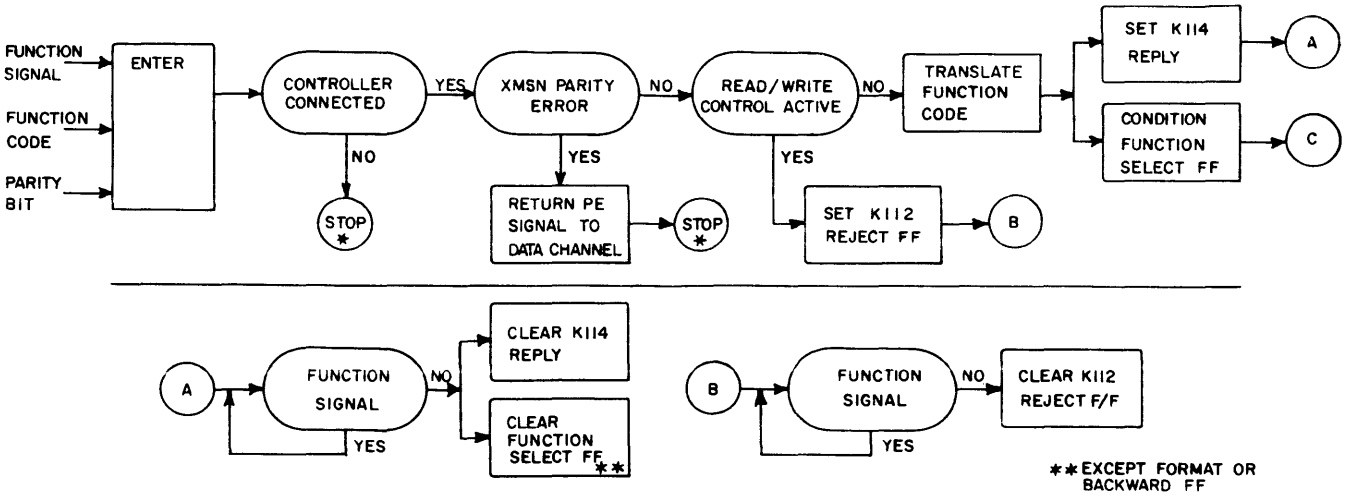
In the transport, two Select Density FFs are conditioned to match this request. The condition of the FFs are used in the transport to control the transfer rate of the Read Gate Circuit when tape is being read. The connected transport holds a constant Reply (p. 3-27) to the controller as to the density of tape it is prepared to handle.

As the Reply signal changes to match the requested density selected, one of three AND gates into D102 is made and the term goes to zero, allowing the reply to be generated when the Reply FF (K114) sets.



The Reply signal, when K114/115 sets, has the same result as was seen in the preceding section; that is, the Function signal drops, clearing the Reply FF.

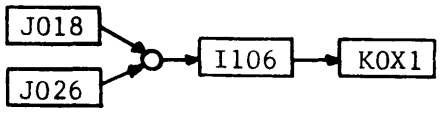
OX AND 4X FUNCTIONS



C (indicates flow chart progresses to these codes)

0005 Clear - This Function clears the connected tape transport, but the controller remains connected in the sense that status is still available to the channel.

0000 Release - This Function performs the same action as 0005 Clear, breaking the same AND gate into inverter I106 (page 3-3) but is not relevant to the 322X. The Function Code is included for compatibility of codes for other tape controllers.



When either of the above Function Select FFs are set, the Clear Unit Connect FFs (term I106) clears all eight Unit Select FFs (page 3-5).

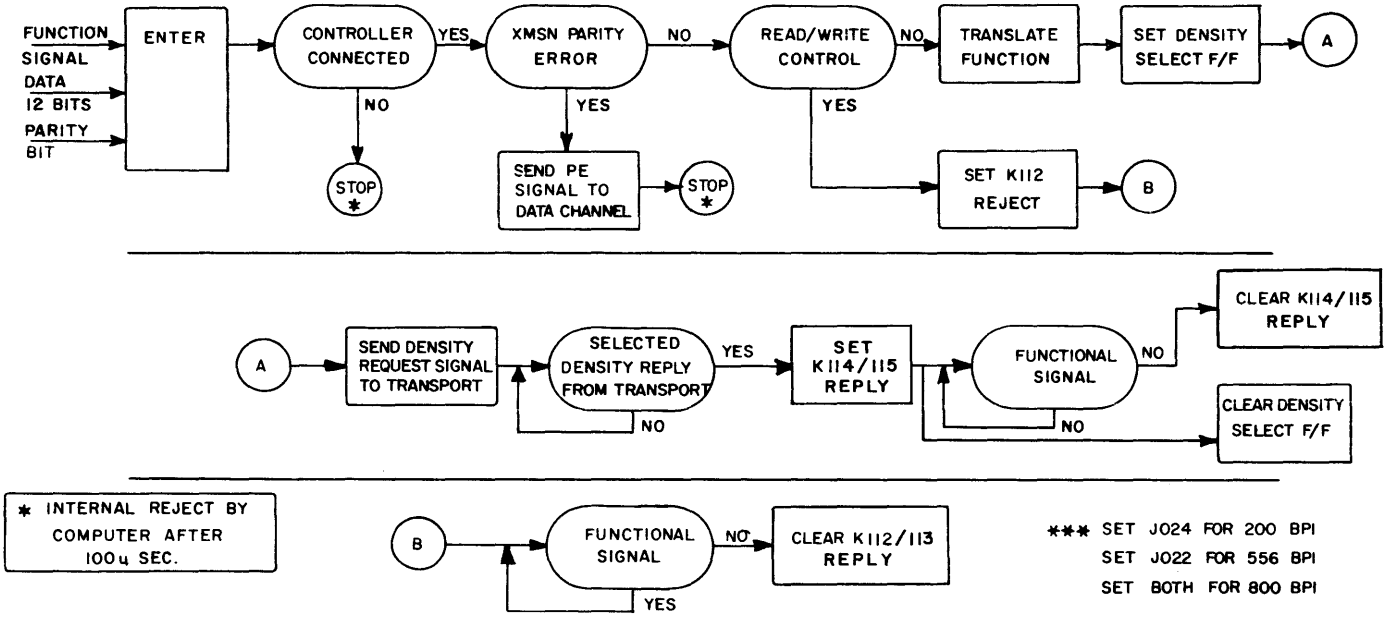
0001 Binary and 0002 BCD - These Functions are used to set or clear the Format Select FF (J020/021), which conditions the Write Parity Generator (p. 9). If J020/021 is set, the Slave Inverter (D130, page 3-7), outputs a logical "1". This lights the BCD Indicator on the control panel and conditions the seventh bit of the frame to write an even number of bits.

If J020/021 is Clear, the Slave Inverter (D129) outputs a logical "1". This conditions the seventh bit of the frame to write an odd number of bits

The terms D129 and D130 also condition the Parity Checker (p. 3-1) to check either odd or even parity

0041 Reverse and 0040 Clear Reverse - These Functions are used to set or clear the Backward FF (J038/039). When J038/039 is set, tape moves in reverse and during a Read, a signal is returned to the channel indicating Reverse Read. If a backspace is initiated, tape will move forward rather than its normal reverse. When J038/039 is clear, the controller operates in the normal manner. A Write operation is not affected by the condition of this FF, and all writing is in the forward direction only.

FUNCTION TO CHANGE DENSITY

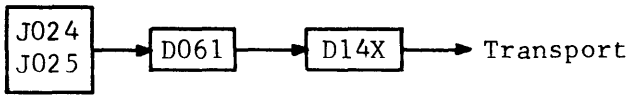


0003 556 BPI
0004 200 BPI
0006 800 BPI

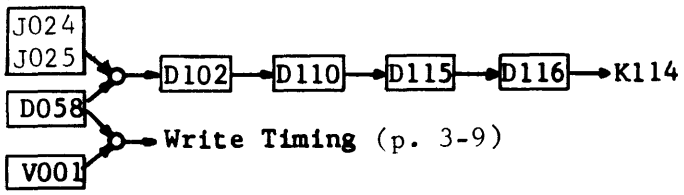
These codes are used to change frequency of the Write oscillator in the controller and the frequency of the Read Gate Circuit in the 60X Tape Transport. The density is determined by the condition of two FFs in the transport.

A signal is generated in the controller as a result of the Function Code, setting one (or both) of the Density Select FFs in the controller and thereby placing a signal on the Unit Request Lines to the connected transport.

Example: Set J024/025 Density 200 B.P.T.



The signal to the transport conditions the Density FFs in the transport. The condition of these FFs are constantly on-line as replies to the controller (p. 3-7). When the Density Reply from the transport, matches the density, request, a reply is sent to the Channel.



The Density Reply from the transport will enable one of three oscillators which control the frequency at which frames are written. The oscillator control the Write Timing Chain.

FUNCTION OPERATION

This section is presented using only simplified logic drawings and flow charts. More detailed information may be found in the Diagram Manual.

FORMAT FUNCTION	FIGURE	FLOW CHART FIGURE	DIAGRAM PAGE
Parity Mode	2-6	2-3	3-7, 11, 19
Clear	2-7	2-4	3-3, 7
Release	2-7	2-5	3-3, 7
Density	2-11	2-8, 9, 10	3-7, 9, 15, 23, 27
Reverse Read	2-14	2-12, 13	3-7, 15, 23

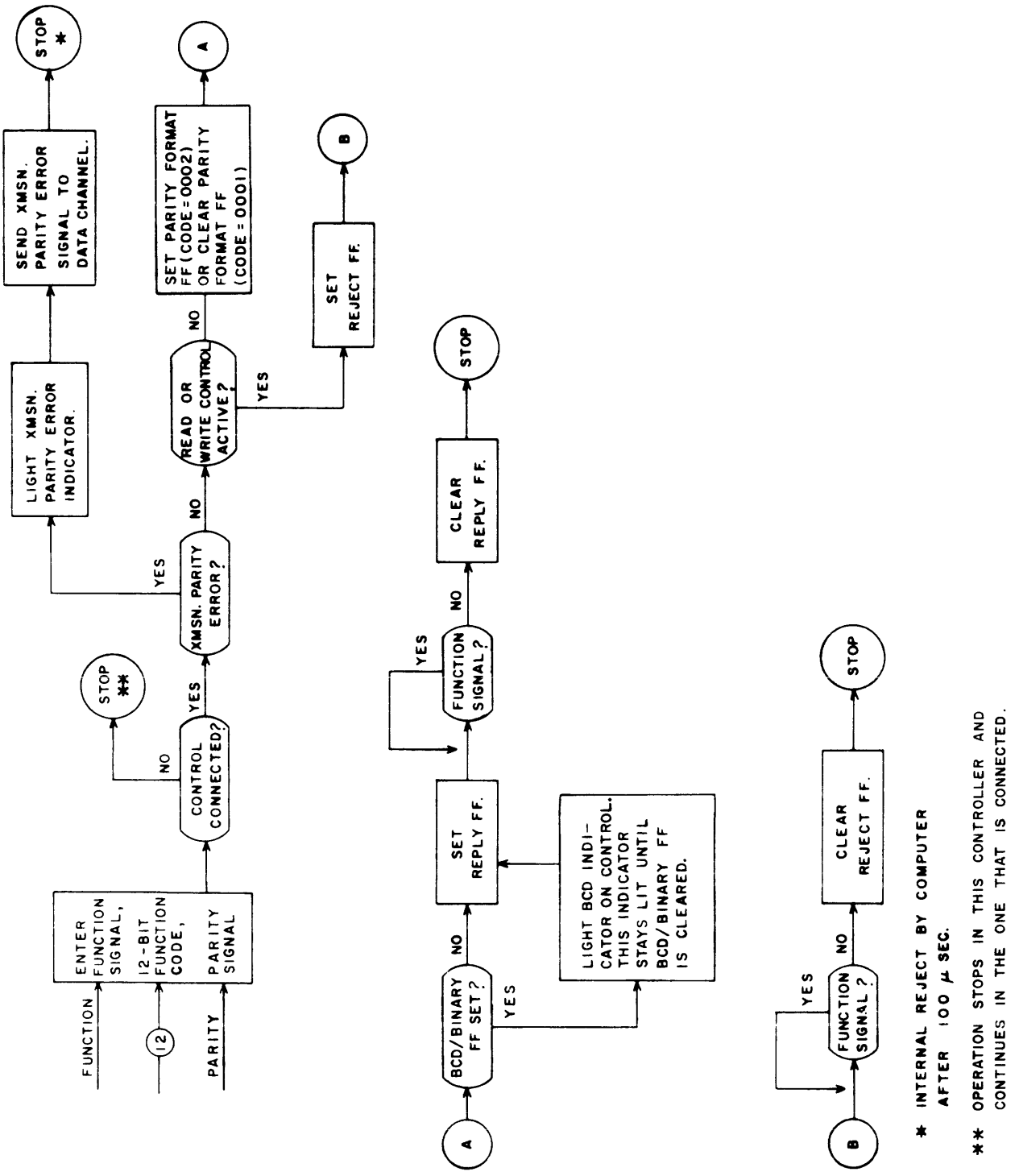


Figure 2-3. Parity Mode Operation

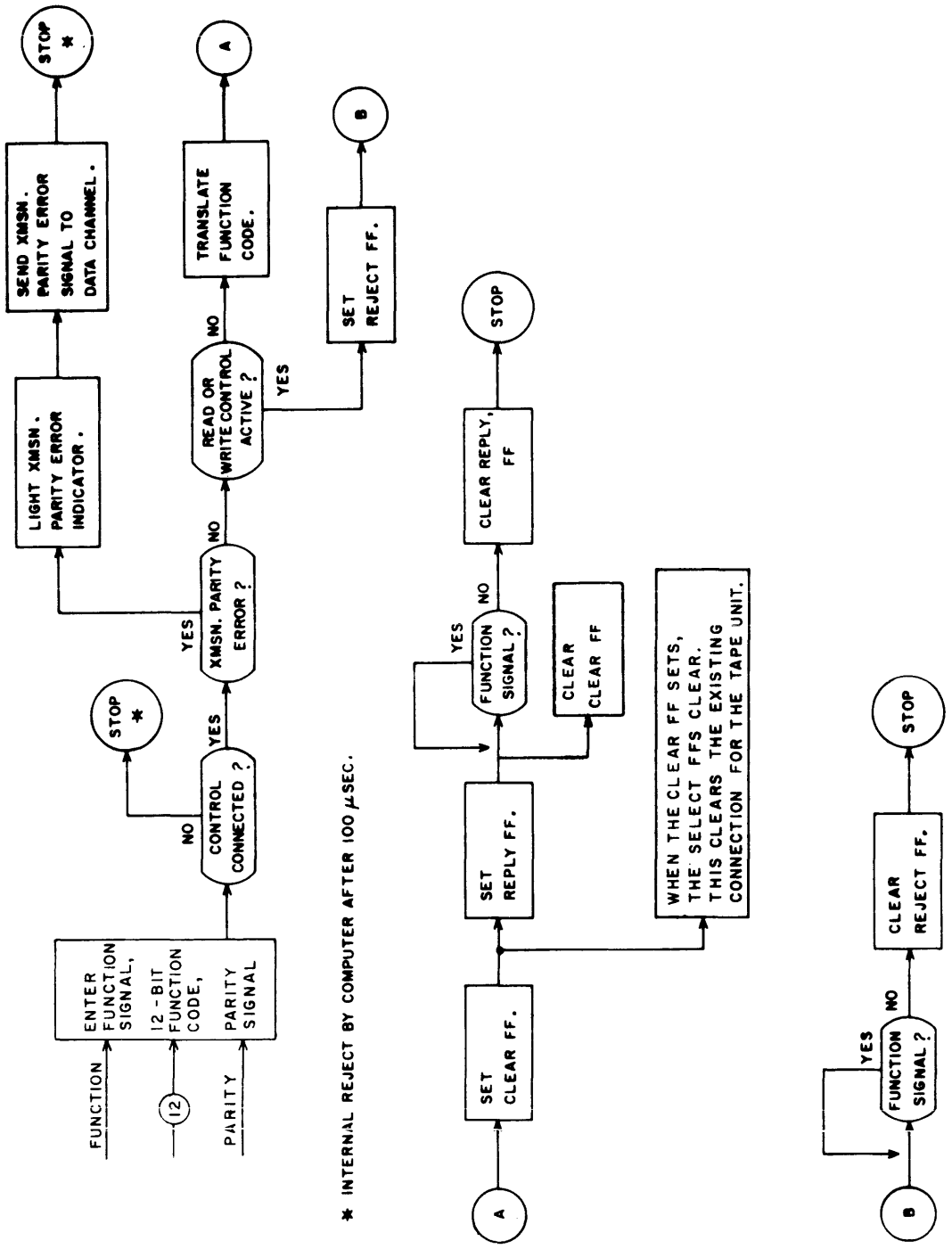


Figure 2-4. Clear Operation

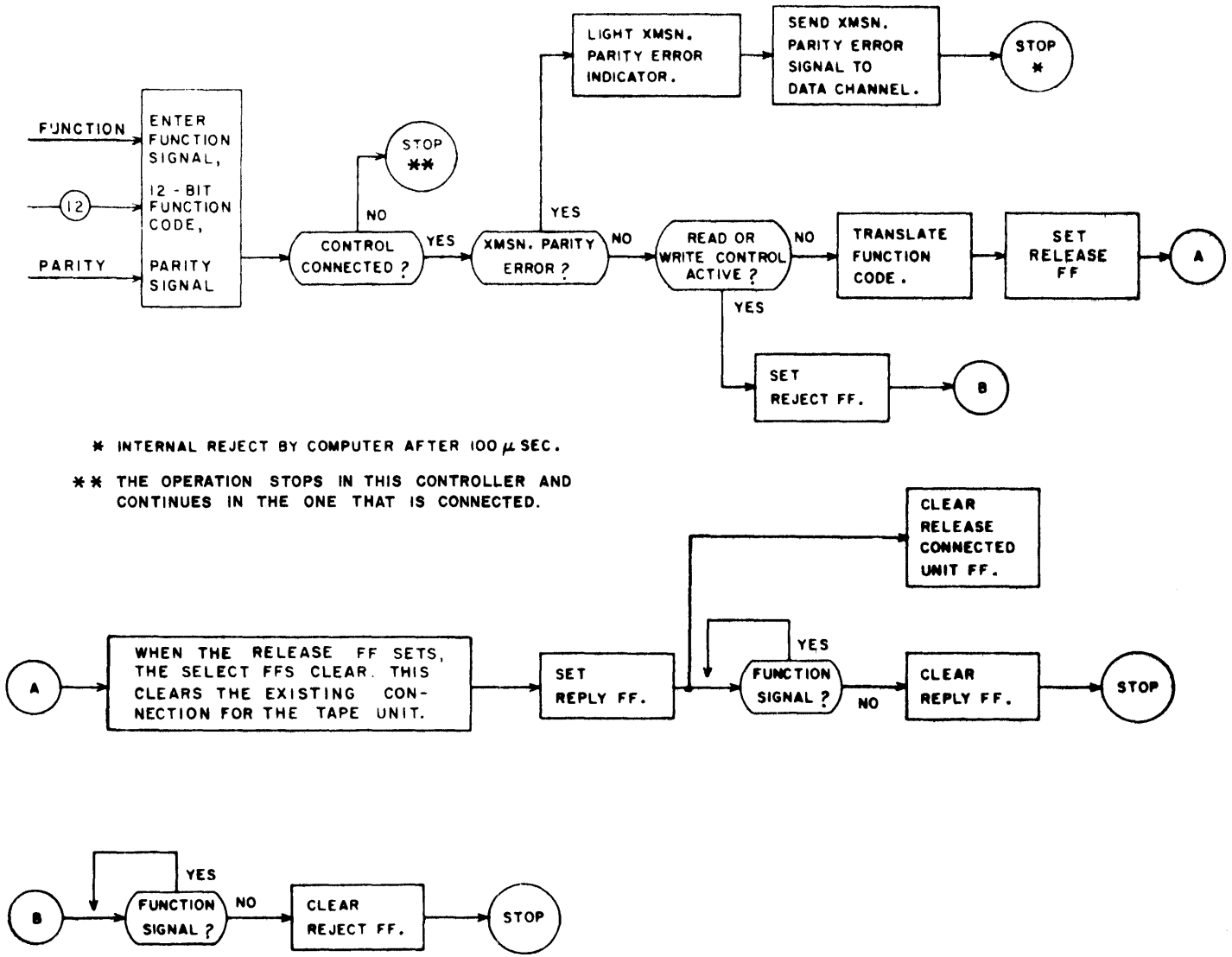


Figure 2-5. Release Operation

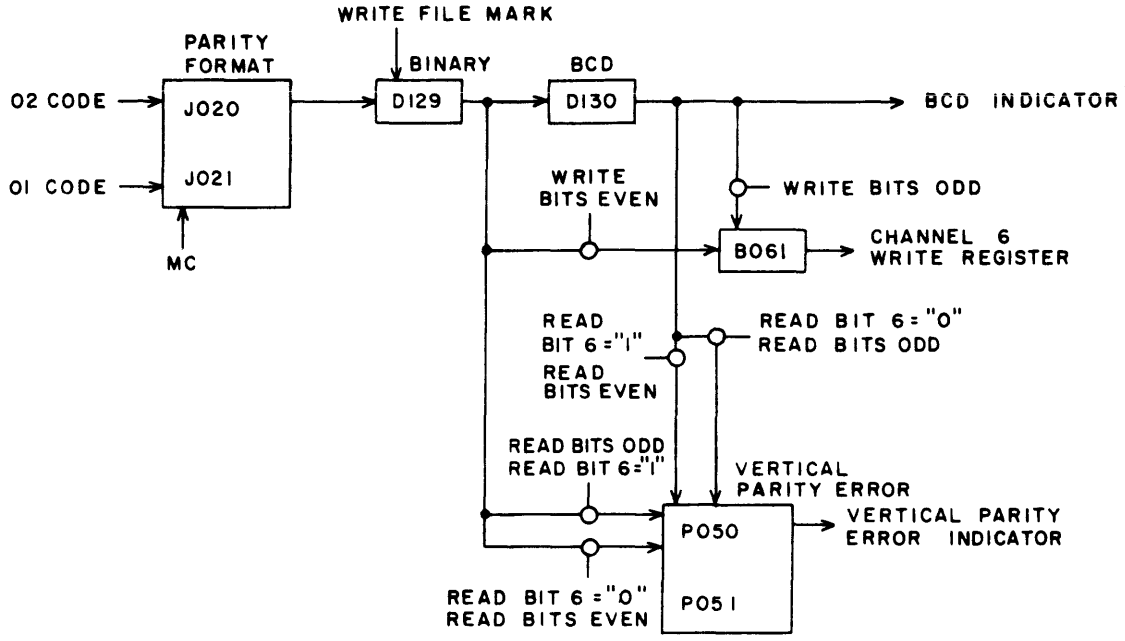


Figure 3-2-6. Parity Mode

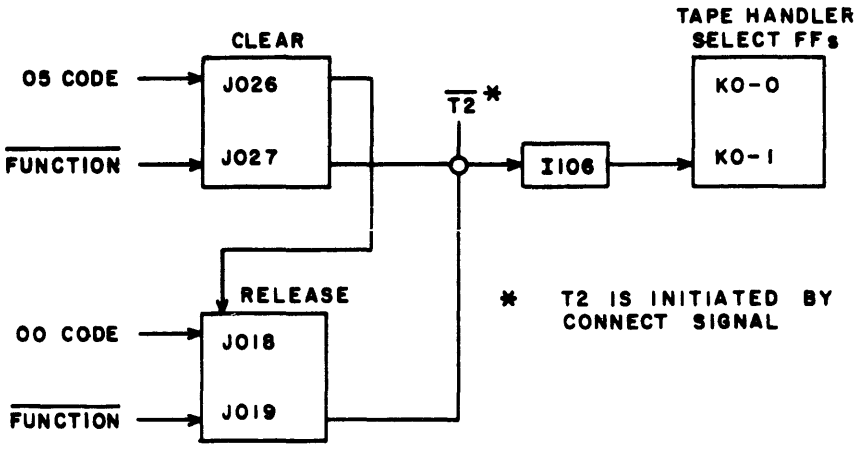


Figure 2-7. Clear and Release

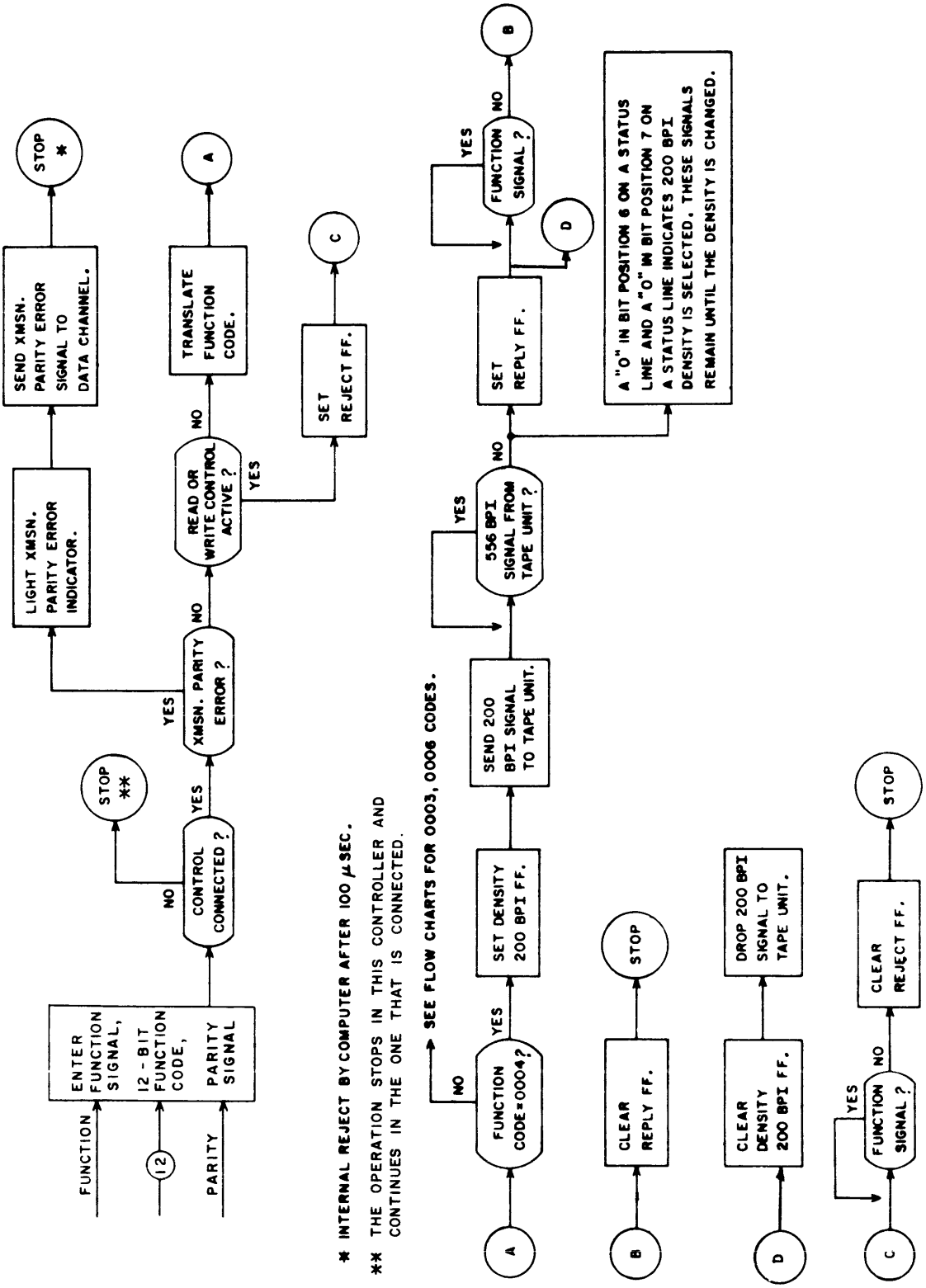


Figure 2-8. 200 BPI Operation

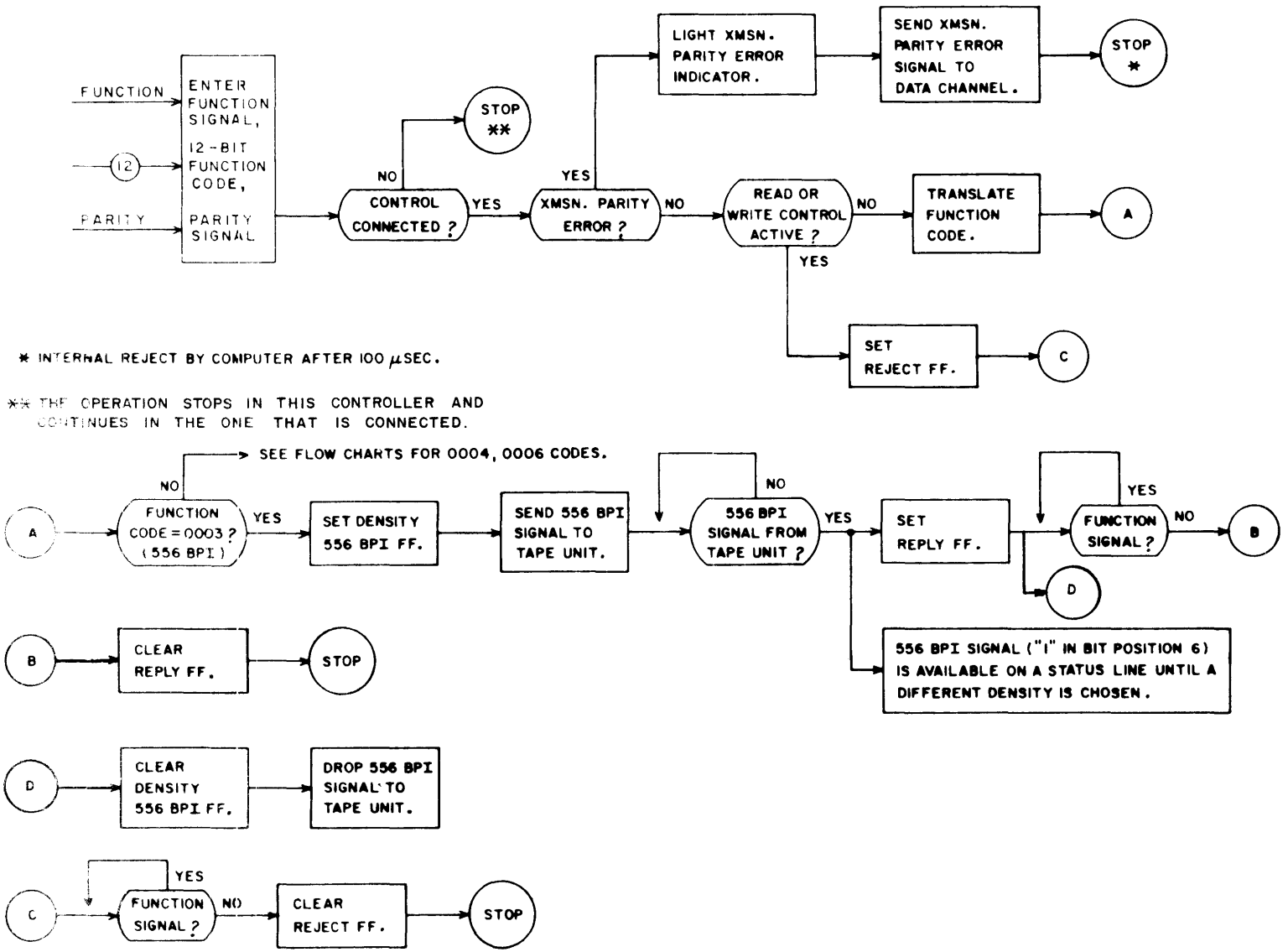


Figure 2-9. 556 BPI Operation

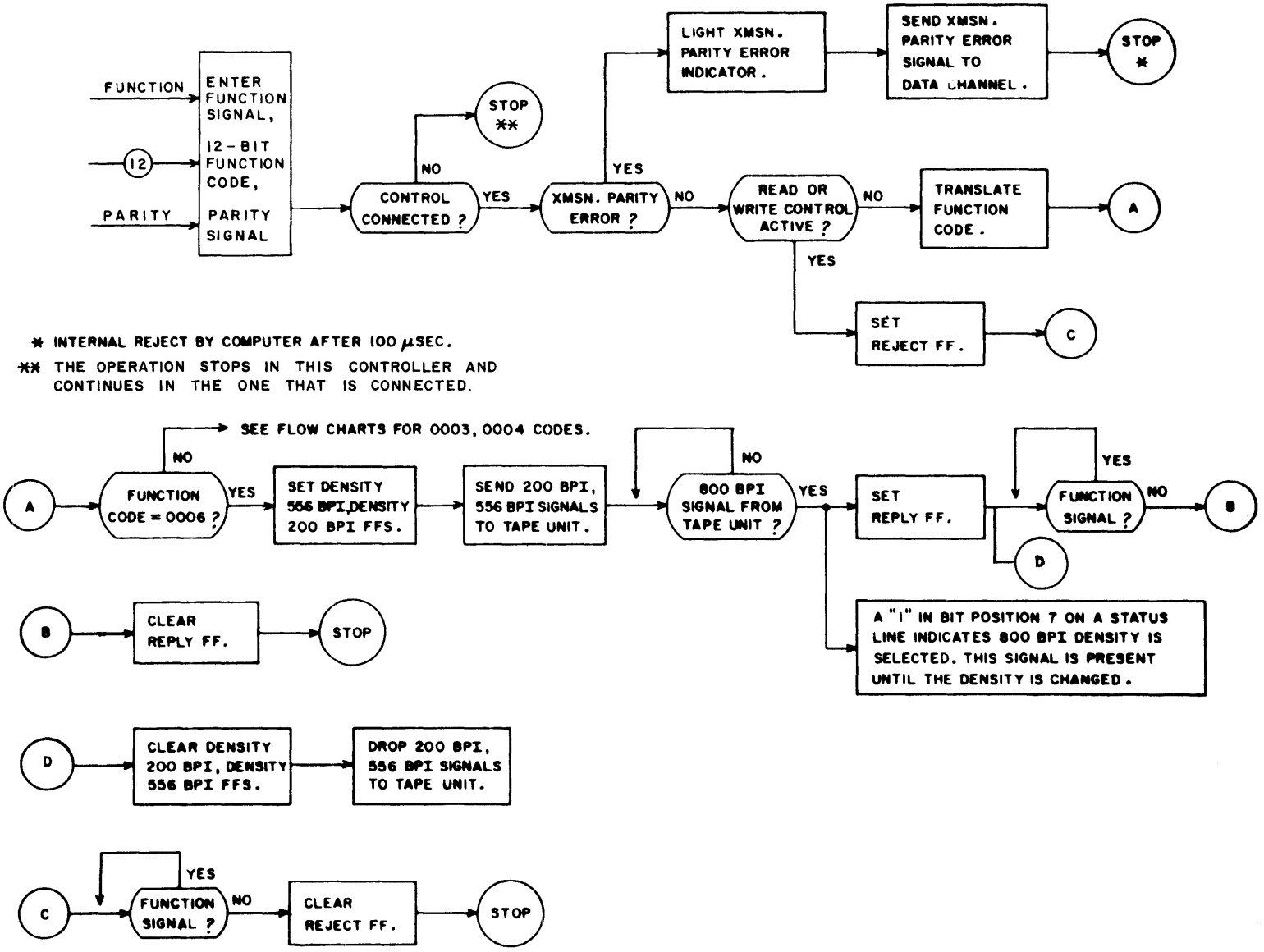


Figure 2-10. 800 BPI Operation

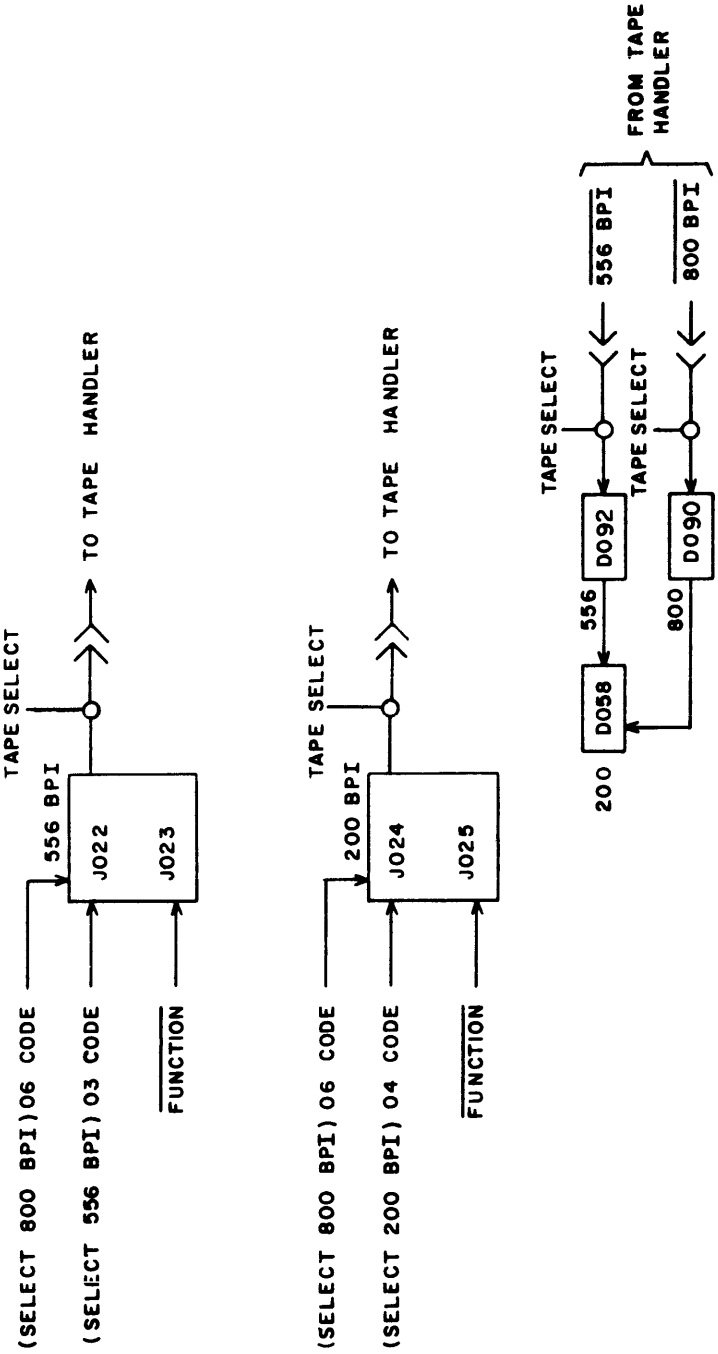


Figure 2-11. Density

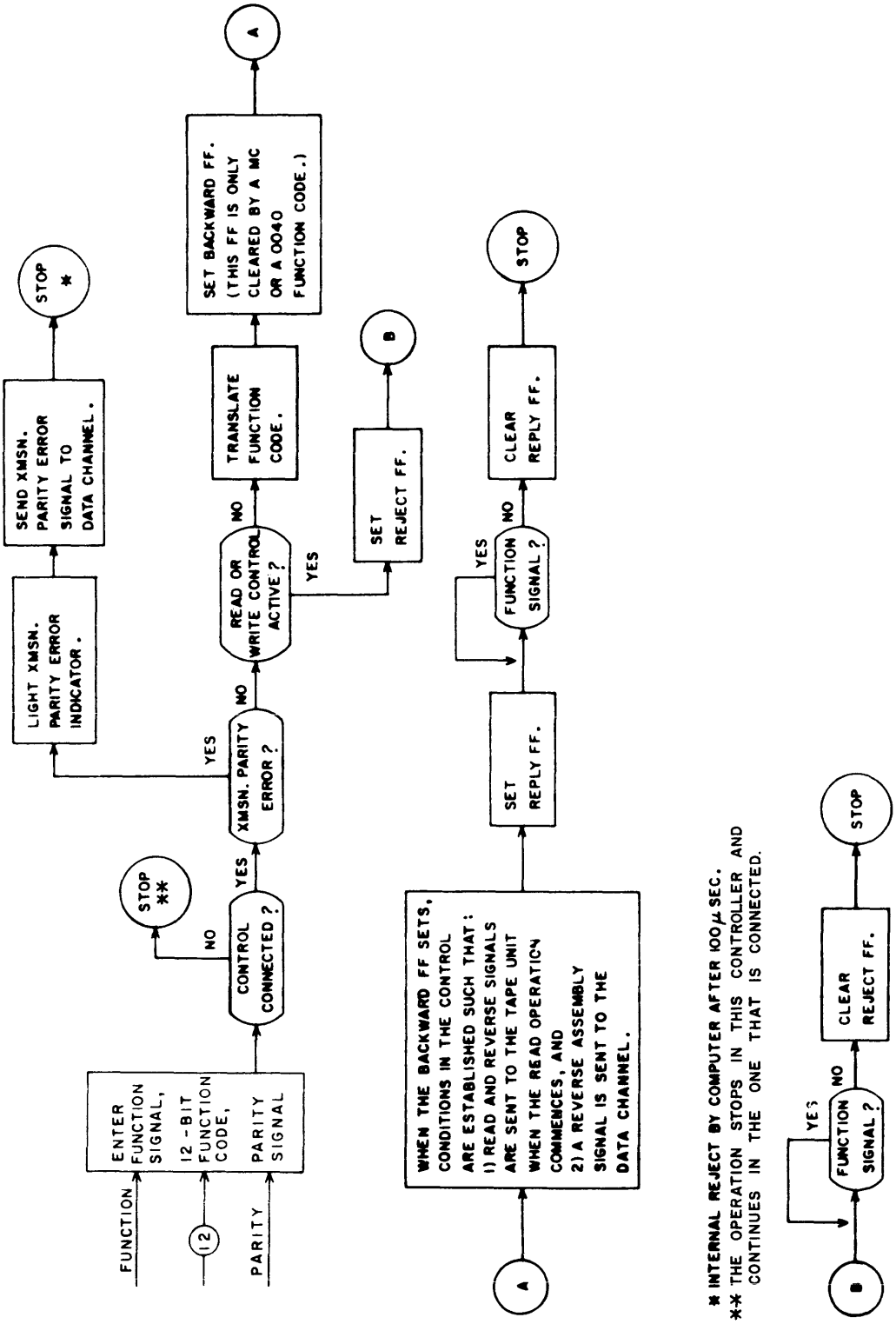


Figure 2-12. Reverse Operation

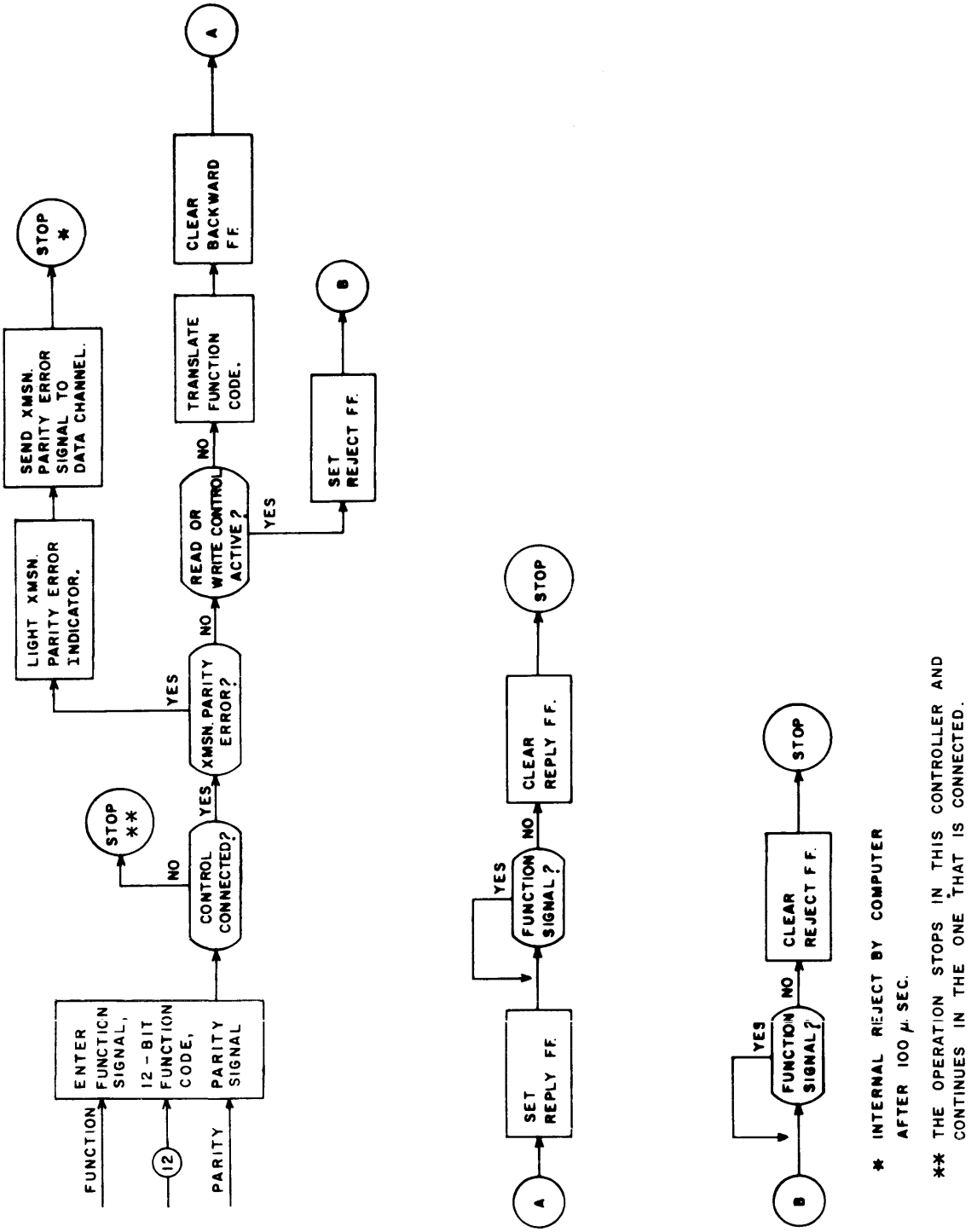


Figure 2-13. Clear Reverse Operation

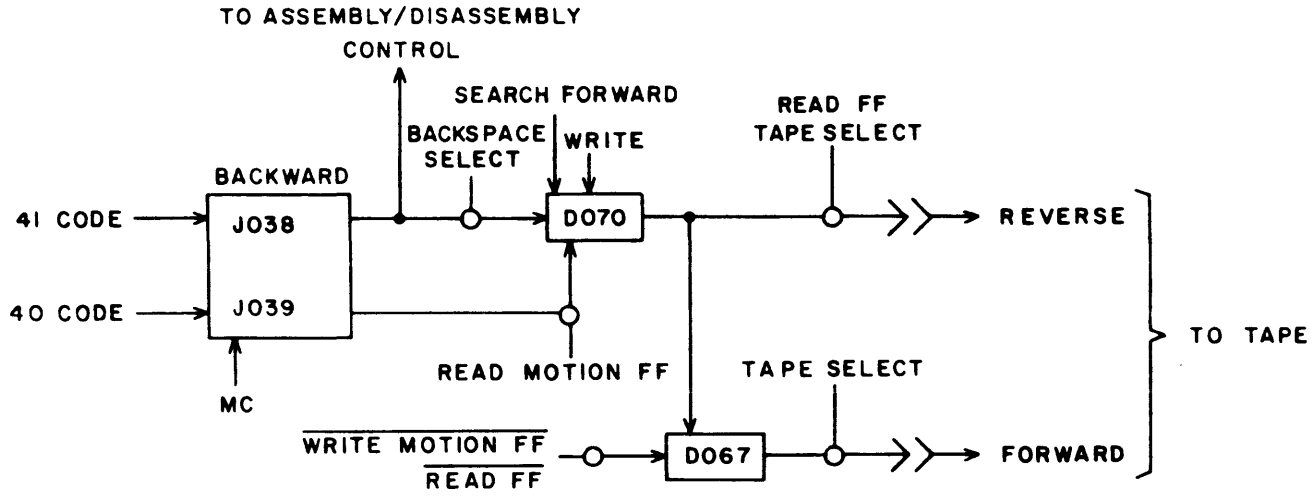


Figure 2-14. Tape Motion Signals

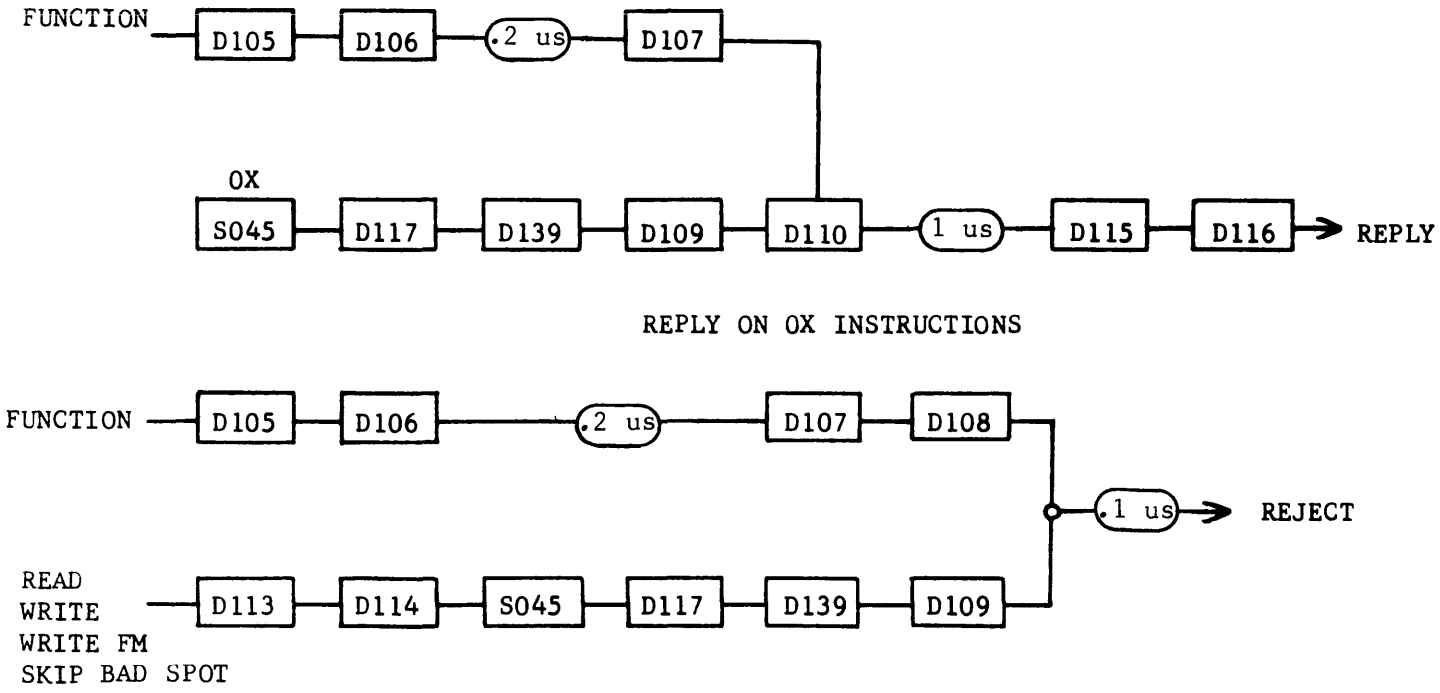


Figure 2-15. Reject on OX Instructions

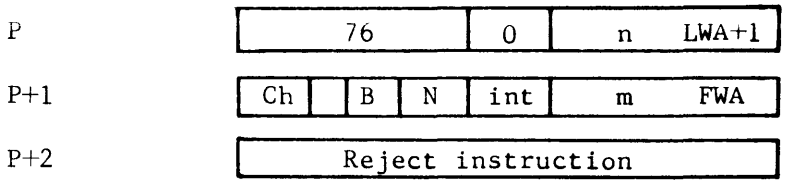
WRITE OPERATION

During Write the channel outputs a Write signal to indicate an output operation. This signal remains on the line until the output is complete. A Data signal accompanies the Write signal indicating that a 12-bit byte is ready for output.

The Write signal causes the controller to produce Forward and Write Enable signals to the transport. As each 12-bit byte is processed, a Reply goes to the channel. The channel drops the Data signal and the 12-bit data byte to clear for the next byte.

The transport complies with the Forward and Write signals and moves tape forward under the write Lead magnetically recording the data. The controller disassembles the 12-bit byte into 6-bit frames, adds a parity bit and produces a Sprocket pulse to synchronize the recording.

PROGRAM CONSIDERATION



Ch - Channel
B - "1" Backward
N - "1" 24-bit transfer, "0" for 24 to 12-bit disassembly
int - Interrupt on completion

The 76.0 code initiates a write operation. If the instructions of P and P+1 are satisfied, Main Control continues at P+3 while Block Control processes the output. If the channel designated is busy when P+1 is executed, the Reject instruction is read and executed.

The controller times the acceptance of 12-bit bytes of data and processes each byte into frames, sending each frame with a Write Sprocket signal to the transport where the frame is written on tape.

NOTE

Text page references are to the controller diagrams. The Write Operation Flow Diagram (Figure 2-16) should be used while reading the text.

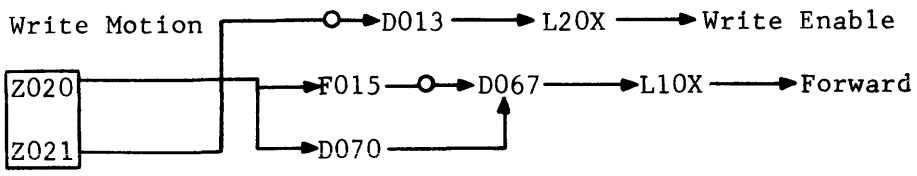
WRITE MOTION

The Write signal enters R017 (page 3-1) to start tape motion. The following conditions for the Write operation to progress are examined at AND gates and OR gates (page 3-9) as the Write signal attempts to set the Write Motion FF (Z020/021).

1. The tape transport must be connected (I114, P. 3-3)
2. The connected transport must have a Write Ring in place on the supply reel and be returning a Reply to indicate its presence (D027, P. 3-25).
3. Interrupts from previous operation must have been cleared (J036 p. 3-7).
4. A Skip Bad Spot or Write File Mark Function operation must have been completed (F011, P. 3-9).
5. A previous Lost Data indication must have been cleared (Z070/071, p. 3-9).
6. The Write Control FF (Z022/023) must be clear (Y043, p. 3-9).
7. The connected transport must be returning a Ready signal saying that it can be controlled by the channel (D003, p.3-25).
8. The connected transport must be returning a signal saying tape is not moving, exception non-stop write. (D011 and I135, p. 3-25 and 3-11).

If conditions 1 through 4 are satisfied, a constant set which has been held on Z036/037 (Write Data Lockout) will be removed and Z036/037 will clear, since F002 is a "1" from the Write Control FF (Z022/023).

If all conditions are satisfied Z020/021 (Write Motion) will set, sending a Write Signal through D013 (p. 3-23), along with a Forward signal through D067, to the connected transport.

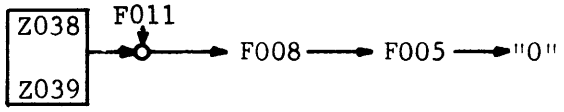


A Busy signal will be returned through D009 (page 3-25) when tape starts to move, leaving K124/125 in a set condition.

WRITE CONTROL

No frame will be written on tape until Z022/023 (Write Control) is set, thereby enabling the data signal path. The first frame is recorded 3/4 of an inch from a preceding check character, or 3 inches from a Load Point Marker.

1. From Load Point - If the tape is at Load Point, this indication returns through D015 (page 3-25) setting Z038/039 (Load Point FF). This disables these short delays (Y024 and Y057) thru F005 allowing 6 inches of tape movement before data is recorded.



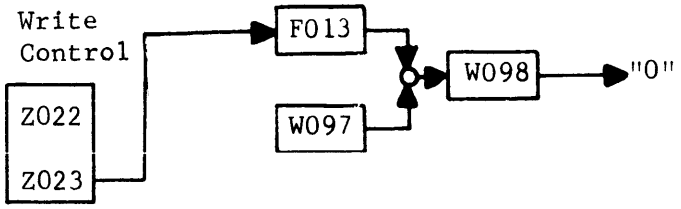
When Z020/021 (Write Motion) sets, the longest delay path is also disabled due to Load Point Reply (D015) into F003. With Write Motion setting, the forward signal is sent to the transport and tape movement starts. D015 goes to zero 10 msec after tape moves off the load point. Now the delay path through F003 is fully enabled. The 30 ms delay allows four and on-half inches of movement. The total time period (40 msec) moves tape six inches; 3 inches bringing the load point marker under the recording head, plus 3 inches to that point where the 1st frame is to be written.

2. From Record Gap - If the tape is stopped in a Record gap the shortest delay times out first.

Write Control (Z022/023) is set through F007 when either delay path times out. Setting Write Control cause F002 the end of record clear signal to drop to zero, thereby partially enabling W067. At this instant, the Controller acknowledges the Data Signal and is ready to transfer data.

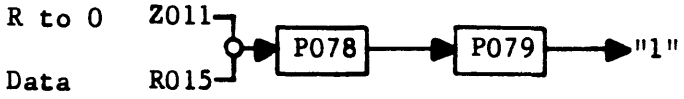
End of Record Clear has also started a 1 ms time delay through F010. If the data transfer does not occur within this time, Lost Data (Z070/071) will set. This disables W067 which prevents a late transfer from occurring.

The clear output of Write Control has caused the Clear W. signal (W098) to drop to zero, enabling the W. Register to perform its function of changing data from the channel into a form usable at the transport.



DATA SIGNAL WITH DATA AND PARITY

The Data signal, data and the parity bit arrive at the receiver cards R000-R011 and R012 (page 3-1). The bits are immediately checked for transmission parity error. The parity strobe results from the data signal.



In the event the data was in error, the Parity Error FF (K116/117) will set, returning a parity error signal to the channel. The Write operation will not be disturbed and will accept the erroneous data to be recorded.

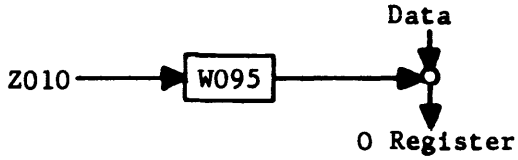
R TO 0 TRANSFER

The Data Signal (R015, page 3-1) from the Channel is present at the input to W066 (page 3-9) from 2 to 60 usec after the Write Signal. The AND gate was otherwise enabled when tne Write Data Lockout (Z036/037) was left clear by the Write signal. Connected (I114) was present or Write would not have been accepted. A clear is removed from Z010/011 (R to 0 FF) when W066 is fully enabled. End of Record (F002) --the clear output of Write Control-- is a zero, giving W076 all-zeros input driving the output to "1". The Write Resync FF (Z012/013 must be clear; and, after the delay, sets Z010/011 (R to 0) with these results:

1. Removes the Clear 0 Register Signal - As the R to 0 FF sets, W091 and W092 (page 3-11) are driven from "1" to "0",

removing a clear that had been held on the 0 Register. This assures an intially clear 0 Register.

2. Enables R to 0 - The data on Receiver cards R000-R011 are enabled to condition the 12-bit 0 Register (page 3-11) as the R to 0 FF sets, by driving W095 and W096 to "1"



WRITE RESYNC

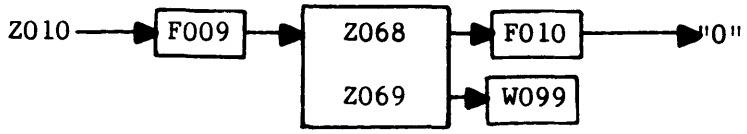
Delayed 0.1 usec from the R to 0 Transfer

sets Z012/013 (Write Resync FF)

with the following effect:

1. Disables the Data signal input from W067. Another input to the 0 Register is not needed as a result of this Data signal. Write Resync (Z012/013) will act as a toggle, allowing inputs of 12-bit bytes to be changed into frames.

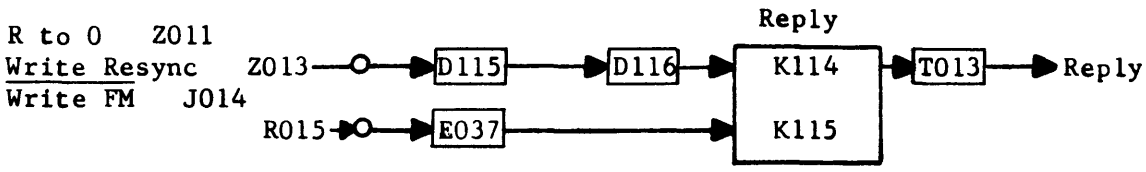
2. Disables F010 before 1 ms delay times out and lost data is detected. This results from Z068/069 setting;



but it should be noted that W099 is partially enabled to allow lost data under another circumstance.

3. Prevents the 0 Register from being cleared during disassembly mode until two frames have been generated and sent to the transport.

4. Sends the Reply to the channel, acknowledging receipt of data. As the Write Resync sets, the path to set the Reply FF K114/115 is made.



The Reply signal received in the channel causes the data signal to drop, clearing the Reply FF and dropping the Reply signal.

The absence of the data signal also causes W066 (page 3-9) to revert to a logical "1", clearing the R to 0 FF (Z010/011).

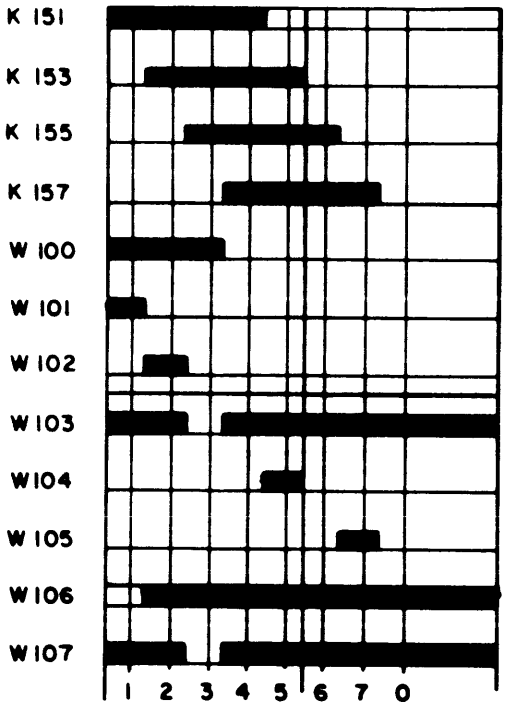
WRITE TIMING AND DENSITY CONDITIONING

As soon as the Controller is powered up, 3 oscillators begin to function. Their outputs are converted to logical 1 pulses by an associated V term. These circuits produce the basic transfer frequencies to control the transfer rate. The Density Reply from the connected tape unit determines which frequency will be used. For example, a 200 BPI Density, reply (D058, p. 3-2) will enable the 30KC oscillator to start the timing chain every 33 1/3 usec.

The inverter I141 is pulsed at the same rate as I140. If the connected transport is a 606 or 607 at 150 ips tape speed, the inverter I141 outputs each time it is pulsed. If a 603 or 604 is connected and tape moves at 75 ips, the rate must be halved. The OR input to I141 disables the output on alternate pulses, using the counter K160/161 and K162/163.

Each logical "1" output from I141 initiates a pass down the Write Timing Chain. Each pass down the chain controls the preparation and writing of one frame on tape. The progress of the chain is translated into the enables needed to process the data from channel to transport.

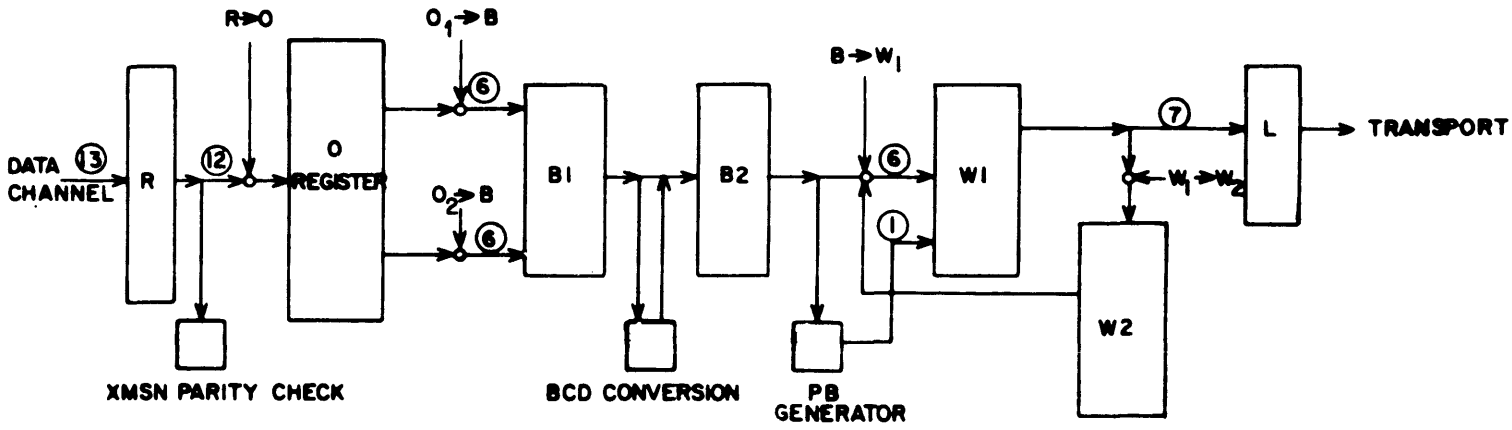
WRITE TIMING



Times 0 through 7 are assigned to these enables (W100-W107) for ease in referring to them.

DATA FLOW

Data will be processed through the controller on the diagramed path.

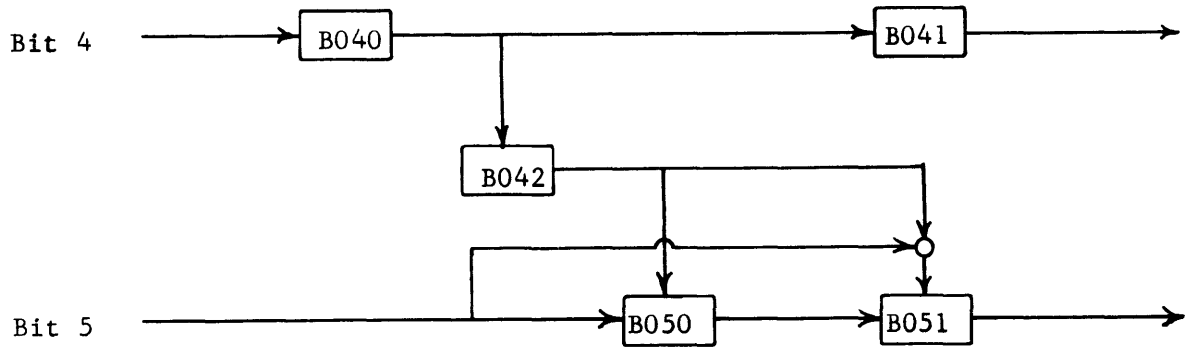


At this point, the O Register is loaded with a 12-bit byte from the channel as a result of the R to O transfer. The problem now is to disassemble the information into two 6-bit frames; convert from internal to external BCD codes, if required; generate a parity bit; convert the information to change on "1" data; and deliver the frame to the transport. The disassembly counter will control the order in which the bits from the O Register are selected. Two passes of the Write Timing Chain will be needed, one for each of the two frames which will result from a single data channel output.

The O to B transfer is the disassembly function. Either the upper six bits or the lower six bits from the O Register will be gated to the B_1 inverters. The condition of the disassembly counter, being advanced by timing, will determine the order of disassembly. If DK_1 is clear, the upper six bits will transfer; if set, the lower six bits will transfer.

Data appearing in B_1 will feed through and appear in B_2. The network between these two inverter ranks can cause a conversion from internal to external BCD.

The rule for conversion is: if bit four is a "1", complement bit five (bit four remains unchanged).



The codes for selected characters are:

	internal	external
A	21	61
I	31	71
S	62	22
Z	71	31

Passing bits four and five through this net work will prove the conversion.

An excention to the rule is in the case of the character 0 which has the Internal Code 00 and the External Code 12. The network is not affected by this code: however, all B_1 outputs will be ones, fully enabling the AND gate into B002 and forcing B004 to a logical "0". Inverter B004 breaks AND gates into B011 and B031, converting the 00 code entering B_1 inverters to a 12 code coming from the B_2 inverters.

Conversion is not performed for: 1) binary mode, 2) conversion negated, or 3) writing a file mark.

The output of B_2, which is six information bits, is fed into a Write Parity generator (page 3-11). Actually, the network checks the bits present to determine whether they total odd or even in number. If the total is even, inverter P014 will output a logical "1". Parity must be odd in Binary mode and even in BCD mode. Terms D129 (Binary and D130 (BCD, page 3-7) condition the output of P014 to product the required parity bit. The possible conditions are:

Word Count Even, P014 is "1"

1. Binary-- Odd Parity
   P014 ⟶ B060 ⟶ B061 ⟶ W060
   Write a "1" (frame count makes parity odd)
2. BCD-- Even Parity
   P014 ⟶ B061 ⟶ W060
   Write a "0" (frame count leaves parity even)

Word Count Odd P014 is "0"

3. Binary-- Odd Parity
   P014 ⟶ B060 ⟶ B061 ⟶ W060
   Write a "0" (Frame Count leaves parity odd)
4. BCD-- Even Parity
   P014 ⟶ B061 ⟶ W060
   Write a "1" (Frame Count makes parity even)

The B to W_1 transfer converts the information frame of seven bits so far produced, into change-on-ones data. The W_1 and W_2 Registers work in conjuction with each other. A logical "1" from B_2 inverters changes the state of the corresponding FF in the W_1 Register. For example, the table (on the next page) shows the data from the 0 Register in octal form, bits from B_2 inverter (binary form), the condition of W_1 as it progresses, the binary bits appearing on-line to the transport, and translation of the line bits.

TABLE 2-1

From 0 Register	From B_2 Inverters	State of W_1 Register	Bits on Line
Nothing	000 000	C C C C C C	000 000
63	110 011	S S C C S S	110 011
46	100 110	C S C S C S	010 101
45	100 101	S S C C C C	110 000
23	010 011	S C C C S S	100 011
51	101 001	C C S C S C	001 010
46	100 110	S C S S C C	101 100
43	100 011	C C S S S S	001 111

The W_2 register is equalized (W_1 to W_2) after each B to W_1 transfer to enable a change-on-ones operation from the B_2 inverters. The contents of the W_1 register are accompanied by a Sprocket Signal timed to record frames in a uniform pattern as dictated by density.

SEQUENCE FOR DATA TRANSFER

1. Data Signal with data
   - Sets Z010/011 (R to 0 FF)
     - Drop Clear 0 Register signal
     - Gate R to 0
   - Set Z012/013 (Write Resync)
   - Sets K114/015 (Reply FF)
     - Data signal drops
       - Clear K114/015 (Reply FF)
       - Clear Z010/011 (R to 0 FF)

2. Gate upper six bits from the 0 Register to the transport
   - Time 0 - Set Z014/015 (Write gate)
   - Time 1 - Transfer W_1 to W_2
     Transfer DK_1 to DK_2
   - Time 1-3 - Gate 0^2 to B
   - Time 2-3 - Gate B to W_1
   - Time 3 - Set Z008/009 (Write Sprocket FF)
     Send Sprocket to transport
   - Time 5 - Advance DK Counter
   - Time 7 - Clear Z008/009 (Write Sprocket)
     Clear Z014/015 (Write gate)

3. Gate lower six bits from the 0 Register to the transport
   - Time 0 - Set Z014/015 (Write Gate)
   - Time 1 - Transfer W_1 to W_2 and DK_1 to DK_2
   - Time 1-3 - Gate 0^1 to B
   - Time 2-3 - Gate B to W
   - Time 3 - Set Z008/009 (Write Sprocket FF)
   - Time 5 - Advance DK Counter
     Clear Z008/009 (Write Sprocket FF)
   - Time 7 - Clear Z012/013 (Write Resync FF)
     Clear 0 Register
     Clear Z014/015 (Write gate FF)

At the completion of the preceding sequence, a new Data signal with data will cause the sequence to be repeated. New Data signals should be available as the Write Resync FF clears.

If a new data signal is not present prior to Time 5 (W104) when a new frame should have been written and the Write Signal is still up:

Set Z070/071 (Lost Data) through W099

disabling W067 and preventing later arrival of data.

The Check Character will be written and a normal terminate will occur to preserve that portion of the record received in good condition.

TERMINATE

The controller prepares for end of record when the 12-bit byte of data from the channel has been sent to the transport. Each Time 5 (W104), as the second frame is processed from the byte, the Initiate Check Character FF (Z000/001) is set. If a new Data Signal arrives, the R to 0 FF sets and the Initiate Check character FF is cleared. The normal terminate will occur when the entire specified block of information from memory has been transferred by the block Control Section of the computer. At that time, the channel drops the Write signal (R017) and no new Data signal is generated.

As R017 (Write signal) goes to zero, Z036/037 (Write Data Lockout) sets. The possibility of lost data occurring is disabled by clearing Z068/069 and holding W099 to zero.

Three frames must be missed before the check character will be written. The controller will then revert to its static condition ready for a new operation. The Check Character is progressing since the Initiate Check Character could not be cleared and the End of Record Strobes W106 and W107 occur at Times 1 and 3.

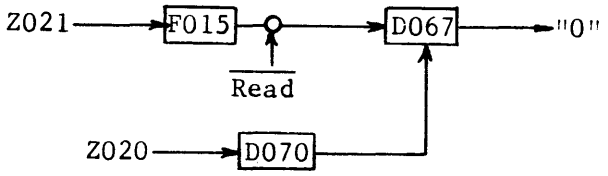
Miss 1st frame	Time 1	Set Z002/003	SSCC
	Time 3	Set Z004/005	SSSC
Miss 2nd frame	Time 1	Clear Z002/003	SCSC
	Time 3	Set Z006/007	SCSS
Miss 3rd frame	Time 1	Set Z002/003	SSSS
	Time 3	Clear Z004/005	SSCS

The required space for the Check Character gap has been allowed and the Check Character must be written. A change of the W_1 Register is needed to produce the Check Character. Clearing W_1 will produce this change

in those FFs of the W_1 Register which are set at that time.

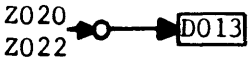
Time 1	Clear Z002/003
	Clear W_1 Register
	["0" → W076 → W097 → ○ → W098 → W_1]
	Set Z030/031 (Write Terminate I)
Time 3	Set Z008/009 (Write Sprocket)
Time 7	Clear Z008/009 (Write Sprocket)
	Clear Z000/001 (Initiate Check Character)

The Check Character is now on tape and the controller must revert to its static state. At Time 1 the Write Terminate FF was set. A time delay must elapse during which time the tape moves into the record gap. When this delay ends, Write Terminate I and Write Motion FFs. clear. Write Motion clearing causes the Forward signal to the transport to drop.



This causes tape to stop approximately 0.3 inch from the check character.

The clear output from the Write Motion FF delays 1 usec then clears the Write Control. At this point the Write signal to the transport is dropped.



The End of Record Clear (F002) signal goes to "1"

Clear Z032/033 (Write Term II)
Disabling Data signal input W067
Killing Lost Data (F010)
And holding Z036/037 (Write Data Lockout) both set and clear

NON-STOP WRITE

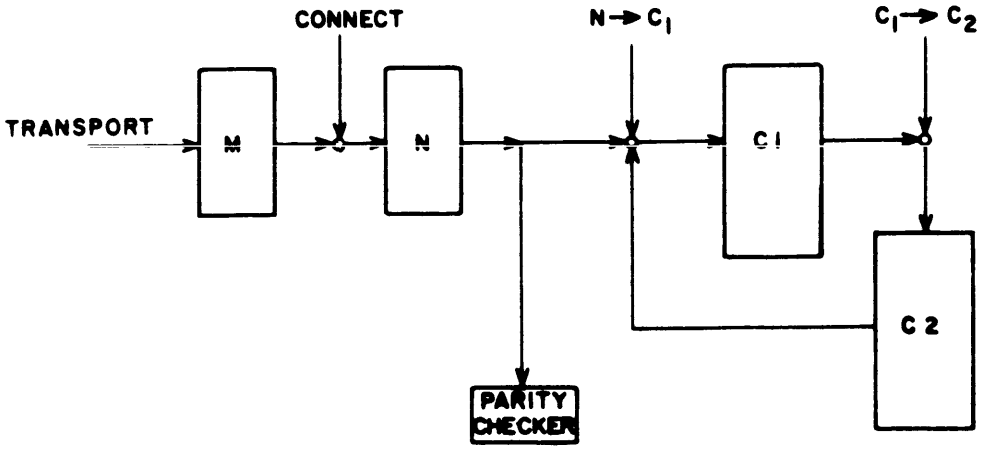
When terminating a write operation, the Forward signal to the tape transport drops. Current is reversed through the forward voice coil valve (this valve controls vacuum to the capstan) in an attempt to remove vacuum from the capstan. Its travel time will be approximately 1.25 ms. If a new Write signal appears at the controller, the Write Motion flip-flop could reset 1.1 usec after it was cleared. A new Forward and Write signal will be sent to the transport when the Write Motion FF sets. The valve again energizes to apply vacuum to the forward capstan. During the 1.1 usec, with the Forward signal absent, the valve moved very little physically. The tape did not stop between the two records.

WRITE REPLY (READ AFTER WRITE)

The accurancy of a recording is checked by reading each frame, including the Check Character. After recording a frame, moving tape 0.3 inches will place that frame beneath the read head. It takes the frame two milliseconds to move from the write head to the read head. The read head detects the recorded bits and sends them to the controller.

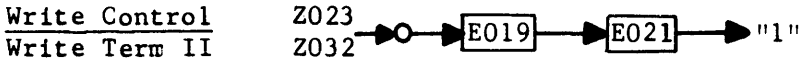
This data is not returned to the channel. Each individual frame is checked for vertical parity error by comparing the number of data bits to the parity bit. Longitudinal parity is checked when the read head reaches the record gap.

When the Check Character is read, each track should have written an even number of "1" bits. As the data is read (including the Check Character) it is stored in a double ranked register similar to the W register. If the number of :1: bits read back in each track is even, the C register will be clear. If any track read back an odd number of bits, the End of Record signal (D039 and Parity Error (P053) set the Longitudinal Parity Error FF (page 3-21).



When Write Motion (Z020/021) sets and before Write Control sets, the C register is cleared.

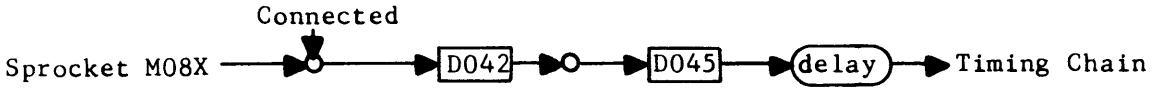
As Write Control sets, the clearing term (E026) reverts to zero. When Z022 (Write Control) sets, the Read/Write Active signal (E021, page 3-15) comes up



enabling the Read Timing Chain.

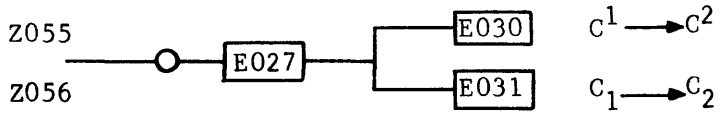
The presence of the data from the transport is signaled by the Read Sprocket (D042 or D044, page 3-27) a Reply signal which goes to "0" from its static "1" condition.

When the Read/Write Active signal is present, each Sprocket signal starts a pass down the Read Timing Chain.



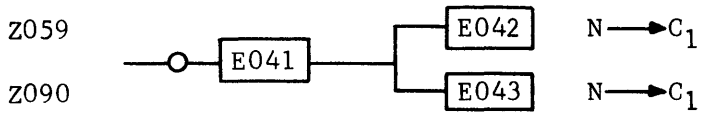
Time 1 As the first FF (Z054/055) sets

C_1 to C_2 which equalizes the C Registers



Time 2 — As the second FF (Z056/057) sets, Sets Z052/053 (Reply Timing Chain Lockout FF) to prevent a second start of timing on the same Sprocket signal.

Time 3 — As the third FF (Z058/059) sets, N to C_1 transfers data coming from the transport in to the C Register.

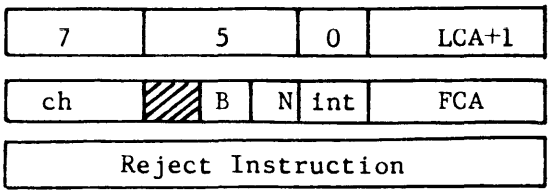


As the Sprocket signal from the transport is removed, D042 and D044 are both ones and the Reply Timing Chain Clockout FF (Z052/053) is cleared. This operation repeats as each Sprocket arrives. It should be realized that the C_1 Register is progressing in the same manner as the W_1 Register, though approximately 2 ms. behind in time. At the end of the Write operation as the check character conditions C_1, it, like the W_1 Register, should finish in a completely clear state. As the tape transport clears motion, and tape stops in the record gap, an End of Record reply D039 is returned.

At this time, if no recording error has occurred, C_1 will be clear. All zeros are fed into P052 (p. 3-21), causing the term to output a "1". Any FF in the C_1 Register not clear, indicates an error. A logical "1" is felt into P052, causing the Longitudinal Parity Error FF to set.

WRITE OPERATION
(6 bit)

PROGRAM FOR WRITE CHARACTER



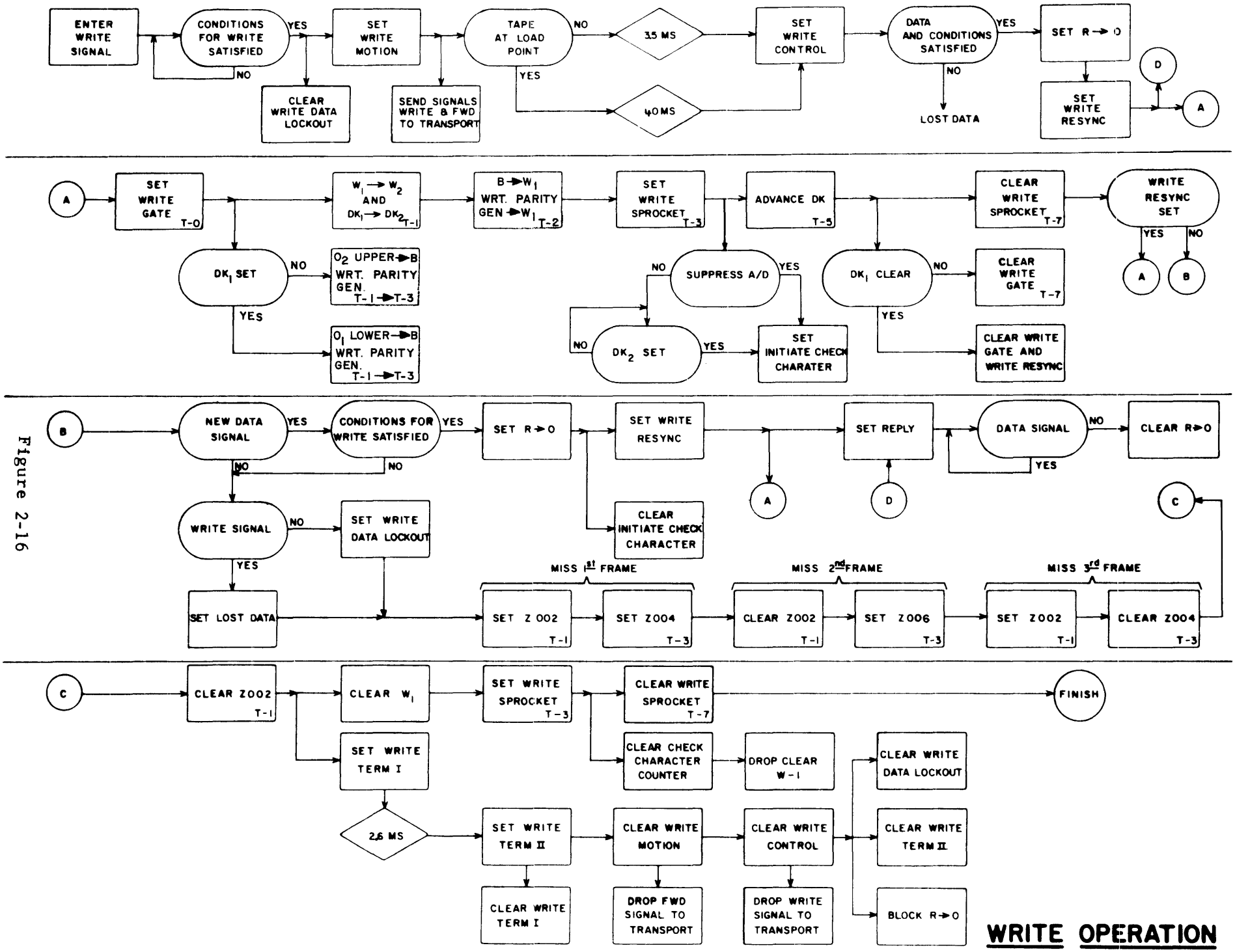


Figure 2-16

WRITE OPERATION

This program puts the Write signal and Suppress AD signal (R022) on line.

1. Set J046/047 (Suppress AD)
   Hold DK_1 Clear

2. Initiate Write Circuits and Tape Motion

DATA SIGNAL WITH 6-BIT BYTE

1. Set Z010/011 (R to 0)
   Remove Clear 0 signal
   Gate R to 0

   Set Z012/013 (Write Resync)
   Block another Data signal
   Block Clear 0 Register (W094)

   Set Z068/069 (Lost Data Conditioning)

   Set K114/115 (Reply)

2. Data signal drops (from the Reply)
   Clear K114/115 (Reply)
   Clear Z010/011 (R to 0)

3. Generate the Frame

Time 0	Set Z014/015 (Write Gate)
Time 1	W_1 to W_2
Time 1-3	Gate 0_1 to B
Time 2-3	Gate B to W
Time 3	Set Z008/009 (Sprocket)
Time 5	Set Z000/001 (Initiate Check Character)
Time 7	Clear Z008/009 (Sprocket) Clear Z012/013 (Write Resync) Clear 0 (permit input Data signal) Clear Z014/015 (Write Gate)

4. New Input Data signal - Repeat 1-3
   No New Data signal - Write Check Character

FUNCTION OPERATIONS - MOTION DIRECTIVES

The functions causing motion directives are very similar to the Format Functions. The Function signal, with a 12-bit Function Code, is put on the channel from the computer. Only the connected controller may accept the signal. The function code is in the form XXCD. The codes causing

Tape Motion will have a "1" in the C position.

Those functions which cause Motion are:

TAPE MOTION			
Rewind	0010	Search End of File Mark Backward	0014
Rewind Unload	0011	Write End of File Mark	0015
Backspace*	0012	Skip Bad Spot	0016
Search End of File Mark Forward	0013		

* Backspace following a Reverse Read moves tape forward one record.

All but Write End of File Mark and Skip Bad Spot, are used to index the tape to the position needed to read or write on the tape.

A definition and description of each operation is included in this text along with specific flow charts.

At this point a detailed explanation of the function should not be necessary and use of the flow chart is encouraged to carry through the operation in the prints.

The format for programming these functions are the same as specified in the proceding section on Functions for Format.

SKIP BAD SPOT

The Skip Bad Spot FFs (Figure 2-17) simulate a partial write operation. The Write Motion FF (page 3-9) is set as if the write signal were present. The 30 ms (70 ms) delay path to set the Write Control FF is initiated (this allows time for the tape to move 4½ inches. This delay is adjustable from 3 to 6 inches. When the Write Control FF is set, Write Termination I FF sets and a Write termination procedure ensues.

WRITE FILE MARK

The Write File Mark FFs (figure 2-19 and page 2-55) simulate a write operation which automatically writes one frame (17 BCD) and its check character on the tape. The Write Motion FF (page 3-9) is set as if the Write signal were present (figure 2-19). The 30 ms (70) delay path to set the Write Control FF is initiated (this allows time for the tape to move 4½ inches). This delay is adjustable from 3 to 6 inches. When the Write Control FF is set, the R to 0 FF is set as if the Data signal were present. The File Mark is then sent to the W_1 register as if it were a frame of data. The normal End of Record precedure (leaving 3 blank frames

and then writing the check character) follows.

SEARCH FORWARD TO FILE MARK

The Search Forward to File Mark FF (figure 2-20 and page 2-57) simulates a partial read operation. The Read FF (page 3-23) is set as if the Read Motion FF were set by the Read signal (figure 2-20). The Forward signal, the Read signal, and the Stop on File Mark signal are sent to the tape handler. The Stop on File Mark signal modifies the End of Record circuit in the tape handler so that the End of Record signal is returned to the Controller, only when a File Mark is sensed. This permits tape motion continue over any End of Record gaps.

SEARCH BACKWARD TO FILE MARK

This operation is identical to Search Forward except that the Search Backward to File Mark FF (figure 2-21 and page 2-58) initiates reverse, rather than forward, tape motion.

BACKSPACE

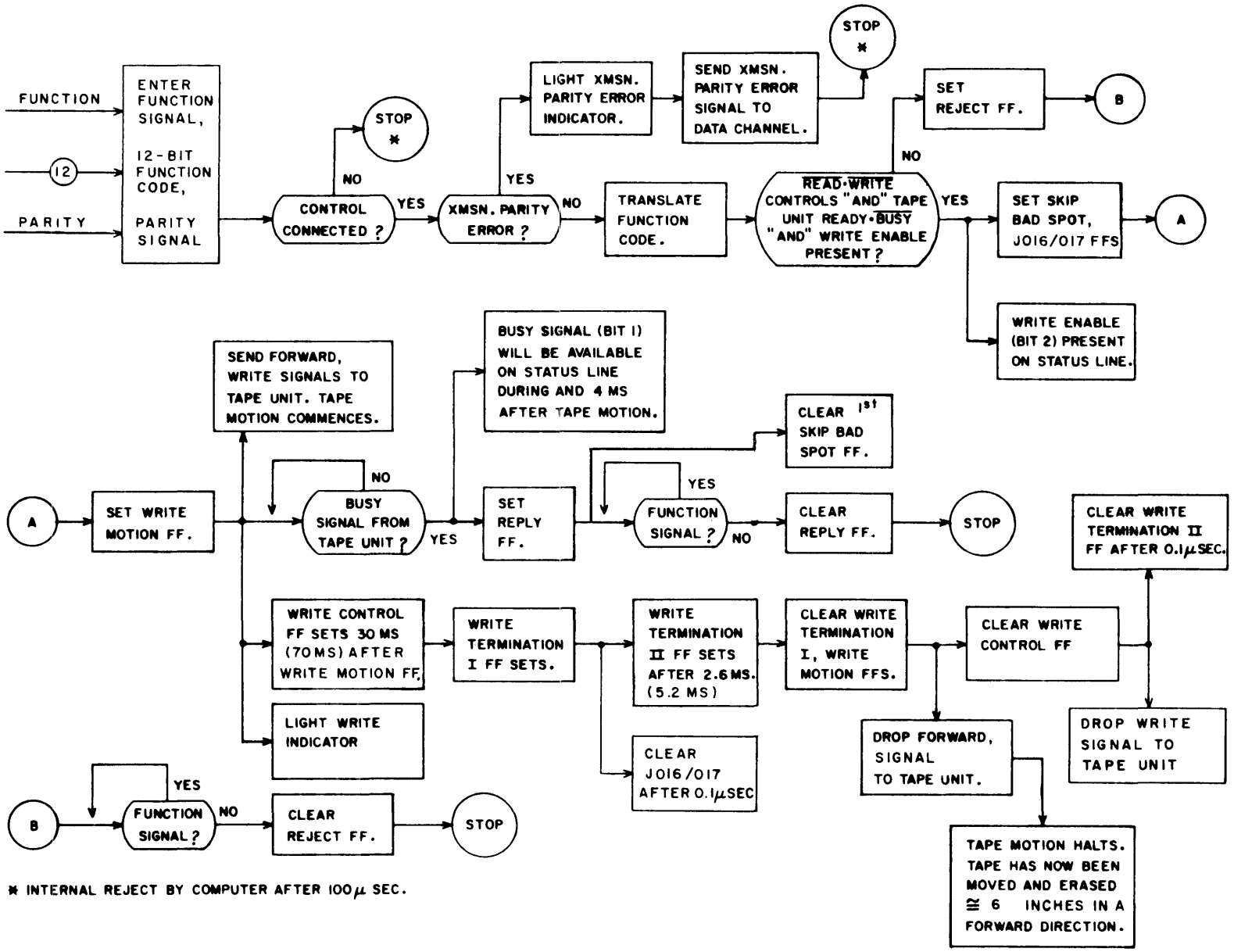
The Backspace FF (figure 2-22 and page 2-59) simulates a partial reverse read operation. The Read FF (page 3-23) is set as if the Read Motion FF were set by the Read signal. The Reverse signal and the Read signal are sent to the tape handler. Tape motion continues until the tape handler senses an End of Record.

REWIND

The Rewind FF (figure 2-23 page 2-60) sends to the connected tape handler the Rewind signal (figure 2-23). This signal instructs the tape handler to rewind at high speed to the nearest Load Point. The controller is free to perform another operation with a different tape handler. When the rewinding tape handler senses the Load Point, tape motion terminates. Ready and Load Point signals are then sent to the controller. A new operation is then possible on this unit.

REWIND UNLOAD

The Rewind Unload FF (figure 2-24 and page 2-61) sends to the connected tape handler the Rewind Unload signal (figure 2-24). This signal instructs the tape handler to rewind at high speed until the tape is completely off the reel. The controller is free to assume some other operation with a different tape handler. Further Rewind Unload operations with the tape handler are impossible until the tape is manually reloaded.



* INTERNAL REJECT BY COMPUTER AFTER 100μ SEC.

Figure 2-17. Skip Bad Spot

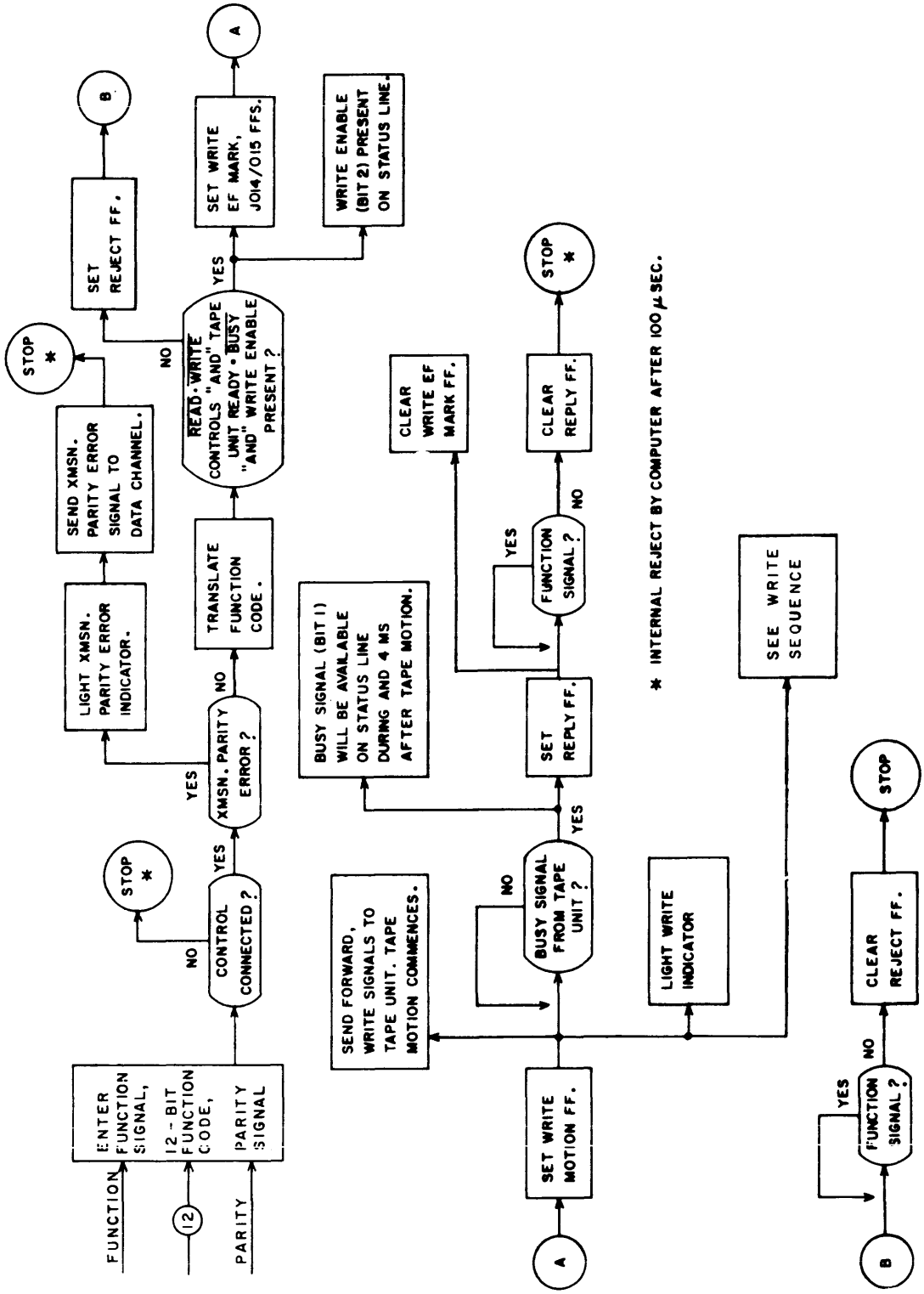


Figure 2-19. Write File Mark.

WRITE SEQUENCE FOR WRITE FILE MARK

Set Z022 (Write Control)
Drop Clear W_1 signal
Drop End of Record Clear signal (F002 to "0")
Set Z010 (R to 0)
Drop Clear 0 signal (0 Register Clear)
Block R to 0 Transfer (D123 to W095 to "0")

Set Z012 (Write Resync)

Time 0 Set Z014 (Write Gate)
Time 1 W_1 to W_2
DK_1 to DK_2 (S S)
Time 1-3 0 -- B not needed
D123 to B to 17_8
Time 2-3 Gate B to W (17_8 to W_1)
Time 3 Set Z008 (Sprocket)
Clear J014 (Write FM)
Time 5 Advance DK (C S)
Set Z000 (Initiate Check Character)
Time 7 Clear Z008 (Sprocket)
Clear Z012 (Write Resync)
Clear Z014 (Write Gate)

Miss Three Frames

The Check Character Counter is progressed by the Timing Chain.

Write Check Character

Time 1 Clear Z002 (S C C S)
Clear W_1 (Signal)
Set Z030 (Write Term I)
Time 3 Set Z008 (Sprocket)
Time 7 Clear Z008 (Sprocket)
Clear Z000 Initiate Check Character)

Set Z032 Write Term II
Clear Z030 (Write Term I)
Clear Z020 (Write Motion)
(Drop Fwd Signal)
Clear Z022 (Write Control)
(Drop Write Enable signal)
End of Record Clear signal F002 to "1"
Clear Z032 (Write Term II)

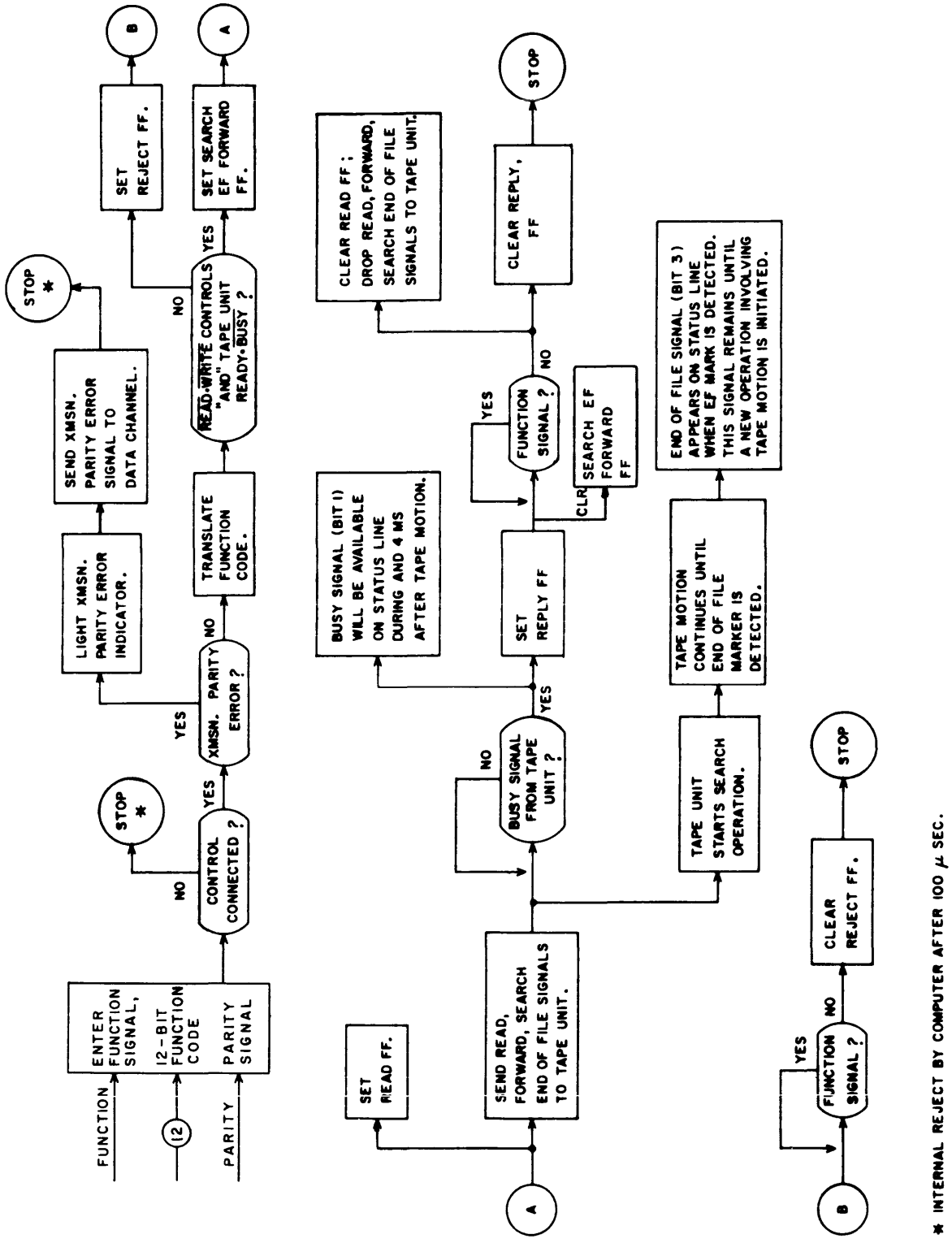


Figure 2-20. Search Forward to File Mark.

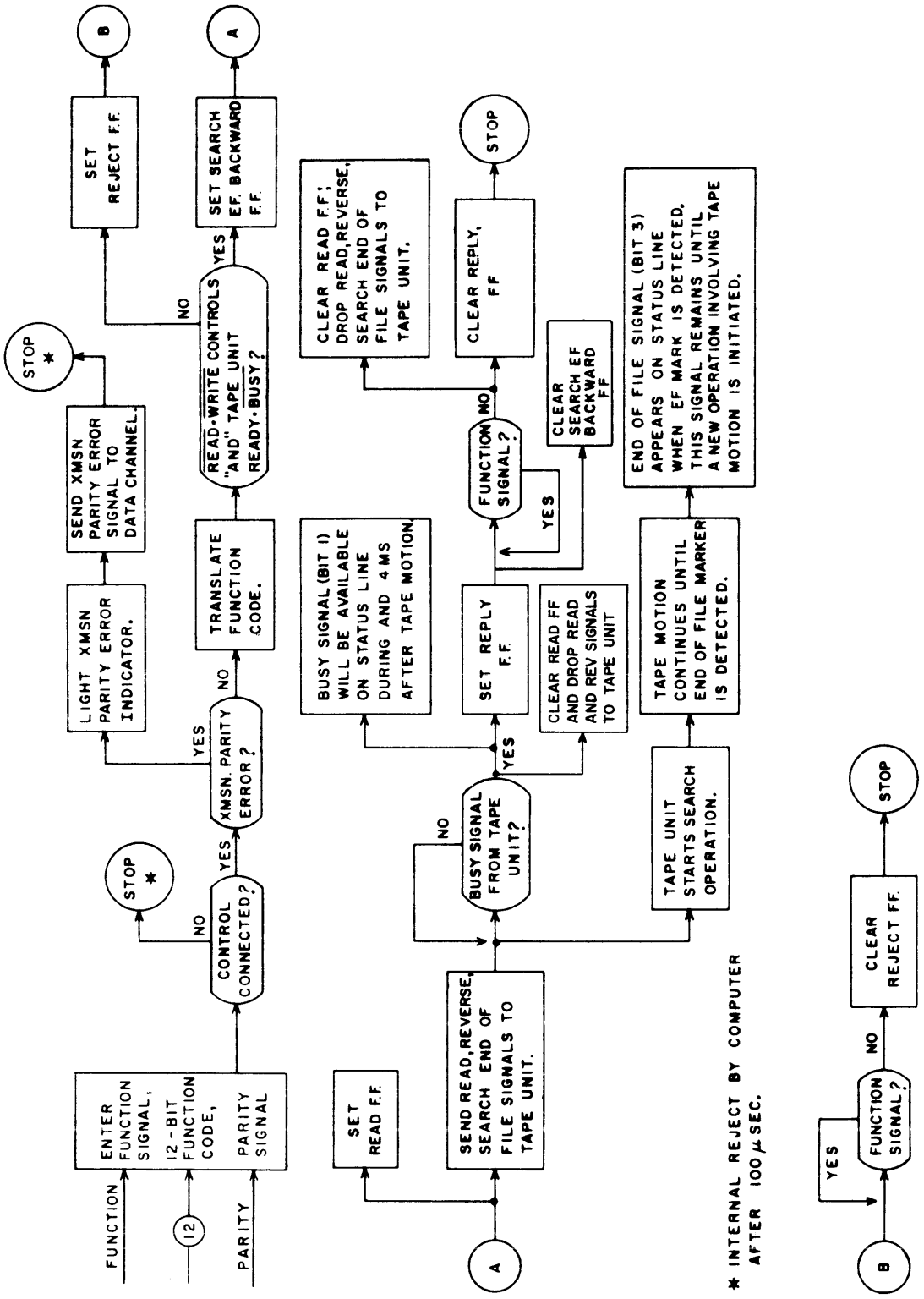


Figure 2-21. Search Backward to File Mark.

Figure 2-22. Backspace.

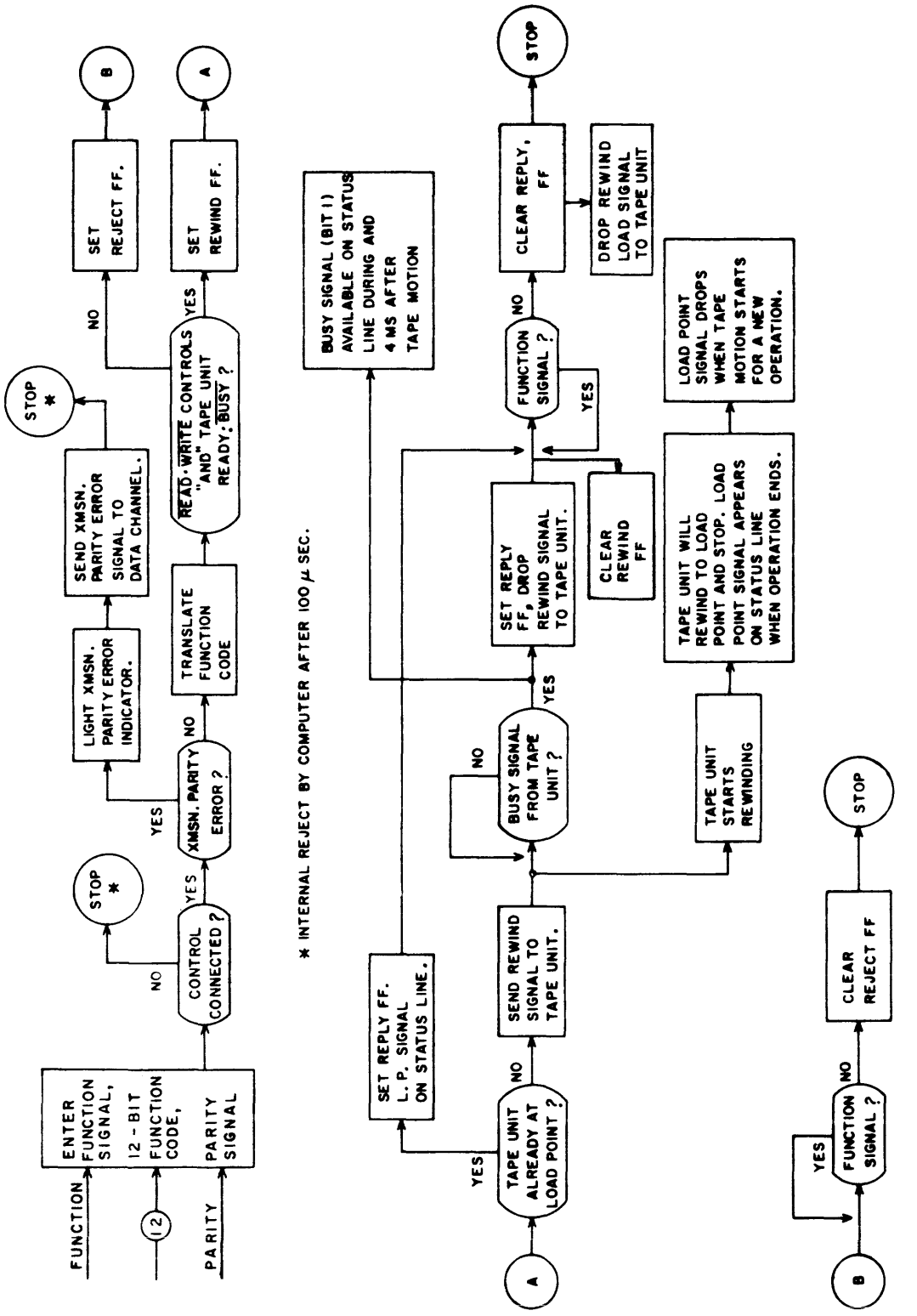


Figure 2-23. Rewind.

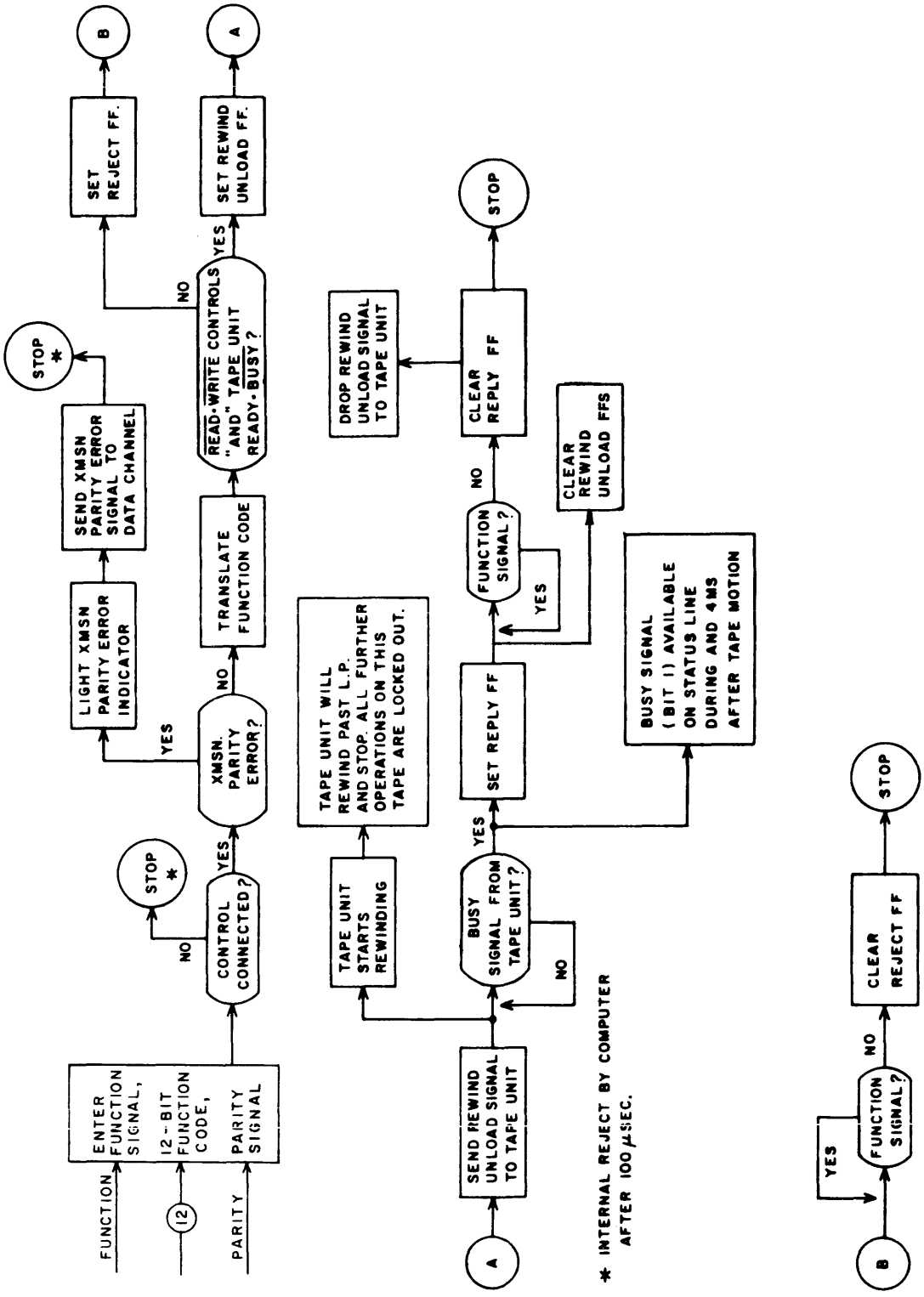


Figure 2-24. Rewind Unload.

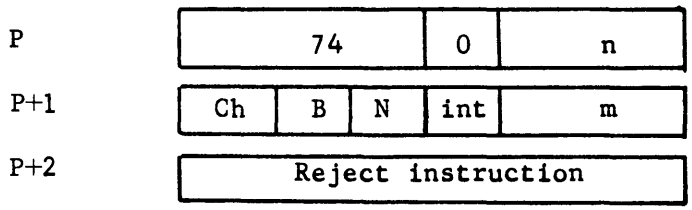
READ OPERATION

During a Read operation, the controller modifies and synchronizes data as it passes from the tape handler to the Data Channel. The modification is performed as the data passes through the appropriate registers in the controller. The "internal register transfer" and synchronization are controlled by timing elements within the controller. The timing elements are activated by signals from the handler and the Channel.

In the Read operation, an amount of information is called for by allocating a specific area of memory into which the data can be stored. The Read signal is produced in Block Control and placed on the Channel, thereby conditioning the controller. The controller produces a Forward signal which moves tape in the transport. A Data signal is produced for each 12-bit byte of data from the controller.

The tape transport, upon receiving the Forward signal, moves the tape under the read head. Each 6-bit data frame and its parity bit is detected and returned to the controller, accompanied by the Sprocket signal. When the record is complete, tape stops with the read head in the Record Gap.

PROGRAM CONSIDERATION



n - last word address plus one 17 bits
m - first word address
B - "1" indicates backward storage
N - "1" for no assembly, "0" for 12 to 24 assembly
int - interrupt upon completion
Ch - channel

As the instruction at P is read. Main Control recognizes it as a Block Control instruction requiring the information from P+1 to be complete. Accordingly, the contents of P+1 will also be read up.

A Reject will occur in the channel on which this operation is directed, if the controller is still busy with the previously-initiated operation. The instruction from P and P+1 will be elaborated and the Reject instruction from P+2 will be read and executed.

If the channel is not busy and no Reject indicated, Main Control proceeds in the main program by reading and executing the next instruction from P+3.

Block Control simultaneously processes the I/O instruction.

Within Block Control, the 74.0 is translated and a Read signal (R016, page 3-1), Data signal (R015), and Channel Busy signal (R020) are placed on the designated channel.

NOTE

Page references are to the controller diagrams. Use the Read Operation Flow Diagram while reading the text.

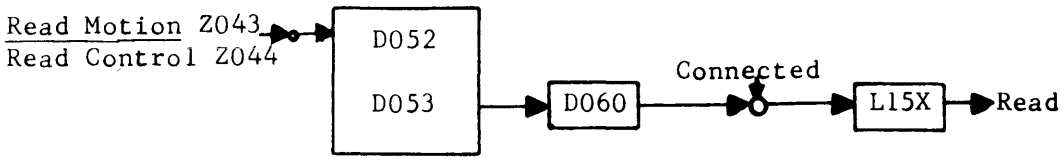
READ SIGNAL

The Read signal enters the controller (R016, page 3-1) with the Data signal (R015) and initiages a Read Operation. Certain conditions must be satisfied for the Read operation to proceed.

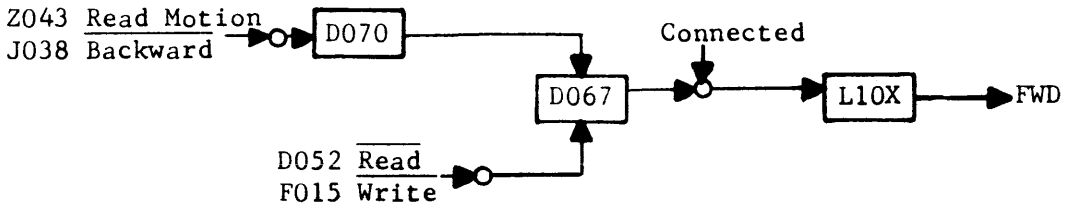
1. The controller must be connected (I118, page 3-3).
2. Interrupts from a previous operation must have been cleared (J036, page 3-7)
3. Lost data, from a previous operation, must have been cleared (Z070/071, page 3-9).
4. The connected transport must be returning a Ready Reply (D004, page 3-25).
5. The Read Data Lockout FF must be set (Z041, page 3-15).
6. The connected transport must have tape stopped and be returning a Not Busy Reply (D010) forcing the network on page 3-25 into proper condition for a read (I134, page 3-11); exception: non-stop read.

The conditions, if satisfied, set Z042/043 (Read Motion FF) and prepare the controller for read.

1. Start Tape Motion--as Read Motion sets, the Read FF (page 3-23) is set, sending the Read Request signal to the connected transport. The



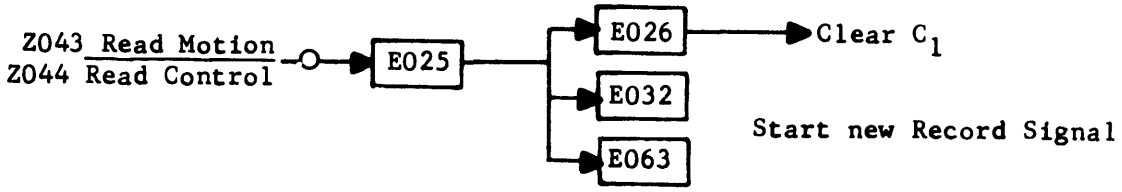
conditions are correct to send a Forward Request signal to the transport.



The Read Forward Conditioning FF (K120, page 3-11) would be set.

2. Start New Record

The same terms as used to set Read are used to establish the required circuits for the new operation.



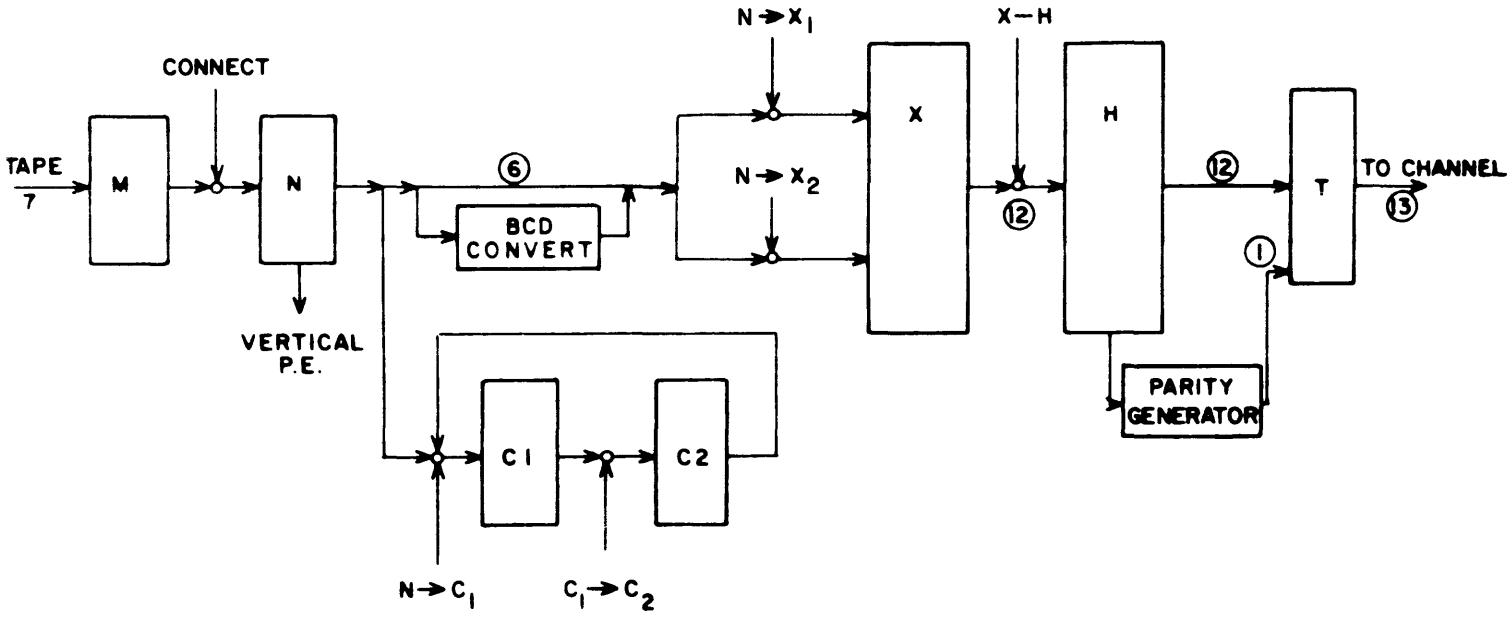
1. Clear AK_1 (Z064/065, page 3-15)
2. Clear Z092/093 (Enable AK Counter. (page 3-15).
3. Clear Z076/077 (End of Record II, (page 3-15).
4. Clear C_1 Register (page 3-21).
5. Clear Read and Write Conditioning FFs (page 3-11).

Set Z044/045 (Read Control) after a 10 usec delay. The Start New Record pulse is removed, leaving the C register and the AK Counter clear. At the same time, the Read/Write Active signal comes up,

the Begin Record I and II FFs are cleared, and the Reply Timing Chain is enabled to respond to sprockets being returned from the transport.

The controller is conditioned to accept frames from the transport, assemble frames into bytes and send the byte to the channel. Tape motion was initiated when Read Motion (Z042/043) set. As the tape moves, the first frame appearing under the Read Head is processed back to the controller. A Read Sprocket accompanies the data to indicate the presence of the frame on the line. This sprocket provides timing needed to process the frames into a data word and pass it through the controller. The Data signal (R015) is present, demanding a word to be supplied to the Channel.

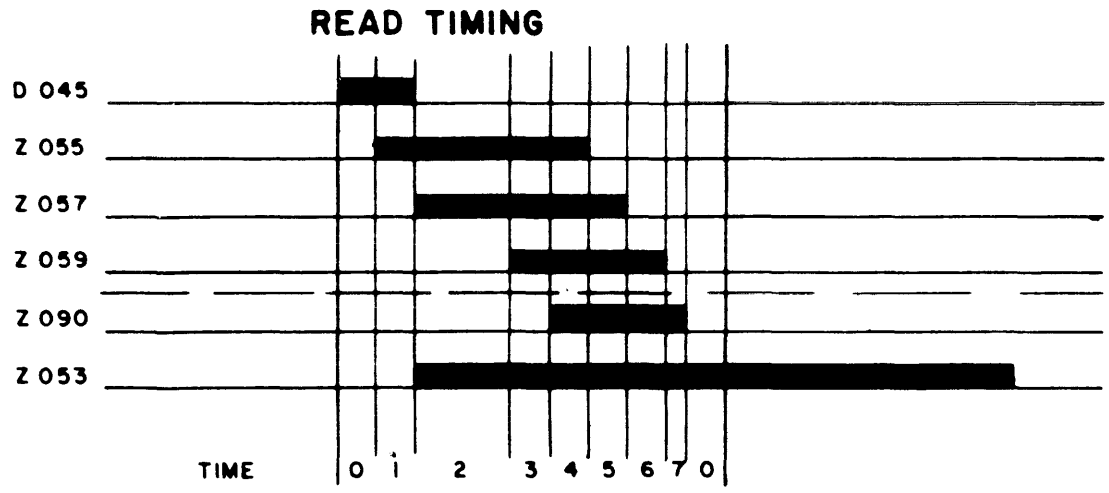
The path of data through the controller is shown in the following illustration:



READ SPROCKET

As the Read Sprocket appears from the transport, D042 (p. 3-27) or D044 goes to a zero, forcing D045 (p. 3-15) to a logical "1". This starts a pass through the timing chain.

The pass through the chain can be translated into times for convenience of explanation. A diagram of the timing chain with time translation would be:

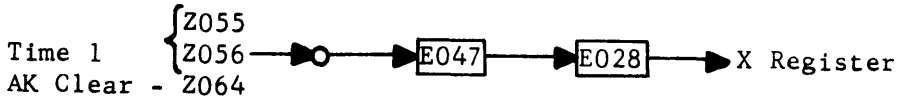


At time 2, the Reply Timing Chain Lockout FF sets. With this FF set, the timing chain will complete its pass, but will be unable to begin another. When the Sprocket signal ends, a delay will be initiated to clear the Reply Timing Lockout FF. The delay time depends upon the density selected. Clearing the flip-flop will allow the timing chain to start on the next read sprocket. Each sprocket received causes one pass through the timing chain, processing the frame into the word for return to the channel.

ASSEMBLY COUNTER CLEAR

The frame is available on the M cards (p. 3-17). It is passed through the N inverters and undergoes a vertical parity check (P. 3-19) as the sprocket starts a timing pass. The Assembly Counter (AK_1) is clear.

At Time 1, the X Register is cleared to receive the frame:



The C_1 Register is transferred to the C_2 Register, causing them to be the same or equalized.

The AK_1 rank, which is clear, is transferred to rank 2, causing both ranks to be clear.

If this is the very first frame of the record:

Clear Z040/041 (Read Data Lockout) which was left set by the Read signal entering. This removes the constant clear that has been on the H Register, and the Read operation can proceed.

The Read FF (D052/053, page 3-23) which was set when Read Motion set, has been holding a Read and a Forward signal to the Transport. The required movement of tape is in process, as evidenced by the receipt of this first frame. The transport is so designed that if no new frame is read, tape motion will stop. The Read and Forward signals are no longer needed. At time 1, the Read FF is cleared and the signals will drop.

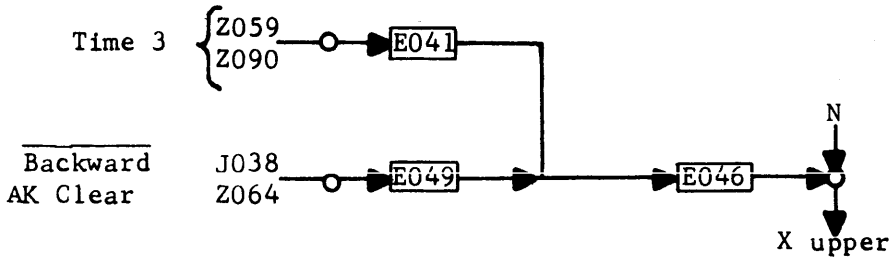
At Time 2---

Set Z052/053 (Reply Timing Chain Lockout FF), disabling D045. This prevents a random pulse from initiating a second start down the timing chain.

If this is the first frame of a new record, set Z060/061 (Begin Record I FF).

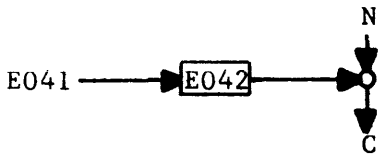
At Time 3 ---

Transfer the six information bits from the frame into the X register. The X register is twelve bits in size, and this transfer must be to the upper six bits of X, to be properly assembled. The condition of the AK counter, presently clear, causes this assembly to occur:



The information received has, at this time, passed through the parity checker, and vertical parity will be checked. A parity error will cause the Vertical Parity Error F (P050/051) to set. The error conditions are those that were discussed in Read Reply during Write.

The entire 7-bit frame is transferred into the C_1 Register to be retained for a longitudinal parity error check after the entire record has been read.



At Time 6 ---

Advance the AK counter in preparation for the next frame to arrive. The AK_2 will be clear. The set condition of AK_1 will assure movement of the next frame into X lower.

ASSEMBLY COUNTER ODD

The first sequence will be finished. Time 0 will come up and exist until another sprocket arrives from the transport, starting another timing pass, and processing another frame. This pass starts with the AK counter set.

At Time 1 ---

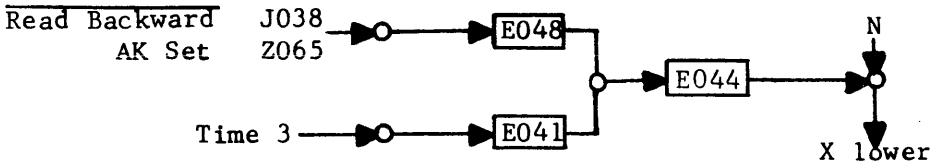
Equalize the C_1 and C_2 Registers
Equalize the AK counter (both set)
If this is the 2nd frame of a new record, set Z062/063 and begin Record II

At Time 2 ---

Set Z052/053 (Reply Timing Chain Lockout)

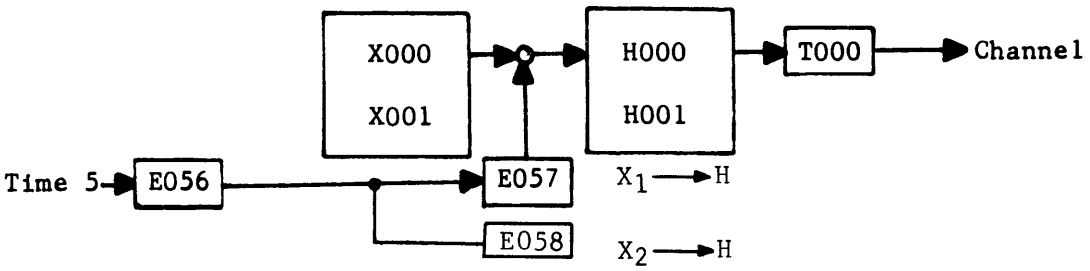
At Time 3 ---

Transfer the frame from N to C_1 and check vertical parity for error. Transfer the six information bits of the frame into X lower. The condition of AK_1 will determine the transfer to the proper part of the X Register.



At Time 5 ---

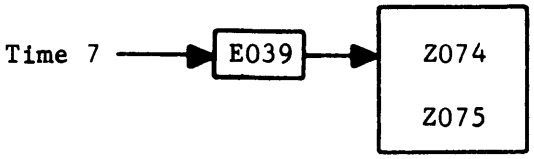
The contents of the X register transfer to the H register. At this time the X register will be holding a full 12-bit byte. Whatever is transferred into H will be felt on the transmitter cards and will be on the channel.



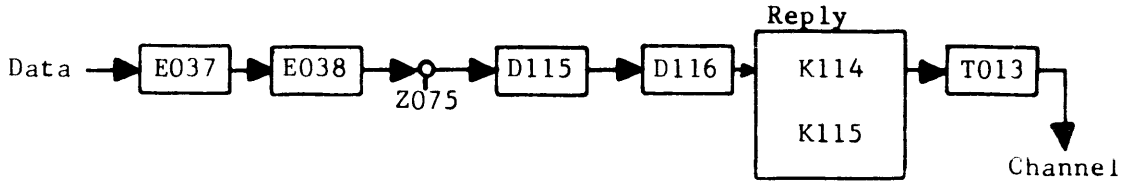
The enabling term, E057, will also set the Hold FF (Z094/095). This flip-flop is used to detect a Lost Data condition.

At Time 7 ---

Two frames from the transport have been assembled in X, transferred into H, and placed on-line to the channel along with a transmission parity bit from the parity generator. A Reply to the channel is needed for the data on-line to be accepted. At time 7, the final inputs are correct and the Read Ready FF is set.



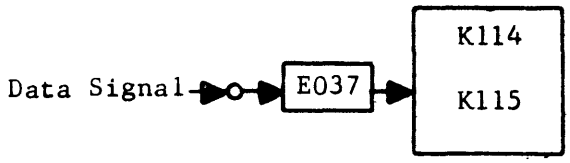
The Data signal and Read Ready going set produce the Reply.



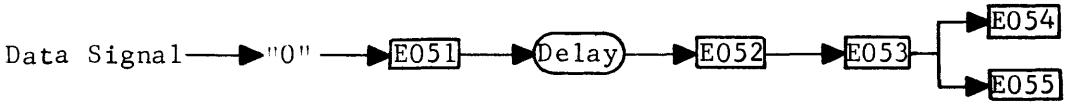
The Reply FF going set will clear Z074/075 (Read Ready FF).

A Reply to the channel will cause block control to accept the word, store it in memory, and drop the Data signal.

The absence of R015 (Data signal) causes the Reply FF to clear along with



the H Register in preparation for the next byte (2 frames) assembled from the transport, unless the Read signal also drops, indicating the



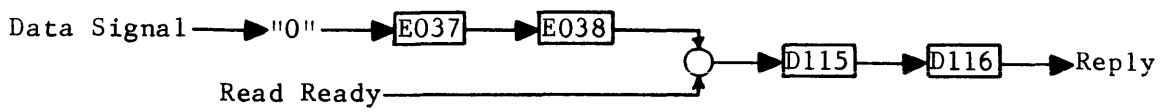
the block of input has been satisfied. In this event the operation is terminated.

If a new data signal arrives, another word must be assembled and furnished to the channel. The sequences specified are repeated.

LOST DATA

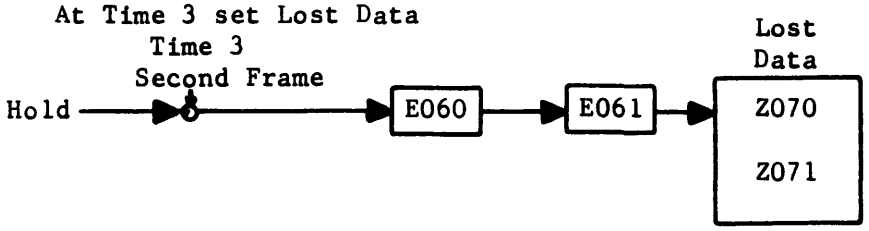
If the Read signal is still up (indicating the block of input data required has not yet been satisfied) and the Data signal is not present, a Lost Data situation will occur.

With the absence of the Data signal, a new sprocket will arrive, loading X upper and the timing from this sprocket ends. Another sprocket and frame cause a second pass of timing as this frame is loaded into X lower. At time 5, however, the Hold FF was set as the assembled byte is transferred into H. At time 7, the Read Ready FF sets. At this, point the required reply cannot be sent because the Data signal is absent, and the Clear H



term (E055) remains a "0", retaining a word in H.

A third sprocket will arrive, loading X upper. A fourth sprocket will arrive, loading X lower at time 3. If at this instant the Data signal has not arrived, Lost Data will have occurred, since the contents of H (first byte) will be garbled by having the second word, now in X, forced in on top of the first word in H.



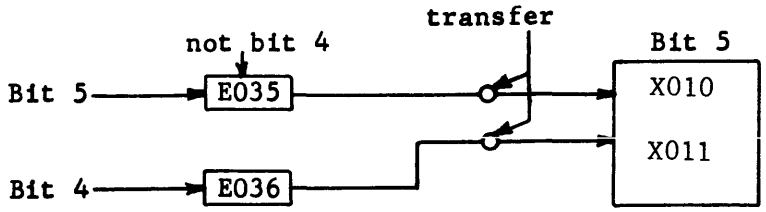
Clear the Read Ready FF
Set Z072/073 (End of Record Disconnect)

An End of Record signal is returned to the channel, causing the Read Signal to drop and the terminate sequence to proceed.

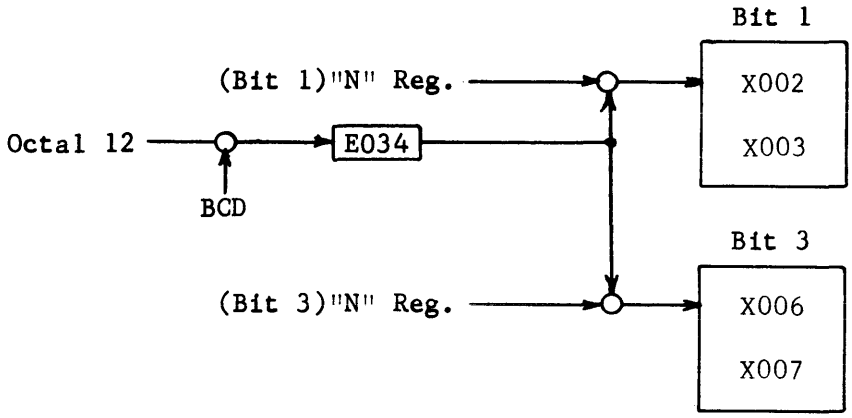
EXTERNAL TO INTERNAL BCD CONVERSION

During binary or BCD mode, if Negate BCD conversion is selected, data passing through the X Register will not be affected.

External BCD data, which must be changed to internal BCD, will be converted as it enters the X Register. The bit 5 flip-flop will set if bit 4 is present ("1") and bit 5 is absent ("0"). This fulfills the rule: If bit 4 is present complement bit 5. The bit 5 flip-flop will also set if bit 5 is present and bit 4 is absent.



The external BCD code of an octal 12 must be converted to an internal BCD code of 00. This can be accomplished by detecting the presence of an octal 12 and preventing bit 1 and bit 3 flip-flops from setting.



TERMINATE

The Terminate sequence can be entered for three reasons:

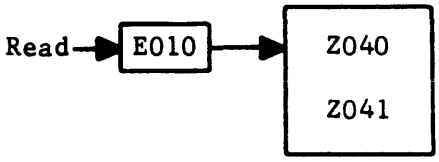
1. Read signal and Data signal removed from the channel, indicating the input block of data required by the program has been satisfied. If the programmer knows the exact size of the record on this tape, the removal of read and data signals will coincide with the entry of the read head into the record gap and the record is equal to the requested block. If the programmer asked for an input which is less than record size, the Read and Data signals drop in advance of the record gap. It is then possible for many frames to remain. These frames will be read but not transferred to the channel.

2. The programmer asked for more data than the record contains. No new sprockets form the transport indicates the recod gap has been detected.

3. Lost Data has occurred and nothing more will be returned to the channel.

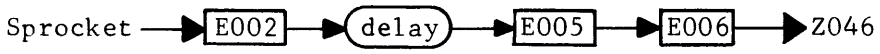
Record Equal to Requested Block

If the read and data signals are removed just as the Check Character gap is entered, set Z040/041 (Read Data Lockout FF) at the time the Read signal drops.



This action will hold the H Register clear and the Check Character, which

is about to be read, cannot be returned to the channel. The read head, being in the Check Character gap, does not detect a new frame and no new sprocket can be returned by the transport to the controller. The sprocket will be absent during a period of time during which three sprockets could have occurred, causing Z046/047 (End of Record I) to be set.



A sprocket will appear when the Check Character is read; however, Read Data Lockout and End of Record I are holding H clear. The resulting timing pass, as the Check Character is read, puts the Check Character into the C Register, but not back to the channel. When the transport's read head enters the record gap, a sufficient number of missing frames will stop tape motion and return an End of Record signal to the controller. The signal causes the End of Record II FF to set and the controller to revert to a static condition, ready to respond to a new operation instruction.

End of Record II enables the set output of read control to clear read motion and, after a delay, to clear read control.

The AND gate into E019 is broken, causing the output to go to a logical "1", clearing Z060/061 (Begin Record I and II). The logical "1" is inverted through E021 (the Read/Write Active inverter), disabling further passes through the timing chain.

Record Greater Than Requested Block

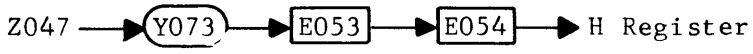
If the Read and Data signals drop, indicating the block required has been satisfied, the Read Data Lockout FF (Z040/041) will set, holding the H Register clear.

Sprockets will continue to appear as each frame is read, each sprocket starting a timing pass. While no data is being returned to the channel, vertical parity is being checked on the unused frames and each frame goes to the C Register. When the record gap is detected, Z046/047 (End of Record I) sets, blocking a check of the vertical parity of the Check Character. As the Check Character is read, another pass through the timing chain places

the Check Character into the C_1 Register. The End of Record is now returned from the transport and the tape stops with the recording heads in the record gap. This signal enables setting of Z076/077 (End of Record II). Read Motion clears, which drops the Read/Write Active signal and clears Begin Record I and II.

Record Smaller Than Requested Block

If the programmer is not sure of the record size, but does want all of the record, he may designate a memory block larger than the record could be. In this event, the sprockets fail to appear in the Check Character gap, setting End of Record while the Read and Data signals are still present. End of Record I holds the H Register clear.



If the End of Record I FF is set when the Read Data Lockout FF is still clear, the End of Record Disconnect FF (Z072/073) will set, thereby returning the disconnect to the channel. The disconnect clears Read and Data signals and terminate the input. As the Data signal drops, the End of Record FF will be cleared. The Check Character is read and the controller is conditioned to static state upon receipt of the End of Record signal from the transport.

Lost Data

This is terminated in a manner similar to small record. H is held clear by the absence of the Data signal. As the Lost Data FF sets, the End of Record Disconnect FF also sets. The Disconnect will drop the Read and Data signals. The remainder of the record will be read. Detection of the Check Character gap sets EOR I. The End of Record signal from the transport allows EOR II to set and normal clearing of the controller results.

NON-STOP READ

The Read operation is terminated by the tape transport. When the record gap is sensed, an End of Record signal is sent to the controller. This sets the End of Record II FF. The Read Motion FF clears, clearing the Read Control FF 1 usec later. If a new Read signal is present, the Read Motion FF can re-set. New Forward and Read signals will be sent to the transport to the set input of the Forward FF. This setting signal will remain until the first frame of the next record is read -- read time 1 clears the Read FF (D052/053, p. 3-23). The End of Record signal is 10 usec in duration. When this signal drops, a pulse attempts to clear the Forward FF. Since the set input is held longer than the clear, the Forward FF remains set causing vacuum to be applied to the forward capstan

continuously. Tape does not stop between the two records.

A CONDENSED SEQUENCE FOR READ OPERATION

```
Set Z042/043 (Read Motion FF)
     Sets D052/053 (Read FF)
         Send Read and Forward signal to transport
     Clear C1 Register
     Start new record
         Clear J040/041 (Channel Busy FF)
         Clear P054/055 (Longitudinal PE)
         Clear P050/051 (Vertical PE)
         Clear Z076/077 (End of Record II)
         Clear Z092/093 (AK Enable)
         Clear Z064/065 (AK I)

Set Z044/045 (Read Control FF)
     Read/Write Active signal

Sprocket from transport starts timing chain
```

Odd Frame

```
     Time 1 -- Clear X
               C1 to C2
               AK1 to AK2
                  (1st frame only)
                    Clear Z040/041 (Read Data Lockout)
                    Clear D052/053 (Read FF)
                        Drop Read and FWD signal

     Time 2 -- Set Z052/053 (Reply Timing Chain Lockout
               (1st frame only)
                  Set Z060/061 (Begin Record I FF)

     Time 3 -- N to C1
               N to X2
               Check Vertical Parity

     Time 6 -- Advance AK
```

Even Frame

```
     Time 1 -- Block Clear X
               C1 to C2
               AK1 to AK2
                  (second frame only)
                     Set Z062/063 (Begin Record II)
```

Time 2 -- Set Z052/053 (Reply Timing Chain Lockout)

Time 3 -- N to C_1
N to X_1
Check Vertical Parity

Time 5 -- X to H

Time 6 -- Advance AK

Time 7 -- Set Z074/075 (Read Ready)
Sets K114/115 (Reply)
Clear Z074/075 (Read Ready)
Reply knocks down data signal
Clear K114/115 (Reply)
Clear H Register

Next sprocket starts through odd-frame sequence again.

TERMINATE

E002 goes to "1" between frames
E002 expends delay in Check Character Gap
Sets Z046/047 (End of Record I)
Read and Data signal drops
Sets Z040/041 (Read Data Lockout)
Hold H clear
Read Check Character
Sprocket starts timing
Time 1 -- Clear X
C_1 to C_2
Time 3 -- N to C_1
N to X

End of Record signal from Transport
Check longitudinal parity
Set Z076/077 (End of Record II)
Drop Read/Write Active signal
Clear Begin Record I and II
Clear Z046/047 (End of Record I)
Clear Z042/043 (Read Motion)
Clear Z044/045 (Read Control)

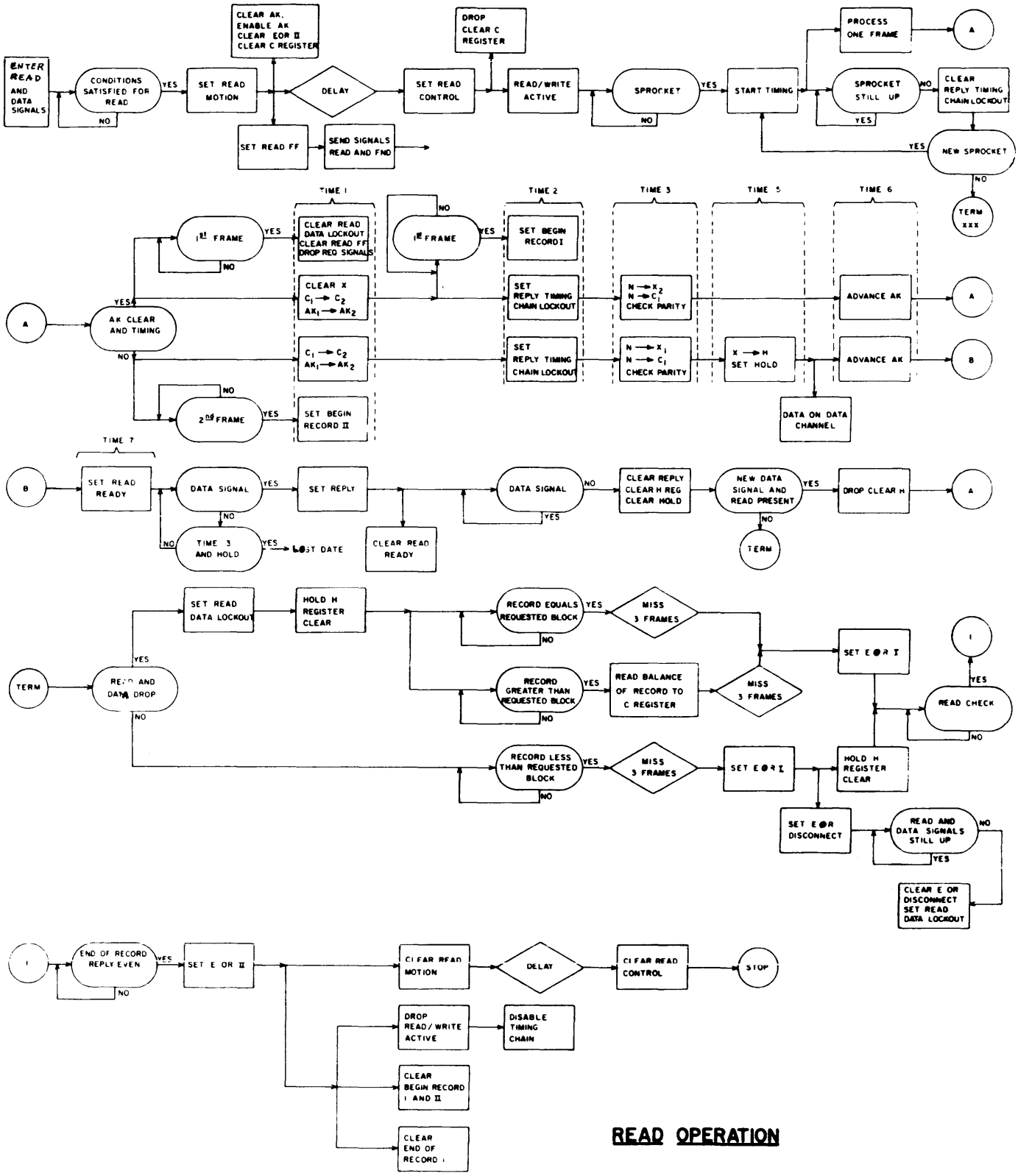
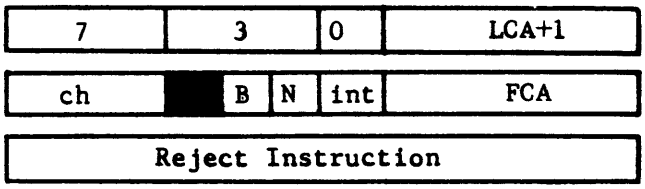

ENTER READ AND DATA SIGNALS
CONDITIONS SATISFIED FOR READ
YES
NO
SET READ MOTION
CLEAR AK, ENABLE AK CLEAR EOR II CLEAR C REGISTER
DELAY
SET READ FF
SEND SIGNALS READ AND FND
SET READ CONTROL
DROP CLEAR C REGISTER
READ/WRITE ACTIVE
SPROCKET
START TIMING
PROCESS ONE FRAME
A
SPROCKET STILL UP
CLEAR REPLY TIMING CHAIN LOCKOUT
NEW SPROCKET
TERM XXX
TIME 1
TIME 2
TIME 3
TIME 5
TIME 6
1ST FRAME
CLEAR READ DATA LOCKOUT CLEAR READ FF DROP REQ SIGNALS
1ST FRAME
SET BEGIN RECORD I
CLEAR X C1 → C2 AK1 → AK2
SET REPLY TIMING CHAIN LOCKOUT
N → X2 N → C1 CHECK PARITY
ADVANCE AK
A
AK CLEAR AND TIMING
C1 → C2 AK1 → AK2
SET REPLY TIMING CHAIN LOCKOUT
N → X1 N → C1 CHECK PARITY
X → H SET HOLD
ADVANCE AK
B
2ND FRAME
SET BEGIN RECORD II
DATA ON DATA CHANNEL
TIME 7
B
SET READ READY
DATA SIGNAL
SET REPLY
DATA SIGNAL
CLEAR REPLY CLEAR H REG CLEAR HOLD
NEW DATA SIGNAL AND READ PRESENT
DROP CLEAR H
A
TIME 3 AND HOLD
LOST DATE
CLEAR READ READY
TERM
SET READ DATA LOCKOUT
HOLD H REGISTER CLEAR
RECORD EQUALS REQUESTED BLOCK
MISS 3 FRAMES
SET E OR I
I
TERM
READ AND DATA DROP
RECORD GREATER THAN REQUESTED BLOCK
READ BALANCE OF RECORD TO C REGISTER
MISS 3 FRAMES
READ CHECK
RECORD LESS THAN REQUESTED BLOCK
MISS 3 FRAMES
SET E OR I
HOLD H REGISTER CLEAR
SET E OR DISCONNECT
READ AND DATA SIGNALS STILL UP
CLEAR E OR DISCONNECT SET READ DATA LOCKOUT
I
END OF RECORD REPLY EVEN
SET E OR II
CLEAR READ MOTION
DELAY
CLEAR READ CONTROL
STOP
DROP READ/WRITE ACTIVE
DISABLE TIMING CHAIN
CLEAR BEGIN RECORD I AND II
CLEAR END OF RECORD I
READ OPERATION

Figure 2-25

READ OPERATION

(6 bit)

PROGRAM FOR READ CHARACTER



This program causes the Read signal (R016), Suppress AD signal (R022), and the Data signal (R015) to appear on-line.

1. Set J046/047 (Suppress AD)
   Disable AK advance (Stays Clear)
2. Initiation of Read Circuits and Tape Motion

SPROCKET STARTS TIMING

Time 1 Clear X
C_1 to C_2
(1st Frame only)
Clear Z040/041 (Read Data Lockout)
Clear D052/053 (Read)
Drop Fwd and Read signals to transport

Time 2 Set Z052/053 (Reply Timing Chain Lockout)
(1st Frame only)
Sets Z060/061 (Begin Record I)

Time 3 N to 0_1
N to X_1 lower

Time 5 X to H
Set Z094/095 (Hold)

Time 7 Set Z074/075 (Read Ready)
Set K114/115 (Reply)

Reply signal causes Data signal to drop
Clear K114/115 (Reply)
Clear H Register
Clear Z094/095 (Hold)

If the record had been written in character output, it should be read in character.

If a record, written in character output with an odd number of frames is read in word input, there will be no frame to load X lower on the last byte. An automatic timing pass will occur as the Check Character gap is detected, loading X lower with zeros, thereby permitting the Reply and Transfer.

REVERSE READ

FUNCTION - REVERSE

P	7 7 . 1 Ch	0041
P+1	Reject Instruction	

PROGRAM - READ

The Read signal and Data signal are on-line.

1. Set Z042/043 (Read Motion)
   Set D052/053 (Read)
   Send Read to transport
   Send Reverse to transport
   Set K122/123 (Read Reverse)
   Send Read Backward to the Channel

   Start New Record signal

   Set Z044/045 (Read Control)
   Read/Write Active (E021) comes up.

2. Tape Moving Backward
   a. Sprocket starts timing (Check Character)

      Time 1 Clear X
      C_1 to C_2
      AK_1 to AK_2 (C C)
      (1st Frame only)
      Clear Z040/041 (Read Data Lockout)
      Clear D052/053 (Read)
      Drop Read and Reverse signals

      Time 2 Set Z052/053 (Reply Timing Chain Lockout)

(1st Frame only)
Set Z060/061 (Begin Record I)

Time 3 N to C_1
N to X lower

Time 6 Advance AK (S C)

3. Detect Check Character Gap
(E002 to Y038 to E005 to "0")
Re-establish Circuit (E005 to E008 to "1")
Clear AK_1 (C C)
Clear X (Check Character retained in C Register)
Clear Vert Parity Error FF

4. Assemble

Sprocket - Start Timing (Last frame in the record).

Time 1 Clear X
C_1 to C_2
AK_1 to AK_2
(Set Z062/063, Begin Record II, 2nd Frame)

Time 2 Set Z052/053 (Reply Timing Chain Lockout)

Time 3 N to C
N to X lower

Time 6 Advance AK (S C)

SPROCKET START TIMING

Time 1 Block Clear X
C_1 to C_2
AK_1 to AK_2 (S S)

Time 2 Set Z052/053 (Reply Timing Chain Lockout)

Time 3 N to C_1
N to X upper

Time 5 X to H
Set Z094/095 (Hold)

Time 6 Advance AK (C S)

Time 7 Set Z074/075 (Read Ready)
Set K114/115 (Reply)

Start termination in record gap which looks like the Check Character gap, causing Z046/047 (End of Record) to Set.

INTERRUPT

In the 3000 Computer Systems, Block Control is dependent upon Main Control for initiation of operations. Once initiated, however, Block Control and Main Control each proceed concurrently with their separate operations.

The interrupt scheme of the system is such as to keep Block Control in as near a continuous operation as is possible with the much slower peripheral equipment. The Interrupt notifies Main Control that the previously-initiated operation in Block Control is finished and requires re-initiation. Proper utilization of the Interrupt results in a time savings and increased efficiency of the system.

In the magnetic tape system, there are three reasons for interrupt to occur and have the Block Control re-initiated.

1. When the tape system becomes Ready and is not Busy.
2. When a previously-initiated operation is properly ended.
3. When a previously-initiated operation is abnormally ended.

A brief review of the Interrupt Sequence and its use is:

1. Condition controller to interrupt on End of Operation.
2. Initiate an Output to Tape of a Block of Data.
3. Main Control enters the Interrupt Sequence which will:
    a. Place the address of the next unexecuted instruction of the Main program in ML 00004.
    b. Identify the source of the Interrupt in the lower 12 bits of ML00055.
    c. ML00005 directs control to the address of a subroutine to precess the Interrupt. The subroutine must accomplish the following:
        1. Clear the Interrupt
        2. Re-initiate Block Control
        3. Re-enable Interrupt System
        4. Jump back to the next unexecuted instruction in Main Control

There are eight lines in the I/O Control cable over which the Interrupt signal returns to the channel. Each controller will use a separate line corresponding to the position of the Equipment Selection switch. In this manner the channel and line produce the identification required for ML00005 in the Interrupt sequence.

Interrupt, as it pertains to the magnetic tape system, must then be discussed in two sections:
1. Selecting, by a Function Operation, a condition to cause the interrupt.
2. The detection of the condition to produce the interrupt.

FUNCTION - SELECT (OR RELEASE) INTERRUPT CONDITION

The object of this function is to set or clear one of the three Interrupt Conditioning FFs (p. 3-7), and to recognize or detect one of many possible conditions, when it does occur. By examination, it can be determined there are six inputs, two to each of the three Conditioning FFs with each input enabled by a different Function Code. The codes used to condition these FFs then are:

INTERRUPT			
0020	Interrupt on Ready and Not Busy	0021	Release Interrupt on Ready and Not Busy
0022	Interrupt on End of Operation	0023	Release Interrupt on End of Operation
0024	Interrupt on Abnormal End of Operation	0025	Release Interrupt on Abnormal End of Operation

A Program for the function would be

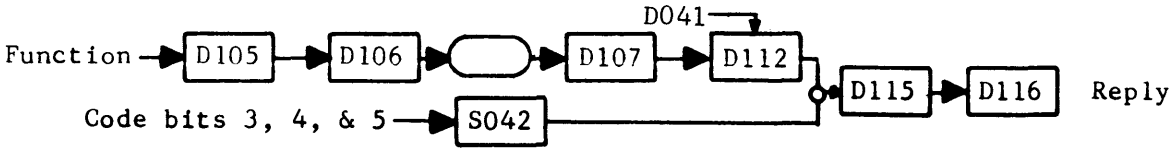
77.1	ch	code

Reject Instruction

Block Control detecting instruction, 77.1, places a Function signal, the 12-bit Function Code and the Transmission Parity on the channel.

In the connected controller, the Function signal (p. 3-7) enables the translation of the second octal number, producing the 2X translation (S042 - p. 3-7). The lowest octal bit is translated on page 3-3. The two translation AND to produce one of the six possible inputs to the Condition FFs (p. 3-7).

A Reply is returned to the channel immediately as a result of the 2X translation of bits 3, 4 and 5. The path of the Reply is:



The Reply causes the Function signal and Code to be removed from the channel clearing the Reply FF and ending the Operation.

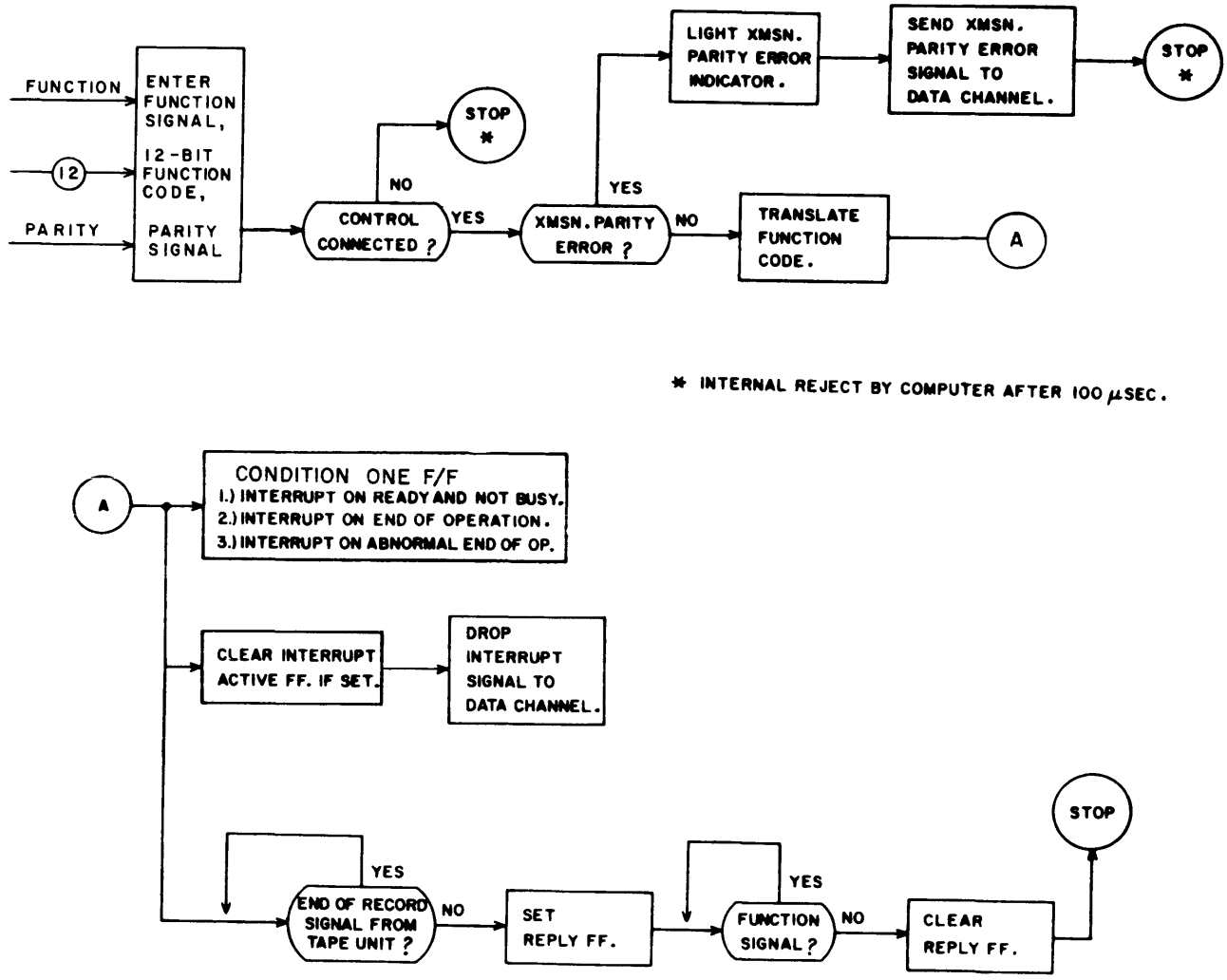


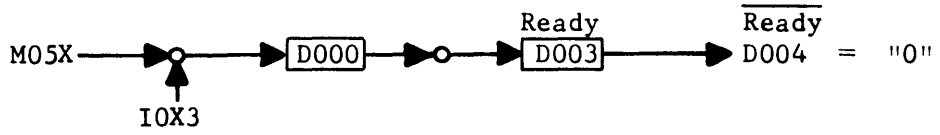
Figure 2-26. Select Interrupt Condition

The Interrupt signal is produced by detecting one of many possible conditions, as it occurs within the tape system. These possible conditions are characterized by the type of interrupt selected and are grouped in the three specific categories.

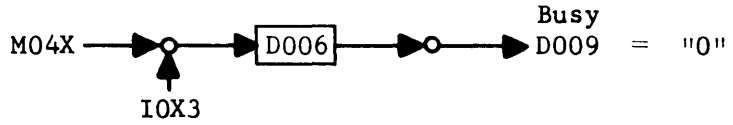
Interrupt on Ready and Not Busy

The Interrupt FF (J034/035) will set when inverter D103 becomes a logical "1", enabling the AND gate at the set output of J028/029 (Interrupt on Ready and Not Busy FF).

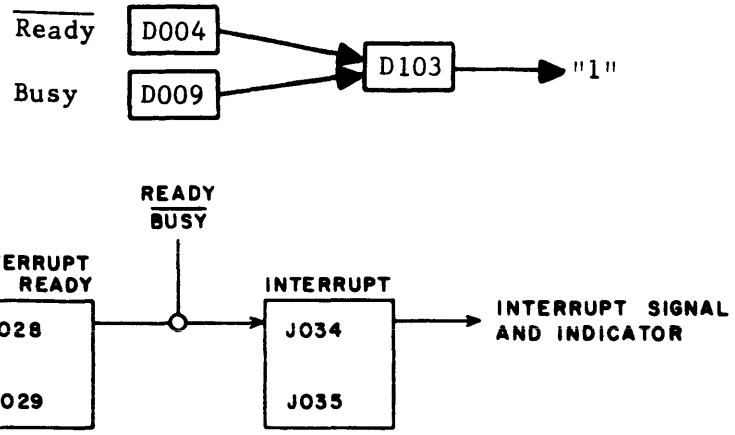
Ready is a Reply from the connected tape handler (p. 3-25) meaning thatt the Ready switch is lighted and manual control from the panel is no longer possible. Control is to be accomplished by the controller, as directed by the channel.



Busy is a Reply from the connected tape handler (p. 3-25) meaning that tape is moving. For this Interrupt to be detected, tape must be motionless and the tape unit Ready.



Inverter D103 becomes a logical "1" when the connected transport is returning a signal, saying Ready and Not Busy.



Interrupt on End of Operation

The Interrupt FF (J034/035) will set when inverter D041 (End of Record, a delayed Reply from the Transport) becomes a logical "1", provided J040 (Channel Not Busy FF) is also set.

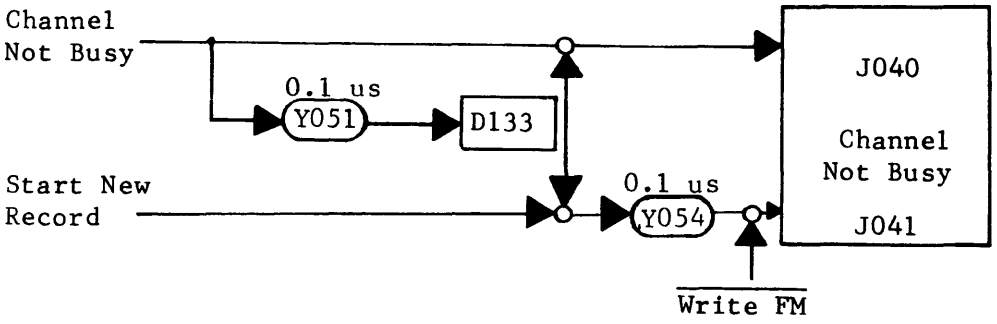
The Channel Not Busy FF (J040/041) clears as a result of the Start New Record signal (E032, p. 3-21).

1. When a Read Operation starts
2. When a Write Operation starts
3. When a Function-Skip Bad Spot starts

It is prevented from clearing when the Function-Write File Mark starts.

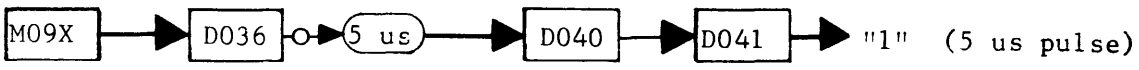
The Channel Not Busy FF (J040/041) sets when the channel goes from Busy (R020 = "0") to Not Busy (R020 = "1"), producing a 0.1 usec pulse from the satisfied AND gate.

The Channel Not Busy FF setting, indicates Input or Output operation on the channel has ended.

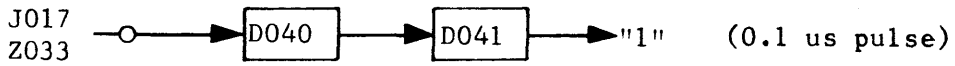


Inverter D041 (End of Record) becoming a logical "1", indicates that operation on the transport has ended. It will become "1":

1. When the End of Operation signal comes from the transport 200 usec after reading a Check Character (during a Read/Write Reply or Write File Mark), or 200 usec after detecting the Load Point Marker (during a Rewind).



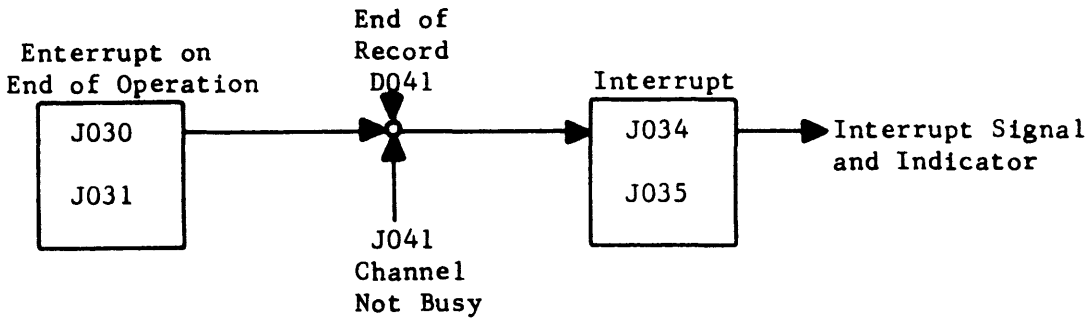
2. As a pseudo End of Record (after erasing 4½ inches -- adjustable from 3 to 6 inches) of tape during the Function Skip Bad Spot.



The Interrupt occurs when both channel and transport have finished their respective functions in an operation and:

1. Tape is stopped in Record Gap after Read or Write.
2. File Mark has been located during a Search File Mark Backward or Forward and Tape is stopped in the Record Gap.
3. The Load Point has been located during a Rewind and tape is stopped on the Load Point.
4. A Skip Bad Spot Function has been completed and tape is stopped approximately 4½ inches (adjustable from 3 to 6 inches) from the last Check Character.

The system is now ready for another operation.



Interrupt on Abnormal End of Operation

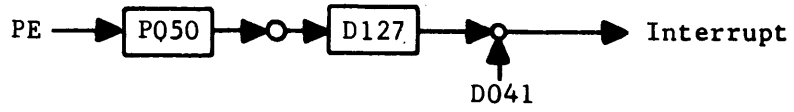
This Interrupt is used when an unusual condition for re-initiation is expected to occur, but includes several of the conditions found in the Interrupt on End of Operation as a Programming convenience.

The Interrupt FF (J034/035) will set when:

1. An error has been detected in the operation. The Interrupt will not occur immediately but will be delayed until the operation is complete and the End of Record signal (D041) becomes a logical "1". These include:

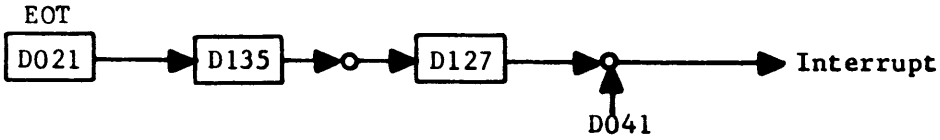
   a. Vertical Parity Error (P050/051)

b. Longitudinal Parity Error (P054/055)
c. Lost Data (Z070/071)



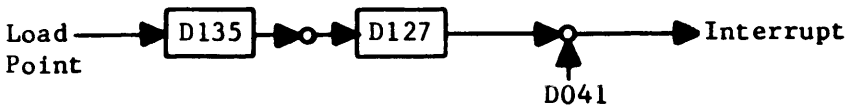
This indicates a need for corrective action, possibly a repeat of the operation.

2. The End of Tape Reflective Marker has been passed during a Read, Write Reply, or Function (Write File Mark). The Interrupt does not occur immediately but is delayed until the operation is complete and the End of Record signal (D041) becomes a logical "1"



This indicates that another operation in a Forward direction should not occur due to the risk of dropping the tape leader from the supply reel and thereby creating a fault condition in the handler.

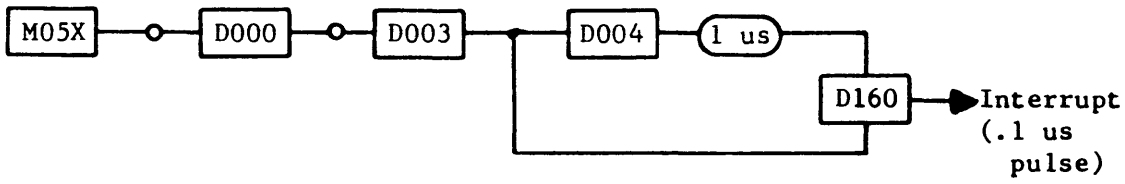
3. The Load Point Marker has been detected during a Rewind or the File Mark has been located during a Search File Mark. These causes are materially the same as conditions 2 and 3 for Interrupt on End of Operation, and produces the interrupt when D041 (End of Record signal) becomes a logical "1".



The indication is a programming convenience and can be used to determine which of several subroutines should be entered after the same cause of interrupt.

4. If the connected tape handler should become Not Ready during an operation, the Interrupt will occur without delay.

   A connected handler could become Not Ready for a number of reasons; such as, turning off power on the transport, manually clearing Ready at the Manual Control Panel, or moving the Unit Select switch on the transport.



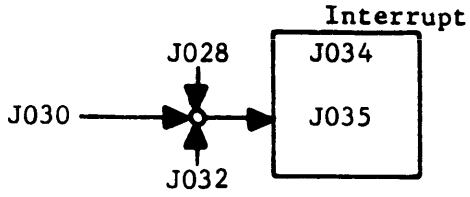
The Ready is lost during the Clear or Release functions, but the interrupt is prevented from occurring during the execution of these functions.

The Ready is lost during a Connect operation when at connect time 2 and all Unit Select FFs are cleared, preparing to select a new transport. The Interrupt is prevented from occurring by the action of K118/119 (Connect FF).

CLEARING INTERRUPT

A new Read or Write operation may not preceed until interrupt has been cleared. Within the subroutine which will process the interrupt, the first step indicated was to clear the interrupt. This clearing may be accomplished in several ways.

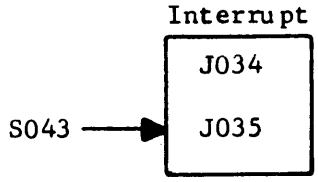
1. The Interrupt FF is held clear if all of the three Interrupt Select FFs are in a clear condition.



All Interrupt Select FFs may be cleared by Functions 0021, 0023, or 0025, or by an External Master Clear from the console.

This, however, would disable further use of the Interrupt System until re-established by another function (0020, 0022, or 0024).

2. If the functions 0021, 0023, or 0025 had been used, a 2X translation from S042 and S043 (page 3-7) would have occurred, clearing the Interrupt FF (J034/035) in the process.

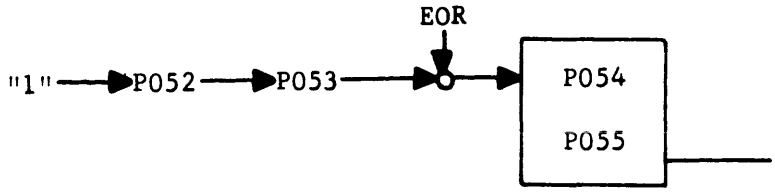


Here again, the Interrupt System would need to be re-established by a Function 0020, 0022, or 0024.

3. If the cause of the Interrupt had been Interrupt on Ready and Not Busy, Function 0020 would produce a 2X translation, clearing the Interrupt (J034/035) and leaving the Interrupt System enabled to produce another Interrupt when the tape system again goes Ready and Not Busy.

   If the cause of the Interrupt had been Interrupt on Ready and Not Busy, Function 0022 could be used, producing the 2X translation to clear the Interrupt and preparing the system to Interrupt next on an End of Operation.

   There are many combinations possible.

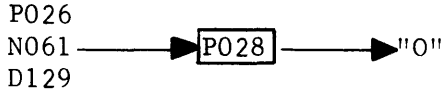


Each frame read back to the controller, except the Check Character, is checked for vertical parity error. The parity checker (p. 3-19) can be looked upon in the same way as the parity generator. Data from the N cards is fed into the checker. The determination made is: Is there an even number of bits in the six information bits of the frame? If the total is even, inverter P026 outputs a logical "1".

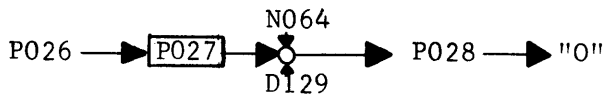
The Parity Error FF (P050/051) sets at time 3 as the N to C transfer occurs. The situations which will <u>not</u> cause a vertical parity error are:

Binary Mode -- Odd Frame (D129=1)

1. Even word and parity bit

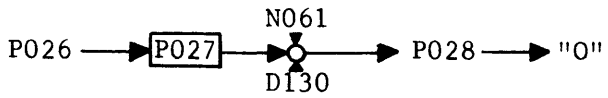


2. Odd word and no parity bit

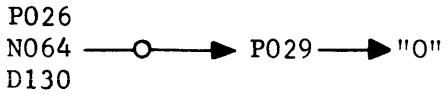


BCD Mode -- Even Frame D130 = 1

3. Odd word and parity bit



4. Even word and no parity bit

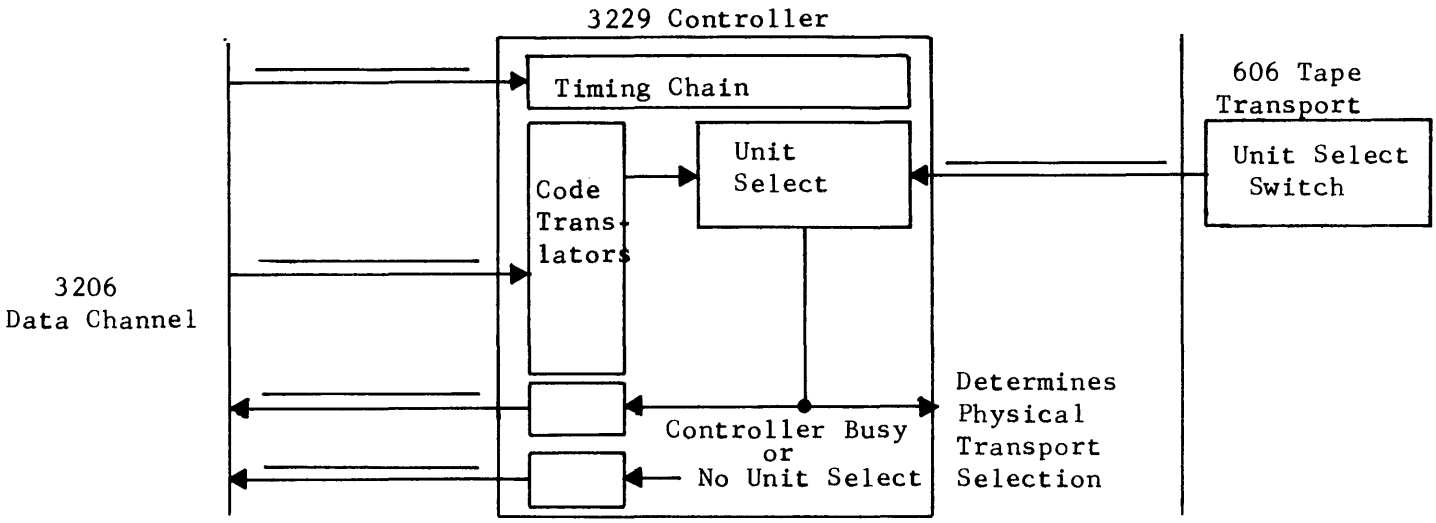


Any other combinations will set the Parity Error FF.

STUDY PROBLEMS

I. CONNECT OPERATION

1. Fill in the following block diagram signal flow.



2. The channel sends the _____ signal to start the Connect Timing Chain.

3. The 12 bit Connect Code contains what two pieces of information for the Magnetic Tape System.

   a.
   b.

4. _____ Parity is used with the Connect Code.

5. A Transmission Parity Error will:

a.	be caused by odd data bits and a parity bit.	T	F
b.	be caused by odd data bits and no parity bit.	T	F
c.	be caused by even data bits and a parity bit.	T	F
d.	be caused by even data bits and no parity bit.	T	F
e.	set the Reject FF K112/113 in the controller.	T	F
f.	be available as a status indication if an error occurs on the Connect.	T	F

6. What visual indication will the programmer notice on the controller if a Transmission Parity Error occurs?

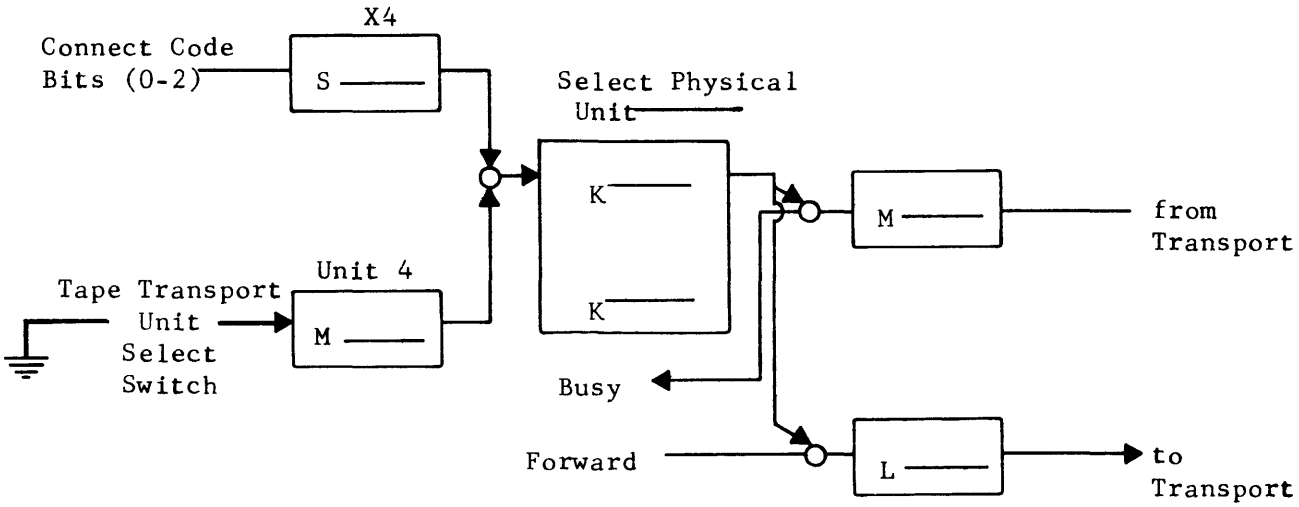
7. There are _____ possible "M" cards for each of _____ possible Tape Transport selections.

8. The "M" card that outputs a Logical 1 signifies _____
_____
_____.

9. With the following physical and logical transport designations, what "M" cards (p. 3-5) output a logical 1.

Physical	Logical	"M" Card (P. 3-5)
A	5	M_____
B	7	M_____
C	1	M_____
D	0	M_____
E	6	M_____
F	4	M_____
G	2	M_____
H	3	M_____

10. Using the above designations complete the following. The tape unit to be selected is 4.



11. Re-arrange the following events into proper sequence by filling the options into the blank spaces below.

Assume Connect Code and Controller Switch agree, no Transmission Parity Error has occurred, and the controller is not busy with a previous operation.

a. Connect Signal - RO13
b. Clear Unit Select FF's P-4
c. "Strobe Pulse" used for checking Transmission Parity Error
d. Set "Reject" FF K112/113 if controller is busy
e. Enable Status Lines to channel

f. Set "Reply" FF K114/115 if Unit Select FF's have set
g. Transmission Parity Bit - R012
h. Clear "Connect" FF K118/119
i. Set "Controller Connect" FF K110/111
j. Set "Unit Select" FF p. 109
k. Start Connect Timing Chain
l. Set "Reject" FF K112/113 if no "Unit Select" FF has set
m. Set "Connect" FF K118/119
n. Connect Code R000-R011 P1

1. Receive _____, _____ and _____ from the channel.

2. _____, and _____ _____.

3. T1 _____, and _____ _____.

4. T2 _____, _____ and _____.

5. T3 _____.

6. T4 _____, _____ and _____.

II. STATUS INSTSRUCTION

1. A Status Response will always be returning from the connected unit. T F

2. What information can the programmer receive from the Magnetic Tape System using the Status Response?

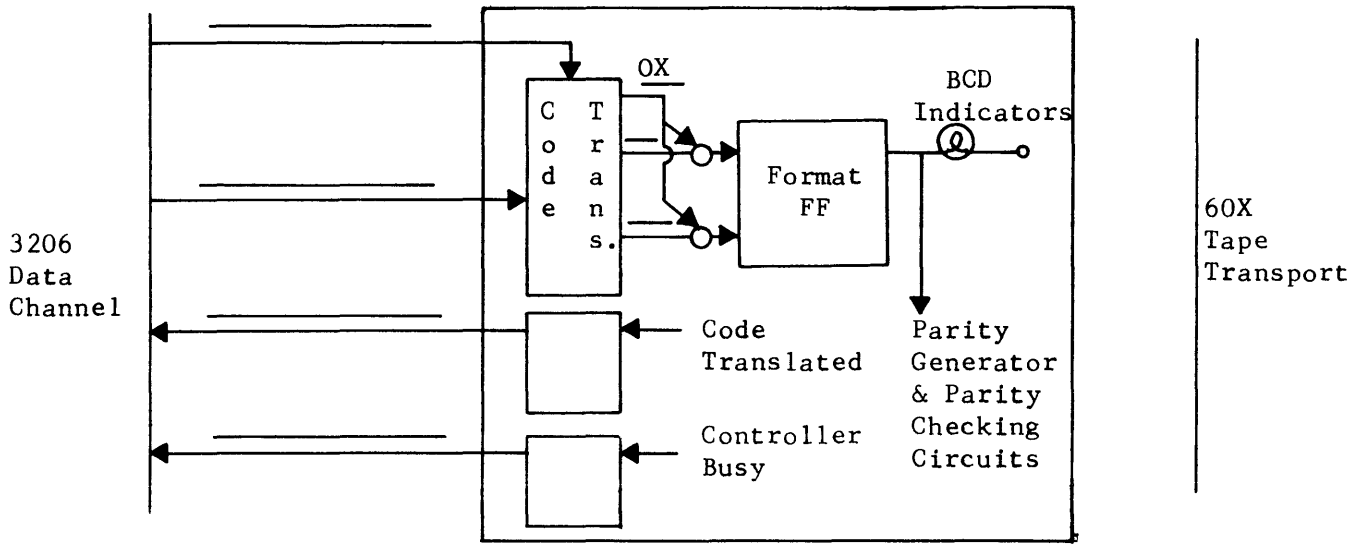
3. What will the following program be used to check.

```
0000 - 77000000
0001 - 01000000
0002 - 77200100
0003 - 00000000
0004 - 77100003
0005 - 01000004
0006 - 00000000
```

4. May more than one response be present on the Status Lines when Status is checked? If no, explain why. If Yes, give a realistic example.

III. FORMAT SELECTION (BINARY-BCD)

1. Fill in the following block diagram signal flow.



2. The format selection determines whether an odd or even number of bits shall be exchanged between controller and Tape Transport, and controller and channel. T F

3. What conditions must exist in the controller before the Function Code can be translated?

   a.
   b.
   c.
   d.
   e.

4. What would cause an external reject when selecting the format?

5. The format FF has two main circuits to control. What are they?

   a.
   b.

6. The programmer's visual indication, when the Binary format is selected, is an illuminated lamp on the controller. T F

7. The format selection was made prior to a Write Operation. Which would cause a parity error?

   a. An even number of data bits with a BCD Selection T F
   b. An even number of data bits with a Binary Selection T F
   c. An odd number of data bits with a BCD Selection T F
   d. An odd number of data bits with a Binary Selection T F

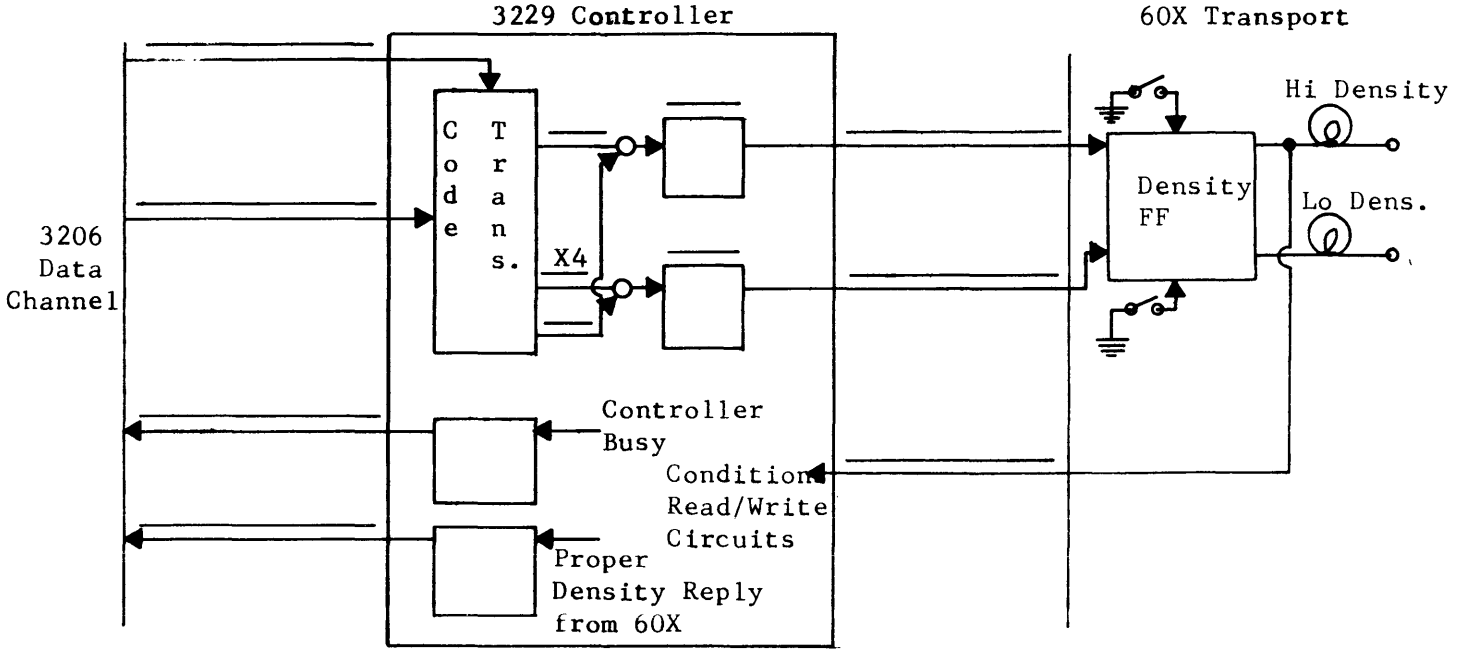
8. The format selection was made prior to a Read Operation. Which would cause a parity error?

   a. A BCD format, a parity bit, and an odd number of data bits T F
   b. A BCD format, a parity bit, and an even number of data bits T F
   c. A BCD format, no parity bit, and an odd number of data bits T F
   d. A BCD format, no parity bit, and an even number of data bits T F
   e. A Binary format, a parity bit, and an odd number of data bits T F
   f. A Binary format, a parity bit, and an even number of data bits T F
   g. A Binary format, no parity bit, and an odd number of data bits T F
   h. A Binary format, no parity bit, and an even number of data bits T F

9. The Format FF clears when the format selection is completed. T F

IV. DENSITY SELECTION

1. Fill in the following block diagram signal flow.



2. What type of reject will occur if a Transmission Parity Error occurs on a Density Instruction?

3. What other condition will cause this type of reject during a Density Instruction?

4. Why can't the Density FF's set if the Controller is busy?

5. When changing from low to hi density, what visual indication would show the change had taken place?

6. Can density be changed other than by a Function Instruction? If yes, indicate the method.

7. How does the returning 60X Density Signal affect the Write Circuits?

8. How does it affect the "Read Circuits"?

9. Complete the following chart.

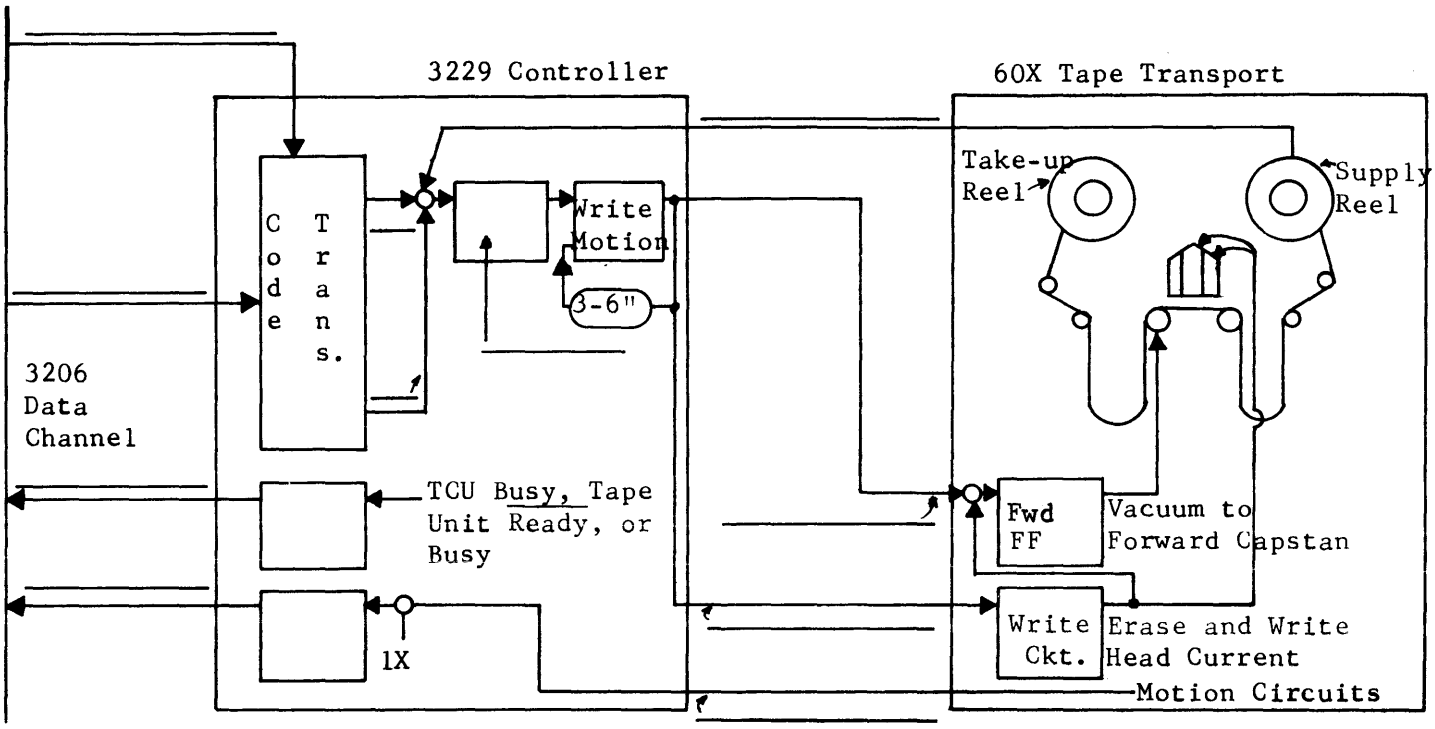
Density	Transfer Rate	Frame Space (u sec)	Frame Space (inches)
200 BPI			
556 BPI			
800 BPI			

10. What prevents the "Reply" Signal from returning to the channel before the proper density signal arrives from the 60X?

11. When the "Reply" Signal is sent to the channel, what happens to the Density FF's in the controller? In the transport?

V. SKIP BAD SPOT

1. Fill in the following block diagram signal flow.



2. Would a "Write" Signal be sent to the selected tape transport if it is not ready? If no, explain what prevents it? If yes, how does the signal affect the transport? Give a detailed explanation.

3. What conditions would prevent the "Skip Bad Spot" FF from setting when the code has been translated?

   a.
   b.
   c.

4. When an option is false, explain why it is false:

   During a "Skip Bad Spot" Instruction,

a.	An "External Reject" Signal is sent to the channel if the File Protect Ring is not on the Supply Reel	T	F
b.	"R to 0" FF Z010/011 Pg. 8 will set but no data transfers to the Write Register	T	F
c.	The "Write Control" FF prevents the setting of the "Write" Register	T	F
d.	No current flow is allowed in the tape transport's Erase and Write heads	T	F

5. List 7 operations that would cause a loss of the "Write Now Possible" Signal (I135 pg. 115)

   a.
   b.
   c.
   d.
   e.
   f.
   g.

6. A malfunction disabling the Write Timing Chain would prevent this operation T F

7. Arrange the following events into proper sequence. If some are not needed for this operation, draw a line through them on the list and do not include these in the sequence.

a. Clear Write Terminate I FF
b. Set Write Terminate II FF
c. Send Write Signal to 60X
d. Clear Skip Bad Spot J016/017
e. Set Write Gate
f. Clear Write Motion
g. Drop Forward Signal to 60X
h. Clear R to 0
i. Set Write Terminate I
j. Clear Write Resync
k. Send Reply Signal to The Data Channel
l. Clear Write Terminate II FF
m. Set R to 0
n. Set Skip Bad Spot FF's
o. Send Forward Signal to 60X
p. Clear Write Gate
q. Set Write Resync
r. Drop Write Signal to 60X
s. Set Write Motion
t. Set Write Control
u. Arrival of Function Signal
v. Clear "Skip Bad Spot" FF J012/013
w. Clear Write Control
x. Arrival of Function Code

8. Before the Write Terminate I FF can set, the Check Character must be written. T F

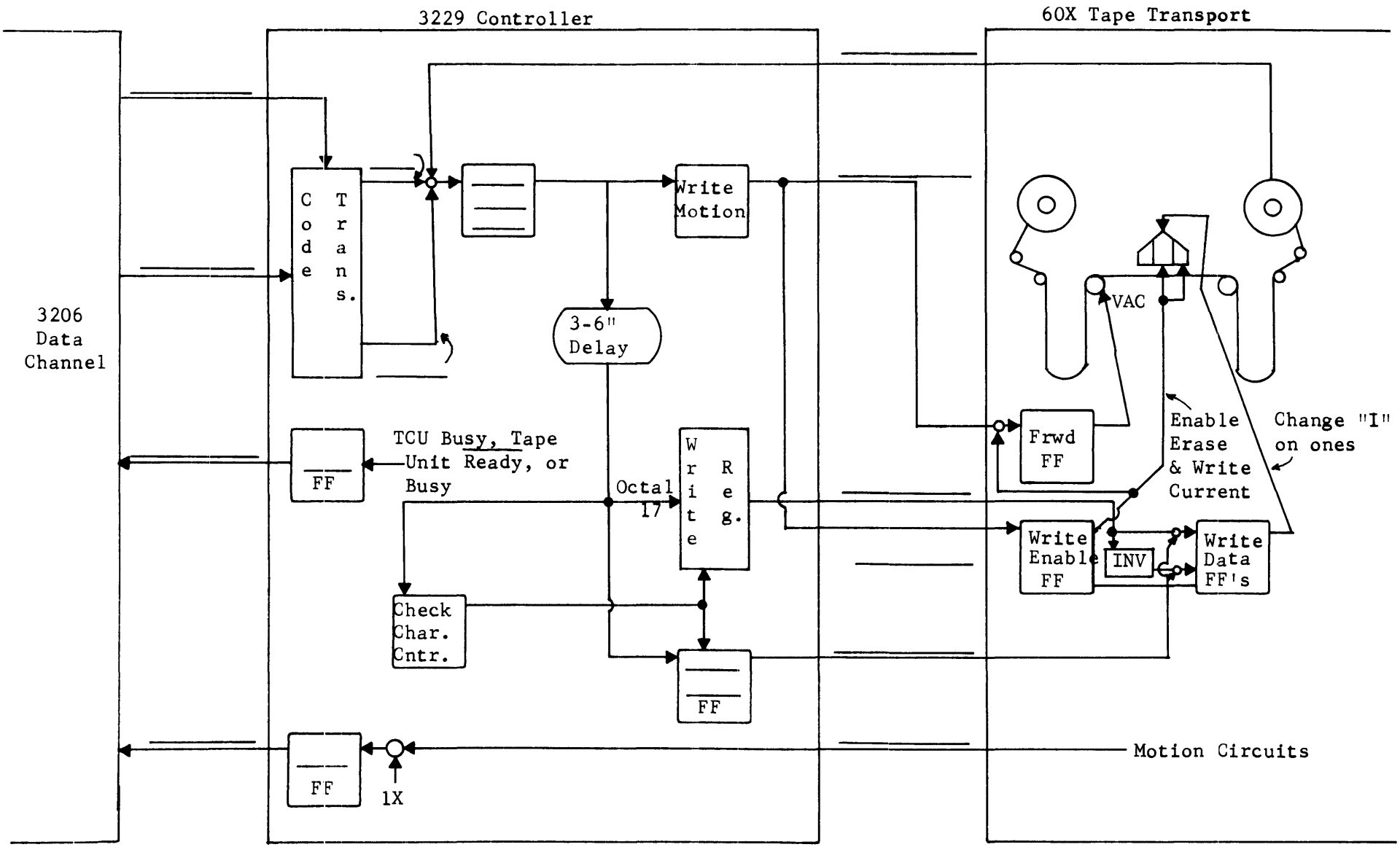
9. How does the controller know when the Tape Transport has erased tape the proper distance.

10. What causes the "End of Operation" Signal to be missing from the Status Lines during this operation?

11. The normal "End of Record" Signal from the Tape Transport cannot be generated unless one frame has been read. How do we generate the "End of Record" Signal which clears FF J044/045 Pg. 111 during a Skip Bad Spot Instruction?

VI. WRITE FILE MARK

1. Fill in the following block diagram signal flow



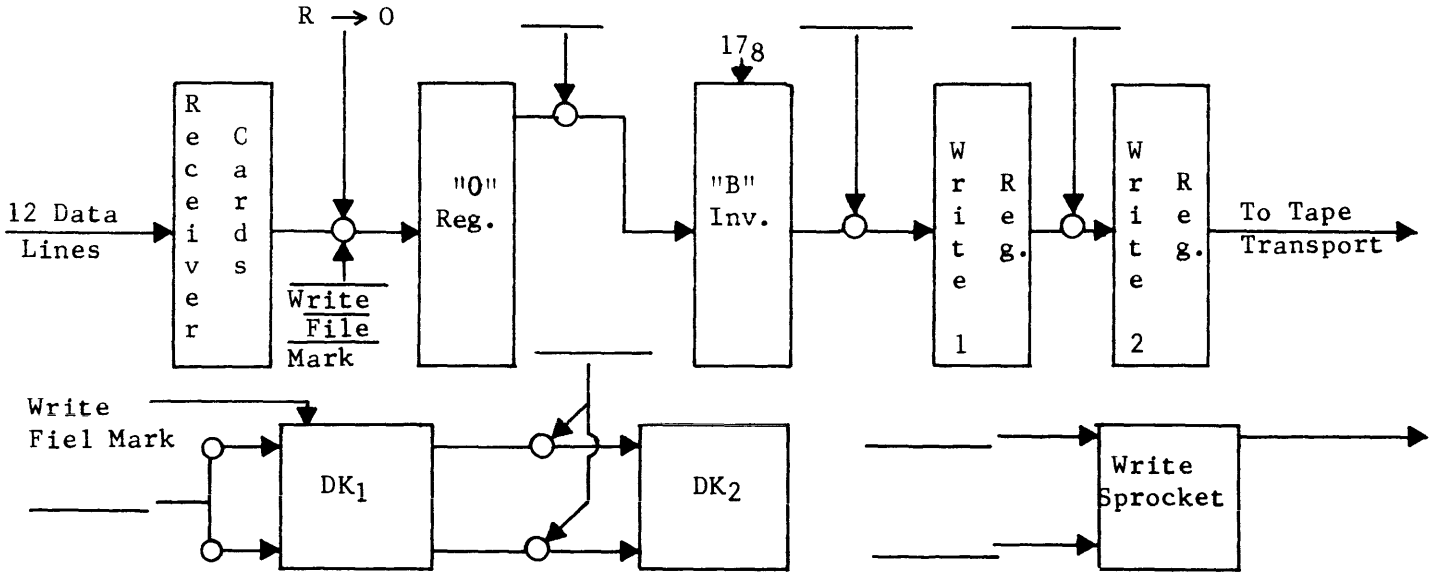
2. How can the same three Write oscillators operate 75 as well as 150 inch per second Tape Transports?

3. How long will the Timing Chain remain active when it begins a pass?

4. Fill in the proper Write Time beside the following terms.

Term	Time
a. 0 → B (W100)	_____
b. $W_1 \rightarrow W_2$ (W101)	_____
c. $DK_1 \rightarrow DK_2$ (W087)	_____
d. B → W (W102)	_____
e. Start Sprocket (W103-A Zero)	_____
f. Advance DK (W104)	_____
g. Clear Sprocket (W105)	_____

5. Fill the above enables into this simplified block diagram.



6. Would this operation start tape movement if the File Protect Ring was missing from the Transport's Supply Reel? If no, explain what prevents it? If yes, when it tape stopped?

7. Setting the Write Fill Mark FF, immediately:

   a. Places the File Mark in the Write Register
   b. Sets the Disassembly Counter
   c. Clears the "Write Data Lockout" FF
   d. Sets R to O FF
   e. Changes format to BCD if it was Binary
   f. Prevents an R to O Transfer

8. What prevents the shorter delays from expiring first, to set the Write Control FF after only a 3/4 inch delay? p. 113

9. What two events occur when the Write Control FF sets?

   a.
   b.

10. A malfunction disabling the Write Timing Chain would prevent this operation T F

11. Rearrange the following events into the proper sequence.

Preparing To Write A File Mark

a. Set Disassembly Counter I
b. Clear Write File Mark FF J010/011
c. Set R to 0 FF
d. Place an "Octal 17" in "B" Inverters
e. Clear R to 0 FF
f. Set the "Write File Mark" FF
g. Set "Write Resync"
h. Receive Function Code & Signal
i. Send Forward Signal to 60X
j. Format changed to BCD
k. Send Write Signal to 60X
l. Set Write Motion
m. Send "Reply" Signal to Channel
n. Remove Clear from W_1 Register
o. Set Write Control

After rearranging the above events, review by again following them through the logic diagrams. At this time tape should be moving with current flowing through the Erase and Write Head. A Reply has returned to the Channel.

12. Rearrange these events into the proper sequence.

Writing The File Mark

a. Clear Disassembly Counter I
b. Set Disassembly Counter II
c. "O_2 to B" Transfer
d. Set Write Gate
e. "DK_1 to DK_2" Transfer
f. Enable Transfer Terms (W084-W089)
g. Set Write Sprocket FF
h. File Mark written on tape
i. Clear Write Resync
j. Clear Write File Mark FF J014/015
k. Clear Write Gate
l. Advance DK Pulse
m. "B to W_1" Transfer
n. "W_1 to W_2" Transfer
o. Set Check Character Counter Enable FF Z000/001
p. Disable Transfer Terms (W084-W089)
q. Clear "Write Sprocket" FF

Again review the properly rearranged sequence in your logic diagrams. The File Mark has been written and the Check Character Counter is enabled.

13. Writing The Check Character

a. Z002/003 Clear, Z004/005 Clear, & Z006/007 Set
b. Set Write Terminate I
c. Z002/003 Set, Z004/005 Clear, & Z006/007 Clear
d. Z002/003 Clear, Z004/005 Set, & Z006/007 Set
e. Z002/003 Set, Z004/005 Set, & Z006/007 Clear
f. Z002/003 Clear, Z004/005 Set, & Z006/007 Clear
g. Z002/003 Set, Z004/005 Set, & Z006/007 Set
h. Z002/003 Set, Z004/005 Clear, & Z006/007 Set
i. Clear W_1 Register
j. Clear Check Character Counter Enable FF Z000/001
k. Write Check Character on tape
l. Set Write Sprocket FF
m. Z002/003 Clear, Z004/005 Clear, & Z006/007 Clear
n. Clear Write Sprocket FF

Review logic diagrams. The Check Character has been written in the 4th frame position on tape. The Check Character will be an Octal _____.

14. Terminating The Write File Mark Operation

a. Drop Forward Signal to 60X
b. Clear Write Terminate I
c. Clear Write Terminate II
d. Drop Write Signal to 60X
e. Clear Write Control
f. Set Write Terminate II
g. Place a Steady Clear on W_1 Register
h. Disable the setting of the "R to 0" FF
i. Clear Write Motion

Review the rearranged sequences in the logic diagrams. The Forward & Write Signals drop and Motion is stopped in the Transport. Write Head Current remains.

15. Why can't the Disassembly Counter advance, with each pass through the Timing Chain, when incrementing the Check Character Counter?

16. How much time is needed from the last data frame until the Check Character is written? (Check Character Gap in u sec) (200 BPI)

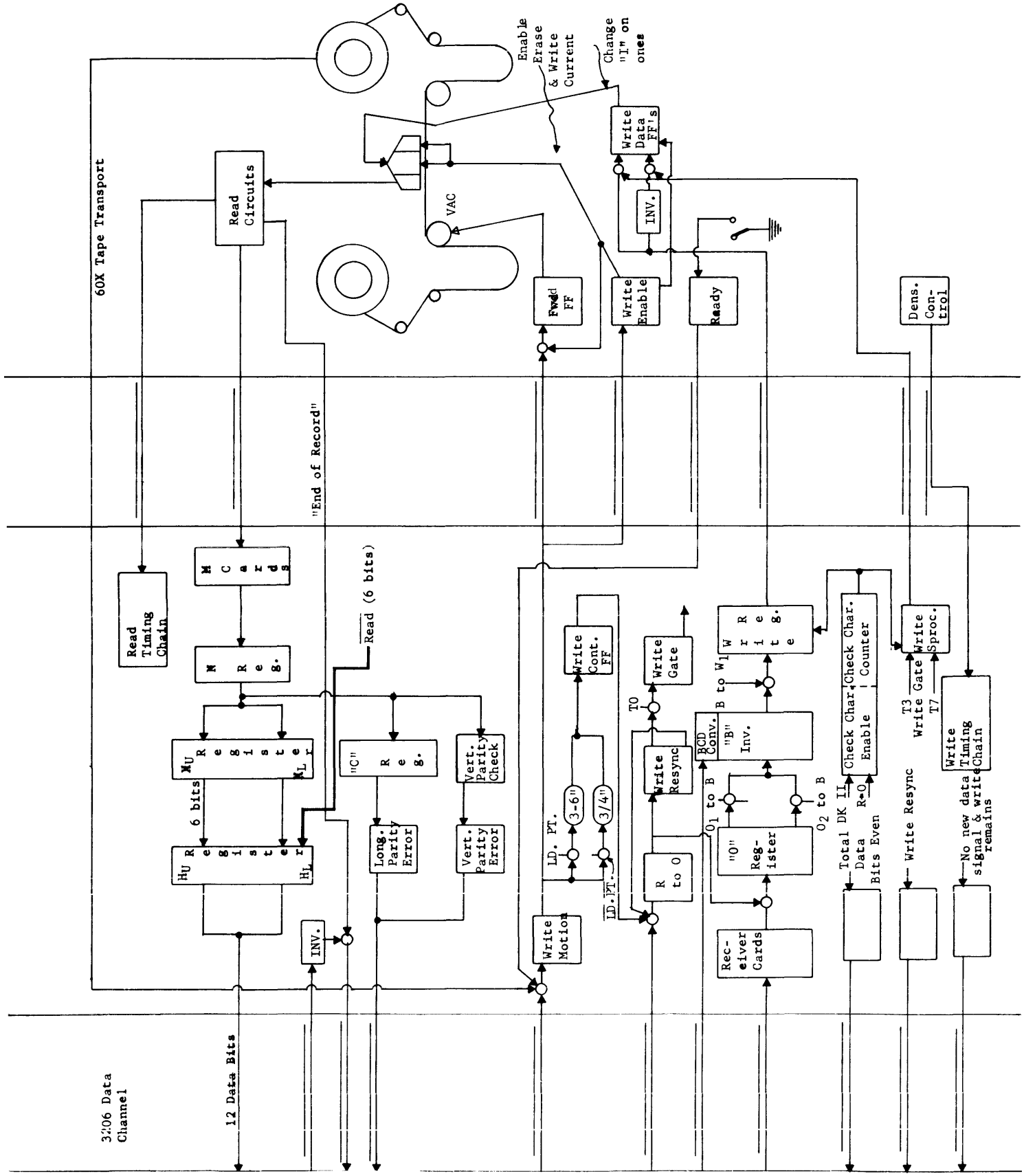
17. What is the duration of the Write Sprocket using a 150 inch per second transport? A 75 inch transport?

18. What is the purpose of the Write Resync FF?

19. What is the purpose of the Delay Y041 (Y058) between Write Terminate I and II?

VII. WRITE OPERATION (12 AND 6 BIT MODE)

I. COMPLETE THE FOLLOWING BLOCK DIAGRAM.



2. Which Flip Flop is the first to set during a 12 bit Write Operation?

3. Which of the below conditions would prevent the setting of the Flip Flop you have listed?

   a. Lost Data FF set
   b. Write Resync FF set
   c. Write Control FF set
   d. The selected tape unit has no File Protect Ring.
   e. All tape units are prepared to write; however, the wrong unit is selected by accident.
   f. The previous Write Operation is completed but tape is still moving.
   g. If the selected tape is rewinding

4. How is a six inch Delay achieved when writing from Load Point?

5. During a Write Operation, The R → 0 FF accomplishes 5 tasks. What are they?

   a.
   b.
   c.
   d.
   e.

6. When will the R to 0 FF clear?

7. When does the Write Timing Chain begin to sequence data through the controller?

8. When the Write Gate FF sets, where are the 12 bits of data located?

9. When does the "Reply" Signal return to the Channel?

10. Describe

    a. How the "Lost Data" FF sets if the first data frame is absent.

    b. How does the tape motion stop?

11. What is the purpose of the "O" Register?

12. WHat is the purpose of the "B" Cards?

13. What is the rule for converting Internal to External BCD? Which code is the exception?

14. What is the purpose of the Write Register?

15. Why is a Write Sprocket Signal used with the Magnetic Tape System?

16. What factors determine which portion of the "0" Register is to be written on the tape?

    a.
    b.

17. List the conditions that will generate a Parity Bit?

18. a. What is the condition of the Disassembly Counter when the first six bit word is sent to the Transport?

    b. Which six bit byte is sent to the Transport first?

19. Why can't the "Check Character Gap Counter Enable" FF set after the first six bit transfer?

20. Which of the Write Circuit FF's will set and clear with each written frame?

    a.
    b.

21. After the second frame is written on tape, how is the "0" Register cleared?

22. a. How is the "Lost Data" FF set when a 12 bit byte is absent (not to include the first frame)?

    b. How is the tape motion stopped?

23. What keeps the Check Character Gap Counter inactive while data is being written?

24. Why does the counter begin to increment after the last frame?

25. When the correct gap has been formed, how is the Check Character written?

26. When and how is the termination started?

27. The data which was written will be read and parity will be checked. How is the Read Timing Chain Enabled during a Write Operation?

28. How is the Read Timing Chain able to remain synchronized with the data being read?

29. Fill in the following blanks with the proper Read Time.

a. Clear X _____

b. C_1 to C_2 _____

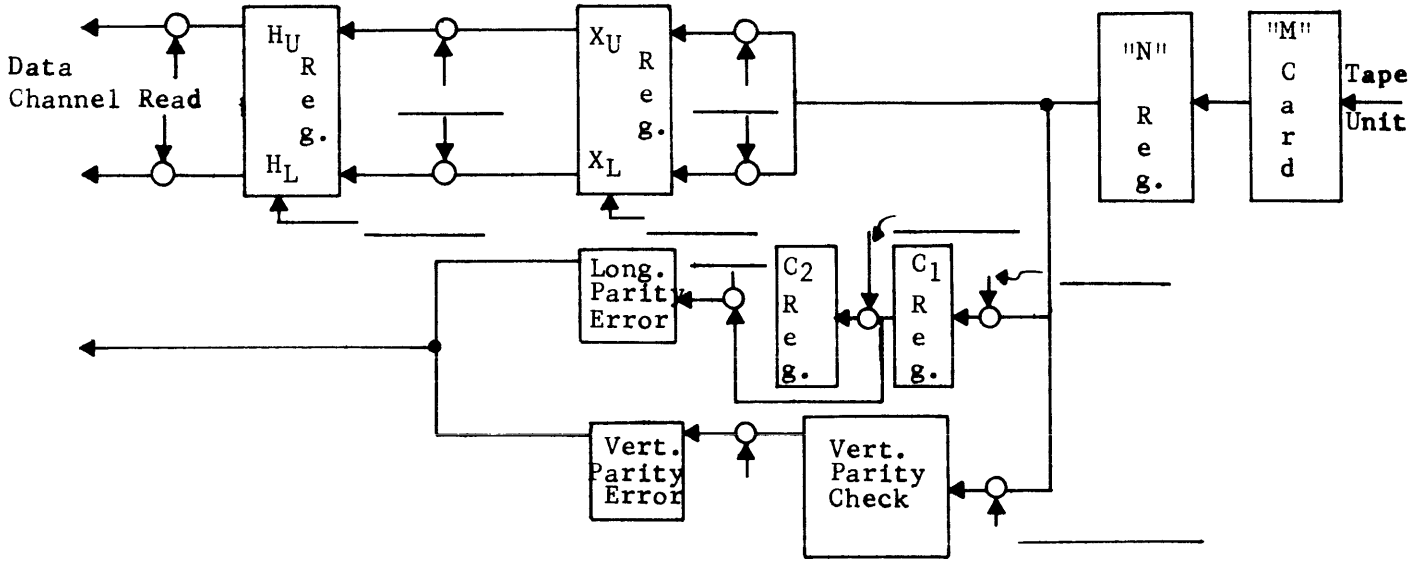
c. N to C_1 _____

d. N to X _____

e. X to H _____

f. Clear H _____

30. Place the above terms in the proper blanks below.



31. How long does the Reply Timing Chain Lockout FF remain set?

    a. 200 BPI: _____

    b. 556 BPI: _____

    c. 800 BPI: _____

32. List the conditions that will give a Vertical Parity Error?

33. What is the purpose of the "C" Register?

34. Why is the "End of Record"Pulse used to time the checking of the "C" Register?

35. Tape motion will automatically be stopped by the controller if a Parity Error occurs. T F

36. How is the tape motion stopped if a Parity Error has occurred? If no Parity Error is present?

37. When motion stops the Read Head has reached the Record Gap?

    a. True

    b. False, where will the Read Head be positioned?

38. What additional signal is needed to write only six bits of each computer output?

39. Explain the affect of this signal on each of these items.

    a. Setting the Write Control FF

    b. Advancing the Disassembly Counter

    c. Generating the Write Sprocket Signal

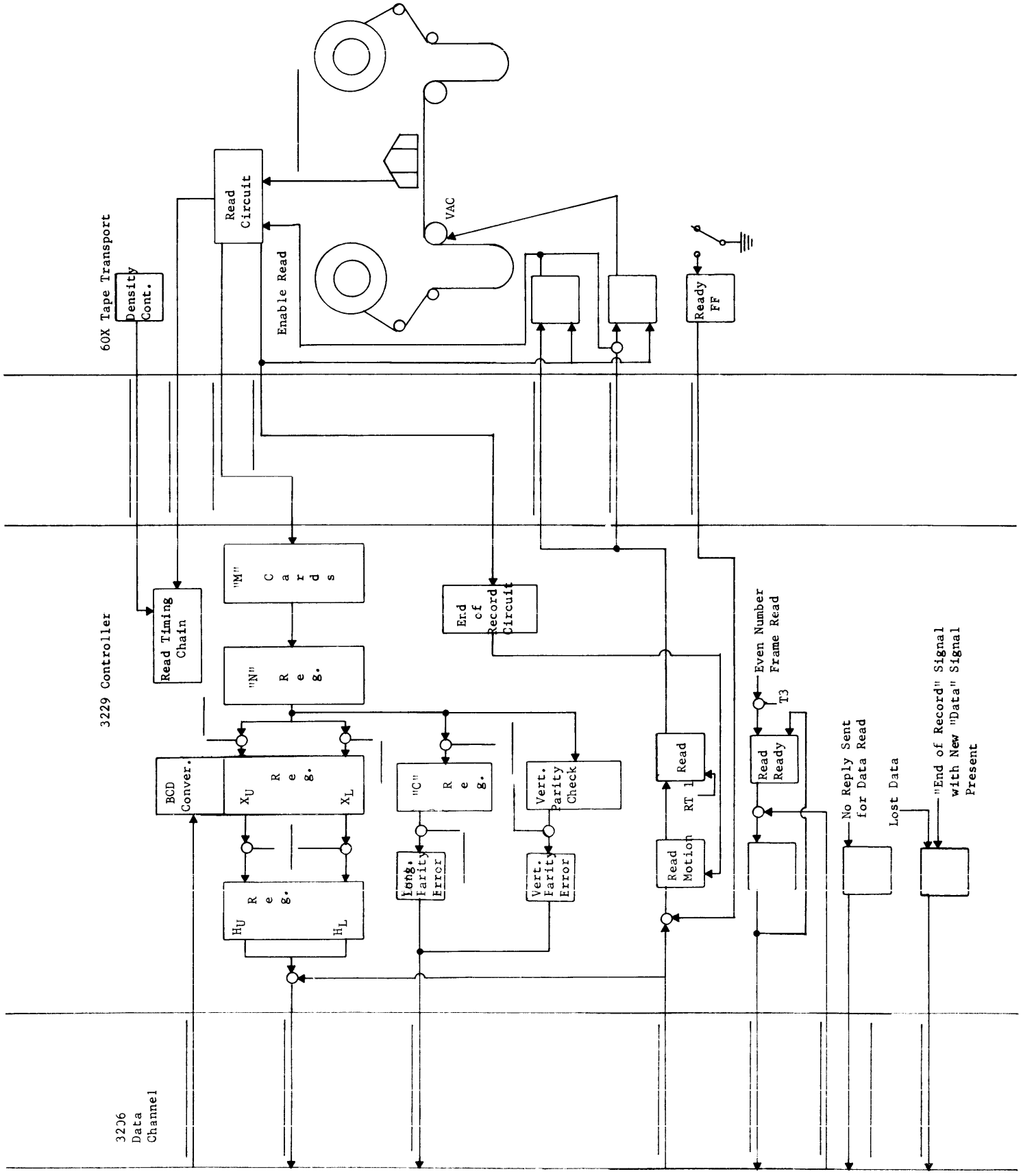
    d. Setting the "Lost Data" FF

    e. Setting the "Check Character Gap Enable" FF

    f. Gating data from "0" to B.

VIII. READ OPERATION (12 AND 6 BIT MODE)

I. COMPLETE THE FOLLOWING BLOCK DIAGRAM.



The following questions deal with a 12 bit Read Operation. "Read Backward" is not selected.

2. What is the purpose of the "Read Motion" FF?

3. Which of these conditions will prevent the "Read Motion" FF from setting?

   a. Selected Tape Transport not ready

   b. Lost Data Condition

   c. Read Control Set

   d. No data signal accompanying the Read

   e. Selected tape unit is searching for a File Mark

   f. A Read Signal present before the Busy Signal drops on the previously initiated Read Operation

   g. Read Signal present before Busy Signal drops on a previously selected Write Operation.

   h. Read Data Lockout FF set

4. A "Start New Record" Signal is generated for _____ u sec during a Read Operation.

5. What functions are accomplished by the "Start New Record" Signal?

   a.
   b.
   c.
   d.
   e.
   f.
   g.

6. What conditions determine which part of the "X: Register receives data?

   a.
   b.
   c.

7. To which part of the "X" Register are odd frames placed?

8. What is the condition of the Assembly Counter at this time?

9. What starts the Read Timing Chain?

10. Using only the following Enables, arrange them into the proper sequence for assemblying two frames. Enables may be used more than once.

    a. Clear the "X" Register

    b. C_1 to C_2

    c. N to C_1

    d. N to X_1

    e. N to X_2

    f. X_1 to H

    g. X_2 to H

    h. Clear the "H" Register

    Odd Frame

    Even Frame

11. What is the rule for converting External to Interal BCD?

12. Explain how the logic converts the External BCD 12 to an Internal BCD Zero.

13. What happens when the "Read Ready" FF sets?

14. What conditions will clear the "H" Register?

    a.
    b.
    c.
    d.

15. What circuit is controlled by Begin Record I and II FF's?

16. What is the purpose of Begin Record I and II FF's?

17. How is the "Hold" FF used to detect a "Lost Data" condition?

18. What is the purpose of the "End of Record" Circuits?

19. What conditions are needed to time out the "End of Record" delays?

20. When will the delays time out before the data within a record is read.

21. When will the Read Motion FF clear?

22. What would happen if the computer requested another input after the "End of Record" Signal is received from the Tape Transport?

23. How will the "Suppress Assembly/Disassembly" Signal affect a Read Operation?

24. Explain how the Supress A/D Signal affects each of these items.

    a. Read Motion FF

    b. End of Record I FF

    c. Assembly Counter

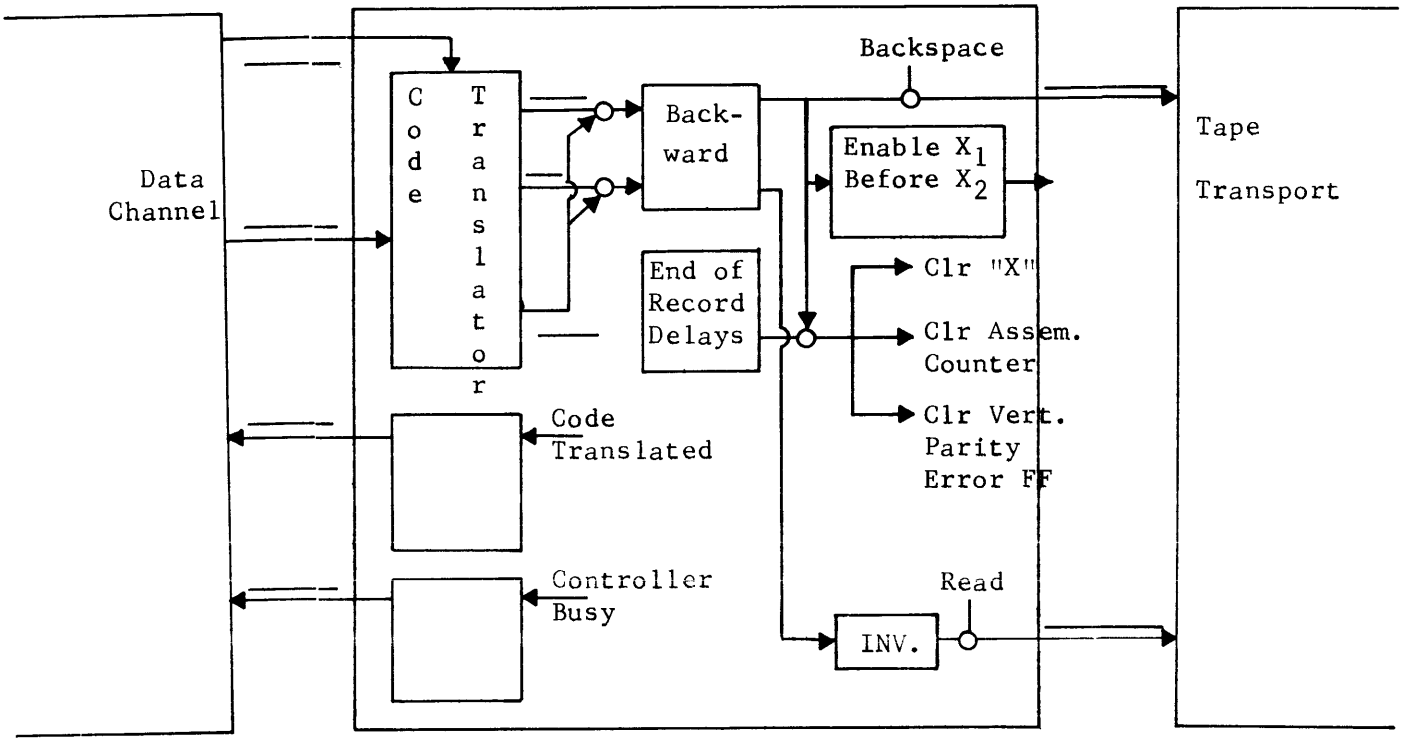
    d. Read Ready

e. N to X Transfer

f. X to H Transfer

IX. READ BACKWARD (SELECTION OR RELEASE)

1. Complete the following Block Diagram.



2. Can the "Backward" FF be selected if the Transport is busy? If the controller is busy? Why?

3. If the "Backward" FF is set which way will tape move when a "Read" Signal arrives? If a "Backspace" is selected?

4. When performing a Read Operation with the "Backward" FF set, the first frame Read will:

   a. Contain data
   b. Be returned to the computer
   c. Be stored in a register in the controller
   d. Always contain an even number of logic one bits if in BCD Mode
   e. Be followed by the Check Character Gap
   f. Set "Begin Record I" FF
   g. Set "Begin Record II" FF
   h. Advance the "Assembly" Counter
   i. Set the Longitudinal Parity Error FF
   j. Set the Vertical Parity Error FF
   k. Be placed in X upper
   l. Be placed in X lower

5. What will happen to these circuits in the Check Character Gap? Explain why each must occur.

   a. The "X" Register

   b. The Assembly Counter

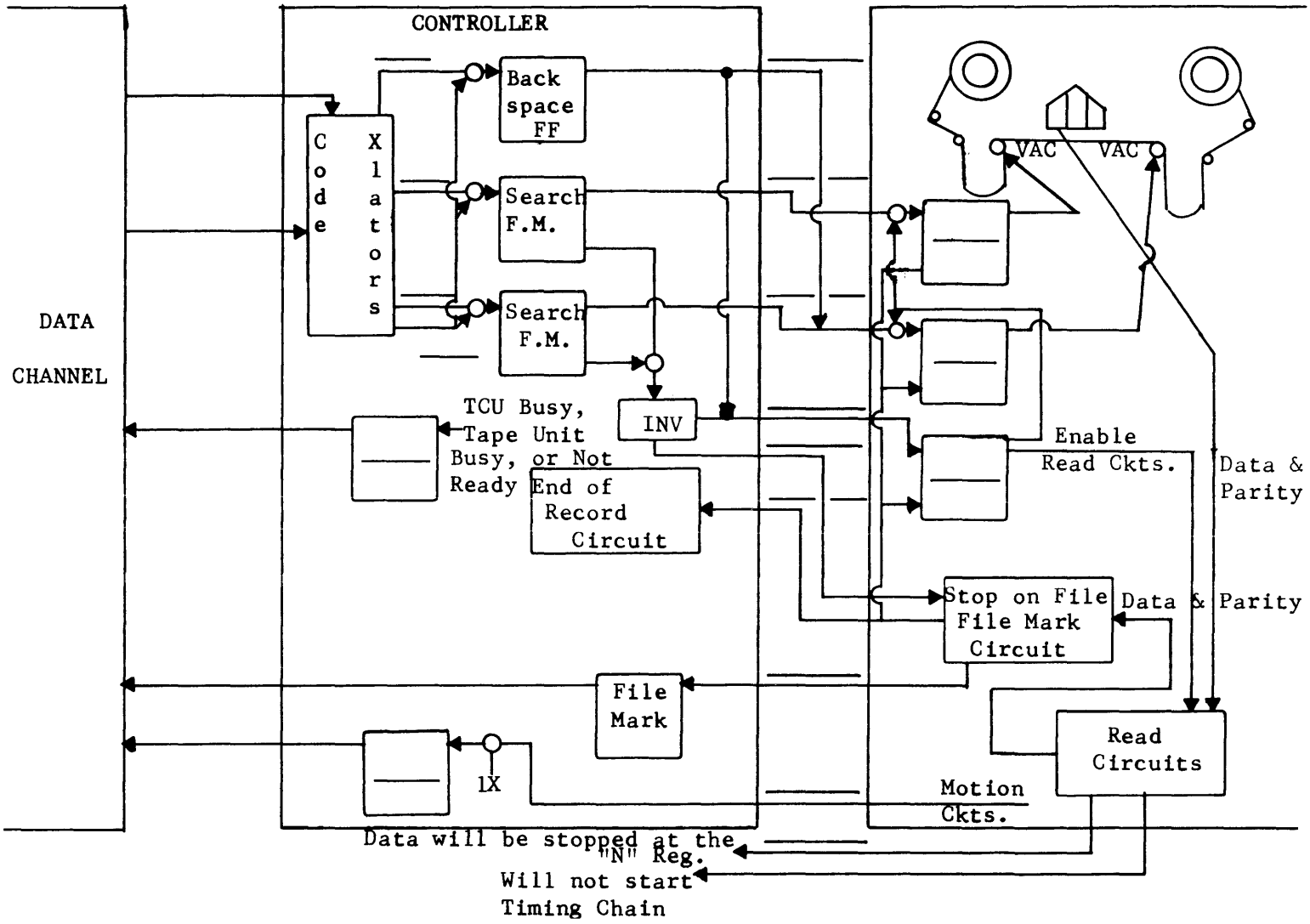
   c. The Vertical Parity Error FF

6. Why shouldn't the "C" Register be cleared also?

7. Where will the Read Head be situated when tape motion stops?

X. SEARCH FOR FILE MARK FORWARD, REVERSE, AND BACKSPACE

1. Complete the following Block Diagram.



2. What is the purpose of a Search For File Mark instruction?

3. What conditions are needed to set the Search For File Mark FF's?

4. When is the "Reply" sent to the Channel?

5. What happens to the data sent to the controller? What prevents the data from entering the computer?

6. Why can't a Parity Error occur when searching for a file mark?

7. Tape continues to move even when the "Search For File Mark" FF's clear. How does tape motion stop?

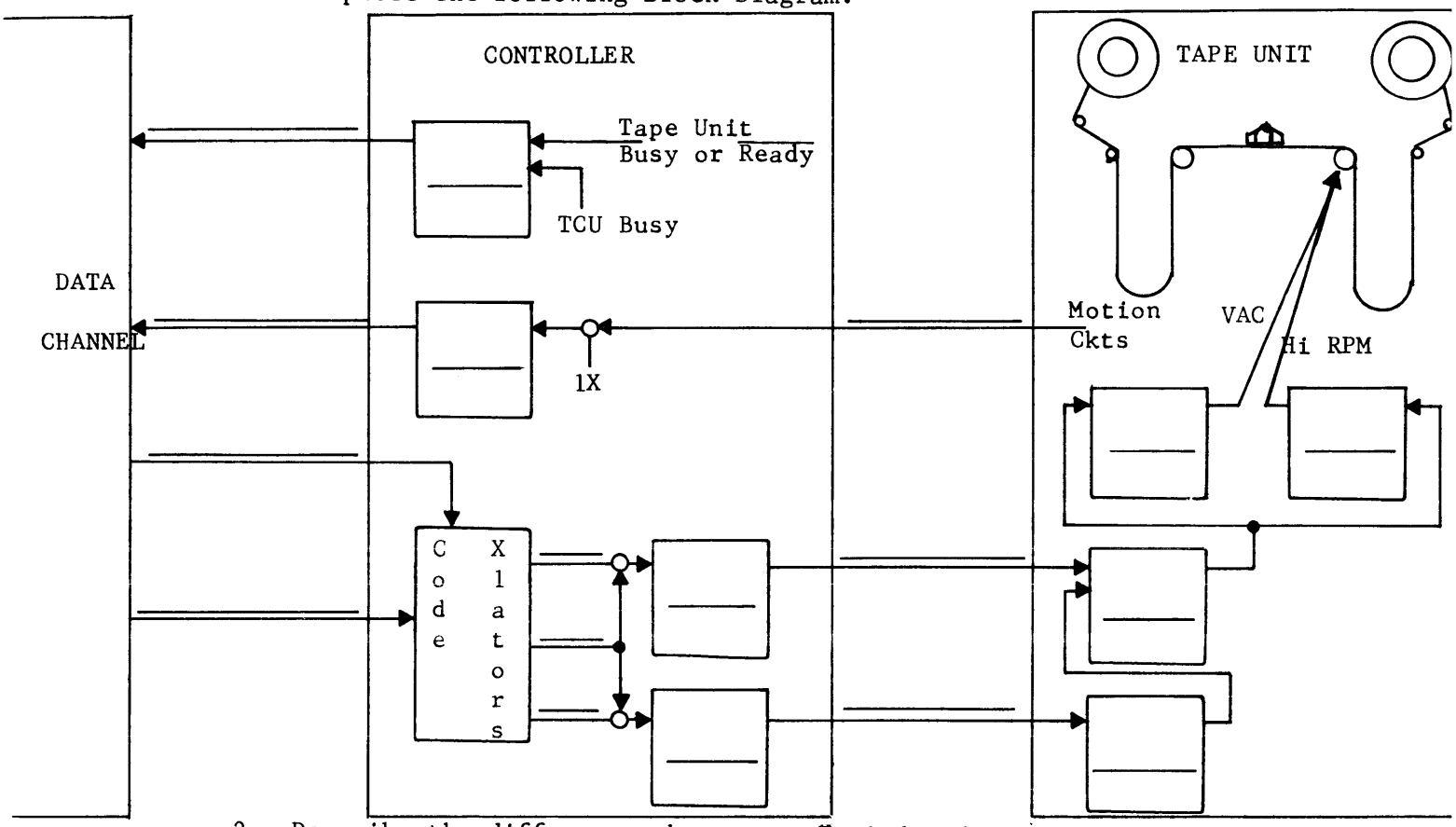
8. When the "File Mark" FF, p. 3-29, has set, what conditions are needed to clear it?

9. What is the purpose of a "Backspace" Operation?

10. How is tape motion stopped when performing a "Backspace"?

XI. REWIND AND REWIND UNLOAD OPERATIONS

1. Complete the following Block Diagram.



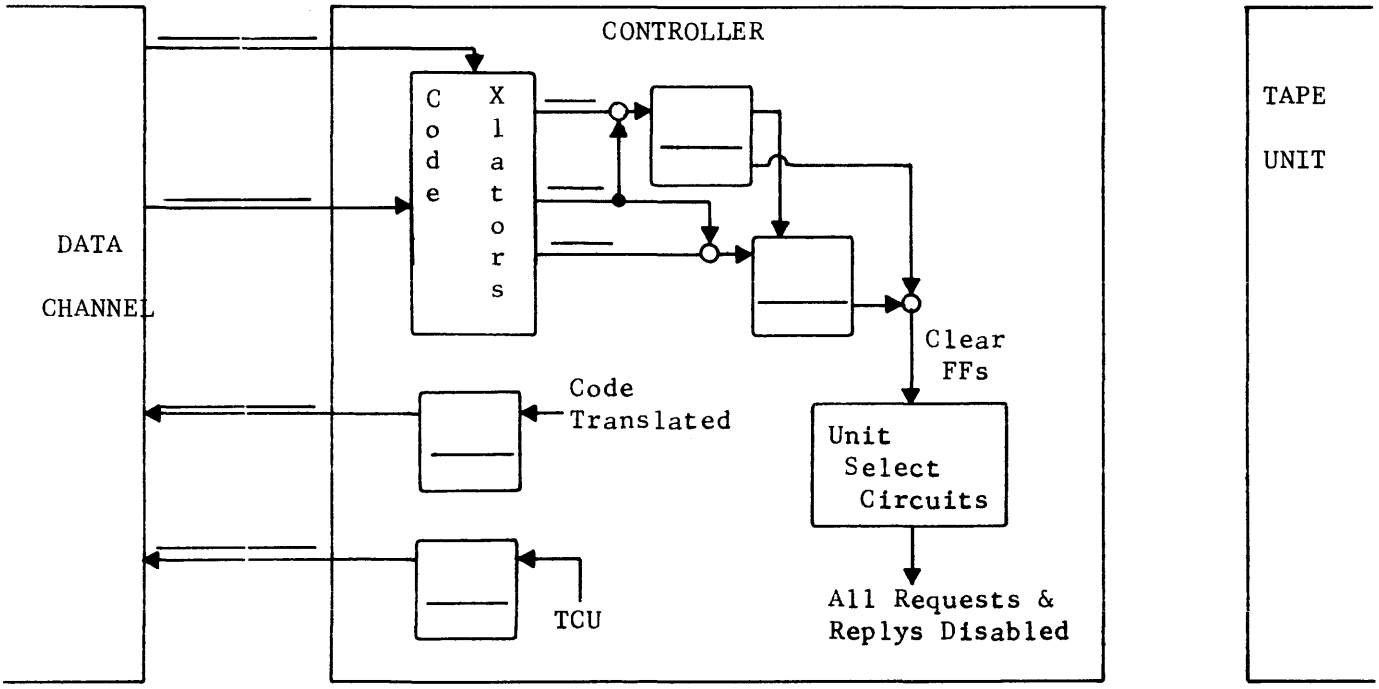
2. Describe the differences between a Rewind and a Rewind Unload Operation.

3. A "Rewind" instruction has been selected but tape is already at "Load Point." Is a "Reply" sent back to the Channel? If yes, explain how. If no, how is the computer able to continue with the next instruction?

4. How is a "Reply" Signal sent to the computer if a "Rewind Unload" Operation is selected?

XII. RELEASE AND CLEAR INSTRUCTIONS

1. Complete the following Block Diagram.



2. What is the purpose of the "Release" instruction?

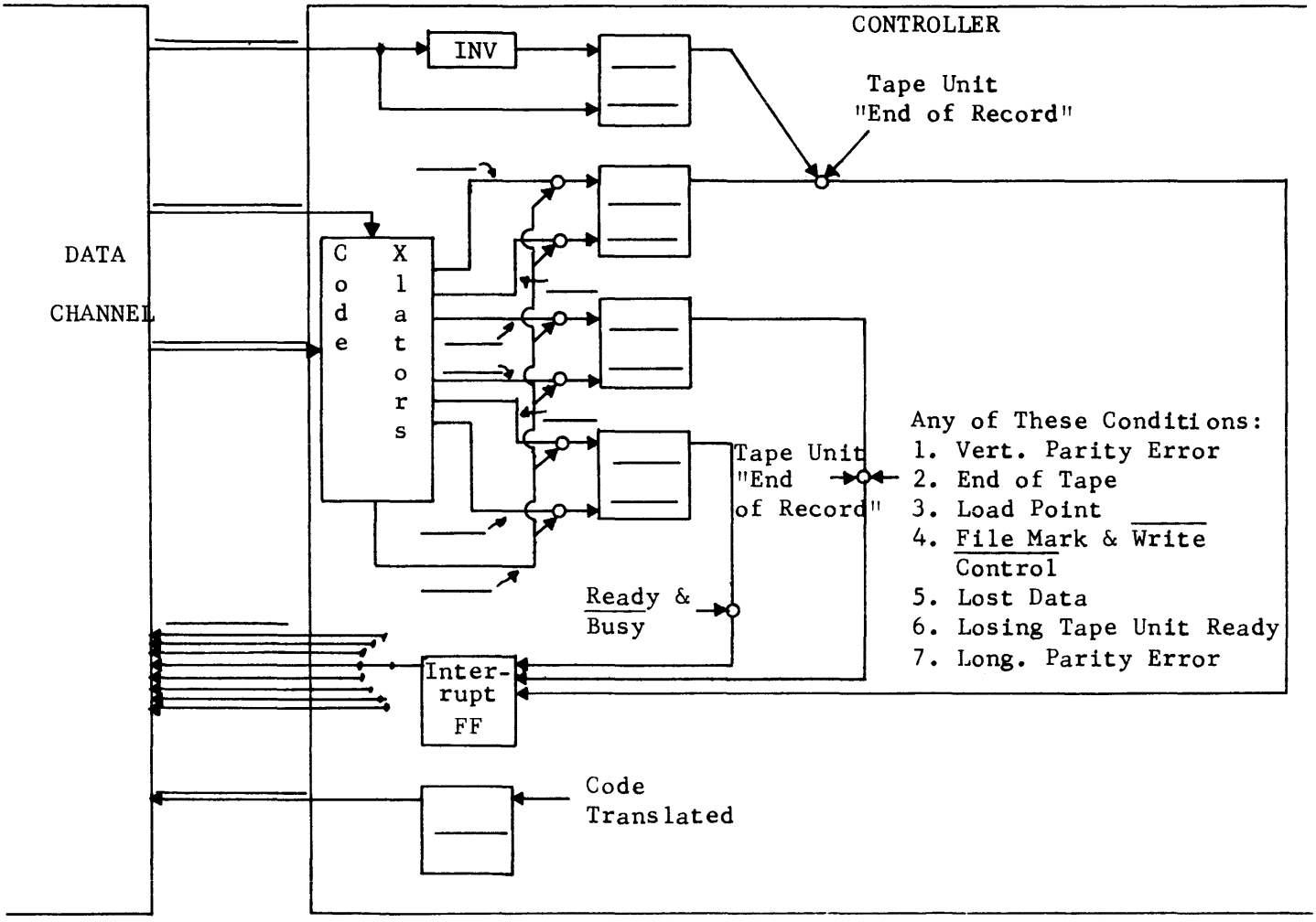
3. Describe the difference between a "Release" and "Clear" instruction.

4. The controller is no longer connected to the Channel after the "Release" has been performed. T F

5. What instructions may be performed after a "Clear" instruction?

XIII. INTERRUPT SELECTIONS AND RELEASES

1. Complete the following Block Diagram.



2. What is the purpose of the Interrupt Circuits?

3. What prevents a "Reject" Signal when selecting or releasing an Interrupt?

4. If all three Interrupts have been selected, can the programmer determine the type of Interrupt generated?

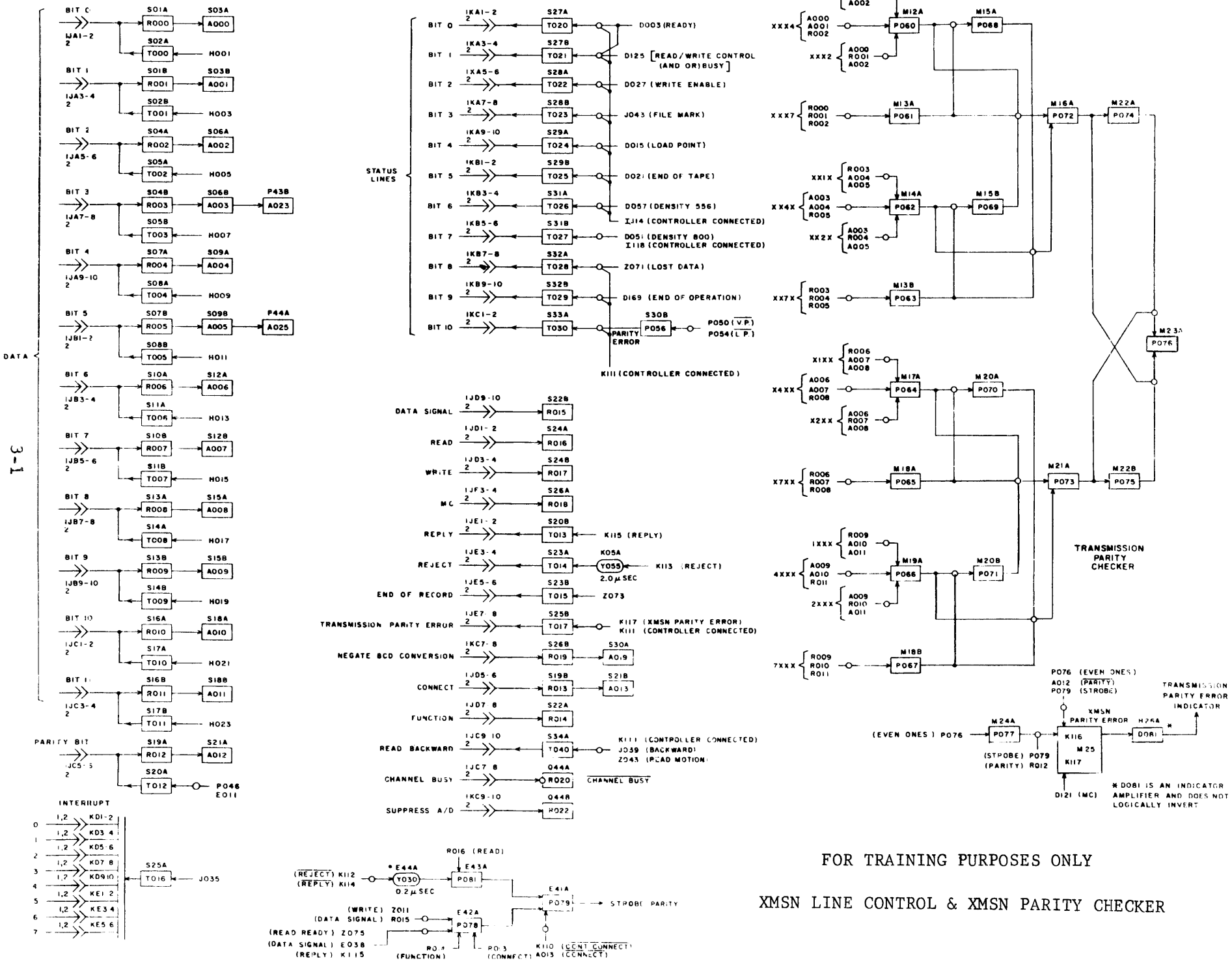
5. What Interrupt conditions will disable the Read and Write Circuits?

6. What can clear the Interrupt FF J034/035 if it has set?

CHAPTER III

LOGIC DIAGRAMS

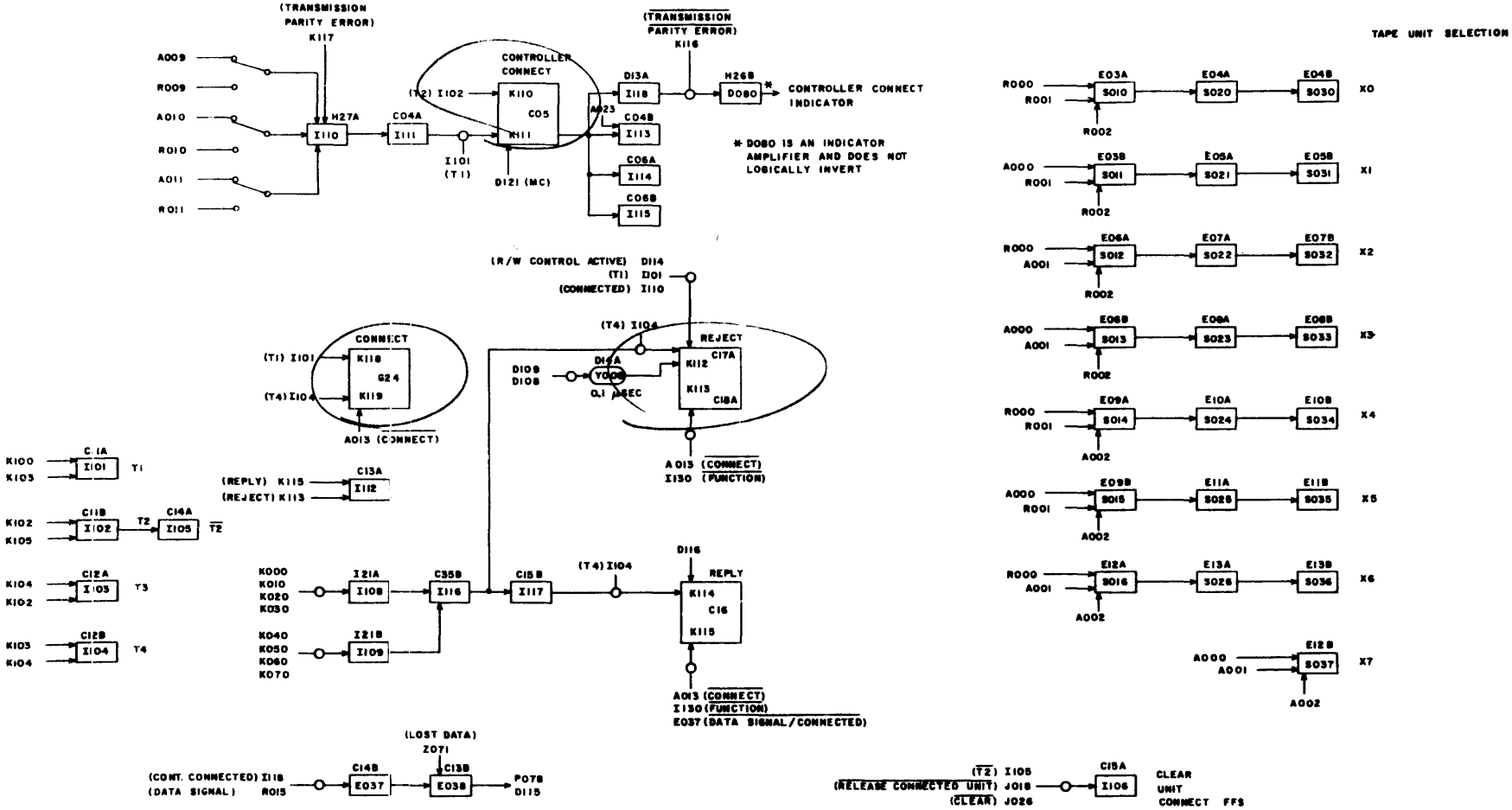
TERM	LOCATION	PAGE	DEFINITION
D003	I26A	3-25	Ready
D015	I28A	3-25	Load Point
D021	I29A	3-25	End of Tape
D027	I30A	3-25	Write Enable
D051	I34B	3-27	800 BPI
D057	H22B	3-27	556 BPI
D121	D05B	3-7	Master Clear
D125	D43B	3-7	Read/Write Control and/or Busy
D169	L07B	3-7	E.O.P.
E011	D29A	3-15	Read
E038	C13B	3-3	Connect·Data Sig·Lost Data
H001	K20	3-19	Bit 0
H003	K21	3-19	Bit 1
H005	K22	3-19	Bit 2
H007	K23	3-19	Bit 3
H009	K24	3-19	Bit 4
H011	K25	3-19	Bit 5
H013	K26	3-19	Bit 6
H015	K27	3-19	Bit 7
H017	K28	3-19	Bit 8
H019	K29	3-19	Bit 9
H021	K30	3-19	Bit 10
H023	K31	3-19	Bit 11
I114	C06A	3-3	Cont. Connect
I118	D13A	3-3	Cont. Connect
J035	D07A	3-7	Interrupt
J039	C41	3-7	Backward
J043	I37	3-25	File Mark
K110	C05	3-3	Cont. Connect
K111	C05	3-3	Cont. Connect
K112	C17A	3-3	Reject
K113	C18A	3-3	Reject
K114	C16	3-3	Reply
K115	C16	3-3	Reply
P046	M44B	3-19	Even Bits
P050	E39A	3-19	Vertical Parity Error
P054	J18	3-21	Longitudinal Parity Error
Z011	F30	3-9	R to 0
Z043	D31A	3-15	Read Motion
Z071	C03	3-9	Lost Data
Z073	D25	3-15	End or Record Disconnect
Z075	D26	3-15	Read Ready



FOR TRAINING PURPOSES ONLY

XMSN LINE CONTROL & XMSN PARITY CHECKER

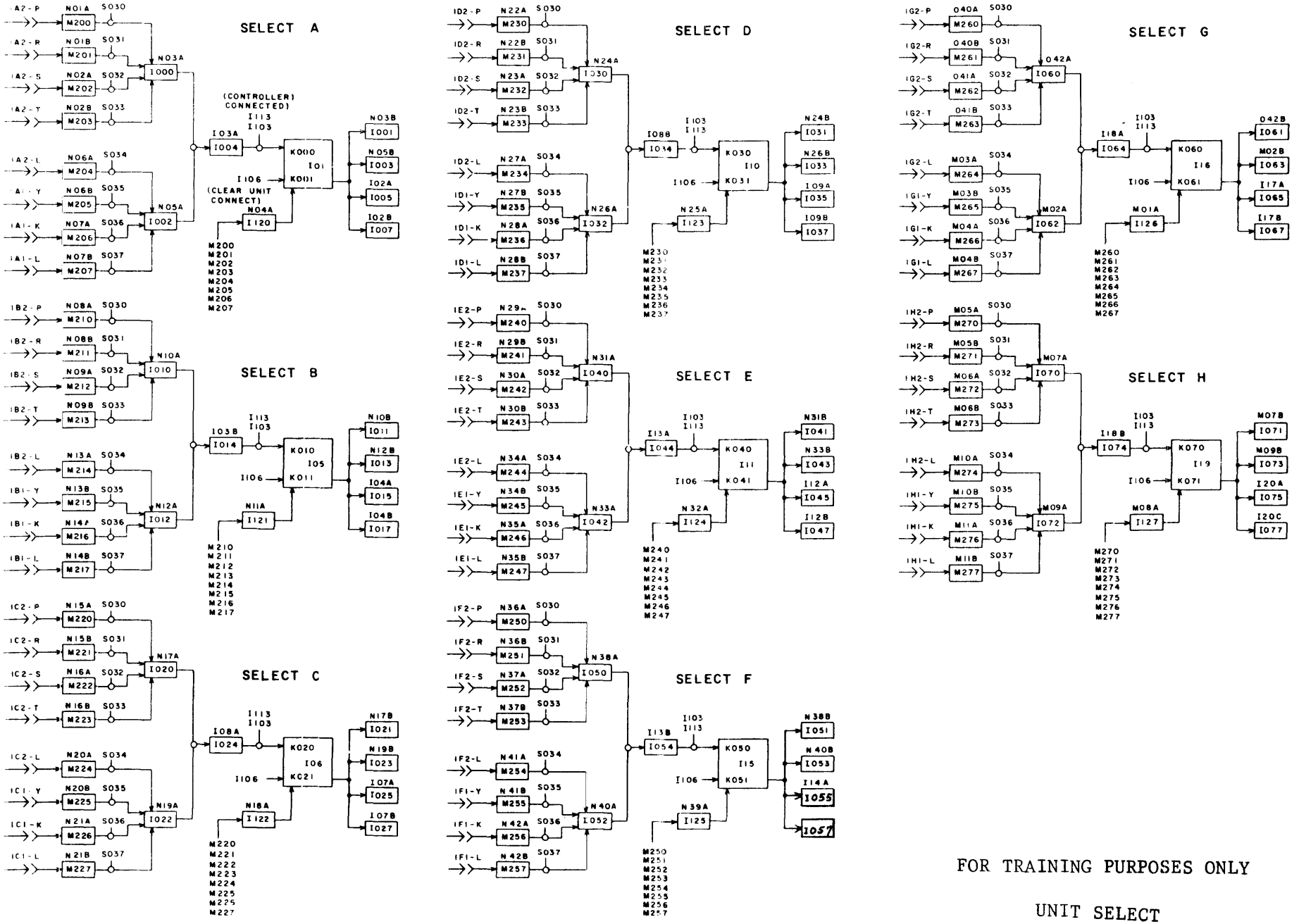
TERM	LOCATION	PAGE	DEFINITION
A002	S06A	3-1	$\overline{\text{Bit 2}}$
A009	S15B	3-1	Bit 9
A010	S18A	3-1	Bit 10
A011	S18B	3-1	Bit 11
A013	S21B	3-1	Connect Signal
A023	P43B	3-1	Bit 3
D108	C22A	3-7	Function Signal · $\overline{\text{2X}}$
D109	D37A	3-7	1X · 0X · 4X
D114	D43A	3-7	Read/Write Control
D115	D39A	3-7	Reply
D116	D40A	3-7	Reply
D121	D05B	3-7	Master Clear
I130	C32B	3-7	Function + Connect
J018	C33	3-7	Release
J026	C40	3-7	Clear
K000	I01	3-5	Select A
K010	I05	3-5	Select B
K020	I06	3-5	Select C
K030	I10	3-5	Select D
K040	I11	3-5	Select E
K050	I15	3-5	Select F
K060	I16	3-5	Select G
K070	I19	3-5	Select H
K116	M25	3-1	XMSN Parity Error
K117	M25	3-1	XMSN Parity Error
P078	E43A	3-1	Connect + Function + Data Sig.
R000	S01A	3-1	Bit 0
R001	S01B	3-1	Bit 1
R002	S04A	3-1	Bit 2
R009	S13B	3-1	Bit 9
R010	S16A	3-1	Bit 10
R011	S16B	3-1	Bit 11
R013	S19B	3-1	Connect Signal
R015	S22B	3-1	Data Signal
Z071	C03	3-9	Lost Data



FOR TRAINING PURPOSES ONLY

UNIT CONNECTION

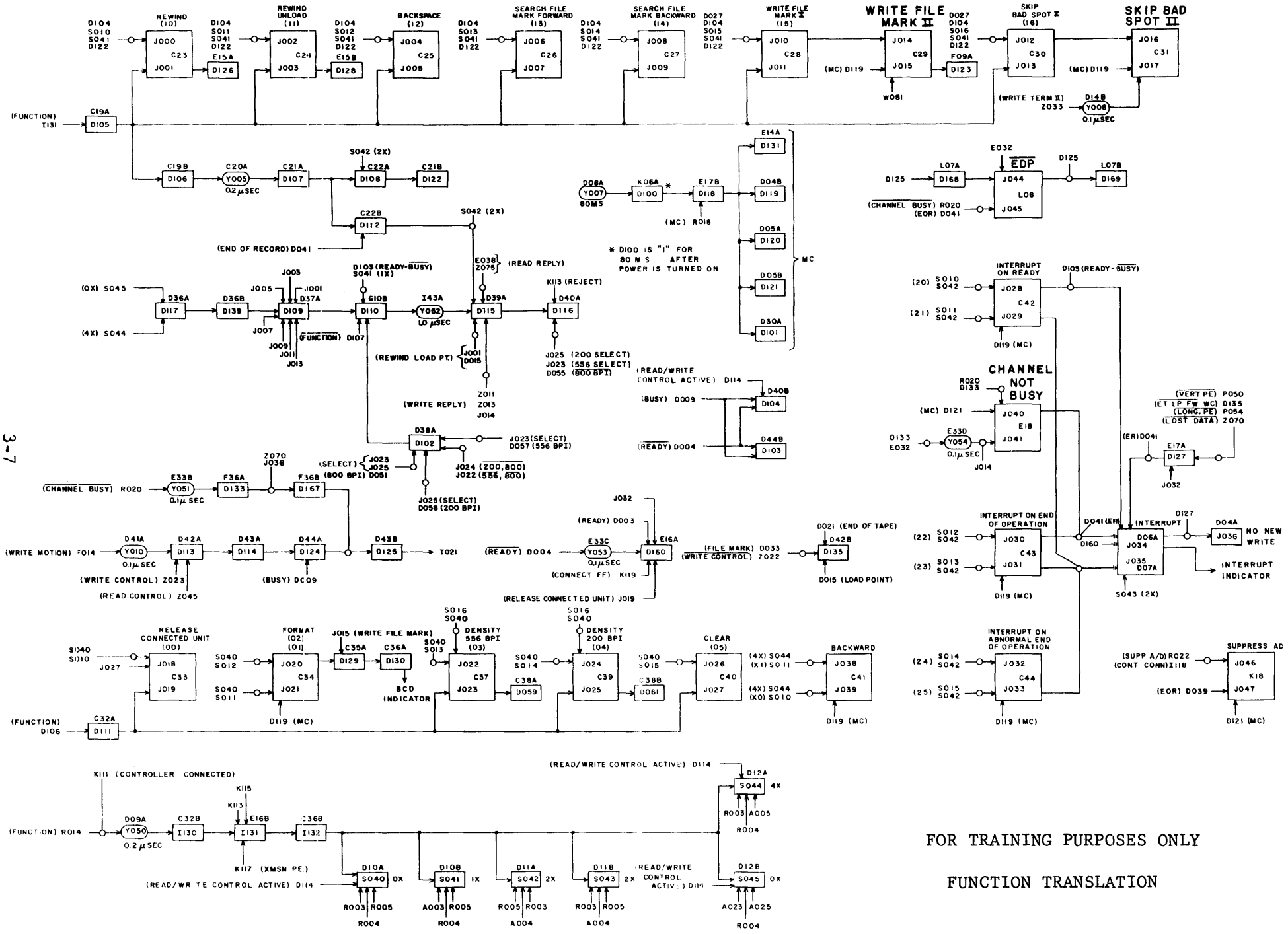
TERM	LOCATION	PAGE	DEFINITION
I103	C12A	3-3	Connect Time 3
I106	C15A	3-3	T2 + Release + Clear
I113	C04B	3-3	Controller Connect
S030	E04B	3-3	X0
S031	E05B	3-3	X1
S032	E07B	3-3	X2
S033	E08B	3-3	X3
S034	E10B	3-3	X4
S035	E11B	3-3	X5
S036	E13B	3-3	X6
S037	E14B	3-3	X7



FOR TRAINING PURPOSES ONLY

UNIT SELECT

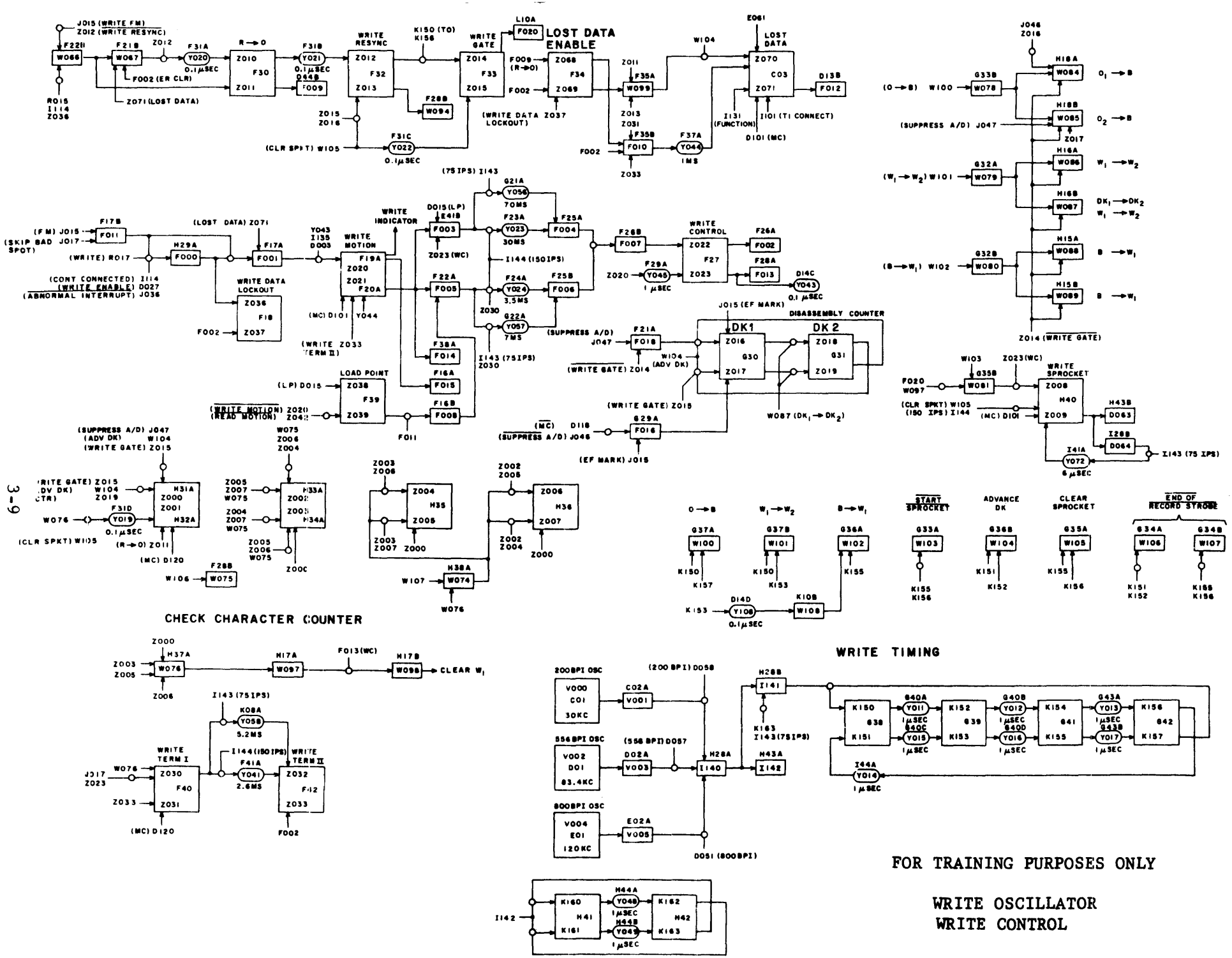
TERM	LOCATION	PAGE	DEFINITION
A003	S06B	3-1	Bit 3
A004	S09A	3-1	Bit 4
A005	S09B	3-1	Bit 5
A023	P43B	3-1	Bit 3
A025	P44A	3-1	Bit 5
D003	I26A	3-25	Ready
D004	I26B	3-25	Ready
D009	I27A	3-25	Busy
D015	I28A	3-25	Load Point
D021	I29A	3-25	End of Tape
D027	L30A	3-25	Write Enable
D033	I31A	3-25	File Mark
D039	I32A	3-27	End of Record
D041	I34A	3-27	End of Record
D051	I34B	3-27	800 BPI
D055	H29B	3-27	800 BPI
D057	H22B	3-27	556 BPI
D058	G20B	3-27	200 BPI
E032	J22B	3-21	Begin New Record
E038	C13B	3-3	Connected·Data·L.Data
F014	F38A	3-9	Write Motion
I118	D13A	3-3	Controller Connect
K111	C05	3-3	Controller Connect
K113	C18A	3-3	Reject
K115	C16	3-3	Reply
K117	M25	3-1	XMSN Parity Error
K119	G24	3-3	Connect FF
P050	E39A	3-19	Vertical Parity Error
P054	J18	3-21	Longitudinal P.E.
R003	S04B	3-1	Bit 3
R004	S07A	3-1	Bit 4
R005	S07B	3-1	Bit 5
R014	S22A	3-1	Function Signal
R018	S26A	3-1	Master Clear
R020	Q44B	3-1	Channel Busy
R022	Q44B	3-1	Suppress A/D
S010	E03A	3-3	X0
S011	E03B	3-3	X1
S012	E06A	3-3	X2
S013	E06B	3-3	X3
S014	E09A	3-3	X4
S015	E09B	3-3	X5
S016	E12A	3-3	X6
T021	S27B	3-1	R/W Cont. and/or Busy
W081	G35B	3-9	Write Sprocket (T3)
Z011	F30	3-9	R to 0
Z013	F32	3-9	Write Resync
Z022	F27	3-9	Write Control
Z023	F27	3-9	Write Control
Z033	F42	3-9	Write Terminate II
Z045	D34	3-5	Read Control
Z070	C03	3-9	Lost Data
Z075	D26	3-5	Read Ready



FOR TRAINING PURPOSES ONLY

FUNCTION TRANSLATION

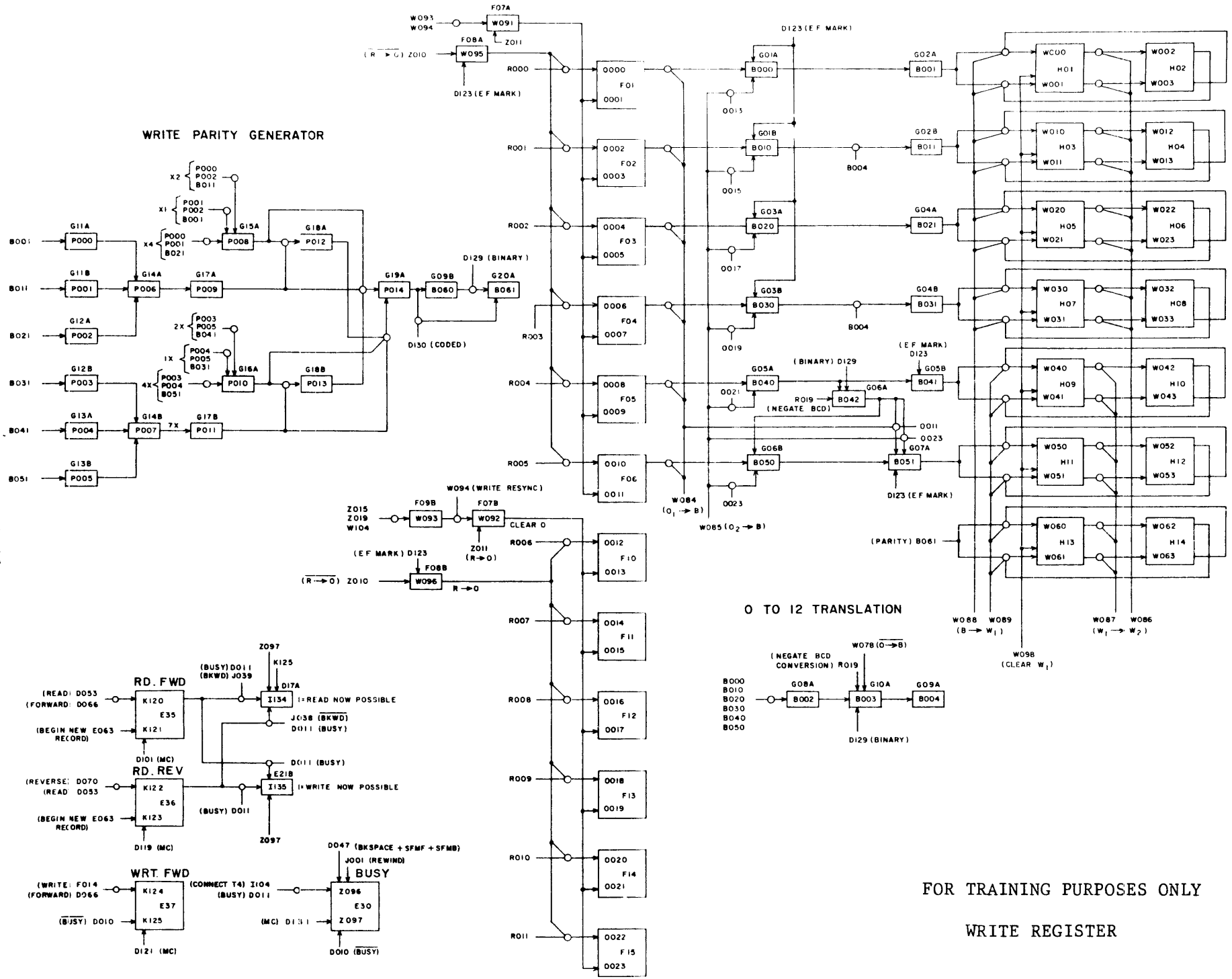
TERM	LOCATION	PAGE	DEFINITION
D003	I26A	3-25	Ready
D015	I28A	3-25	Load Point
D027	I30A	3-25	Write Enable
D045	D15B	3-15	
D051	I34B	3-27	800 BPI
D057	H22B	3-37	556 BPI
D058	G20B	3-27	200 BPI
D101	D30A	3-7	Master Clear
D118	E17B	3-7	Master Clear
D120	D05A	3-7	Master Clear
D124	D44A	3-7	Read/Write Control And/Or Busy
E061	L12A	3-15	Lost Data
I101	C11A	3-3	Connect Time
I114	C06A	3-3	Controller Connected
I131	E16B	3-7	Translate Function Code
I135	E21B	3-11	Write Possible
I143	K07A	3-15	75 IPS
I144	K06B	3-15	150 IPS
J015	C29	3-7	Write File Mark
J017	C31	3-7	Skip Bad Spot
J036	D04A	3-7	Abnormal EOP Interrupt
J046	K18A	3-7	Suppress A/D
J047	K18C	3-7	Suppress A/D
R015	S22B	3-1	Data Signal
R017	S24B	3-1	Write Signal
R022	Q44B	3-1	Suppress A/D
Z042	D30A	3-15	Read Motion
Z075	D26	3-15	Read Ready



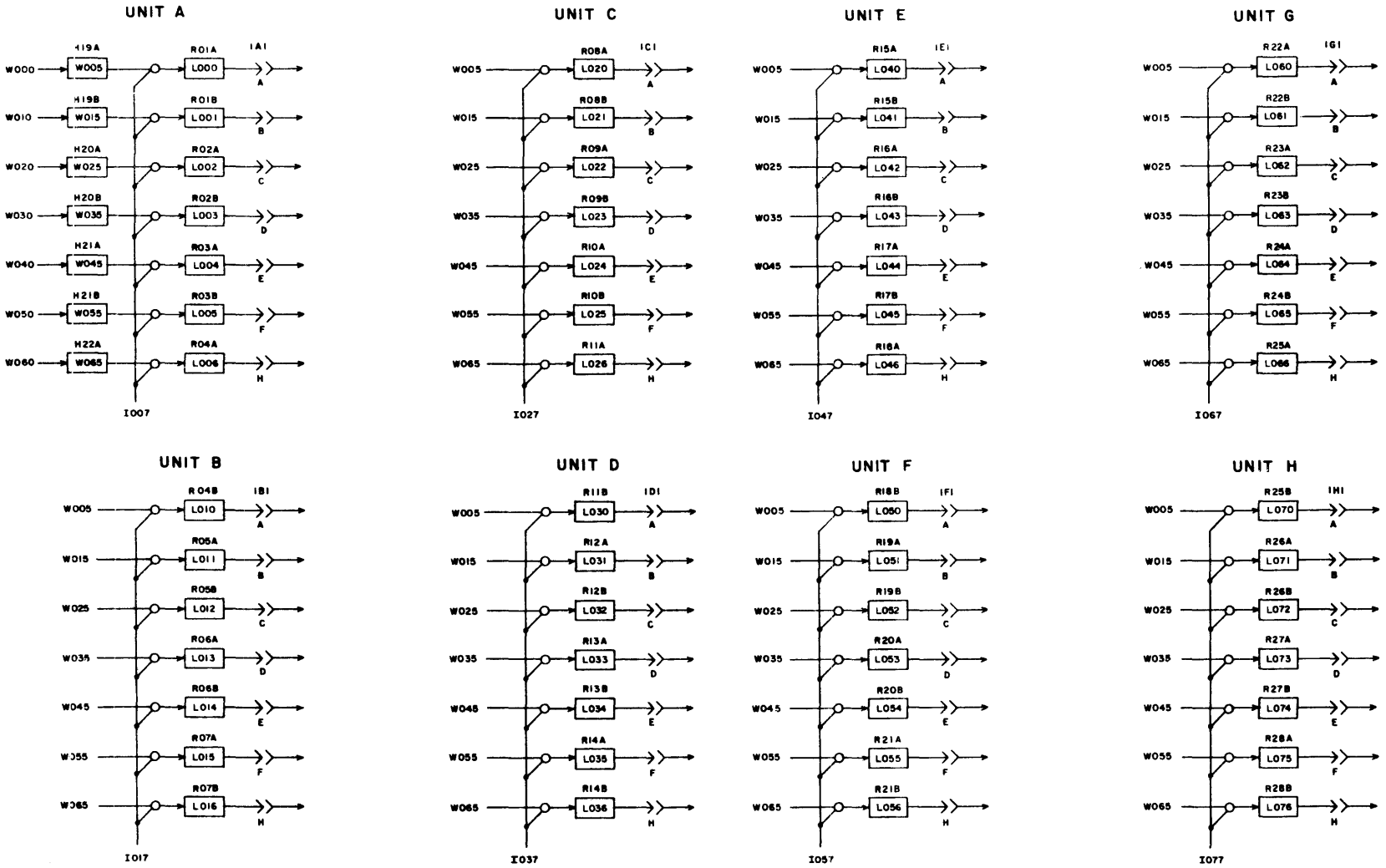
FOR TRAINING PURPOSES ONLY

WRITE OSCILLATOR
WRITE CONTROL

TERM	LOCATION	PAGE	DEFINITION
D010	E14B	3-25	$\overline{\text{Busy}}$
D011	M44A	3-25	Busy
D047	I24A	3-23	Read
D053	I25	3-23	$\overline{\text{Read}}$
D066	L10B	3-23	Reverse
D070	I36A	3-23	Reverse
D101	D30A	3-7	Master Clear
D119	D04B	3-7	Master Clear
D121	D05B	3-7	Master Clear
D123	F09A	3-7	Write File Mark
D129	C35A	3-7	Binary
D130	C36A	3-7	BCD
D131	E14A	3-7	Master Clear
E063	H30B	3-21	Begin New Record
F014	F38A	3-9	Write Motion
I104	C12B	3-3	Connect Time 4
J001	C23	3-7	Rewind
J038	C41	3-7	Backward
J039	C41	3-7	Backward
R000	S01A	3-1	Bit 0
R001	S01B	3-1	Bit 1
R002	S04A	3-1	Bit 2
R003	S04B	3-1	Bit 3
R004	S07A	3-1	Bit 4
R005	S07B	3-1	Bit 5
R006	S10A	3-1	Bit 6
R007	S10B	3-1	Bit 7
R008	S13A	3-1	Bit 8
R009	S13B	3-1	Bit 9
R010	S16A	3-1	Bit 10
R011	S16B	3-1	Bit 11
R019	S26B	3-1	Negate BCD Conversion)
W078	G33B	3-9	$0 \longrightarrow B$
W084	H18A	3-9	$0_1 \longrightarrow B$ (T1, T2, T3)
W085	H18B	3-9	$0_2 \longrightarrow B$ (T1, T2, T3)
W086	H16A	3-9	$W_1 \longrightarrow W_2$ (T1)
W087	H16B	3-9	$W_1 \longrightarrow W_2$ (T1)
W088	H15A	3-9	$B \longrightarrow W_1$
W089	H15A	3-9	$B \longrightarrow W_1$
W094	F28B	3-9	Write Resync
W098	H17B	3-9	Clear W_1
W104	G36B	3-9	Advance DK (T5)
Z010	F30	3-9	$R \longrightarrow 0$
Z011	F30	3-9	$R \longrightarrow 0$
Z015	F33	3-9	Write Gate
Z019	G31	3-9	DK II


WRITE PARITY GENERATOR
RD. FWD
RD. REV
WRT. FWD
BUSY
0 TO 12 TRANSLATION
(NEGATE BCD CONVERSION) R019
(CLEAR W1)
FOR TRAINING PURPOSES ONLY
WRITE REGISTER

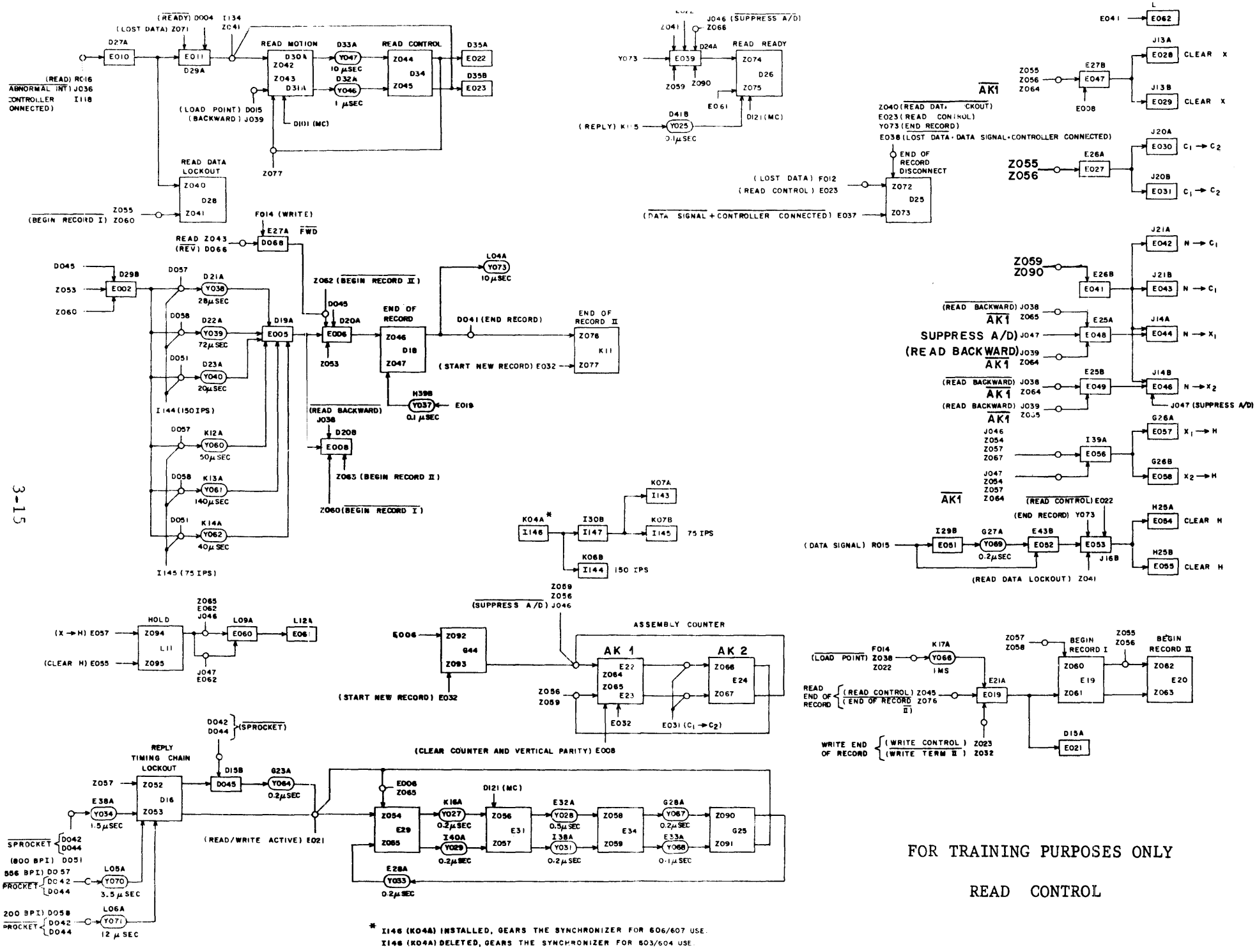
TERM	LOCATION	PAGE	DEFINITION
I007	I02B	3-5	Select A
I017	I04B	3-5	Select B
I027	I07B	3-5	Select C
I037	I09B	3-5	Select D
I047	I12B	3-5	Select E
I057	I14B	3-5	Select F
I067	I17B	3-5	Select G
I077	I20C	3-5	Select H
W000	H01	3-11	Write FF (Track 0)
W010	H03	3-11	Write FF (Track 1)
W020	H05	3-11	Write FF (Track 2)
W030	H07	3-11	Write FF (Track 3)
W040	H09	3-11	Write FF (Track 4)
W050	H11	3-11	Write FF (Track 5)
W060	H13	3-11	Write FF (Track 6)



FOR TRAINING PURPOSES ONLY

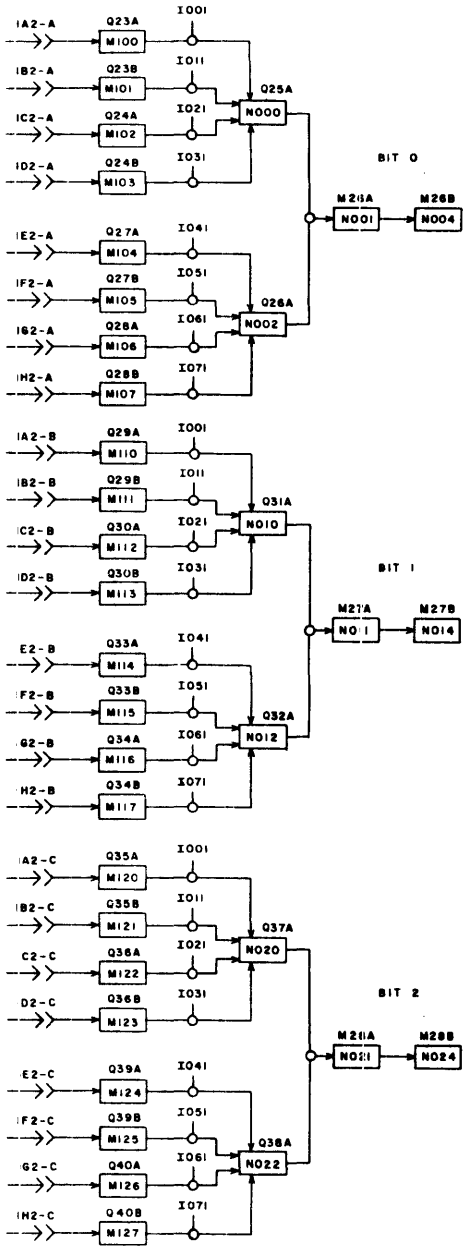
DATA OUTPUT

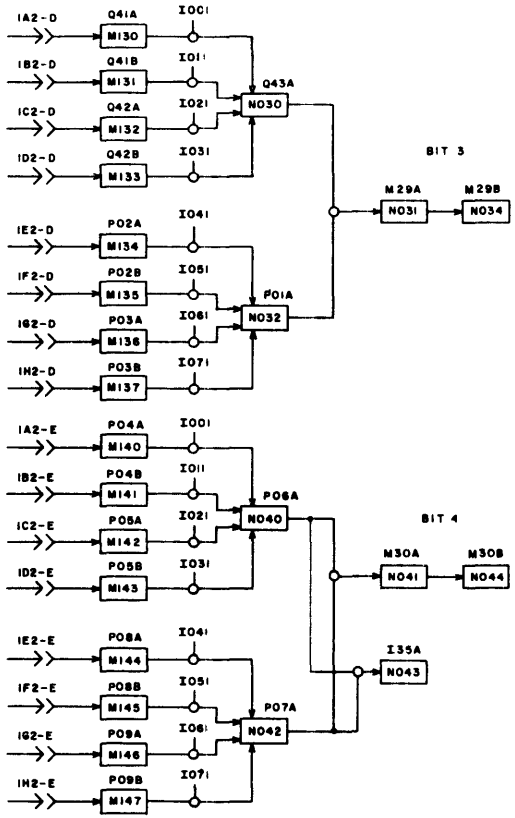
TERM	LOCATION	PAGE	DEFINITION
D004	I26B	3-25	$\overline{\text{Ready}}$
D015	I28A	3-25	Load Point
D039	I32A	3-27	End Of Record
D041	I34A	3-27	$\overline{\text{End Of Record}}$
D042	O30A	3-27	$\overline{\text{Read Sprocket}}$
D044	O31A	3-27	Read Sprocket
D051	I34B	3-27	800 BPI
D057	H22B	3-27	556 BPI
D058	G20B	3-27	$\overline{\text{200 BPI}}$
D066	L10B	3-23	Reverse
D101	D30A	3-7	Master Clear
D120	D05A	3-7	Master Clear
D121	D05B	3-7	Master Clear
D124	D44A	3-7	Read/Write Control And/Or Busy
E032	J22B	3-21	$\overline{\text{Begin New Record}}$
E037	C14B	3-3	Connected + Data
E038	C13B	3-3	Connected . Data . $\overline{\text{Lost Data}}$
F012	D13B	3-9	Lost Data
F014	F38A	3-9	Write Motion
I118	D13A	3-3	Controller Connect
I134	D17A	3-11	Read Possible
J036	D04A	3-7	$\overline{\text{Abnormal}}$ EOP Interrupt
J038	C41	3-7	$\overline{\text{Backward}}$
J039	C41	3-7	$\overline{\text{Backward}}$
J046	K18A	3-7	Suppress A/D
J047	K18C	3-7	Suppress A/D
K115	C16	3-3	Reply
R015	S22B	3-1	Data Signal
R016	S24A	3-1	$\overline{\text{Read Signal}}$
Z022	F27	3-9	Write Control
Z023	F27	3-9	Write Control
Z032	F42	3-9	$\overline{\text{Write Terminate II}}$
Z038	F39	3-9	$\overline{\text{Load Point}}$
Z070	C03	3-9	Lost Data
Z071	C03	3-9	Lost Data

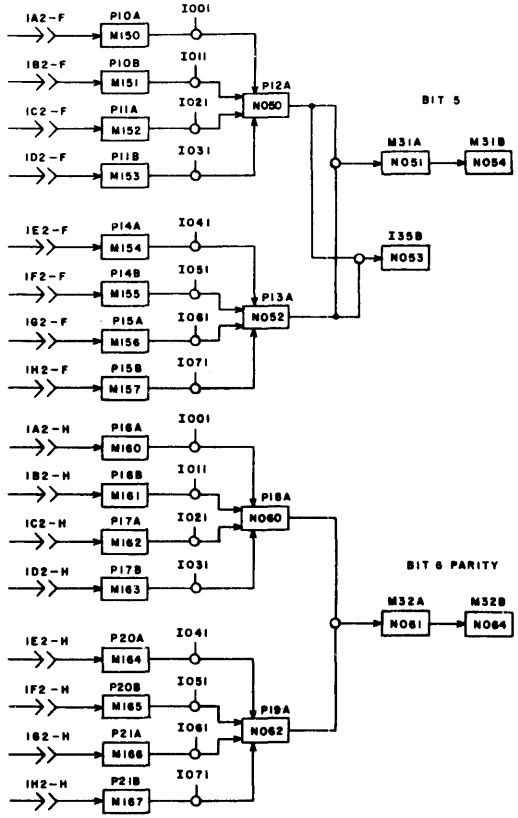


* I146 (K04A) INSTALLED, GEARS THE SYNCHRONIZER FOR 606/607 USE.
I146 (K04A) DELETED, GEARS THE SYNCHRONIZER FOR 603/604 USE.

TERM	LOCATION	PAGE	DEFINITION
I001	N03B	3-5	Select A
I011	N10B	3-5	Select B
I021	N17B	3-5	Select C
I031	N24B	3-5	Select D
I041	N13B	3-5	Select E
I051	N38B	3-5	Select F
I061	042B	3-5	Select G
I071	M07B	3-5	Select H



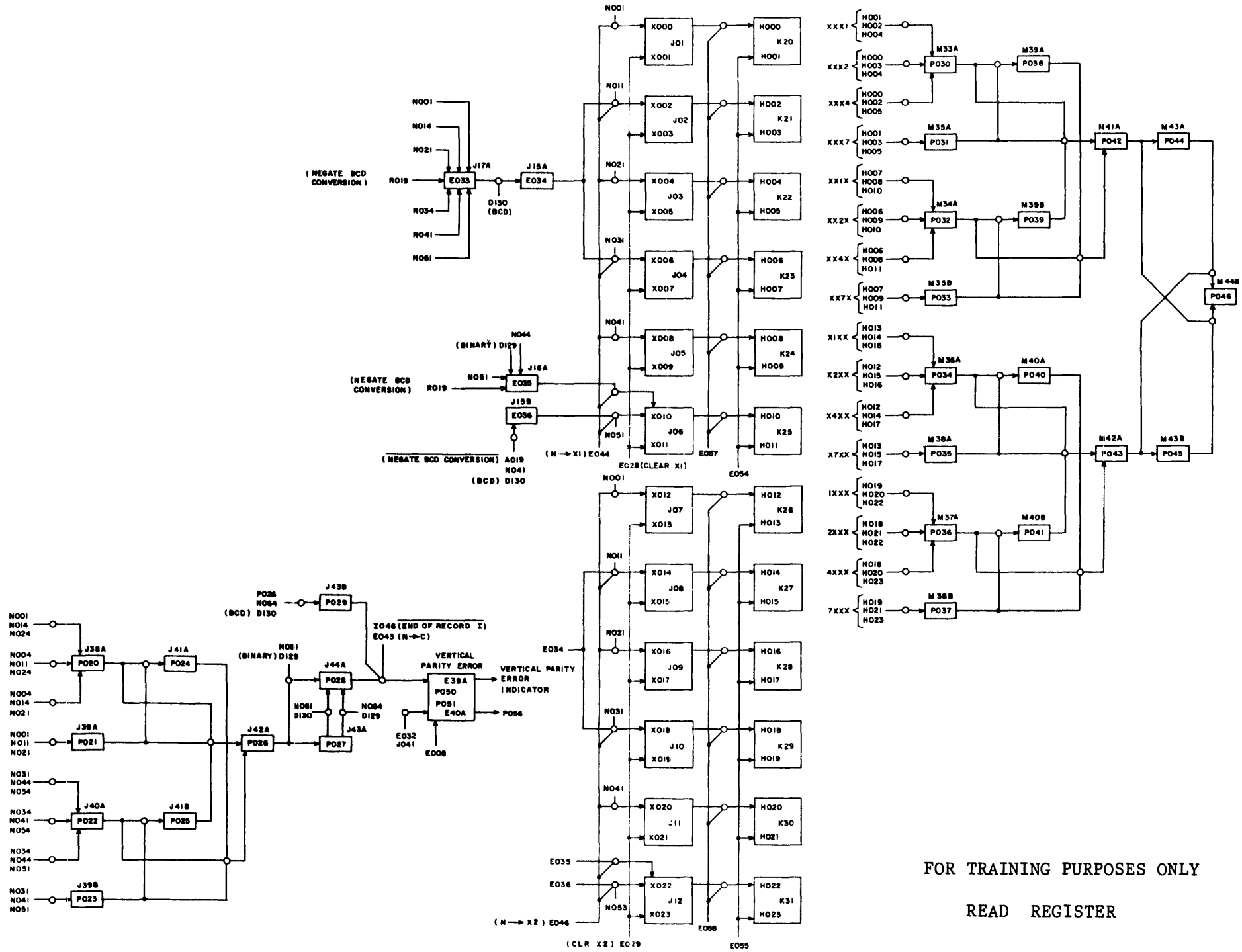




FOR TRAINING PURPOSES ONLY

READ REPLIES FROM 606

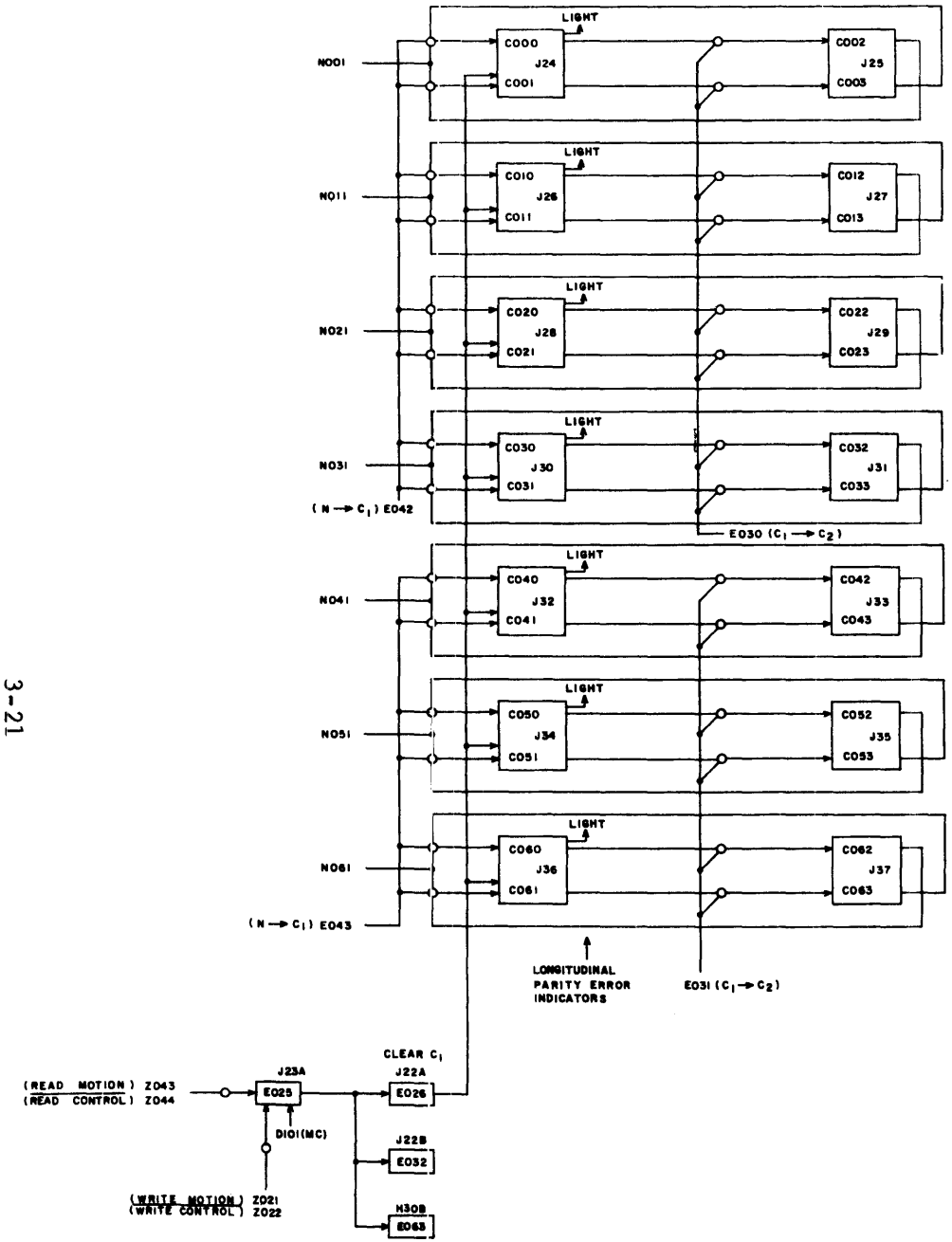
TERM	LOCATION	PAGE	DEFINITION
A019	S30A	3-1	Negate BCD Conversion
D129	C35A	3-7	Binary
D130	C36A	3-7	BCD
E008	D20B	3-15	Read Backward
E029	J13B	3-15	Clear X
E032	J22B	3-21	Begin New Record
E043	J21B	3-15	N C_1
E046	J14B	3-15	N X_2
E054	H25A	3-15	Clear H
E055	H25B	3-15	Clear H
E057	G26A	3-15	X_1 H
E058	G26B	3-15	X_2 H
J041	E18	3-7	Channel Busy
N001	M26A	3-17	Bit 0
N011	M27A	3-17	Bit 1
N014	M27B	3-17	Bit 1
N021	M28A	3-17	Bit 2
N031	M29A	3-17	Bit 3
N034	M29B	3-17	Bit 3
N041	M30A	3-17	Bit 4
N044	M30B	3-17	Bit 4
N051	M31A	3-17	Bit 5
N053	M35B	3-17	Bit 5
N061	M32A	3-17	Bit 6
N064	M32B	3-17	Bit 6
P056	S30B	3-1	Parity Error
R019	S26B	3-1	Negate BCD Conversion
Z046	D18	3-5	End Of Record

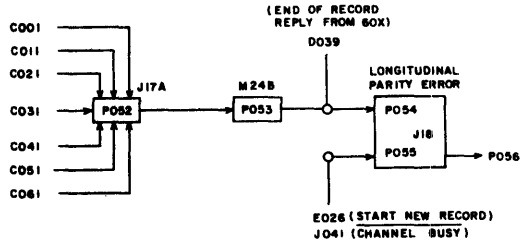


FOR TRAINING PURPOSES ONLY

READ REGISTER

TERM	LOCATION	PAGE	DEFINITION
D039	I32A	3-27	End of Record
D101	D30A	3-7	Master Clear
E030	J20A	3-15	C_1 C_2 (T1)
E031	J20B	3-15	C_1 C_2 (T1)
E042	J21A	3-15	N C_1 (T3)
E043	J21B	3-15	N C_1 (T3)
J041	E18	3-7	Channel Busy
N001	M26A	3-17	Bit 0
N011	M27A	3-17	Bit 1
N021	M28A	3-17	Bit 2
N031	M29A	3-17	Bit 3
N041	M30A	3-17	Bit 4
N051	M31A	3-17	Bit 5
N061	M32A	3-17	Bit 6
P056	S30B	3-1	Parity Error
Z021	F20A	3-9	Write Motion
Z022	F27	3-9	Write Control
Z043	D31A	3-15	Read Motion
Z044	D34	3-15	Read Control



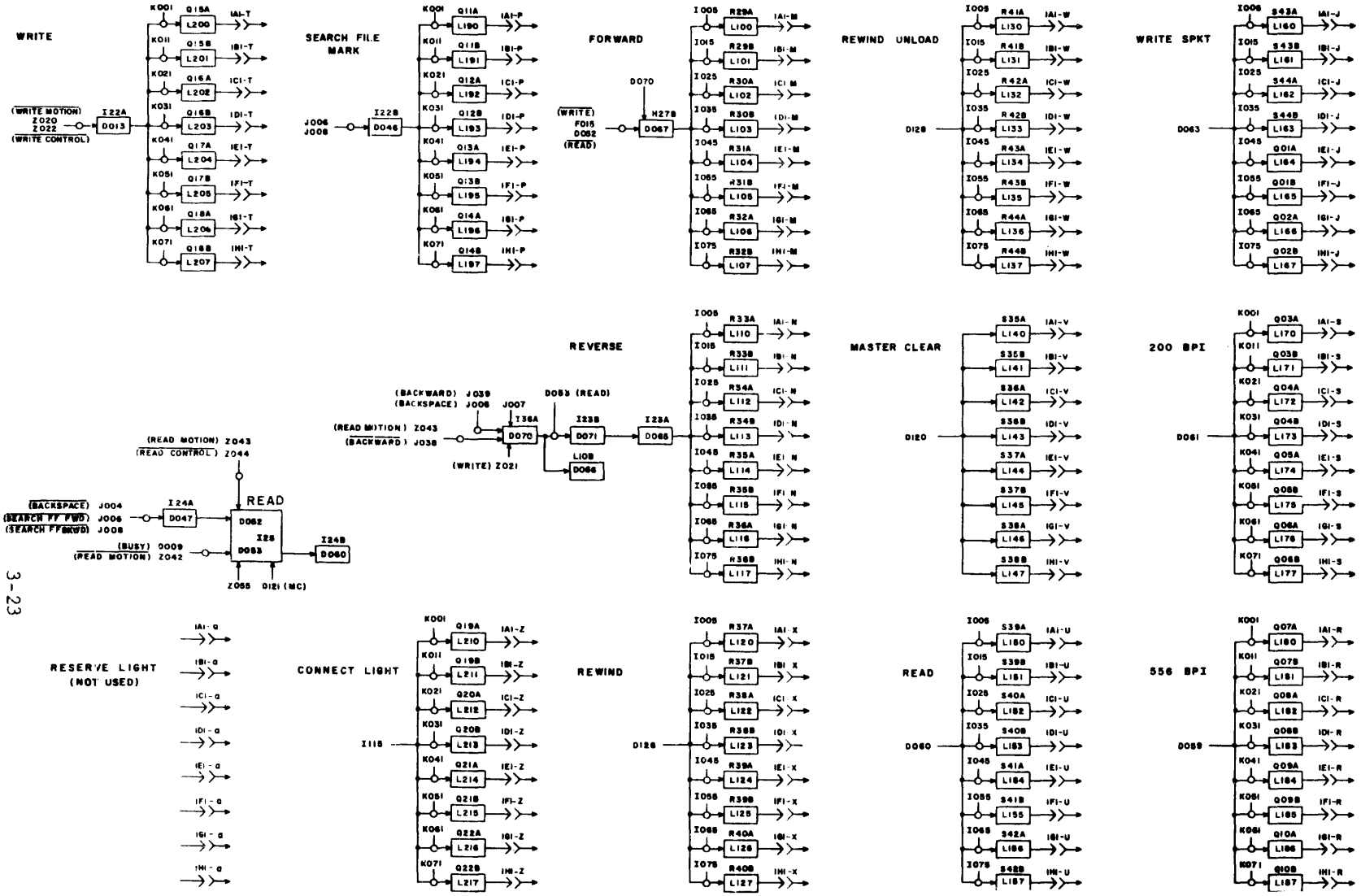


LONGITUDINAL PARITY CHECKER

FOR TRAINING PURPOSES ONLY

LONGITUDINAL PARITY CHECKER

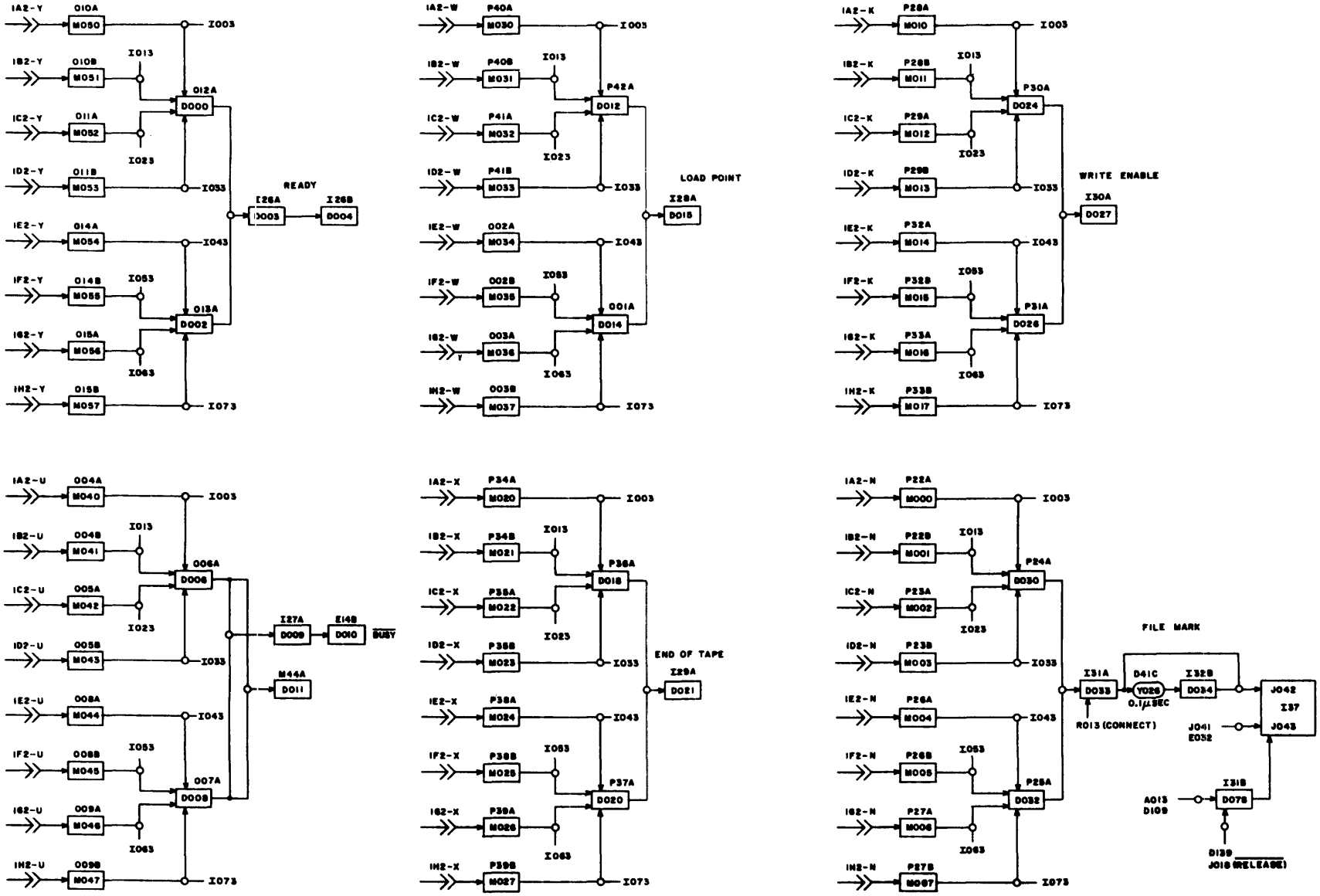
TERM	LOCATION	PAGE	DEFINITION
D009	I27A	3-25	Busy
D059	C38A	3-7	556 or 800 BPI
D061	C38B	3-5	200 or 800 BPI
D063	H43B	3-9	Write Sprocket
D120	D05A	3-7	Master Clear
D121	D05B	3-7	Master Clear
D126	E15A	3-7	Rewind
D128	E15B	3-7	Rewind Unload
F015	F16A	3-9	Write Motion
I005	I02A	3-5	Select A
I015	I04A	3-5	Select B
I025	I07A	3-5	Select C
I035	I09A	3-5	Select D
I045	I12A	3-5	Select E
I055	I14A	3-5	Select F
I065	I17A	3-5	Select G
I075	I20A	3-5	Select H
I115	C06B	3-3	Controller Connected
J004	C25	3-7	Backspace
J005	C25	3-7	Backspace
J006	C26	3-7	Search File Mark Forward
J007	C26	3-7	Search File Mark Forward
J008	C27	3-7	Search File Mark Backward
J038	C41	3-7	Backward
J039	C41	3-7	Backward
K001	I01	3-5	Select A
K011	I05	3-5	Select B
K021	I06	3-5	Select C
K031	I10	3-5	Select D
K041	I11	3-5	Select E
K051	I15	3-5	Select F
K061	I16	3-5	Select G
K071	I19	3-5	Select H
Z020	F19A	3-9	Write Motion
Z021	F20A	3-9	Write Motion
Z022	F27	3-9	Write Control
Z042	D30A	3-15	Read Motion
Z043	D31A	3-15	Read Motion
Z044	D34	3-15	Read Control
Z055	E30A	3-15	Read Time 1 + 2 + 3 + 4



FOR TRAINING PURPOSES ONLY

UNIT REQUESTS

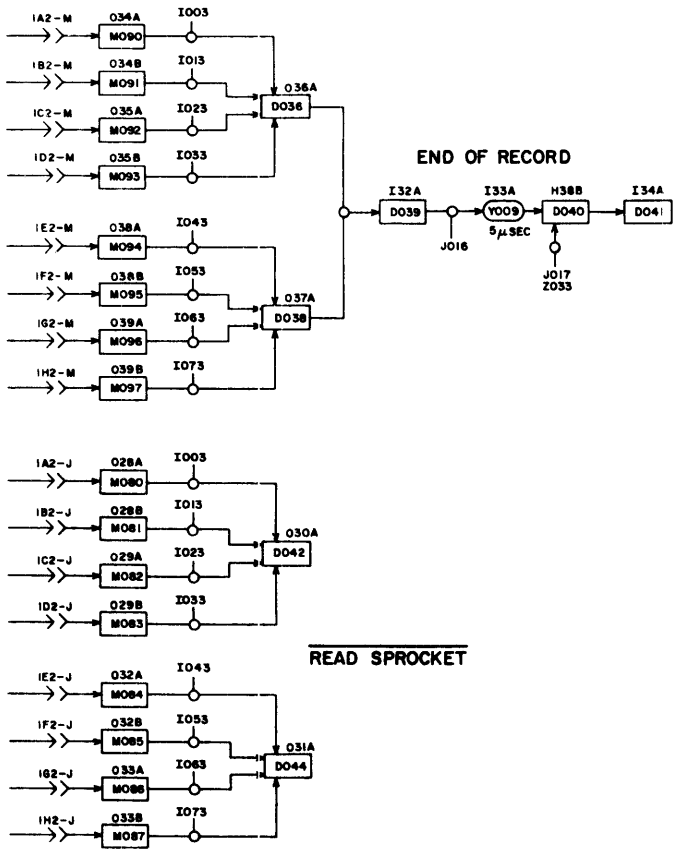
TERM	LOCATION	PAGE	DEFINITION
A013	S21B	3-3	Connect Signal
D109	D37A	3-7	$\overline{1X} + \overline{0X} + \overline{4X}$
D139	D36B	3-7	0X + 4X
E032	J22B	3-21	Begin New Record
I003	N05B	3-5	Select A
I013	N12B	3-5	Select B
I023	N19B	3-5	Select C
I033	N26B	3-5	Select D
I043	N33B	3-5	Select E
I053	N40B	3-5	Select F
I063	M02B	3-5	Select G
I073	M09B	3-5	Select H
J018	C33	3-7	Release
J041	E18	3-7	Channel Busy
R013	S19B		Connect Signal

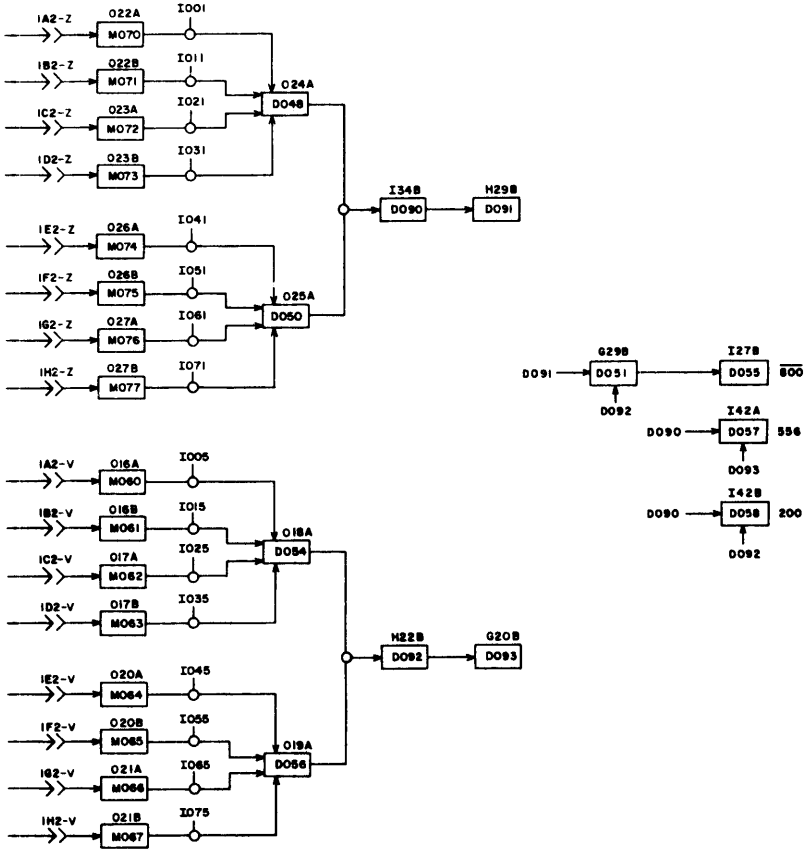


FOR TRAINING PURPOSES ONLY

REPLIES FROM 60X
(PART 1 OF 2)

TERM	LOCATION	PAGE	DEFINITION
I001	N03B	3-5	Select A
I003	N05B	3-5	Select A
I005	I02A	3-5	Select A
I011	N10B	3-5	Select B
I013	N12B	3-5	Select B
I015	I04A	3-5	Select B
I021	N17B	3-5	Select C
I023	N19B	3-5	Select C
I025	I07A	3-5	Select C
I031	N24B	3-5	Select D
I033	N26B	3-5	Select D
I035	I09A	3-5	Select D
I041	N13B	3-5	Select E
I043	N33B	3-5	Select E
I045	I12A	3-5	Select E
I051	N38B	3-5	Select F
I053	N40B	3-5	Select F
I055	I14A	3-5	Select F
I061	042B	3-5	Select G
I063	M02B	3-5	Select G
I065	I17A	3-5	Select G
I071	M07B	3-5	Select H
I073	M09B	3-5	Select H
I075	I20A	3-5	Select H
J016	C31	3-7	Skip Bad Spot
J017	C31	3-7	Skip Bad Spot
Z033	F42	3-9	Write Terminate II



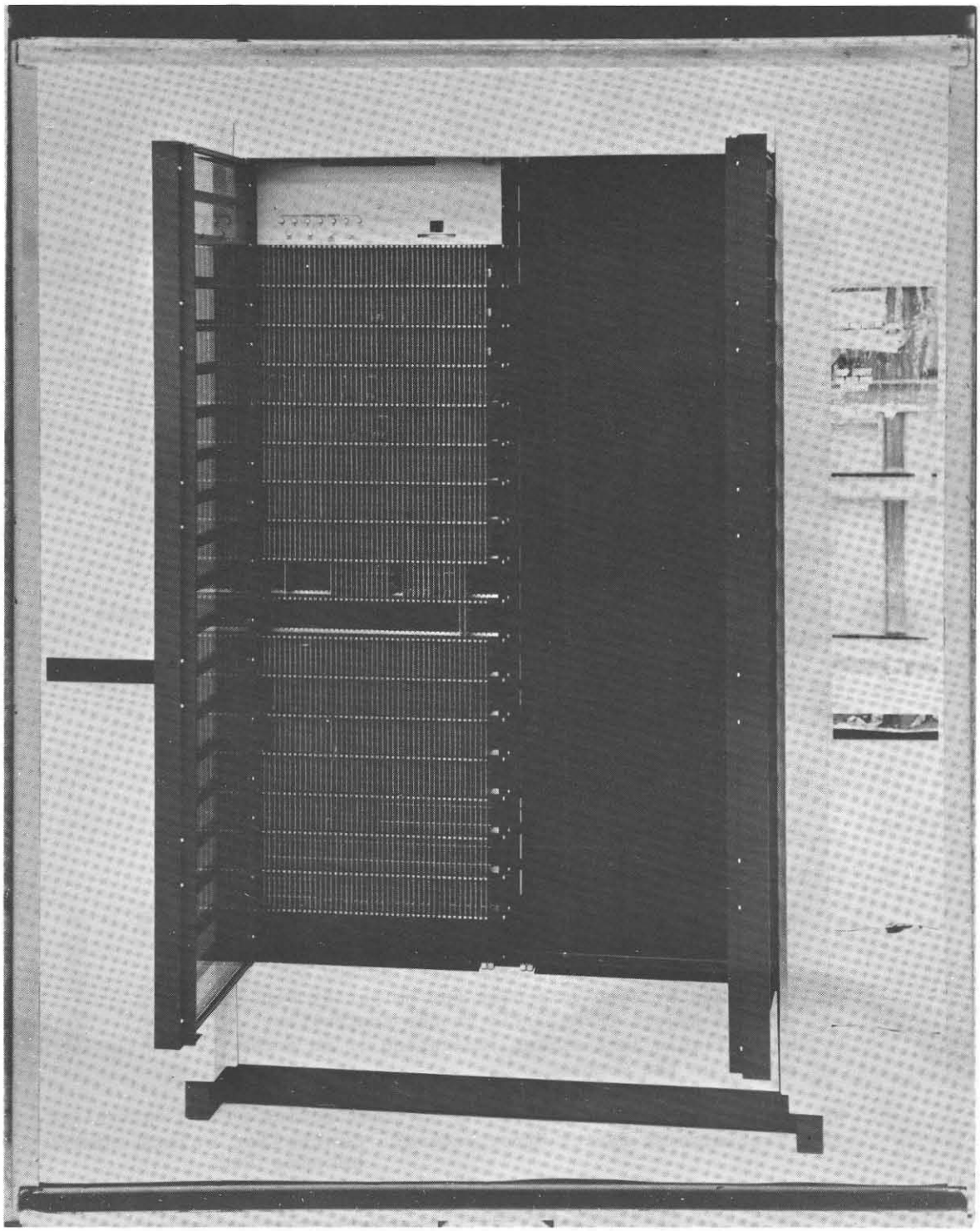


FOR TRAINING PURPOSES ONLY

REPLIES FROM 60X
(PART 2 OF 2)

APPENDIX A

STUDY PROBLEM ANSWERS

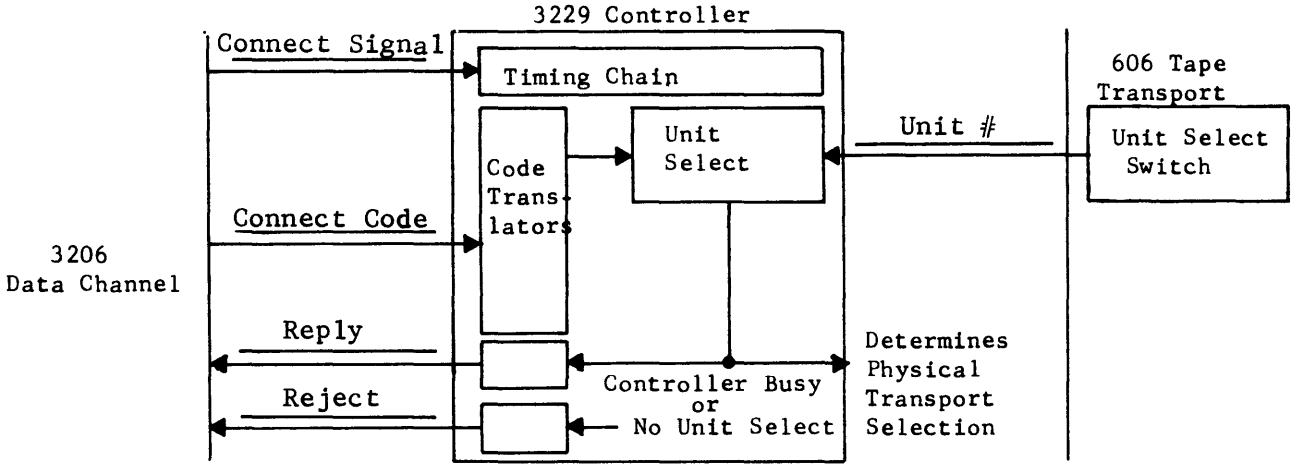


3228/3229 Magnetic Tape Controller

SECTION III STUDY PROBLEM ANSWERS

I. CONNECT OPERATION

1. Fill in the following block diagram signal flow.



2. The channel sends the Connect signal to start the Connect Timing Chain.

3. The 12 bit Connect Code contains what two pieces of information for the Magnetic Tape System.

   a. Controller #
   b. Unit #

4. Odd Parity is used with the Connect Code.

5. A Transmission Parity Error will:

		T	F
a.	be caused by odd data bits and a parity bit.	(T)	F
b.	be caused by odd data bits and no parity bit.	T	(F)
c.	be caused by even data bits and a parity bit.	T	(F)
d.	be caused by even data bits and no parity bit.	(T)	F
e.	set the Reject FF K112/113 in the controller.	T	(F)
f.	be available as a status indication if an error occurs on the Connect.	T	(F)

6. What visual indication will the programmer notice on the controller if a Transmission Parity Error occurs? Controller select number becomes Red.

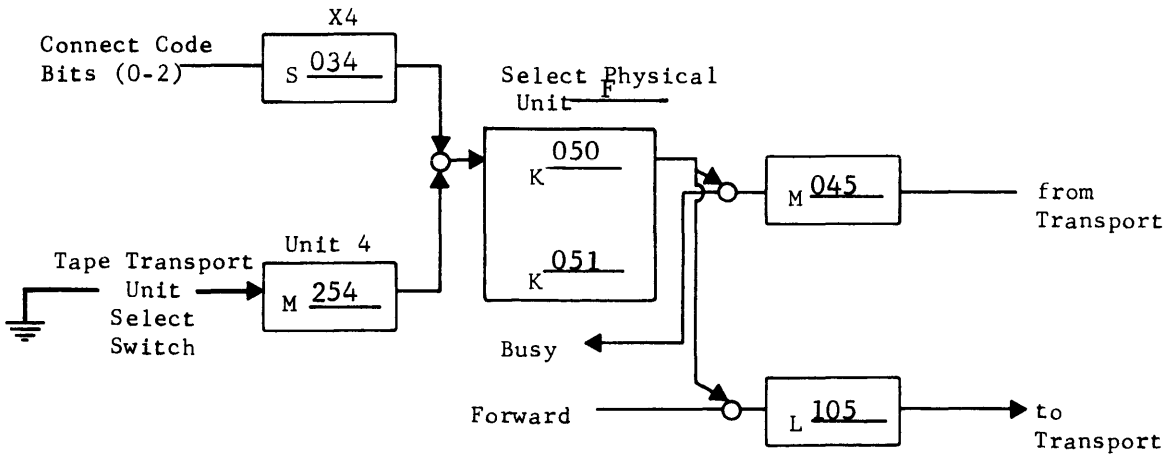
7. There are eight possible "M" cards for each of eight possible Tape Transport selections.

8. The "M" card that outputs a Logical 1 signifies what number has been designated that physical unit.

9. With the following physical and logical transport designations, what "M" cards (p. 3-5) output a logical 1.

Physical	Logical	"M" Card (P. 3-5)
A	5	M 205
B	7	M 217
C	1	M 221
D	0	M 230
E	6	M 246
F	4	M 254
G	2	M 262
H	3	M 273

10. Using the above designations complete the following. The tape unit to be selected is 4.



11. Re-arrange the following events into proper sequence by filling the options into the blank spaces below.

Assume Connect Code and Controller Switch agree, no Transmission Parity Error has occurred, and the controller is not busy with a previous operation.

a. Connect Signal - R013
b. Clear Unit Select FF's P-4
c. "Strobe Pulse" used for checking Transmission Parity Error
d. Set "Reject" FF K112/113 if controller is busy
e. Enable Status Lines to channel

f. Set "Reply" FF K114/115 if Unit Select FF's have set
g. Transmission Parity Bit - R012
h. Clear "Connect" FF K118/119
i. Set "Controller Connect" FF K110/111
j. Set "Unit Select" FF p. 109
k. Start Connect Timing Chain
l. Set "Reject" FF K112/113 if no "Unit Select" FF has set
m. Set "Connect" FF K118/119
n. Connect Code R000-R011 P1

1. Receive (a), (n) and (g) from the channel.
2. (k), and (c).
3. T1 (m), and (d).
4. T2 (b), (i) and (e).
5. T3 (j).
6. T4 (h), (f) and (l).

II. STATUS INSTSRUCTION

1. A Status Response will always be returning from the connected unit. (T) F

2. What information can the programmer receive from the Magnetic Tape System using the Status Response?

Bit 0 - Ready
Bit 1 - Read/Write Control (and-or) Busy
Bit 2 - Write Enable
Bit 3 - File Mark
Bit 4 - Load Point
Bit 5 - End of Tape
Bit 6 - 556 BPI Density
Bit 7 - 800 BPI Density
Bit 8 - Lost Data
Bit 9 - End of Operation
Bit 10 - Parity Error (Vertical or Longitudinal)

3. What will the following program be used to check.

0000 - 77000000 - Connect Cont. #0 & Tape #0
0001 - 01000000 - If Reject Jump to 0000
0002 - 77200100 - Sense External Status Lines for Bit 6
0003 - 00000000 - Bit Six Present "Halt"
0004 - 77100003 - Function to Select 556 BPI
0005 - 01000004 - If Reject Recycle to 0004
0006 - 00000000 - Stop after selecting 556 BPI

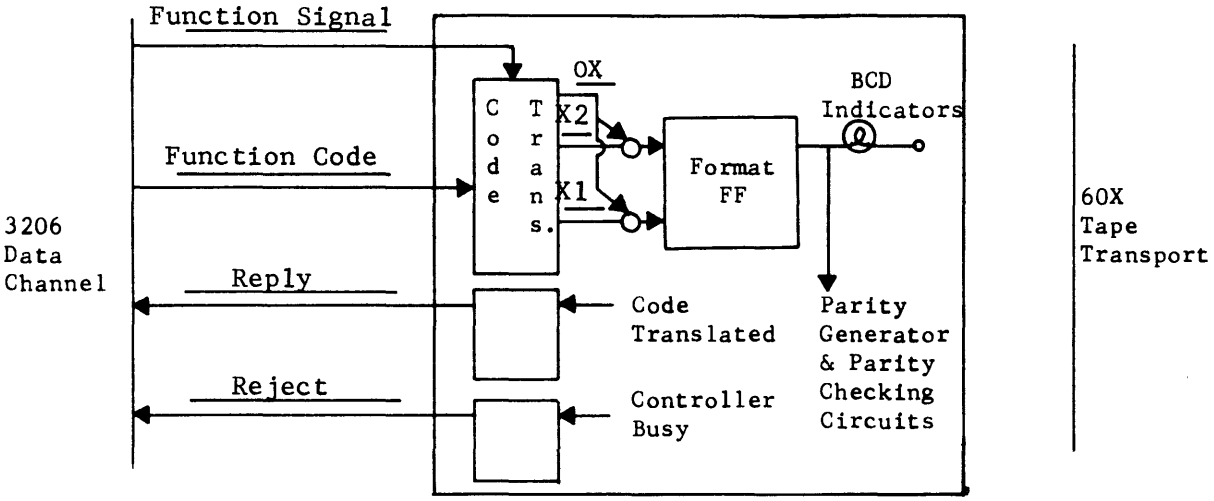
4. May more than one response be present on the Status Lines when Status is checked? If no, explain why. If Yes, give a realistic example.

Yes - More than one status may be present.

Bit 0 - Ready
Bit 4 - Load Point
Bit 6 - 556 BPI Density

III. FORMAT SELECTION (BINARY-BCD)

1. Fill in the following block diagram signal flow.



2. The format selection determines whether an odd or even number of bits shall be exchanged between controller and Tape Transport, and controller and channel. T (F)

3. What conditions must exist in the controller before the Function Code can be translated?

   a. Controller Connected
   b. No Reply Signal
   c. No Reject Signal
   d. Xmsn Parity Error (Not)
   e. Read/Write Control Not Busy

4. What would cause an external reject when selecting the format?

   Read/Write Control Busy

5. The format FF has two main circuits to control. What are they?

   a. Parity Generator
   b. Parity Checker

6. The programmer's visual indication, when the Binary format is selected, is an illuminated lamp on the controller. T (F)

7. The format selection was made prior to a Write Operation. Which would cause a parity bit?

a.	An even number of data bits with a BCD Selection	T	(F)
b.	An even number of data bits with a Binary Selection	(T)	F
c.	An odd number of data bits with a BCD Selection	(T)	F
d.	An odd number of data bits with a Binary Selection	T	(F)

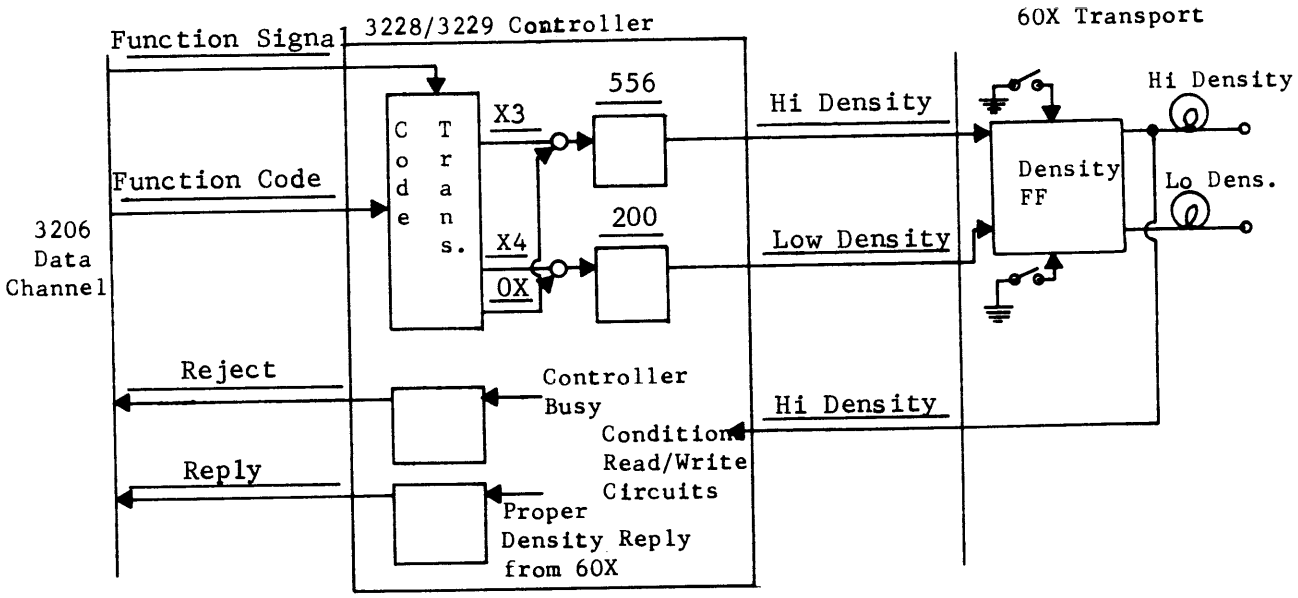
8. The format selection was made prior to a Read Operation. Which would cause a parity error?

a.	A BCD format, a parity bit, and an odd number of data bits	T	(F)
b.	A BCD format, a parity bit, and an even number of data bits	(T)	F
c.	A BCD format, no parity bit, and an odd number of data bits	(T)	F
d.	A BCD format, no parity bit, and an even number of data bits	T	(F)
e.	A Binary format, a parity bit, and an odd number of data bits	(T)	F
f.	A Binary format, a parity bit, and an even number of data bits	T	(F)
g.	A Binary format, no parity bit, and an odd number of data bits	T	(F)
h.	A Binary format, no parity bit, and an even number of data bits	(T)	F

9. The Format FF clears when the format selection is completed. T (F)

IV. DENSITY SELECTION

1. Fill in the following block diagram signal flow.



2. What type of reject will occur if a Transmission Parity Error occurs on a Density Instruction?

   Internal Reject

3. What other condition will cause this type of reject during a Density Instruction?

   Controller not connected

4. Why can't the Density FF's set if the Controller is busy?

   S040 (Translator 0X) forced to output a Logic Zero

5. When changing from low to hi density, what visual indication would show the change had taken place?

   Transport Indicator changes

6. Can density be changed other than by a Function Instruction? If yes, indicate the method.

   Yes, manual selection from the transport.

7. How does the returning 60X Density Signal affect the Write Circuits?

   Controls rate of which timing chain is started.

8. How does it affect the "Read Circuits"?

   Selects Delay used to clear Reply timing chain Lockout F/F.
   Selects "End of Record" Delays.

9. Complete the following chart.

Density	Transfer Rate	Frame Space (u sec)	Frame Space (inches)
200 BPI	30,000	33.3 usec	.005
556 BPI	83,400	12 usec	.0018
800 BPI	120,000	8.3 usec	.00125

10. What prevents the "Reply" Signal from returning to the channel before the proper density signal arrives from the 60X?

    D102 holds D110 to a zero out until Density Reply returns.

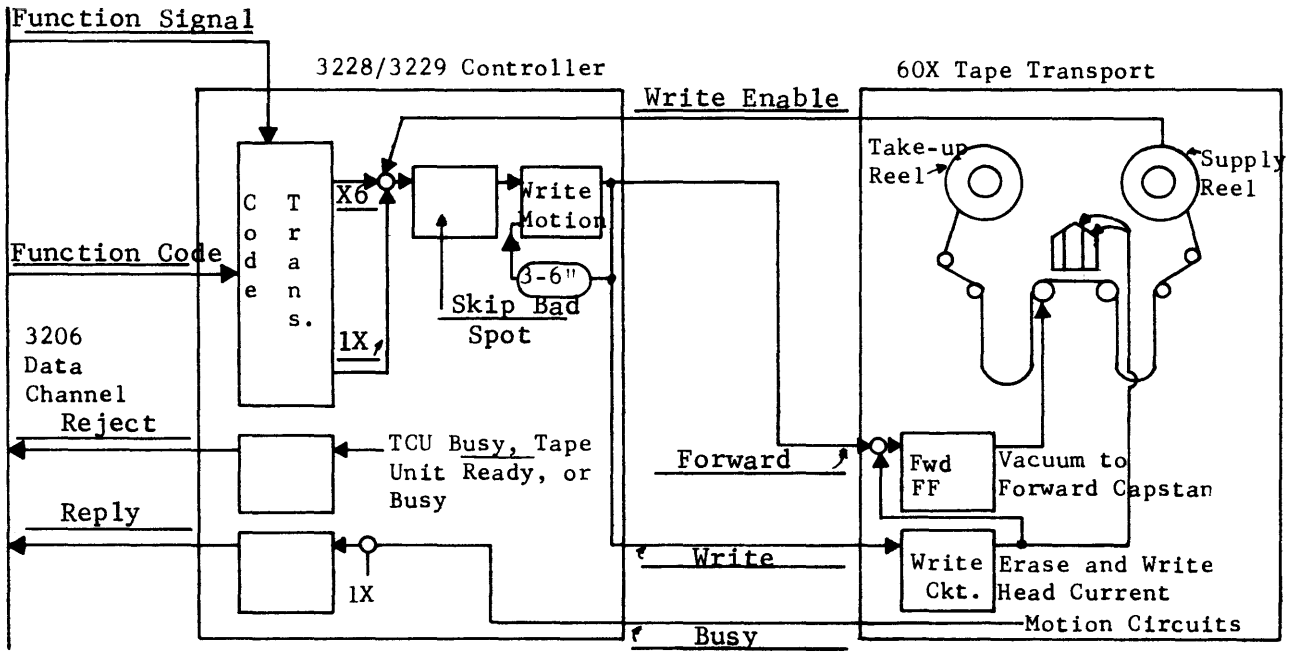
11. When the "Reply" Signal is sent to the channel, what happens to the Density FF's in the controller? In the transport?

    They are cleared in the controller.

    Transport FF's are not affected.

V. SKIP BAD SPOT

1. Fill in the following block diagram signal flow.



2. Would a "Write" Signal be sent to the selected tape transport if it is not ready? If no, explain what prevents it? If yes, how does the signal affect the transport? Give a detailed explanation.

No, because the "Skip Bad Spot" FF cannot set if the transport is not ready.

3. What conditions would prevent the "Skip Bad Spot" FF from setting when the code has been translated?

   a. No "File Protect Ring" on selected transport supply reel.
   b. Transport Ready
   c. Transport Busy
   d. Read/Write Control active

4. When an option is false, explain why it is false:

   During a "Skip Bad Spot" Instruction,

   a. An "External Reject" Signal is sent to the channel if the File Protect Ring is not on the Supply Reel — (T) F
   b. "R to O" FF Z010/011 Pg. 8 will set but no data transfers to the Write Register — T (F)
   c. The "Write Control" FF prevents the setting of the "Write" Register — (T) F
   d. No current flow is allowed in the tape transport's Erase and Write heads — T (F)

5. List 7 operations that would cause a loss of the "Write Now Possible" Signal (I135 pg. 115)

   a. Read Forward Sel. & Busy
   b. Read Reverse Sel. & Busy
   c. Rewind
   d. Backspace
   e. Search for File Mark Forward
   f. Search for File Mark Backward
   g. Connecting to a Busy Transport

6. A malfunction disabling the Write Timing Chain would prevent this operation — T (F)

7. Arrange the following events into proper sequence. If some are not needed for this operation, draw a line through them on the list and do not include these in the sequence.

12 a. Clear Write Terminate I FF
11 b. Set Write Terminate II FF
5 c. Send Write Signal to 60X
14 d. Clear Skip Bad Spot J016/017

13 f. Clear Write Motion
15 g. Drop Forward Signal to 60X

10 i. Set Write Terminate I

7 k. Send Reply Signal to The Data Channel
17 l. Clear Write Terminate II FF

3 n. Set Skip Bad Spot FF's
6 o. Send Forward Signal to 60X

18 r. Drop Write Signal to 60X
4 s. Set Write Motion
9 t. Set Write Control
2 u. Arrival of Function Signal
8 v. Clear "Skip Bad Spot" FF J012/013
16 w. Clear Write Control
1 x. Arrival of Function Code

8. Before the Write Terminate I FF can set, the Check Character must be written. T (F)

9. How does the controller know when the Tape Transport has erased tape the proper distance.

   A 6 inch Delay Times Out

10. What causes the "End of Operation" Signal to be missing from the Status Lines during this operation?

    D169 End of Operation is a Logic Zero

    D125 - Busy = Logic 1
    E032 - Start New Record Set FF j044/045

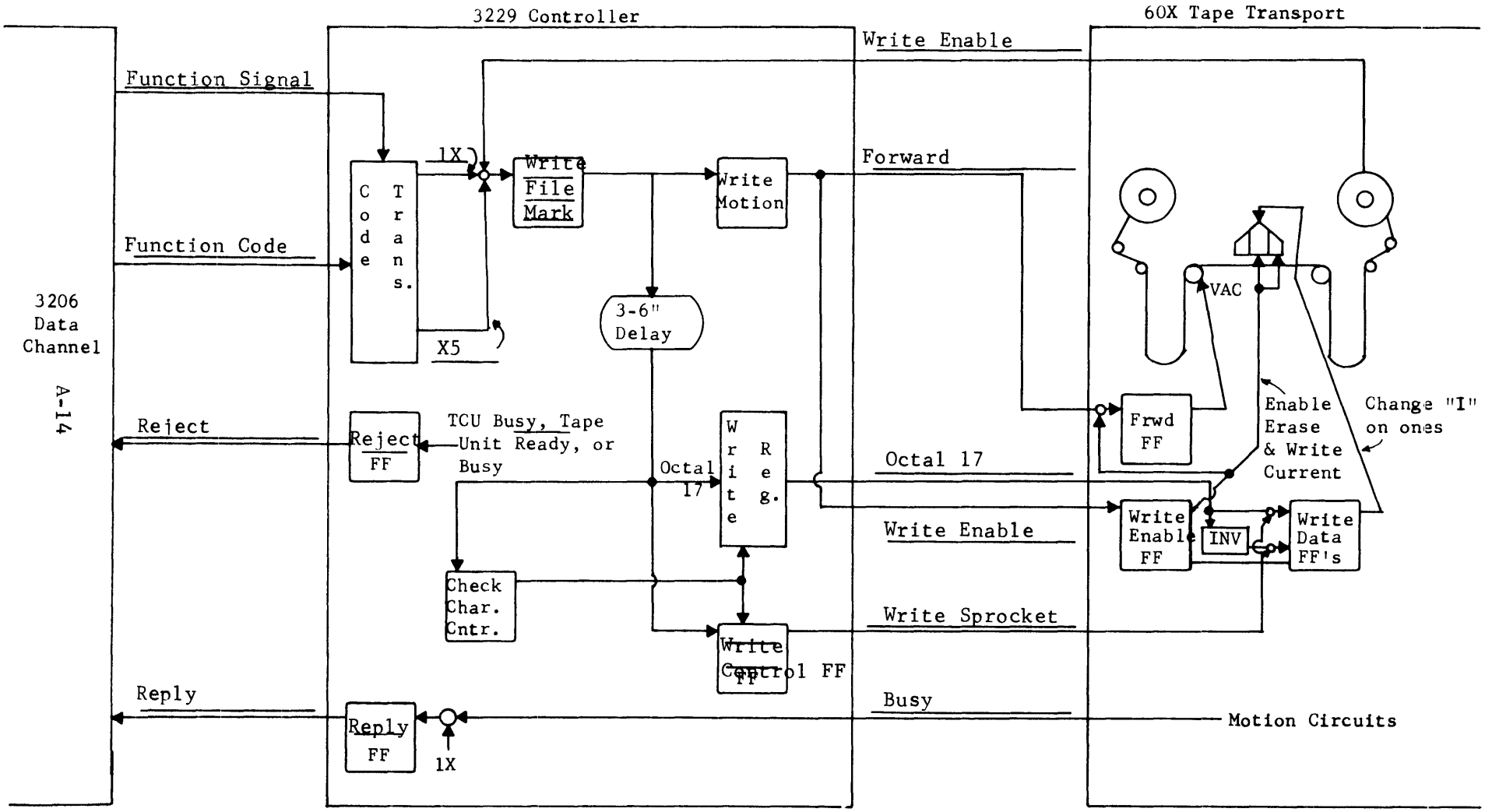
11. The normal "End of Record" Signal from the Tape Transport cannot be generated unless one frame has been read. How do we generate the "End of Record" Signal which clears FF J044/045 Pg. 111 during a Skip Bad Spot Instruction?

    A false "End of Record" Signal is generated by

    J017 - Skip Bad Spot FF
    Z033 - Write Terminate II FF

VI. WRITE FILE MARK

1. Fill in the following block diagram signal flow



2. How can the same three Write oscillators operate 75 as well as 150 inch per second Tape Transports?

   By using a counter the timing chain is started at a rate half as fast.

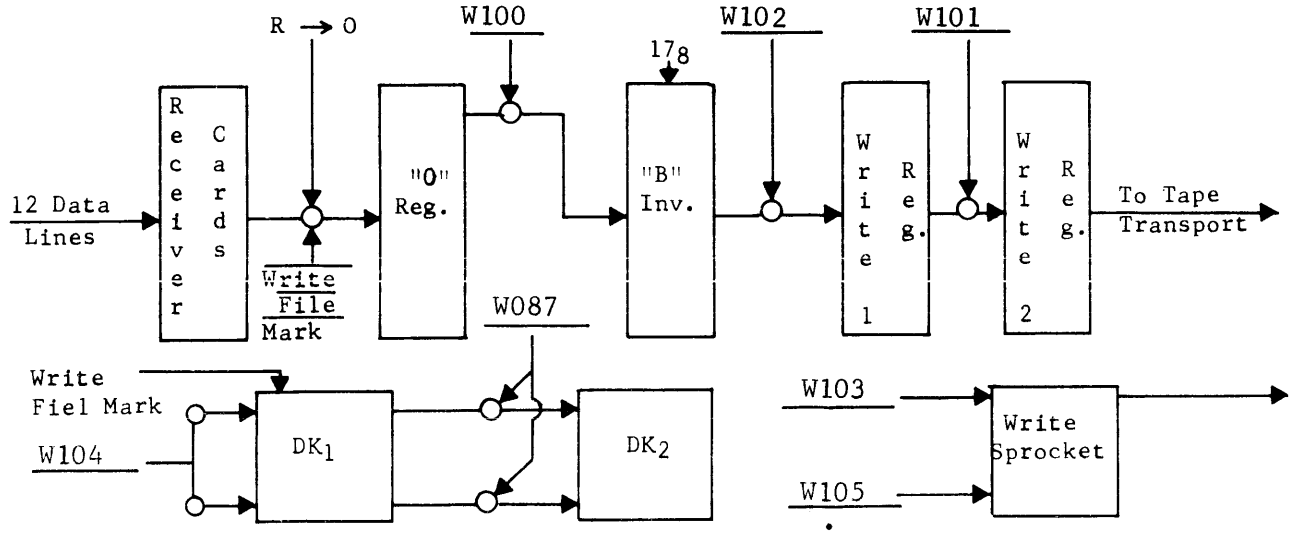
3. How long will the Timing Chain remain active when it begins a pass?

   7 usec.

4. Fill in the proper Write Time beside the following terms.

Term	Time
a. $0 \longrightarrow B$ (W100)	T1
b. $W_1 \longrightarrow W_2$ (W101)	T1
c. $DK_1 \longrightarrow DK_2$ (W087)	T1
d. $B \longrightarrow W$ (W102)	T2
e. Start Sprocket (W103-A Zero)	T3
f. Advance DK (W104)	T5
g. Clear Sprocket (W105)	T7

5. Fill the above enables into this simplified block diagram.



6. Would this operation start tape movement if the File Protect Ring was missing from the Transport's Supply Reel? If no, explain what prevents it? If yes, when it tape stopped?

   No - Write File Mark FF cannot set.

7. Setting the Write File Mark FF, immediately:

   a. Places the File Mark in the Write Register
   (b) Sets the Disassembly Counter
   c. Clears the "Write Data Lockout" FF
   d. Sets R to 0 FF
   (e) Changes format to BCD if it was Binary
   (f) Prevents an R to 0 Transfer

8. What prevents the shorter delays from expiring first, to set the Write Control FF after only a 3/4 inch delay? p. 113

   F011 is outputting a Logic Zero when writing a File Mark. F008 outputs a Logic One disabling the 3.5 msec delay.

9. What two events occur when the Write Control FF sets?

   a. Remove clear from W_1
   b. Enable setting of R$\longrightarrow$0 FF

10. A malfunction disabling the Write Timing Chain would prevent this operation (T) F

11. Rearrange the following events into the proper sequence.

Preparing To Write A File Mark

3	a.	Set Disassembly Counter I
10	b.	Clear Write File Mark FF J010/011
13	c.	Set R to 0 FF
4	d.	Place an "Octal 17" in "B" Inverters
15	e.	Clear R to 0 FF
2	f.	Set the "Write File Mark" FF
14	g.	Set "Write Resync"
1	h.	Receive Function Code & Signal
7	i.	Send Forward Signal to 60X
5	j.	Format changed to BCD
8	k.	Send Write Signal to 60X
6	l.	Set Write Motion
9	m.	Send "Reply" Signal to Channel
12	n.	Remove Clear from W_1 Register
11	o.	Set Write Control

After rearranging the above events, review by again following them through the logic diagrams. At this time tape should be moving with current flowing through the Erase and Write Head. A Reply has returned to the Channel.

12. Rearrange these events into the proper sequence.

Writing The File Mark

12 a. Clear Disassembly Counter I
4 b. Set Disassembly Counter II
3 c. "0_2 to B" Transfer
1 d. Set Write Gate
~~e. "DK_1 to DK_2" Transfer~~
2 f. Enable Transfer Terms (W084-W089)
7 g. Set Write Sprocket FF
8 h. File Mark written on tape
14 i. Clear Write Resync
9 j. Clear Write File Mark FF J014/015
15 k. Clear Write Gate
11 l. Advance DK Pulse
6 m. "B to W_1" Transfer
5 n. "W_1 to W_2" Transfer
10 o. Set Check Character Counter Enable FF Z000/001
16 p. Disable Transfer Terms (W084-W089)
13 q. Clear "Write Sprocket" FF

Again review the properly rearranged sequence in your logic diagrams. The File Mark has been written and the Check Character Counter is enabled.

13. Writing The Check Character

7 a. Z002/003 Clear, Z004/005 Clear, & Z006/007 Set
8 b. Set Write Terminate I
1 c. Z002/003 Set, Z004/005 Clear, & Z006/007 Clear
4 d. Z002/003 Clear, Z004/005 Set, & Z006/007 Set
2 e. Z002/003 Set, Z004/005 Set, & Z006/007 Clear
3 f. Z002/003 Clear, Z004/005 Set, & Z006/007 Clear
5 g. Z002/003 Set, Z004/005 Set, & Z006/007 Set
6 h. Z002/003 Set, Z004/005 Clear, & Z006/007 Set
9 i. Clear W_1 Register
12 j. Clear Check Character Counter Enable FF Z000/001
10 k. Write Check Character on tape
11 l. Set Write Sprocket FF
14 m. Z002/003 Clear, Z004/005 Clear, & Z006/007 Clear
13 n. Clear Write Sprocket FF

Review logic diagrams. The Check Character has been written in the 4th frame position on tape. The Check Character will be an Octal 17.

14. Terminating The Write File Mark Operation

4 a. Drop Forward Signal to 60X
2 b. Clear Write Terminate I
7 c. Clear Write Terminate II
8 d. Drop Write Signal to 60X
5 e. Clear Write Control
1 f. Set Write Terminate II
9 g. Place a Steady Clear on W_1 Register
6 h. Disable the setting of the "R to 0" FF
3 i. Clear Write Motion

Review the rearranged sequences in the logic diagrams. The Forward & Write Signals drop and Motion is stopped in the Transport. Write Head Current remains.

15. Why can't the Disassembly Counter advance, with each pass through the Timing Chain, when incrementing the Check Character Counter?

Write Gate FF Z014/Z015 is clear which blocks the advance pulse.

16. How much time is needed from the last data frame until the Check Character is written? (Check Character Gap in u sec) (200 BPI)

133.2 usec

17. What is the duration of the Write Sprocket using a 150 inch per second transport? A 75 inch transport?

    4 usec - 6 usec

18. What is the purpose of the Write Resync FF?

    a. Prevents another data transfer before all present data is written on tape.

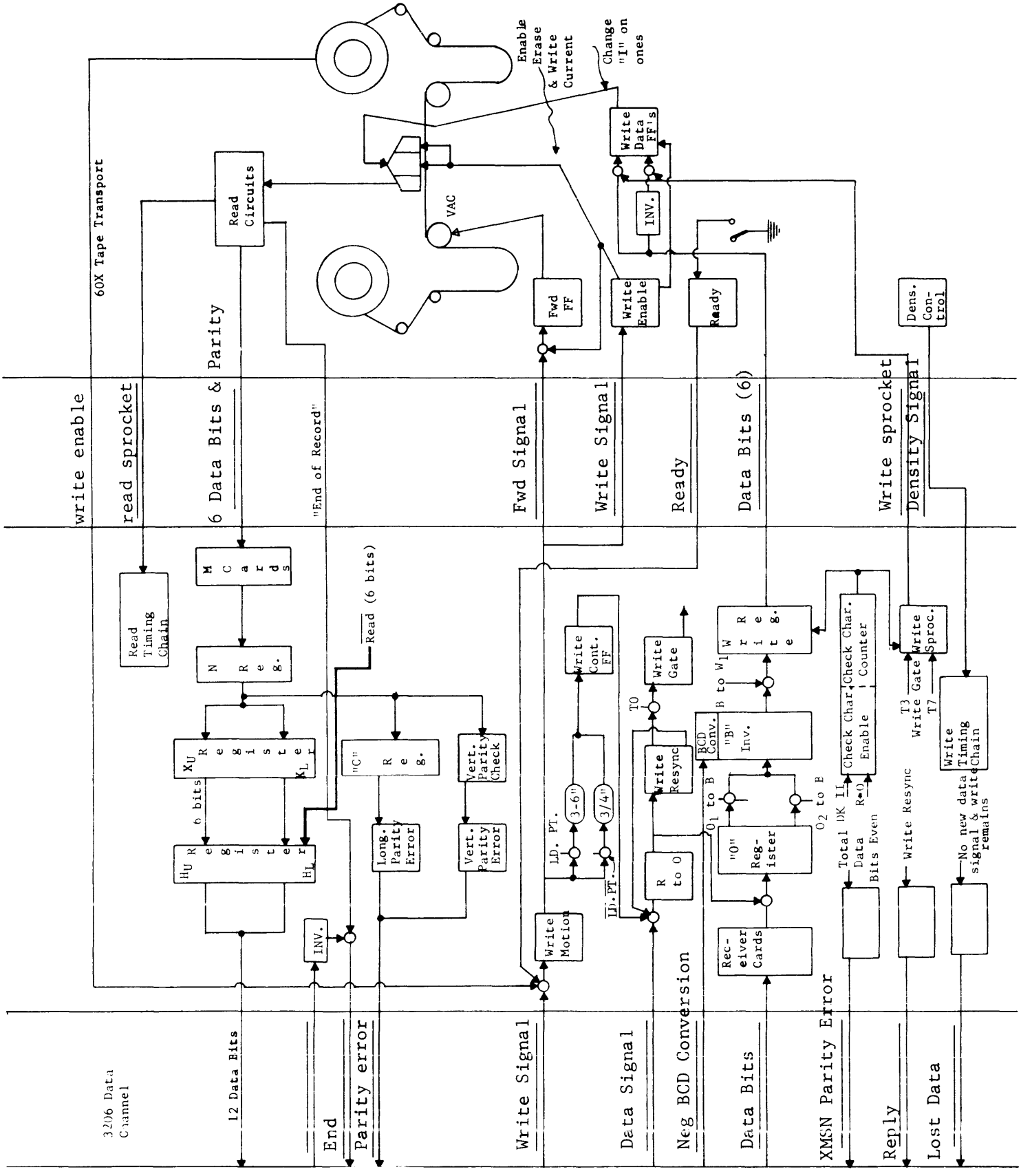
    b. Enables setting of Write Gate FF at Time 0.

19. What is the purpose of the Delay Y041 (Y058) between Write Terminate I and II?

    Enables the reading of the check character before tape motion is stopped.

VII. WRITE OPERATION (12 AND 6 BIT MODE)

I. COMPLETE THE FOLLOWING BLOCK DIAGRAM.



2. Which Flip Flop is the first to set during a 12 bit Write Operation?

   Write Motion

3. Which of the below conditions would prevent the setting of the Flip Flop you have listed?

   (a) Lost Data FF set
   b. Write Resync FF set
   (c) Write Control FF set
   (d) The selected tape unit has no File Protect Ring.
   e. All tape units are prepared to write; however, the wrong unit is selected by accident.
   f. The previous Write Operation is completed but tape is still moving.
   (g) If the selected tape is rewinding

4. How is a six inch Delay achieved when writing from Load Point?

   10 msec to drop load point signal
   30 msec from Y023
   40 msec = 6 inches
   3.5 msec delay disabled

5. During a Write Operation, The R → 0 FF accomplishes 5 tasks. What are they?

   a. Gate data from receiver cards to 0 Register.
   b. Remove clear from 0 Register.
   c. Clear Check Character Counter Enable FF.
   d. Set Z068/069 Lost Data Circuit.
   e. Set Write Resync.

6. When will the R to 0 FF clear?

   When the data signal drops.

7. When does the Write Timing Chain begin to sequence data through the controller?

   When the Write Gate FF sets.

8. When the Write Gate FF sets, where are the 12 bits of data located?

   0 Register.

9. When does the "Reply" Signal return to the Channel?

   When the Write Resync FF sets.

10. Describe

    a. How the "Lost Data" FF sets if the first data frame is absent.

       Through Delay Y044.

    b. How does the tape motion stop?

       Y044 also clears Write Motion FF dropping forward and stopping tape motion.

11. What is the purpose of the "0" Register?

    To store the 12 data bits during Disassembly.

12. What is the purpose of the "B" Cards?

    Convert Internal BCD to External BCD

13. What is the rule for converting Internal to External BCD? Which code is the exception?

    If Bit 4 is present complement Bit 5

14. What is the purpose of the Write Register?

To change data bits to NRZI

15. Why is a Write Sprocket Signal used with the Magnetic Tape System?

To provide a means of alignment on the transport.

16. What factors determine which portion of the "0" Register is to be written on the tape?

a. Disassembly Counter
b. Suppress A/D

17. List the conditions that will generate a Parity Bit?

BCD - Odd data bits
Binary - Even data bits

18. a. What is the condition of the Disassembly Counter when the first six bit word is sent to the Transport?

Clear

b. Which six bit byte is sent to the Transport first?

Upper six

19. Why can't the "Check Character Gap Counter Enable" FF set after the first six bit transfer?

The Disassembly Counter II is still cleared.

20. Which of the Write Circuit FF's will set and clear with each written frame?

a. Write Sprocket
b. Write Gate

21. **After the second frame is written on tape, how is the "0" Register cleared?**

    By clearing write resync FF.

22. a. **How is the "Lost Data" FF set when a 12 bit byte is absent (not to include the first frame)?**

    W099 outputs a one and T5 lost data is set.

    b. **How is the tape motion stopped?**

    Normal termination.

23. **What keeps the Check Character Gap Counter inactive while data is being written?**

    R 0 transfers keep the check char. enable FF clear which holds a clear on the other FF's in the counter.

24. **Why does the counter begin to increment after the last frame?**

    No R 0 transfer the enable FF stays set.

25. **When the correct gap has been formed, how is the Check Character written?**

    By clearing the write register I.

26. **When and how is the termination started?**

    When the check character is formed by W076 setting write terminate I FF.

27. The data which was written will be read and parity will be checked. How is the Read Timing Chain Enabled during a Write Operation?

By the read sprocket generated by the transport.
And by E_{021} (Read/Write active) being a "1".

28. How is the Read Timing Chain able to remain synchronized with the data being read?

The read sprocket accompanying the data starts the timing chain.

29. Fill in the following blanks with the proper Read Time.

a. Clear X — T1 counter even

b. C_1 to C_2 — T1

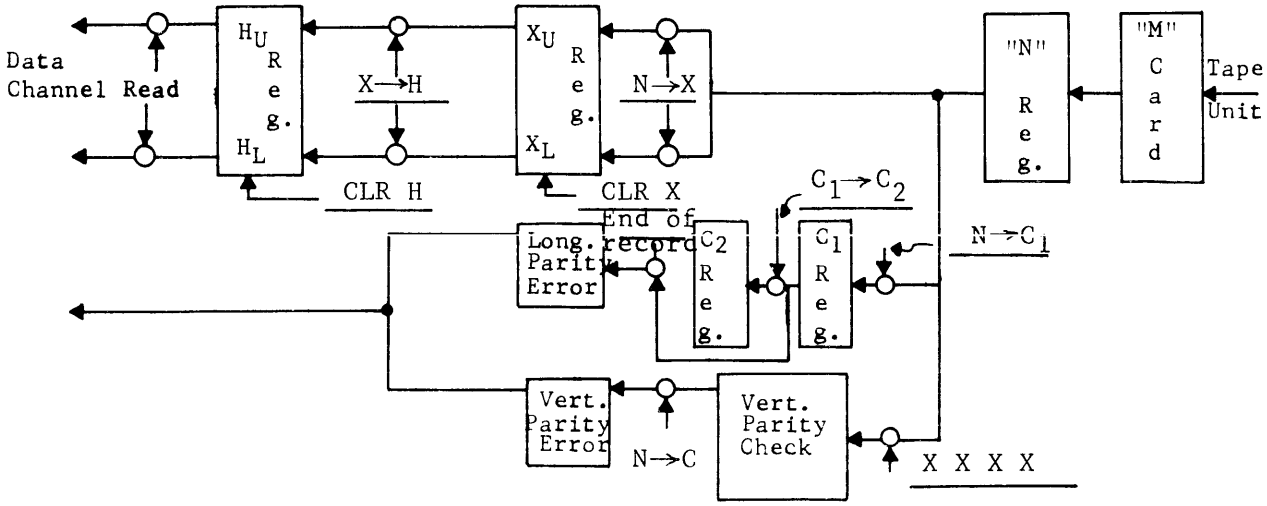
c. N to C_1 — T3

d. N to X — T3

e. X to H — T5

f. Clear H — Data Signal Drops

30. Place the above terms in the proper blanks below.



31. How long does the Reply Timing Chain Lockout FF remain set?

    a. 200 BPI: 13.6 u sec

    b. 556 BPI: 5.1 u sec

    c. 800 BPI: 3.1 u sec

32. List the conditions that will give a Vertical Parity Error?

    BCD - Odd Data Bits - No Parity
    Even Data Bits - Parity
    Binary - Odd Data Bits - Parity
    Even Data Bits - No Parity

33. What is the purpose of the "C" Register?

    To check longitudinal parity.

34. Why is the "End of Record"Pulse used to time the checking of the "C" Register?

    The check character will have been read.

35. Tape motion will automatically be stopped by the controller if a Parity Error occurs. T (F)

36. How is the tape motion stopped if a Parity Error has occurred? If no Parity Error is present?

    Normal termination.

37. When motion stops the Read Head has reached the Record Gap?

    (a) True

    b. False, where will the Read Head be positioned?

38. What additional signal is needed to write only six bits of each computer output?

    Suppress assembly/disassembly.

39. Explain the affect of this signal on each of these items.

a. Setting the Write Control FF

No affect.

b. Advancing the Disassembly Counter

Disables the advance.

c. Generating the Write Sprocket Signal

No affect.

d. Setting the "Lost Data" FF

No affect.

e. Setting the "Check Character Gap Enable" FF

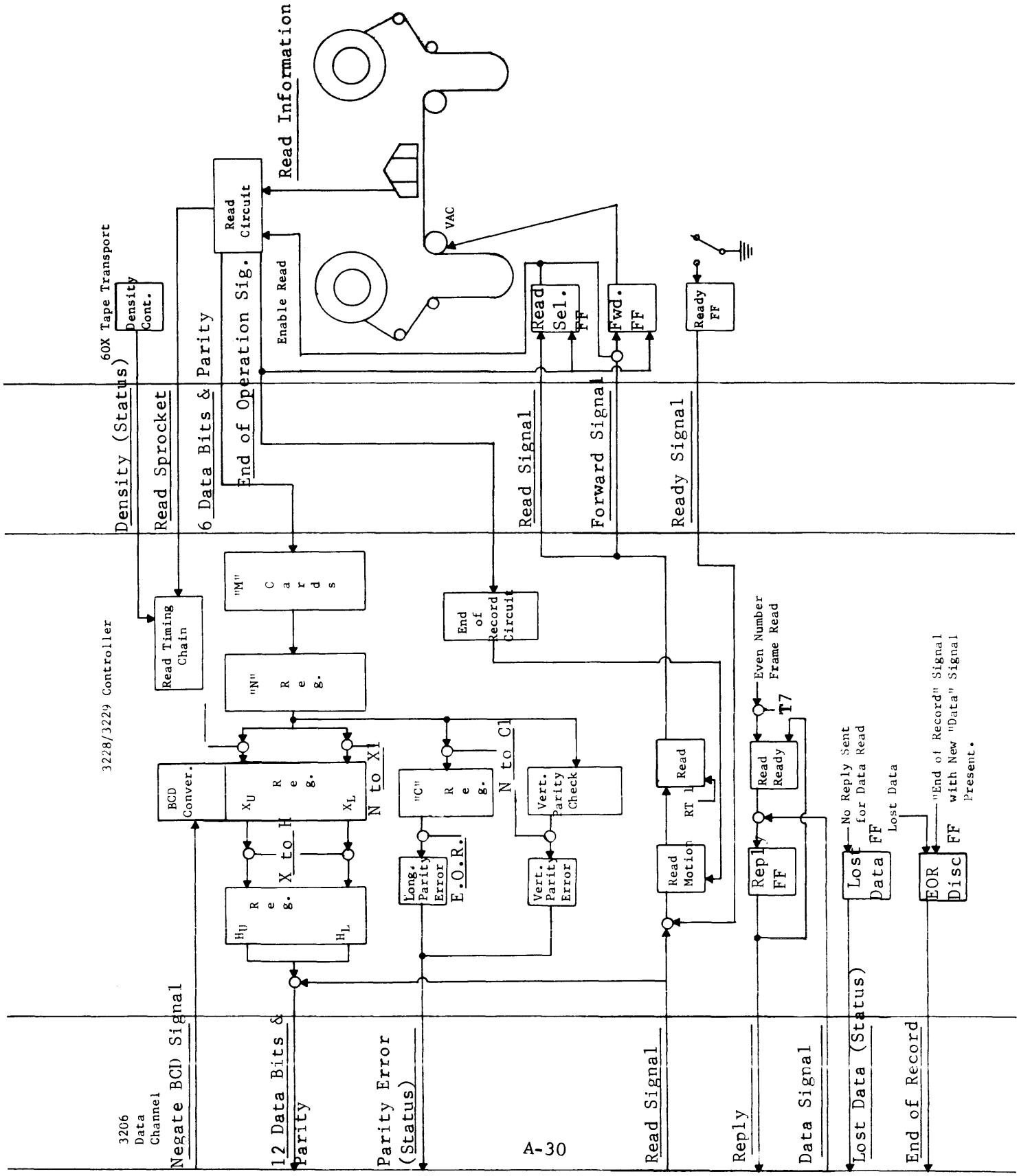
Sets after recording first six bits.

f. Gating data from "0" to B.

Allows only 0_1 B.

VIII. READ OPERATION (12 AND 6 BIT MODE)

I. COMPLETE THE FOLLOWING BLOCK DIAGRAM.



The following questions deal with a 12 bit Read Operation. "Read Backward" is not selected.

2. What is the purpose of the "Read Motion" FF?

   To send the "Read" and "Forward" signals to the transport.

3. Which of these conditions will prevent the "Read Motion" FF from setting?

   (a) Selected Tape Transport not ready

   (b) Lost Data Condition

   (c) Read Control Set

   d No data signal accompanying the Read

   (e) Selected tape unit is searching for a File Mark

   f. A Read Signal present before the Busy Signal drops on the previously initiated Read Operation

   (g) Read Signal present before Busy Signal drops on a previously selected Write Operation.

   h. Read Data Lockout FF set

4. A "Start New Record" Signal is generated for 10 u sec during a Read Operation.

5. What functions are accomplished by the "Start New Record" Signal?

   a. Clear Longitudinal Parity Error FF
   b. Clear C_1 Register
   c. Clear Vertical Parity Error FF
   d. Clear Assembly Counter Enable FF
   e. Clear Assembly Counter FF
   f. Clear End of Record II FF
   g. Clear File Mark FF
   h. Set End of Operation FF

6. What conditions determine which part of the "X: Register receives data?

   a. Backward Selection
   b. Assembly Counter I FF
   c. Suppress A/D

7. To which part of the "X" Register are odd frames placed?

   Upper

8. What is the condition of the Assembly Counter at this time?

   Assembly counter clear.

9. What starts the Read Timing Chain?

   Read Sprocket.

10. Using only the following Enables, arrange them into the proper sequence for assemblying two frames. Enables may be used more than once.

    a. Clear the "X" Register

    b. C_1 to C_2

    c. N to C_1

    d. N to X_1

    e. N to X_2

    f. X_1 to H

    g. X_2 to H

    h. Clear the "H" Register

    <u>Odd Frame</u>

    1. a
    2. b
    3. c
    4. e

    <u>Even Frame</u>

    1. b
    2. c
    3. d
    4. f
    5. g
    6. h

11. What is the rule for converting External to Interal BCD?

Bit 4 present complement bit 5.

12. Explain how the logic converts the External BCD 12 to an Internal BCD Zero.

When an octal 12 is detected in BCD the and gates used to set bits 1 and 3 are broken.

13. What happens when the "Read Ready" FF sets?

A reply is returned to the channel.

14. What conditions will clear the "H" Register?

a. Dropping the data signal.
b. Setting end of record FF.
c. Clearing read control FF.
d. Setting read data lockout FF.

15. What circuit is controlled by Begin Record I and II FF's?

End of record circuit.

16. What is the purpose of Begin Record I and II FF's?

Begin record I FF prevents end of record delays from timing out in the record gap prior to the data.

Begin record II FF assures we must have two frames read before we set the end of record I FF.

17. How is the "Hold" FF used to detect a "Lost Data" condition?

If it remains set the data in "H" register was not cleared. Before the next 12 bit word is placed in H the Hold FF enables the setting of lost data FF.

18. What is the purpose of the "End of Record" Circuits?

    1. Clear read motion.
    2. Prevent vertical parity check.

19. What conditions are needed to time out the "End of Record" delays?

    2 1/3 frame spaces without data.

20. When will the delays time out before the data within a record is read.

    Read backward.

21. When will the Read Motion FF clear?

    When the end of record signal is sent to the controller.

22. What would happen if the computer requested another input after the "End of Record" Signal is received from the Tape Transport?

    An "end of record disconnect" would occur.

23. How will the "Suppress Assembly/Disassembly" Signal affect a Read Operation?

    6 bits can be transmitted to the channel at a time.

24. Explain how the Supress A/D Signal affects each of these items.

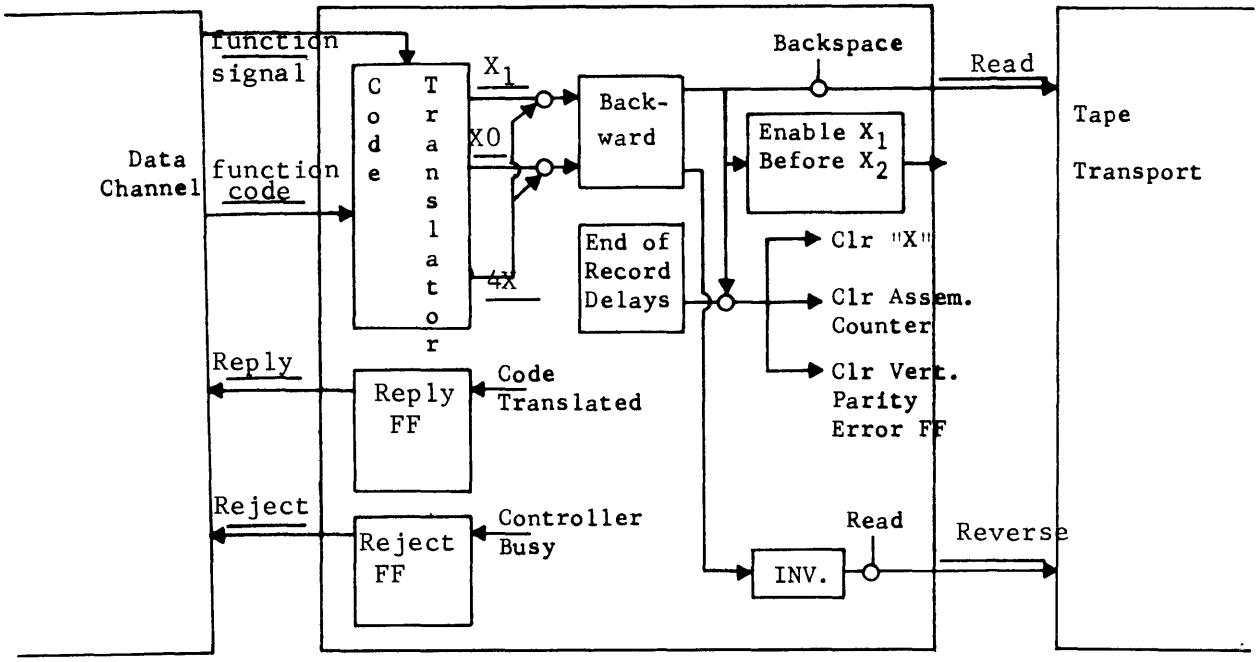
    a. Read Motion FF
       No affect.
    b. End of Record I FF
       No affect.
    c. Assembly Counter
       Disable the advance pulses.
    d. Read Ready
       Allowed to set each frame read.

e. N to X Transfer
   N only gated to X_1
f. X to H Transfer

   Enabled T5 of each frame read.

IX. READ BACKWARD (SELECTION OR RELEASE)

1. Complete the following Block Diagram.



2. Can the "Backward" FF be selected if the Transport is busy? If the controller is busy? Why?

No. No. R/W control Active (D114) blocks the function code translation.

3. If the "Backward" FF is set which way will tape move when a "Read" Signal arrives? If a "Backspace" is selected?

Reverse, Forward.

4. When performing a Read Operation with the "Backward" FF set, the first frame Read will:

   a. Contain data
   b. Be returned to the computer
   (c) Be stored in a register in the controller
   d. Always contain an even number of logic one bits if in BCD Mode
   (e) Be followed by the Check Character Gap
   (f) Set "Begin Record I" FF
   g. Set "Begin Record II" FF
   (h) Advance the "Assembly" Counter
   i. Set the Longitudinal Parity Error FF
   j. Set the Vertical Parity Error FF
   k. Be placed in X upper
   (l) Be placed in X lower

5. What will happen to these circuits in the Check Character Gap? Explain why each must occur.

   a. The "X" Register

      Cleared to prevent reading the check character as data.

   b. The Assembly Counter

      Reset to even to enable correct assembling of new data.

   c. The Vertical Parity Error FF

      Cleared to prevent a possible parity error from the check counter.

6. Why shouldn't the "C" Register be cleared also?

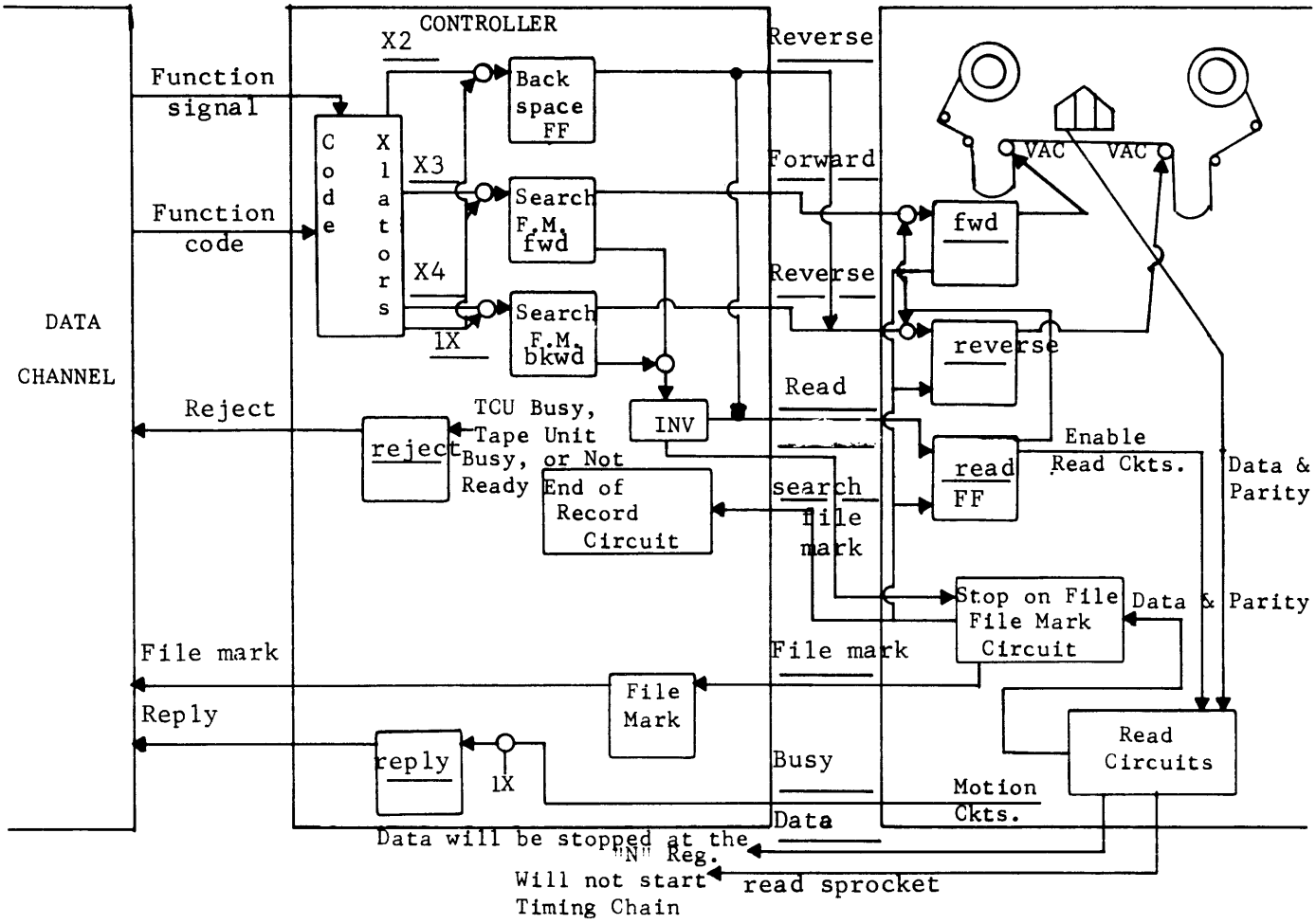
   Needed for longitudinal parity check.

7. Where will the Read Head be situated when tape motion stops?

   In the record gap preceding the record that was just read in reverse.

X. SEARCH FOR FILE MARK FORWARD, REVERSE, AND BACKSPACE

1. Complete the following Block Diagram.



2. What is the purpose of a Search For File Mark instruction?

Prevents stopping of tape motion in each record gap while searching for a reference point (17_8)

3. What conditions are needed to set the Search For File Mark FF's?

a. R/W control not active.
b. Tape unit ready and not busy.

4. When is the "Reply" sent to the Channel?

   As soon as tape motion commences, causing a "busy" signal to be generated.

5. What happens to the data sent to the controller? What prevents the data from entering the computer?

   E021 (R/W Active) remains a zero and blocks the read timing chain. The data is lost in the N cards.

6. Why can't a Parity Error occur when searching for a file mark?

   The output of the parity checker is never strobed.

7. Tape continues to move even when the "Search For File Mark" FF's clear. How does tape motion stop?

   Stop on File Mark Circuit in the transport stops tape motion.

8. When the "File Mark" FF, p. 3-29, has set, what conditions are needed to clear it?

   Channel Busy and Begin New Record or Connect Signal or New Function or Clear or Release.

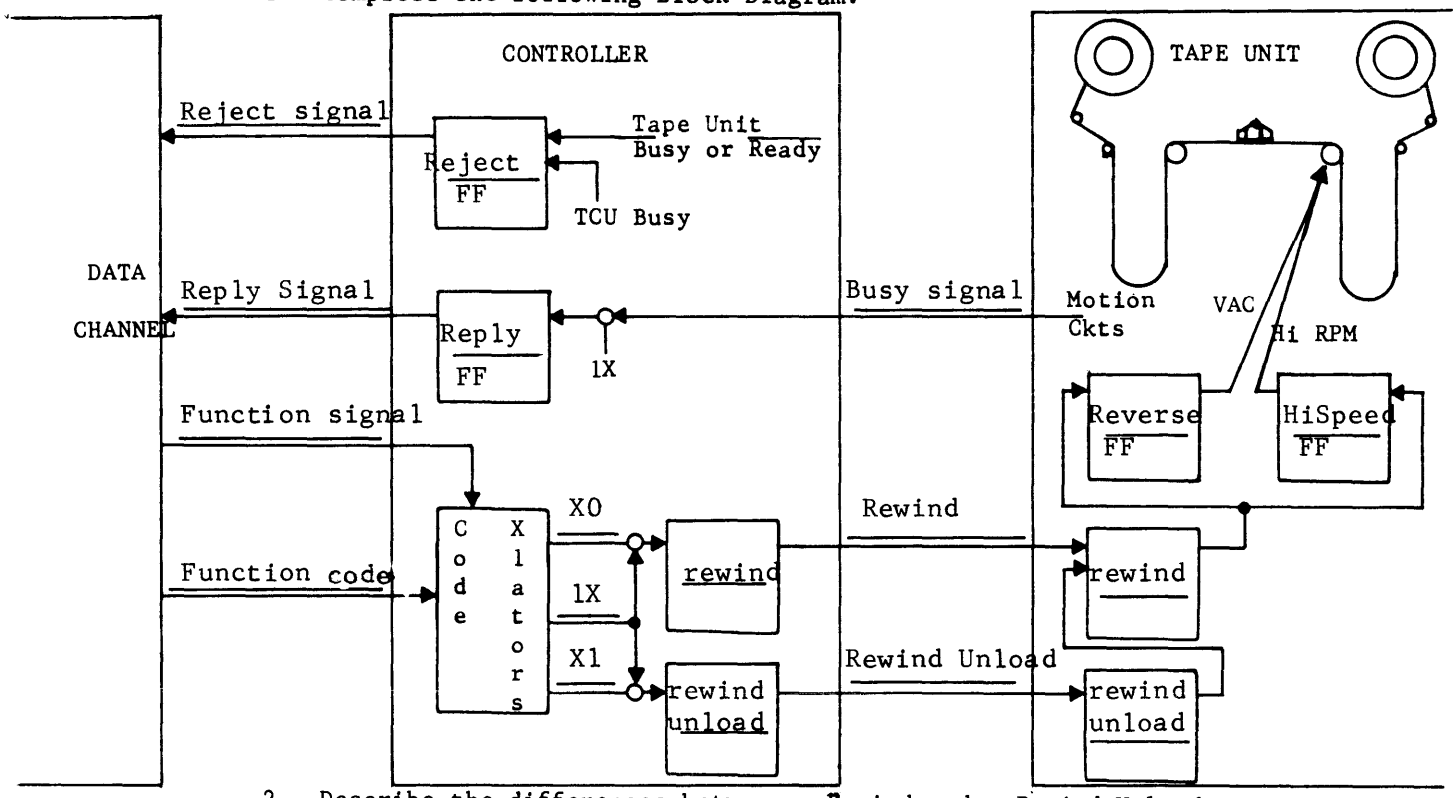
9. What is the purpose of a "Backspace" Operation?

   To position a previously written or read record over the read/write heads to enable that record to be rewritten or reread.

10. How is tape motion stopped when performing a "Backspace"?
    By the transport when a record gap is detected.

XI. REWIND AND REWIND UNLOAD OPERATIONS

1. Complete the following Block Diagram.



2. Describe the differences between a Rewind and a Rewind Unload Operation.

Rewind - Moves tape high speed reverse to load point where tape motion ceases.

Rewind Unload - moves tape high speed reverse to load point, then low speed until all tape is off of take-up reel.

3. A "Rewind" instruction has been selected but tape is already at "Load Point." Is a "Reply" sent back to the Channel? If yes, explain how. If no, how is the computer able to continue with the next instruction?

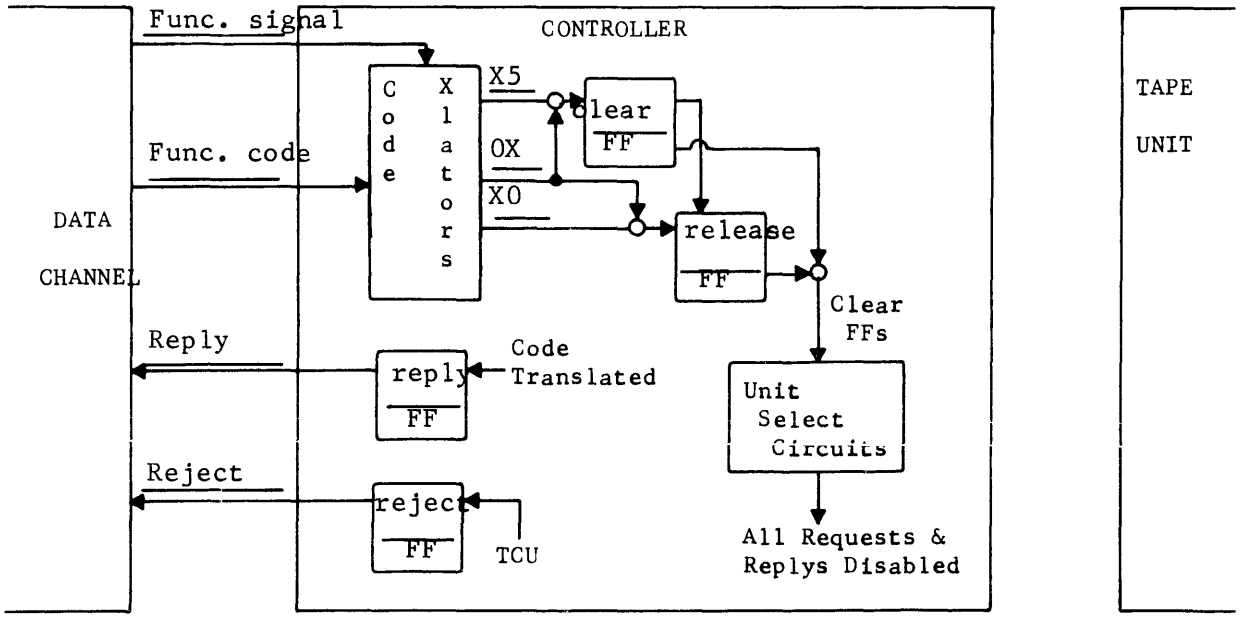
Yes, Lower "and" gate to D115 is made.

4. How is a "Reply" Signal sent to the computer if a "Rewind Unload" Operation is selected?

D109 outputs a "zero" when the function is selected.
D110 outputs a "one" when tape motion commences.

XII. RELEASE AND CLEAR INSTRUCTIONS

1. Complete the following Block Diagram.



2. What is the purpose of the "Release" instruction?

   Clears the unit select FF's.

3. Describe the difference between a "Release" and "Clear" instruction.
   Identical. Release is included in the 322X controllers to provide compatibility with the other 3000 series tape controllers.

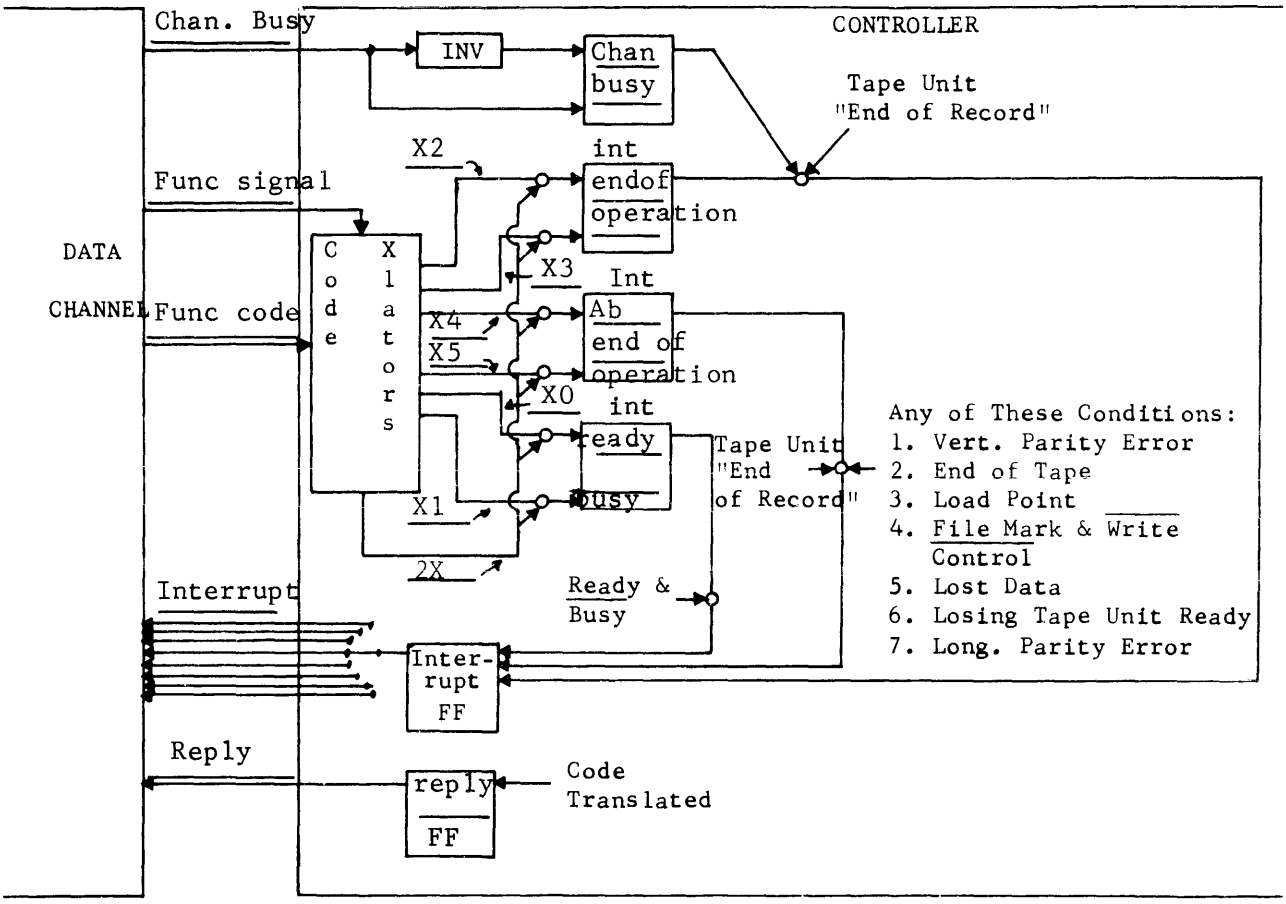
4. The controller is no longer connected to the Channel after the "Release" has been performed. T (F)

5. What instructions may be performed after a "Clear" instruction?

   "Connect" or another "clear".

XIII. INTERRUPT SELECTIONS AND RELEASES

1. Complete the following Block Diagram.



2. What is the purpose of the Interrupt Circuits?

Increase the efficiency of the system by releasing the computer from constantly having to monitor the I/O gear.

3. What prevents a "Reject" Signal when selecting or releasing an Interrupt?

   D108 = $\overline{2X}$. This blocks the setting of the Reject FF.

4. If all three Interrupts have been selected, can the programmer determine the type of Interrupt generated?

   Yes. By checking status.

5. What Interrupt conditions will disable the Read and Write Circuits?

   End of operation and abnormal end of operation.

6. What can clear the Interrupt FF J034/035 Pg. 111 if it has set?

   Master clear or a new 2X function code.

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