

Equipment Diagrams

CONTROL DATA 8092
TELEPROGRAMMER

Equipment Diagrams

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TELEPROGRAMMER

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8092 TERM LIST

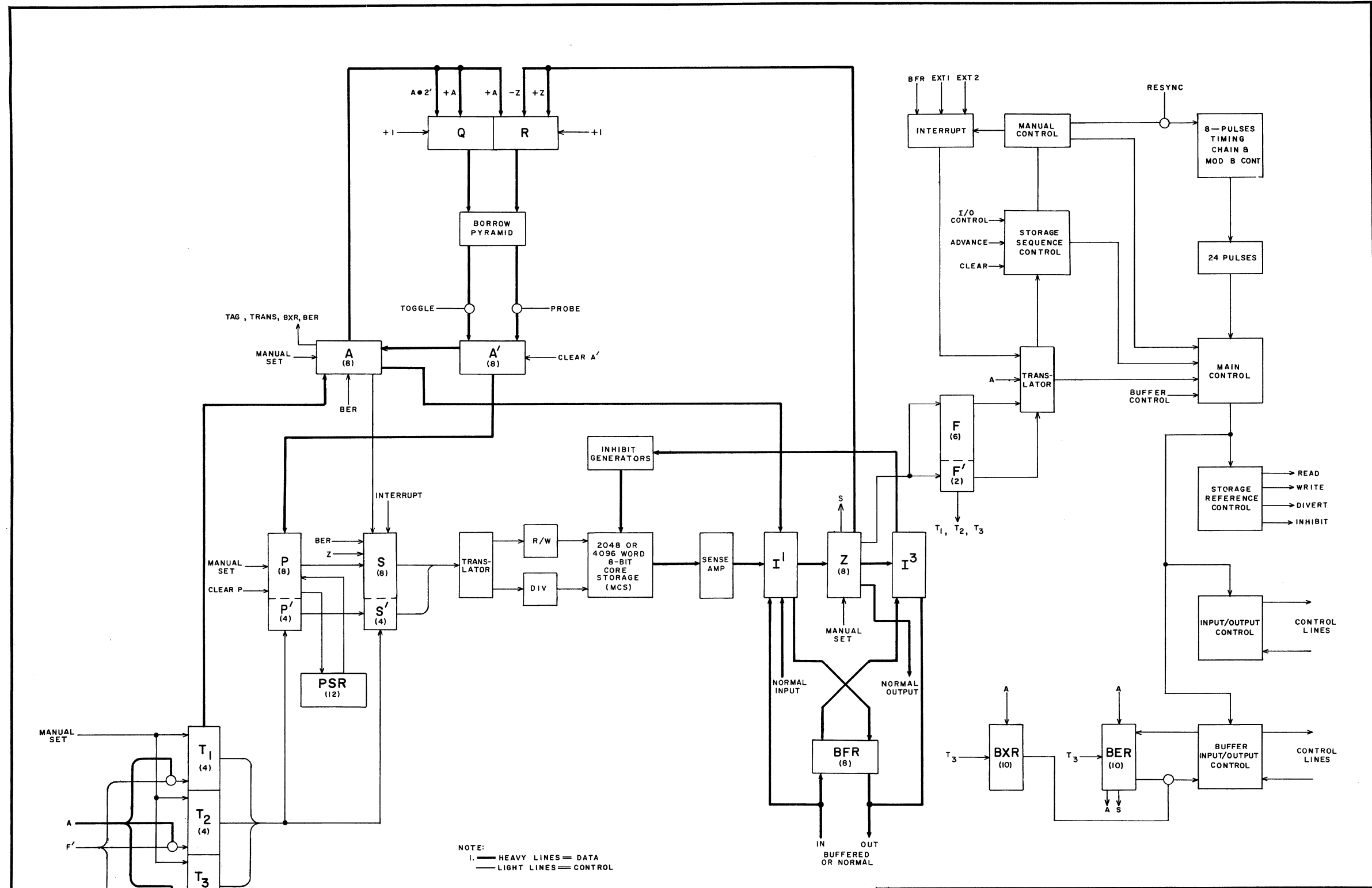
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A000, A010, A070	A Register	8	F081	001 XXX	4
A100, A110, A170	A' Register	7	082	01X XXX	4
C000- C007	Clocks	13	083	01X XXX	4
E000, E010-, E070	Stage Enable (SE) F/F's	6	084	100 XXX	4
E001, E011-, E071	No Stage Enable (SE) F/F's	6	085	101 XXX	4
E200, E201, E202	Group Enable (GI) A' Register	7	086	110 XXX	4
E300, E301, E302	Group Borrow Generators (GBG) A' Register	7	087	111 XXX	4
E400, E401, E402	Group Borrow Input (GBI) A' Register	7	088	000 XXX	4
E500, E501-, E507	Stage Probe Input (SPI) A' Register	7	089	000 XXX	4
F002	XXX XX0	4	090	001 XXX	4
003	XXX XXI	4	091	100 XXX	4
012	XXX XOX	4	092	101 XXX	4
013	XXX XIX	4	093	101 XXX	4
014	XXX XOX	4	094	110 XXX	4
015	XXX XIX	4	095	110 XXX	4
022	XXX OXX	4	096	111 XXX	4
023	XXX IXX	4	097	111 XXX	4
025	XXX IXX	4	098	111 XXX	4
031	XX0 XXX	4	099	111 XXX	4
041	XOX XXX	4	101	XIX XXX XX	4
042	XOX XXX	4	112	000 XXX	4
050	IXX XXX	4	114	111 XXX	4
052	OXX XXX	4	115	111 IXX, 111 111	4
053	IXX XXX	4	120	111 01X	4
054	XXX 100	4	121	111 01X	4
056	XXX 000	4	122	111 01X	4
057	XXX XII	4	123	111 01X	4
059	XXX IXX, XXX 111	4	124	111 101	4
060	XXX X10	4	125	111 101	4
061	XXX 001	4	127	111 01X	4
062	XXX 010	4	130	000 101	4
063	XXX 011	4	131	XXX IX1	4
064	XXX 100	4	132	OX1 XXX	4
065	XXX 110	4	133	OX1 XXX	4
066	XXX 111	4	134	011 XXX	4
067	XXX X01	4	F200	$G \rightarrow \overline{[(Ent. + Swp.) (SSI)]} \overline{[(4X + SX.C')]}$	5
068	XXX X00	4	F206	$\overline{[(SSI) (OBA) + C \overline{[(Ent. + Swp.) (SSI)]}]} \overline{[(4X + 5X.C' + 76) + 72.C'B \overline{[(Ent. + Swp.) (SSI)]}]} \overline{[(SSI)]} A (Ent)(Swp.) (SSI) + D \overline{[(Ent. + Swp.) (SSI)]} + (Swp.)$	5
069	XXX X10	4	F208	(Buff BSY) (04 + 05 + 70 + 71) + 6X (Jump SAT)	5
070	XXX 00X	4	F209	F208	5
071	XXX 001	4	F211	6X (Jump SAT) + (Buff BSY) (04 + 05 + 70 + 71)	5
072	XXX 010	4	F213	$\overline{17 + 23 + 24 + 27 + 33 + 37 + 44 + 45 + 46 + 47 + 52 + 56}$	5
073	XXX 011	4	F214	$31 + 35 + 41 + 45 + 51 + 55 + 72.C' + 73.C'$	5
074	XXX 100	4			
075	XXX 110	4			
076	XXX 111	4			
077	XXX X01	4			
078	XXX 00X	4			
079	XXX IX1	4			
080	000 XXX	4			

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F216	$\overline{[(Ent. + Swp.) (SSI)]} [B (11 + 15 + 41 + 45 + 51 + 55 + 72.C' + 73.C') + C (load + 00 + 04 + 05 + 10 + 14 + 20 + 24 + 30 + 34 + 6X + 70 + 71 + 72 + 73 + 74 + 75)] + A [(Ent.) (Swp.) (SSI)] + D (Ent. + Swp.) (SSI) + (Ent. + Swp.)$	5	F311	$\overline{Z \rightarrow F/F'}$	5
F222	$\overline{[(Ent. + Swp.) (SSI)]} [B (11 + 15 + 41 + 45 + 51 + 55 + 72.C' + 73.C') + C (Load + 00 + 04 + 05 + 10 + 14 + 20 + 24 + 30 + 34 + 6X + 70 + 71 + 72.C' + 73.C' + 74 + 75)] + A [(Ent.) (Swp.) (SSI)] + D [(Ent. + Swp.) (SSI)] + (Ent. + Swp.)$	5	F313	$\overline{Z \rightarrow Ou}$	5
F226	$12 + 16 + 22 + 26 + 32 + 36 + 42 + 46$		F315	$\overline{+Z \rightarrow R}$	5
F229	$11 + 12 + 13 + 15 + 16 + 17 + 22 + 23 + 26 + 27 + 31 + 32 + 33 + 35 + 36 + 5X.C' + 4X$	5	F316	$\overline{-Z \rightarrow R}$	5
F232	$04 + 05 + 20 + 21 + 22 + 23 + 30 + 31 + 32 + 33 + 5X + 70 + 72 + 74 + 75 + IX + 4X + 6X$	5	F317	$\overline{+I \rightarrow R}$	5
F233	$72 + 73 + 75$	5	F318	$\overline{A \rightarrow R}$	5
F235	01	5	F319	$\overline{A \rightarrow Q}$	5
F236	$5X + 72 + 73 + 75$	5	F320	$\overline{A.2' \rightarrow Q}$	5
F239	$5X.C' + 75.C' + (72 + 73) (A' 0) (I/O Seq.)$	5	F321	$\overline{+I \rightarrow Q}$	5
F242	$(Load) + 6X (Jump SAT) + 40 + 44 + 77 + (Buff BSY) (04 + 05 + 70 + 71)$	5	F322	Block Probe A'	5
F243	$C' + 55 + 75$	5	F323	$\overline{A' \rightarrow A}$	5
F248	A/O	5	F324	$\overline{A \rightarrow Tag Reg}$	5
F251	Jump SAT	5	F325	$\overline{Tag Reg \rightarrow A}$	5
F252	Jump SAT	5	F326	$\overline{A \rightarrow BER. I_3 \rightarrow BER}$	5
F256	$20 + 21 + 22 + 23 + 30 + 31 + 32 + 33 + (72 + 73) C [(Ent. + Swp.) (SSI)]$	5	F327	$\overline{A \rightarrow BXR, I_3 \rightarrow BXR}$	5
F261		5	F328	$\overline{BER \rightarrow A}$	5
F271	13	5	F329	$\overline{A' \rightarrow P, Tag \rightarrow P'}$	5
F300	$\overline{Adv. P_1 \text{ by } I}$	5	F331	$\overline{INP \rightarrow Z: \overline{76} + \overline{C} + (Ent + Swp) + (SSI)}$	5
F301	$\overline{P_2 - P_1}$	5	F332	$\overline{01 + \overline{D} + (Ent. + Swp) + (SSI)}$	7
F302	$\overline{P \rightarrow S, P' \rightarrow S'}$	5	F580	$70 + 71$	18
F303	$\overline{5.C'}$	12	F502	$\overline{[(Load + (Clear F/F') + (Ent + Swp))] (70 + 71)}$	18
F304	$\overline{Z \rightarrow S}$	5	F503	$\overline{[(Load) (Clear F/F') (Ent + Swp)] (70 + 71)}$	18
F305	$\overline{Tag \rightarrow S'}$	5	G000 - G207	Read Write Drivers	13
F306	$\overline{A \rightarrow S}$	5	H000 - H007	Plain Timing Delay's	3
F307	$\overline{MCS \rightarrow Z}$	5	H201 - H231	SSC Timing Delay's	2
F308	$\overline{INP \rightarrow Z: (Ent. + Swp.) (SSI) [B.72.C' + C(load)]}$	5	I001 - I005	Z Register	9
F310	$\overline{Clear F/F'}$		I006	Enables -- S	12
			I011 - I015	Z Register	9
			I016	S Register	12
			I021 - I025	Z Register	9
			I026	S Register	12
			I031 - I034	Z Register	9
			I036	S Register	12
			I041 - I045	Z Register	9
			I046	S Register	12
			I051 - I055	Z Register	9
			I056	S Register	12
			I061 - I065	Z Register	9
			I066	S Register	12
			I071 - I075	Z Register	9

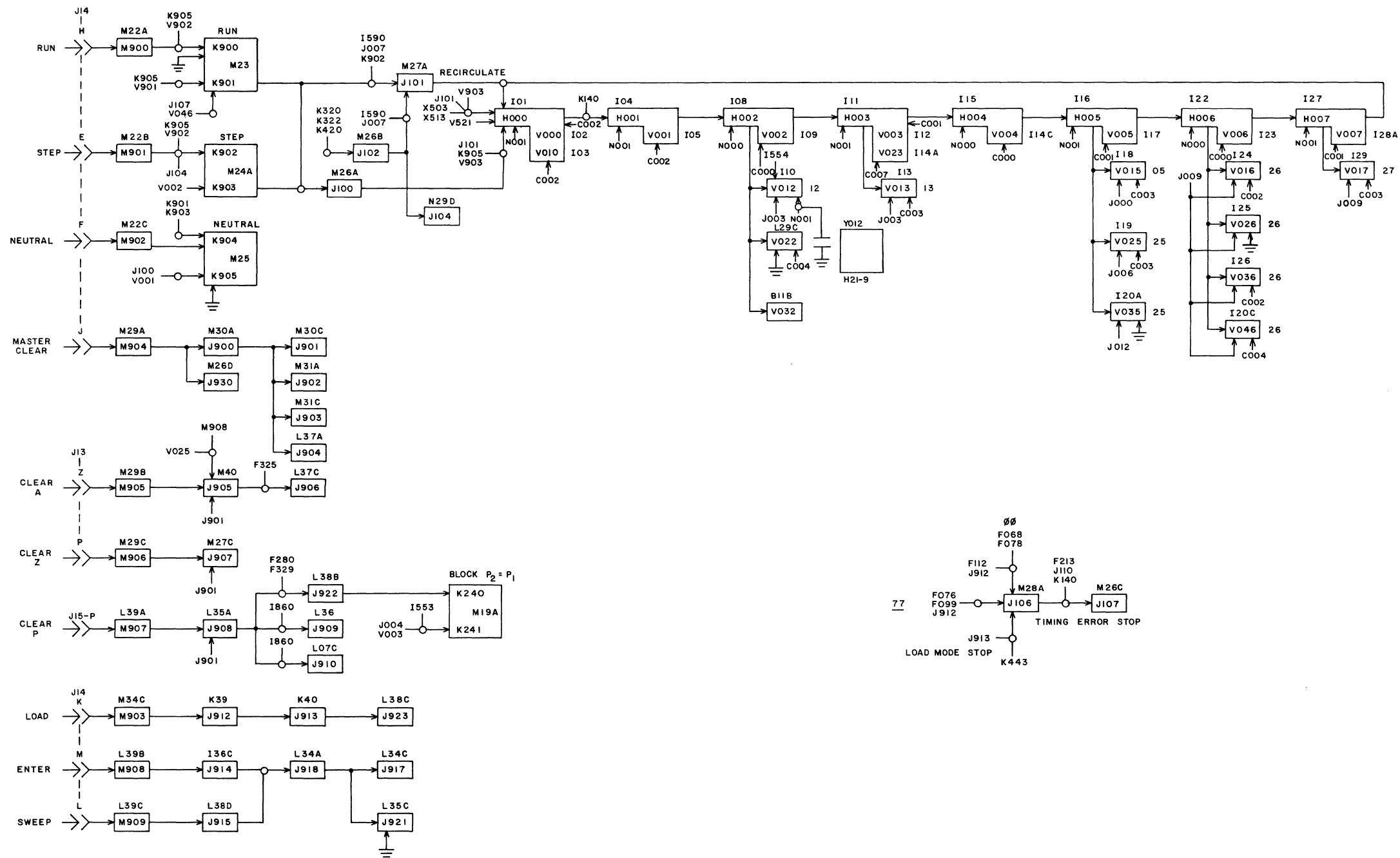
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I076	S Register	12	J104 - J107	Main Timing	3
I200 - I219	A Register	8	J109 - J111	I/O Control	16
I300 - I369	Tag Register 1, 2, 3	15	J107	Timing Error Stop	2
I400 - I401	A ¹ Register	7	J200	$\overline{A} + (\text{Ent}) + (\text{Swp}) + (\text{SSI})$	2
I402	A ¹ ≠ 0	7	J211 - J212	B $\overline{[(\text{Ent.} + \text{Swp.}) (\text{SSI})]}$	2
I403	A ¹ = 0	7	J221 - J222 - J223	C $\overline{[(\text{Ent.} + \text{Swp.}) (\text{SSI})]}$	2
I404 - I414	O Register	8	J224 - J225 - J226	C ¹	2
I500 - I538	BFR, BER, BXR	19	J227 - J228	\overline{C}^1	2
I519	BER = BXR		J231 - J232 - J233	D $\overline{(\text{Ent.} + \text{Swp.}) (\text{SSI})}$	2
I550	A $\overline{(\text{Ent}) (\text{Swp}) (\text{SSI})} + B \overline{(\text{Ent} + \text{Swp}) (\text{SSI})} +$ $(74 + 75 + 76) \overline{[(D (\text{Ent} + \text{Swp}) (\text{SSI}))]}$ $(\text{Load} + \overline{[(\text{Ent.} + \text{Swp}) (13) (00 + 01 + 02 + 03$ $+ 06 + 07 + 77) (011 \text{ 5X (Jump SAT) + (04 + 05$ $+ 70 + 71) (\text{Buff BSY})]} + C \overline{(\text{Ent} + \text{Swp}) (\text{SSI})}$ $(55 + 75)$	18	J235	I/O Control	16
I551	$\overline{(\text{IBA})} + \overline{(\text{OBA})}$	18	J243	(I/O Seq. Set)	16
I554	(Buffer Cycle)	18	J400 - J440	$(\text{Load}) + B \overline{[(\text{Ent.} + \text{Swp}) (\text{SSI})]}$	16
I560	BFR → Buff Output Cable (B. O. C)	18	J441	$(\text{Main Timing Fault})$	2
I561	Z → B.O.C.	18	J446	Storage	13
I562	Z → B.O.C.	18	J560	(Master Clear)	3
I570	(Buff RDY) + (IBA) + $\overline{(\text{input RDY})}$	18	J562 - J565	(Master Clear)	3
I571	INP → BFR	18	J900	$(\text{Master Clear } (\overline{\text{Clear Z}}))$	3
I573	(Buffer Cycle) + (OBA) + $\overline{(\text{Time 22})}$	18	J901 - J902 - J903	$(\text{Master Clear } (\text{Clear P}))$	3
I574	MCS → BFR	18	J904	Clear P ¹	3 & 10
I577	Buff INP Cable → Z	18	J907	$\overline{\text{Load}}$	3
I580	Clear Buffer Controls	18	J908	$\overline{\text{Load}}$	3
I582	Clear Buffer	18	J909 - J910	Enter	3
I588	(Buffer Busy)	18	J912	$\overline{(\text{Enter} + \text{Sweep})}$	3
I590	(SSI)	18	J913	$\overline{\text{Load}}$	3
I593	(Buff Cycle)	18	J914	(Master Clear)	3
I852	(Int. 10, 20, 30, 40)	17	J917 - J921	Timing Chain Excursion Counters	2
I853	Block P → S	17	J923	Divert	13
I857	(Block P → S) (I/O Seq) $\overline{(\text{Ent} + \text{Swp}) (\text{Load}) (\overline{13})}$	17	J930	Read	13
I859	(Master Clear) (Time 26) $(D \overline{(\text{Ent} + \text{Swp}) (\text{SSI})})$	17	K000 - K002	Write	13
I860	Clear P, P ¹	17	K010 - K013	Inhibit	13
I861	Interrupt Address → S	17	K100	Timing Fault	2
I862	(Int. 10, 20, 30, 40)	17	K110	A Cycle	2
I863	Interrupt Address Enable → S	17 & 12	K120	B Cycle	2
I872	Interrupt Address → PSR	17	K130	C Cycle	2
J000 - J031	Main Control Timing	2	K140	C ¹ Cycle	2
J100 - J103	Main Control Timing	3	K200	D Cycle	2
J103	Recirc		K210	Block P ₂ = P ₁	3
			K220	Wait Output	16
			K222 - K224	Function Ready	16
			K230	Wait Input	16
			K240		
			K320		
			K322		
			K420		

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K440	I/O Seq.	16	N212	$\overline{[(A \rightarrow \text{Tag}) + D + (\text{Ent.} + \text{Swp.}) + (\text{SSI})]}$ (Time 01)	7
K522	Sample	16	N230	Toggle A': $\overline{N232}$	7
K524	Enable	16	N232	$\overline{[(A \rightarrow \text{Tag}) + \overline{D} + (\text{Ent.} + \text{Swp.}) + (\text{SSI})]}$ (Time 23)	7
K800 - K802 - K810	Resync. Counter	2	N800 - N801	Clocks	2
K812	Manual Interrupt	16	0000 - 0010 - 0050	O Register	6
K850	Manual Interrupt	16	P000 - P010 - P070	P ₁ Register	10
K852	Manual Interrupt	16	P002 - P012 - P072	P ₂ Register	10
K854	Manual Interrupt 10	16	P100 - P110 - P120	P ₁ Register	10
K856	Buffer Interrupt	16	P130	P ₁ Register	10
K858	Buffer Interrupt 20	16	P102 - P112 - P122	P ₂ Register	10
K860	External Interrupt 30	16	P132	PSR - Register	11
K862	External Interrupt 40	16	P200 - P314	Q Inverters	6
K864	Interrupt Lockout	16	Q000 - Q010 - Q070	R Inverters	6
K900	Run	3	R000 - R010 - R070	Divert F/F's, S Register	13/12
K902	Step	3	S000 - S010 - S050	R/W Driver F/F's, S Register	13/12
K904	Neutral	3	S060 - S070	R/W Drive F/F's, S Register	13/12
L000 - L010 - L110	O Register Inputs	8	S100 - S110 - S120	Storage Translators	13
L321	Information Ready	16	S130	Stage Borrow F/F's (SB)	6
L322	Function Ready	16	T000 - T507	Timing	3
L323	Master Clear	16	U000 - U010 - U070	Storage Sequence Control	2
L330	I/O Sequence	16	V000 - V046	I/O Start of Timing	16
L331	Load Mode	16	V201 - V231	Resync Timing	2
L421	Input Request	16	V521	Adv. P ₁ by 1	10
L500 - L510 - L610	BFR Outputs	19	V901 - V903	Clear S and S'	12
L512	Information Ready	18	W000 - W005	Adv. BER: $\overline{(\text{Buff Cycle})}$ (time 13)	19
L513	Input Request	18	W020 - W023	ADV. BER	19
L514	Function Ready	18	W024	I0-6 → S	12
L515	Master Clear	18	W028	P ₁ → P ₁ P ₁ → P ₂ , P ₁ → P ₂	10
M000 - M010 - M070	Z Register Inputs	9	W058	Clear Z	9
M330	Output Resume	16	W070 - W073	Strobe	9
M420	Input Ready	16	W100	Enable Z → S	12/17
M424	Input Disconnect	16	W102	Input → Z	9
M500 - M510 - M570	BFR Inputs	19	W110	Clear F, Z → F	4
M512	Output Resume	18	W122 - W124		
M513	Input Ready	18	W130 - W160		
M514	Input Disconnect	18			
M850	Manual Interrupt Input	17			
M851 - M852	External Interrupt Input	17			
M900	Run	3			
M901	Step	3			
M902	Neutral	3			
M903	Load	3			
M904	Master Clear	3			
M905	Clear A	3			
M906	Clear Z	3			
M907	Clear P	3			
M908	Enter	3			
M909	Sweep	3			
N000 - N005	Timing Control	2			
N210	Clear A' : N212	7			

<u>Logic Symbol</u>	<u>Function</u>	<u>Page</u>
W162 - W164	Z → 0	8
W200 - W314	R & Q Inverters	6
W250 - W264	A [†] → A, BER → A, TAG → A	8
W266 - W269	A → BER	19
W320 - W327	Z Register	9
W330 - W363	BXR	19
W364 - W368	TAG 1, 2, 3	15
W370 - W375	(Buff Cycle) (Time 02)	19
W460 - W464	A [†] → P, TAG → P [†]	10
W800	P → P [†]	11
W810	$\overline{13} + (\text{Load}) + (\overline{\text{Clear F}}) + (\text{Ent.} + \text{Swp}) +$ (Time 23)	11
W813	13 (Load) (Clear F) ($\overline{\text{Ent.} + \text{Swp.}}$) (Time 23)	11
X000 - X010 - X020 X030	Tag 1 Register	15
X100 - X110 - X120 X130	Tag 2 Register	15
X200 - X210 - X220 X230	Tag 3 Register	15
X500	Block Seq. Interrupt (F/F)	18
X502	Storage Seq. Interrupt (SSI) (F/F)	18
X504	Buffer Cycle (F/F)	18
X506	Buffer Ready (F/F)	18
X508	Buffer Input (IBA) (F/F)	18
X510	Buffer Output (OBA) (F/F)	18
X512	Buffer Step (F/F)	18
X514	Initiate Buffer Output (F/F)	18
X516	Buffer Busy (F/F)	18
X518	Buffer Sync. (F/F)	18
X700 - X710 - X770	BFR Register	
X800 - X810 - X890	BXR Register	19
X900 - X910 - X990 X902 - X912 - X992	BER Register	19
Y006 - Y507	Storage	13
Z000 - Z010 - Z070	Z Register	9



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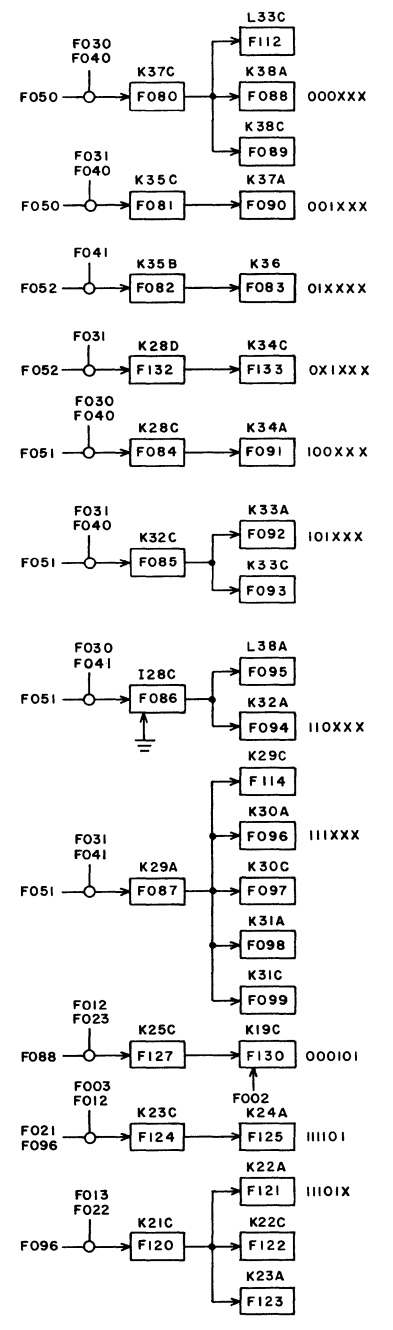
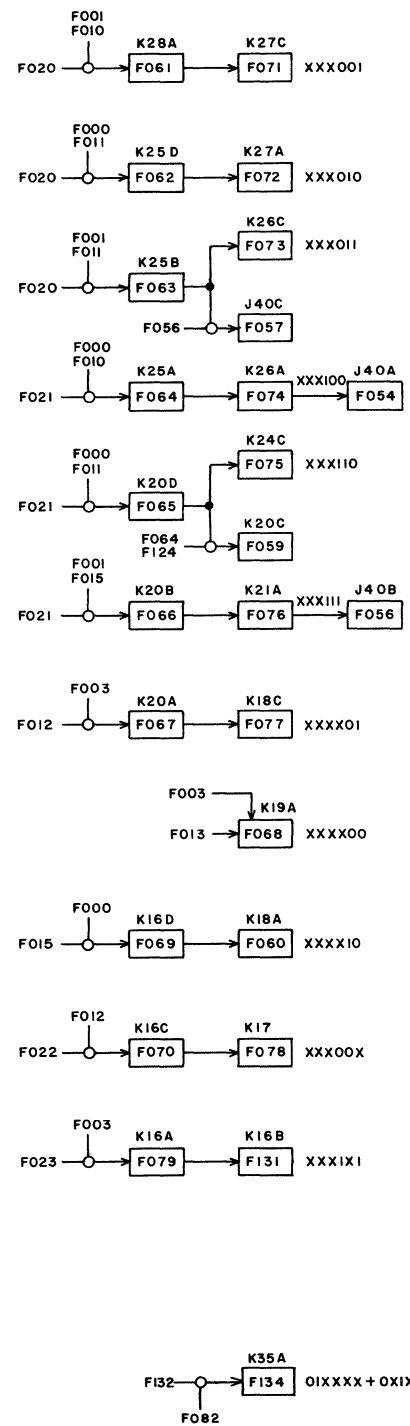
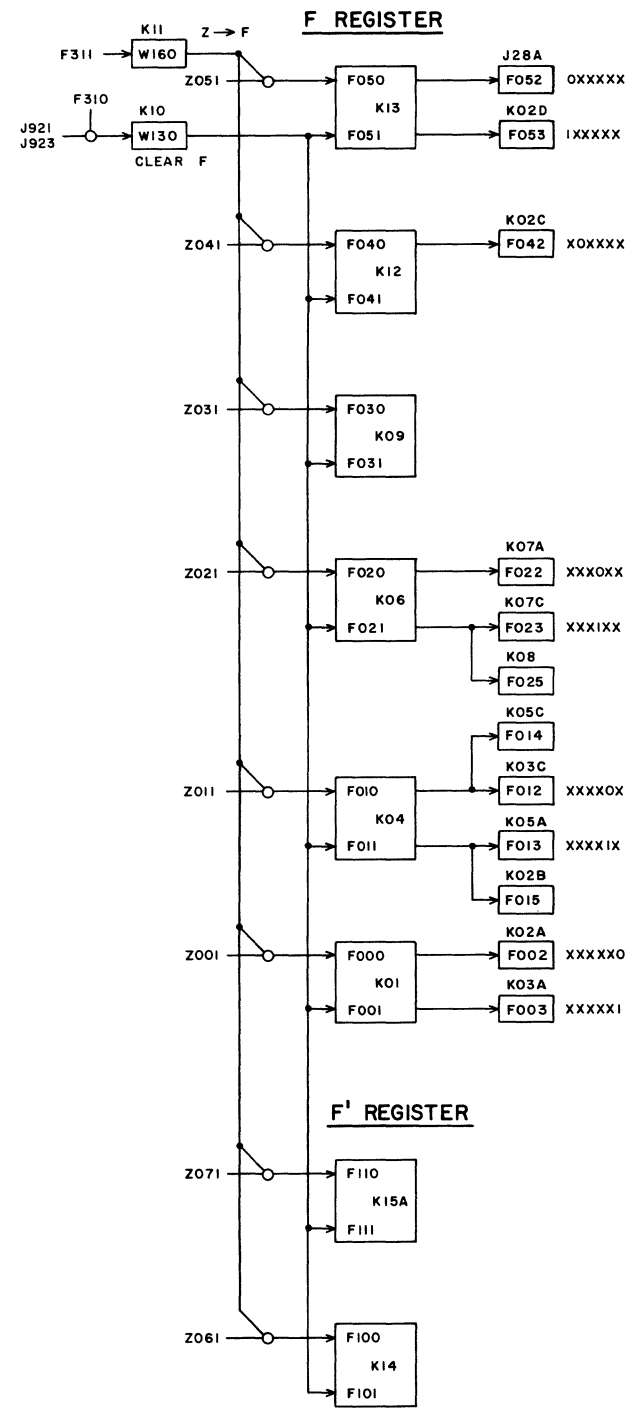
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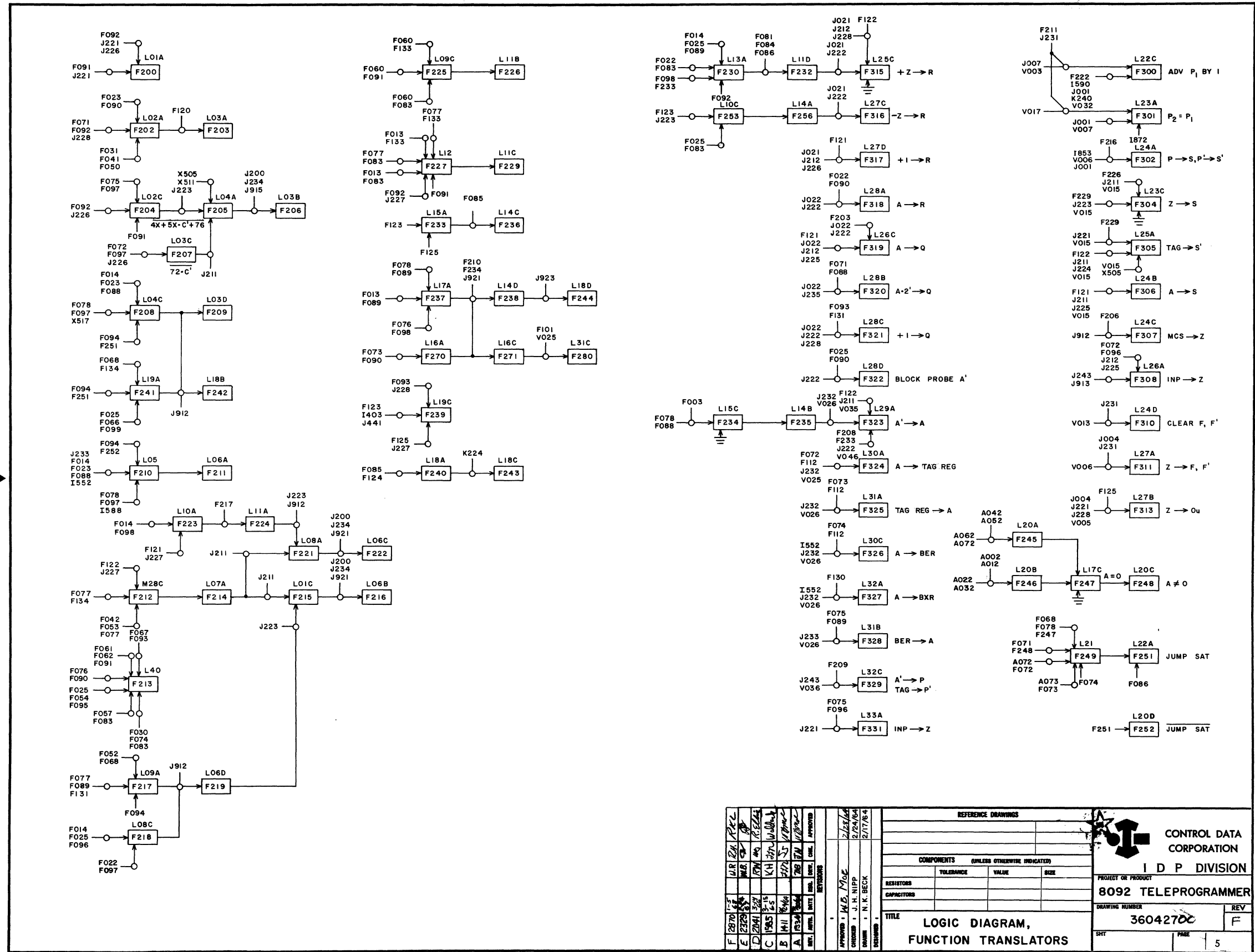
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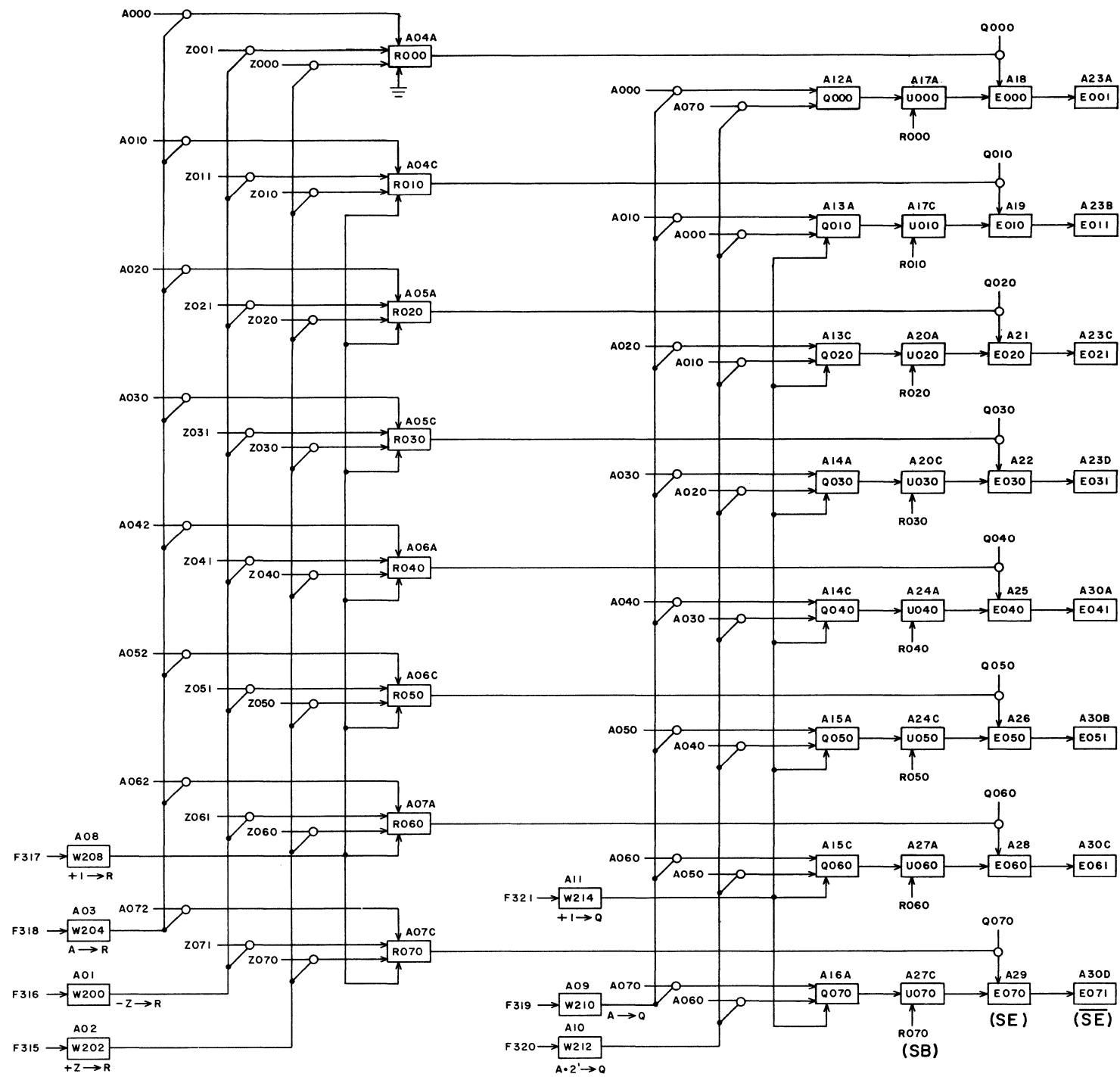
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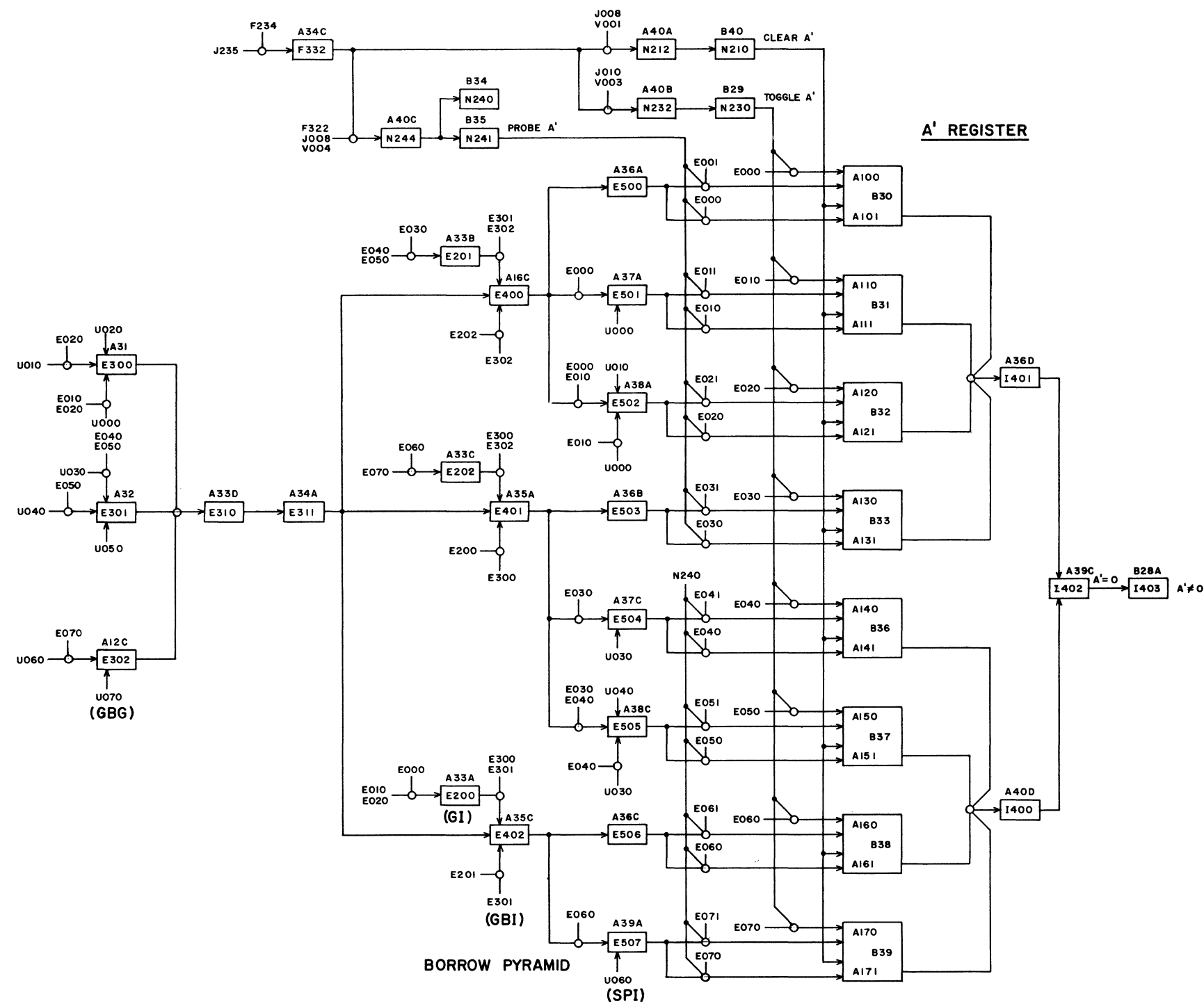


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	RESISTORS		
CAPACITORS			
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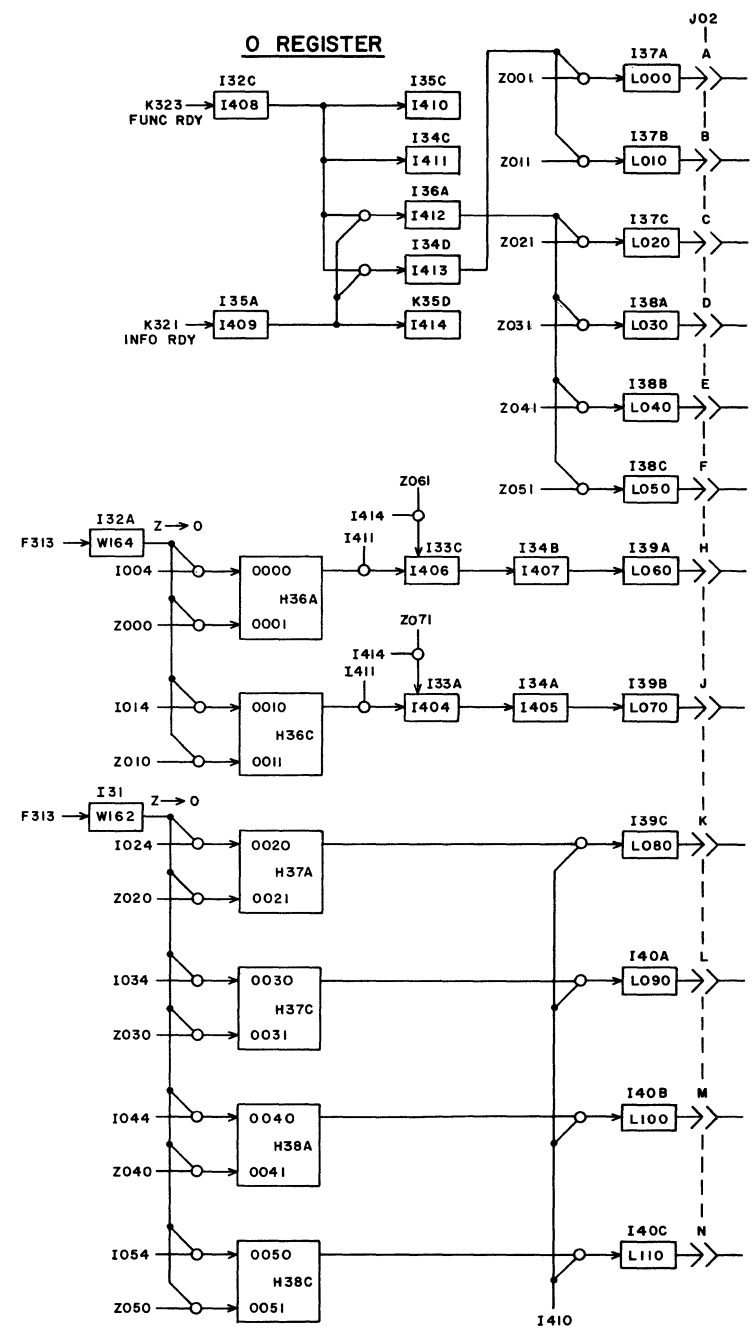
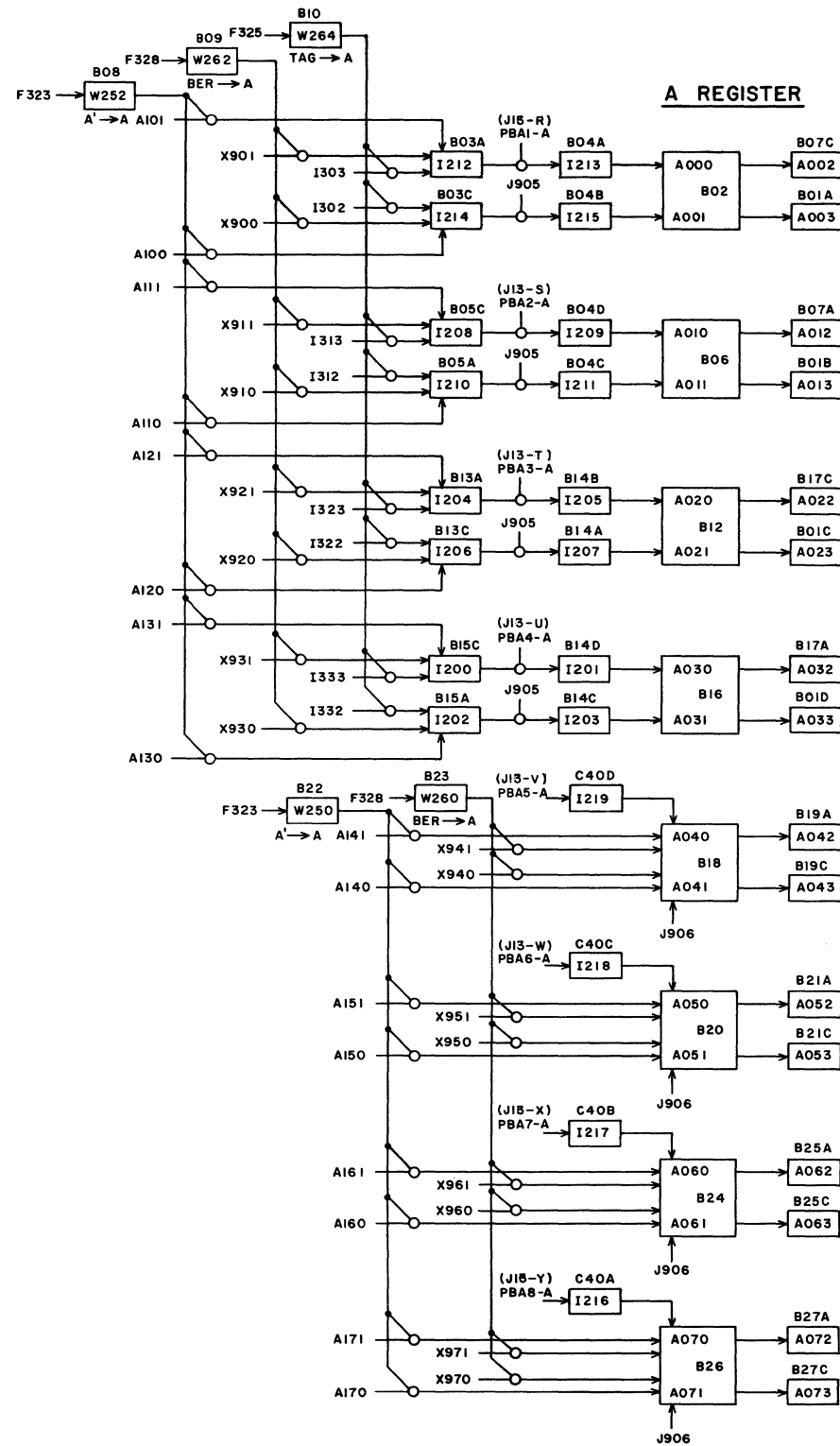
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CAPACITORS			
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7



REV.	DATE	BY	CHK.	APPROVED
C	12/01/64	R.M. R.	R.E.E.	
B	5/8/64	K.H.		
A	1/3/64	J.H.		

REF. DRAWING	COMPONENTS (UNLESS OTHERWISE INDICATED)
	RESISTORS
	CAPACITORS
TITLE LOGIC DIAGRAM REGISTERS - A AND O	

CONTROL DATA CORPORATION
I D P DIVISION

PROJECT OR PRODUCT
8092 TELEPROGRAMMER

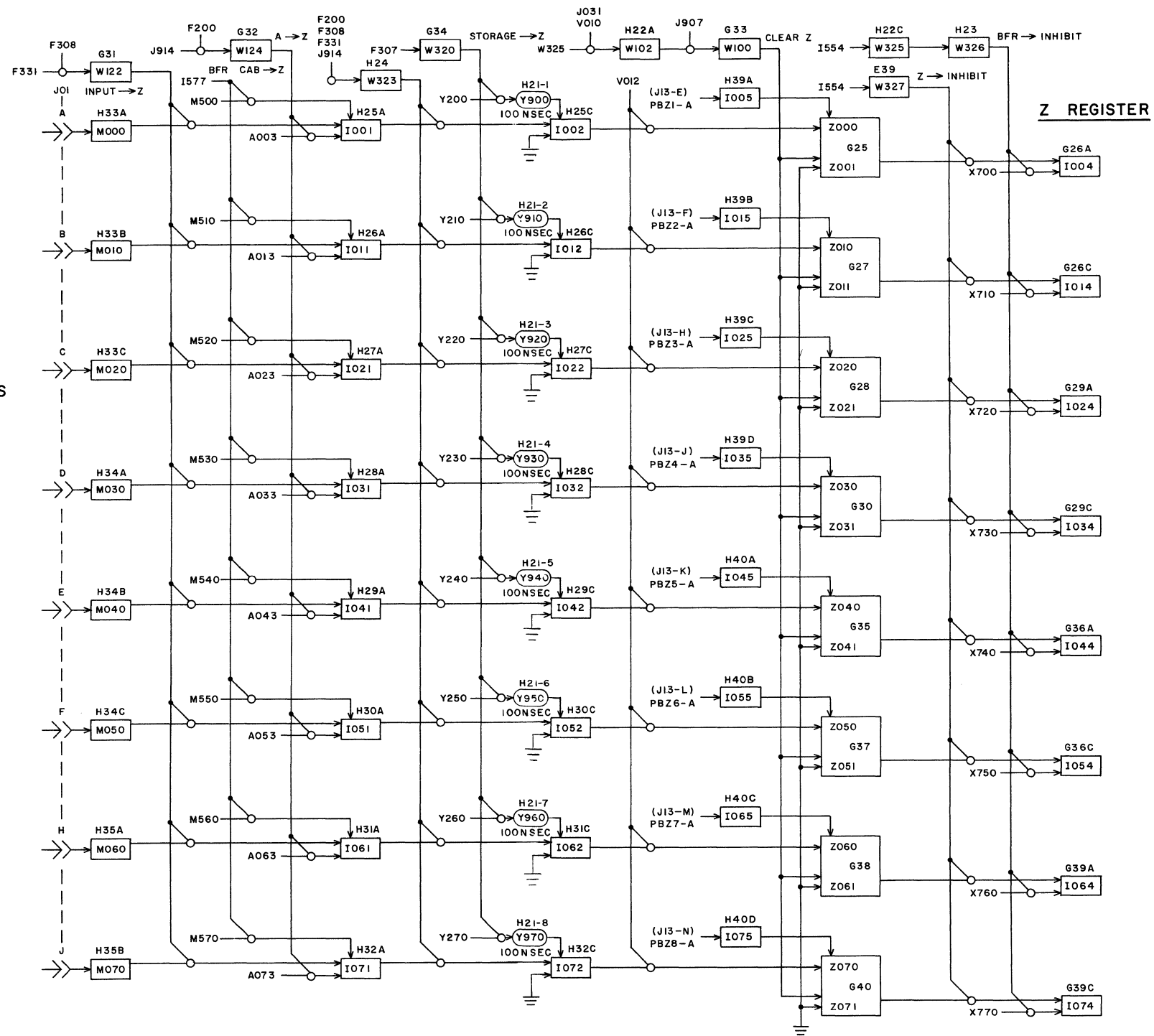
DRAWING NUMBER
360429

REV
C

SHEET
8

SENSE AMPLIFIERS

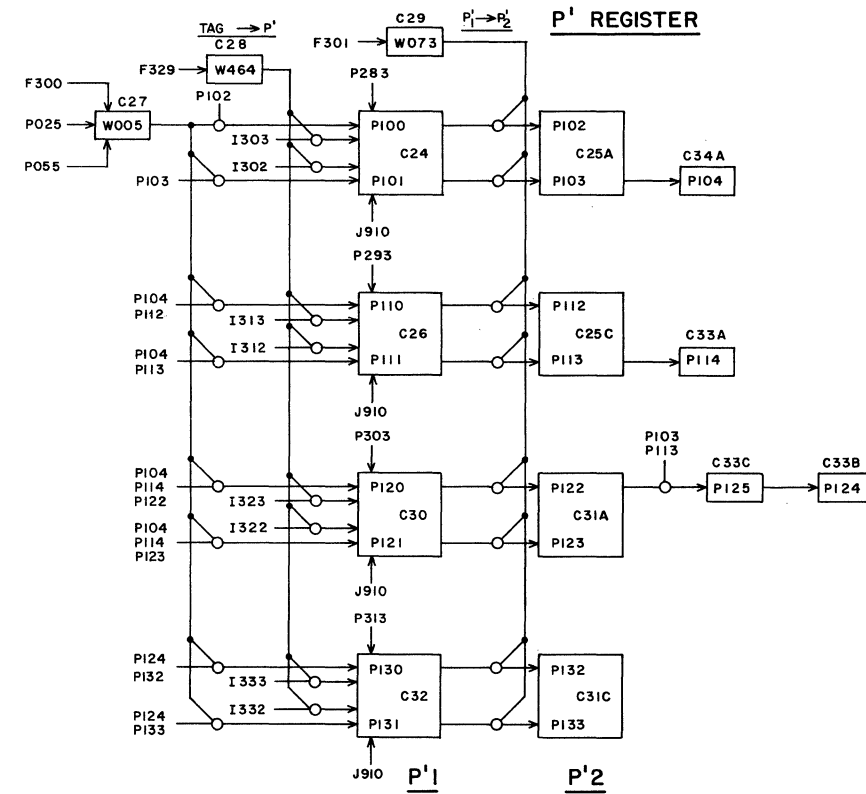
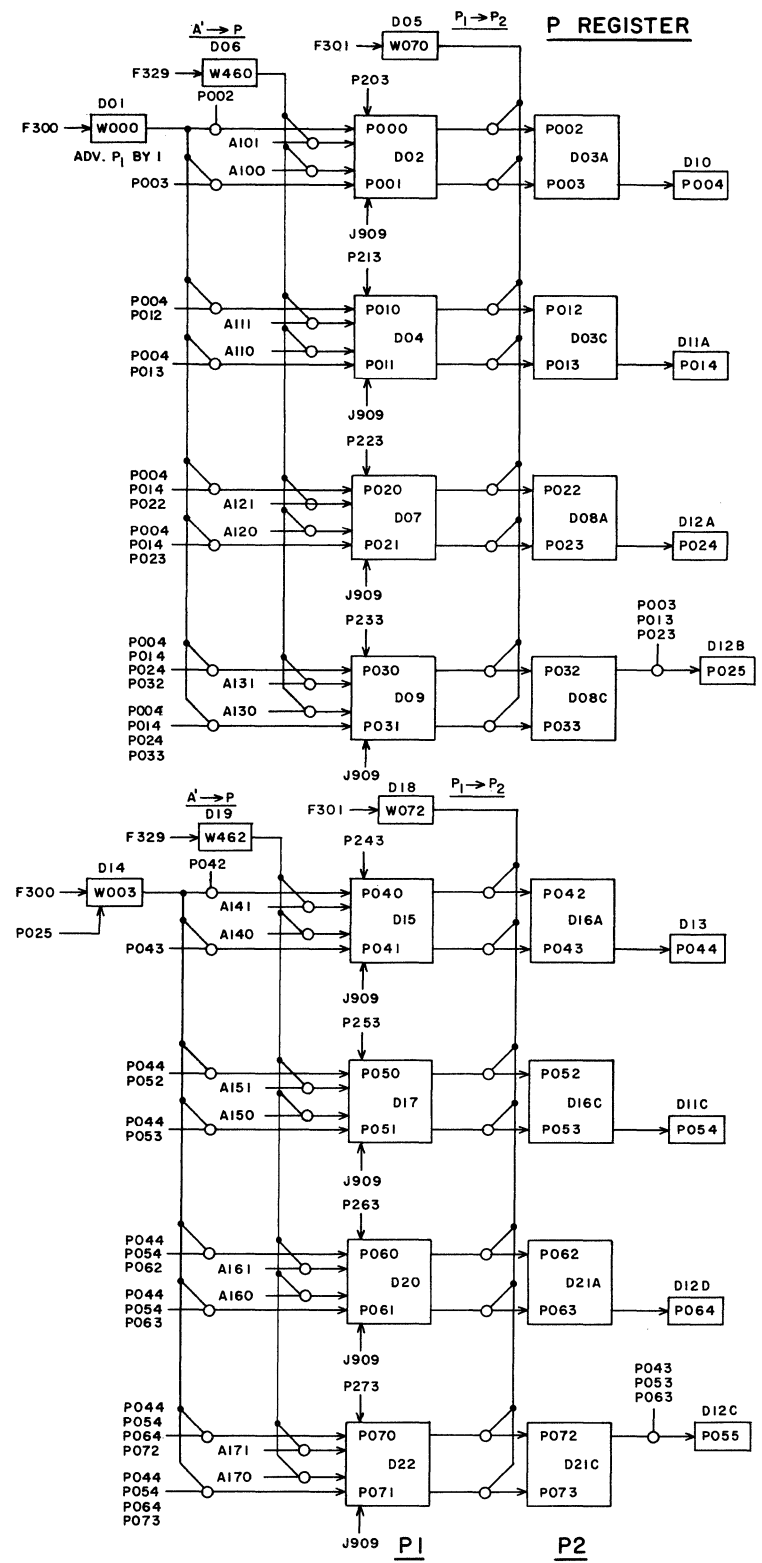
- H01 Y200
- H02 Y210
- H03 Y220
- H04 Y230
- H05 Y240
- H06 Y250
- H07 Y260
- H08 Y270



REV. DATE		REV. DATE		REV. DATE		REV. DATE	
B	1/6/64	A	1/6/64				
APPROVED: J. H. NIPP				APPROVED: N. K. BECK			
CHECKED: J. H. NIPP				CHECKED: N. K. BECK			
DESIGNED: J. H. NIPP				DESIGNED: N. K. BECK			
DRAWN: J. H. NIPP				DRAWN: N. K. BECK			
DATE: 2/24/64				DATE: 2/7/64			

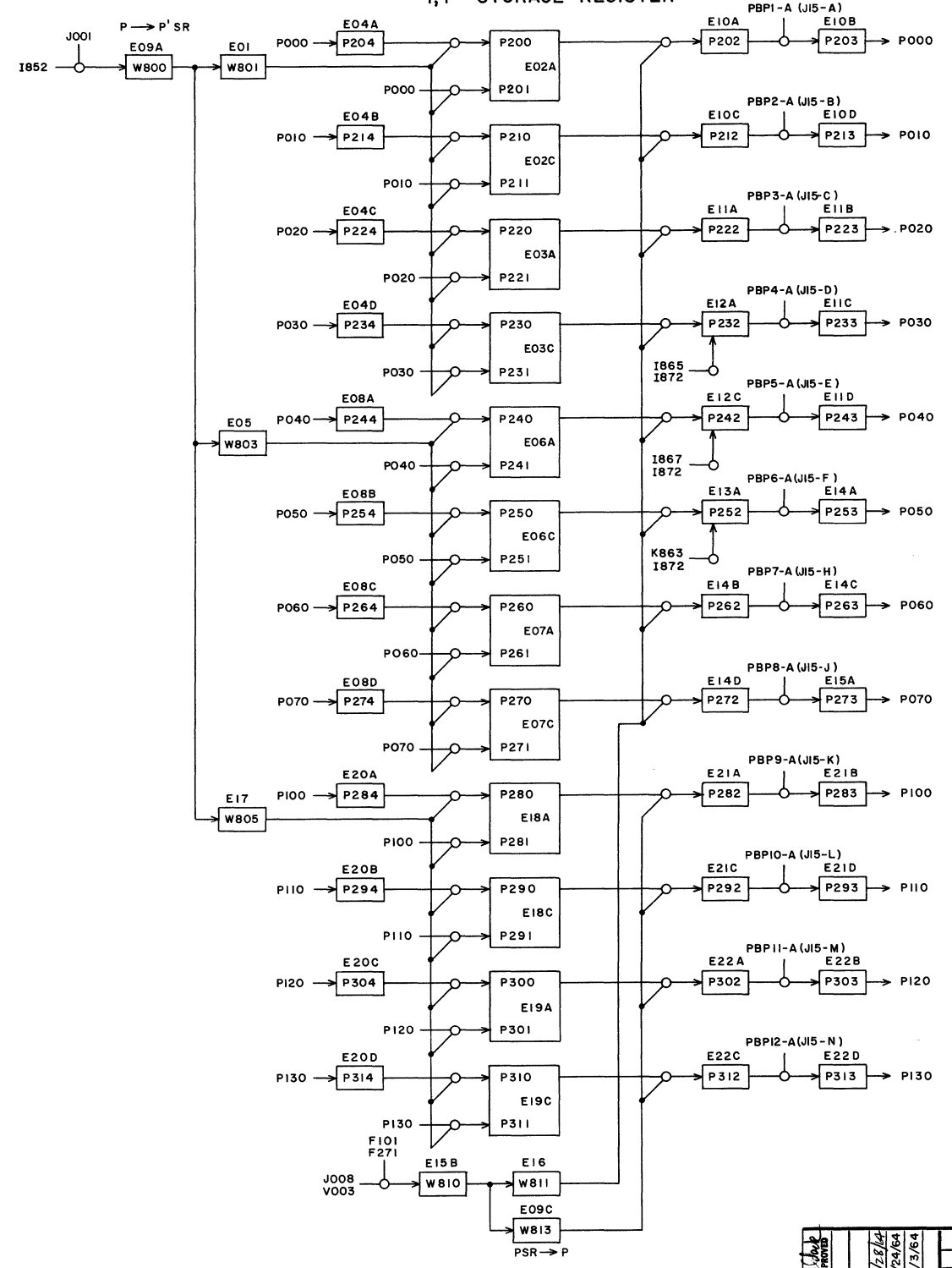
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COMPONENTS (UNLESS OTHERWISE INDICATED)			
RESISTORS	TOLERANCE	VALUE	SIZE
CAPACITORS	TOLERANCE	VALUE	SIZE
TITLE			
LOGIC DIAGRAM REGISTER-Z			

CONTROL DATA CORPORATION	
I D P DIVISION	
PROJECT OR PRODUCT	
8092 TELEPROGRAMMER	
DRAWING NUMBER	REV
364158	B
SHT	PAGE
	9




REVISIONS APPROVED: W.B. MOE CHECKED: J.H. NIPP DRAWN: N.K. BECK DESIGNED:	REFERENCE DRAWINGS			CONTROL DATA CORPORATION I D P DIVISION PROJECT OR PRODUCT 8092 TELEPROGRAMMER DRAWING NUMBER 360430 REV A
	COMPONENTS (UNLESS OTHERWISE INDICATED)			
	RESISTORS	TOLERANCE	VALUE	SIZE
	CAPACITORS			
TITLE				SHEET 10
LOGIC DIAGRAM REGISTERS - P AND P'				

P, P' STORAGE REGISTER



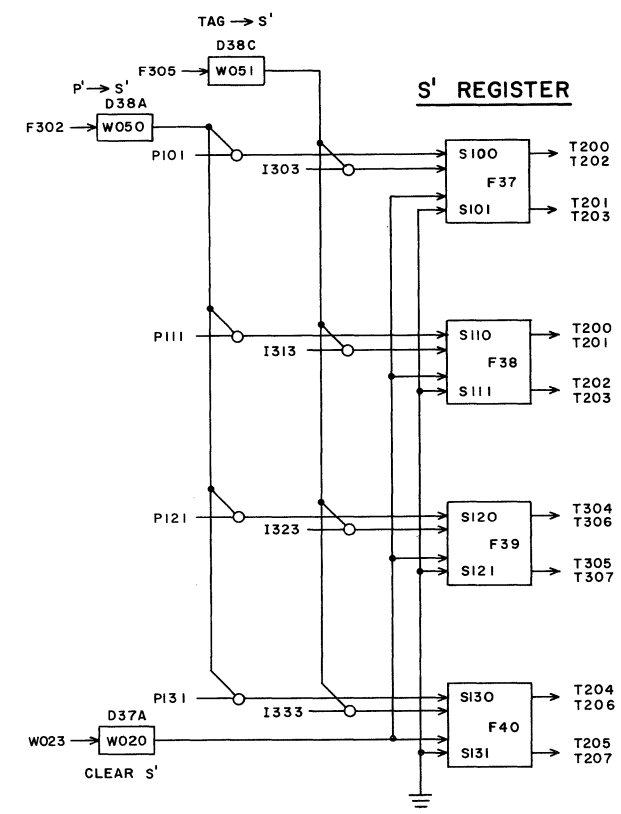
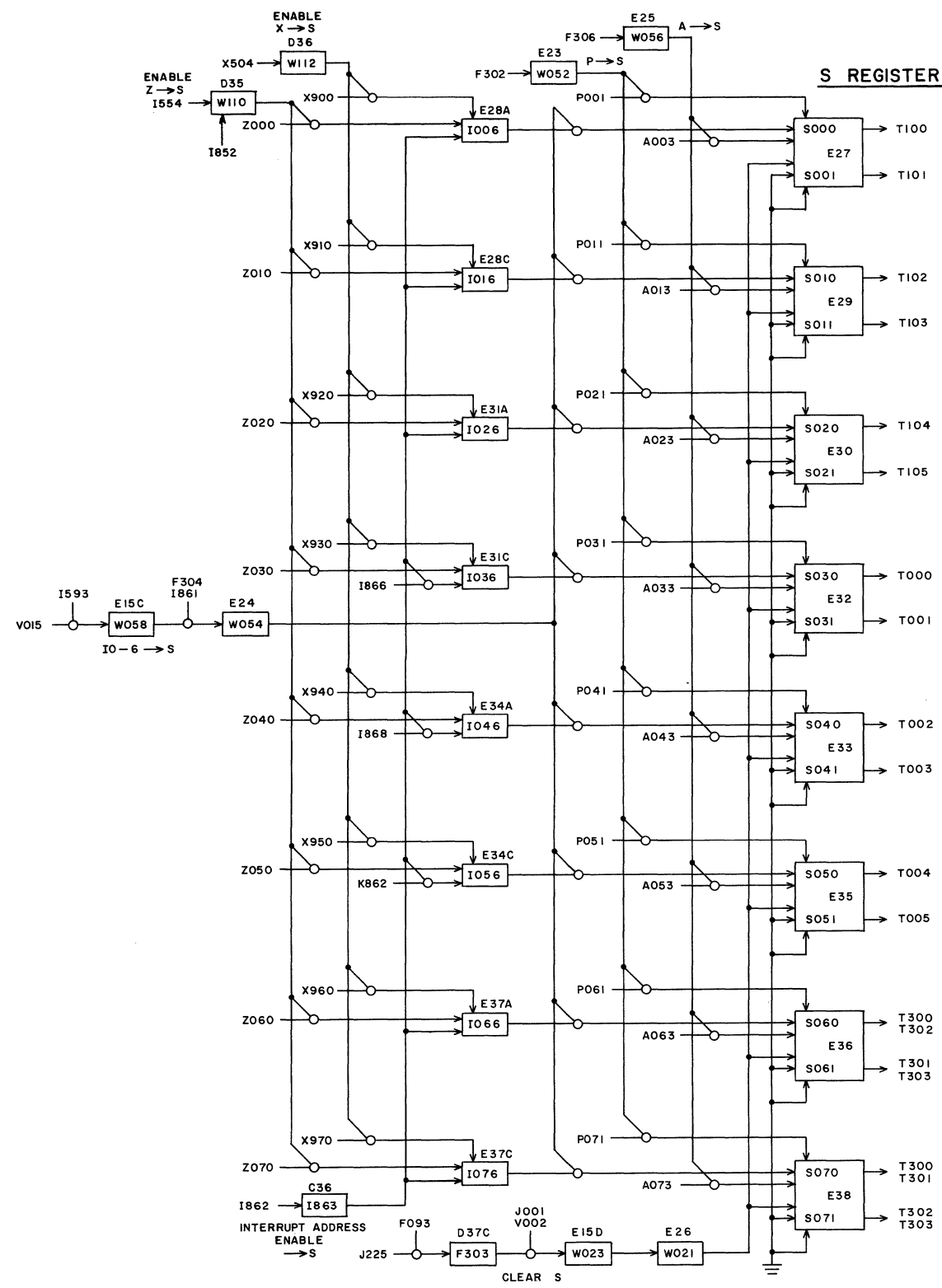
APPROVED	DATE	BY
2/2/64	J.F. NIPP	
CHECKED	DATE	BY
2/24/64	J.F. NIPP	
DRAWN	DATE	BY
2/13/64	N.K. BECK	
DESIGNED		

REFERENCE DRAWINGS			
COMPONENTS (UNLESS OTHERWISE INDICATED)			
RESISTORS	TOLERANCE	VALUE	SIZE
CAPACITORS			
TITLE			
LOGIC DIAGRAM REGISTER - PSR			

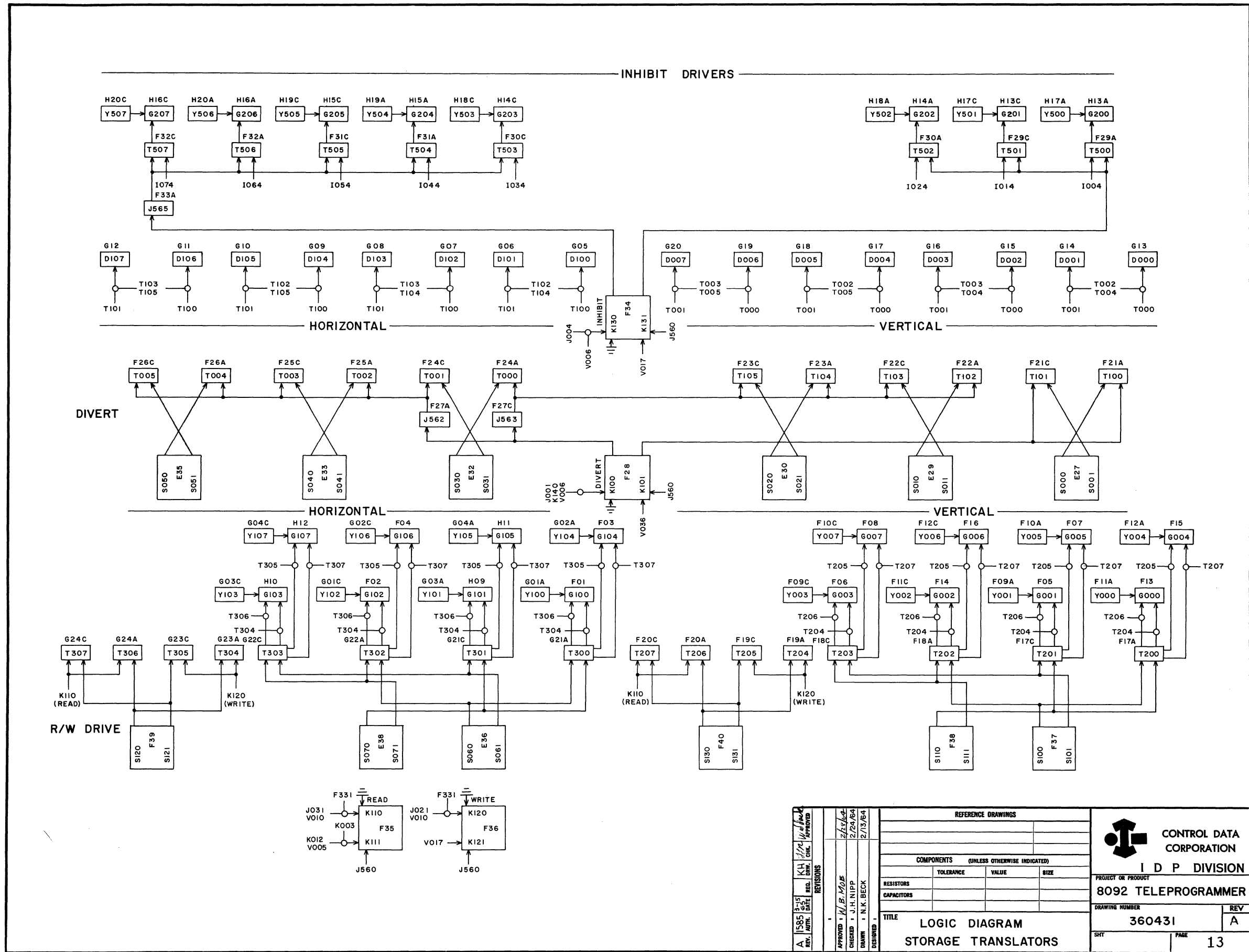


CONTROL DATA CORPORATION
I D P DIVISION

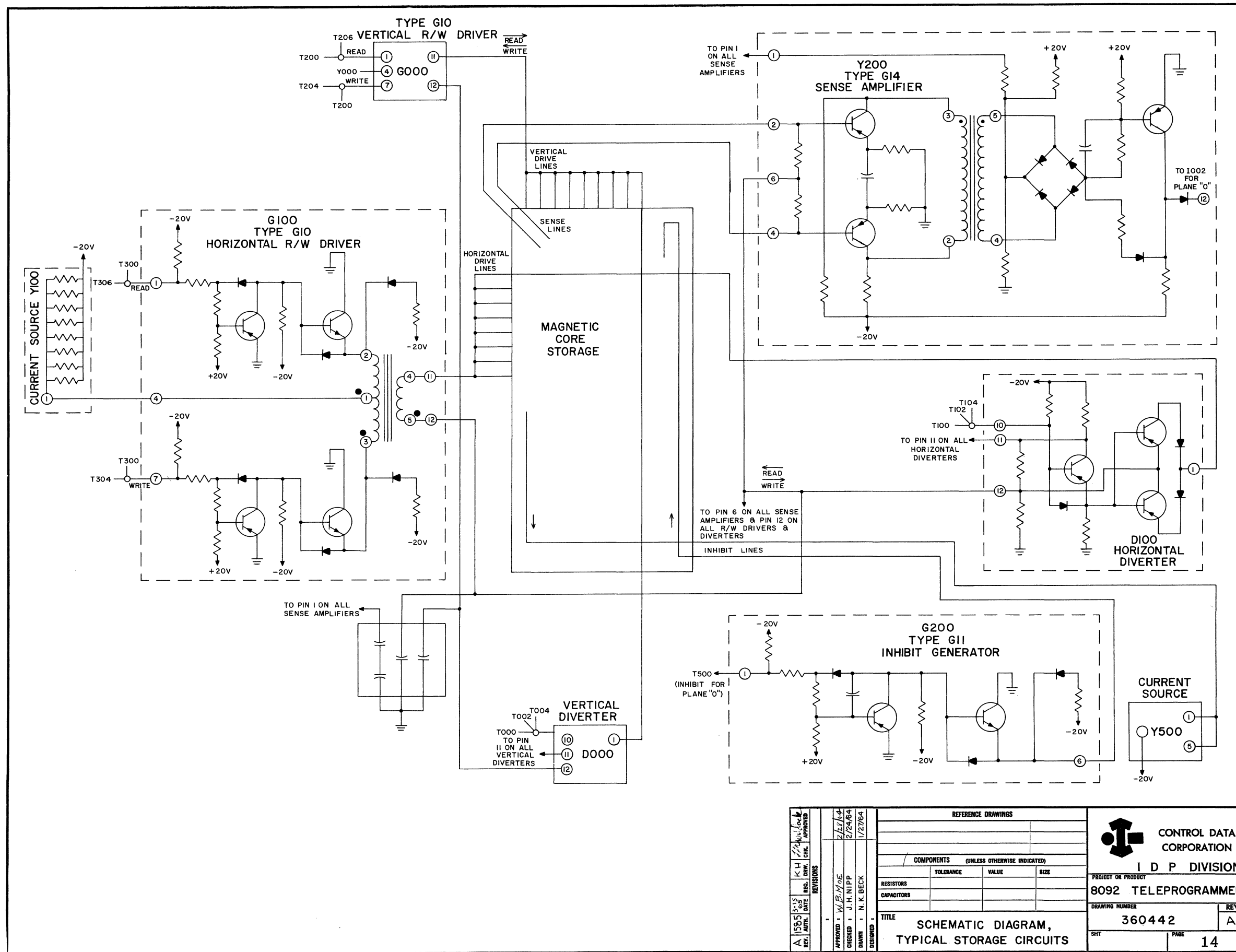
PROJECT OR PRODUCT	
8092 TELEPROGRAMMER	
DRAWING NUMBER	REV
364159	A
SHT	PAGE
11	11



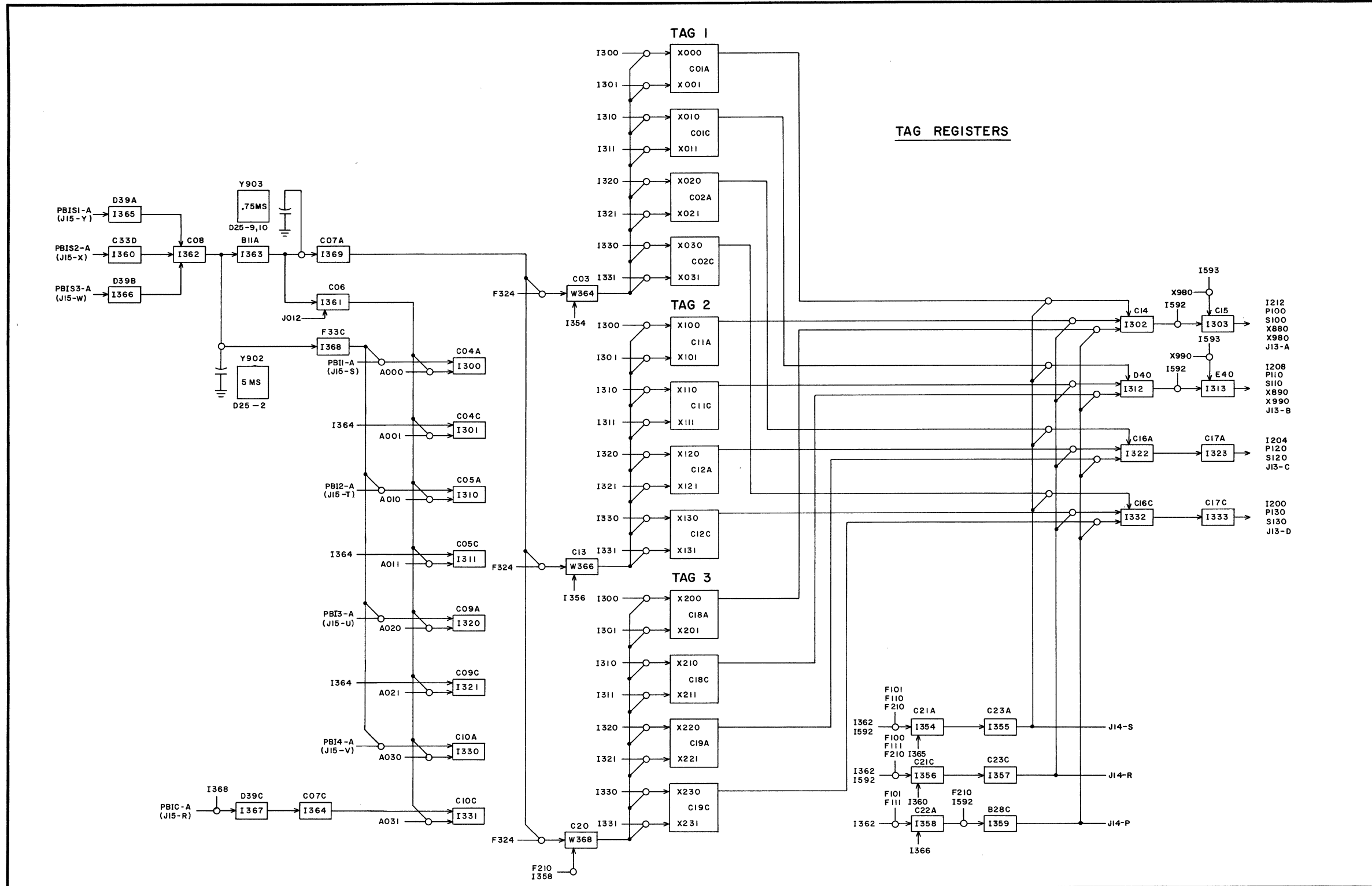
APPROVED: <i>[Signature]</i> CHECKED: J. H. NIPP DRAWN: N. K. BECK DESIGNED:		REFERENCE DRAWINGS _____ _____ _____ _____		CONTROL DATA CORPORATION I D P DIVISION PROJECT OR PRODUCT 8092 TELEPROGRAMMER																			
REVISIONS 1. 1/15/64 2. 2/24/64 3. 2/5/64		COMPONENTS (UNLESS OTHERWISE INDICATED) <table border="1"> <thead> <tr> <th>RESISTORS</th> <th>TOLERANCE</th> <th>VALUE</th> <th>SIZE</th> </tr> </thead> <tbody> <tr> <td> </td> <td> </td> <td> </td> <td> </td> </tr> <tr> <td> </td> <td> </td> <td> </td> <td> </td> </tr> <tr> <td> </td> <td> </td> <td> </td> <td> </td> </tr> <tr> <td> </td> <td> </td> <td> </td> <td> </td> </tr> </tbody> </table>			RESISTORS	TOLERANCE	VALUE	SIZE															
RESISTORS	TOLERANCE	VALUE	SIZE																				
TITLE LOGIC DIAGRAM REGISTERS - S AND S'		DRAWING NUMBER 364160		REV A																			
SHEET 12		PAGE 12																					




APPROVED: <i>[Signature]</i> CHECKED: J.H. NIPP DRAWN: N.K. BECK DESIGNED:		REFERENCE DRAWINGS COMPONENTS (UNLESS OTHERWISE INDICATED) RESISTORS CAPACITORS	CONTROL DATA CORPORATION I D P DIVISION PROJECT OR PRODUCT 8092 TELEPROGRAMMER DRAWING NUMBER 360431 REV A
TITLE LOGIC DIAGRAM STORAGE TRANSLATORS	SHEET 13	PAGE 13	

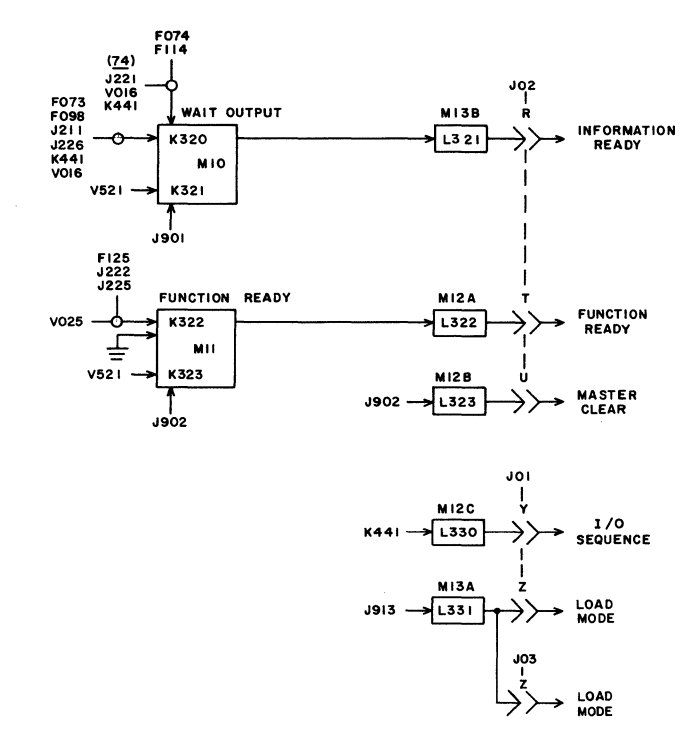
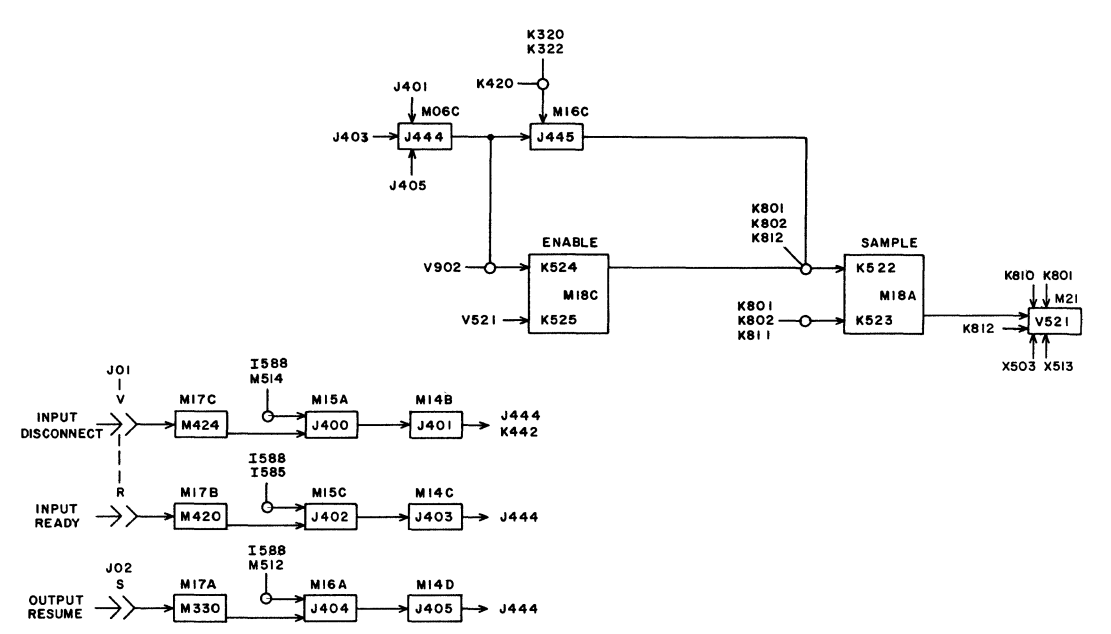
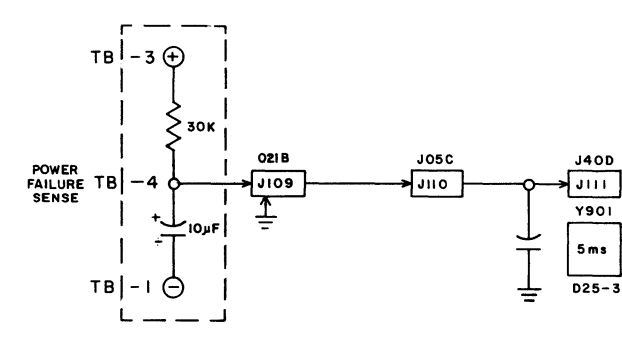
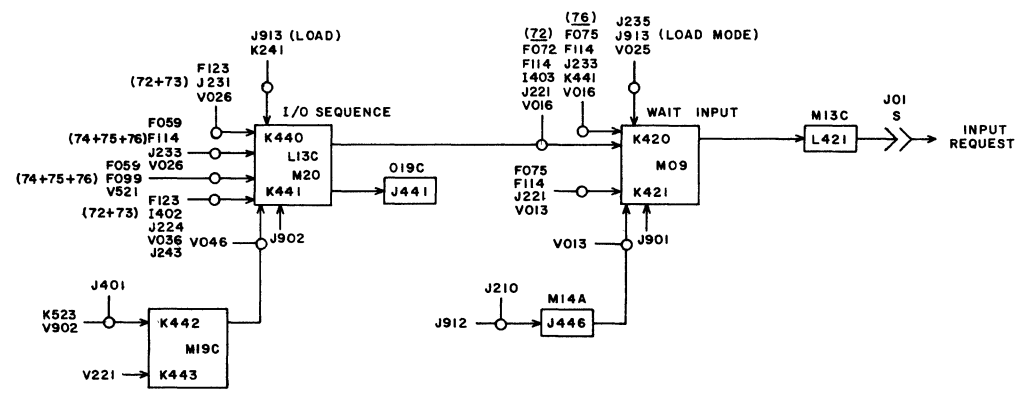


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K.H.		K.H.		K.H.		K.H.		K.H.	
2/24/64		2/24/64		1/27/64					
J.H.NIPP		J.H.NIPP		N.K.BECK					
DESIGNED		DESIGNED		DESIGNED					
TITLE		TITLE		TITLE		TITLE		TITLE	
SCHEMATIC DIAGRAM,		SCHEMATIC DIAGRAM,		SCHEMATIC DIAGRAM,		SCHEMATIC DIAGRAM,		SCHEMATIC DIAGRAM,	
TYPICAL STORAGE CIRCUITS		TYPICAL STORAGE CIRCUITS		TYPICAL STORAGE CIRCUITS		TYPICAL STORAGE CIRCUITS		TYPICAL STORAGE CIRCUITS	
REFERENCE DRAWINGS		REFERENCE DRAWINGS		REFERENCE DRAWINGS		REFERENCE DRAWINGS		REFERENCE DRAWINGS	
COMPONENTS (UNLESS OTHERWISE INDICATED)		COMPONENTS (UNLESS OTHERWISE INDICATED)		COMPONENTS (UNLESS OTHERWISE INDICATED)		COMPONENTS (UNLESS OTHERWISE INDICATED)		COMPONENTS (UNLESS OTHERWISE INDICATED)	
TOLERANCE		TOLERANCE		TOLERANCE		TOLERANCE		TOLERANCE	
VALUE		VALUE		VALUE		VALUE		VALUE	
SIZE		SIZE		SIZE		SIZE		SIZE	
RESISTORS		RESISTORS		RESISTORS		RESISTORS		RESISTORS	
CAPACITORS		CAPACITORS		CAPACITORS		CAPACITORS		CAPACITORS	
CONTROL DATA CORPORATION		CONTROL DATA CORPORATION		CONTROL DATA CORPORATION		CONTROL DATA CORPORATION		CONTROL DATA CORPORATION	
I D P DIVISION		I D P DIVISION		I D P DIVISION		I D P DIVISION		I D P DIVISION	
PROJECT OR PRODUCT		PROJECT OR PRODUCT		PROJECT OR PRODUCT		PROJECT OR PRODUCT		PROJECT OR PRODUCT	
8092 TELEPROGRAMMER		8092 TELEPROGRAMMER		8092 TELEPROGRAMMER		8092 TELEPROGRAMMER		8092 TELEPROGRAMMER	
DRAWING NUMBER		DRAWING NUMBER		DRAWING NUMBER		DRAWING NUMBER		DRAWING NUMBER	
360442		360442		360442		360442		360442	
REV		REV		REV		REV		REV	
A		A		A		A		A	
SHEET		SHEET		SHEET		SHEET		SHEET	
PAGE		PAGE		PAGE		PAGE		PAGE	
14		14		14		14		14	

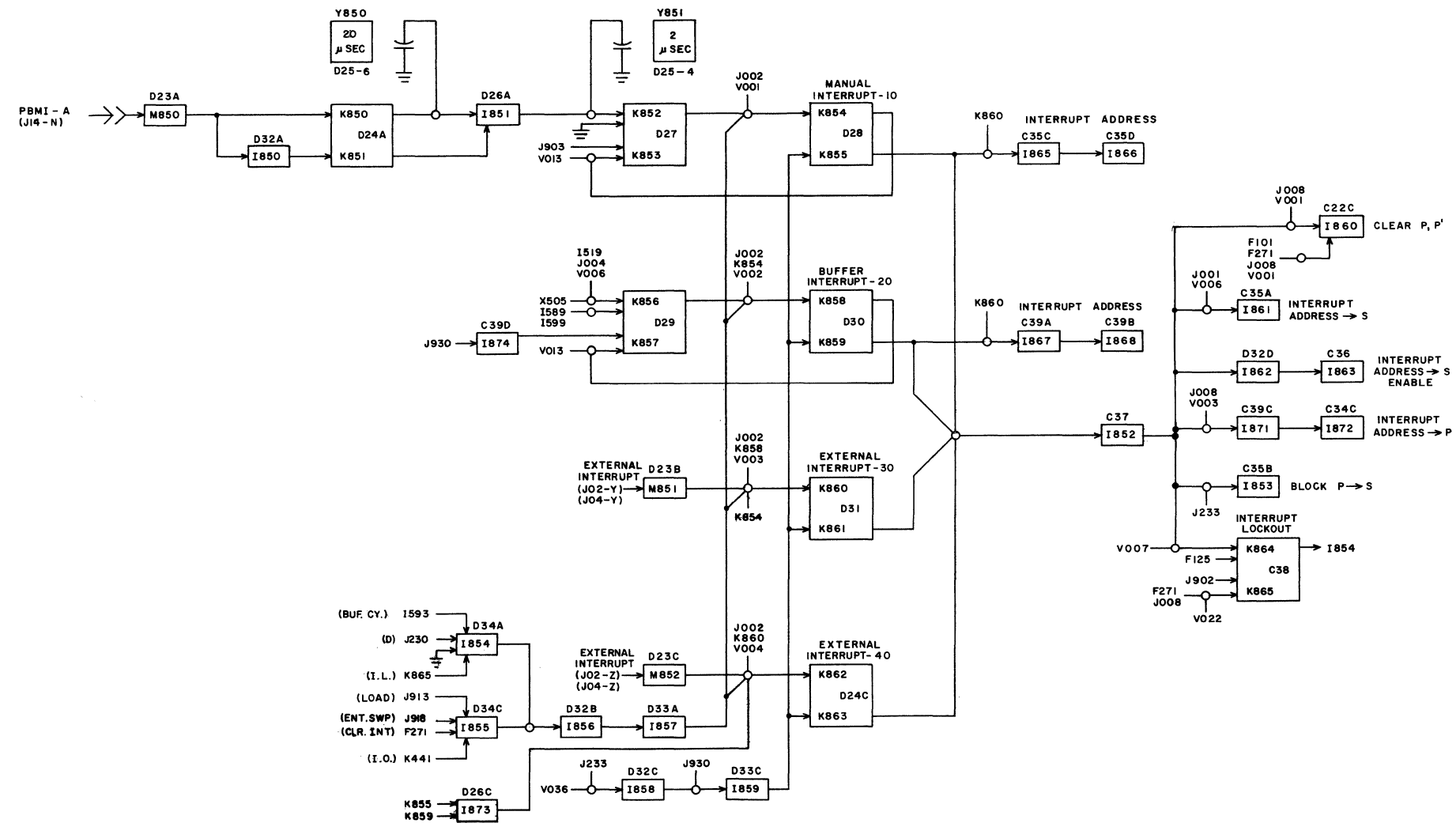


TAG REGISTERS

APPROVED: <i>[Signature]</i> CHECKED: J. H. NIPP DRAWN: N. K. BECK DESIGNED:	REFERENCE DRAWINGS _____ _____ _____		 CONTROL DATA CORPORATION I D P DIVISION PROJECT OR PRODUCT 8092 TELEPROGRAMMER DRAWING NUMBER 360433 SHEET PAGE 15
	COMPONENTS (UNLESS OTHERWISE INDICATED)		
	RESISTORS	TOLERANCE VALUE SIZE	
	CAPACITORS	TOLERANCE VALUE SIZE	
	TITLE LOGIC DIAGRAM, REGISTER - TAG 1, 2, & 3		



REV. AUTH. DATE		REV. AUTH. DATE		REV. AUTH. DATE		REV. AUTH. DATE		REV. AUTH. DATE		REV. AUTH. DATE		REV. AUTH. DATE		REV. AUTH. DATE	
1	2/2/64	2	2/2/64	3	2/2/64	4	2/2/64	5	2/2/64	6	2/2/64	7	2/2/64	8	2/2/64
APPROVED: W. B. Mc...		CHECKED: J. H. NIPP...		DRAWN: N. K. BECK...		DESIGNED: ...		REFERENCE DRAWINGS		COMPONENTS (UNLESS OTHERWISE INDICATED)		RESISTORS		CAPACITORS	
TITLE		LOGIC DIAGRAM,		INPUT/OUTPUT CONTROL		CONTROL DATA CORPORATION		I D P DIVISION		PROJECT OR PRODUCT		8092 TELEPROGRAMMER		DRAWING NUMBER	
360425		REV		E		PAGE		2 OF 2		PAGE		16			

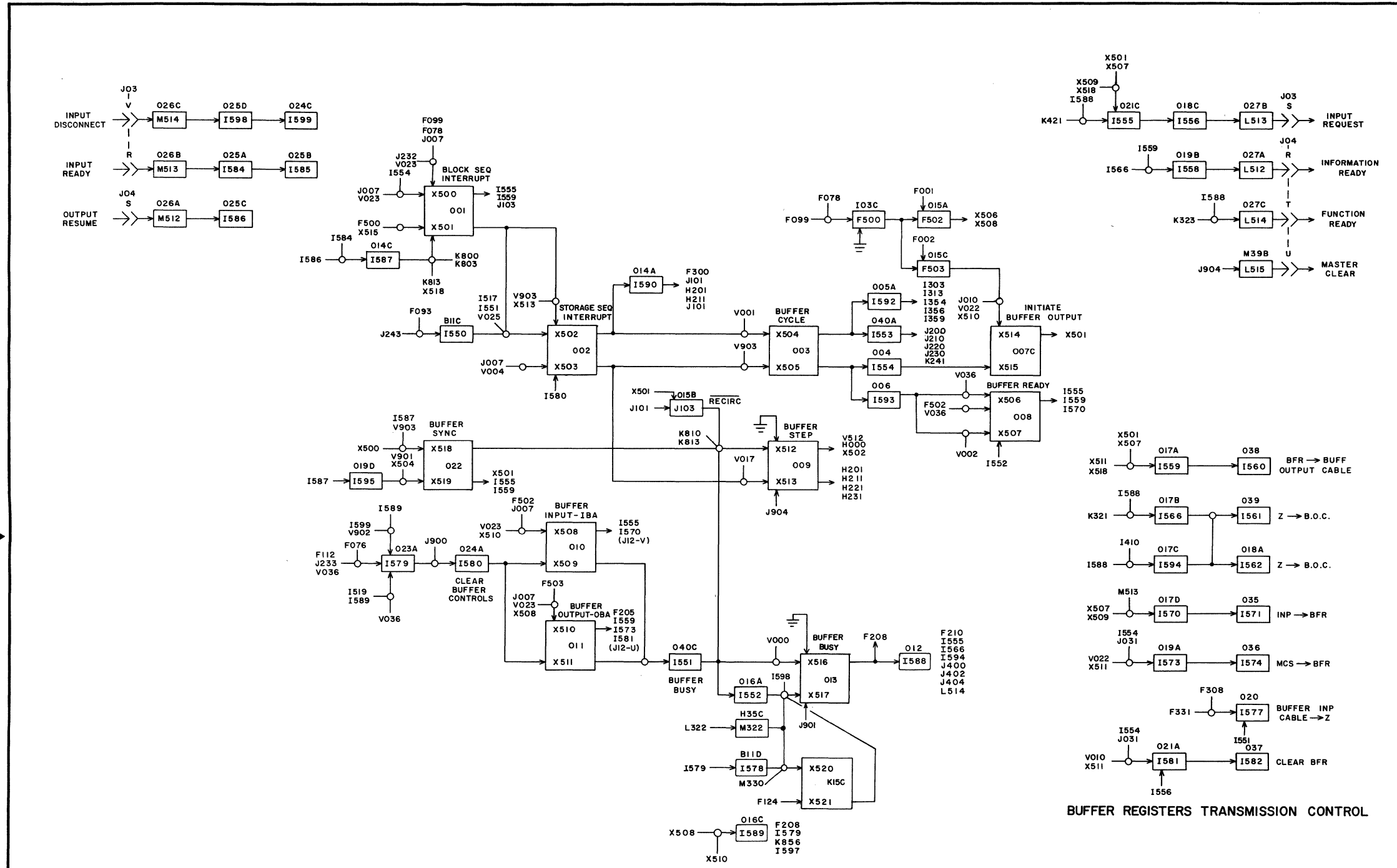


REV		DATE		BY		CHK		APP	
E	2/28/64								
D	2/24/64								
C	1/31/64								
B	1/31/64								
A	1/31/64								

APPROVED	W. B. MOE	2/24/64
CHECKED	J. H. NIPP	2/24/64
DRAWN	K. K. BECK	1/31/64
DESIGNED		

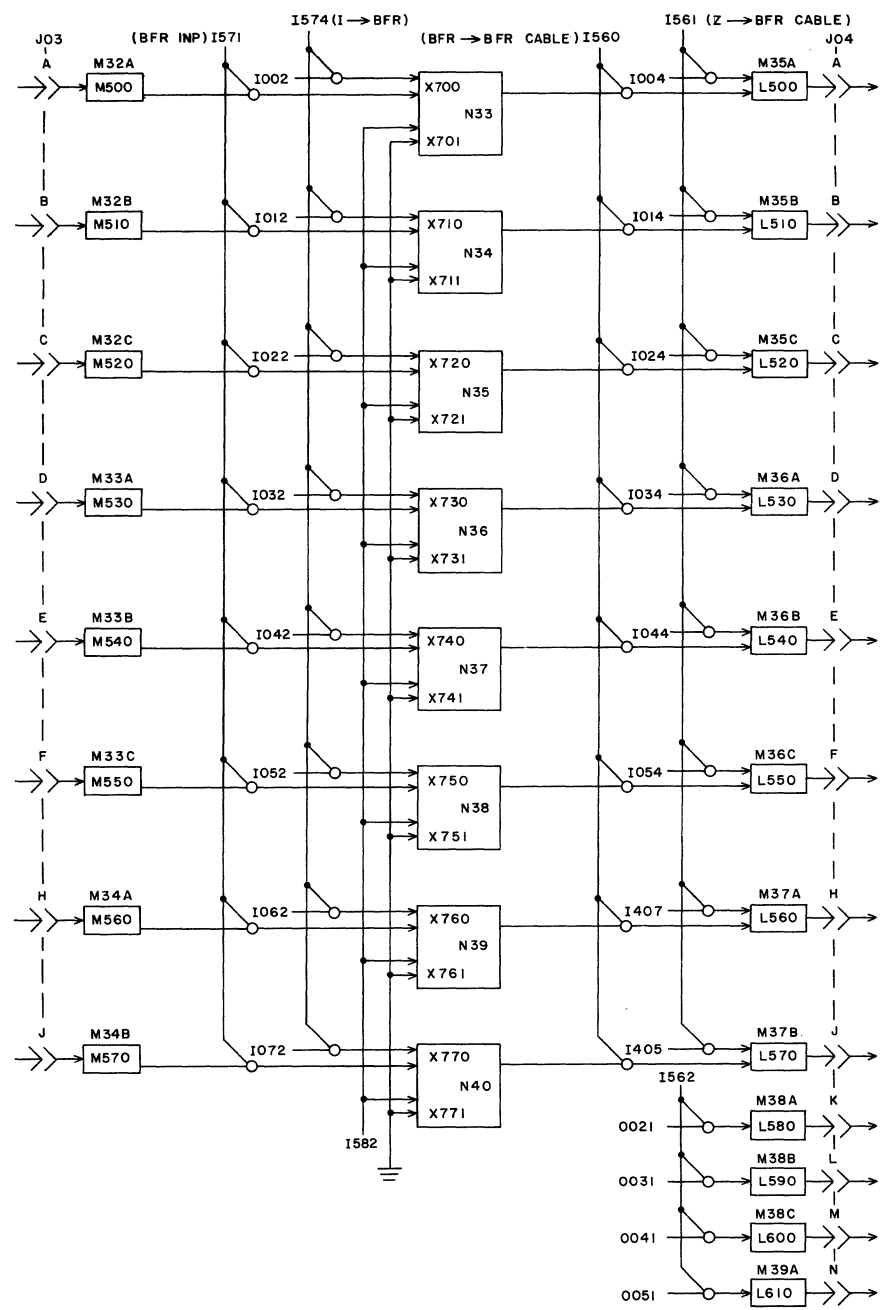
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COMPONENTS (UNLESS OTHERWISE INDICATED)		
RESISTORS	TOLERANCE	VALUE SIZE
CAPACITORS		
TITLE		
LOGIC DIAGRAM INTERRUPT		

CONTROL DATA CORPORATION	
I D P DIVISION	
PROJECT OR PRODUCT	
8092 TELEPROGRAMMER	
DRAWING NUMBER	REV
360434	E
SHT	PAGE
	17

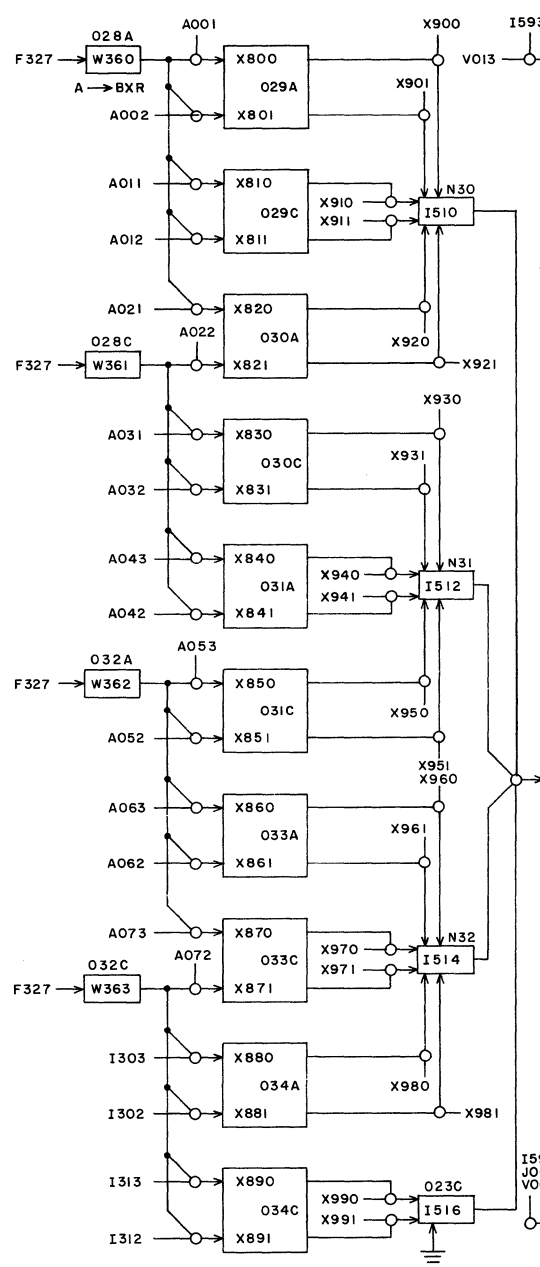


BUFFER REGISTERS TRANSMISSION CONTROL

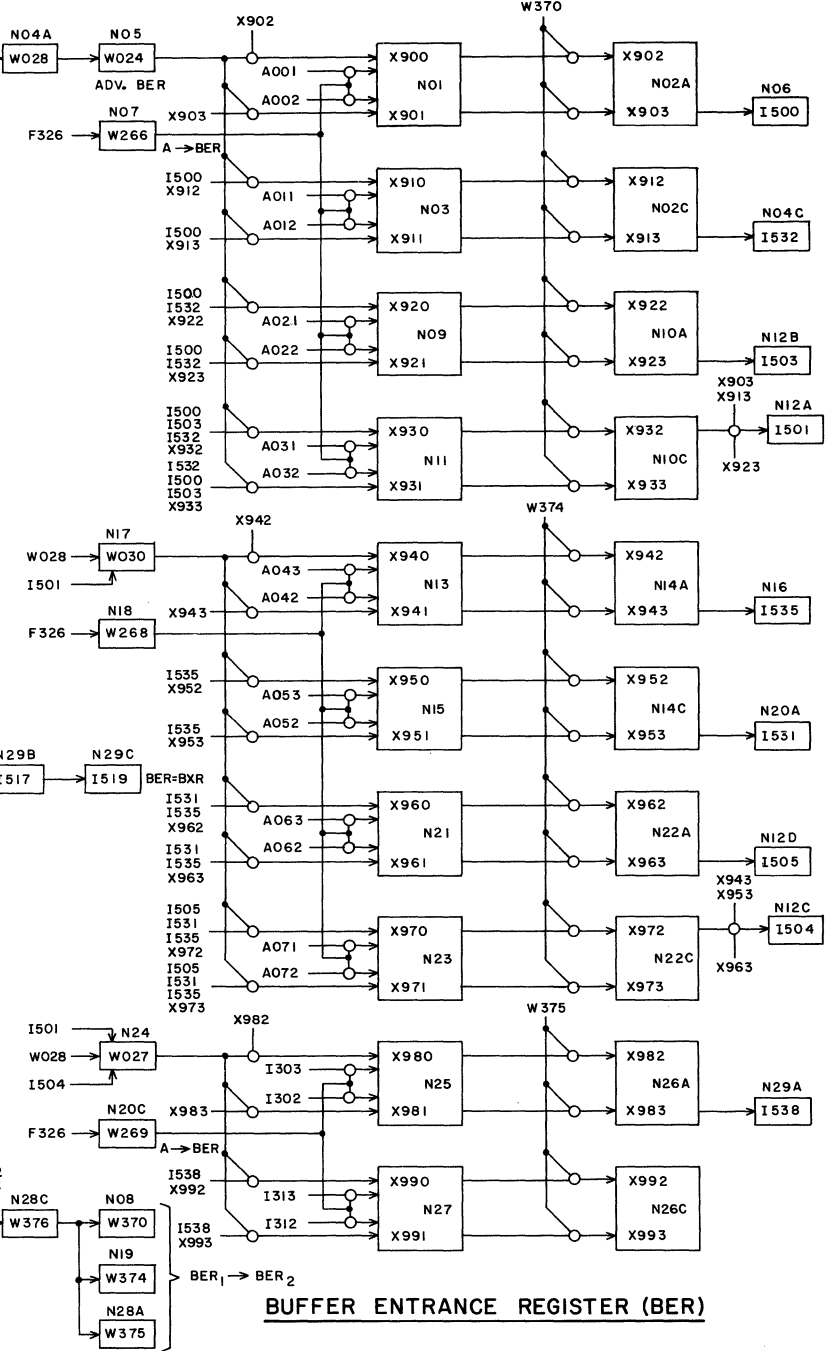
APPROVED: W. B. JOE		2/25/64		DRAWN: J. H. NIPP		2/25/64		CHECKED: N. K. BECK		2/12/64	
DESIGNED: J. H. NIPP		2/25/64		DRAWN: N. K. BECK		2/12/64		CHECKED: N. K. BECK		2/12/64	
REVISIONS		DATE		BY		REASON		APPROVED		DATE	
H	2/25/64	W.B.J.	2/25/64	W.B.J.	W.B.J.	W.B.J.	W.B.J.	W.B.J.	W.B.J.	W.B.J.	W.B.J.
G	2/25/64	J.H.N.	2/25/64	J.H.N.	J.H.N.	J.H.N.	J.H.N.	J.H.N.	J.H.N.	J.H.N.	J.H.N.
F	2/25/64	K.H.	2/25/64	K.H.	K.H.	K.H.	K.H.	K.H.	K.H.	K.H.	K.H.
E	2/25/64	P.G.	2/25/64	P.G.	P.G.	P.G.	P.G.	P.G.	P.G.	P.G.	P.G.
D	2/25/64	M.C.	2/25/64	M.C.	M.C.	M.C.	M.C.	M.C.	M.C.	M.C.	M.C.
C	2/25/64	A.H.	2/25/64	A.H.	A.H.	A.H.	A.H.	A.H.	A.H.	A.H.	A.H.
B	2/25/64	H.S.	2/25/64	H.S.	H.S.	H.S.	H.S.	H.S.	H.S.	H.S.	H.S.
A	2/25/64	T.B.	2/25/64	T.B.	T.B.	T.B.	T.B.	T.B.	T.B.	T.B.	T.B.
TITLE		LOGIC DIAGRAM		BUFFER CONTROLS		REFERENCE DRAWINGS		COMPONENTS (UNLESS OTHERWISE INDICATED)		RESISTORS	
DRAWING NUMBER		36044700		REV		H		PROJECT OR PRODUCT		8092 TELEPROGRAMMER	
PAGE		18		CONTROL DATA CORPORATION		I D P DIVISION		DRAWING NUMBER		36044700	
REV		H		PROJECT OR PRODUCT		8092 TELEPROGRAMMER		DRAWING NUMBER		36044700	
PAGE		18		CONTROL DATA CORPORATION		I D P DIVISION		DRAWING NUMBER		36044700	



BUFFER DATA REGISTER (BFR)

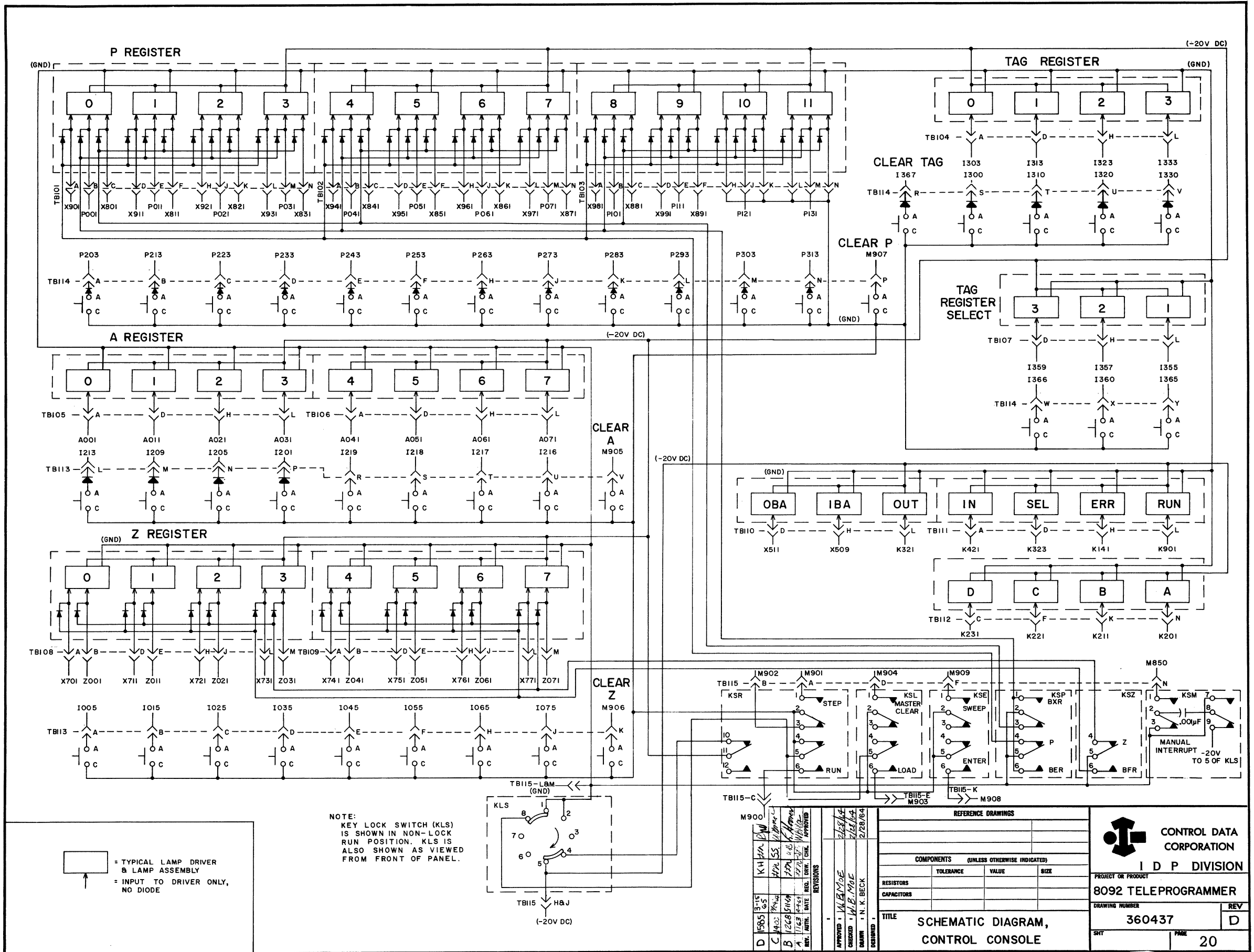




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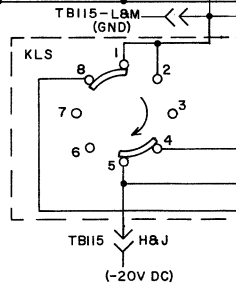
BUFFER ENTRANCE REGISTER (BER)

1585-15 REV. AUTH. DATE 1585-15 1/30/64 APPROVED: W.B. MOE CHECKED: J.H. NIPP DRAWN: N.K. BECK DESIGNED:	REFERENCE DRAWINGS		
	COMPONENTS (UNLESS OTHERWISE INDICATED)		
	RESISTORS	TOLERANCE	VALUE
	CAPACITORS	TOLERANCE	VALUE
TITLE			CONTROL DATA CORPORATION I D P DIVISION PROJECT OR PRODUCT 8092 TELEPROGRAMMER DRAWING NUMBER 360432 REV A
LOGIC DIAGRAM REGISTERS- BFR, BXR, BER			SHT PAGE 19

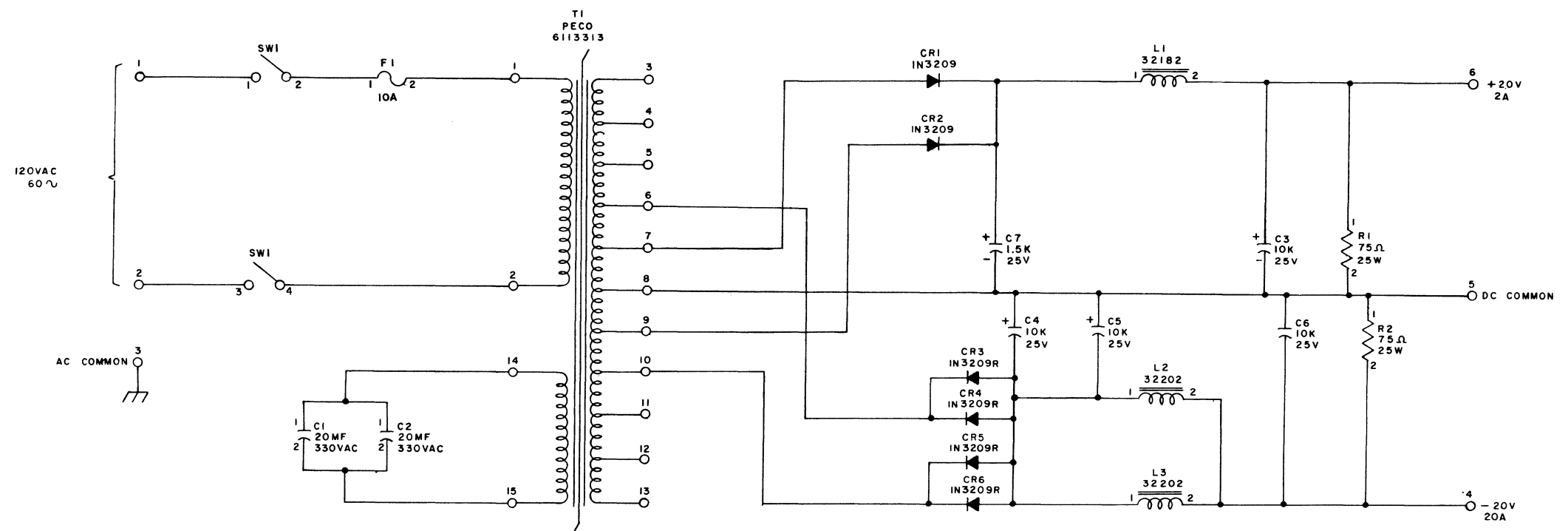


 = TYPICAL LAMP DRIVER & LAMP ASSEMBLY
 = INPUT TO DRIVER ONLY, NO DIODE

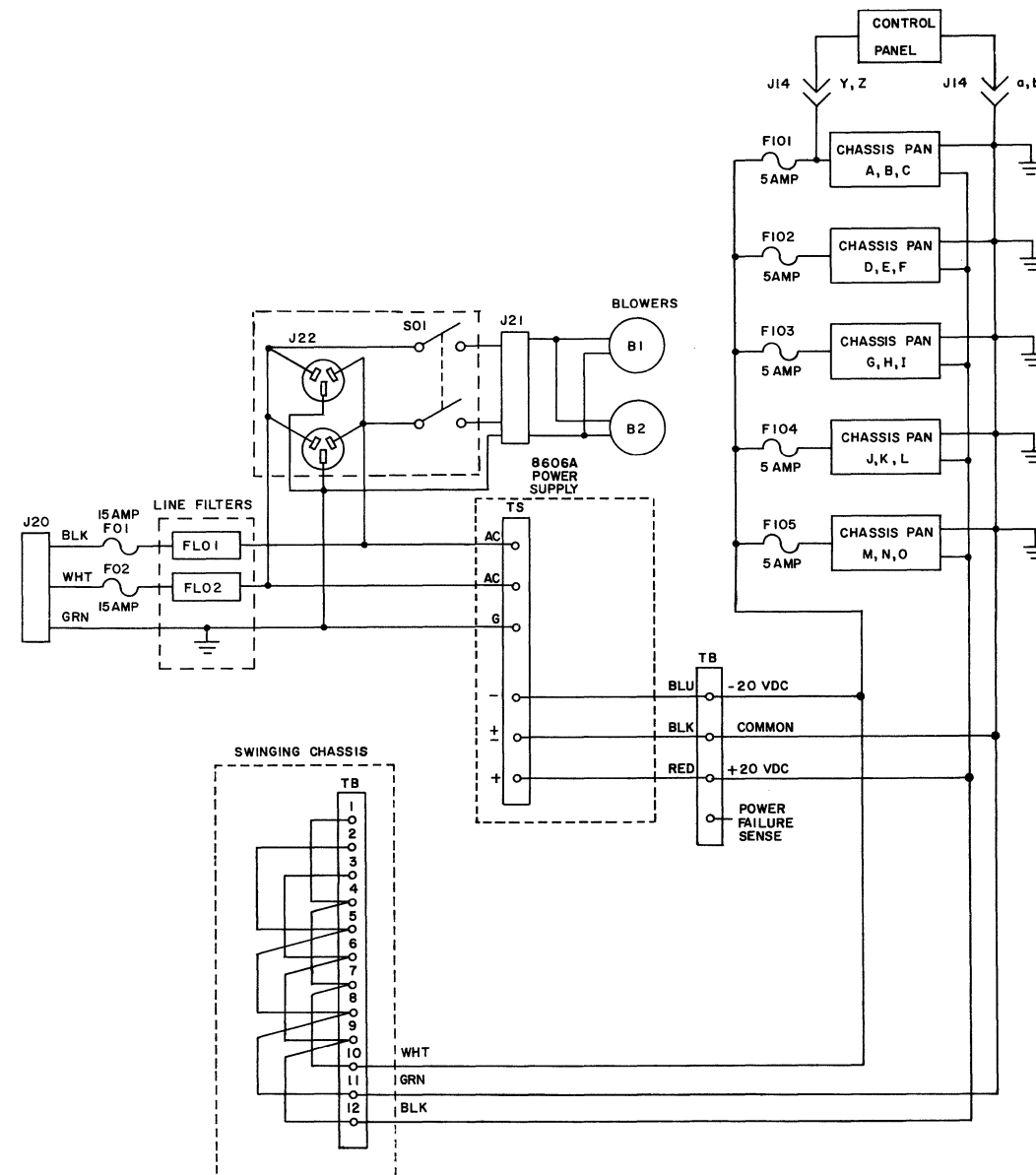
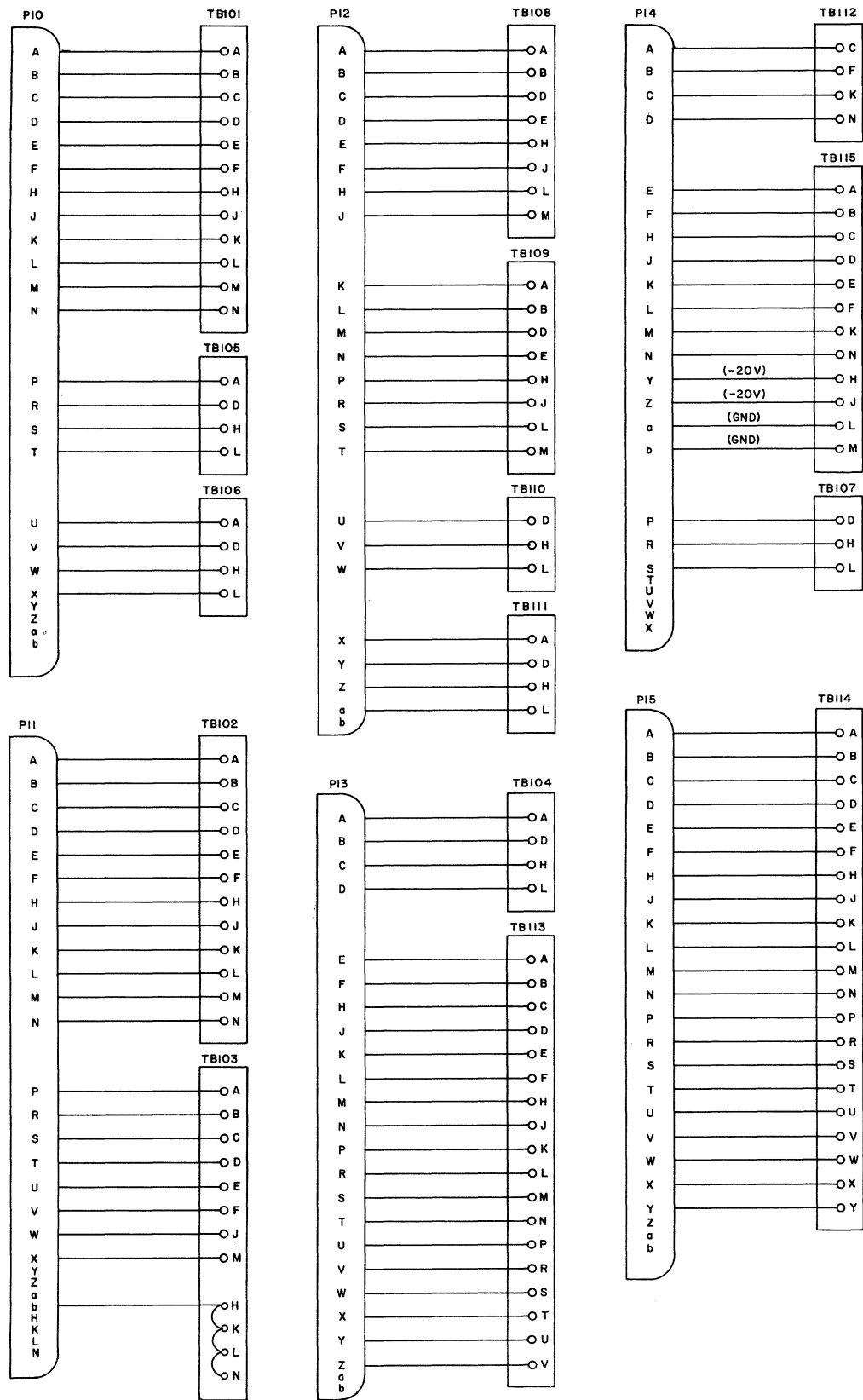
NOTE:
 KEY LOCK SWITCH (KLS)
 IS SHOWN IN NON-LOCK
 RUN POSITION. KLS IS
 ALSO SHOWN AS VIEWED
 FROM FRONT OF PANEL.




REVISIONS			
D	1585	6/5	K.H. FIN. J.W.
C	1423	7/14/64	H.P. SS. J.W.
B	1268	5/14/64	J.P. J.W.
A	1168	4/14/64	J.P. J.W.
REV. DATE: 11/21/64			
DRAWN: I. N. K. BECK			
CHECKED: W. E. MOE			
APPROVED: W. E. MOE			
DATE: 2/28/64			
DESIGNED: I. N. K. BECK			
REFERENCE DRAWINGS			
COMPONENTS (UNLESS OTHERWISE INDICATED)			
RESISTORS	TOLERANCE	VALUE	SIZE
CAPACITORS			
TITLE			
SCHEMATIC DIAGRAM, CONTROL CONSOLE			
PROJECT OR PRODUCT		CONTROL DATA CORPORATION	
DRAWING NUMBER		I D P DIVISION	
8092 TELEPROGRAMMER		REV	
360437		D	
SHT	PAGE		20



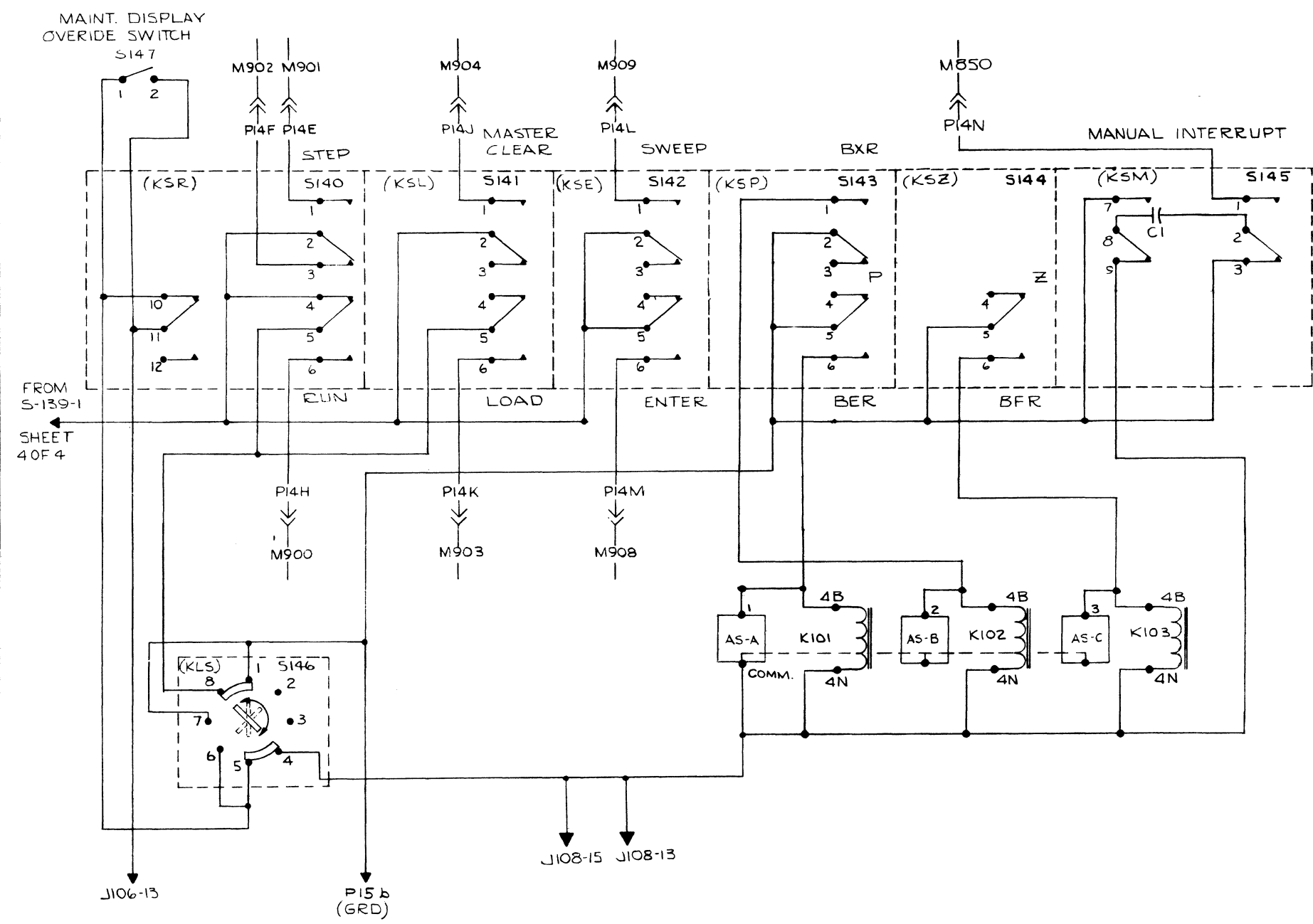
REF. DATE DESIGNED APPROVED CHECKED DRAWN DISTRIBUTED	REFERENCE DRAWINGS		
	COMPONENTS (UNLESS OTHERWISE INDICATED)		
	TOLERANCE	VALUE	SIZE
	RESISTORS		
TITLE			CONTROL DATA CORPORATION
SCHEMATIC, POWER SUPPLY-			I D P DIVISION
MODEL 8606-A			PROJECT OR PRODUCT
DRAWING NUMBER		REV	
364071			
PAGE			
21			



A 1985 REV. AUTH. DATE K.H. 1/10/64 REC. DATE 1/10/64 CHC. APPROVED 1/10/64	REVISIONS 1/10/64 1/10/64	APPROVED 1/10/64 3/4/64 N.K. BECK DRAWN DESIGNED	REFERENCE DRAWINGS		
			COMPONENTS (UNLESS OTHERWISE INDICATED)		
RESISTORS			TOLERANCE	VALUE	SIZE
CAPACITORS					
TITLE			DRAWING NUMBER		
CABLING & AC-DC DIST			360441		
			REV. A		
			PAGE 22		


CONTROL DATA CORPORATION
I D P DIVISION
 PROJECT OR PRODUCT
8092 TELEPROGRAMMER
 DRAWING NUMBER
360441
 REV. A
 PAGE 22

REVISIONS							
REV.	ECO.	ZONE	DESCRIPTION	DRFT.	DATE	CHK'D	APPD.
A			RELEASED		11-20-64		WAM
B	8230		REVISED PER ECO	RAH	4-5-65		FES

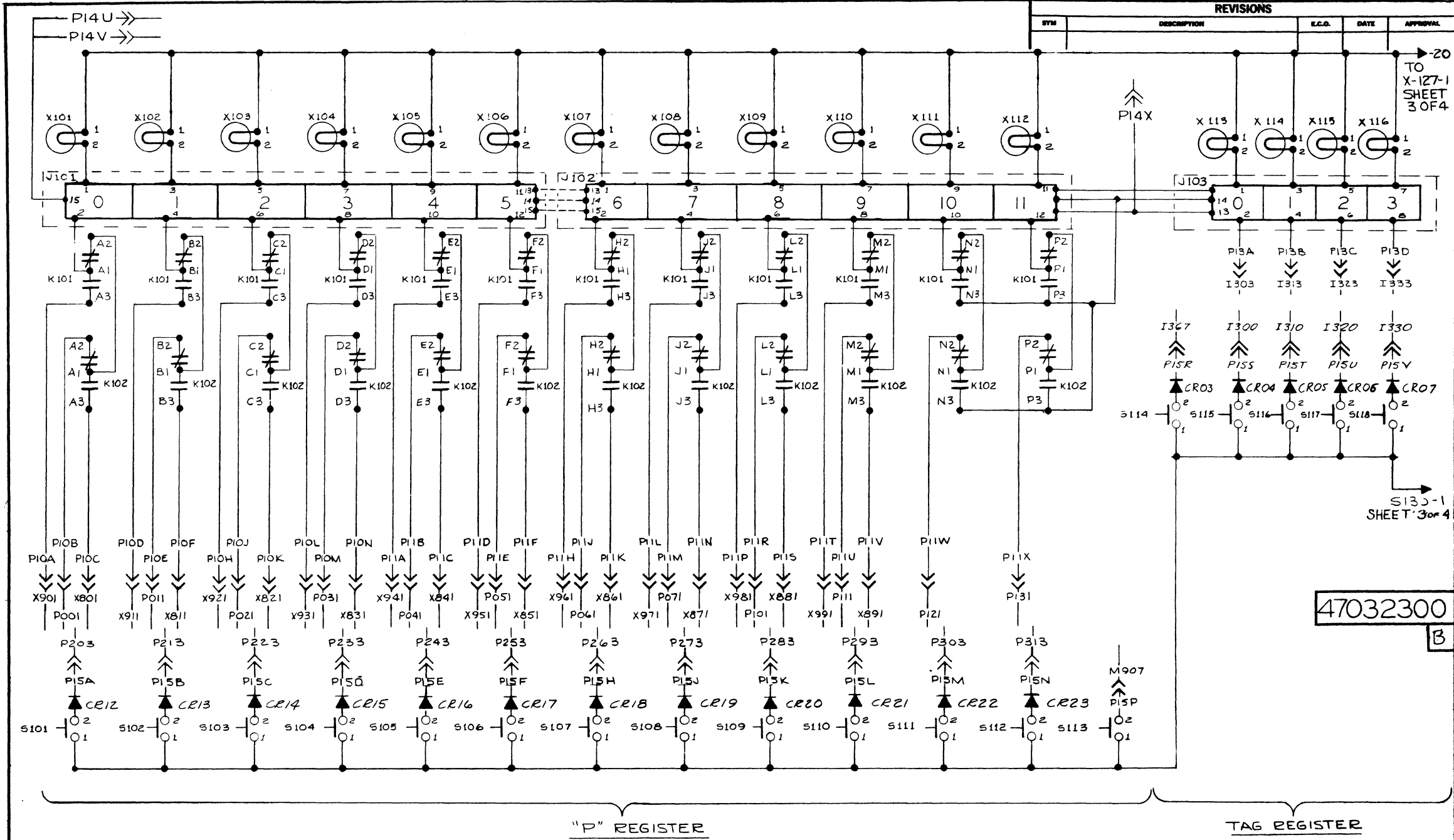


2. DOTTED LINES SHOW CONNECTIONS WITHIN A CONNECTOR OR COMPONENT.

1. KEY LOCK SWITCH KLS IS SHOWN IN NON-LOCK RUN POSITION. KLS IS ALSO SHOWN AS VIEWED FROM FRONT OF PANEL.

NOTES:

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS: DECIMALS: ANGLES:		CONTROL DATA		TITLE	
DO NOT SCALE DRAWING		CEDAR ENGINEERING DIVISION DIGITAL ENGINEERING DEPARTMENT MINNEAPOLIS, MINNESOTA		SCHEMATIC DIAGRAM 8092 DISPLAY	
MATERIAL	PRODUCT	8092 DISPLAY	SIZE	DRAWING NO.	REV
FINISH	DRAWN	R. Williams 11-13-64	C	47032300	B
	CHECKED	J. J. J. 11-13-64			
	ENGINEER	R. Williams 11-13-64			
	APPROVED				
	SCALE			Page 23	SHEET 1 OF 4



TO X-127-1 SHEET 3 OF 4

S135-1 SHEET 3 OF 4

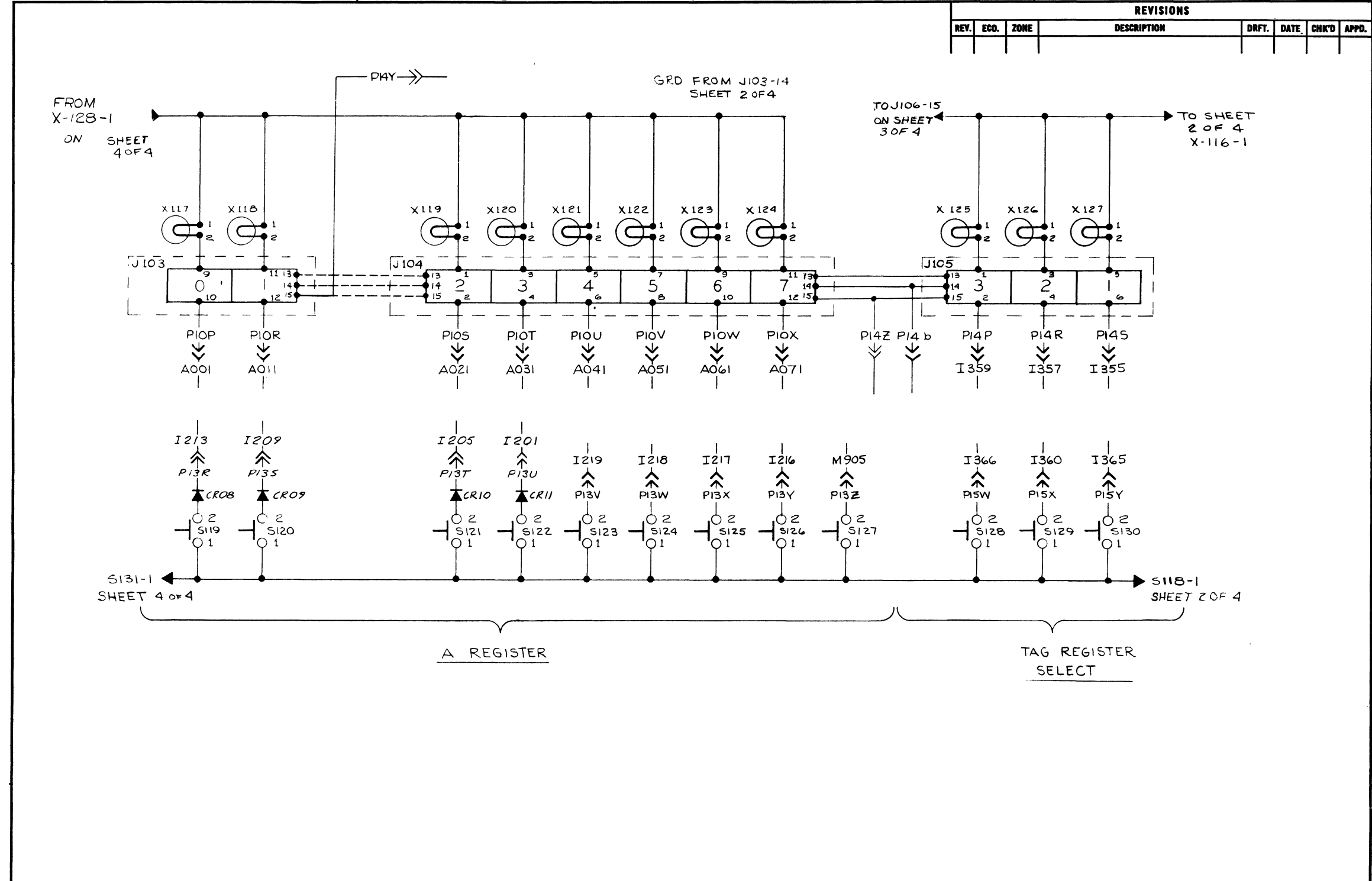
47032300 B

"P" REGISTER

TAG REGISTER

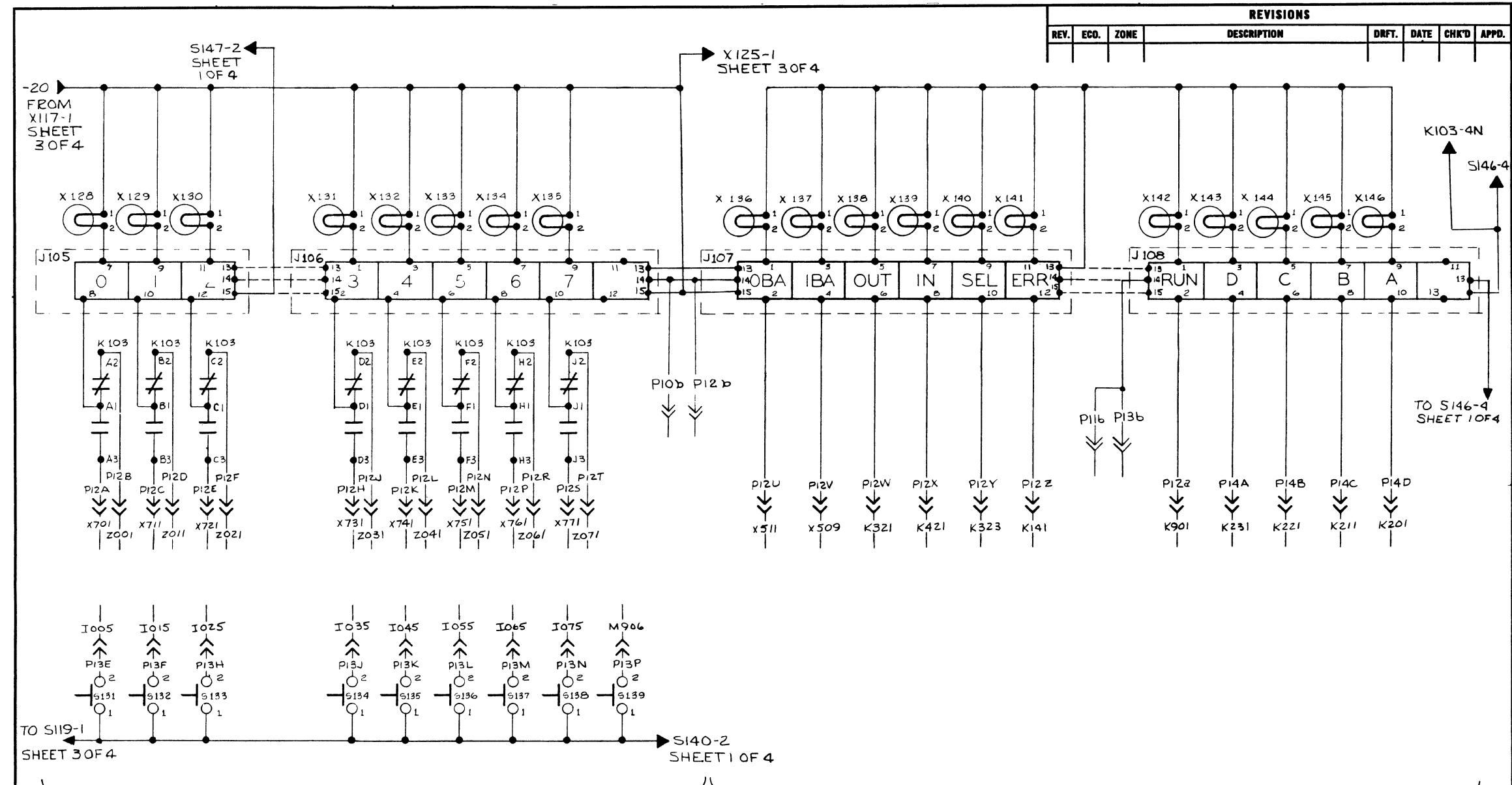
ITEM	REQD.	PART NO.	DESCRIPTION	MATL.	MATL. SPEC.	NEXT ASSY.	USED ON	QTY. RECD.
LIST OF MATERIAL								
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE: FRACTIONS: ±1/64 DECIMALS: (0.00)±0.01 (0.00)±0.005 BREAK ALL EDGES AND SHARP CORNERS DIMENSIONS APPLY AFTER PLATING OR HEAT TREAT. SHARPEN NO LOOSE CORNERS PERMITTED. TIGHT SPACES PERMITTED IF THEY CANNOT BE DETECTED BY NORMAL VISION OR TOUCH. SURFACE FINISH: ✓ ALL INSIDE SURFACES ✓ ALL OUTSIDE SURFACES			DRAWN: _____ CHECKED: _____ ENGR: _____ PDR: _____ FURISH: _____	SCHEMATIC DIAGRAM 8092 DISPLAY		CONTROL DATA CORP CEDAR ENGINEERING DIVISION 8000 WEST 20TH ST. MINNEAPOLIS 16 MINNESOTA		
							Page 24	47032300
							2 OF 4	

REVISIONS							
REV.	ECO.	ZONE	DESCRIPTION	DRFT.	DATE	CHK'D	APPD.



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS: DECIMALS: ANGLES: * * *	CONTROL DATA		TITLE	
	CEDAR ENGINEERING DIVISION DIGITAL ENGINEERING DEPARTMENT MINNEAPOLIS, MINNESOTA		SCHEMATIC DIAGRAM 8092 DISPLAY	
DO NOT SCALE DRAWING	PRODUCT	SIZE	DRAWING NO.	REV
MATERIAL	8092 DISPLAY	C	47032300	B
FINISH	DRAWN	SCALE	Page 25	SHEET 3 OF 4
	CHECKED			
	ENGINEER			
	APPROVED			

REVISIONS						
REV.	ECO.	ZONE	DESCRIPTION	DRFT.	DATE	CHK'D APPD.

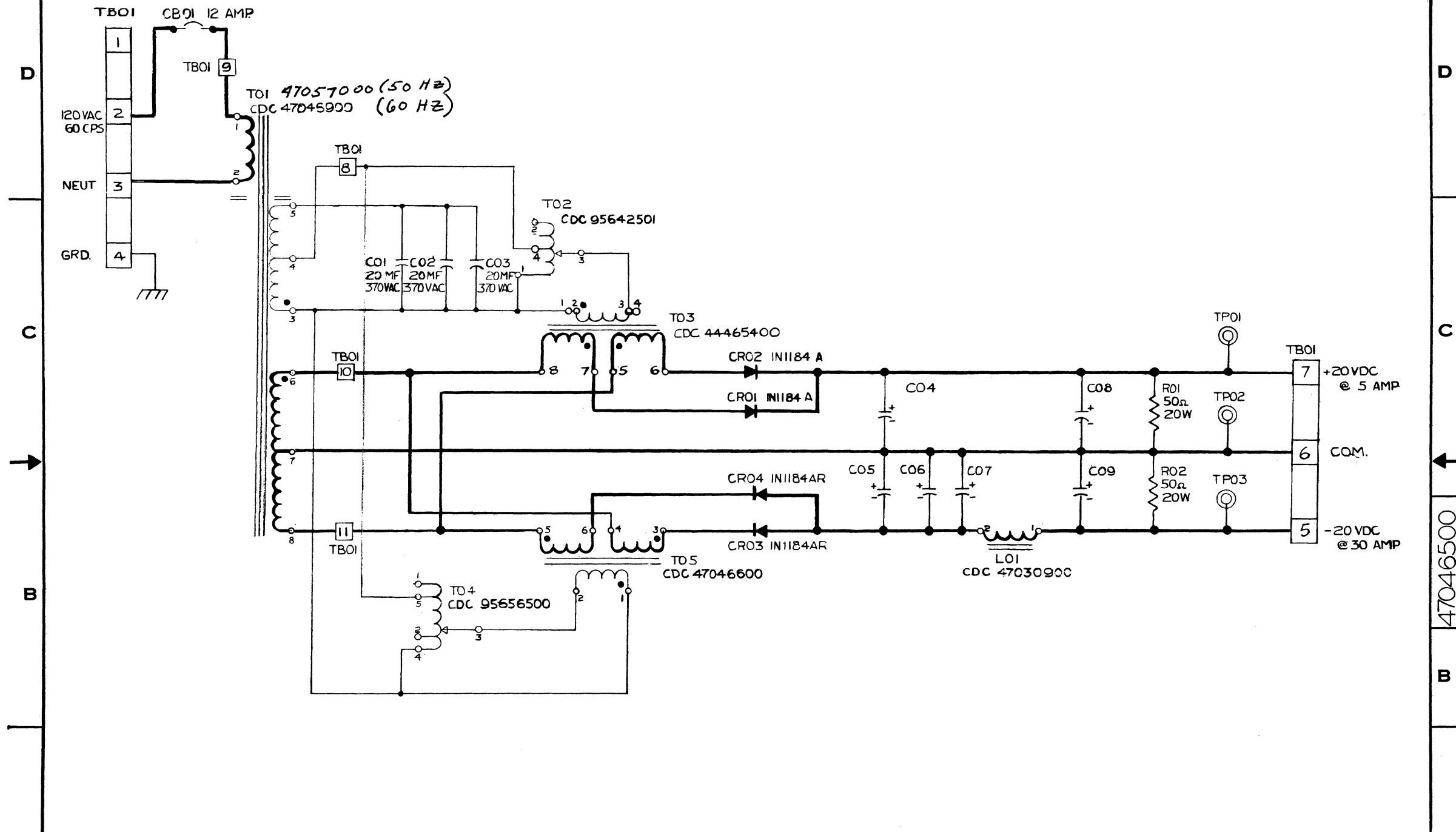


'Z' REGISTER

LEGENDS

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS: DECIMALS: ANGLES: * * *	CONTROL DATA CORPORATION		TITLE SCHEMATIC DIAGRAM, 8092 DISPLAY	
	CEDAR ENGINEERING DIVISION DIGITAL ENGINEERING DEPARTMENT MILWAUKEE, WISCONSIN		PRODUCT 8092 DISPLAY	DRAWING NO. 47032300
DO NOT SCALE DRAWING	DRAWN	CHECKED	ENGINEER	APPROVED
SCALE	SIZE C	DRAWING NO. 47032300		REV B
Page 26			SHEET 4 OF 4	

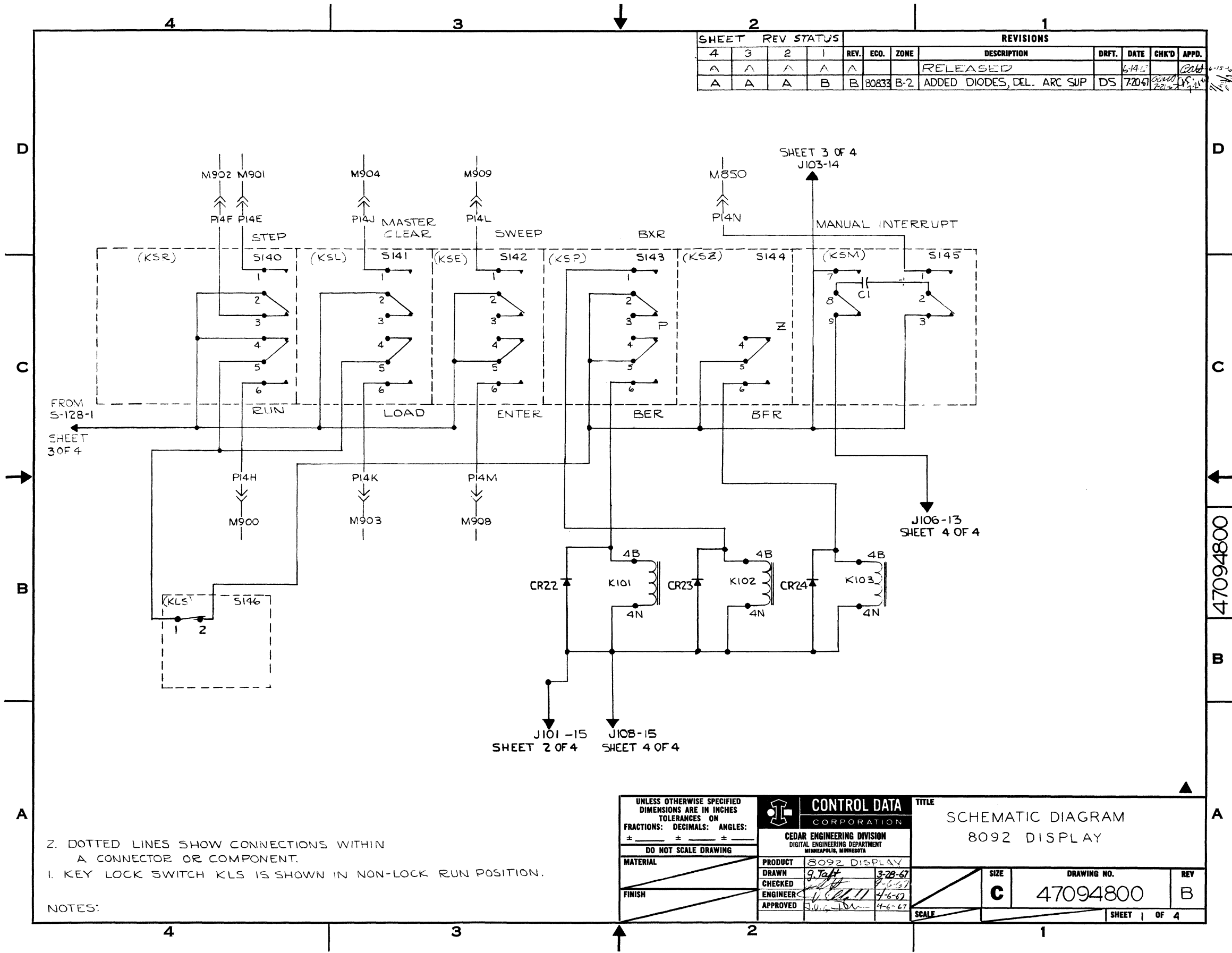
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REV.	ECO.	ZONE	DESCRIPTION	DRFT.	DATE	CHK'D APPR.
A			RELEASED		3-22-64	PPM



NOTE: C04 THROUGH C09 ARE 55,000 MFD @ 25 VDC.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS: DECIMALS: ANGLES: * * *		CONTROL DATA		TITLE SCHEMATIC, POWER SUPPLY FERRORESONANT, 60 CPS + 50 CPS	
DO NOT SCALE DRAWING		CEDAR ENGINEERING DIVISION DIGITAL ENGINEERING DEPARTMENT MINNEAPOLIS, MINNESOTA		DRAWING NO. 47046500	
PRODUCT	TELEPROGRAMMER	SCALE		SIZE	C
DRAWN	D. SCOFIELD 12-3-65				
CHECKED	<i>[Signature]</i> 12-3-65				
ENGINEER	<i>[Signature]</i> 12/3/65				
APPROVED	<i>[Signature]</i> 12/3/65				
Page 27			SHEET 1 OF 1		

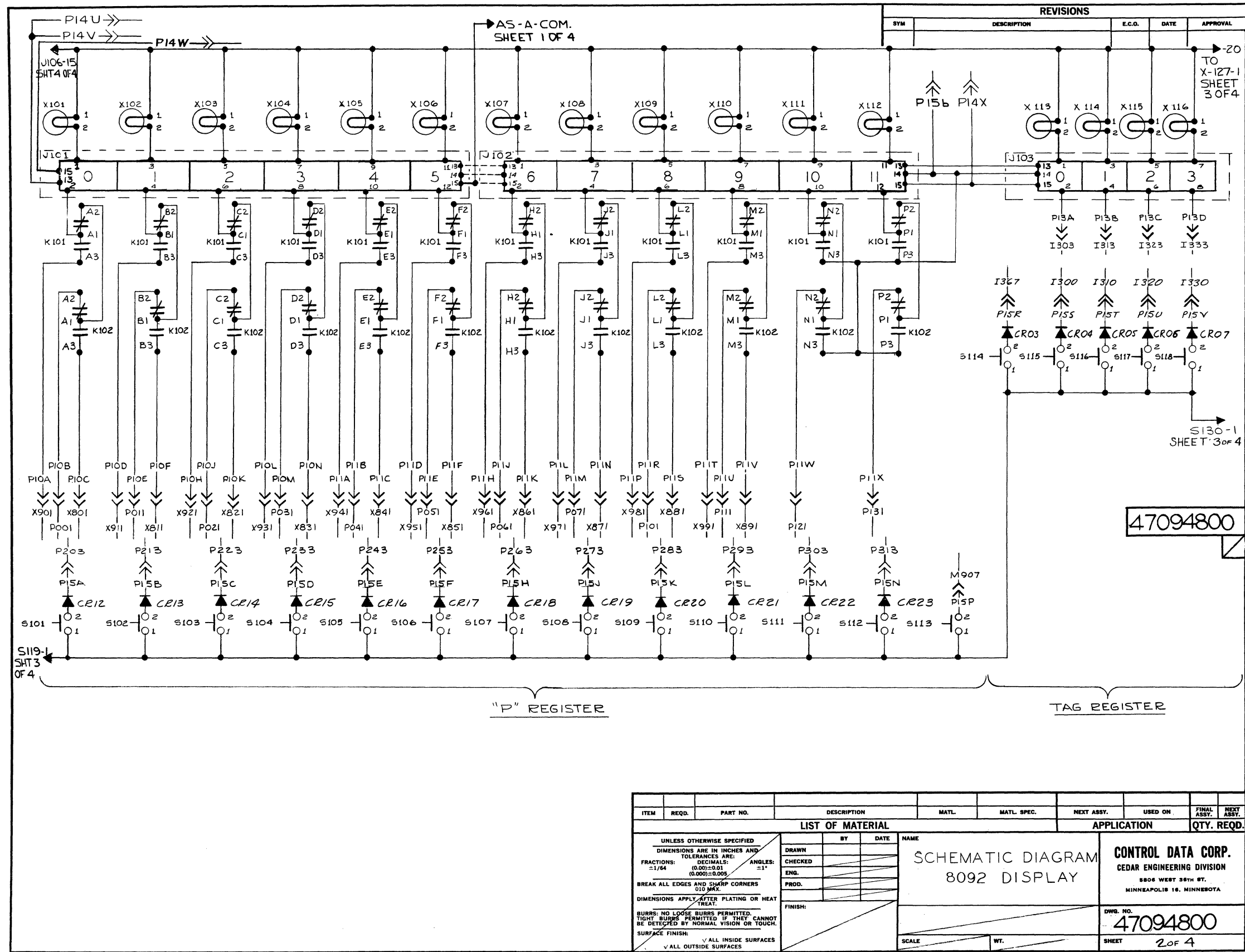
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4	3	2	1	REV.	ECO.	ZONE	DESCRIPTION	DRFT.	DATE	CHK'D	APPD.
A	A	A	A	A			RELEASED		6-14-67		
A	A	A	B	B	80833	B-2	ADDED DIODES, DEL. ARC SUP	DS	7-20-67		



2. DOTTED LINES SHOW CONNECTIONS WITHIN A CONNECTOR OR COMPONENT.
 1. KEY LOCK SWITCH KLS IS SHOWN IN NON-LOCK RUN POSITION.

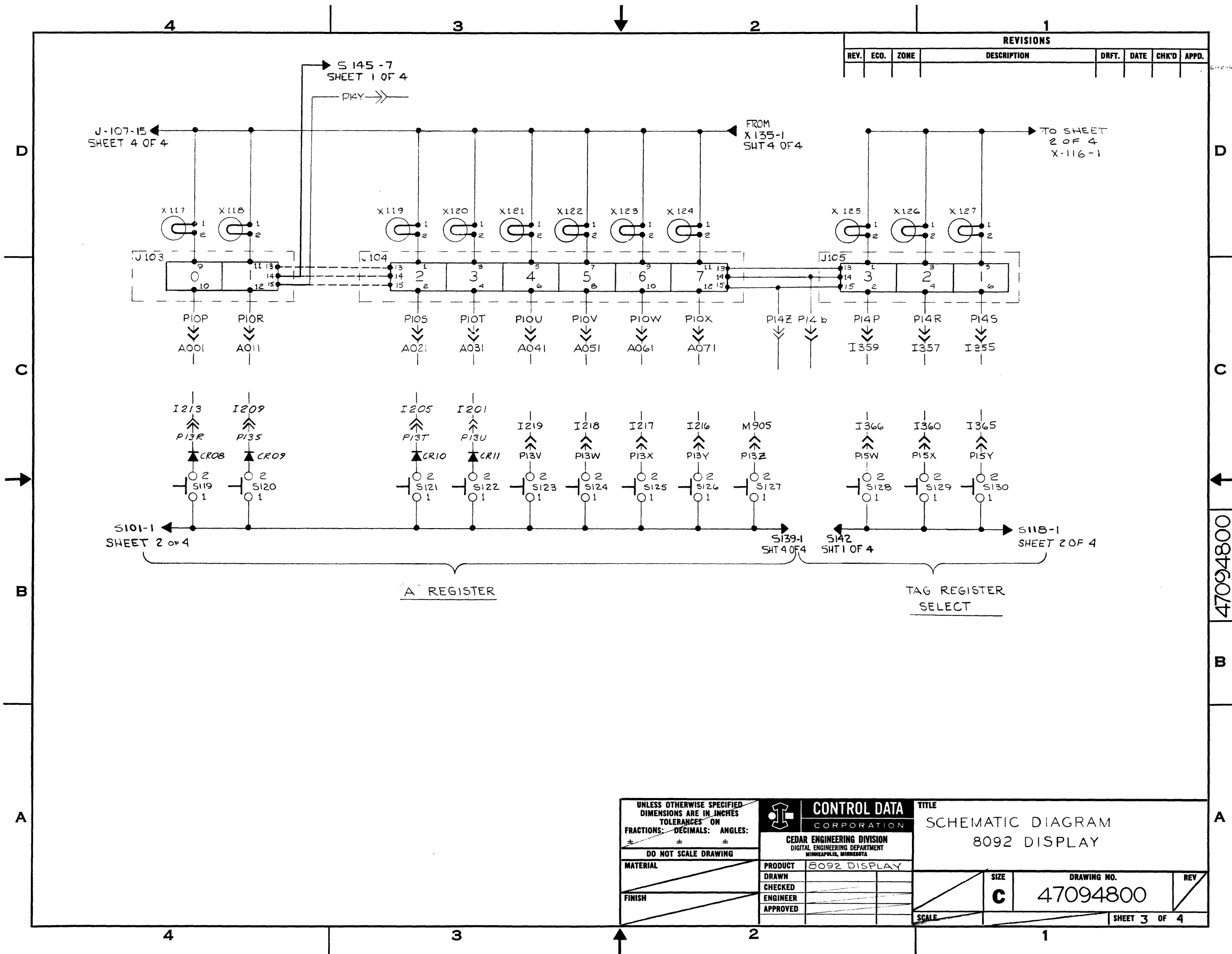
NOTES:

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS: DECIMALS: ANGLES: ± .005 ± .001 ± .001		CONTROL DATA CORPORATION		TITLE	
DO NOT SCALE DRAWING		CEDAR ENGINEERING DIVISION DIGITAL ENGINEERING DEPARTMENT MINNEAPOLIS, MINNESOTA		8092 DISPLAY	
MATERIAL	PRODUCT 8092 DISPLAY	DRAWN G. Toft	3-28-67	SIZE C	DRAWING NO. 47094800
FINISH	CHECKED [Signature]	ENGINEER [Signature]	4-6-67	REV B	
	APPROVED [Signature]		4-6-67	SCALE	SHEET 1 OF 4



SYM	DESCRIPTION	E.C.O.	DATE	APPROVAL

ITEM	REQD.	PART NO.	DESCRIPTION	MATL.	MATL. SPEC.	NEXT ASSY.	USED ON	FINAL ASSY.	NEXT ASSY.	QTY. REQD.
LIST OF MATERIAL										
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE: FRACTIONS: ±1/64 DECIMALS: (0.0005-0.01) ±.0005 ANGLES: ±1° BREAK ALL EDGES AND SHARP CORNERS 0.10 R. DIMENSIONS APPLY AFTER PLATING OR HEAT TREAT. BURRS: NO LOOSE BURRS PERMITTED. TIGHT BURRS PERMITTED IF THEY CANNOT BE DETECTED BY NORMAL VISION OR TOUCH. SURFACE FINISH: ✓ ALL INSIDE SURFACES ✓ ALL OUTSIDE SURFACES										
DRAWN			BY		DATE		NAME			
CHECKED			BY		DATE		SCHEMATIC DIAGRAM			
ENG.			BY		DATE		8092 DISPLAY			
PROD.			BY		DATE		CONTROL DATA CORP.			
FINISH:			BY		DATE		CEDAR ENGINEERING DIVISION			
SCALE			BY		DATE		8806 WEST 38TH ST.			
WT.			BY		DATE		MINNEAPOLIS 16, MINNESOTA			
DWG. NO.							47094800			
SHEET							2 OF 4			




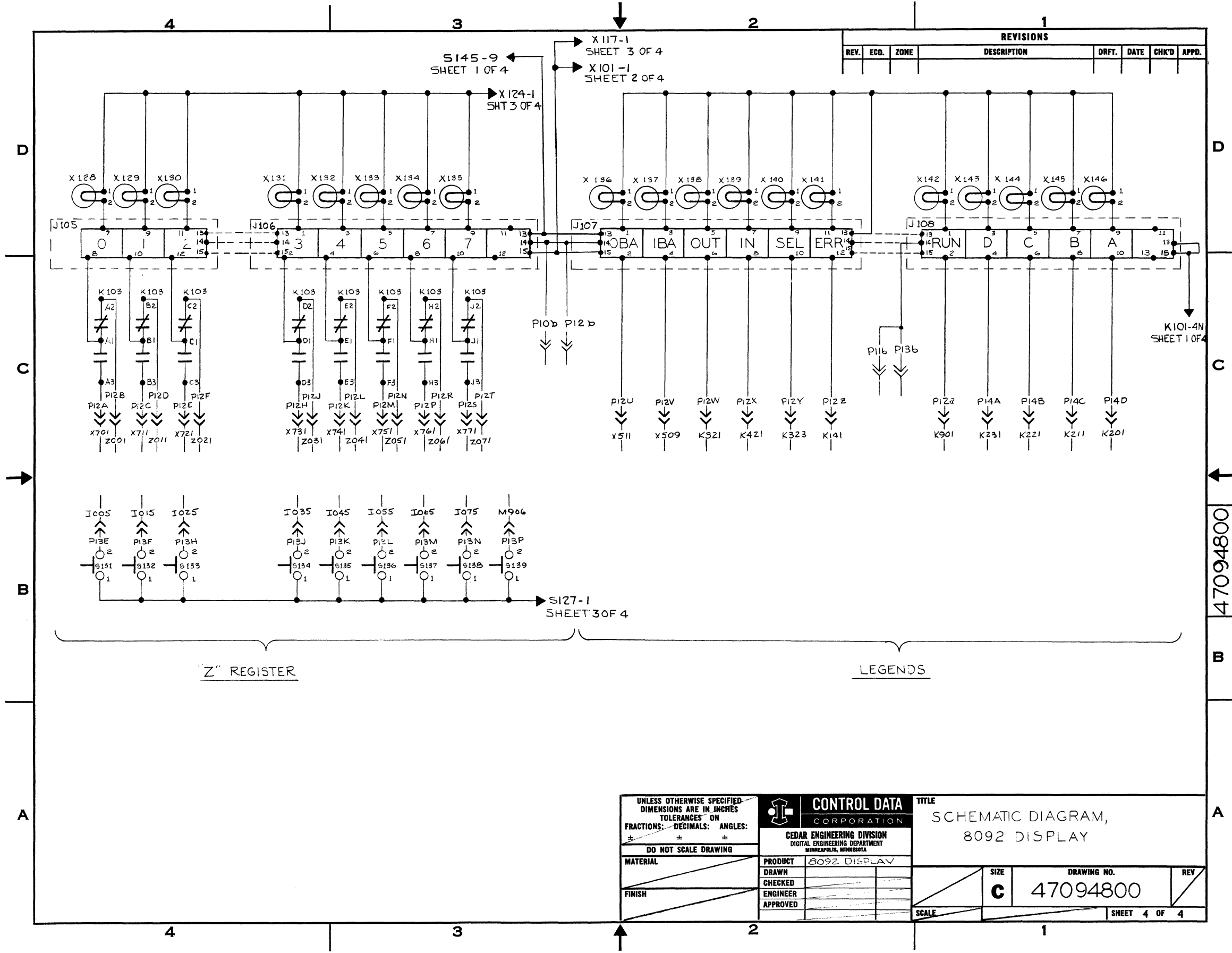
REVISIONS						
REV.	ECO.	ZONE	DESCRIPTION	DRFT.	DATE	CHK'D APPD.

A REGISTER

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UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS: DECIMALS: ANGLES: ± ± ± DO NOT SCALE DRAWING	 CONTROL DATA CORPORATION		TITLE SCHEMATIC DIAGRAM 8092 DISPLAY	
	CEDAR ENGINEERING DIVISION DIGITAL ENGINEERING DEPARTMENT MINNEAPOLIS, MINNESOTA		DRAWING NO. 47094800	
	MATERIAL FINISH	PRODUCT 8092 DISPLAY	SIZE C	REV
	SCALE		SHEET 3 OF 4	



REVISIONS						
REV.	ECD.	ZONE	DESCRIPTION	DRFT.	DATE	CHK'D APPD.

S145-9 SHEET 1 OF 4
 X117-1 SHEET 3 OF 4
 X101-1 SHEET 2 OF 4
 X124-1 SHT 3 OF 4

K101-4N SHEET 1 OF 4

S127-1 SHEET 3 OF 4

"Z" REGISTER

LEGENDS

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UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS: DECIMALS: ANGLES:		 CONTROL DATA CORPORATION CEDAR ENGINEERING DIVISION DIGITAL ENGINEERING DEPARTMENT MINNEAPOLIS, MINNESOTA	TITLE SCHEMATIC DIAGRAM, 8092 DISPLAY	
DO NOT SCALE DRAWING			PRODUCT 8092 DISPLAY	SIZE C
MATERIAL	FINISH	DRAWN	CHECKED	ENGINEER
		APPROVED	SCALE	
			SHEET 4 OF 4	

COMMENT SHEET

MANUAL TITLE 8090 TELEPROGRAMMER Equipment Diagrams

PUBLICATION NO. 36810900 REVISION _____

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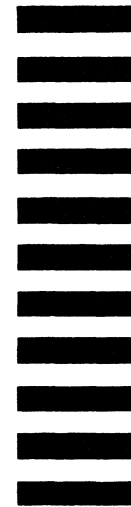
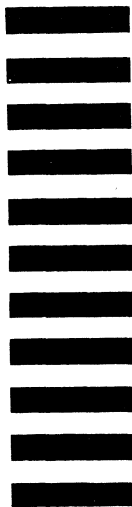
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