Equipment Diagrams

CONTROL DATA 8092
TELEPROGRAMMER

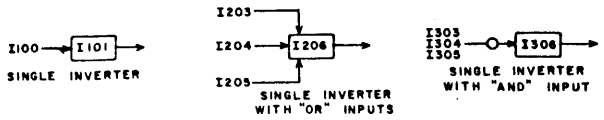
IDP 368 109 01

RECORD OF REVISIONS

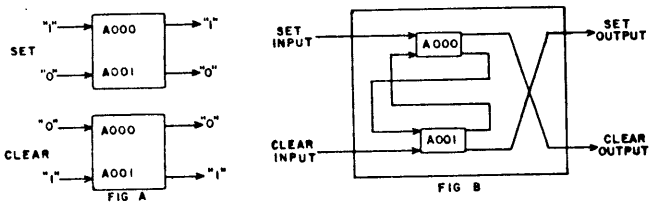
REVISION NUMBER	NOTES
368 109 01	(4-15-65) Includes ECO's 1163, 1198, 1268, 1334, 1354, 1402, 1403, 1411, 1431, 1470, 1505, and 1585.
368 109 00B	(8-18-66) INCLUDES ECO NUMBERS 2041 AND 2085. ENTERED 6 FEB 67 BKP

TABLE OF CONTENTS

SINGLE INVERTER - A single inverter inverts input signals so that a "1" input results in a "0" output and a "0" input results in a "1" output. Inputs to symbols are identified by arrowheads.

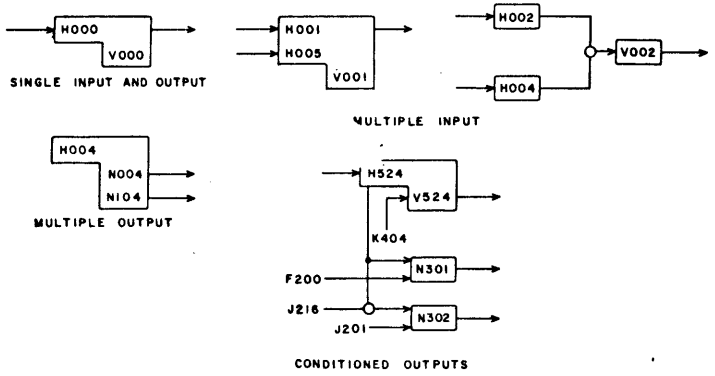


FLIP FLOP (FF) - The flip flop is a storage device with two stable states, designated "1" or Set, and "0" or Clear. It is composed of two inter-connected inverters; the logical symbol (figure A) is a square formed by the combination of the two single inverter symbols. By convention, "1" (or Set) inputs and outputs are shown with the upper part of the symbol and "0" (or Clear) inputs and outputs are shown with the lower part of the symbol. This diagrammatic convention simplifies the actual interconnection of the two inverters as shown in figure B.

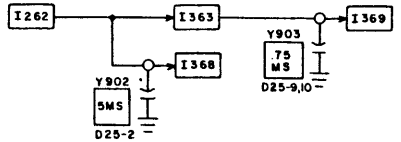


CONTROL DELAY - A control delay consists of an H--- part, which receives the input, and a V--- or N--- part, which provides the output. The output is a clocked pulse which is delayed with respect to the input pulse by one phase time of the clock (0.2 microsecond). Conventions which apply to control delays are:

1. Clock pulse inputs to control delays are not shown on the diagrams and must be obtained from the equation file.
2. The logical number designation indicates the clock phase of the output signal. An odd number indicates an odd clock phase; an even number indicates an even clock phase.
3. The time scales shown on all sequence diagrams are in 0.2 microsecond (1 clock phase time) intervals.



CAPACITIVE DELAY - A capacitive delay is used in an AND configuration to delay the "1" input to a logic element. The capacitor is shown with the curved (negative) plate adjoining the AND symbol. A small box shows the equation file symbol assigned to that delay, the duration of the delay, and the coordinate jack and pin number where physical connection to the capacitor(s) is made.



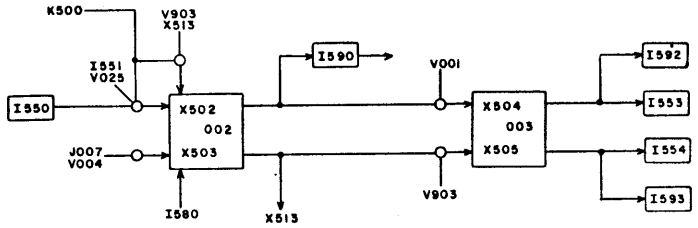
SYMBOLICAL REPRESENTATION OF TYPICAL EQUATIONS

X504 = V001 X503
31 003A: I554: I593:

X505 = V903 X502
31 003C; I592: I553

X502 = V903 X513 X500 + I550 I551 V025 X500
32 002A: X513: X505:

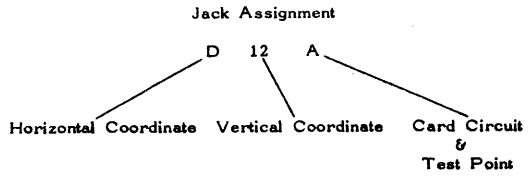
X503 = I580 + J007 V004
32 002C: I590: X504



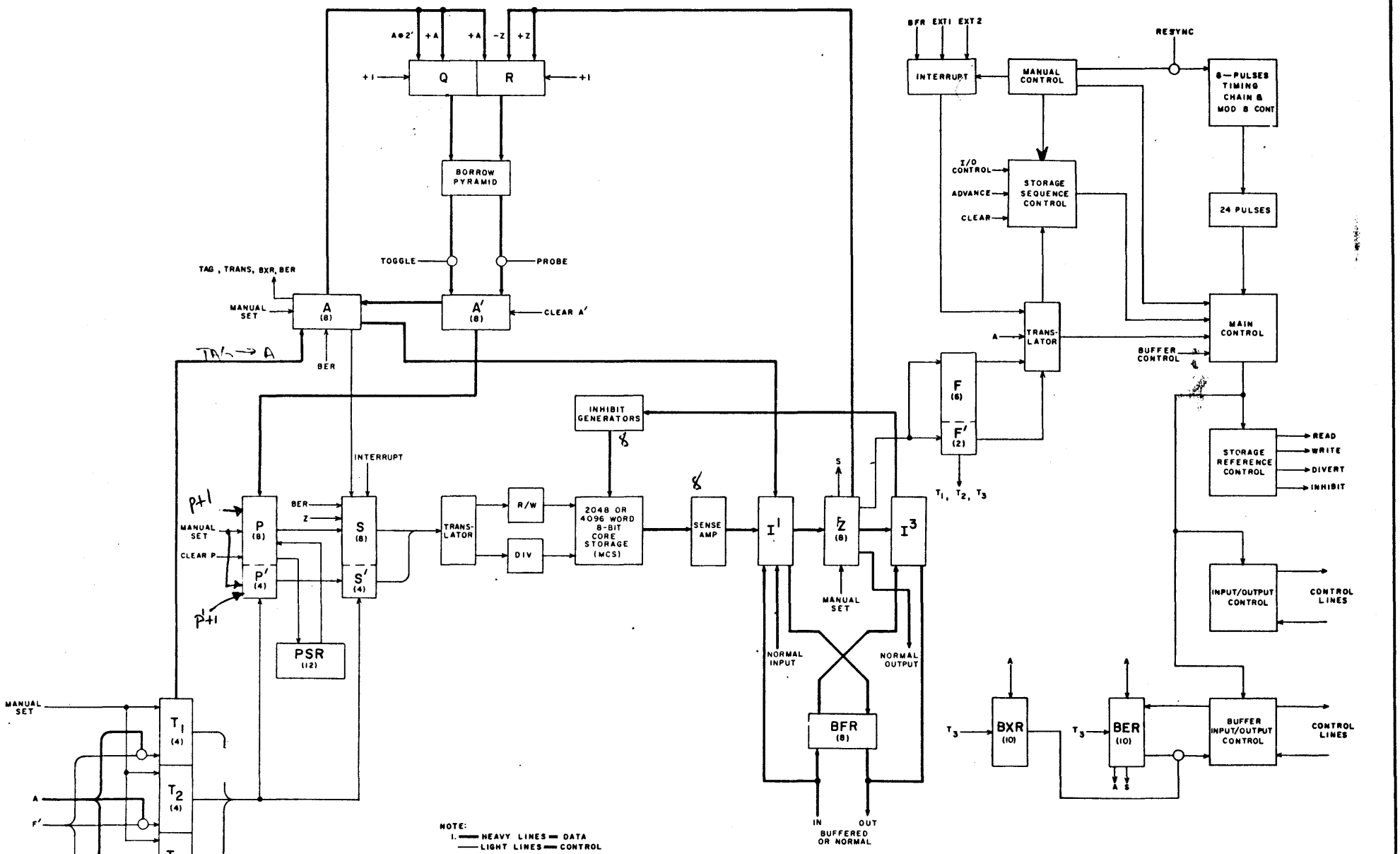
JACK ASSIGNMENTS - The jack assignments of the printed circuit cards associated with each logic symbol appear near the logical designation on the diagram. Jack assignments indicate the physical location of a printed circuit card.

Plug-in cards are designed with from one to four circuits, denoted by the letters A, B, C, or D. The omission of the circuit letter denotes a one circuit card. Two circuit inverter cards are labeled (top circuit, as card is viewed in the chassis connector) and C. Three circuit input (M---) and output (L---) amplifiers are labeled A, B, and C.

Single flip flop cards are not identified by circuit, but it is understood that the even-numbered inverter is associated with circuit A, the odd-numbered inverter with circuit C.



KEY TO SYMBOLS USED ON LOGIC DIAGRAMS



REV	DESCRIPTION	DATE	APPROVED
A	1589	7-15	KH

DESIGNED	
DRAWN	
CHECKED	
APPROVED	

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

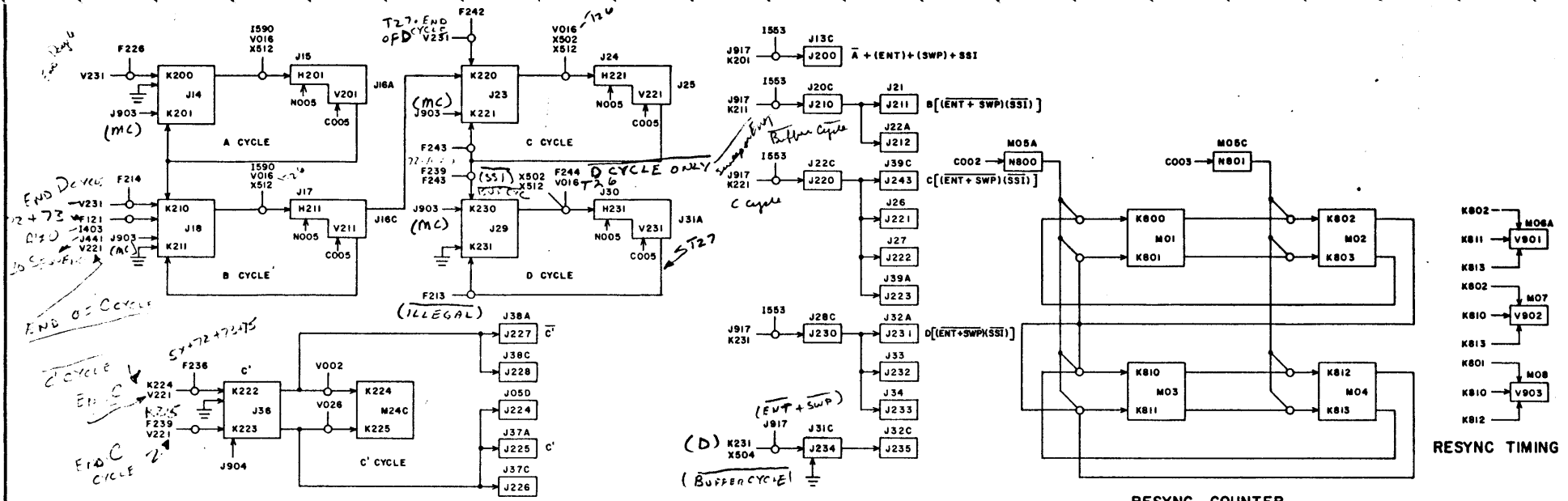
TITLE: BLOCK DIAGRAM, TELEPROGRAMMER—MODEL 8092

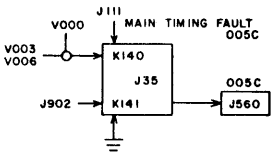
CONTROL DATA CORPORATION
IDP DIVISION

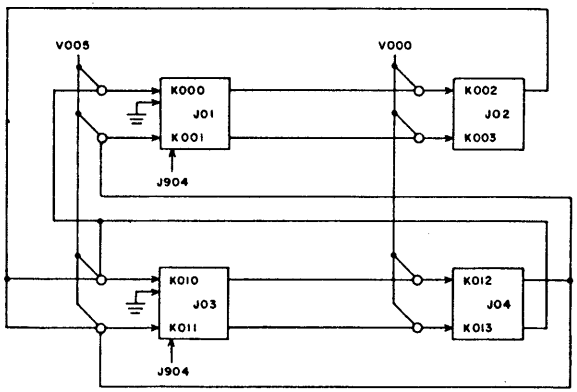
PROJECT OR PRODUCT

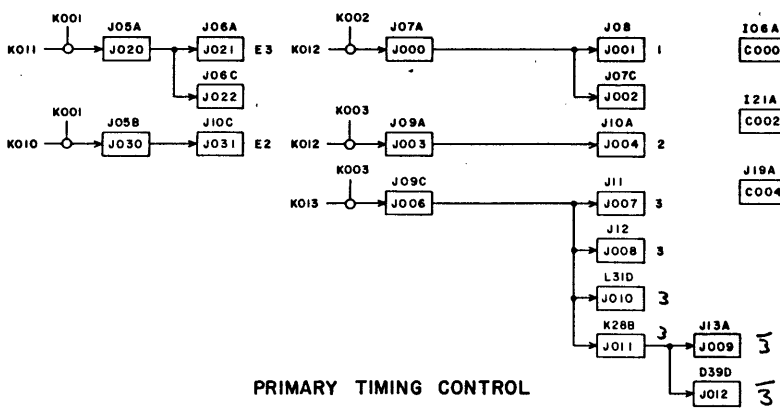
DRAWING NUMBER 364038 REV A

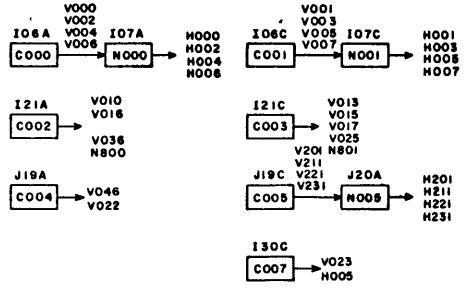
PAGE 1











A	1585	P.S.	KH	2/24/64	
REV.	NOTE	BY	REL. DWG.	CHK.	APPROVED

REVISIONS

APPROVED		2/24/64
CHECKED	J.H. NIPP	2/24/64
DRAWN	N.K. BECK	2/21/64
DESIGNED		

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

TITLE

LOGIC DIAGRAM,
MAIN CONTROL

CONTROL DATA CORPORATION
I D P DIVISION

PROJECT OR PRODUCT
8092 TELEPROGRAMMER

DRAWING NUMBER
360426

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SHT
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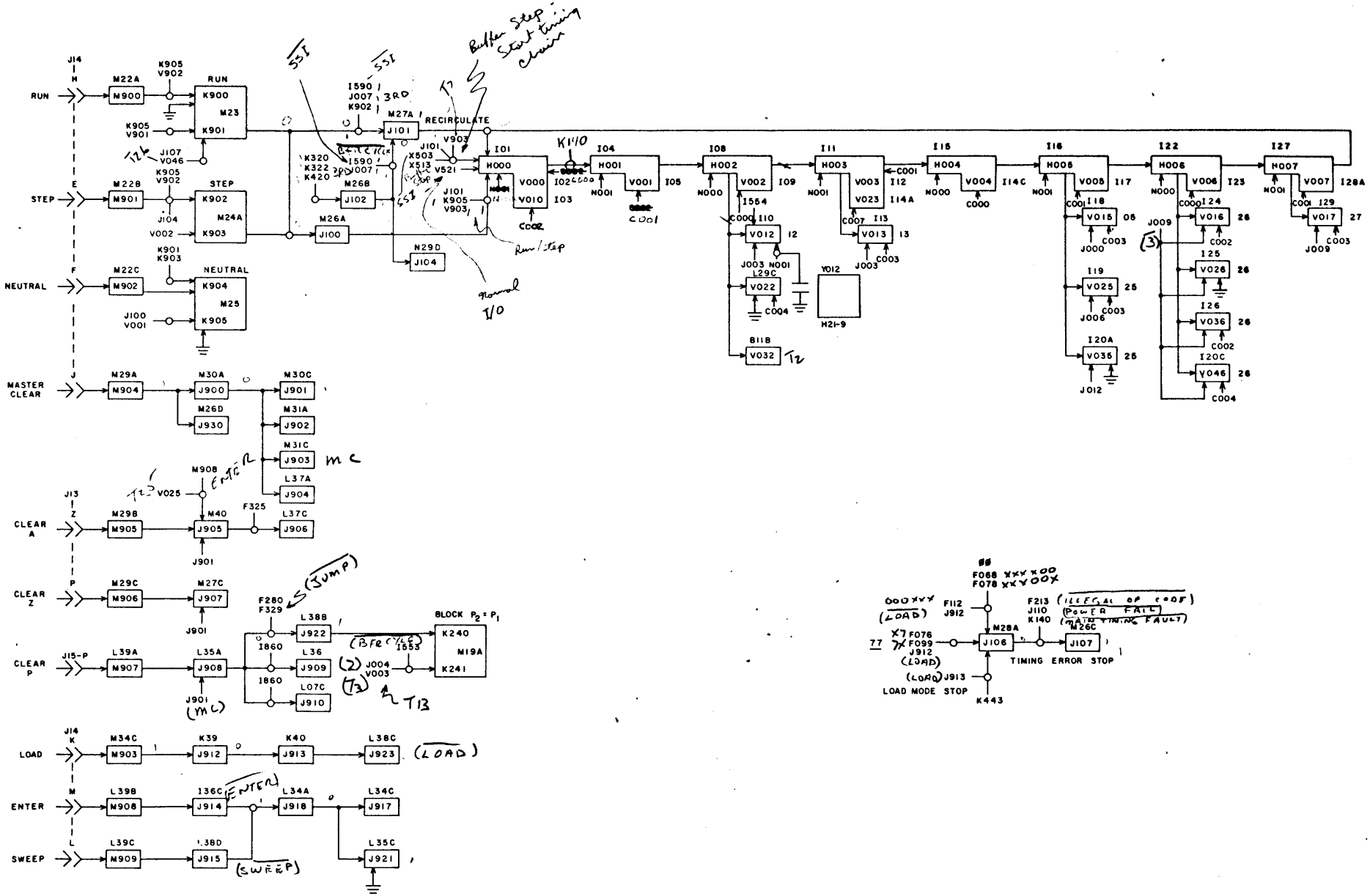

B	SSD 115-0015	KH	2/24/64		
A	115-0015	WL	2/24/64		
REV.	AUTH.	DATE	REQ.	DRW.	CHK.

REVISIONS

APPROVED
CHECKED J. H. NIPP 2/24/64
DRAWN I. N. K. BECK 2/24/64
DESIGNED

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

TITLE
LOGIC DIAGRAM,
MAIN TIMING

CONTROL DATA CORPORATION
I D P DIVISION

PROJECT OR PRODUCT
8092 TELEPROGRAMMER

DRAWING NUMBER
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REV
B

SHT

PAGE
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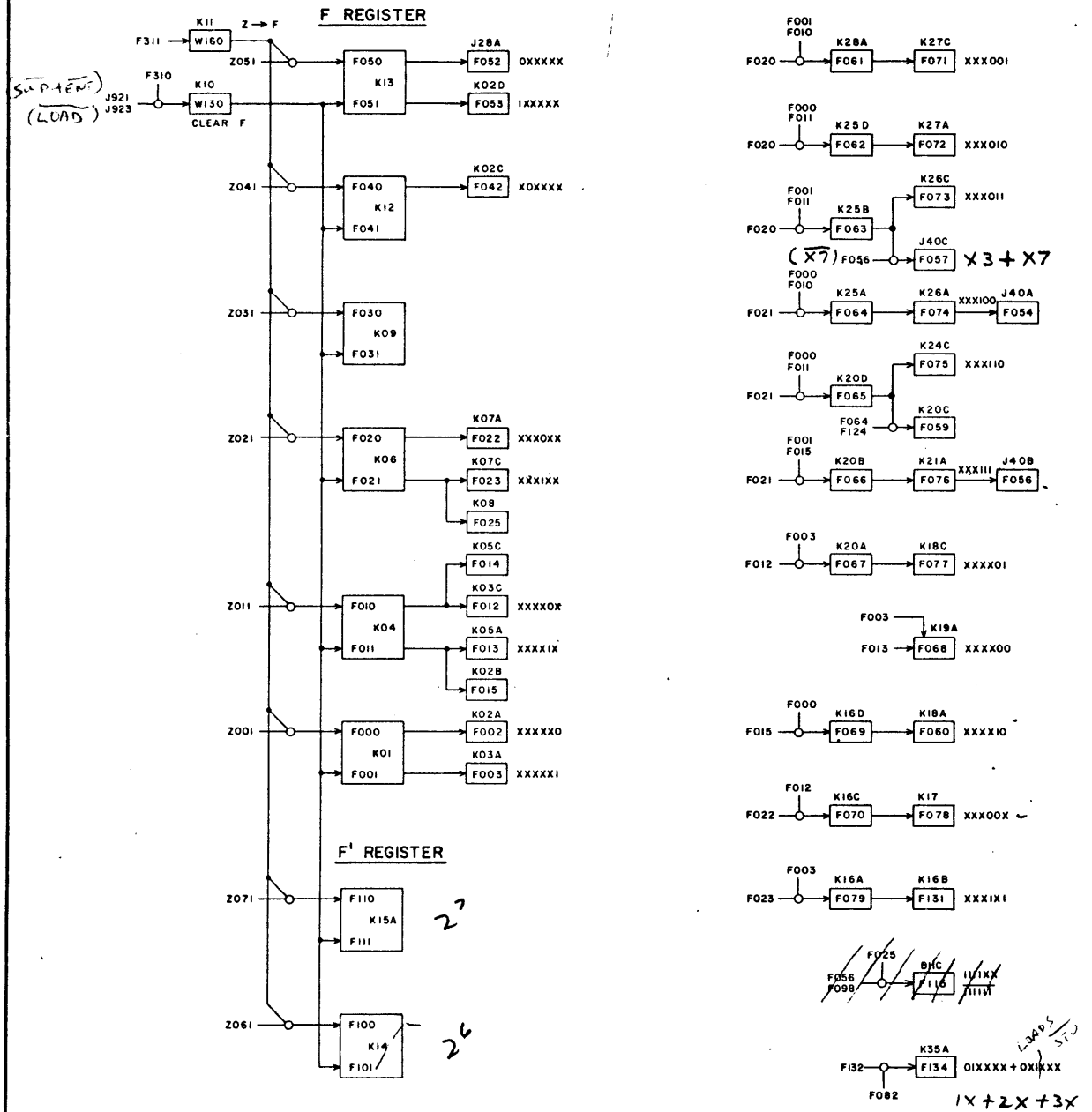

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A	163	10/22/64	JK			

APPROVED • W. C. MOE
CHECKED • J. H. NIPP 2/24/65
DRAWN • N. K. BECK 2/14/64
DESIGNED •

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

TITLE
LOGIC DIAGRAM,
REGISTERS, F & F' & TRANSLATORS

CONTROL DATA CORPORATION
I D P DIVISION

PROJECT OR PRODUCT
8092 TELEPROGRAMMER

DRAWING NUMBER
360449

REV
B

SHT

PAGE
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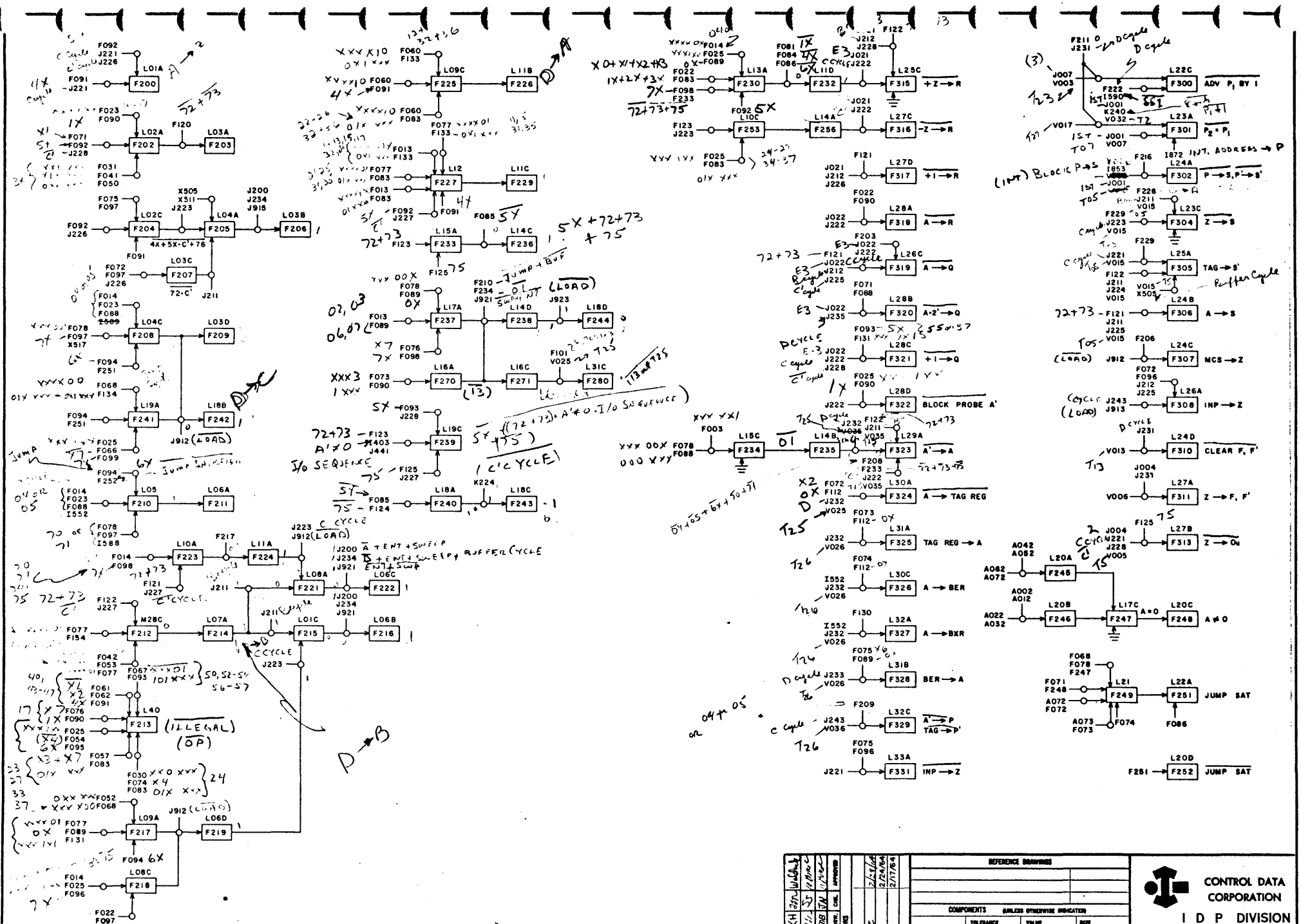
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F323
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F325
F326
F327
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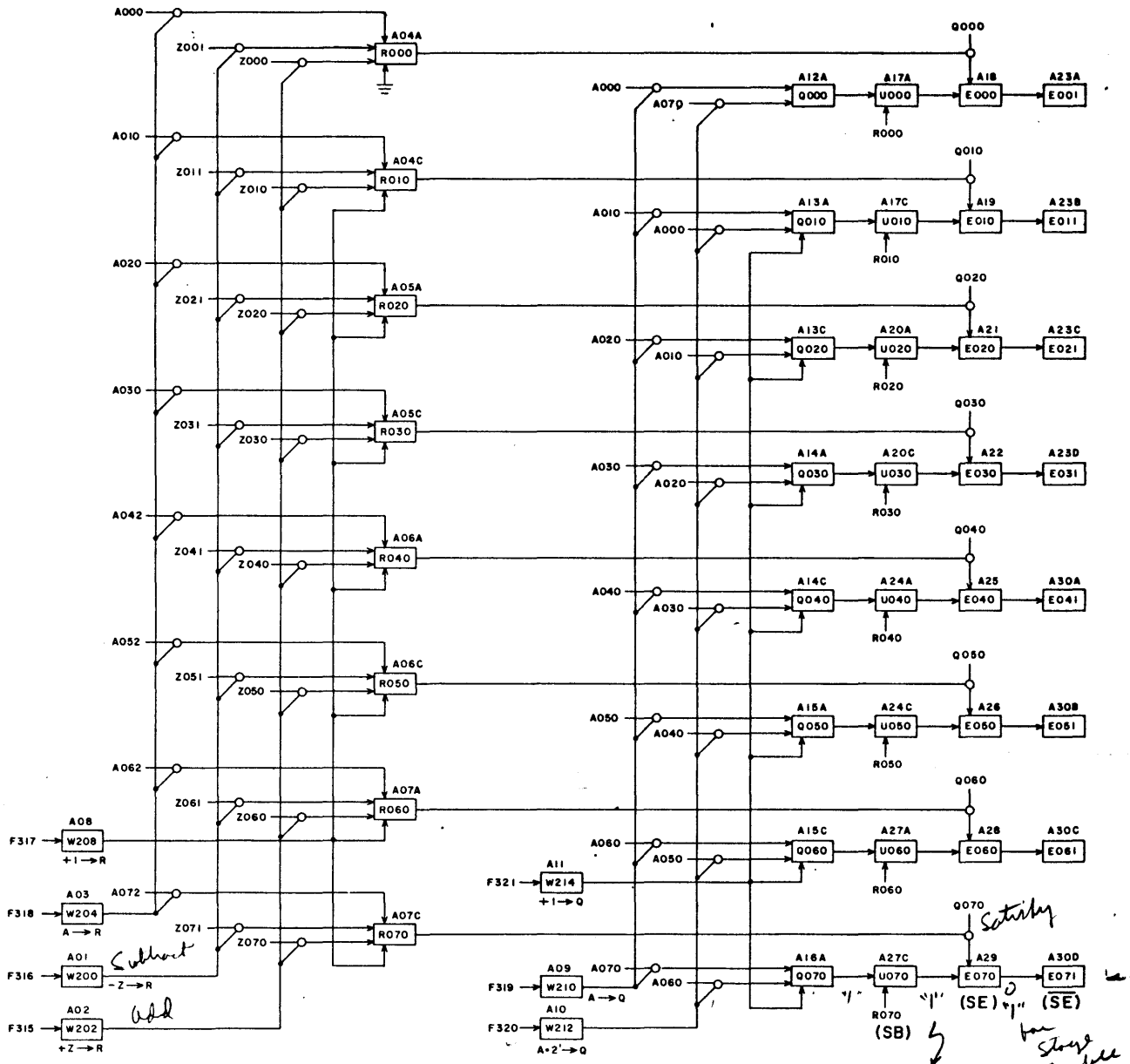
F329
F331
F234
F235
F239
(ILLEGAL)
(OP)
(LOAD)
ADV P1 BY 1
P2 → P1
1872 INT. ADDRESS → P
TAG → S'
MCS → Z
CLEAR F, F'
JUMP SAT
BLOCK PROBE A'
TAG REG
TAG REG → A
INP → Z
JUMP SAT
CONTROL DATA CORPORATION
I D P DIVISION
8092 TELEPROGRAMMER
360427
LOGIC DIAGRAM,
FUNCTION TRANSLATORS



SUBTRACT

OUTPUTS → R = Z

→ Q = A

ADD

R = Z

Q = A

REV.	APPR.	DATE	SEL. DRW.	CHK.	APPROVED		
REVISIONS							
-					APPROVED	W.B. Nipp	2/24/64
					CHECKED	J.H. NIPP	2/24/64
					DRAWN	N.K. BECK	2/18/64
					DESIGNED	-	

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

TITLE

LOGIC DIAGRAM,
R AND Q INVERTERS

CONTROL DATA CORPORATION

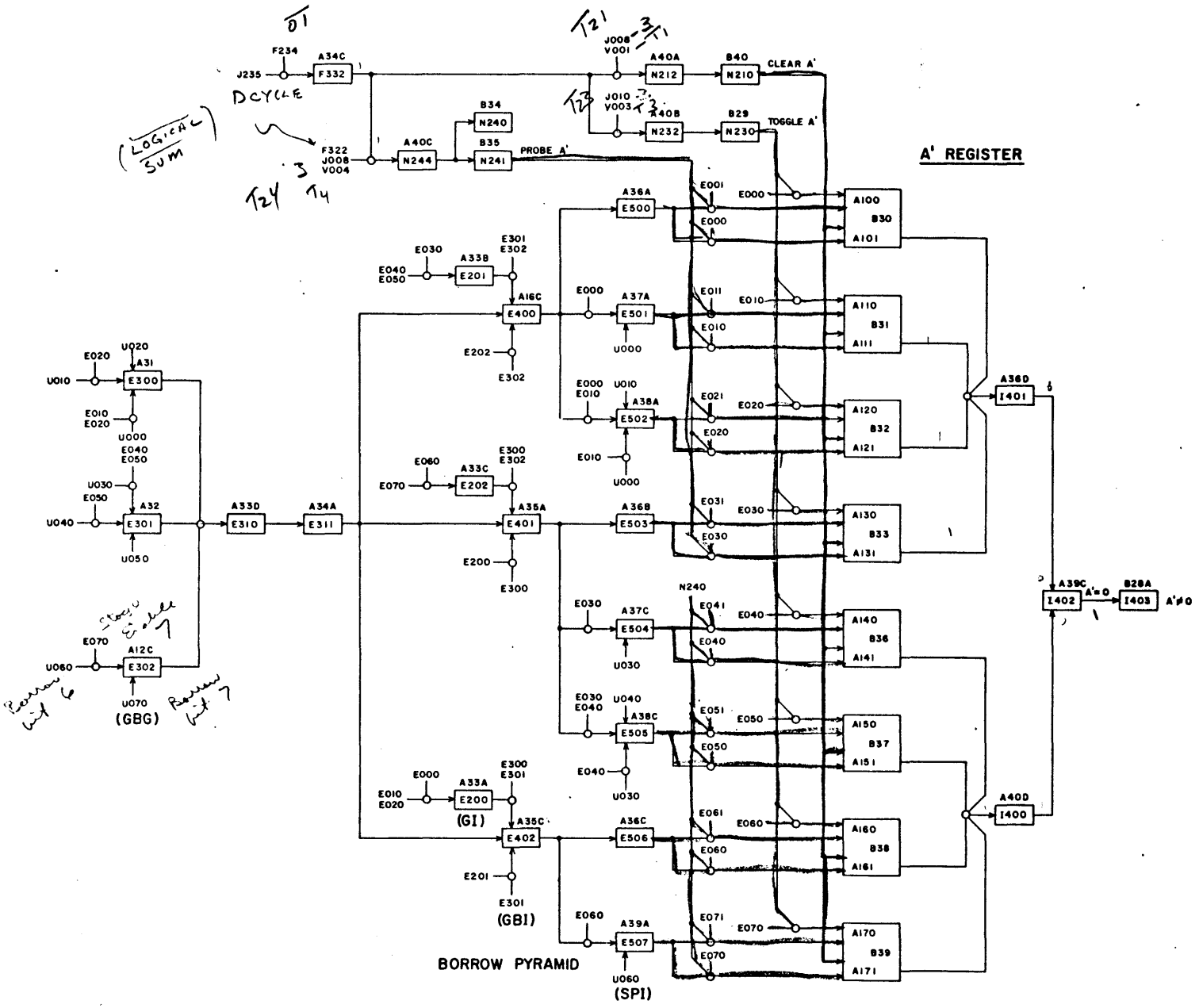
I D P DIVISION

PROJECT OR PRODUCT

8092 TELEPROGRAMMER

DRAWING NUMBER 360428 REV

SHT PAGE 6



REV.	REVISIONS	DATE	REL. DWG.	CHK.	APPROVED

APPROVED - W.S. Hall 2/18/64
CHECKED - J.H. NIPP 2/24/64
DRAWN - N.K. BECK 2/19/64
DESIGNED -

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

TITLE
LOGIC DIAGRAM,
REGISTER - A'

CONTROL DATA CORPORATION
I D P DIVISION

PROJECT OR PRODUCT
8092 TELEPROGRAMMER

DRAWING NUMBER
364157

REV

SHT

PAGE
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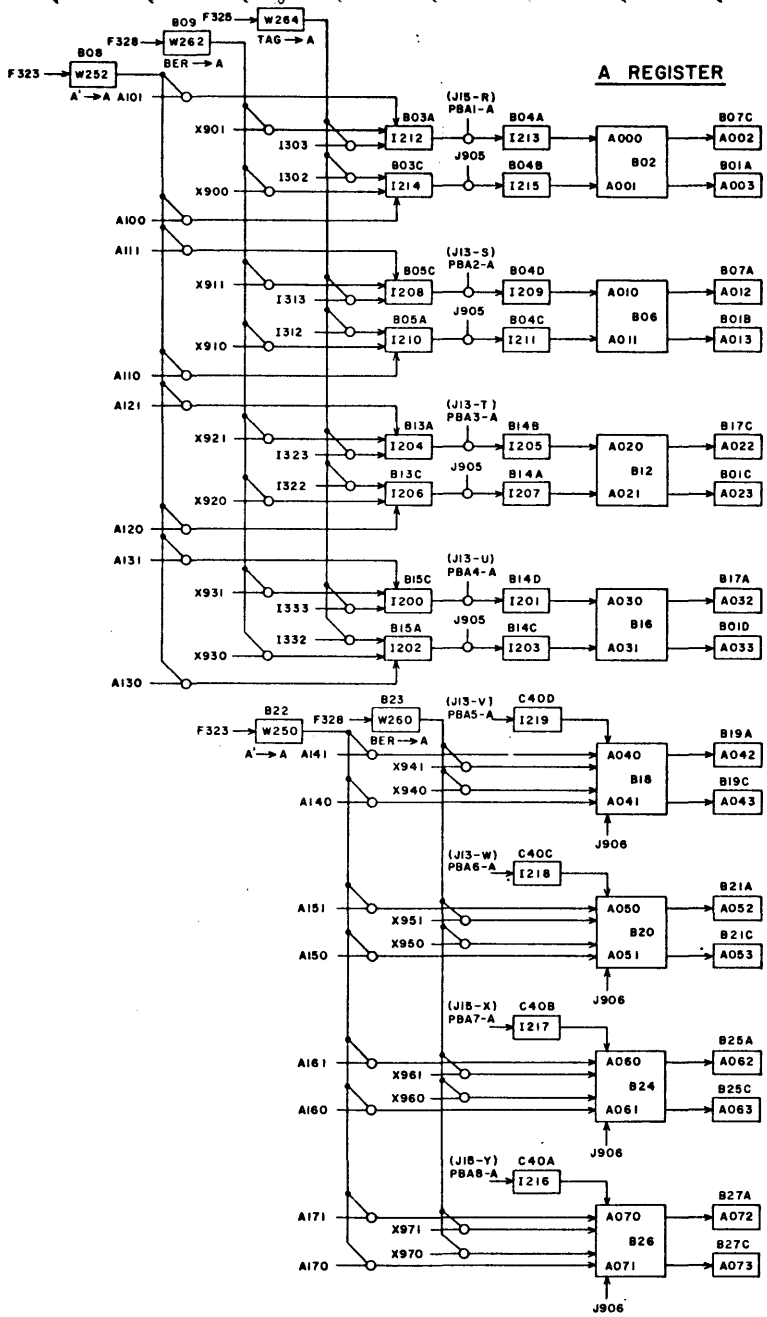

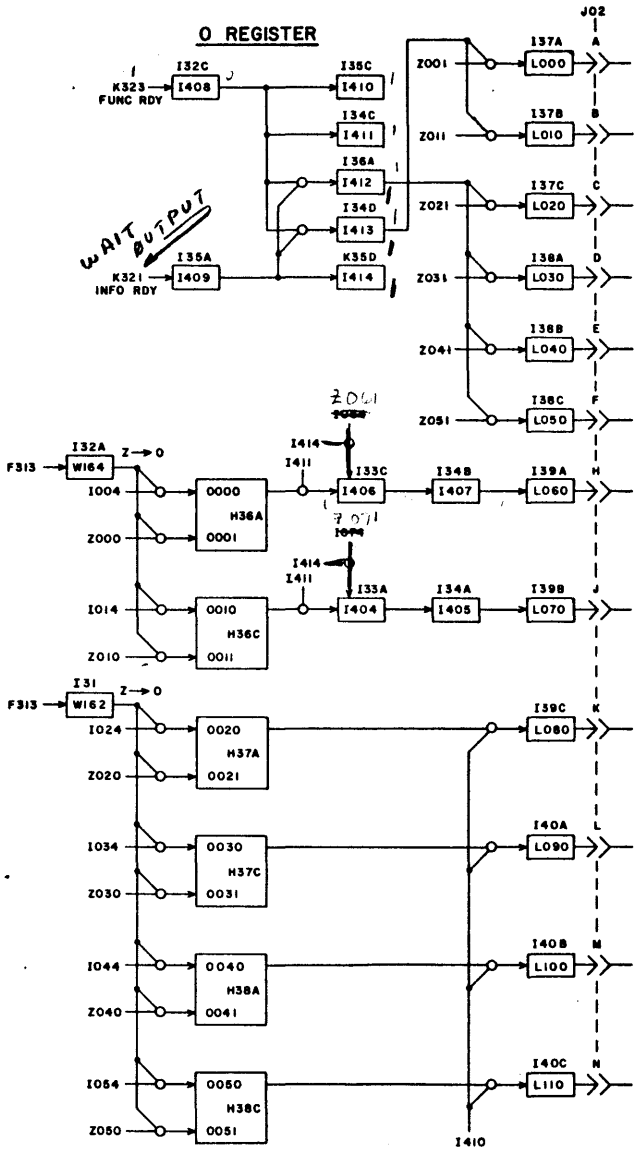

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A	1354	2/24/64	MB	[illegible]		

APPROVED - W.B. MOE 2/24/64
CHECKED - J.H. NIPP 2/24/64
DRAWN - N.K. BECK 2/6/64
DESIGNED -

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

TITLE
LOGIC DIAGRAM
REGISTERS - A AND O

CONTROL DATA CORPORATION
I D P DIVISION

PROJECT OR PRODUCT
8092 TELEPROGRAMMER

DRAWING NUMBER
360429

REV
B

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PAGE
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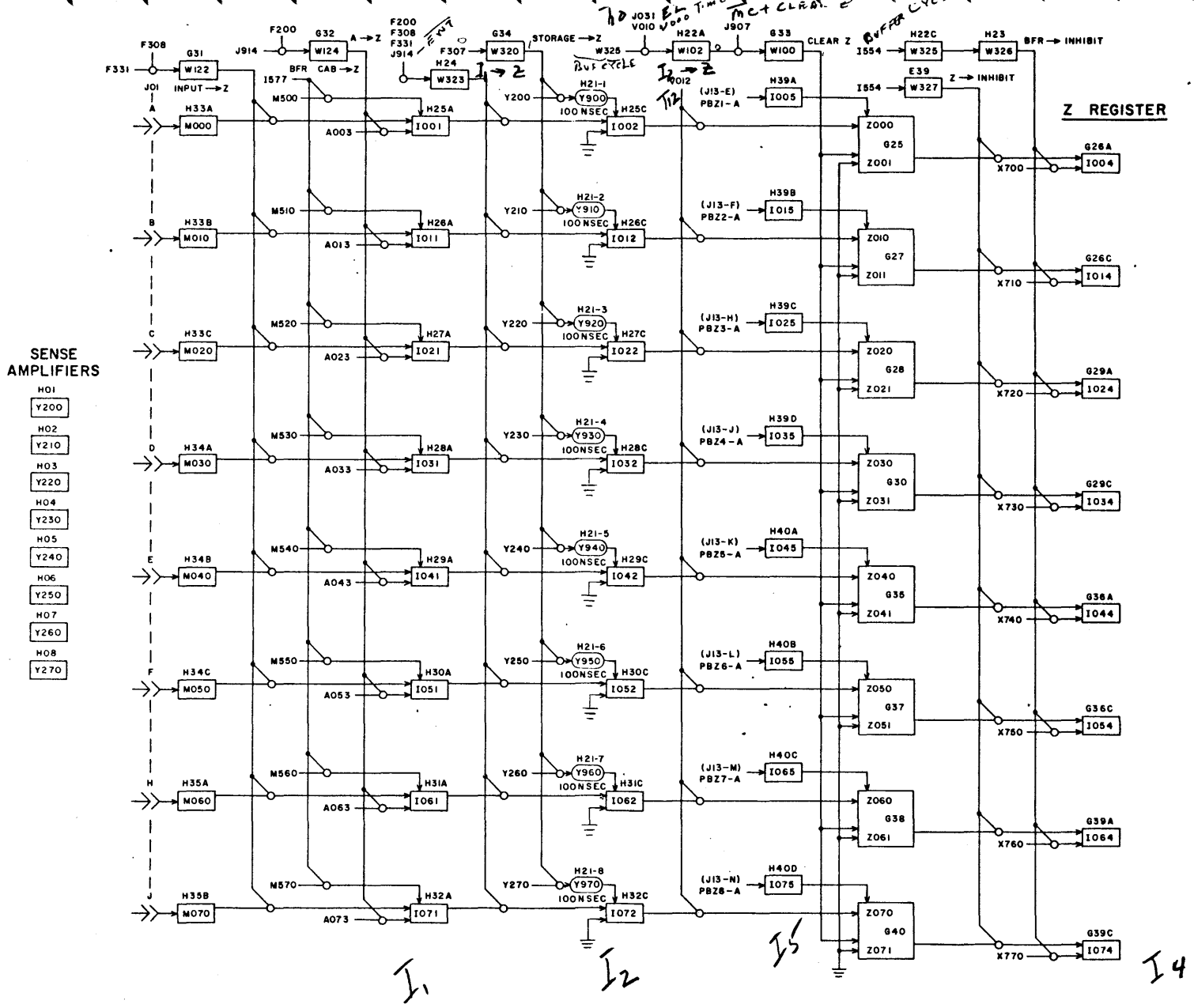

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B	1585	3-11-65				
A	1402	12-1-64		KH	JN	SS

APPROVED • W. E. NINE 2/24/64
CHECKED • J. H. NIPP 2/24/64
DRAWN • N. K. BECK 2/7/64
DESIGNED •

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

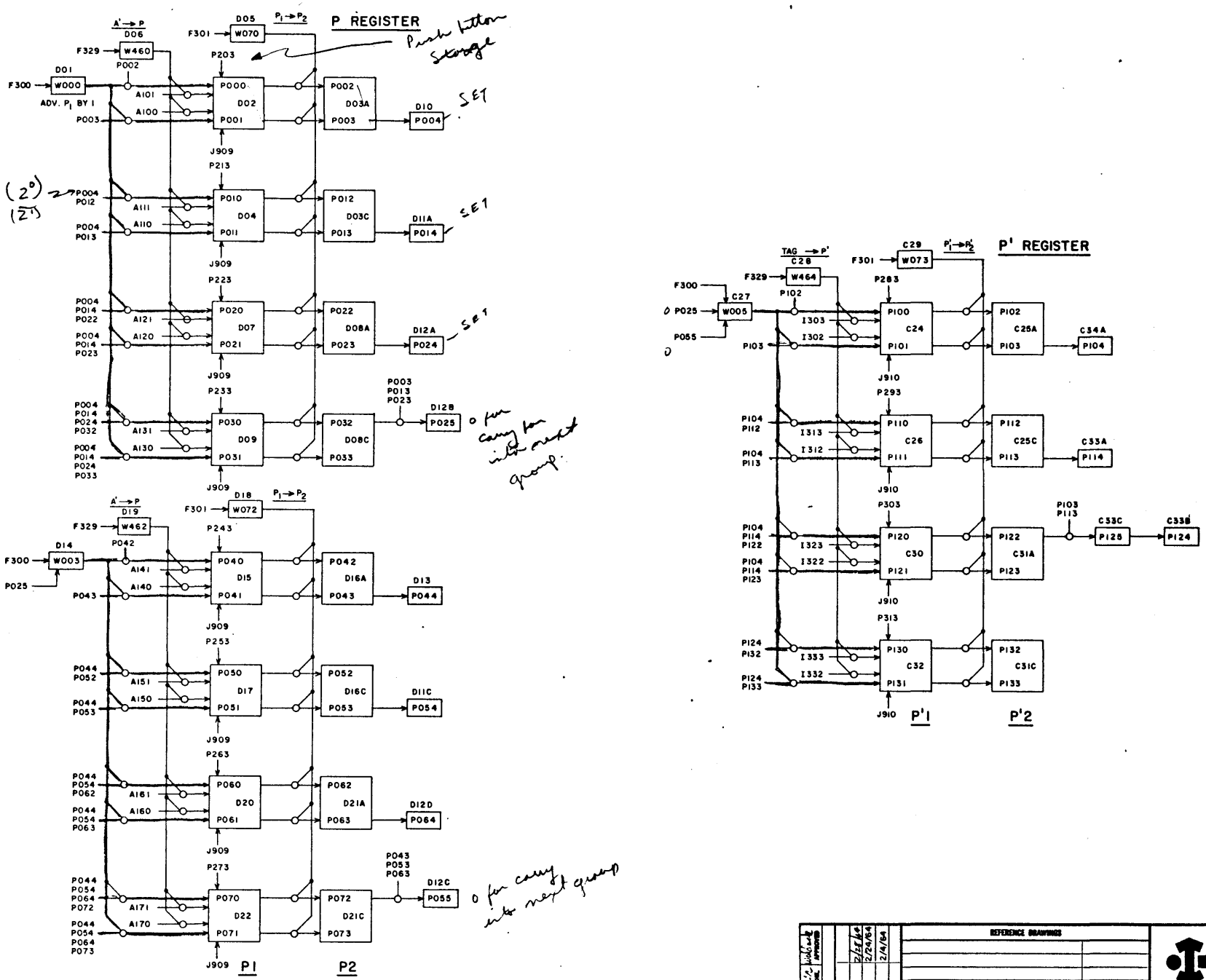
TITLE
LOGIC DIAGRAM
REGISTER-Z

CONTROL DATA CORPORATION
I D P DIVISION

PROJECT OR PRODUCT
8092 TELEPROGRAMMER

DRAWING NUMBER 364158 REV B

SHT PAGE 9



REVISIONS				
LTR	ENGR. APPR.	DATE	REQ. APPR.	CHG. APPROVED
A	1585	3-15-65	KH	

APPROVED • W.E.McC 7/15/64
CHECKED • J.H.NIPP 2/24/64
DRAWN • N.K.BECK 2/4/64
DESIGNED •

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

TITLE
LOGIC DIAGRAM
REGISTERS – P AND P'

CONTROL DATA CORPORATION
I D P DIVISION

PROJECT OR PRODUCT
8092 TELEPROGRAMMER

DRAWING NUMBER
360430

REV
A

SHT

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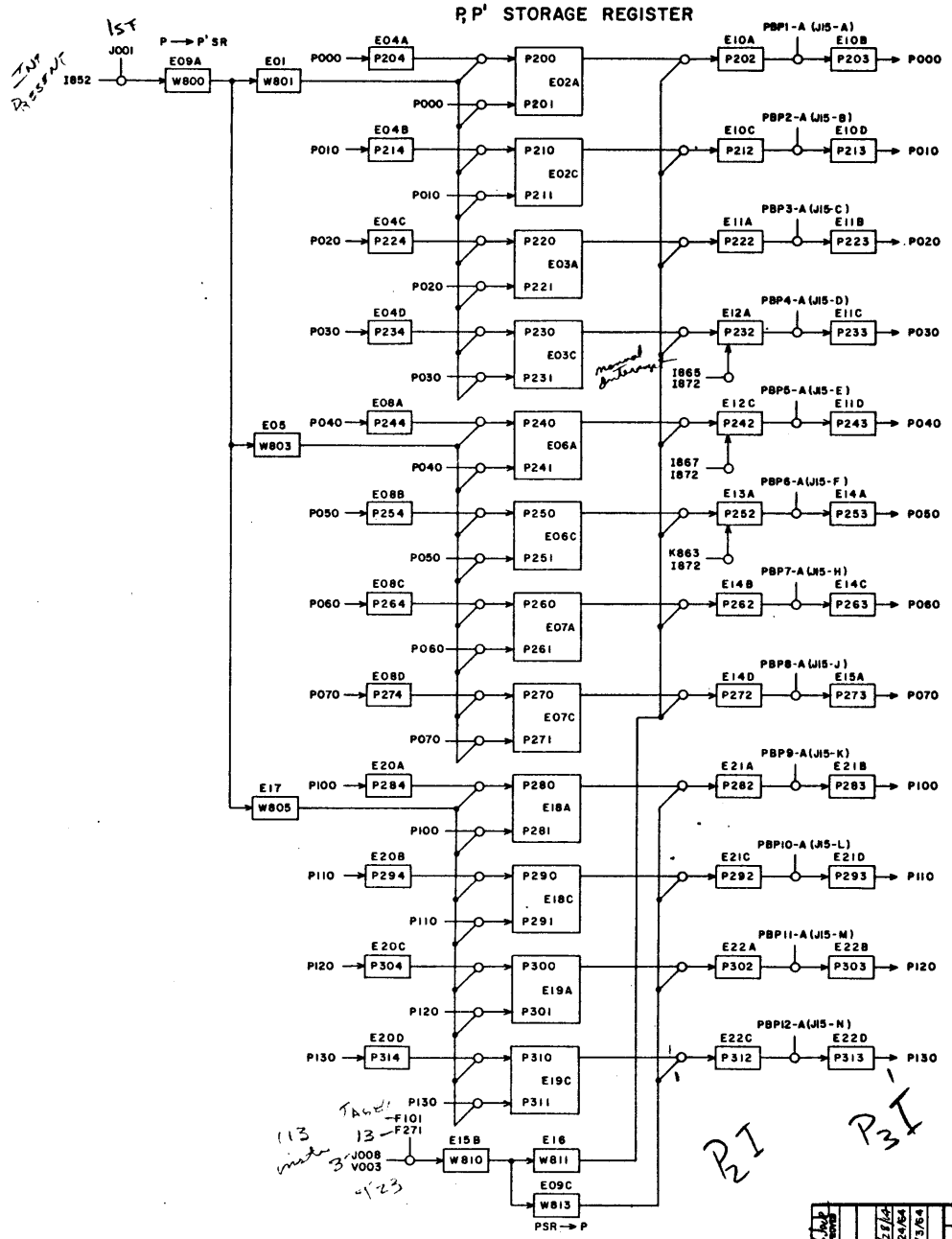
10



REV.	AUTH.	DATE	REVISIONS	DES.	DRW.	CHK.	APPROVED
A	ISRS	2-25-64			KH		

APPROVED • W. E. Hoe 2/26/64
CHECKED • J H NIPP 2/24/64
DRAWN • N K BECK 2/3/64
DESIGNED •

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

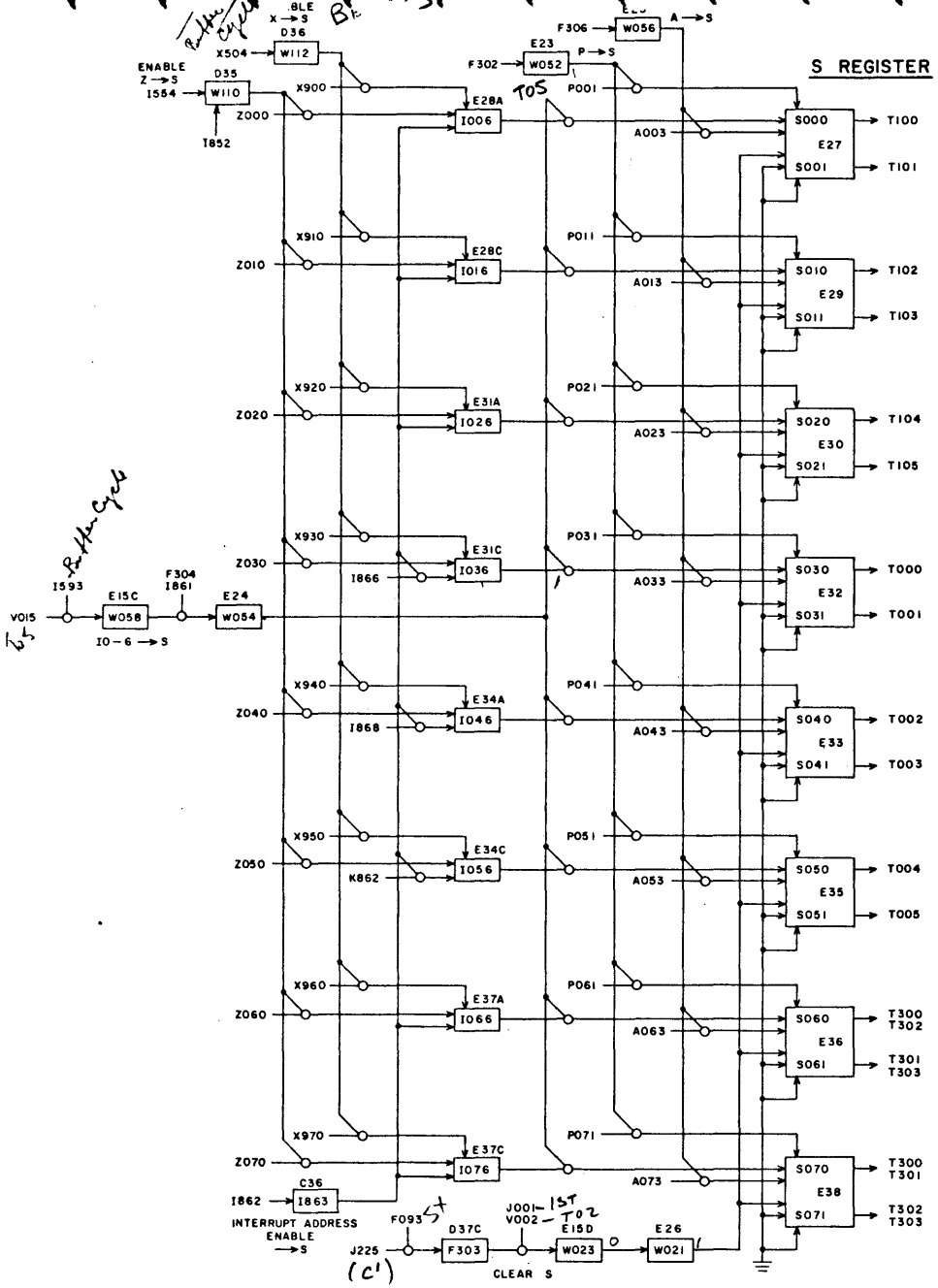
TITLE
LOGIC DIAGRAM
REGISTER – PSR

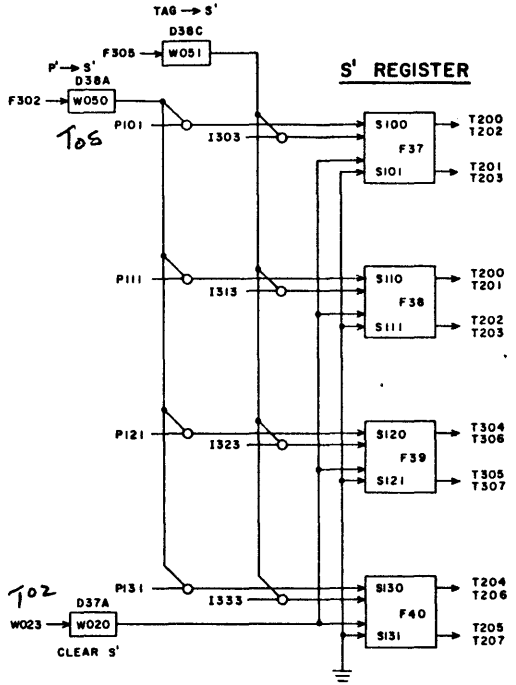
CONTROL DATA CORPORATION
I D P DIVISION

PROJECT OR PRODUCT
8092 TELEPROGRAMMER

DRAWING NUMBER 364159 REV A

SHT PAGE 11





REVISIONS			
REV.	ADVICE	DATE	APPROVED
A	1585	2/5/64	KH

DESIGNED - N.K. BECK 2/5/64
DRAWN - N.K. BECK 2/5/64
CHECKED - J.H. NIPP 2/24/64
APPROVED - W.P. MOE 2/26/64

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

TITLE
LOGIC DIAGRAM
REGISTERS - S AND S'

CONTROL DATA CORPORATION
I D P DIVISION

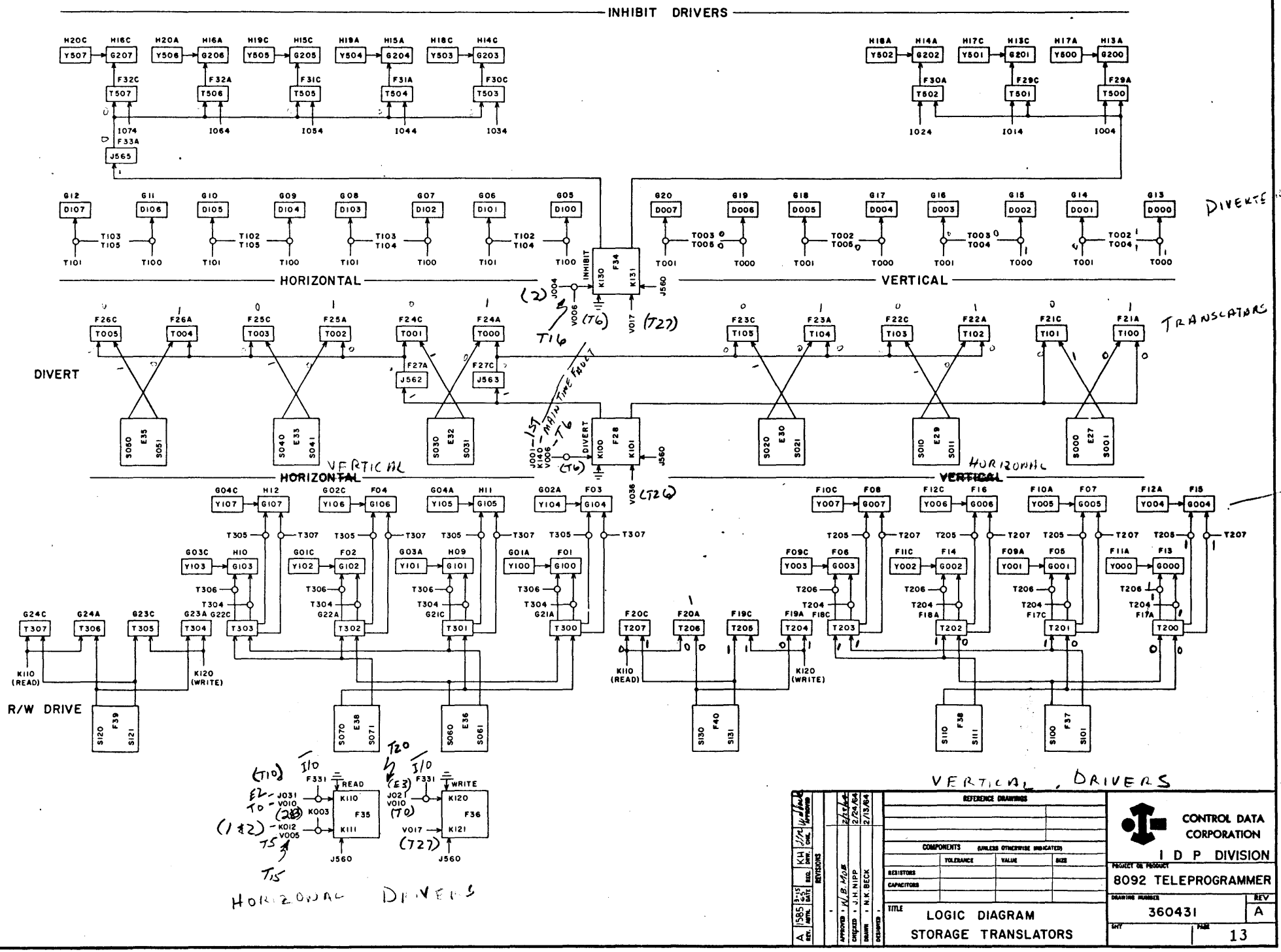
PROJECT OR PRODUCT
8092 TELEPROGRAMMER

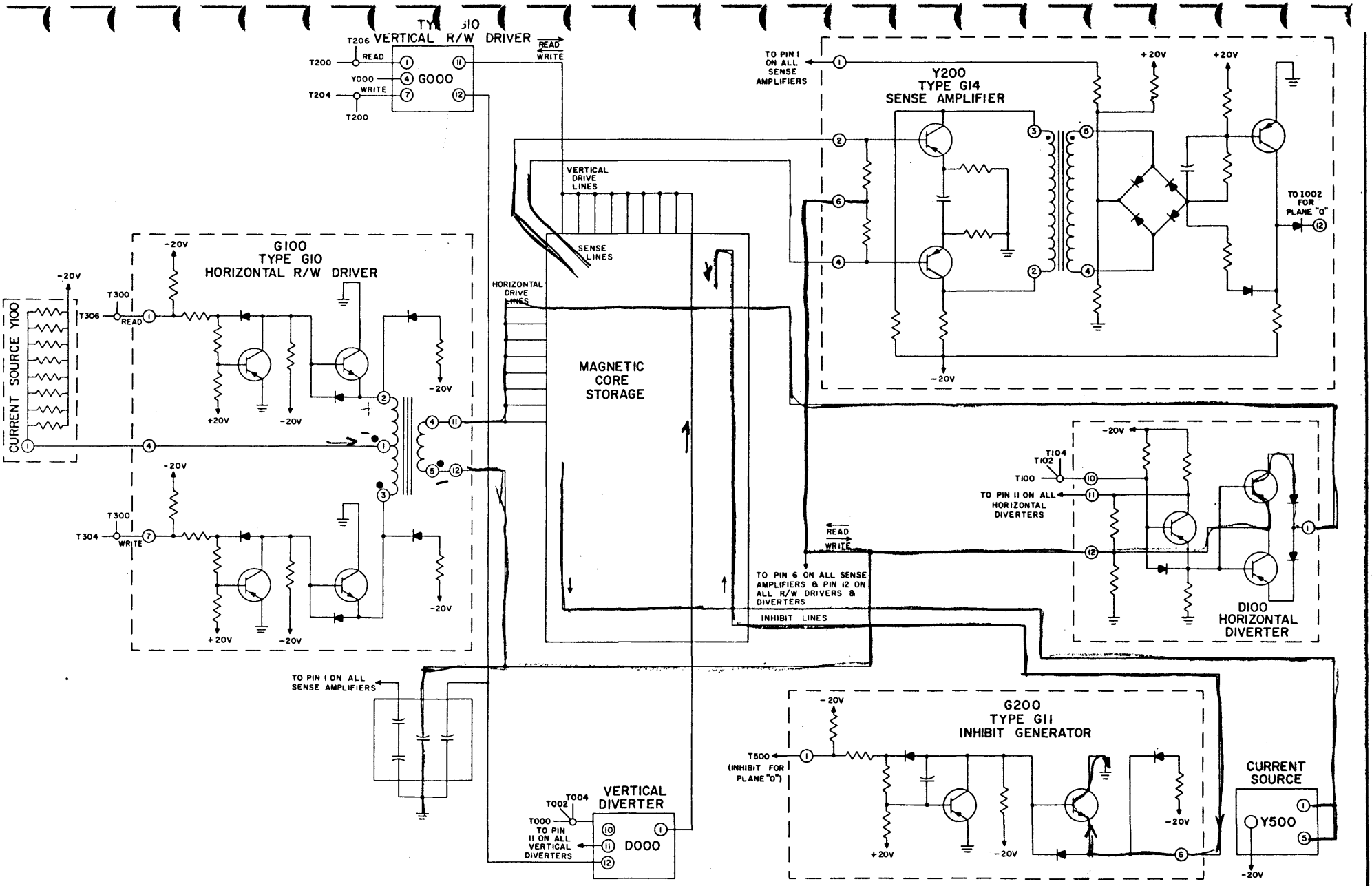
DRAWING NUMBER
364160

REV
A

SHT

PAGE
12


INHIBIT DRIVERS
HORIZONTAL
VERTICAL
DIVERT
TRANSLATORS
HORIZONTAL
VERTICAL
R/W DRIVE
HORIZONAL DRIVERS
VERTICAL DRIVERS
REFERENCE DRAWINGS
COMPONENTS (UNLESS OTHERWISE INDICATED)
RESISTORS
CAPACITORS
TOLERANCE
VALUE
SIZE
TITLE
LOGIC DIAGRAM
STORAGE TRANSLATORS
CONTROL DATA CORPORATION
I D P DIVISION
PROJECT OR PRODUCT
8092 TELEPROGRAMMER
DRAWING NUMBER
360431
REV
A
SHT
13
APPROVED
CHECKED
DRAWN
DESIGNED
J.H. NIPP
N.K. BECK
2/13/64
2/24/64
REVISIONS



REV.	LTR	DATE	REVISIONS	DRW.	CHK.	APPROVED
A	1585	3-15-63	-	K.W.		

APPROVED - W.B. Hoe 2/24/64
CHECKED - J.H. NIPP 2/24/64
DRAWN - N.K. BECK 1/27/64
DESIGNED -

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	WATTAGE	SIZE
RESISTORS			
CAPACITORS			

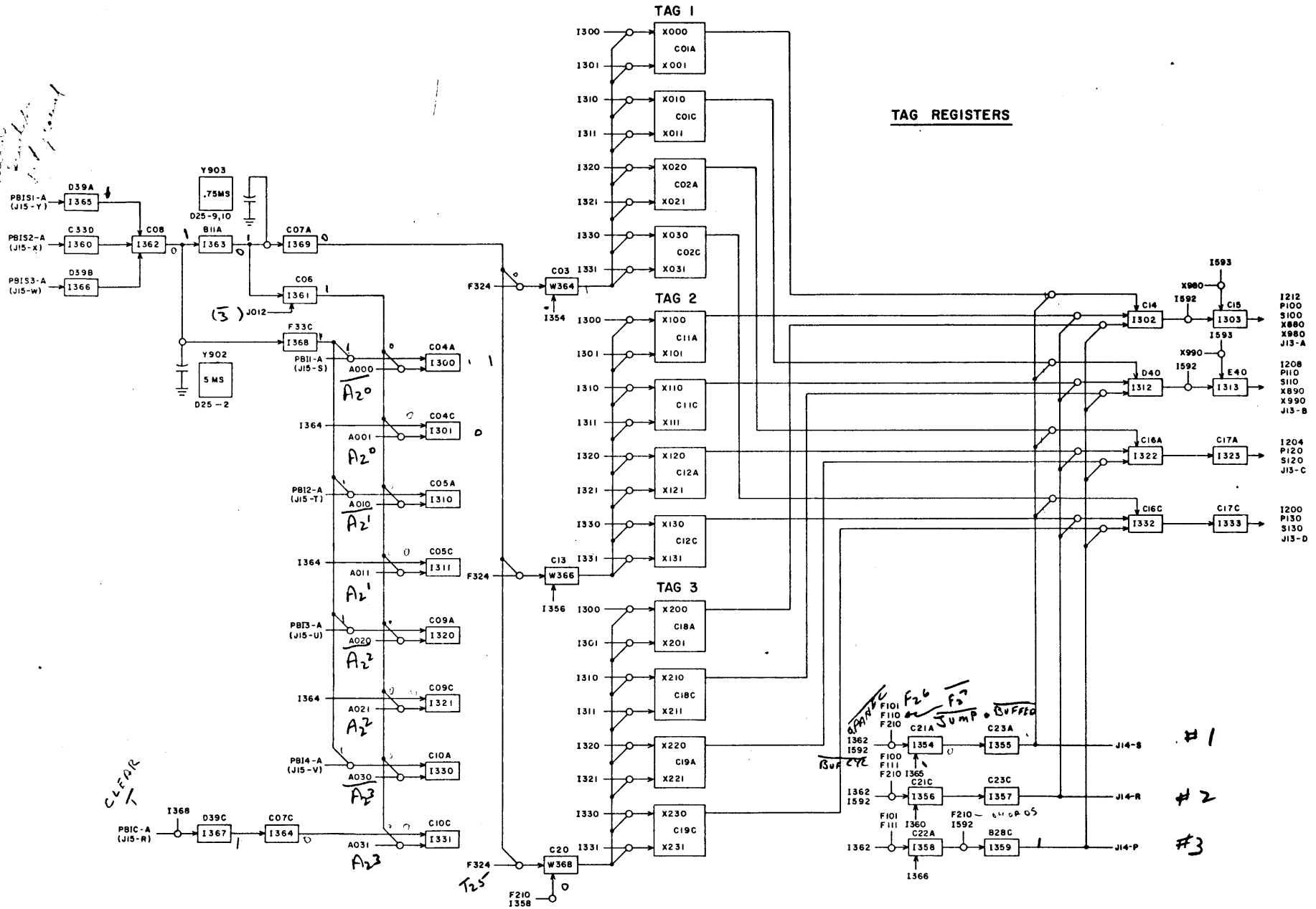
TITLE
SCHEMATIC DIAGRAM,
TYPICAL STORAGE CIRCUITS

CONTROL DATA CORPORATION
I D P DIVISION

PROJECT OR PRODUCT
8092 TELEPROGRAMMER

DRAWING NUMBER 360442 REV A

SHT PAGE 14



REV.	A		
AUTH.	1585		
DATE	2-5		
REVISIONS			
DRW.	KH		
CHK.			
APPROVED	W.E.P.	2/24/64	
CHECKED	J.H. NIPP	2/24/64	
DRAWN	N.K. BECK	2/10/64	
DESIGNED			

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

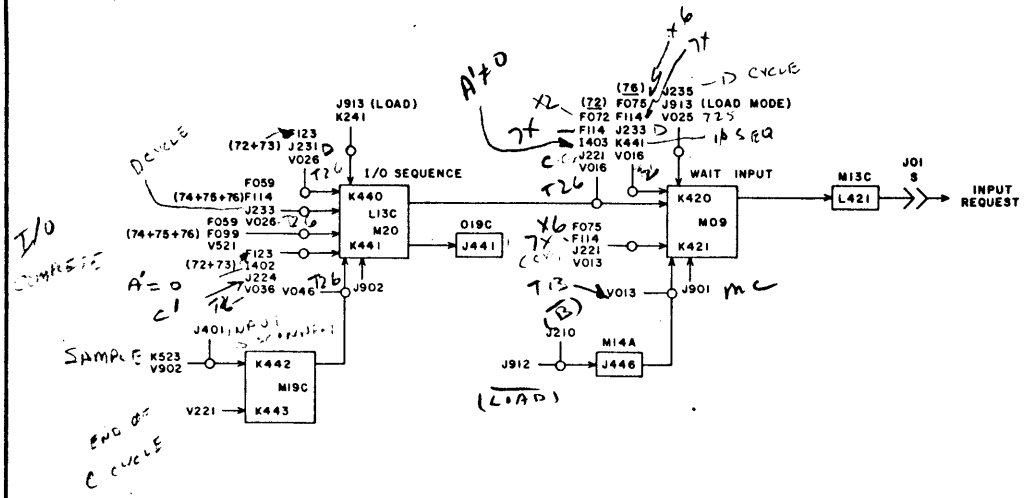
TITLE: LOGIC DIAGRAM, REGISTER - TAG 1,2,& 3

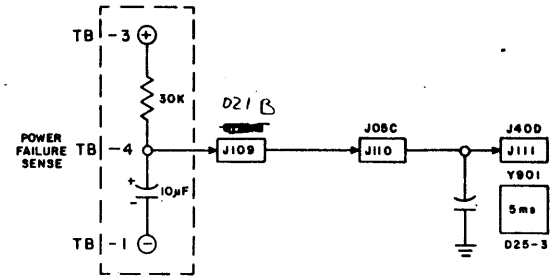
CONTROL DATA CORPORATION
I D P DIVISION

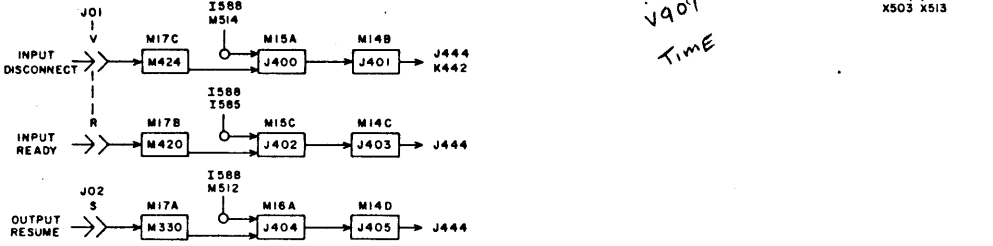
PROJECT OR PRODUCT: 8092 TELEPROGRAMMER

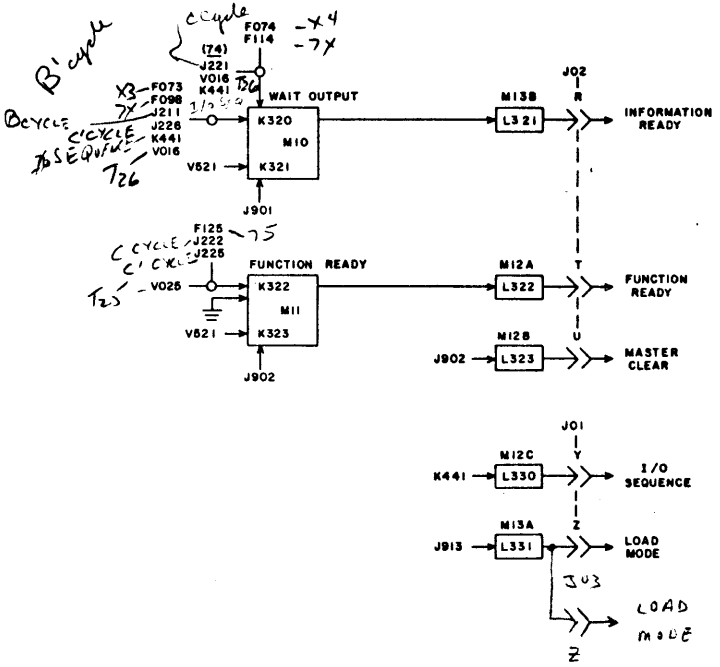
DRAWING NUMBER: 360433 REV: A

SHT: PAGE: 15









REVISIONS					
REV.	NOTE	DATE	DRN.	CHK.	APPROVED
A	1954	2/24/64			
B	1411	2/24/64			
C	1585	3-19-65	KH		

DESIGNED - N. K. BECK 2/20/64
DRAWN - J. H. NIPP 2/24/64
CHECKED - W. E. MOE 2/24/64
APPROVED

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

TITLE: LOGIC DIAGRAM, INPUT/OUTPUT CONTROL

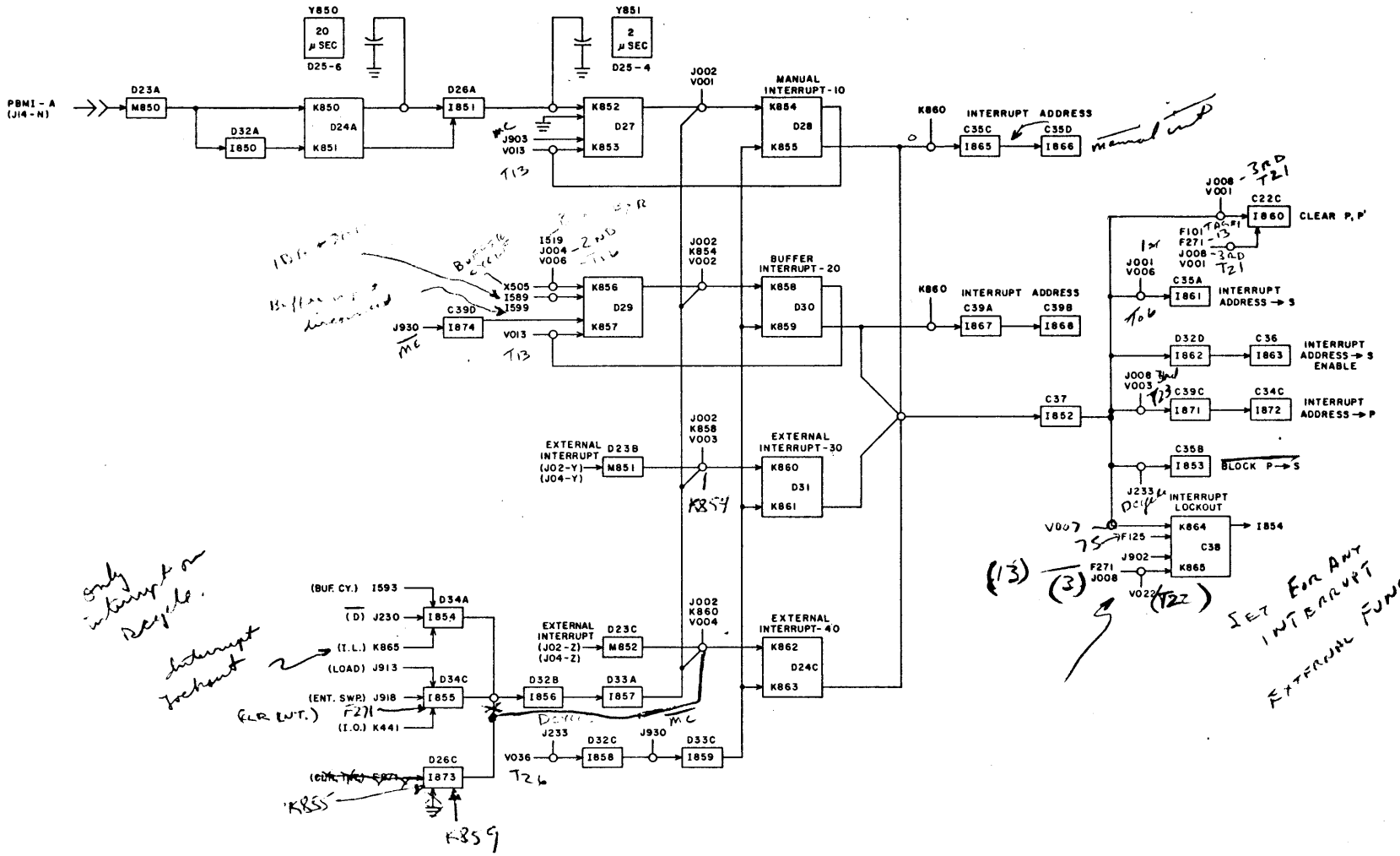
CONTROL DATA CORPORATION
I D P DIVISION

PROJECT OR PRODUCT: 8092 TELEPROGRAMMER

DRAWING NUMBER: 360425 REV: C

SHT: PAGE: 16

D



REV.	AUTH.	DATE	REVISIONS	CHK.	APPROVED
C	1585	3-5-64	REQ.		
B	1354	2-24-64	DRW.		
A	1334	1-31-64			

APPROVED - W. E. McKee 2/24/64
CHECKED - J. H. NIPP
DRAWN - N. K. BECK 1/31/64
DESIGNED -

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

TITLE
LOGIC DIAGRAM
INTERRUPT

CONTROL DATA CORPORATION
I D P DIVISION

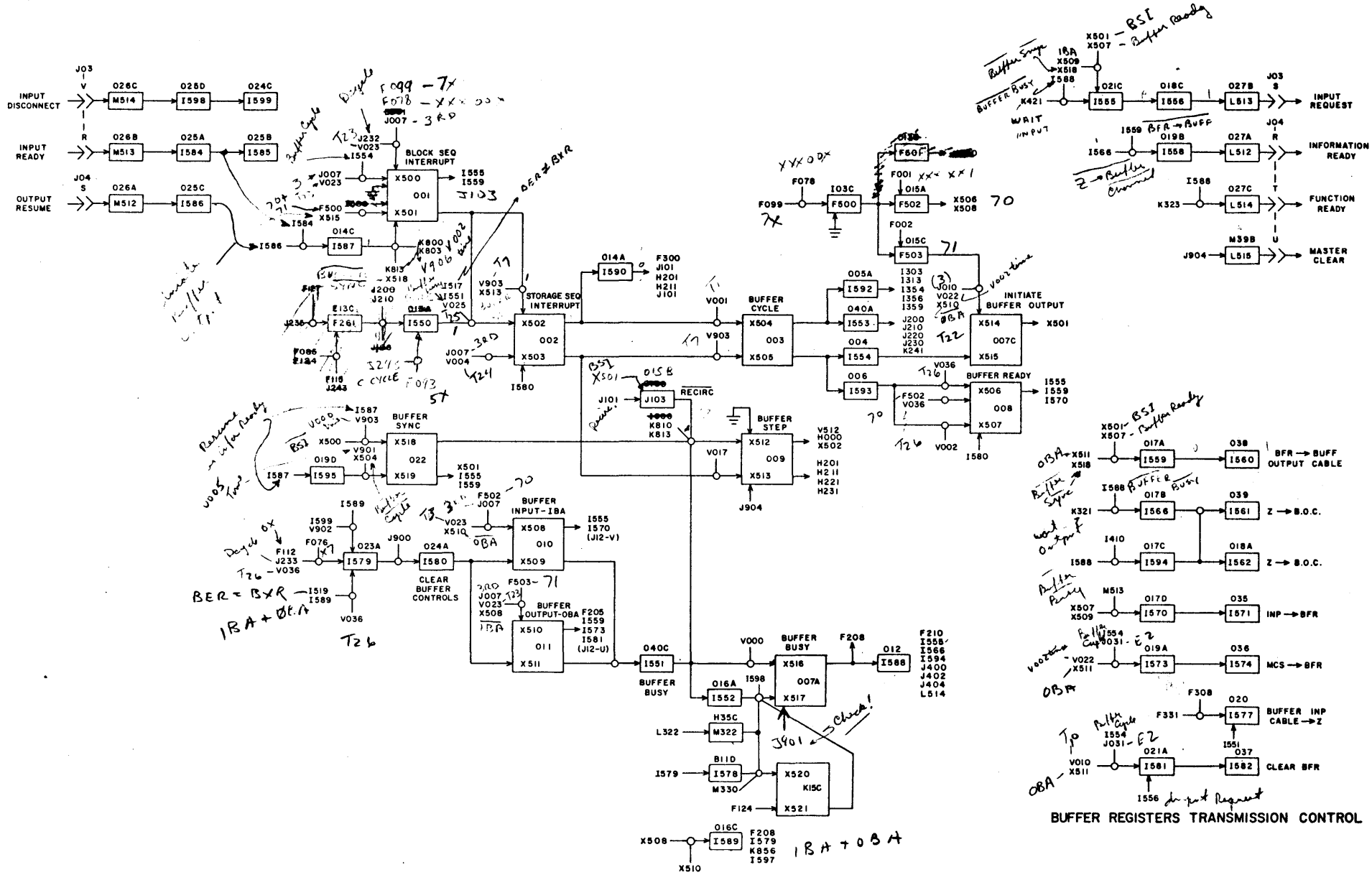
PROJECT OR PRODUCT
8092 TELEPROGRAMMER

DRAWING NUMBER
360434

REV
P

SHT

PAGE
17



REV.	DATE	REVISIONS	APPROVED
A	1334		
B	1411		
C	1451		
D	1470		
E	1505		
F	1585		

DESIGNED • N.K. BECK 2/12/64
DRAWN • J.H. NIPP 2/24/64
CHKD. • V.B. MC
APPROVED •

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

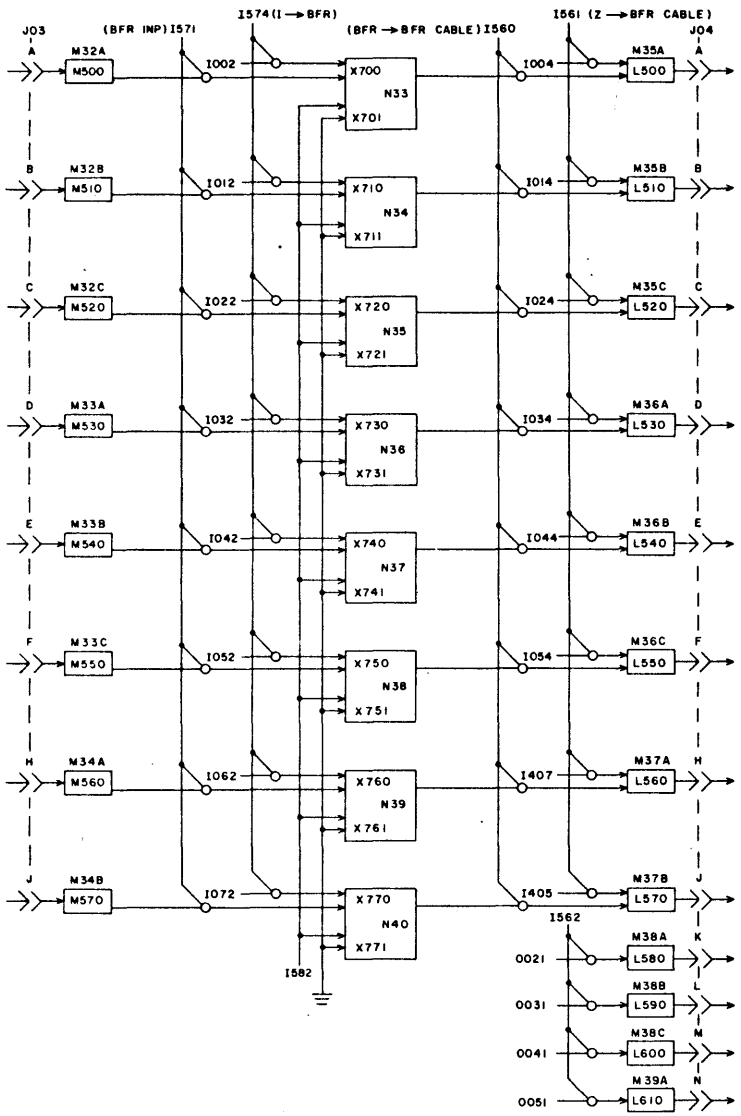
TITLE
LOGIC DIAGRAM
BUFFER CONTROLS

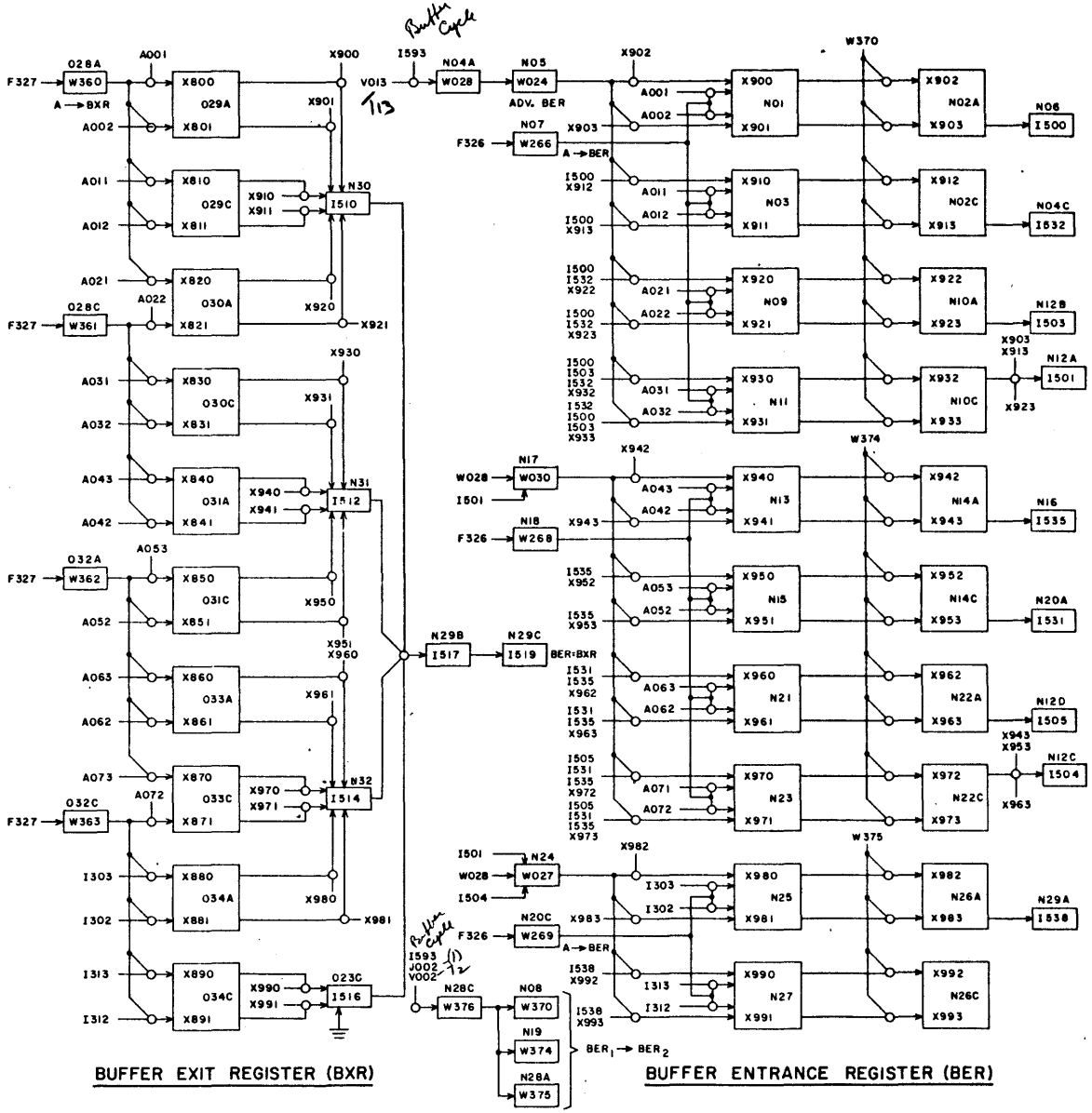
CONTROL DATA CORPORATION
I D P DIVISION

PROJECT OR PRODUCT
8092 TELEPROGRAMMER

DRAWING NUMBER 360447 REV F

SHT PAGE 18





BUFFER EXIT REGISTER (BXR)

BUFFER ENTRANCE REGISTER (BER)

A	1565	3-25-64	KH			
REV.	AUTH.	DATE	REGL. DRW.	CHKL.	APPROVED	

REVISIONS

APPROVED • W. E. Hoehn 2/24/64
CHECKED • J. H. NIPP 2/24/64
DRAWN • N. K. BECK 1/30/64
DESIGNED •

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

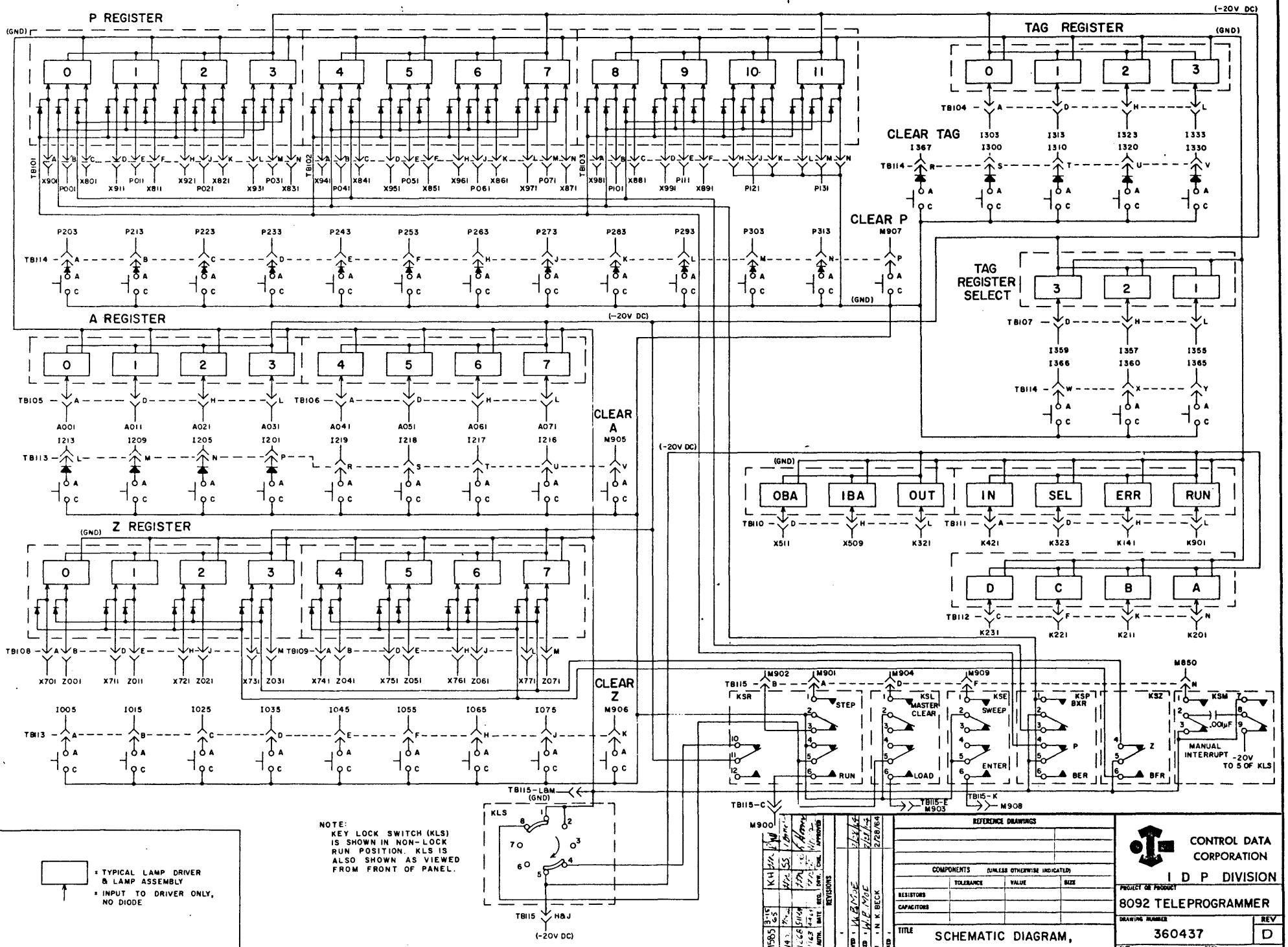
TITLE
LOGIC DIAGRAM
REGISTERS - BFR, BXR, BER

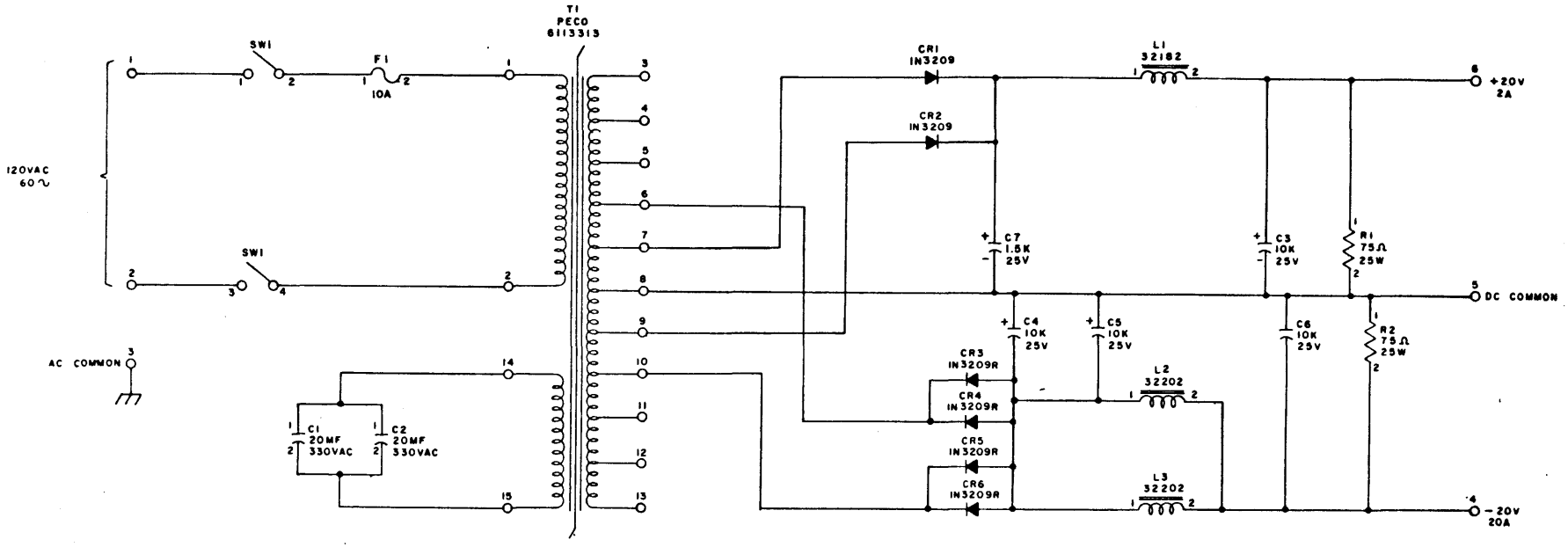
CONTROL DATA CORPORATION
I D P DIVISION

PROJECT OR PRODUCT
8092 TELEPROGRAMMER

DRAWING NUMBER 360432 REV A

SHT PAGE 19


P REGISTER
A REGISTER
Z REGISTER
TAG REGISTER
TAG REGISTER SELECT
CLEAR TAG
CLEAR P
CLEAR A
CLEAR Z
(GND)
(-20V DC)
OBA
IBA
OUT
IN
SEL
ERR
RUN
KSR
KSL MASTER CLEAR
KSE
KSP BXR
KSZ
KSM
STEP
SWEEP
ENTER
RUN
LOAD
BER
BFR
.001μF
MANUAL INTERRUPT -20V TO 5 OF KLS
KLS
TB115-L8M
TB115-C
TB115-E M903
TB115-K M908
TB115 H8J
M900
M901
M902
M904
M909
M850
NOTE:
KEY LOCK SWITCH (KLS) IS SHOWN IN NON-LOCK RUN POSITION. KLS IS ALSO SHOWN AS VIEWED FROM FRONT OF PANEL.
= TYPICAL LAMP DRIVER & LAMP ASSEMBLY
= INPUT TO DRIVER ONLY, NO DIODE
REFERENCE DRAWINGS
COMPONENTS (UNLESS OTHERWISE INDICATED)
TOLERANCE
VALUE
SIZE
RESISTORS
CAPACITORS
APPROVED
CHECKED
DRAWN
DESIGNED
CONTROL DATA CORPORATION
I D P DIVISION
PROJECT OR PRODUCT
8092 TELEPROGRAMMER
DRAWING NUMBER
360437
REV
D
SHT
PAGE
20
TITLE
SCHEMATIC DIAGRAM, CONTROL CONSOLE



REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

REV. APPVD. DATE SEL. REV. CHG. APPROVED

REVISIONS

APPROVED -

CHECKED -

DRAWN - 11/19/63

RELEASED -

TITLE

SCHEMATIC, POWER SUPPLY—
MODEL 8606-A

CONTROL DATA CORPORATION

I D P DIVISION

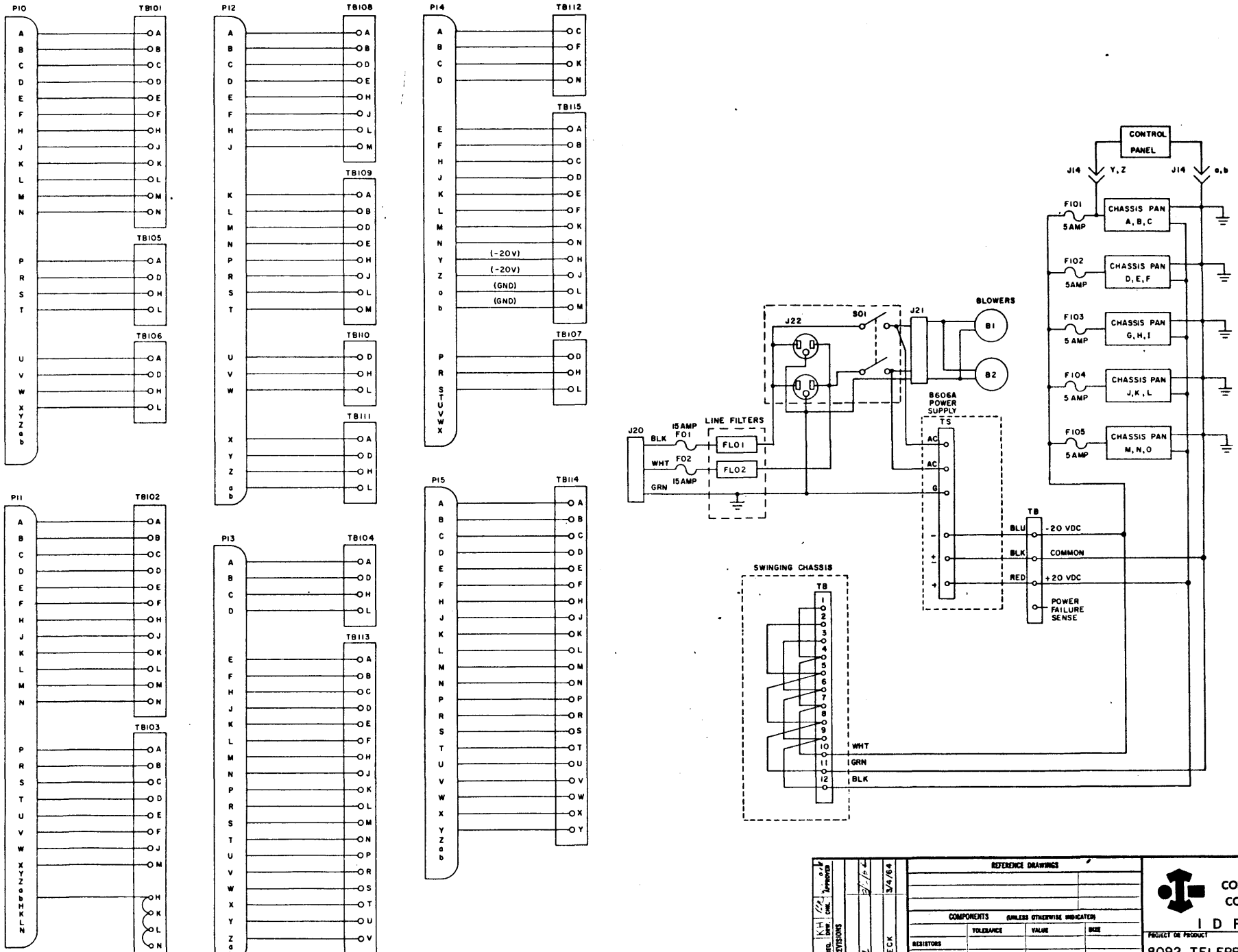
PROJECT OR PRODUCT

DRAWING NUMBER 364071

REV

SIZE

PAGE 21



REV.	AUTH.	DATE	REVISIONS	DWN.	CHK.	APPROVED
A	1585	8/5/64		KH		

DESIGNED
DRAWN J. N. K. BECK 3/4/64
CHECKED
APPROVED

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

TITLE
CABLING & AC-DC DIST

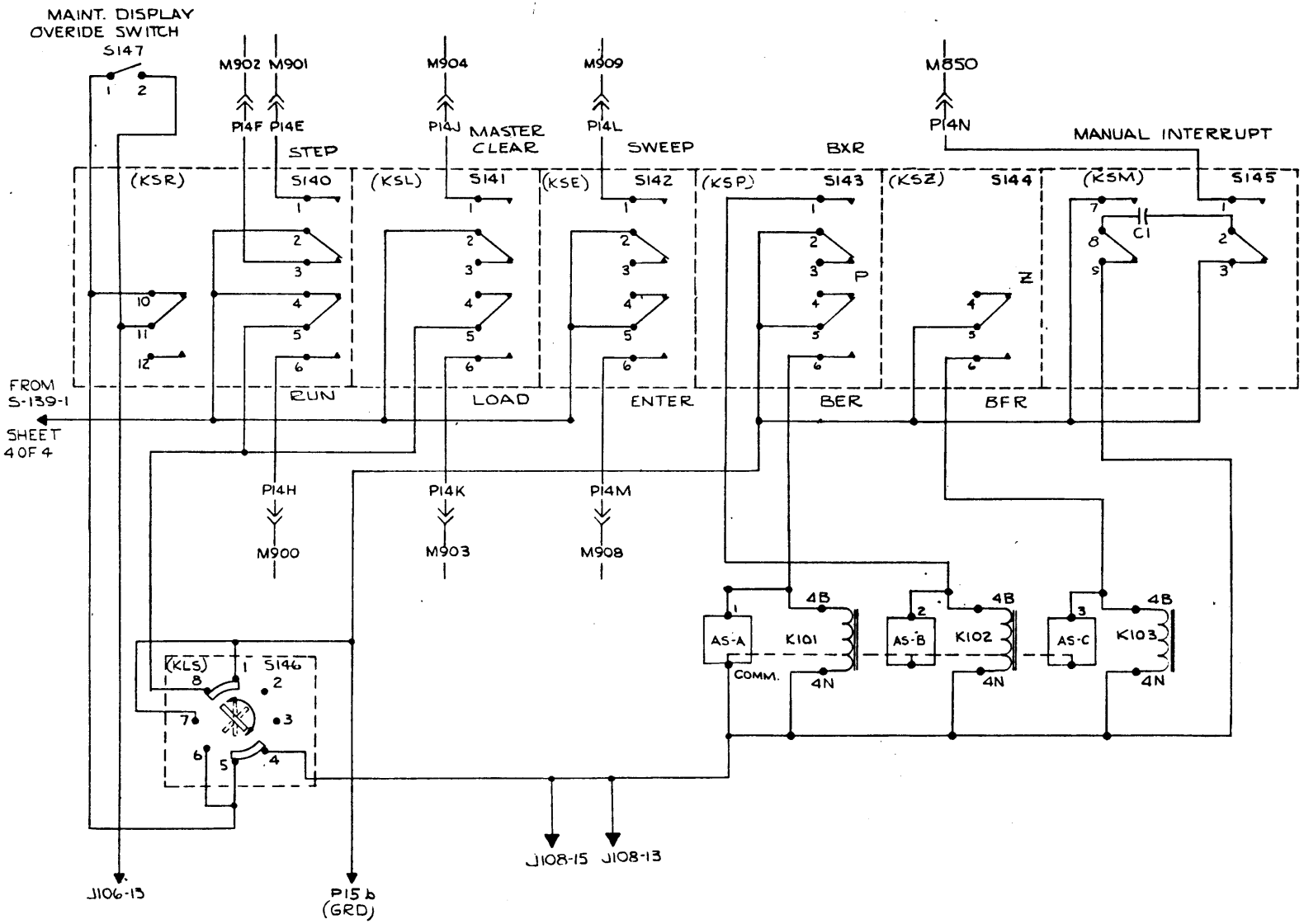
CONTROL DATA CORPORATION
I D P DIVISION

PROJECT OR PRODUCT
8092 TELEPROGRAMMER

DRAWING NUMBER 360441 REV A

SHT PAGE 22

REVISIONS							
REV.	ECO.	ZONE	DESCRIPTION	DRFT.	DATE	CHK'D	APPD.
A	—	—	RELEASED	—	[illegible]	—	[illegible]
B	20232		REVISED PER ECO	RAH	4-5-69	[illegible]	FES



2. DOTTED LINES SHOW CONNECTIONS WITHIN A CONNECTOR OR COMPONENT.
1. KEY LOCK SWITCH KLS IS SHOWN IN NON-LOCK RUN POSITION. KLS IS ALSO SHOWN AS VIEWED FROM FRONT OF PANEL.

NOTES:

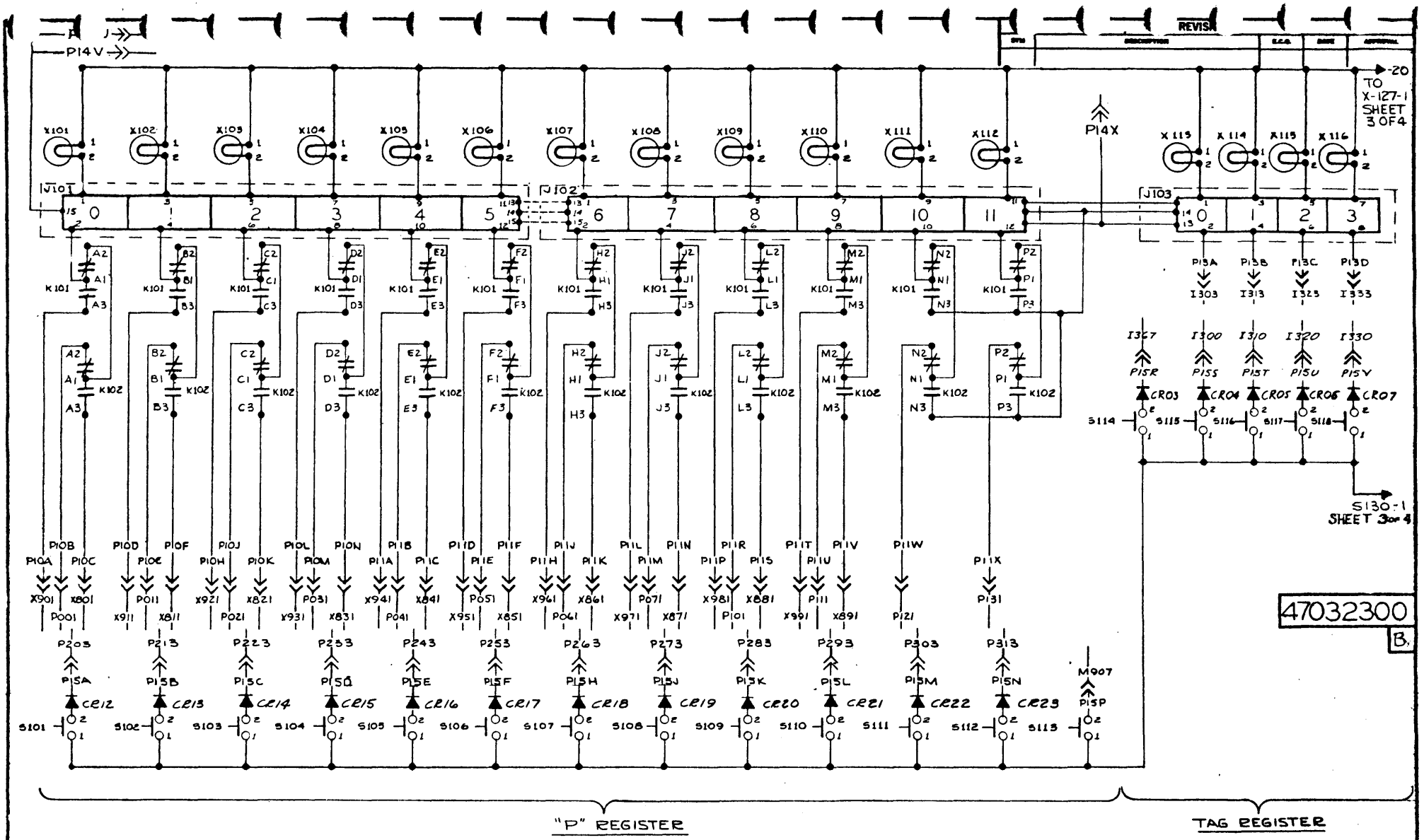
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON FRACTIONS: DECIMALS: ANGLES:
± ± ± ±
DO NOT SCALE DRAWING
MATERIAL
FINISH

CONTROL DATA CORPORATION
CEDAR ENGINEERING DIVISION
DIGITAL ENGINEERING DEPARTMENT
MINNEAPOLIS, MINNESOTA

PRODUCT	8092 DISPLAY	
DRAWN	P. Alexander	4-13-68
CHECKED	[illegible]	11-13-68
ENGINEER	[illegible]	11-13-68
APPROVED		

TITLE
SCHEMATIC DIAGRAM
8092 DISPLAY

SIZE C | DRAWING NO. 47032300 | REV B
SCALE
SHEET 1 OF 4



47032300 B.

ITEM	REQD.	PART NO.	DESCRIPTION	MATL.	MATL. SPEC.	NEXT ASSY.	USED ON	FINISH ASSY.	MFGY ASSY.

LIST OF MATERIAL — APPLICATION — QTY. REQD.

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND TOLERANCES ARE:
FRACTIONS: ±1/64 DECIMALS: (0.00) ±0.01 (0.000) ±0.005 ANGLES: ±1°
BREAK ALL EDGES AND SHARP CORNERS .010 MAX.
DIMENSIONS APPLY AFTER PLATING OR HEAT TREAT.
BURRS: NO LOOSE BURRS PERMITTED. TIGHT BURRS PERMITTED IF THEY CANNOT BE DETECTED BY NORMAL VISION OR TOUCH
SURFACE FINISH: √ ALL INSIDE SURFACES √ ALL OUTSIDE SURFACES

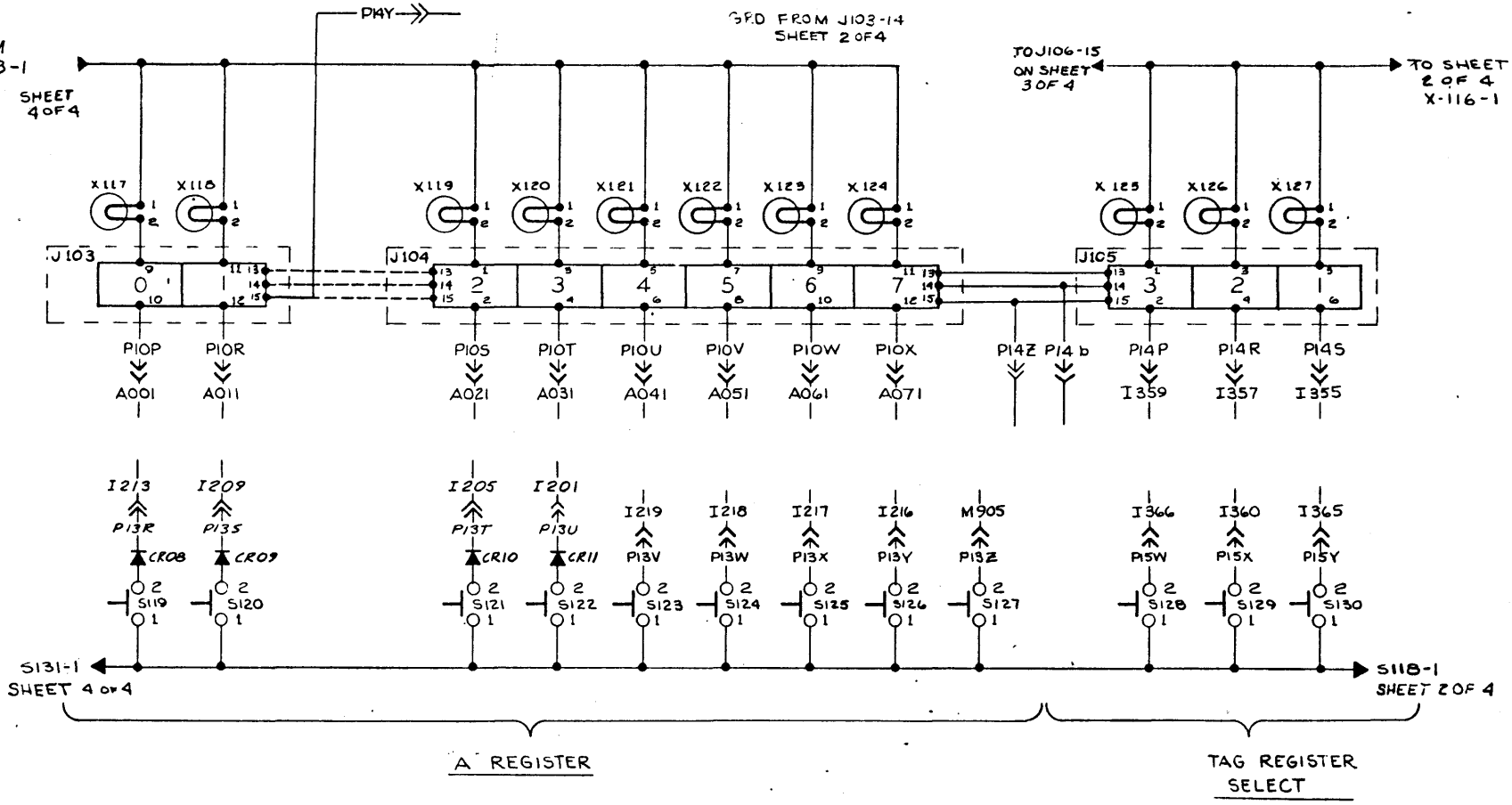
	BY	DATE
DRAWN		
CHECKED		
ENG.		
PROG.		
PROJ.		

NAME: SCHEMATIC DIAGRAM 8092 DISPLAY

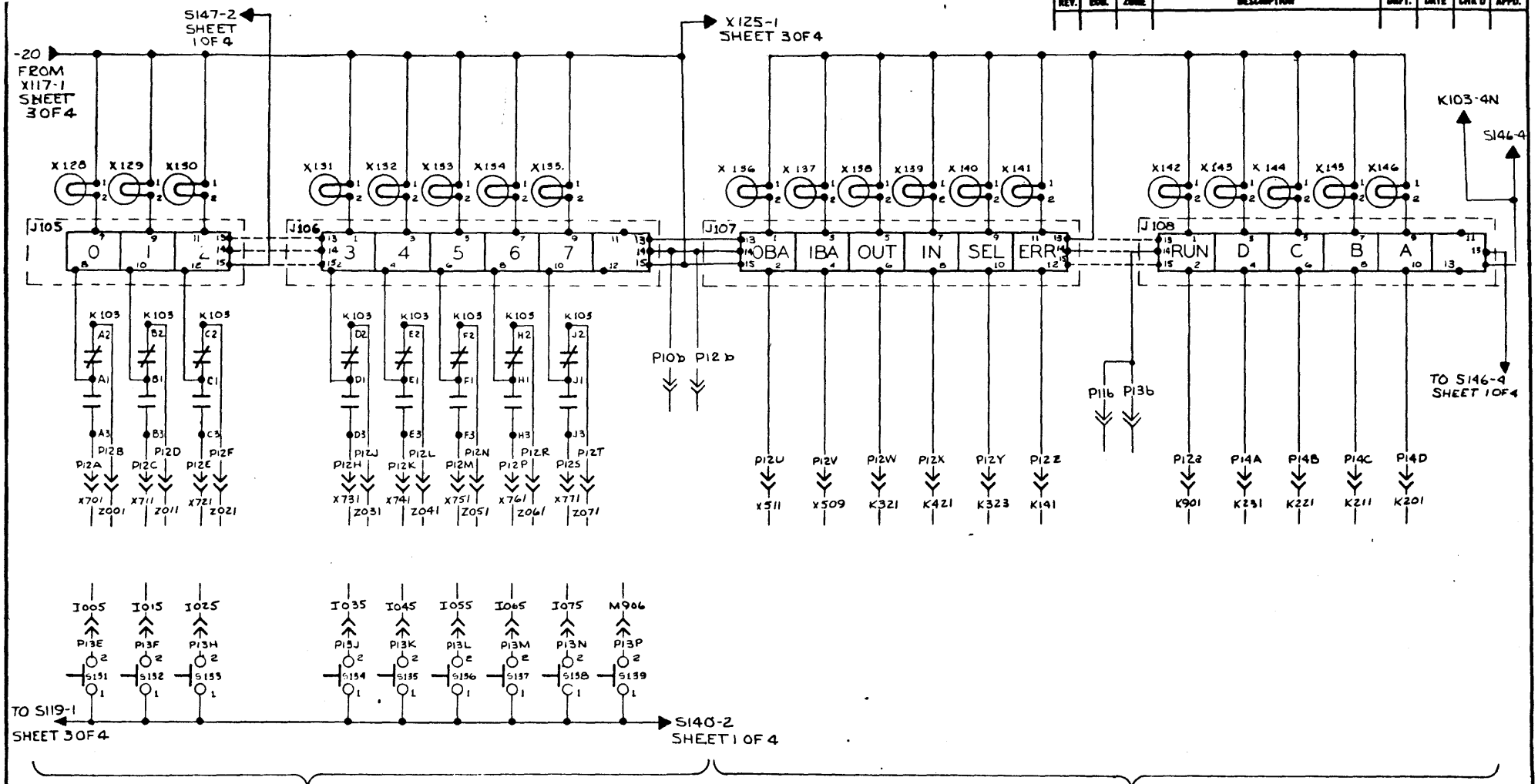
CONTROL DATA CORP.
CEDAR ENGINEERING DIVISION
8000 WEST 78th ST. MINNEAPOLIS 10, MINNESOTA

DWG. NO. 47032300
SCALE — WT. — SHEET 2 OF 4

REVISIONS							
REV.	ECO.	ZONE	DESCRIPTION	DRFT.	DATE	CHK'D	APPD.



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS: ± DECIMALS: ± ANGLES: ±	CONTROL DATA	TITLE	SCHEMATIC DIAGRAM 8092 DISPLAY
DO NOT SCALE DRAWING	CEDAR ENGINEERING DIVISION DIGITAL ENGINEERING DEPARTMENT BLOOMINGTON, MINNESOTA		
MATERIAL	PRODUCT 8092 DISPLAY	SIZE C	DRAWING NO. 47032300 REV B
FINISH	DRAWN / CHECKED / ENGINEER / APPROVED	SCALE	SHEET 3 OF 4



REV.	ECO.	ZONE	DESCRIPTION	DRFT.	DATE	CHK'D	APPD.

REVISIONS

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON FRACTIONS: ± DECIMALS: ± ANGLES: ±
DO NOT SCALE DRAWING
MATERIAL
FINISH

CONTROL DATA CORPORATION
CEDAR ENGINEERING DIVISION
DIGITAL ENGINEERING DEPARTMENT
MINNEAPOLIS, MINNESOTA

PRODUCT	8092 DISPLAY
DRAWN	
CHECKED	
ENGINEER	
APPROVED	

TITLE
SCHEMATIC DIAGRAM
8092 DISPLAY

SIZE	DRAWING NO.	REV
C	47032300	B

SCALE
SHEET 4 OF 4