CONTROL DATA® CYBER 70™ SERIES MODEL 76 COMPUTING SYSTEM

CONTROL DATA
CORPORATION

The CONTROL DATA CYBER 70 Series/Model 76 is a multipurpose computer system which provides commercial, data-management, scientific and real-time/time-critical capabilities. Model 76 contains a computation section, large and small core memories, input/output multiplexer, peripheral processor units, and a maintenance control unit.

The computation section consists of 9 arithmetic and logic function units, 24 operating registers, and a 12-word instruction stack. Functional units operate in parallel and each will handle multiple instructions simultaneously, in a segmented fashion. Segmentation time of each unit is 27.5 nanoseconds. Operating concurrently, the functional units receive operands from, and deliver results back to, the 24 operating registers. Hence, this section of the system executes an average of 15 million instructions per second. The 12 word instruction stack can hold 24 to 40 of the most current instructions. Up to 39 of these non-contiguous instructions can be executed without further references to memory for instructions.

Two types of memories have been designed into the Model 76. These are the small core memory (SCM), a very high performance, and a slower large core memory (LCM). This combination provides the access rate and storage resources required, without the costs of large, high-performance memories. Data and instructions can be transferred between the two memories at a maximum rate of one 60-bit word every 27.5 nanoseconds, or 36 million words per second.

To allow for varying system requirements, memory facilities can be configured with four different size combinations:

MEMORY (in 60-bit words)

*Model 76 — Memory Designator**	*SCM — Size*	*LCM — Size*
76 - 18	65,536	512,000
76 - 16	32,768	512,000
76 - 14	65,536	256,000
76 - 12	32,768	256,000

*Any Model 76 can be upgraded to the 76-18.

The multiplexer can have up to 15 full-duplex input/output channels, which can transfer a total of 18 million words per second. Each channel can assemble or disassemble 12-bit channel data to or from the 60-bit internal memory words. Each I/O channel has its own fixed input buffer and output buffer in SCM (normally 128 or 256 words).

Up to 13 peripheral processor units (PPU's) can be employed with the Model 76. Each PPU has its own 12-bit, 4096 word-phased memories (2 banks), and each has eight I/O channels as well as individual operating registers and an arithmetic section. The primary function of the PPU is to control, direct, and disseminate I/O data between the multiplexer and local or remote computer stations, and/or peripherals.

The maintenance control unit (MCU) is a specially-designed PPU, with the ability to control/scan all activities within the processor and memory sections of the Model 76. The MCU also includes a card reader and a cathode-ray tube visual display, with entry keyboard. Facilities are provided for on-line maintenance and diagnostic programs used in testing all sections of the system. Tests are also performed in parallel with normal system operations. The MCU detects, diagnoses, and logs all system errors — both recoverable and non-recoverable — for later statistical analysis.

Several varieties of computer stations are normally connected to the PPU's of a Model 76. Each such computer station operates under control of its own operating system, and is responsible for supporting unit-record, magnetic-tapes, and communication equipment. Data is read and written at the stations, blocked and deblocked into convenient record sizes for processing by the Model 76.

SPECIFICATIONS

CPU Computation Section:

- 60-bit internal word
- 24 operating registers
- 9 independent functional units
- 12-word instruction stack
- 15 and 30-bit instruction lengths
- Binary computation in fixed and floating point format
- Synchronous internal logic, with 27.5 nanosecond clock period
- Interrupt structure

Memory (SCM):

- 65,536 or 32,768 words of coincident current memory (60-bits plus 5 parity)
- 32 or 16 independent, phased banks
- 2048 words per bank
- 275 nanosecond read/write cycle time
- 27.5 nanosecond per word maximum transfer rate

Memory (LCM):

- 512,000 or 256,000 words of linear select memory (60-bits plus 4 parity)
- 8 or 4 independent, phased banks
- 64,000 words per bank
- 8 words read simultaneously, each reference
- 1760 nanosecond read/write cycle time
- 27.5 nanosecond per word maximum transfer rate

Input/Output Multiplexer (MUX):

- Up to 15 independent channels (asynchronous)
- Each channel full duplex
- 15 independent, 12 to 60-bit, assembly/disassembly registers
- 55 nanoseconds per 60-bit word transfer rate (MUX to SCM)

Peripheral Processor Units (PPU's):

- Up to 13 independent processors
- 4096 words of coincident current memory per PPU (12-bits plus 1 parity)
- 2 independent, phased banks/PPU
- 275 nanosecond read/write cycle time
- 8 full duplex I/O channels/PPU
- 12 and 24-bit instruction lengths
- Binary computation in fixed-point format

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