SENTINEL CHIP

Spec. No. 349-500-001
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Programmer's Model

REGISTER 0

	READ (status)	WRITE (command)
Bit 7	Tape Ready	~~Test Mode~~ Enable Interrupt
6	Operation Complete	Command Gate
5	Read Gate from tape	Tape Reset
4	Overrun error	Tape Write
3	Tape Busy	Command Bit 3
2	Tape Data Error	Command Bit 2
1	Tape Interrupt	Command Bit 1
0	Filemark	Command Bit 0

REGISTER 1

Bit 7	0	~~N/U~~ Test Mode
6	0	N/U
5	0	N/U
4	0	N/U
3	0	N/U
2	0	N/U
1	0	N/U
0	0	~~Enable Interrupt~~ Output Control

REGISTER 2

Most significant byte of transfer counter (counts down)

REGISTER 3

Least significant byte of transfer counter (counts down)

Reg. 3 must be written before Reg. 2.

Writing Reg. 2 resets any outstanding request from previous aborted command.

REGISTER 0, READ STATUS

Bit 7 - Tape Ready

This is a direct input from the Sentinel tape drive. It indicates power on and cartridge ready. Read Sense and Device Health Check commands may be issued to determine if power is indeed off when Tape Ready is not present.

In loop-back mode this is the Write Gate signal which is internally generated to envelope write data.

Bit 6 - Operation Complete

This is an internally generated status which indicates completion of a tape command. Its operation is as follows:

1) System reset sets operation complete.
2) Command Gate resets operation complete.
3) Trailing edge of Tape Busy after a command acknowledge sets operation complete.
4) Transfer of last byte of write data sets operation complete.

In loop-back mode this status is generated as above except that the Tape Busy signal is internally generated from Command Bit 3.

Bit 5 - Read Gate

This is the Read Gate signal from the tape which envelopes the read data.

In loop-back mode this signal is internally generated from Command Bit 2.

Bit 4 - Overrun Error

This is an internally generated status which indicates that the data transfer did not complete successfully because a memory cycle was not obtained in time for a transfer to or from memory to be completed.

This status bit is reset by writing to register 0.

This status bit is not altered by the loop-back mode.

Bit 3 - Tape Busy

This is a direct input from the Sentinel tape drive. It indicates that the tape is performing some operation. A command will not be acknowledged while Busy is on. The trail-

ing edge of Busy causes the setting of the Operation Complete status.

A Busy generated by the Sentinel because of a reposition operation should present no problem since the Operation Complete status is forced reset until a Command Acknowledge is received to reset the Command Gate.

In loop-back mode this signal is internally generated from Command Bit 3.

Bit 2 - Tape Data Error

This is a direct input from the Sentinel tape drive. It indicates that a data error was detected by the tape electronics and that error recovery must be performed by the controller.

In loop-back mode this signal is internally generated from Command Gate.

Bit 1 - Tape Interrupt

This is a direct input from the Sentinel tape drive. It indicates that an abnormal condition occurred. A Read Sense command must be issued.

In loop-back mode this signal is internally generated from the Write Data.

Bit 0 - File Mark Detected

This is a latched status signal generated from the File Mark Detected pulse from the Sentinel tape drive. It indicates that a file mark was detected by the read operation.

This status will be reset by assertion of Command Gate. It can not be reset until the removal of the Tape Busy signal because the Tape File Mark Detected remains on for some length of time less than Busy.

In loop-back mode the Command Bit 0 signal is used to set this status. It is still reset by Command Gate.

REGISTER 0, WRITE COMMAND

Bit 7 - Test Mode

If this bit is set the device is placed in a loop-back mode in which signals which are normally outputs are instead fed back inside the device as if they replaced inputs. The actual outputs will not be asserted while in loop-back mode so that this mode may be used for diagnostic purposes without effecting tape operation.

The effect of this mode is identical to what would occur if, in the normal operating mode, the outputs were connected to the inputs as follows:

OUTPUT	(looped to)	INPUT
Tape Reset		Command Acknowledge
Command Gate		Tape Data Error
Command Gate		Data Clock
Command Bit 3		Tape Busy
Command Bit 2		Read Gate
Command Bit 1		Read Data
Command Bit 0		Tape File Mark Detected
Write Gate		Tape Ready
Write Data		Tape Interrupt

Bit 6 - Command Gate

This bit signals the Sentinel tape drive that a command is to be initiated. The command is specified by Command Bits 3 t 0. The Command Gate is reset by the Command Acknowledge input from the Sentinel. It may also be reset by writing a zero to it.

In loop-back mode this signal becomes the Data Error status signal and is also used as the clock for read or write test data. In loop-back mode it is reset from the Reset signal which is looped to become Command Acknowledge.

Bit 5 - Tape Reset

This bit causes the reset of the Sentinel tape drive. It must be asserted for at least 4 microseconds but no more than 25 microseconds.

In loop-back mode this signal generates Command Acknowledge to reset Command Gate.

Bit 4 - Tape Write Operation

This signal is used internally to activate the write data sequencing. The microprocessor should set this bit only when issuing the Write command to the Sentinel. When Tape Busy is asserted the write sequencer will generate Write Gate.

In loop-back mode this signal is used to activate the write data sequencing to generate (when Command Bit 3 is on) the Write Gate signal which is looped to Tape Ready.

Bits 3 to 0 - Command Bits 3 to 0

These are the four command bits which identify the operation to be performed by the Sentinel when a Command Gate is sent. The command bits pass directly out to the Sentinel without affecting internal operations.

In loop-back mode these signals become, respectively, Tape Busy, Read Gate, Read Data and Tape File Mark Detected.

REGISTER 1, WRITE

Bit 0 - INTERRUPT ENABLE

This bit, if a one, enables the interrupt request from the device to the microprocessor. The interrupt condition is the Operation Complete status.

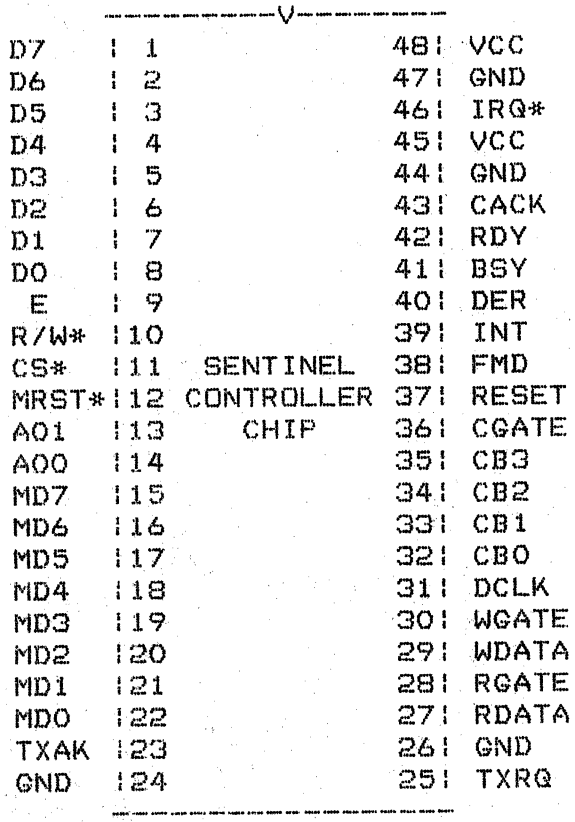
REGISTERS 2 and 3, BYTE COUNTER

These registers (2 is most significant) are a 16-bit loadable down counter which is decremented on each data transfer to or from memory.

When performing a read operation the counter will be decremented by the number of bytes read. If initially zero it will contain the two's complement of the number of bytes transferred on completion of the read. A decrement to zero will not stop the data transfer for a read.

When performing a write operation the counter will be decremented to zero. When the last byte is transferred to the internal buffer the counter decrements from one to zero causing the write sequencer to alter its operation to transfer the final data bits and remove Write Gate.

PINOUT


D7 1
D6 2
D5 3
D4 4
D3 5
D2 6
D1 7
D0 8
E 9
R/W* 10
CS* 11
MRST* 12
A01 13
A00 14
MD7 15
MD6 16
MD5 17
MD4 18
MD3 19
MD2 20
MD1 21
MD0 22
TXAK 23
GND 24
48 VCC
47 GND
46 IRQ*
45 VCC
44 GND
43 CACK
42 RDY
41 BSY
40 DER
39 INT
38 FMD
37 RESET
36 CGATE
35 CB3
34 CB2
33 CB1
32 CB0
31 DCLK
30 WGATE
29 WDATA
28 RGATE
27 RDATA
26 GND
25 TXRQ
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D7, D6, D5, D4, D3, D2, D1, D0 - PINS 1-8:

These are the microprocessor data bus connections. Control and status registers are accessed over this bus. D7 is the most significant bit.

MD7, MD6, MD5, MD4, MD3, MD2, MD1, MD0 - Pins 15-22:

These are the memory data bus connections. Data transfers occur over this bus. In a single bus microprocessor design the two data buses may be tied together. MD7 is the most significant bit.

E - Pin 9:

This is the enable clock signal from the microprocessor which indicates valid control signals on the R/W*, CS*, A01, and A00 pins. It is used internally to enable output drivers for the microprocessor data bus if R/W* is high and CS* is low or to load an internal register from the microprocessor data bus if R/W* is low and CS* is low.

R/W* - Pin 10:

This control signal determines the direction of data transfer on the microprocessor data bus. A high indicates a transfer from the chip; a low indicates a transfer to the chip. This signal is gated internally with E and CS* to generate an output enable and internal write clocks. Data will be written to the command register when the earlier of R/W* going high, E going low or CS* going high occurs.

CS* - Pin 11:

This is the chip select signal. It is used to qualify the E and R/W* signals and is intended to be an address decode.

A01, A00 - Pins 13,14:

These two lines provide a register address for the chip. The register address decodes are:

A01	A00	Register
0	0	Read status, write command
0	1	Write interrupt enable
1	0	Most significant byte of transfer counter
1	1	Least significant byte of transfer counter

MRST* - Pin 12:

If this signal is brought low the command register is cleared and the COMPLETE status is set. The interrupt enable is not cleared. The transfer counter is unaltered. The RESET signal to the Sentinel will not be asserted.

IRQ* - Pin 46:

This is an open drain interrupt request output. It is low when the COMPLETE status is set and the interrupt enable bit has been set.

TXRQ - Pin 25:

This output signal is used to request a memory data transfer. The request signal will be removed by an acknowledgement.

TXAK - Pin 23:

This input signal acknowledges a memory data transfer. Data out will be valid during the acknowledge. Data will be latched internally at the trailing edge of the acknowledge.

CACK, RDY, BSY, DER, INT, FMD - Pins 43-38:

These are inputs from the tape drive. CACK is command acknowledge which resets command gate. RDY, DER and INT are part of the status register. BSY is in the status register and is used to set the COMPLETE status and generate Write Gate. FMD is latched internally to generate the file mark detected status.

RESET - Pin 37:

This output to the tape drive causes a drive reset. No internal logic is provided to limit its output to the 4 microsecond to 25 microsecond range; this must be done by the microprocessor.

CGATE - Pin 36:

This output indicates that a command is being presented on the Command Bits. It is reset by a Command Acknowledge (CACK).

CB3, CB2, CB1, CB0 - Pins 35-32:

These are the Command Bits. They are not internally decoded for any purpose. They are defined by the Sentinel specification as follows:

CB3	CB2	CB1	CB0	Command
0	0	0	0	Not used
0	0	0	1	Device health checks
0	0	1	0	(Reserved for future use)
0	0	1	1	Read Sense
0	1	0	0	Read
0	1	0	1	Search file mark
0	1	1	0	Read file
0	1	1	1	Backspace
1	0	0	0	Write
1	0	0	1	Write file mark
1	0	1	0	Cartridge health check
1	0	1	1	Erase
1	1	0	0	(Reserved for future use)

1	1	0	1	Rewind
1	1	1	0	Restore
1	1	1	1	(Reserved for future use)

DCLK - Pin 31:

This is the drive supplied data clock. Read data is latched by the trailing edge of this clock. Write data is shifted by the trailing edge of this clock.

WGATE - Pin 30:

This output envelopes the Write Data. It is generated from the Write bit of the command register and the BSY input from the tape drive. It is removed to indicate the last data bit shortly after the last DCLK.

WDATA - Pin 29:

This is the bit serial data to be written to the tape. Write data is changed following the trailing edge of DCLK.

RGATE - Pin 28:

This is the input from the drive which envelopes the Read Data. It is used to activate the read sequencer in the controller chip which generates memory requests.

RDATA - Pin 27:

This is the bit serial data read from the tape. Read data is sampled while DCLK is high and latched at the trailing edge of DCLK.