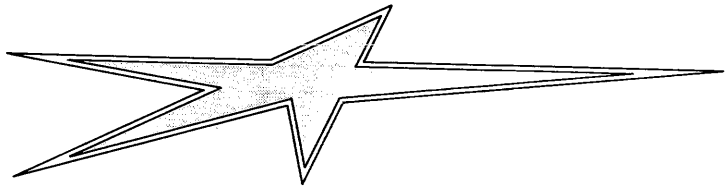
CONTROL DATA
CORPORATION



CONTROL DATA® STAR PERIPHERAL STATIONS
PAGING (DRUM) STATION
HIGH CAPACITY DISK STATION
SERVICE STATION
844 STORAGE STATION
MAGNETIC TAPE STATION
UNIT RECORD STATION
DISPLAY/EDIT STATION
STAR-1B SERVICE STATION
STAR-100 SERVICE STATION
STORAGE (MEDIA) STATION
STAR-100 MAINTENANCE CONTROL UNIT
STAR-65 MAINTENANCE CONTROL UNIT

HARDWARE REFERENCE MANUAL

NOTICE

ALL REFERENCES IN THIS MANUAL TO CAPABILITIES/ PERFORMANCE OF THE STAR STATIONS AND ASSOCIATED PERIPHERAL DEVICES ARE NOMINAL VALUES AND MAY IN SOME CASES BE THE MAXIMUM CAPABILITIES OF THE DEVICES. THE ACTUAL CAPABILITIES ENCOUNTERED IN A SYSTEM ARE DEPENDENT ON THE PARTICULAR HARDWARE AND SOFTWARE CONFIGURATION USED.

REVISION RECORD

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	2-25, 2-86, 2-117, 2-157, 3-10, 3-37, A-1 through A-59 (revised and renumbered), C-3, C-4,
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	2-67, 2-68, 2-70, 2-71 through 2-74, 2-82, 2-84, 2-85, 2-87, 2-88, 2-89, 2-91 through
	2-106, 2-108, 2-109, 2-110, 2-112, 2-113, 2-114, 2-120, 2-128, 2-135, 2-136, 2-137,
	2-146, 2-147, 2-152, 2-155, 2-156, 2-157, 2-165, 3-1, 3-3, 3-8, 3-9, 3-10, 3-13, 3-17,
	3-19, 3-20, 3-21, 3-28, 3-29, 3-31, 3-33, 3-34, 3-35, 3-38, 3-40, 3-46, 3-48, 3-51
	through 3-56, 3-60, 3-62, 3-68, 3-69, 3-79, 3-94 through 3-100, 3-103, 3-104, 3-105,
	4-1, 4-15, 5-1, 5-6, 5-8, A-1 through A-9, A-11, A-14 through A-19, A-22, A-23, A-24,
	A-27, A-30 A-31, A-32, A-34, A-46 through A-51, A-54, A-55, A-57, A-63 through A-66,
	A-70 through A-79, B-2 through B-9, C-1 through C-4, C-9 through C-15. Add the follow-
	ing pages: 1-55 through 1-59, 2-94.1 through 2-94.3, 3-106 through 3-109, 5-9 through 5-21,
	A-81 through A-90.
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	2-15, 2-16, 2-17, 2-20 through 2-23, 2-32, 2-39, 2-40, 2-43 through 2-48, 2-52, 2-63
	through 2-68, 2-70, 2-74, 2-80, 2-81, 2-90 through 2-94.3, 2-97, 2-104, 2-105, 2-119,
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PREFACE

This manual contains reference information for the system functions of the CONTROL DATA® STAR Peripheral Stations, descriptions of the station hardware, and some typical procedures necessary to exercise the programmable elements. The STAR stations are a set of peripheral equipment designed for use with a CDC® STAR 100 Computer, and as such, are implemented to some degree by common hardware and software. Other stations may be used in a STAR peripheral system; manuals providing information on this equipment are listed in this preface.

NOTE

Throughout this manual, the abbreviations NOC and NIC denote normal output channel and normal input channel, respectively. As an example of its use in text, the notation NOC-5 indicates normal output channel 5.

Control Data Publications	Publication No.
†STAR-100 Computer Reference Manual	60256000
†STAR-100 Computer Hardware Maintenance Manuals: General Description, Operation, Theory of Operation, Installation and Checkout, Maintenance	60256100
Control Data Large and Medium Scale Computer Systems Site Preparation Manual Section 1 - General Information	60275100
Control Data STAR-100 Computer System Site Preparation Manual Section 2 - System Data	60381600
†STAR-100 Computer Refrigeration System Customer Engineering Manual	60329800
†STAR-100 Peripheral Stations Customer Engineering Manual (Maintenance)	60325300
STAR-100 Peripheral Stations Customer Engineering Diagrams Manuals	
†Station Buffer Unit Core Control	60382000 and 60406700
†Station Buffer Unit Interfaces	60382100 and 60406800
†Station Control Unit	60362900
†Station Display Unit	60382500

†This manual is available on a controlled distribution basis only from:
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All manuals not having the dagger are available from:
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Minneapolis, Minn. 55440

Control Data Publication	Publication No.
FR101B Buffer Controller Reference Manual	60275000
3000 Series Computer Systems I/O Specifications Manual	60048800
7600/CYBER 70 Model 76 Computer Systems I/O Specifications	60408700
Buffer Controller Maintenance Console Customer Engineering Manual (TF201-A03)	58032700
Buffer Controller Maintenance Console II Customer Engineering Manual (TF204-A01)	59344000
CC102-A Display Station Reference/Customer Engineering Manual	82160600
CC601-A/B Display Station Reference/Customer Engineering Manual	82134300
CA115-A Entry Keyboard Reference/Customer Engineering Manual	82160700
405 Card Reader Reference/Customer Engineering Manual	40809300
3649-A Card Reader Controller Reference/Instruction Manual	60097900
415 Card Punch Maintenance Manual	40819600
512-1 Line Printer Reference/Customer Engineering Manual	44980100
3555-1 Line Printer Controller Reference Manual	60231300
HR-600 Line Printer Customer Engineering Manual	44983100
657-1, 2, 3, 4 Magnetic Tape Transports Reference/Customer Engineering Manual	70600200
659-1, 2, 3, 4 Magnetic Tape Transports Reference/Customer Engineering Manual	70601000
841 Multiple Disk Drive Maintenance Manuals	41243500
844 Disk Storage Unit Customer Engineering Manual	70629500
854 Disk Storage Drive Maintenance Manual	41245800
865 Drum Storage Unit Customer Engineering Manual (Modified 865)	60320900
High Capacity Disk Subsystem	60428700
3446-A/B Card Punch Controller Reference Manual	60332100
3447-A Card Reader Controller Reference Manual	60332300
3528 Magnetic Tape Controller Reference Manual	60287600

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FIGURES

FIGURES

TABLES

TABLES

STAR PERIPHERAL STATION INTERFACE CONFIGURATION CHART

	Station / Type of Interface	Paging (Drum) Station	Storage (Media) Station	844 Storage/ Magnetic Tape Station	844 Service Station	STAR 100 Service Station	STAR 1B Service Station	HCD Station	Unit Record Station	Display/ Edit Station	STAR 100 Maintenance Control Unit	STAR 65 Maintenance Control Unit
SCU Interfaces	Microdrum	1	1	1	1	1	1	1	1	1	1	1
	Keyboard	1	1	1	1	1	1	1	1	1	1	1
	CRT	1	1	1	1	1	1	1	1	1	1	1
	SBU Coupler	1	1	1	1	1	1	1	1	1	2	2
	Normal Channels	1	1	1	1	1	1	1	1	1	1	1
	SCU Gate	1	1	1	1	1	1	1	1	1	1	1
	SDU Coupler									1		
	3000 SCU								2		1	1
	854 SCU										1	1
	HR 600										1	1
	Normal Channel Switch										1	1
	STAR-100										1	
	STAR-65											1
SBU Interfaces	3000 I/O		2	2								
	7000 I/O	2				1		2				
	841 MDD		2				2					
	844 DSD			2	1							
	STAR A Data Chans				4	8	6					
	SAC Coupler	1	2	2	2	2	2	2				
	Communication Network Trunk				2							
	Index Compare	1					1					

GENERAL DESCRIPTION 1

GENERAL

Section 1 contains an introduction to the CDC STAR Peripheral Stations. It includes a description of each station and its function, a brief description of each functional element within the station, and a physical description of the station hardware.

PERIPHERAL STATION/COMPUTER SYSTEM OVERVIEW

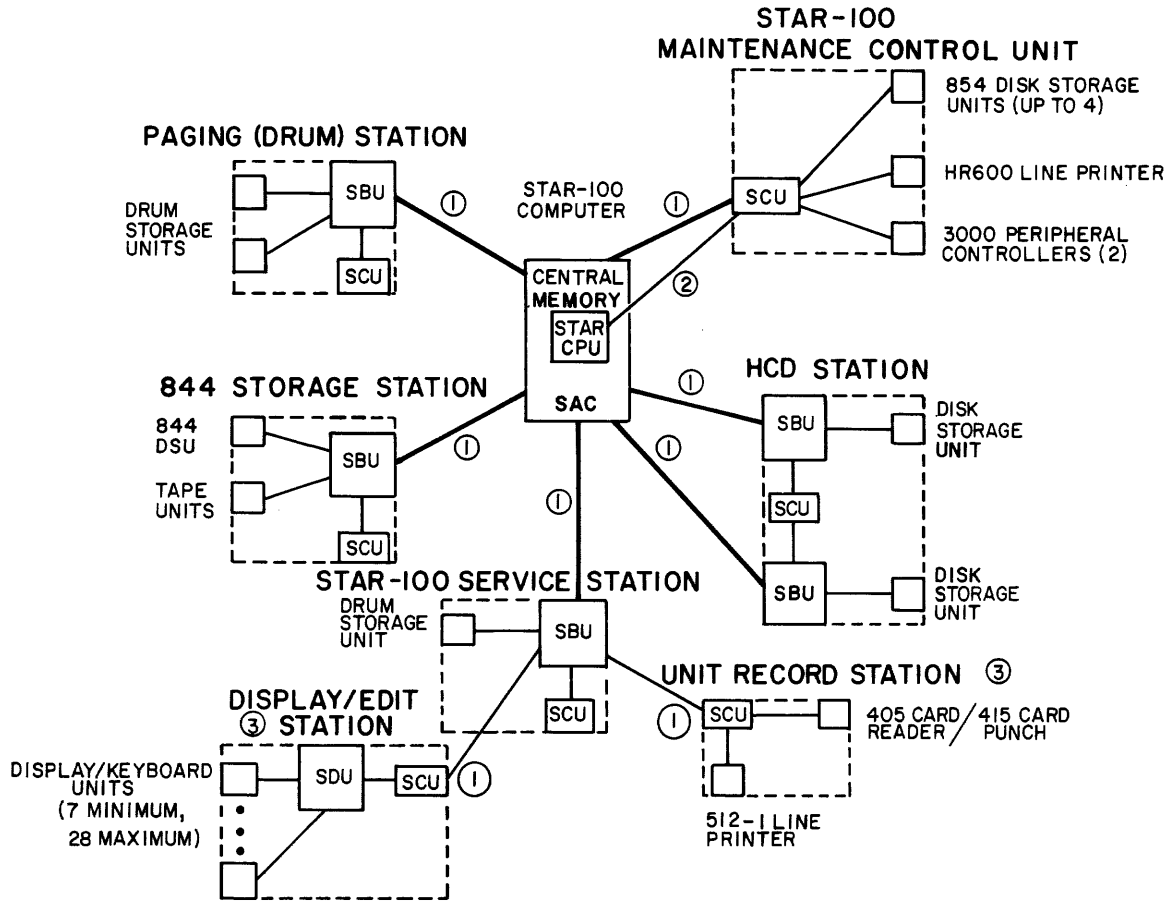
Peripheral stations perform such tasks as detailed control of peripheral equipment, recovery and retransmission of corrected data, manipulation of records and messages as to timing and routing, and the general management of available peripheral resources.

The standard peripheral stations available to handle I/O tasks in STAR computer systems are:

- Paging (Drum) Station
- High Capacity Disk (HCD) Station
- 844 Service Station
- STAR-100 Service Station
- STAR-1B Service Station
- 844 Storage Station
- Magnetic Tape Station
- Unit Record Station
- Display/Edit Station
- Storage (Media) Station
- STAR-100 Maintenance Control Unit
- STAR-65 Maintenance Control Unit

Figure 1-1 illustrates the relationships of some of these standard stations to the central processor and the memory of a STAR-100 Computer.

Peripheral stations are classified as first level or second-level stations according to the position they occupy in the overall system hierarchy. This hierarchy is physical as well as logical in that an I/O data stream is staged twice from second-level stations and once from first-level stations on the way into and out of the STAR central processor. This procedure is necessary since many of the I/O operations usually required of the central processor have been reassigned to one or more levels in the hierarchy. First-level stations connect directly to central memory through STAR storage access control (SAC). Second-level stations (Figure 1-1) communicate indirectly with central memory through a first-level service station. The first-level service station acts as a concen-



NOTES:

① DENOTES STAR DATA CHANNEL

② DENOTES SPECIAL MONITOR/CONTROL LINES TO/FROM STAR CPU

③ DENOTES SECOND-LEVEL STATIONS

CPU = CENTRAL PROCESSING UNIT
SBU = STATION BUFFER UNIT
SCU = STATION CONTROL UNIT
SDU = STATION DISPLAY UNIT
DSU = DISK STORAGE UNIT
HCD = HIGH CAPACITY DISK
SAC = STORAGE ACCESS CONTROL

Figure 1-1. Typical System Configuration, STAR Peripheral Stations

The SBU is basically a 32K- 16-bits per word-core memory with the peripheral interfaces that allow I/O devices to transfer data directly into or out of memory. Control lines from the SCU are used to activate and monitor the various peripheral interfaces. In many cases, several peripheral interfaces can transfer data concurrently. To transfer a block of data to the central processor memory from an I/O peripheral device, the data is first stored in SBU memory and then transferred to central memory via a STAR data channel. Similarly, to transfer a block of data to an I/O device, data is first stored in SBU memory and then transferred to the proper I/O device.

Differences in the varieties of SCUs and SBUs used in the various stations occur primarily in the peripheral interface areas.

STATION CONFIGURATIONS

Figures 1-4 through 1-16 illustrate the major components in each station and methods of interconnection between peripheral equipment and SBUs.

NOTE

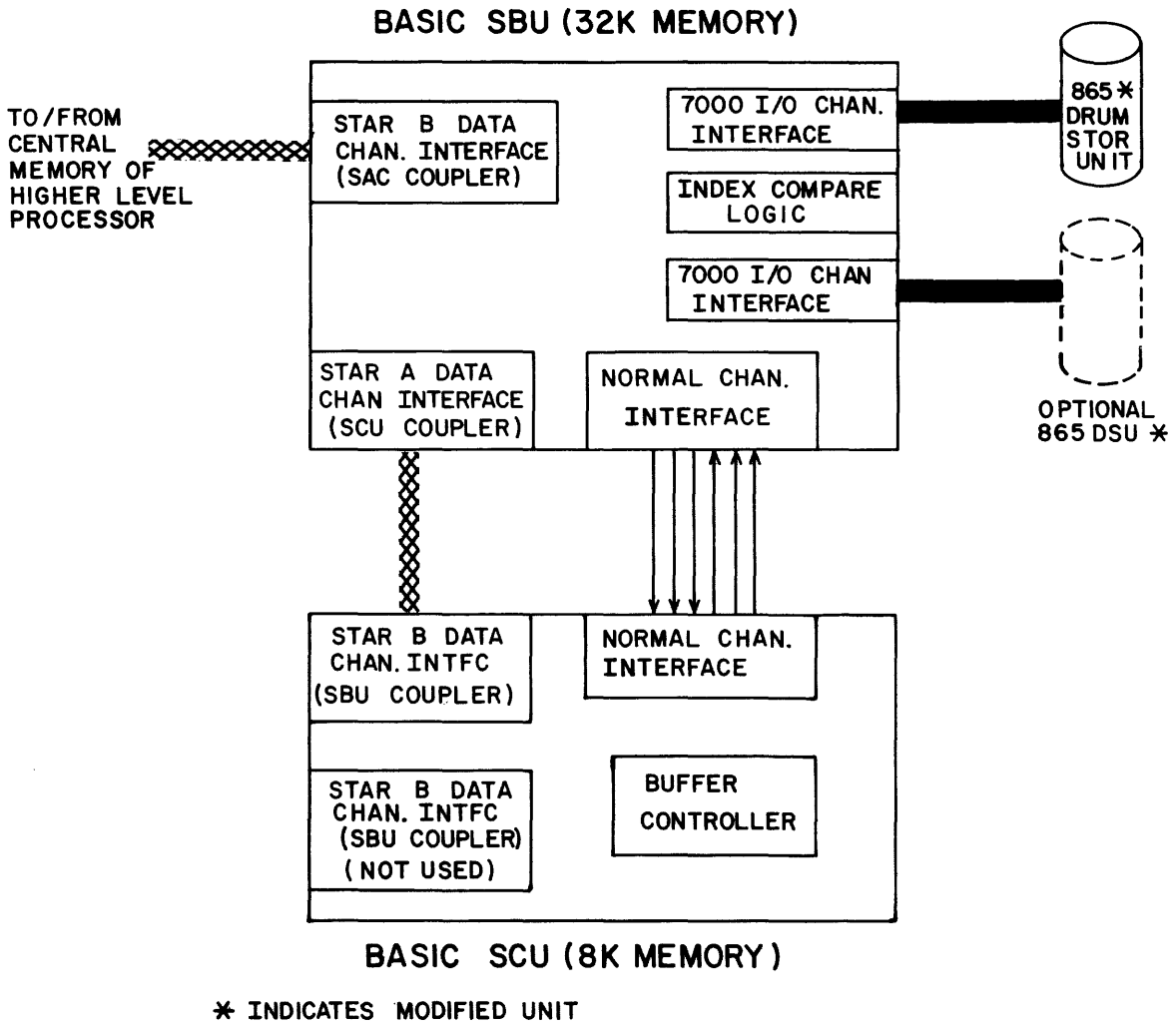
The following illustrations contain A and B data channel interfaces, which are elements associated with the STAR data channel and are explained in detail in pub. no. 60429400.

Also, the term peripheral A interface is used to differentiate the logic connected to the B interfaces of other stations from the A interface which connects to the B interface in the SCU.

STATION DESCRIPTIONS

The following paragraphs describe the functions and logical configurations (building blocks) of the various stations and their interfaces. Most of these building blocks are used in more than one station. The Configuration Chart preceding section 1 lists the types and quantities of interfaces in each station. Figures 1-4 through 1-16 illustrate their relationship in each station.

Since the basic SBU and SCU are both common to many stations, a general discussion of each follows Figure 1-16 and precedes the station descriptions.



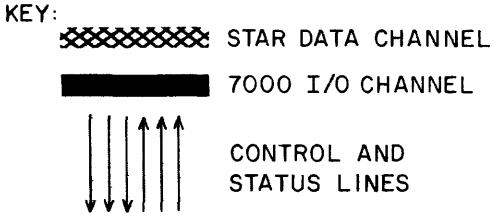


Figure 1-4. Paging (Drum) Station, Typical Configuration

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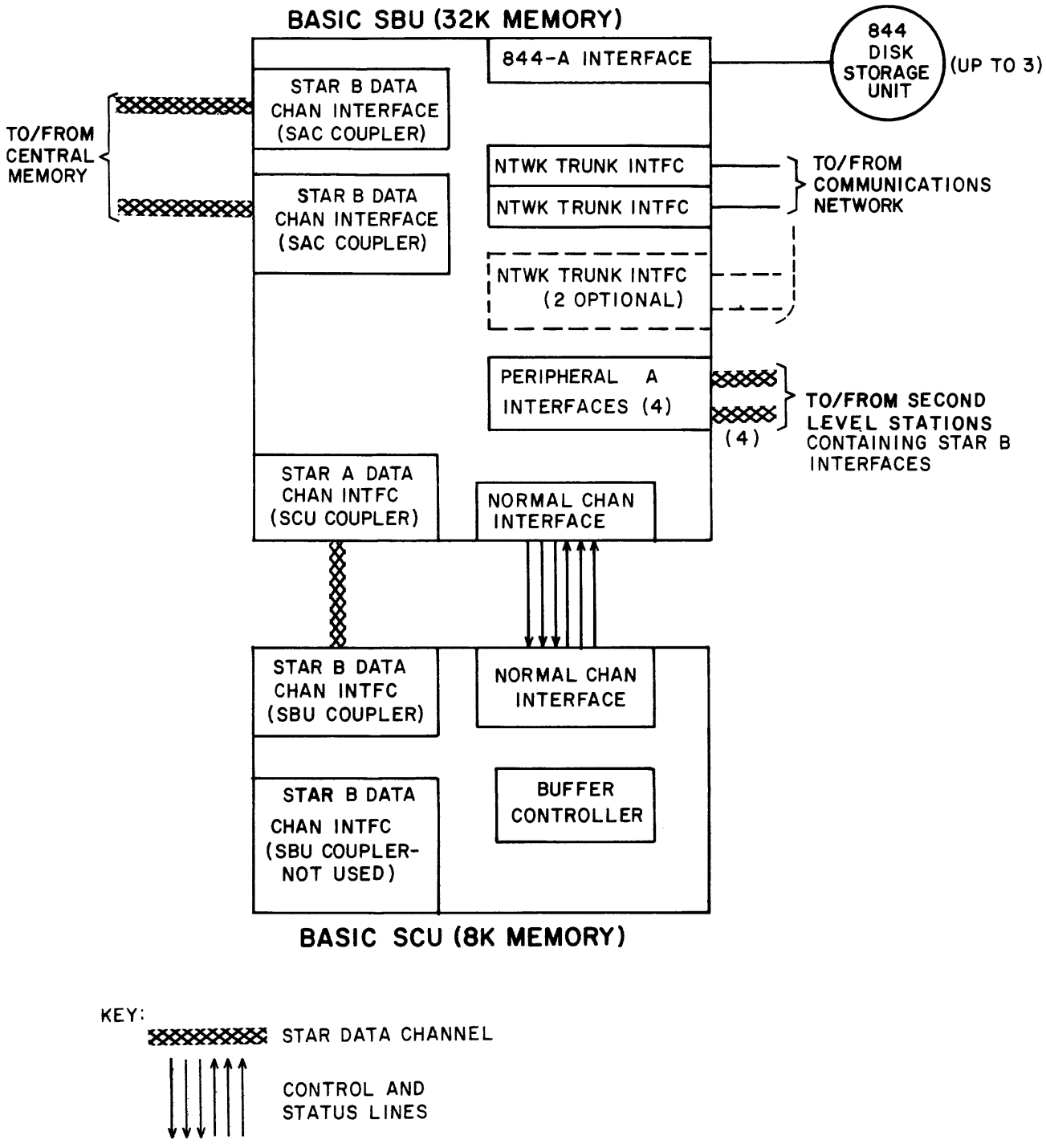


Figure 1-6. 844 Service Station, Typical Configuration

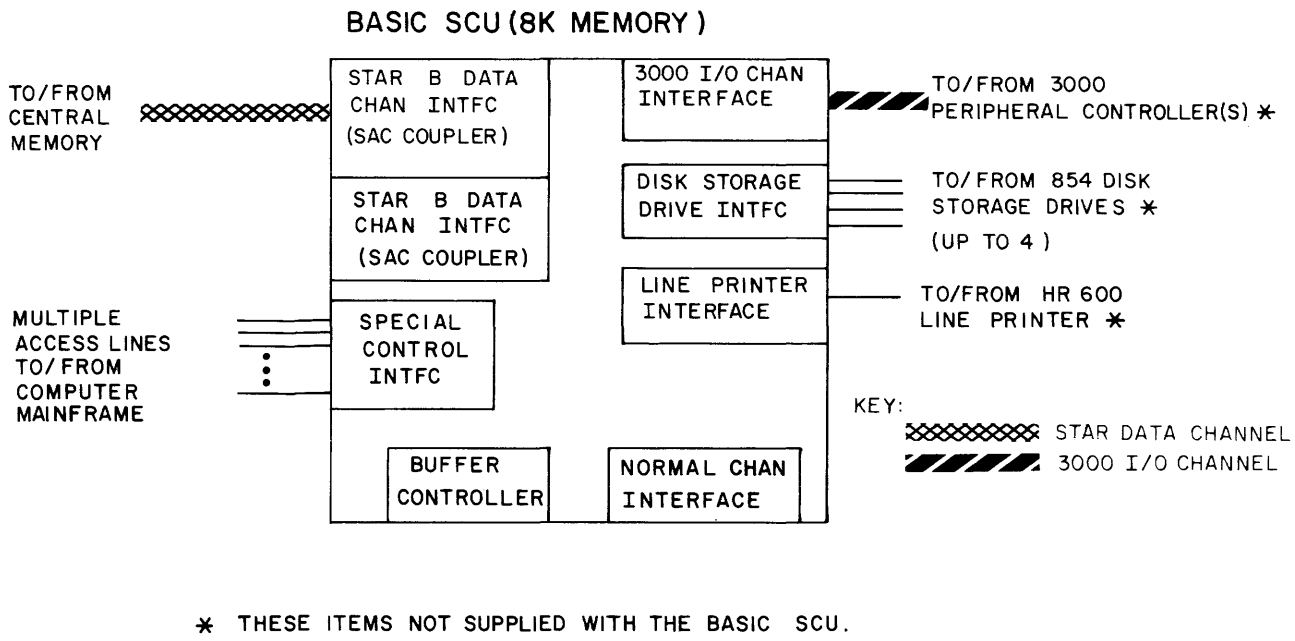


Figure 1-15. STAR-65 Maintenance Control Unit, Typical Configuration

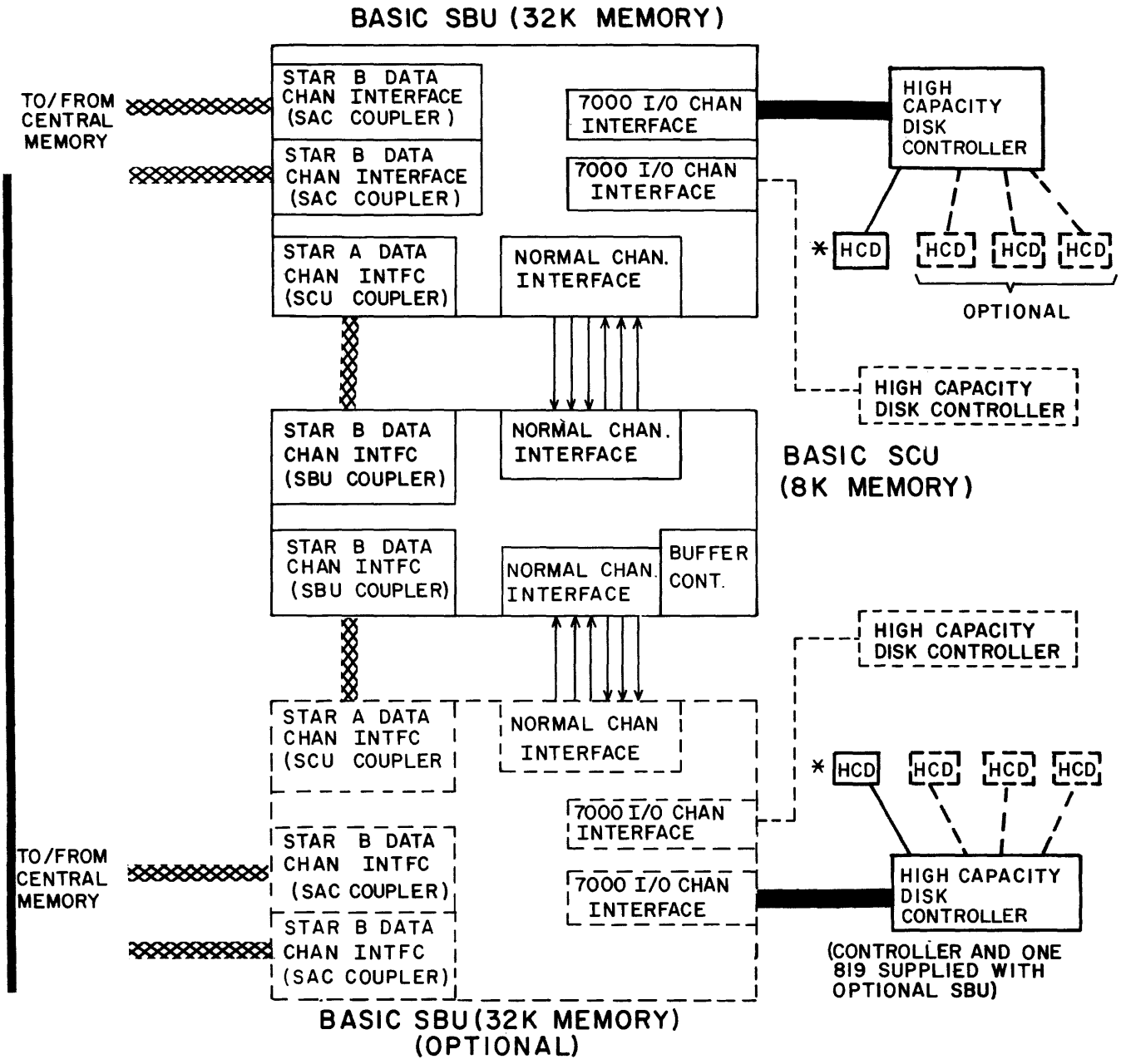


Figure 1-16. High Capacity Disk (HCD) Station, Typical Configuration

STATION BUFFER UNIT

The SBU (Figure 1-17) consists primarily of core memory for intermediate storage of data between the STAR-100 CPU and peripheral devices or other peripheral stations. It also contains core control logic which provides 12 access points in and out of core memory for the various peripheral interfaces. This core memory contains 32,768 16-bit words organized into eight phased banks. The cycle time of each bank is 1.1 microseconds.

Typically, the SBU is used for transferring large amounts of data at high speeds, staging of files and jobs, temporary storage of data and messages, and expansion of the system to subordinate level stations. Therefore, the SCU is relieved of heavy data transfer tasks and is available for higher level control activities even though it controls the SBU and monitors all of its data flow. The SBU is treated as an external memory by the SCU and is not directly addressable by the BC within the SCU. Each functional section within the SBU is discussed in the order listed.

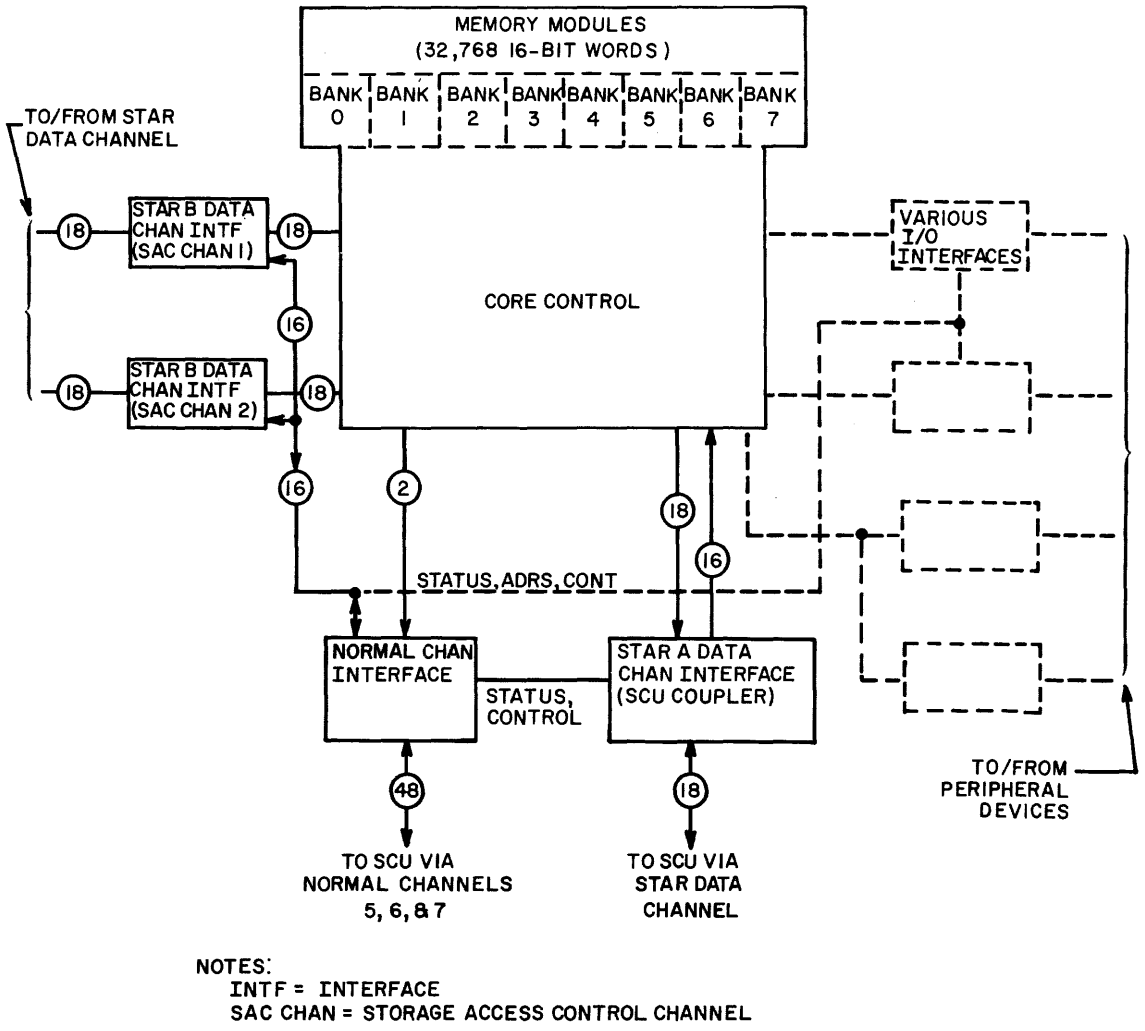
- STAR A data channel interface (SCU coupler)
- STAR B data channel interface (SAC coupler)
- Normal channel interface
- Core control
- Various I/O interfaces

STAR A DATA CHANNEL INTERFACE (SCU COUPLER)

The STAR A data channel interface provides a connection between an access to SBU core and an SCU via the STAR data channel. The A data channel interface is passive, with transfer, control, and initiation being directed by the STAR B data channel interface (active end).

STAR B DATA CHANNEL INTERFACE (SAC COUPLER)

The STAR B data channel interface provides the connection between an access to SBU core and a STAR data channel B end. The B end of the STAR data channel is the controlling end. Normally, the B end is connected to a STAR data channel provided by the SAC of a STAR computer. The B end controls transfers, specifies addresses for the A end, and handles fault conditions.



NOTES:
INTF = INTERFACE
SAC CHAN = STORAGE ACCESS CONTROL CHANNEL

Figure 1-17. Station Buffer Unit Functional Block Diagram

NORMAL CHANNEL INTERFACE

The normal channel interface logic provides a connection in the SBU between the SCU buffer controller normal channel bits and the various interface logic blocks in the SBU. The normal channel bits are used to transmit data, control information to the SBU interfaces, and read in status bits from the SBU interfaces.

This logic block interfaces six 16-bit BC normal channels, three input channels, and three output channels. It contains transmitters, receivers, data fanin and fanout logic, and a decoding section.

CORE CONTROL

The core control logic provides 12 access channels to eight modules of core memory having a total of 32,768 16-bit words of memory. Core memory is phased between modules, each module having independent read/write capability. The maximum memory reference rate is eight references per full memory scan of 1.1 microsecond. The core control logic determines channel priorities, increments channel addresses, checks for page boundaries, controls transfer of data and addresses to memory modules, and provides external timing signals.

I/O INTERFACES

Various types of I/O interfaces are used to enable the transfer of data to or from peripheral devices and an HLP or between second-level stations having B interfaces and an HLP. With one exception (the network trunk interface) all I/O interfaces are controlled by the BC in the SCU and provide status conditions to the BC upon request.

STATION CONTROL UNIT

The SCU (Figure 1-18) is composed of a number of functionally related devices described in the order listed.

- Buffer controller and 1.1-microsecond memory
- Normal channels
- Normal channel interface
- SCU gate
- STAR B data channel interface (SBU coupler A/B)
- Drum/display logic, keyboard, and microdrum

BUFFER CONTROLLER

The BC is the primary control element of any station. It is an internally programmed parallel mode, digital computer having 4096 16-bit words of core memory with a cycle time of 1.1 microseconds. The core memory is expandable to 8K words. The instruction set of the BC was specifically chosen to be compatible with peripheral device-related tasks. The BC provides one 16-bit parallel block transfer channel for high speed data transfer. It also provides up to 512 individually programmed normal channel lines for lower speed data transfer and for peripheral device and station control.

An optional 8K semiconductor memory with a 200-nanosecond cycle time is available in place of the standard 1.1 microsecond core memory in the STAR station control units but is software supported only in the paging and disk stations.

NORMAL CHANNELS

The SCU contains eight normal input channels and eight normal output channels, each of which is 16 bits wide. Channels 0 through 4 are used for the transfer of data and control functions between the programmable elements of the SBU and SCU. Channels 5 through 7 are used for similar functions (data and control) between the various I/O SBU interfaces and the SCU. All normal channel bit assignments for all channels appear in appendix A of this manual.

The 7000 I/O interface provides a stacking feature which allows starting and terminating addresses to be held until needed so the SCU can be free to complete more important control functions.

DRUM STORAGE UNIT

The DSU used in the drum station is a modified version of the CDC standard 865 DSU. The DSU provides the I/O channel with 12-head parallel format accessibility and a standard storage interface. The DSU uses 768 data tracks and four control tracks in the process of accomplishing its storage function. Two of the control tracks are used as master tracks; one is used for clock pulses and one for index marks. The remaining two are spares. The data heads are organized into 64 head groups with 12 read/write heads per group. Data bits are recorded on the drum via the phase modulation method at a clock rate of 2 megabits per second.

HIGH CAPACITY DISK (HCD) STATION

The HCD station (Figure 1-16) provides an extension of mass memory for higher level computer storage. The SBU in this station contains 32K bits of storage. Each 7000 I/O channel interface within the SBU is connected to a separate controller. Each 7000 interface has two channels, one for transmitting function codes and receiving status and one for handling data. Up to a total of four 819 disk files are available by option for connection to a mass storage controller. A second SBU is also available by option and is connected with a disk file subsystem as illustrated in Figure 1-16. The mass storage controller and one 819 disk file are also supplied with the optional SBU.

STATION FUNCTIONAL OPERATION

The SBU in an HCD station receives functions from an HLP. Depending on the function, the SCU initiates operation of the STAR B interface to send or receive data from the HLP. Data is transferred in page increments, each page having 2048 hexadecimal words. As applied to STAR HCD stations, each sector of the 819 disk file contains 2064 words; the first 16 are software header and the remaining 2048 are data. After data is stored in SBU core memory, the SCU initiates operation of one of the 7000 I/O

interfaces to transfer a page of data to the disk itself. The disk's surface is divided into one-page increments so that one page of data from memory may be stored on a one-page sector on the disk. When the HLP requests data, the SCU commands the disk to send data to SBU memory via a 7000 I/O interface. Once data is in SBU memory, the SCU initiates an operation to transfer the data from SBU memory to the HLP via a STAR B interface. The normal channel interface in the SBU provides the path used by the SCU to control the various SBU interfaces. In system configurations requiring two SBUs and one SCU, normal channels 8, 9, and A are used for the second SBU interfaces and are defined as normal channels 5, 6, and 7, respectively.

The HCD station interfaces one or two disk file subsystems via 7000 I/O channel interfaces in the SBU. The description given for the SBU in the drum station also applies to the HCD station except that the HCD station does not use an index compare operation. The SCU in the HCD station performs the same general functions as the SCU in the drum station. However, the HCD station SCU uses the 200-nanosecond memory. Components of the HCD station are as follows:

- SBU (optional SBU identical)
  STAR A data channel interface (SCU coupler)
  STAR B data channel interface (SAC coupler; channels 1 and 2)
  Normal channel interface
  Core control
  1.1-microsecond memory (32K)
  7000 I/O channel interfaces (channels 0 and 1)

- SCU
  Buffer controller and 200-nanosecond memory (8K)
  Normal channel interface
  SCU gate
  Block transfer channel
  STAR B data channel interface (SBU couplers A and B)
  Drum/display logic, keyboard, and microdrum

- Portable maintenance console

- 819 disk file

STAR-100 MAINTENANCE CONTROL UNIT

The STAR-100 maintenance control unit (Figure 1-14) consists primarily of the basic SCU which provides two SAC channel couplers to the central memory of a STAR-100 computer. The SCU also contains a special control interface which is connected to multiple access lines to and from the computer's mainframe. These lines serve as the means for measuring and monitoring functions of the STAR-100 Computer. The maintenance control unit also has a 3000 I/O channel interface, line printer interface, and a disk storage drive interface. A listing of the maintenance control unit's major components is as follows:

- STAR B data channel interface (SAC couplers; channels 1 and 2)
- Special control interface
- Buffer controller
- 3000 I/O channel interface
- 854 disk storage drive interface
- Line printer interface
- Normal channel interface
- Portable maintenance console (external to MCU)

STATION FUNCTIONAL OPERATION

The two SAC coupler interfaces and the special control interface allow the maintenance control unit to regulate information flow, control pulses, and monitor performance of the STAR-100 Computer. The maintenance control unit provides system deadstart capability via the portable maintenance console and system monitoring. The three general modes of operation relative to maintenance control unit/computer program functions are:

- Operation of a computer diagnostic maintenance program used to locate faults and malfunctions within the maintenance control unit.
- Running diagnostic routines on the computer. The maintenance control unit loads diagnostics into the computer via the portable maintenance console, controls and monitors operations of the diagnostics, and indicates the results of the tests on either the line printer or other appropriate peripheral device.

- The maintenance control unit loads the program into the computer via the portable maintenance console and controls and monitors its operation. In this mode of operation, the maintenance control unit is responsible for autoloading the CPU and the BC of first-level stations, running on-line diagnostics, and restarting the CPU.

A special control interface connects to the microcode memory of the STAR-100 Computer. This interface provides the maintenance control unit with the ability to load and store microcode and to load microcode diagnostic routines. The interface also provides control to run the routines under maintenance control unit control.

PERIPHERAL EQUIPMENT

Three types of interfaces are supplied with the MCU for connecting to 3000 peripheral controllers, to a disk storage driver interface, and to a line printer interface. The 854 DSD interface accommodates up to four disk drives. The line printer interface services one line printer.

844 DISK STORAGE UNIT

The 844 disk storage unit, used in several of the peripheral stations, has a storage capacity of 755 million bits grouped in three sectors per track, with each disk surface having a total of 404 usable tracks. The disk rotates at 3600 rpm, and head positioning time over the recording surfaces averages between 10 and 55 milliseconds. The 844 utilizes 19 read/write heads and one track-servo head for recording on its 19 disk surfaces (top of the top disk and bottom of the bottom disk are protective nonrecording surfaces). Data recording rate is 6.8 million bits per second. The 844 uses the 881 disk pack as its recording medium.

854 DISK STORAGE DRIVE

The 854 disk storage drive, used with the STAR-100 or STAR-65 maintenance control unit, has a storage capacity of 53.4×10^6 data bits. The disk pack recording surfaces rotate at 2400 rpm. The data recording rate is 1.25×10^6 data bits per second. Each of the ten disk recording surfaces is subdivided into 200 tracks, thereby providing a total of 2000 tracks for the unit. Head positioning time of the single access mechanism is in the range of 24 to 135 milliseconds.

865 DRUM STORAGE UNIT

The drum storage unit is a model 865 modified to be compatible with a 7000 I/O channel and the 7000 interfaces in the SBUs of the paging (drum) and STAR-100 service stations. It is an electromechanical recording drum having a total storage capacity of 46.1×10^6 bits. The drum is addressable in sectors of quarter or full pages. Refer to Table 1-2 for sector data bit capacity. It rotates at 1800 rpm and uses 12 parallel heads in any one of 64 head groups to cover 768 data tracks.

HIGH CAPACITY DISK (HCD) FILE SUBSYSTEM

The high capacity disk (819 HCD) file subsystem used with the HCD station consists of a mass controller and a high capacity disk. The controller contains the logic for controlling operations between the HCD file and a 7000 I/O channel in an SBU. The HCD file has an operational capacity of over 2.1 billion bits when used in a sectored format of 16 sectors per track, 10 head addresses per cylinder, and 404 cylinders per drive. Head positioning time is an average of 50 milliseconds and rotates at 3600 rpm. The data transfer rate is 38.7 million bits per second. Table 1-2 lists pertinent characteristics of the HCD file subsystem.

TABLE 1-2. PERIPHERAL STORAGE UNIT CHARACTERISTICS

	841 Disk Storage Drive (Modified)	844 Disk Storage Unit	854 Disk Storage Drive	865 Drum Storage Unit (Modified)		High Capacity Disk File (819) Subsystem
Total bit capacity per drive (data)	235.9×10^6	755×10^6	53.4×10^6	46.1×10^6		2.1×10^9 †††
No. of tracks per surface	180	404	200	768		411
Sectors per track	2	3	16	†		16
Rotational speed	2184 rpm	3600 rpm	2400 rpm	1800 rpm		3600 rpm
No. of recording surfaces	20/drive	19/drive	10/drive	1		40/drive
Latency	27.6 ms	16.7 ms	25 ms	33.3 ms		16.7 ms
Access time	24.5-135 ms	10-55 ms	24-135 ms	17 ms		15-80 ms
Bits/sector(data)	32,768	32,768	1664	††		32,768
Clock rate (bits per second)	2.52×10^6	6.8×10^6	1.25×10^6	2×10^6		9.67×10^6
Data transfer rate (bits per second)	2.52×10^6	6.8×10^6	1.25×10^6	24×10^6		38.7×10^6
Disk pack used	871	881	851	NA		NA

†Quarter page has 88 sectors per track; full page has 22 sectors per track.
††Quarter page has 8192 bits per sector; full page has 32,768 bits per sector.
†††Add 2×10^9 bits for each optional HCD added; maximum of 4 per controller.

STATION BUFFER UNIT INTERFACES 2

GENERAL

This section contains a general overview of the station buffer unit (SBU) followed by a brief operational description of the SBU and detailed descriptions of each SBU interface.

NOTE

Throughout this section, word formats illustrating unused bits by the cross-hatch pattern (for example, Figure 2-4) must have these bits all set to zeros. If they are not, undefined results may occur.

SBU OVERVIEW

The SBU consists of a number of functional subsections (Figure 2-1) but functions mainly as a buffer memory for I/O data being transferred between peripheral equipment and a higher level processor (HLP). Each SBU is connected to a companion station control unit (SCU) which controls the input/output interfaces within the SBU. The SBU has the following basic characteristics and capabilities.

- Core memory storage for 32,768 data words organized around eight memory modules of 4096 16-bit words. Each module has independent read/write capability and a 1.1-microsecond cycle time.
- Twelve independent memory access channels (MAC) for connection of input/output interfaces. Each MAC provides for incrementing memory addresses, indicating page boundaries, and controlling data transfer functions.
- A channel priority system which resolves conflicts in any memory module according to a priority number where channel number 0 is the highest priority and channel number 11 is the lowest.
- A phased memory system which permits an effective memory cycle time of up to 136 nanoseconds for references to sequential memory locations.
- The SBU is controlled by the buffer controller (BC) in the SCU via the normal I/O channel interface.

SBU memory connects to I/O interfaces present in an SBU cabinet through the 12 MACs and to the SCU normal channel interface logic. The particular method in which these connections are made is determined by the type of station in which the SBU is to be used. Generally, I/O interfaces allow connection of the SBU to an HLP memory, to other peripheral stations, to peripheral devices, and to the SCU normal channels. The I/O interfaces connect to the SBU core control logic for memory access and to the SCU normal channels for control.

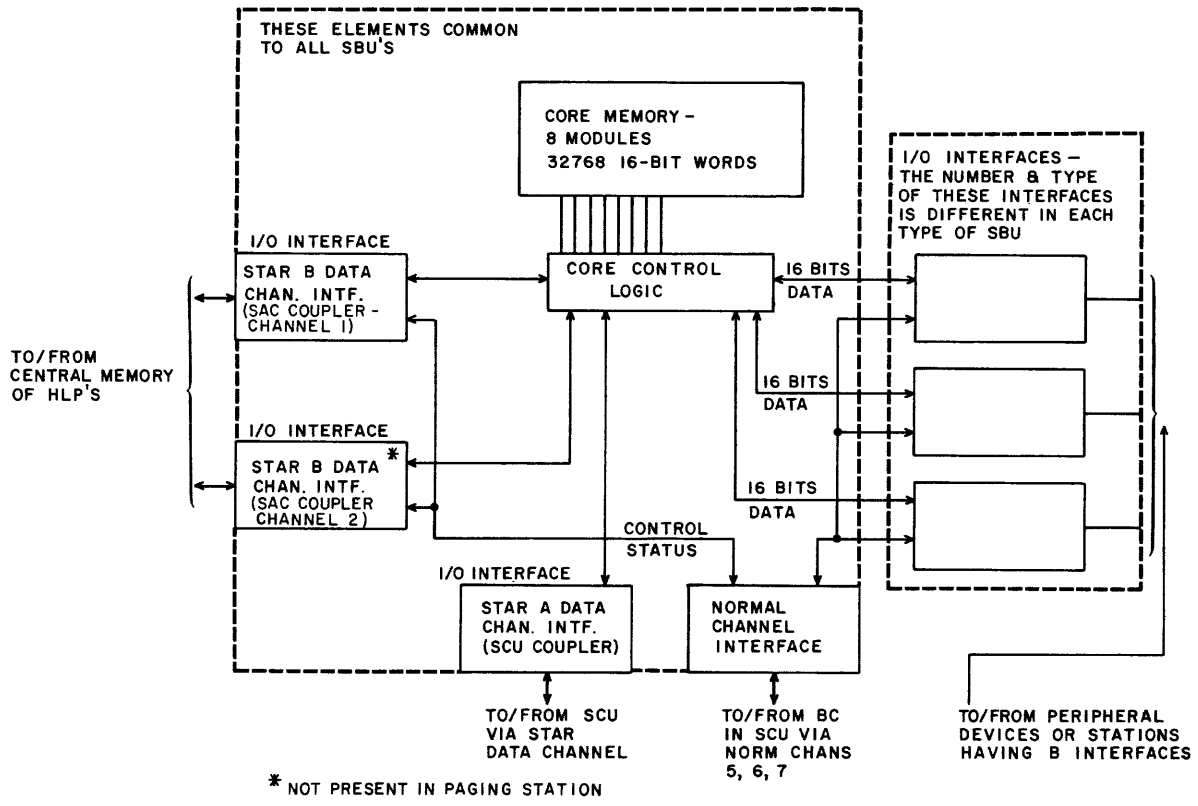


Figure 2-1. SBU Block Diagram

ORGANIZATION OF SBU MEMORY

The SBU memory consists of eight 4096-word modules combined to form 32,768 words of contiguous storage. Memory word length is 18 bits. There are 16 data bits and two parity bits.

The eight memory modules operate independently, permitting memory references to take place concurrently in all eight of the modules. This feature allows overlapping of memory references (bank phasing) to gain an effective memory cycle time much faster than the 1.1-microsecond cycle time of the individual memory modules when the total memory is used in a sequential mode. Overlapping is achieved by assignment of sequential memory addresses to different modules. Immediately after a memory reference has been initiated, a second reference can be initiated for the next sequential location which lies in another module. The second memory reference can proceed before the first is completed. Shortly after the second reference has begun, a reference can be started for the next sequential address which is in a third module, and so on. Eight sequential addresses can be referenced without waiting for completion of previous memory references. The module scanning sequence is fixed. Figure 2-2 shows the timing of the overlapped memory references.

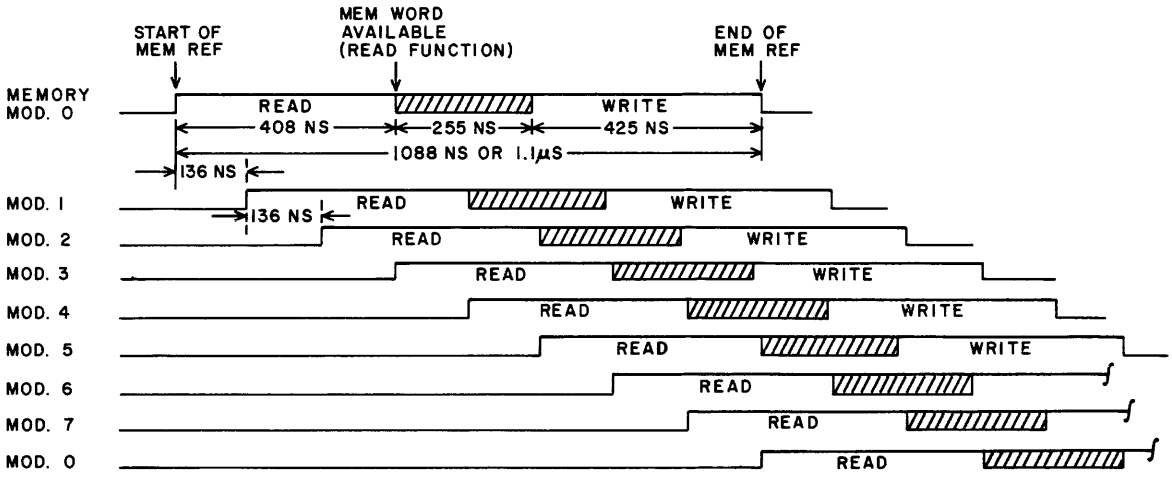


Figure 2-2. Overlapped Memory References

This system yields an effective memory cycle time of 136 nanoseconds during sequential addressing of the SBU. However, during random memory addressing, the effective cycle time is longer. In the worst case, where all memory addresses lie within one module, memory cycle time becomes 1.1 microseconds.

SBU memory is segmented into 16 2048-word pages. Page 0 contains the lowest 2048 addresses; page 1, the next 2048 words, and so on. Some SBU I/O interfaces are page oriented; they are designed to transfer one or more pages of data during each input or output operation.

SBU I/O INTERFACES

The input/output interfaces, present in an SBU, transfer data between peripheral devices and SBU memory.

There are a number of SBU interfaces, each intended for use with a different type of peripheral equipment. The following interfaces are typical of those used in the SBUs.

844 disk interface	Allows 844 disk units to exchange data with SBU memory.
3000 I/O interface	Simulates a standard CDC 3000 I/O channel. Allows 3000-series magnetic tape subsystems to transfer data into or out of SBU memory.
7000 I/O interface	Simulates a standard CDC 7000 I/O channel. Allows 865 and high capacity disk subsystems to transfer data into or out of SBU memory.
STAR B data channel interface	Allows an SBU to transfer data to or from an HLP across a STAR data channel. Acts as the B or active end of a STAR data channel.
STAR A data channel interface	Acts as the A or passive end of a STAR data channel. Allows an SBU to transfer data across a STAR data channel in response to requests from devices equipped with STAR B interfaces.

TABLE 2-1. SBU CONNECT CODES

STATION / INTERFACE	Paging (Drum)	HCD	844 Service	844 Storage	Magnetic Tape	Storage (Media)	STAR-100 Service	STAR-1B Service
7000-0	2_{16}	0_{16}	NA	NA	NA	NA	2_{16}	NA
7000-1	1_{16}	1_{16}	NA	NA	NA	NA	NA	NA
SAC-1	0_{16}	2_{16}	0_{16}	1_{16}	1_{16}	1_{16}	0_{16}	1_{16}
SAC-2	NA	3_{16}	1_{16}	3_{16}	3_{16}	3_{16}	1_{16}	3_{16}
Index compare	3_{16}	NA	NA	NA	NA	NA	NA	5_{16}
SCU coupler	†	†	3_{16}+ NOC-6, bit 8	†	†	†	3_{16}+ NOC-6, bit 8	7_{16}+ NOC-6, bit 1
844-A	NA	NA	2_{16}	0_{16}	0_{16}	NA	NA	NA
844-B	NA	NA	† †	2_{16}	2_{16}	NA	NA	NA
Network trunk	NA	NA	† † †	NA	NA	NA	NA	NA
Peripheral A interface group	NA	NA	3_{16}	NA	NA	NA	3_{16}	7_{16}
3000-0	NA	NA	NA	C_{16}	C_{16}	C_{16}	NA	NA
3000-1	NA	NA	NA	D_{16}	D_{16}	D_{16}	NA	NA
Scanner	NOC-6, bit B	NOC-6, bit B	NOC-6, bit B	6_{16}	6_{16}	6_{16}	NOC-6, bit B	6_{16}
MDD-A (841)	NA	NA	NA	NA	NA	0_{16}	NA	0_{16}
MDD-B (841)	NA	NA	NA	NA	NA	2_{16}	NA	2_{16}

NA = not applicable
NU = not used
† = Connected to dedicated channel between SBU coupler in SCU and SCU coupler in SBU
† † = 2 more 844's optional
† † † = Controlled by remote terminal

TABLE 2-2. SBU MEMORY PRIORITIES

Priority Level	Interface
Paging (Drum) Station	
0	7000 channel 1
1	7000 channel 0
2	SAC channel 1
3	SCU coupler
4	Index compare
HCD Station	
0	7000 channel 0
1	7000 channel 1
2	SCU coupler
3	SAC channel 1
4	SAC channel 2
844 Service Station	
0	844-A
1	Network trunk 1
2	Network trunk 2
3	Network trunk 3
4	Network trunk 4
5	SCU coupler
6	SAC channel 1
7	SAC channel 2
8	Peripheral A No. 1
9	Peripheral A No. 2
10	Peripheral A No. 3
11	Peripheral A No. 4

Priority Level	Interface
STAR-100 Service Station	
0	7000 channel 0
1	SCU coupler
2	SAC channel 1
3	SAC channel 2
4	Peripheral A No. 1
5	Peripheral A No. 2
6	Peripheral A No. 3
7	Peripheral A No. 4
8	Peripheral A No. 5
9	Peripheral A No. 6
10	Peripheral A No. 7
11	Peripheral A No. 8
STAR-1B Service Station	
0	MDD-A (841)
1	MDD-B
2	Index compare
3	SCU coupler
4	SAC channel 1
5	SAC channel 2
6	Peripheral A No. 1
7	Peripheral A No. 2
8	Peripheral A No. 3
9	Peripheral A No. 4
10	Peripheral A No. 5
11	Peripheral A No. 6
844 Storage Station	
0	844-A
1	844-B
2	3000 channel 1
3	3000 channel 2
4	SCU coupler
5	SAC channel 1
6	SAC channel 2

OPERATION FUNCTION CODES

Table 2-3 lists the codes sent from B.

TABLE 2-3. OPERATION FUNCTION CODES

Name	CODE
Write	010_2
Block read	101
Read	001
Special function	011 †
Data	100
Null	000
End of operation	111
Note: Code 110 is illegal. † Applies to STAR-65 only	

Write (010_2)

This code prepares the A interface for a write operation. It also causes the A interface to read in the first word of a two-word starting address that B sends along with this function code.

Block read (101)
Read (001)

The effect of these two codes is identical. They prepare the A interface for a block read operation. They also cause the A interface to read in the first word of a two-word starting address that B sends along with these codes.

Special function (011_2)

This code is used by the STAR-65 maintenance control unit to initiate special functions other than normal input/output operations. The exact meaning of this code must be determined by the users at each end of the channel prior to its use.

Data (100)

This code does not specify an operation. It identifies the accompanying 16-bit word sent from B as the first (most significant) part of a 32-bit data word. Used only during write operations.

Null (000) — This code does not specify an operation. It identifies the accompanying 16-bit word sent from B as the second part of a 32-bit starting address or data word.

End of operation (111) — This code notifies the A interface that the current block read or write operation is complete.

Illegal code (110) — This code should not be used. If issued, the A interface returns an illegal response signal to the B end of the channel.

SYSTEM CONTROL FUNCTIONS

The burden of initiating and controlling I/O operations on the STAR channel lies with the peripheral station at the B end of the channel. This relieves the processor (SCU) at the A end of the channel of much I/O overhead. However, there are situations that require A to send I/O control information to B. System control function codes (Table 2-4) provide a method for A to signal B.

TABLE 2-4. SYSTEM CONTROL FUNCTION CODES

Name	Code	
	Bit D	Bit E
Channel flag	0	1
External flag	1	0
Suspend	1	1
Invalid	0	0

The SCU in the service station uses two normal output channel bits to send these codes to B through the A interface.

Channel flag (01_2) — This code informs the B end of the channel that the system software has placed a message for B in a predetermined area in SBU memory at the A end of the channel. B normally responds to this code by initiating a block read operation to read in the message.

External flag (10_2)	This code directs B to master clear and then enter an autoload sequence.
Suspend (11_2)	This code causes B to terminate a write or block read operation.
Invalid (00)	The service station SCU should not transmit this code. It appears on the channel only if a transmission fault occurs in one of the valid codes. The B end of the channel should assume that a suspend code was intended. It should terminate the data transfer operation in progress and then send an interrupt to A to signal the malfunction.

STARTING ADDRESS FORMAT

The STAR data channel procedure requires that two 16-bit address words (Figure 2-4) be sent from B to A at the beginning of a write or block read operation. The A interface uses only the second address word since only 14 address bits are required to address the entire SBU memory (16K of 32-bit words). A two-word address must be sent to satisfy channel requirements but only one is used by the A interface.

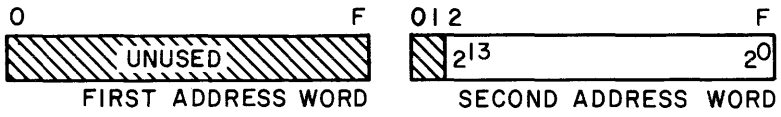


Figure 2-4. STAR Channel Starting Address Format

Memory addressing on the STAR channel is always based on a memory word size of 32 bits. Thus, the SBU memory is regarded as 16K of 32-bit words even though actual SBU memory word size is 16 bits. The A interface always transfers data in multiples of two 16-bit memory words.

STAR CHANNEL TRANSMISSION SEQUENCE

Function codes and data transferred on the STAR channel must follow a fixed sequence. The required sequences for write and block read operations are described in the following paragraphs. Note that each 16-bit unit of information transferred on the data path must be accompanied by a function code.

WRITE SEQUENCE

	Function Code (B to A)	Data Path
Step 1	Write code (010_2)	1st address word (B to A)
Step 2	Null code (000)	2nd address word (B to A)
Step 3	Data code (100)	16-bit data word (B to A)
Step 4	Null code (000)	16-bit data word (B to A)
	Repeat steps 3 and 4 for each additional 32-bit unit of data transferred from B to A.	
Step 5	End of operation code (111)†	Not used
Step 6	Null code (000)	Not used

BLOCK READ SEQUENCE

	Function Code (B to A)	Data Path
Step 1	Block read code (101_2)	1st address word (B to A)
Step 2	Null code (000)	2nd address word (B to A)
Step 3	None	16-bit data word (A to B)
Step 4	None	16-bit data word (A to B)
	Repeat steps 3 and 4 for each additional 32-bit unit of data transferred from A to B.	
Step 5	End of operation code (111)†	Not used
Step 6	Null code (000)	Not used

†If another data transfer operation follows immediately, the end of operation code is not necessary. A new write or block read terminates the previous operation.

PARITY CHECKING

Two types of parity checking take place during A interface operations.

FUNCTION CODE PARITY CHECK

The A interface checks each function code, sent from B, for odd parity. If A detects a function parity error, it notifies B by sending a parity error signal and the illegal signal.

ADDRESS AND DATA PARITY CHECK

The A interface checks each address or data word, sent from B, for odd parity. If A detects a parity error, it notifies B by sending a parity error signal.

SBU MEMORY PARITY CHECK

During a block read operation, the A interface checks parity for each 16-bit data word read from SBU memory. If a parity error occurs, A notifies B by sending a parity error signal. The peripheral A interface also reports an SBU parity error to the SCU on a normal channel bit. A 3-bit bank count, which indicates the SBU memory bank in which a parity error occurred, is also available to the SCU on normal channel bits.

When a parity error occurs, the block read operation continues unless stopped by the B end of the channel. However, the A interface does not accept a function code for a new operation unless B first sends an end of operation code or the SCU issues a program clear to the A interface on the normal channels.

INTERRUPTING THE A INTERFACE

The STAR data channel includes an interrupt line on which B can send an interrupt signal to A. The interrupt signal is used to facilitate communication between B and the SCU system software at the A end of the channel. Communication from B to A consists of two steps.

1. B writes a message for A into a predefined area in SBU memory at the A end of the channel.
2. B sends an interrupt signal to notify A that a message has been placed in SBU memory.

The A interface reports the interrupt signal to the SCU on a normal channel bit.

One such normal channel bit is available for each peripheral A interface in the SBU. It is the responsibility of the system software to periodically scan these interrupt bits and to interpret and act on messages placed in memory by B.

NORMAL CHANNEL CONTROL AND STATUS BITS

Table 2-5 lists and explains each SCU normal channel bit associated with the peripheral A interface. The channel and bit assignments given are for the STAR 100 service station which contains eight peripheral A interfaces. Channel and bit assignments for peripheral A interfaces used in other stations may be different. Refer to appendix A near the end of this manual for a complete set of normal channel bit assignments for all STAR stations.

TABLE 2-5. NORMAL CHANNEL BIT DEFINITIONS FOR PERIPHERAL A INTERFACE

<table>
<tr><th>Channel</th><th>Bit</th><th>Name</th><th>Function</th></tr>
<tr><td>NOC-6</td><td>0</td><td rowspan="8">Sel. periph. intf. 8 → 1</td><td rowspan="8">These bits select one of the A interfaces for SCU control.
When an interface is selected, the SCU can:
1. Send control function codes to B through the selected A interface.
2. Issue program clear and clear interrupt commands to the selected A interface.
3. Read in the parity error bank count from the selected interface.</td></tr>
<tr><td>NOC-6</td><td>1</td></tr>
<tr><td>NOC-6</td><td>2</td></tr>
<tr><td>NOC-6</td><td>3</td></tr>
<tr><td>NOC-6</td><td>4</td></tr>
<tr><td>NOC-6</td><td>5</td></tr>
<tr><td>NOC-6</td><td>6</td></tr>
<tr><td>NOC-6</td><td>7</td></tr>
<tr><td>NOC-6</td><td>C → F</td><td>Connect code (2^3 → 2^0)</td><td>These bits determine which interface or group of interfaces in the SBU is connected to the SCU normal channels. (Refer to Table 2-1 for peripheral A interface connect codes.)</td></tr>
<tr><td>NOC-7</td><td>B</td><td>Clear interrupt</td><td>Setting and then clearing this bit clears the interrupt from B status bit for the selected interface.</td></tr>
<tr><td>NOC-7</td><td>C</td><td>Program clear</td><td>Setting and then clearing this bit clears the following items in the selected A interface.
1. The operation selection (write or block read).
2. The SBU parity error status bit.
3. The parity error bank count.</td></tr>
<tr><td>NOC-7</td><td>D</td><td>Control function bit 2^1</td><td rowspan="2">These two bits are used for transmitting a control function code to B through the selected A interface.
Codes:
Bit D (2^1) | Bit E (2^0) | Function
0 | 0 | Invalid
1 | 0 | External flag
0 | 1 | Channel flag
1 | 1 | Suspend</td></tr>
<tr><td>NOC-7</td><td>E</td><td>Control function bit 2^0</td></tr>
</table>

TABLE 2-5. NORMAL CHANNEL BIT DEFINITIONS FOR PERIPHERAL A INTERFACE

Channel	Bit	Name	Function
NOC-7	F	Control function strobe	Setting this bit causes the selected A interface to transmit a control function code (NOC-7, bits D and E) to B.
NIC-5	0	Memory parity error, SCU coupler	When 1, this bit indicates that an SBU memory parity error has occurred during a block read operation conducted by the SCU coupler.
NIC-5	1	Parity error bank counter 2^2	For the selected interface, these bits indicate the SBU memory bank in which a parity error has occurred. They apply to the SCU coupler as well as the peripheral A interfaces. These bits are meaningful only if one of the parity error status bits is 1.
NIC-5	2	Parity error bank counter 2^1	
NIC-5	3	Parity error bank counter 2^0	
NIC-5	8	Mem. parity error, I/O channel 1	When 1, this bit indicates that a memory parity error has occurred during a block read operation conducted by I/O channel 1.
NIC-5	9	Mem. parity error, I/O channel 2	
NIC-5	A	Mem. parity error, I/O channel 3	
NIC-5	B	Mem. parity error, I/O channel 4	
NIC-5	C	Mem. parity error, I/O channel 5	
NIC-5	D	Mem. parity error, I/O channel 6	
NIC-5	E	Mem. parity error, I/O channel 7	
NIC-5	F	Mem. parity error, I/O channel 8	

TABLE 2-5. NORMAL CHANNEL BIT DEFINITIONS FOR PERIPHERAL A INTERFACE (Cont'd)

Channel	Bit	Name	Function
NIC-6	0	Memory P.E. I/O channel	When 1, this composite status bit indicates a memory parity error on one of eight I/O channels or the SCU channel.
NIC-6	1 ↓ 7		Not used
NIC-6	8	I/O Interrupt-Chan 1	When 1, this bit indicates an interrupt from the B interface on I/O channel 1.
	9	2	
	A	3	
	B	4	
	C	5	
	D	6	
	E	7	
	F	8	

PROGRAMMING SEQUENCES

The following paragraphs indicate the required programming sequence for those A interface activities that can be controlled by the SCU. Normal channel bit assignments referenced are for the STAR 100 service station.

1. Connect Peripheral Interfaces

   Place the appropriate connect code in NOC-6, bits C through F (code 3_{16} for STAR 100 service station).

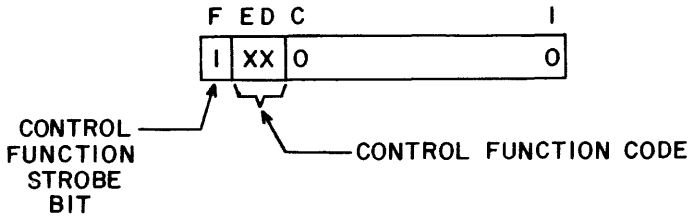
   The SCU remains connected to the group of peripheral A interfaces as long as the connect code is held in NOC-6.

2. Transmit Control Function Code to B

   a. Connect according to step 1.

   b. Select desired A interface (NOC-6, bits 0 through 7).

   c. Set following pattern in A register.



   d. Output from A to NOC-7.
   This causes the selected A interface to transmit the code.

   e. NOC-7 may be cleared immediately.
      Note: This operation does not apply to the SAC coupler.

3. Clear Interrupt

   a. Connect according to step 1.

   b. Select desired peripheral A interface (NOC-6, bits 1 through 8).
      Note: This operation does not apply to the SAC coupler.

   c. Set and then clear interrupt bit (NOC-7, bit B).

4. Program Clear

   a. Connect according to step 1.

   b. Select desired peripheral A interface (NOC-6, bits 1 through 8).

   c. Set and then clear program clear bit (NOC-7, bit C)
      Note: SAC coupler can be program cleared as well as the peripheral A interfaces.

SBU MEMORY PARITY CHECK

During a block read operation, the SCU coupler checks parity for each 16-bit data word read from SBU memory. If a parity error occurs, the SCU coupler notifies B by sending a parity error signal on the STAR channel. Also, the SCU coupler sends a 3-bit bank count that indicates the SBU memory bank in which a parity error occurred to the SCU via normal channel bits.

When a parity error occurs, the block read operation continues unless stopped by the B end of the channel. However, the A interface does not accept a function code for a new operation unless B first sends an end of operation code or the SCU issues a program clear to the A interface.

NORMAL CHANNEL STATUS BITS

In most applications, the only normal channel bits associated with the SCU coupler are three normal input channel bits that carry a parity error bank address for the SCU coupler. The parity error bank address bits indicate the SBU memory bank in which a parity error occurred during a block read operation. They are meaningful only after the SCU coupler has signaled the SCU, via the STAR data channel, that a parity error has occurred. The three address status bits remain valid until the SCU issues an end of operation function code to the SCU coupler.

The normal input channel bit assignments for these status bits are not the same for all stations. In most cases, they occupy three bits of the scanner status word or three bits of one of the normal channel feedback words. Normal channel assignments for each STAR station are listed in appendix A of this manual.

In the three STAR service stations, the normal channel bits for the SCU coupler are a little different than in other stations. Several peripheral A interfaces are present in the service stations. Since the SCU coupler and peripheral A interfaces are quite similar, they share some of the same normal channel bits. The normal channel bits that apply to the SCU coupler in a service station are listed in Table 2-7.

TABLE 2-7. NORMAL CHANNEL BIT DESCRIPTIONS FOR SCU COUPLER INTERFACE

Channel	Bit	Name	Function
NOC-6	D E F	Connect code (2^2) ↓ (2^0)	Three normal output channel bits connect the A interface group within the SBU to the normal channel lines. The A interface group includes the SCU coupler and the peripheral A interfaces. Additional select bits are used to select one interface within the group.
NOC-6	8	Select SCU coupler	This normal output channel bit selects the SCU coupler as the A interface connected to the normal channel lines. It must be used along with the connect code.
NOC-7	C	Program clear	This normal output channel bit clears the selected A interface. Setting and then clearing this bit clears the following items in the SCU coupler. 1. The operation selection (write or block read) 2. The parity error status bit 3. The parity error bank address
NIC-5	0	Memory parity error SCU coupler	This normal input channel bit is a status bit. When 1, it indicates that an SBU memory parity error has occurred during a block read operation conducted by the SCU coupler.
NIC-5	1 2 3	Parity error $\overline{\text{bank}}$ $\overline{\text{address}}$ (three bits)	These three normal input channel bits are status bits shared by the SCU coupler and peripheral A interfaces. For the selected interface, they indicate the SBU memory bank in which a parity error has occurred. To find the memory bank with the parity error, complement the bank counter and count back four banks.

The function strobe bit transfers the null function code and address to the coupler. Again, the coupler automatically forwards the code and address to the HLP.

If an HLP/SBU memory operation has been selected (SCU/SBU select bit equals 1, the second function code (null) causes the coupler and HLP to begin transferring data. If an HLP/SCU operation has been selected (SCU/SBU select bit equals 0), the SCU must individually read-in or transmit each data word.

SYSTEM CONTROL CODES

The system control codes listed in Table 2-9 provide a means for the HLP to send control information to the SAC coupler.

TABLE 2-9. SAC COUPLER SYSTEM CONTROL CODES

Function	Code	
	Bit B	Bit C
Channel flag	0	1
External flag	1	0
Suspend	1	1
Invalid	0	0

The two control function bits appear as status bits on normal input channel 5. Two of the control codes directly affect operation of the peripheral station hardware.

Channel flag (01) — This code sets the channel flag status bit in the SBU scanner status word. It is used to indicate that a message for the peripheral station has been placed in a prearranged area in HLP memory.

External flag (10) — This code forces the SCU to master clear and autoload from the microdrum.

Suspend (11) — This code causes the SAC coupler to terminate a data transfer operation.

Invalid (00) — The HLP does not transmit this code. It appears on the channel only if a transmission fault occurs. If this code appears, the peripheral station software should assume that a suspend code was intended; it should terminate the data transfer operation in progress and then send an interrupt to inform the HLP of the malfunction.

The control function code is captured by two status bits that are available on normal input channel 5 (bits B and C). Associated with the two bits is a control function strobe status bit (normal input channel 5, bit D) that indicates that the HLP has sent a control function code. The two control function status bits are significant only when the function strobe status bit is set.

PARITY CHECKING

Three types of parity checking take place during SAC coupler operations.

ADDRESS AND DATA PARITY CHECK

The SBU generates an odd parity bit for each 8 bits transmitted to the HLP. One odd parity bit accompanies the lower data and address bits (2^7 through 2^0) and one parity bit accompanies the upper 8 data bits (2^{15} through 2^8). During SBU/HLP write operations, data received from the STAR data channel is checked for correct parity. If an error is detected, the HLP sends a parity error signal to the B interface. The B interface sets the STAR B parity error status (NIC-5, bit 5) and terminates the write operation. Similarly, received data from the HLP has one odd parity bit for the upper 8 bits and one odd parity bit for the lower 8 bits of each 16-bit word. The received data, address bits, and parity bits are checked by the B interface for accuracy. During SBU/HLP read operations, HLP read data is checked for parity. If a parity error is detected, the B interface sets the SBU parity error status bit (NIC-5, bit 0) and completes the read operation.

FUNCTION CODE PARITY

The coupler appends an odd parity bit to the 3-bit function code sent to the HLP. If the HLP detects a function parity error, it ignores the function code and returns a signal to the coupler that sets the transmission parity error status bit. This status bit is available to the SCU on normal input channel 5.

HLP READ PARITY †

During block read operations, data read from HLP memory is checked for proper parity. If a parity error occurs, the HLP signals the coupler. In response, the coupler completes the read operation and sets the SAC parity error status bit which is available to the SCU on normal input channel 5.

SBU MEMORY PARITY CHECK

During SBU memory-to-HLP write operations, data read from SBU memory is parity checked. If a parity error occurs, the coupler terminates the write operation and sets the SBU parity error status bit. This status bit appears on normal input channel 5.

† Does not apply where the STAR 100 Computer is the HLP.

SCU CONTROL OF THE SAC COUPLER

Tables 2-10 and 2-11 define the SCU normal channel bits used for control of the SAC coupler. Bit assignments given in the table are for the HCD station. SAC coupler normal channel bit assignments are different for some signals in other stations. Appendix A of this manual contains a full set of normal channel assignments for all STAR stations.

The SAC coupler must remain connected to the SCU in order to receive control information or data from the SCU. The coupler remains connected as long as the SCU holds the unique connect code, assigned to the coupler, on output channel 6, bits C through F.

TABLE 2-10. BIT DESCRIPTIONS FOR SAC COUPLER/NOC-5, -6, AND -7 INTERFACES (HCD STATION)

Channel	Bit	Name	Function
NOC-5	0 ↓ F	TA/SCU Addr/data bit 2^{15} ↓ TA/SCU Addr/data bit 2^{0}	These bits serve two purposes. 1. Transmit SBU terminating address to selected SAC coupler. 2. Transmit SCU address and data to HLP through selected SAC coupler.
NOC-6	0	Starting address SBU	This set/clear† bit is used to strobe the starting address, transmitted by NOC-7 into the SAC coupler.
NOC-6	1	Term. address SBU	This set/clear bit is used to strobe the SBU terminating address, transmitted by NOC-5, into the SAC coupler.
NOC-6	2	Function	This set/clear bit transfers three items of control information from the SCU into the SAC coupler. 1. Function code on NOC-7, bits D, E, and F 2. SBU memory/SCU select bit on NOC-7, bit C 3. HLP starting address word on NOC-5 The coupler then forwards the function code and address word to the HLP.

†A set/clear bit must be set and immediately cleared to perform its intended function.

TABLE 2-10. BIT DESCRIPTIONS FOR SAC COUPLER/NOC-5, -6, AND -7 INTERFACES (Cont'd)
(HCD STATION)

Channel	Bit	Name	Function
NOC-6	3	Program clear	This set/clear bit transfers the following control bits from the SCU into the SAC coupler. 1. Clear parity error, NOC-7, bit 7 2. Clear illegal, NOC-7, bit 8 3. Clear control function, NOC-7, bit 9 4. Master clear, NOC-7, bit A
NOC-6	4	Request	During SCU to HLP write operations, this set/clear bit causes the coupler to transfer a data word from the SCU (via NOC-5) to the HLP.
NOC-6	5	Accept	This bit acknowledges that the SCU has received one word of data on NIC-7. Prior to this the SCU must have received the data word when the first rank full staus bit was true.
NOC-6		Select status	This bit is used to determine whether data or a return address is made available on NIC-7. When bit is set, return address is available; when bit is clear, data is available.
NOC-6	7	Set interrupt	This set/clear bit provides a means of interrupting the central processor (via the SAC channel) and sets the external interrupt bit in the HLP.
NOC-6	C ↓ F	Connect code (2^3 ↓ 2^0)	These bits determine which interface in the SBU is connected to the SCU normal channels. (Refer to Table 2-1 for SAC coupler connect codes.)

TABLE 2-10. BIT DESCRIPTIONS FOR SAC COUPLER/NOC-5, -6, AND -7 INTERFACES (Cont'd)
(HCD STATION)

Channel	Bit	Name	Function
NOC-7	0 ↓ 6	SA bit 2^{15} ↓ ↓ ↓ SA bit 2^{9}	These bits as well as bits 7 through F are used to transmit the SBU starting address information to the SAC coupler. Bits 7 through F serve a dual purpose.
NOC-7	7	SA bit 2^{8}/clear parity error	Used for clearing the three parity error bits (NIC-5, bits 0, 4, and 5) or for bit 2^{8} of the starting address of a memory location in SBU core memory.
NOC-7	8	SA bit 2^{7}/clear illegal	Used for clearing the illegal status bit (NIC-5, bit 6) or for bit 2^{7} of the starting address.
NOC-7	9	SA bit 2^{6}/clear cont. function	Used for clearing the two control function status bits (NIC-5, bits B and C) or for bit 2^{6} of the starting address.
NOC-7	A	SA bit 2^{5}/MC	Used for transmitting the master clear bit to the SBU or for starting address bit 2^{5}.
NOC-7	B	SA bit 2^{4}	Used only for starting address bit 2^{4}.
NOC-7	C	SA bit 2^{3}/select SAC + $\overline{\text{SCU}}$	Other than being used as one bit of the starting address, this bit is used to select a data path between the HLP and the SCU or between the HLP and the SBU. When this bit is a 0, the HLP to SCU path is selected and when it is a 1, the HLP to SBU path is selected.
NOC-7	D ↓ F	Func. code/SA bit 2^{2} ↓ ↓ ↓ ↓ Func. code/SA bit 2^{0}	These bits are used for transmitting bits 2^{2} through 2^{0} of the SBU starting address information to the SAC coupler or for transmitting the desired function code to the HLP via the SAC coupler.

TABLE 2-10. BIT DESCRIPTIONS FOR SAC COUPLER/NOC-5, -6, AND -7 INTERFACES (Cont'd)
(HCD STATION)

Channel	Bit	Name	Function
			Codes: Function / 2^2 / 2^1 / 2^0 Null 0 0 0 Read 0 0 1 Write 0 1 0 Block read 1 0 1 EOP 1 1 1 Data 1 0 0

TABLE 2-11. BIT DESCRIPTIONS FOR SAC COUPLER/NIC-5, -6, AND -7 INTERFACES

Channel	Bit	Name	Function
NIC-5	0	SBU parity error	This status bit is used for indicating a parity error in SBU memory.
NIC-5	1	$\overline{\text{Bank counter}}\ 2^2$	If a parity error occurs, these three bits indicate the not SBU memory bank count. To find the memory bank with the parity error, complement the bank counter and count back four banks.
	2	$\overline{\text{Bank counter}}\ 2^1$	
	3	$\overline{\text{Bank counter}}\ 2^0$	
NIC-5	4	Transmission parity error	This status bit indicates that the HLP has detected a parity error in a function code transmitted from the SCU via the SAC coupler.
NIC-5	5	SAC parity error	This bit is used to indicate that a parity error occurred in the HLP memory during a read operation.
NIC-5	6	Illegal	This status bit indicates that the HLP has: 1. Detected an illegal function (011_2 or 110_2) sent from the SCU, or 2. Detected a parity error in a function code sent from the SCU.

TABLE 2-11. BIT DESCRIPTIONS FOR SAC COUPLER/NIC-5, -6, AND -7 INTERFACES (Cont'd)

Channel	Bit	Name	Function
NIC-5	7	Busy	This bit sets when the SCU transfers an address to the HLP at the beginning of a read or write operation. It remains set until the operation terminates.
NIC-5	8	Term. address compare	This bit is used to indicate that the latest HLP to SCU memory read or write operation is complete.
NIC-5	9	First rank full	This status bit indicates that half of a 32-bit data word from the HLP (read operations only) is available on NIC-7 for read-in by the SCU.
NIC-5	A	Last rank full	This bit indicates a word is in the last rank of buffering in the SAC interface.
NIC-5	B	Control function 2^1	These two bits are control signals which the HLP uses to communicate with the SAC coupler and are coded as follows:
	C	Control function 2^0	

Bit B(Fctn 2^1)	Bit C(Fctn 2^0)	Function
0	0	Invalid
0	1	Channel flag
1	0	External flag
1	1	Suspend

NIC-5	D	Control function strobe	This status bit indicates that the HLP has sent a control function code to the SAC coupler. The SCU can read in the control function on NIC-5, bits B and C.

TABLE 2-11. BIT DESCRIPTIONS FOR SAC COUPLER/NIC-5, -6, AND -7 INTERFACES (Cont'd)

Channel	Bit	Name	Function
NIC-7	0 ↓ F	Data/RA bit 2^{15} ↓ Data/RA bit 2^{0}	These bits serve two purposes. 1. Receive data from HLP during HLP-to-SCU block read operations. 2. Receive return address information. (The return address represents the last SBU address referenced by the SAC coupler.)
		Scanner Status	
NIC-6	A	SAC-1 flag	HLP has sent a channel flag control function code to SAC coupler number 1.
NIC-6	B	SAC-2 flag	HLP has sent a channel flag control function to SAC coupler number 2.
NIC-6	8	SAC-1 not busy	SAC coupler number 1 is not engaged in data transfer.
NIC-6	9	SAC-2 not busy	SAC coupler number 2 is not engaged in data transfer.

PROGRAMMING SEQUENCES

The following procedures are to be used to aid the programmer during the preparation of the program for conducting data transfers between the SCU and the HLP via the SAC coupler.

CONNECTING PROCEDURE

1. Place the appropriate connect code in bits C through F of NOC-6 to select the SAC coupler. (Refer to Table 2-1 for proper code.)
2. Check status (NIC-5) and check for error conditions.
3. If errors are detected, proceed to Error Recovery Sequence procedure.

10. Read in data word on normal input channel 7.
11. If an error is detected, proceed to Error Recovery Sequence procedure.
12. If data transfer is not complete, return to step 8 and continue procedure. If data transfer is complete, proceed to End of Operation sequence.

END OF OPERATION

1. Transmit the end of operation function (code 7 using bits D through F, NOC-7).
2. Set and then clear function bit (NOC-6, bit 2).
3. Return to step 11 of Addressing the HLP procedure to start another data transfer operation.

TESTING STATUS FOR COMPLETION OF DATA TRANSFER

1. Check that the SAC not busy signal is a 1, via bit 8 or 9 of NIC-6 (depending upon the SAC channel selected). If signal is not a 1, proceed to Error Recovery Sequence procedure.
2. Check status bits of NIC-5 for proper completion of data transfer. If an error is detected, proceed to Error Recovery Sequence procedure.
3. Exit to calling subroutine.

ERROR RECOVERY SEQUENCE

1. If this is the third retry, set abort (bit 0 of software control package) status and exit to calling subroutine.
2. Check status bits B and C of NIC-5 for presence of suspend, invalid, or external flag (autoload) control codes from the HLP. If any of these are present, set abort status and exit to calling subroutine.
3. Set master clear via bit A of NOC-7 (SCU to SBU).
4. Set and then clear program clear bit (NOC-6, bit 3).
5. Return to Connecting Procedure and try again for successful data transfer.

3000 I/O CHANNEL INTERFACE

The 3000 I/O channel SBU interface simulates a standard CDC 3000 series 12-bit I/O channel. It controls data transfers between 3518/3528 magnetic tape controllers and SBU memory. Figure 2-8 shows the relationship between the 3000 interface and other system elements.

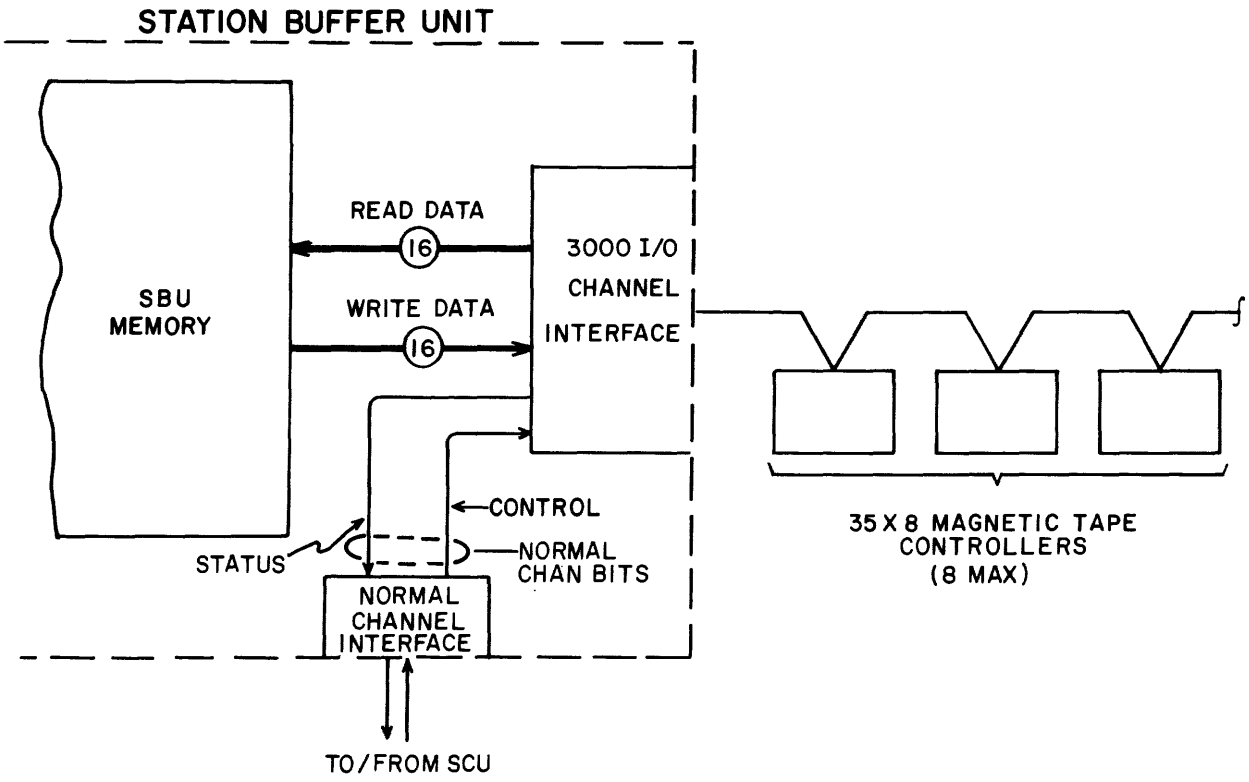


Figure 2-8. 3000 I/O Channel Interface System Relationship

loaded terminating address. If still another page of memory is required, the SCU must issue another page address after the operation has progressed into the second page. The SCU has the transfer time of an entire page to issue the next page address. This process allows a single data transfer operation to progress through several noncontiguous pages.

TERMINATING CONDITIONS

Several conditions may cause the 3000 interface to terminate a data transfer operation.

SBU terminating address/ current address compare	This compare can be used only to terminate a write operation.
End of record	The 3000 interface terminates a read operation when the peripheral device signals that it has reached the end of a record. This is the normal method of terminating a read operation.
Parity error	Three types of parity error terminate a data transfer operation early.

1. An SBU memory parity error can occur only when data is being extracted from memory during a write operation.
2. A read parity error is a transmission parity error in a data byte sent from a 3000 peripheral controller to the 3000 interface or a transmission parity error in a data byte sent from the 3000 interface to a 3000 peripheral controller.
3. Write parity error.

The terminate-on-parity error feature must be selected by a normal channel bit. If not selected, a parity error does not terminate a data transfer operation.

SCU CONTROL OF THE 3000 INTERFACE

The SCU exercises control over the 3000 interface and subordinate peripheral controllers through control information issued on normal output channels 5 and 6. Status information, available on normal input channels 5 and 6, allows the SCU to monitor operation of the 3000 interface and peripheral controllers. Figure 2-15 shows these normal channel bits.

Several types of control information must be sent to the 3000 interface to prepare for and initiate a read or write operation.

Starting address	Specifies the beginning of the source of destination area in SBU memory.
Table address	Specifies location of a code conversion table in SBU memory.
3000 interface function bits	Initiates read or write operations and specifies operating conditions within the 3000 interface.
Peripheral controller connect code	Selects and activates one of the eight possible controllers subordinate to the 3000 interface.
Peripheral controller function codes	Prepares the selected controller for an I/O operation
Master clear 3000 interface	Stops current I/O operation and clears all function selections within the 3000 interface.
3000 interface connect code	Connects 3000 interface to SCU normal input and output channels 5 and 6. A unique 4-bit code distinguishes the 3000 interface from all other I/O interfaces present in the SBU.
Terminating address	Specifies the upper limit of the destination area in SBU memory used for write operations only.

Three 16-bit status words are available on normal input channels 5 and 6. Two of these status words contain information about operating conditions within the 3000 interface. The third word contains status information from the connected peripheral controller.

The 3000 interface must be connected to the SCU in order to receive control information or return status information. The interface remains connected as long as the SCU holds the unique connect code assigned to the 3000 interface on output channel 6. The 3000 interface need not remain connected to the SCU normal channels to maintain a connected condition between the 3000 interface and a 3000 equipment and/or unit.

NORMAL CHANNEL ASSIGNMENTS

All of the normal channel signals used to control the 3000 interface are defined in the following section. The normal channel bit assignments given apply to the storage (media) station. 3000 interface bit assignments for other stations may be different. Appendix A of this manual contains a full set of normal channel assignments for all STAR stations.

NORMAL OUTPUT CHANNEL 5

Normal output channel 5 is used to transmit the following five classes of control information to the 3000 interface.

Terminating address

Starting address

Table address

3000 controller connect/function code

Internal function bits

Control information on normal output channel 5 must be accompanied by one of five strobe signals on normal output channel 6. The purpose of the strobe signals is to identify the class of information being issued and to transfer this information from normal output channel 5 into the interface. Figure 2-15 shows the relationship between the strobe signals and the five classes of control information.

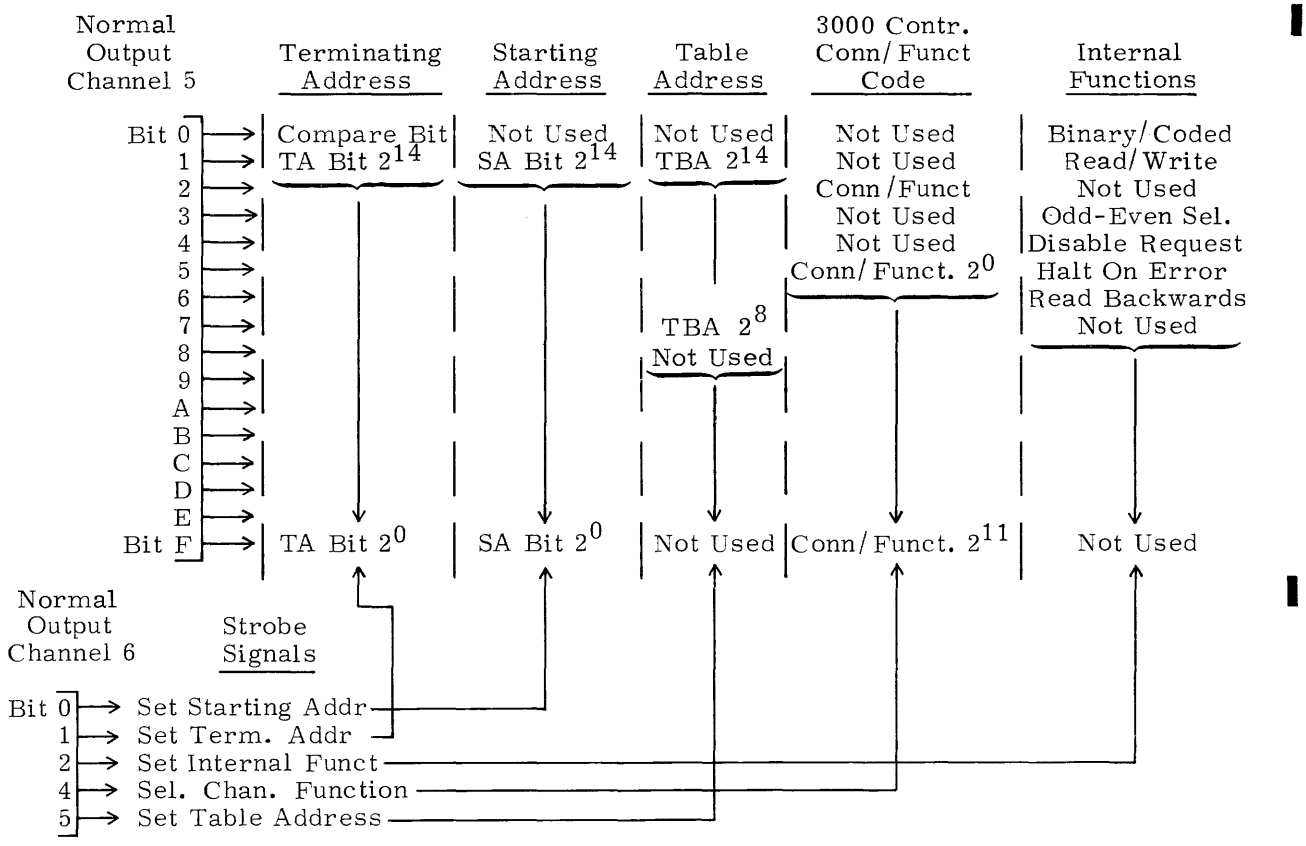


Figure 2-15. Normal Output Channel 5 Control Information, 3000 Interface

TERMINATING ADDRESS

The compare bit (bit 0) is a control bit that is transmitted along with the 15-bit terminating address. If set, this bit causes the 3000 interface to terminate a write operation when the terminating address is reached. It has no effect on a read operation.

The terminating address (bits 1 through F) has two parts.

Bits F through 5 (2^0 through 2^{10}); the lower 11 bits specify the terminating address within a 2K page.

Bits 4 through 1 (2^{11} through 2^{14}); next page address. For read or write operations longer than one page (2048 16-bit words), these bits specify the address of the next memory page.

The SCU must issue this address (2^0 through 2^{14}) in ones complement form.

STARTING ADDRESS

This 15-bit address specifies the starting SBU memory address for a read or write operation. The address must be issued in ones complement form.

TABLE ADDRESS

These seven address bits (channel bits 7 through 1) form the upper (most significant) part of a 15-bit table address. They specify the location of a 256-word code conversion table in SBU memory. When the code conversion mode is in effect, this table is used to convert from 6-bit to 8-bit format and vice-versa. This address must be issued in ones complement form.

3000 CONTROLLER CONNECT/FUNCTION CODE

The connect/function bit (bit 2), which accompanies the 12-bit connect/function code, determines whether the 3000 interface will transmit the code as a connect code or a function code (1 equals connect, 0 equals function). The channel function bit (NOC-6, bit 4) gates the code to the external equipment.

The 3000 channel connect/function code (bits 4 through F) is a 12-bit code forwarded to the 3000 peripheral controllers by the 3000 interface.

These six bits affect the 3000 interface. They specify the type of operation (read or write) that the interface is to perform and establish various operating conditions that affect the way the operation is performed. These bits are activated when the internal function select bit (NOC-6, bit 2) is set.

Bit 0, binary/coded

1. When clear, this bit establishes binary mode. In binary mode, no data conversion takes place during read or write operations.
2. When set, this bit establishes code conversion mode. When this mode is in effect, data is converted between 8-bit and 6-bit format. During a read (input) operation, each 6-bit input character is converted to a corresponding 8-bit character that is then stored in SBU memory. During a write (output) operation, the process is reversed; 8-bit characters from memory are converted to 6-bit output characters. A code conversion table, in SBU memory, specifies the equivalent 6-bit and 8-bit codes.

Bit 1, read/write

1. When clear, this bit initiates a read (input) operation.
2. When set, this bit initiates a write (output) operation.

Bit 2, unused

Bit 3, odd/even select

When clear, this bit causes the 3000 interface to reference all banks in memory consecutively.

When set, this bit causes the 3000 interface to reference every other bank in SBU memory.

Bit 4, disable request

When set, this bit conditions the 3000 interface to inhibit references to SBU memory. A read or write operation increments the memory address normally but the interface neither reads nor writes SBU memory.

Bit 5, halt on error

When set, this bit conditions the 3000 interface to enable the stop-on-parity error feature. The type of parity error affecting the 3000 interface may exist in any one of three categories; SBU memory, a transmission error, or in a magnetic tape controller. If this bit is not set, a parity error does not terminate a data transfer operation and the operation continues until halted by address compare or end of record.

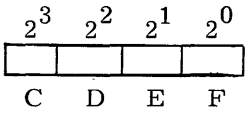
Bit 6, read backwards

When set, this bit reverses storage in memory during a read binary or read coded operation; for read binary, it also reverses the order of assembly. This feature is intended for use when data is being read backwards from tape.

TABLE 2-12. NOC-6 BIT DESCRIPTIONS FOR 3000 INTERFACE

Channel	Bit	Name	Function
NOC-6	0	SA SBU	This bit identifies the information on output channel 5 as an SBU starting address. Setting and then immediately clearing this bit transfers the starting address into the 3000 interface.
NOC-6	1	TA SBU	This bit identifies the information on output channel 5 as the SBU terminating address. Setting and then immediately clearing this bit transfers the terminating address into the 3000 interface.
NOC-6	2	Internal function	This bit identifies the information on output channel 5 as internal function bits. Setting and then immediately clearing this bit transfers the function bits to the 3000 interface. The conditions specified by the function bits remain in effect until new function bits are issued or the interface is cleared.
NOC-6	3	Program clear	This bit clears the 3000 interface. Setting this bit causes the clearing action to take place.
NOC-6	4	Channel function	This bit identifies the information on output channel 5 as a 3000 channel connect or function code. Setting and then immediately clearing this bit causes the 3000 interface to transmit the code to the subordinate 3000 peripheral controllers.
NOC-6	5	Table address-SBU	This bit identifies the information on output channel 5 as the table address. Setting and then immediately clearing this bit transfers the table address (output channel 5, bits 1 through 8) to the 3000 interface.
NOC-6	6	Current address-SBU	Setting this bit selects the current SBU memory address for input as a status word on input channel 5. Once selected, current address status remains available until this bit is

TABLE 2-12. NOC-6 BIT DESCRIPTIONS FOR 3000 INTERFACE (Cont'd)

Channel	Bit	Name	Function
			cleared. When current address status is not selected, the default status word is available on input channel 5.
NOC-6	7-B	Unused	
NOC-6	C-F	Interface connect	Interface connect codes for the 3000 interfaces are: 3000 Channel 0: code C_{16} (1100_2) 3000 Channel 1: code D_{16} (1101_2) This code connects the 3000 interface to SCU normal input and normal output channels 5 and 6 for control purposes. The paths between the normal channels and 3000 interface remain connected only as long as the proper connect code is present on output channel 6. 

NORMAL INPUT CHANNEL 5

Two status words (refer to Table 2-14) from the 3000 interface are available to the SCU on input channel 5.

When the SCU issues the 3000 interface connect code, default status is automatically selected. Current address status is selected by bit 6, normal channel 6.

NORMAL INPUT CHANNEL 6

A 12-bit status word and four control signals from the connected 3000 controller are available on input channel 6 (refer to Table 2-15).

TABLE 2-15. NIC-6 STATUS WORD BIT DESCRIPTIONS FOR 3000 INTERFACE

Channel/Bit	Name	Function
NIC-6/bit 0	Write parity error	This control signal indicates that the 3000 controller has detected a parity error in a data byte or function code sent from the 3000 interface.
NIC-6/bit 1	End of record	This control signal indicates that the 3000 controller has completed sending a record of data.
NIC-6/bit 2	Reject	This control signal indicates the 3000 controller has rejected a function code sent from the 3000 interface, or the 3000 controller failed to respond to a function code within 100 microseconds.
NIC-6/bit 3	Reply	This control signal indicates that the 3000 controller has accepted one of the following units of information sent from the 3000 interface. Connect code Function code Output data byte
NIC-6/bit 4 ↓ NIC-6/bit F	Status bit 11 ↓ Status bit 0	12-bit status word from 3000 controller. Each bit indicates the presence of some operating condition such as ready or busy. The meaning of the bits is different for each type of controller. Refer to appendix A and B for magnetic tape unit status bits.

SCANNER STATUS BITS

Several status bits for the 3000 interface appear in the SBU scanner status word. In the media station, these bits are available on normal input channel 6 (refer to Table 2-16). To access the scanner status word, the SCU must issue the scanner connect code (6_{16} for the media station).

TABLE 2-16. 3000 INTERFACE SCANNER STATUS BITS

Channel/Bit	Name	Function
NIC-6/Bit 6 NIC-6/Bit 8	Response, 3000-0 Response, 3000-1	Indicates that a 3000 controller has returned one of the following response signals to the 3000 interface. End of record Interrupt The specific condition causing response status can be determined by checking 3000 interface status on NIC-5 and NIC-6.
NIC-6/Bit 0 NIC-6/Bit 1	Terminating address empty, 3000-0 Terminating address empty, 3000-1	Indicates that a page boundary has been reached. In multipage operations, it means that the operation has jumped to the next page. If yet another page is required, a new next-page address can now be loaded. The status bit goes to 0 when a new page address is loaded.
NIC-6/Bit 7 NIC-6/Bit 9	Address compare, 3000-0 Address compare, 3000-1	Indicates that a write operation has reached the terminating address and has terminated. Not significant for a read operation.

e. Wait for one of the following scanner status bits.

TA empty status - NIC-6, bit 6 or 8
(Indicates the read operation has progressed to next page.)

Response status - NIC-6, bit 0 or 1
(Indicates that 3000 controller has terminated the read operation or has sent an interrupt.)

1) If TA empty status occurs:

   a) Connect 3000 interface according to step 1.

   b) Load new next-page address according to 5c.

   c) SCU may disconnect from the 3000 interface.

   d) Go back to step 6e.

2) If response status occurs:

   a) Check status available on NIC-5 and NIC-6 to determine if operation terminated normally. Refer to step 7. End of record status indicates normal termination.

3) To determine last word filled in SBU memory:

   a) Connect 3000 interface according to step 1.

   b) Set and then clear current address bit (NOC-6, bit 6). (This selects current address status on NIC-5.)

   c) Input to A register from NIC-5.
   (Bits 5 through 15 contain last word address in final page.)

4) To determine number of bytes in last word:

   a) Connect 3000 interface according to step 1.

   b) Set and then clear table address bit, NOC-6, bit 6.
   (In this case, this is a dummy command that serves only to clear the interface logic to select default status.)

   c) Input to A register from NIC-5.
   (Bits 9 through 12 contain the byte count.)

7. Status input procedure

   a. Controller status

      1) Connect interface and controller (refer to steps 1 and 2).

      2) Input to A from NIC-6.

   b. Default status

      1) Connect interface (refer to step 1).

      2) NOC-6, bit 6 must be clear.

      3) Input to A from NIC-5.

   c. Current address status

      1) Connect interface (refer to step 1).

      2) Set NOC-6, bit 6.

      3) Input to A from NIC-5.

7000 I/O CHANNEL INTERFACE

The 7000 I/O channel interface coordinates data word-size conversion and provides buffering for data transfer between SBU memory and a 7000 peripheral device such as a drum or disk storage subsystem (Figure 2-16). The SCU initiates data transfer operations, monitors status, and terminates these processes through normal channel inputs to the 7000 I/O interface. A 7000 I/O interface contains a control channel and a data channel. The control channel supplies function codes to the system and receives status reports from the system. The data channel exclusively handles data both to and from the peripheral system.

Two 7000 I/O interfaces may operate simultaneously in the SBU completely independent of each other. The SCU differentiates one 7000 I/O interface from the other by using a different connect code for each interface.

The following paragraphs of this subsection describe only the programming characteristics of the 7000 I/O interface; they do not cover the peripheral subsystems that can be connected to the interface. The reader should be familiar with 7000 I/O channel operation and the appropriate programming conventions in order to fully understand this material.

MAIN FUNCTIONS

The principal functions of the 7000 I/O interface are:

Issues function codes to 7000 peripheral subsystems

Governs exchange of data between peripheral subsystems and SBU memory

Performs word assembly/disassembly operations. During input operations, the interface breaks 12-bit bytes from the subsystem into 4-bit segments and packs four of these segments into each 16-bit SBU memory word. During output operations, the interface reverses the process.

Provides a path from the 7000 peripheral subsystem to the SCU for a 12-bit controller status word.

Provides several status bits from the 7000 peripheral subsystem which form part of the SBU scanner status word.

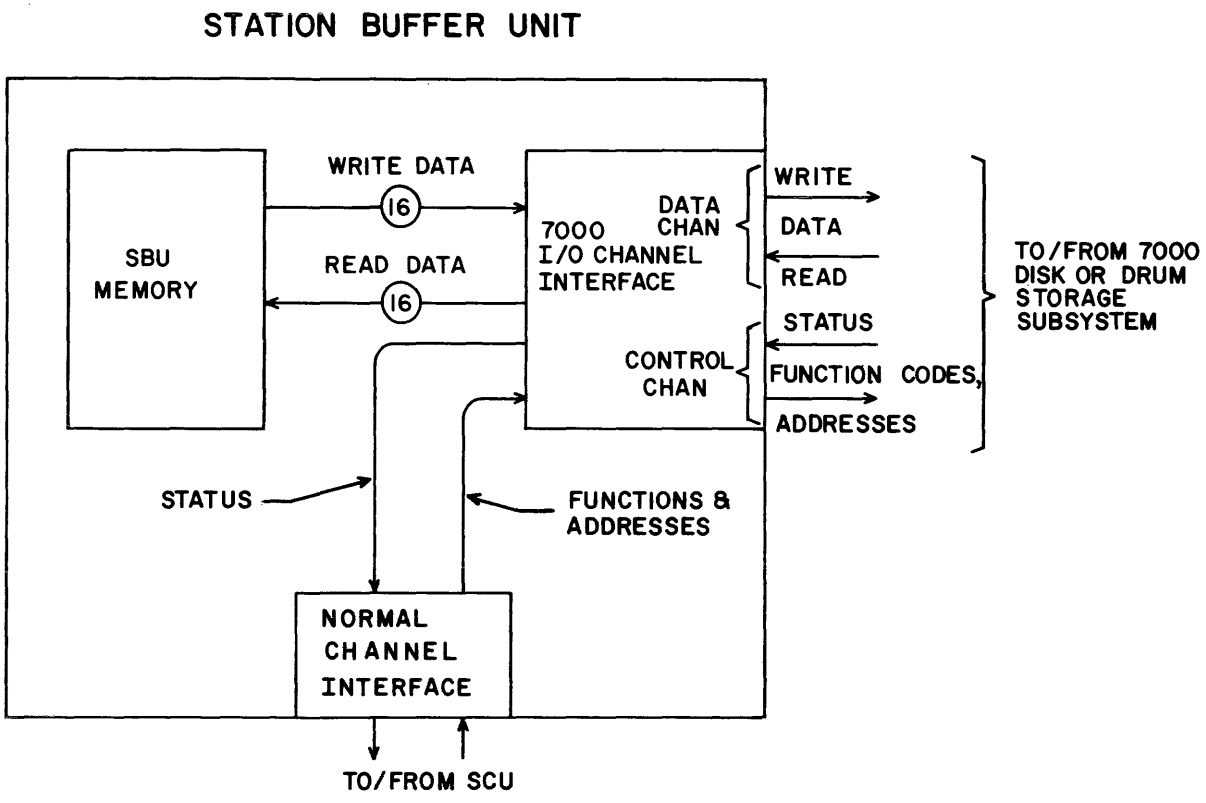


Figure 2-16. 7000 I/O Channel Interface System Relationship

The SCU controls all of these functions by issuing control information on normal output channels 5, 6, and 7. Fulltime attention of the SCU is not required once an operation has been initialized, since the 7000 interface transfers the specified number of data words without continued support from the SCU.

DATA TRANSFERS

All data transfer operations involve the exchange of blocks of data words between SBU memory and the 7000 peripheral subsystem. Before the SCU initiates a data transfer operation, it sends a starting address to the SBU to specify the beginning location in the buffer area of SBU memory where that data word is stored. Likewise, terminating addresses determine the stopping point in SBU memory for that data word. There are two types of data transfer operations, read and write.

The SCU sends function codes to the peripheral subsystem instructing it to perform specified operations. Bits 2^{11}, 2^{10}, and 2^{9} of the function word form a 3-bit function code which determines the operation that will be performed; for example, 001 for write, 000 for read, etc. Also, bit 2^{14} of the function word must be set to a 1 in order to initiate a data transfer. Otherwise, it must remain at a 0.

READ (INPUT) OPERATIONS

The SCU issues a starting address followed by the read function word to initiate the read operation. During this operation, 12-bit words or data bytes from the 7000 peripheral subsystem are divided into 4-bit segments. These segments are then packed into 16-bit words for storage in SBU memory. Figure 2-17 illustrates this procedure.

A terminating address also previously issued by the SCU terminates a read operation. If more than one area in memory is required for the number of data words coming from the 7000 peripheral subsystem, the SCU program must specify another starting and terminating address for the additional data words. A read operation may also be terminated by any abnormal condition, a not ready, a parity error at the end of the data transfer, etc.

Drum or disk parity error	This condition indicates that the 7000 storage subsystem detected a parity error at the end of a read operation or a skew error during a read operation.
Drum or disk abnormal	This condition occurs if the disk or drum becomes not ready or if the storage unit itself detects an unsafe condition. Unsafe conditions could be items such as read and write commands occurring simultaneously, commands received when disk not on-cylinder, improper number of heads selected, etc.

Once an error condition has been established, a detailed status check of the 7000 peripheral device should be made to further identify the source of the malfunction.

In all cases, the occurrence of an error condition stops the 7000 interface operation. If the error condition was an SBU parity error, the bank counter logic preserves the count relating to the address of the bank which failed. The count in the bank counter logic is four counts greater than the bank in which the error occurred. The difference is because of memory cycle timing in the SBU.

Each error condition is cleared by a program clear and must be followed by a new function code in order to reinitiate the data transfer.

STATUS

Three types of status information from the 7000 interface are available to the SCU when used in the disk station. They are normal input channels 5 and 7 and scanner status. In the drum station, the status available to the SCU is obtained via normal input channel 5 or the scanner.

NORMAL INPUT CHANNEL 5 STATUS

Several miscellaneous status bits, such as SBU parity error, disk or drum sector count, bank counter count, disk or drum abnormal, etc., appear on normal input channel 5 for both stations. Tables 2-17, 2-18, and 2-19 define each of these status bits.

SCANNER STATUS

Several 7000 interface status bits (actually from the peripheral device) are available to the SCU as part of the SBU scanner status word that appears on normal input channel 6. All 7000 scanner status bits are applicable to both the 7000-0 and 7000-1 interfaces and are listed as follows:

HCD Station	Drum Station
Disk on-cylinder	Drum sector count (2^0)
Disk error	Drum end of transfer (2^0)
Disk end of transfer (2^1)	Drum error
Disk end of transfer (2^0)	

The meanings of these bits are explained in Tables 2-17 and 2-18.

RETURN ADDRESS STATUS

During 7000 interface/SBU memory read or write operations occurring in the disk station, the current SBU memory address is available to the SCU via normal input channel 7.

TABLE 2-17. BIT DESCRIPTIONS FOR 7000 INTERFACE/NIC-5 AND 6 (DRUM STATION)

Channel	Bit	Name	Function
NIC-5	0	SBU parity error	This bit is used for indicating that a parity error occurred in SBU memory. Bank count FFs in 7000 interface stops at a $\overline{\text{count}}$ four counts greater than bank in which parity error occurred.
NIC-5	1 2 3	$\overline{\text{Bank ctr}}$ 2^2 2^1 2^0	These three bits are the SBU not bank address count.
NIC-5	4 ↓ A	Drum SC 2^6 2^0	These seven bits are the drum sector count.
NIC-5	B	Drum sector stable	This status bit indicates that drum head is not near a sector boundary and that the sector address can be sampled to obtain an accurate address location of the head.
NIC-5	C	Drum EOT bit 2^1	This status bit represents the upper bit of a 2-bit end of transfer counter.
NIC-5	D	Drum abnormal	This status bit indicates an abnormal condition on the 7000 interface connected to the drum.
NIC-5	E	Drum parity error	This status bit indicates that a parity error occurred on the drum.
NIC-5	F	Drum ready	This status bit indicates that the drum is physically ready to operate.
	Scanner Status		
NIC-6	0, 2	Drum SC 2^0	Used with both 7000 interfaces to denote sector count.
NIC-6	1, 3	Drum EOT bit 2^0	Used with both 7000 interfaces to denote the lower order bit of the end of transfer counter.
NIC-6	9, A	Drum error	Used with both 7000 interfaces to indicate an inclusive OR of any drum error detected.

TABLE 2-18. BIT DESCRIPTIONS FOR 7000 INTERFACING/NIC -5, -6, AND -7 (HCD STATION)

Channel	Bit	Name	Function
NIC-5	0	SBU parity error	This bit is used for indicating that a parity error occurred in SBU memory.
NIC-5	1 2 3	$\overline{\text{Bank ctr}}$ 2^2 2^1 2^0	These three bits are the SBU not bank address count.
NIC-5	4 ↓ 9	Disk SC 2^5 ↓ 2^0	These six bits are the disk sector count.
NIC-5	C	Disk not on-cylinder	This bit indicates that the disk file is in the process of positioning.
NIC-5	D	Disk abnormal	This status bit indicates an abnormal condition on the 7000 interface connected to the disk.
NIC-5	E	Disk parity error	This status bit indicates that a parity error occurred in the disk unit.
NIC-5	F	Disk not ready	This status bit indicates that the disk unit is not physically ready to operate.
NIC-7	0 ↓ 2 3	Return function ↓ Return function	Three of these bits are function identifiers which, except for bit 2^{14}, are not used by the hardware but can be used by station software.
	Scanner Status		
NIC-6	0, 4	Disk on-cylinder	Bit 0 (for 7000-0) and bit 4 (7000-1) used to indicate whether or not disk is positioned on requested cylinder.
NIC-6	1, 5	Disk error	Indicates an inclusive OR of any error detected by the 7000 interface (bit 1 for 7000-0, bit 5 for 7000-1)
NIC-6	2, 3, 6, 7	Disk EOT, 2^0 and 2^1	Two status bits used to indicate the status of the end of transfer counter. Bit 2: 7000-0 disk EOT 2^1 Bit 3: 7000-0 disk EOT 2^0 Bit 6: 7000-1 disk EOT 2^1 Bit 7: 7000-1 disk EOT 2^0

TABLE 2-19. BIT DESCRIPTIONS FOR 7000 INTERFACE/NOC-5 AND -6 (DRUM STATION)

Channel	Bit	Name	Function
NOC-5	0	EDS/SDS	EDS: The end data sequence bit accompanying the terminating address indicates that the data transfer(s) will end with the current transfer. This bit is used in streaming several data blocks in succession. SDS: The start data sequence bit accompanying the starting address indicates the start of a data transfer. This bit is used in streaming data from SBU memory to the drum when several blocks of SBU memory are transferred.
NOC-5	1 ↓ F	SA/TA/funct bit 2^{14} ↓ SA/TA funct bit 2^{0}	These bits serve three purposes. 1. Transmit terminating address to SBU. This 15-bit address word is sent to the SBU as the last address of a data block. It is used to end block operations between the SBU and 7000 interface. 2. Transmit starting address to SBU. This 15-bit address word is sent to the SBU as the beginning or starting address of a data block. 3. Transmit function code or bits to the 7000 interface. These 15 bits are available to the SCU for sending a function code or bits to the selected 7000 interface.
NOC-6	0	Starting address SBU (7000-0 and 1)	This set/clear † bit is used to strobe the starting address, transmitted by the SCU into SBU memory for use with the selected 7000 interface.
NOC-6	1	Terminating address SBU (7000-0 and 1)	This set/clear † bit is used to strobe the terminating address, transmitted by the SCU into SBU memory for use with the selected 7000 interface.
NOC-6	2	Function	This set/clear † bit strobes the external function code sent by the SCU into the connected 7000 interface.
NOC-6	3	Program clear	This bit is interpreted as a master clear.

† A set/clear bit is set and immediately cleared in order to perform its intended function.

TABLE 2-19. BIT DESCRIPTIONS FOR 7000 INTERFACE/ NOC-5 AND -6 (DRUM STATION) (Cont'd)

Channel	Bit	Name	Function
NOC-6	4	Disable Error	When this bit is a 1, it disables the effect of the composite error signal in the 7000 interface. The composite error signal is internal to the 7000 interface and is enabled by a 1 on NIC-5, bits 0, E, or F. The disable error signal clears the composite error signal, disables the data record pulse to the drum controller, and allows software to select alternate levels of controller status via external functions.
NOC-6	5 ↓ B		These bits of NOC-6 are not used with the 7000 interface.
NOC-6	C ↓ F	Connect Code	These bits are used by the SCU to connect the 7000 interface in the SBU with the SCU normal channels (refer to Table 2-1 for codes).

PROGRAMMING SEQUENCES

The following paragraphs provide typical examples of the programming steps required to initiate and control data transfer operations through the 7000 interface. The example that follows is based upon an output data transfer to the drum.

CONNECTING TO 7000 INTERFACE

1. Place either connect code 2_{16} (7000 interface 0, drum station) or 1_{16} (7000 interface 1, drum station) on NOC-6, bits C through F. For the disk station, use 2_{16} for 7000 interface 0 or 3_{16} for 7000 interface 1.
2. If only the head selection procedure is required, proceed to Send Function in this section.

SEND STARTING OR TERMINATING ADDRESS SETS

Up to four sets of starting and terminating addresses may be sent to the 7000 interface. If a four-section data transfer is to be made, the SCU program must ensure that each address set is transferred in time to guarantee a continuous data transfer.

1. Place starting address of first data transfer on NOC-5, bits 0 through F. Set bit 0 of the first of the starting address words to inform the interface that this request is the start of a data sequence. (Refer to Figure 2-20.1.) For all other starting addresses, leave bit 0 clear.
2. Set and clear bit 0 (starting address SBU) of NOC-6 to strobe the starting address into the 7000 interface.
3. Place the terminating address of the data transfer corresponding to the starting address of step 2 on NOC-5, bits 0 through F. If this is the last terminating address of a data sequence, set bit 0 of the address. (Refer to Figure 2-20.1.) For all other terminating addresses, leave bit 0 clear.
4. Set and clear bit 1 (terminating address SBU) of NOC-6 to strobe the terminating address into SBU memory.
5. Repeat steps 1 through 4, as required.

TABLE 2-19.1. BIT DESCRIPTIONS FOR 7000 INTERFACE/ NOC-5, -6, AND -7 (HCD STATION)

Channel	Bit	Name	Function
NOC-5	0	EDS/SDS	EDS: The end data sequence bit accompanying the terminating address indicates that the data transfer(s) will end with the current transfer. This bit is used in streaming several data blocks in succession. SDS: The start data sequence bit accompanying the starting address indicates the start of a data transfer(s). This bit is used in streaming data from SBU memory to the disk when several blocks of SBU memory are transferred.
NOC-5	1 ↓ F	SA/TA/funct bit 2^{14} ↓ SA/TA funct bit 2^{0}	These bits serve three purposes. 1. Transmit terminating address to SBU. This 15-bit address word is sent to the SBU as the last address of a data block. It is used to end block operations between the SCU and 7000 interface. 2. Transmit starting address to SBU. This 15-bit address word is sent to the SBU as the beginning or starting address of a data block. 3. Transmit function code or bits to the 7000 interface. These 15 bits are available to the SCU for sending a function code or bits to the selected 7000 interface.
NOC-6	0	SBU starting address (7000-0 and -1)	This set/clear † bit is used to strobe the starting address, transmitted by the SCU into SBU memory for use with the selected 7000 interface.
NOC-6	1	SBU terminating address (7000-0 and -1)	This set/clear † bit is used to strobe the terminating address, transmitted by the SCU into SBU memory for use with the selected 7000 interface.
NOC-6	2	Function	This set/clear † bit strobes the external function codes sent by the SCU into the connected 7000 interface.

† A set/clear bit is set and immediately cleared in order to perform its intended function.

TABLE 2-19.1. BIT DESCRIPTIONS FOR 7000 INTERFACE/ NOC-5, -6, AND -7 (HCD STATION) (Cont'd)

Channel	Bit	Name	Function
NOC-6	3	Program clear	This bit is interpreted as a master clear.
NOC-6	4	Disable error	This signal clears the composite error signal in the 7000 interface and allows software to select alternate levels of disk controller status via external functions.
NOC-6	5, 6, 7		Not used
NOC-6	8	NOC-7 Select	When this bit is set, NOC-7 is connected to NIC-6.
NOC-6	9	NOC-5 Select	When this bit is set, NOC-5 is connected to NIC-6.
NOC-6	A	NOC-6 Select	When this bit is set, NOC-6 is connected to NIC-6.
NOC-6	B	Scanner Select	When this bit is set, the scanner program is connected to NIC-6.
NOC-6	C ↓ F	Connect code	These bits are used by the SCU to connect the 7000 interface in the SBU with the SCU normal channels (refer to Table 2-1 for codes).
NOC-7	0	EDS/SDS	Same function as that given above for NOC-5, bit 0.
NOC-7	1 ↓ F	SA/TA/funct bit ↓ SA/TA/funct bit	Same three functions as those given above for NOC-5, bits 1 through F.
NOC-5, NOC-7	0	Software bit 2^2	These bits on NOC-5 and NOC-7 serve another purpose in addition to those already listed. These bits represent the external function stack in the 7000 interface and can be used by the operating system as software flags. These bits are not used by the hardware.
	2	2^1	
	3	2^0	
NOC-5, NOC-7	1	Data Sequence	This bit accompanies the external functions on NOC-5 and NOC-7. It indicates those disk functions that are data related (read/write).

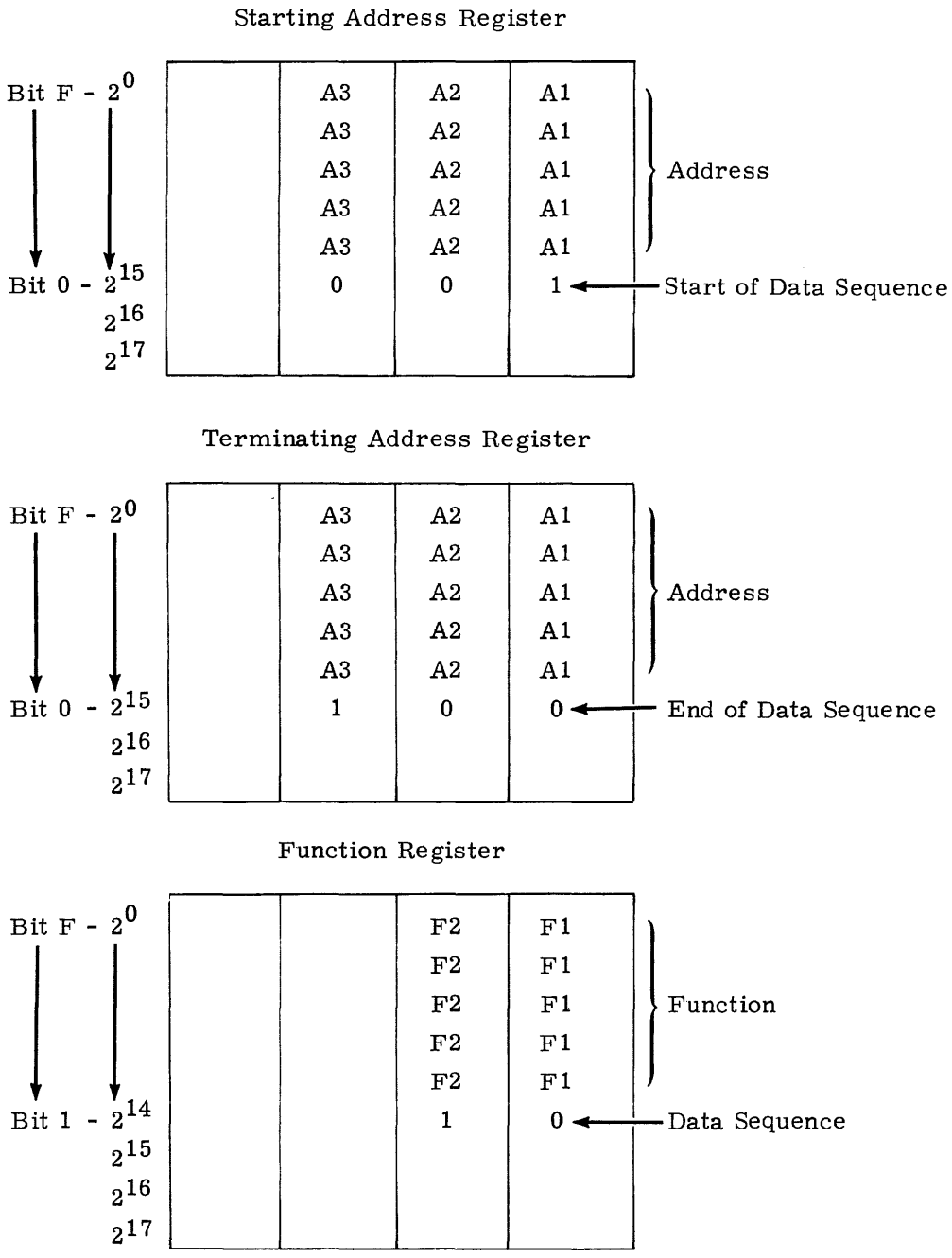


Figure 2-20.1 Typical Register Configuration
For a Data Transfer To The Drum

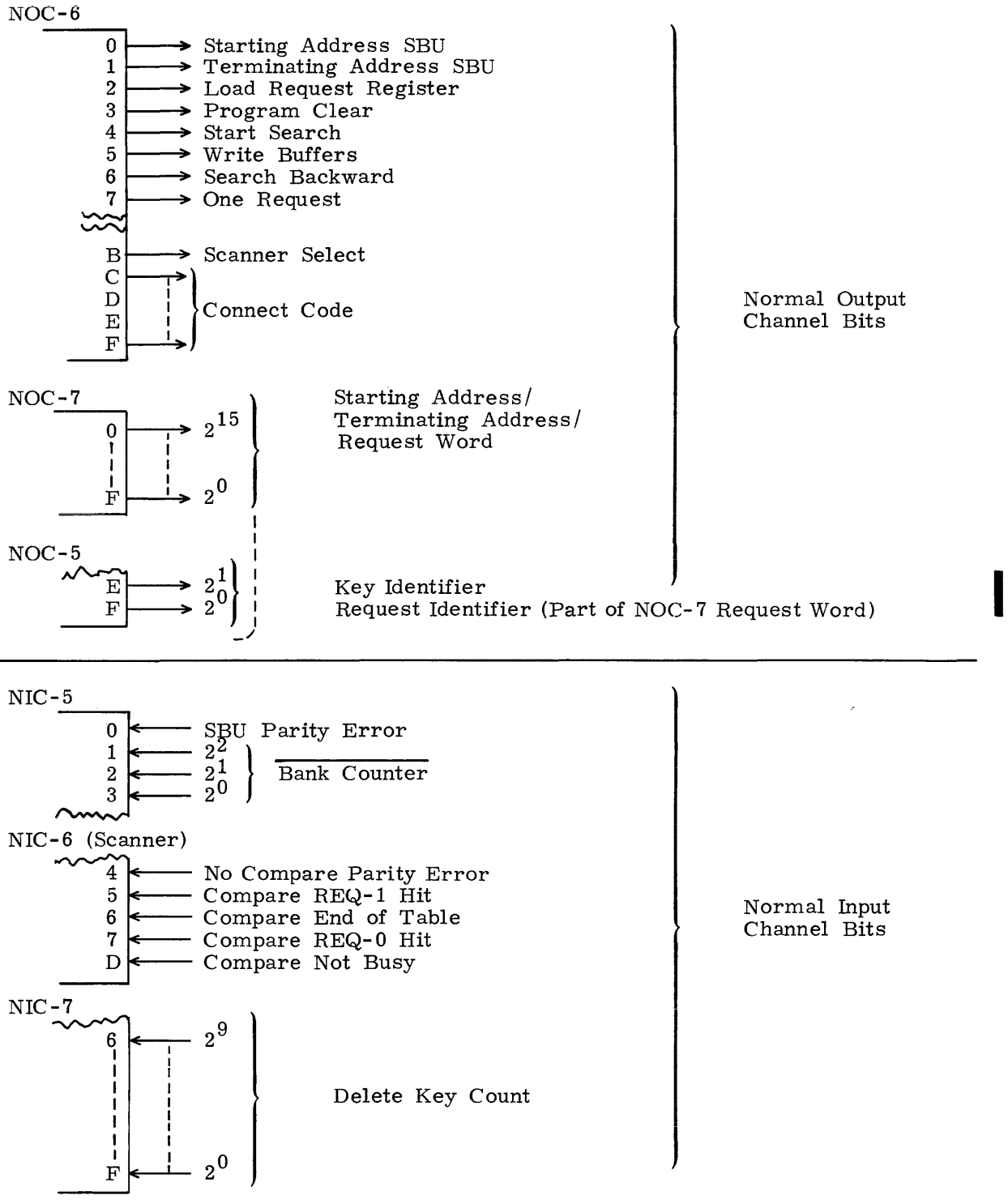


Figure 2-22. Normal Channel Bit Assignments, Index Compare Logic (Drum Station)

SCU CONTROL OF INDEX COMPARE LOGIC

The SCU controls the IC logic using control information issued on normal output channels 5, 6, and 7 (Figure 2-22). Also, the status of various operations occurring within the IC interface is monitored via normal input channels 5, 6, and 7.

There are three basic types of operations that the SCU may instruct the IC logic to perform: the key search, key and virtual address search, and delete key. Each of these operations search a table of 64-bit entries in SBU memory. Prior to the beginning of each type of operation, the SCU instructs the IC logic as to the objective of the search and defines the limits of the area in memory to be searched. The format of each 64-bit entry in the SBU memory table is shown in Figure 2-23. Since the table is in the even memory banks only, the first word is in bank 0, the second in bank 2, etc.

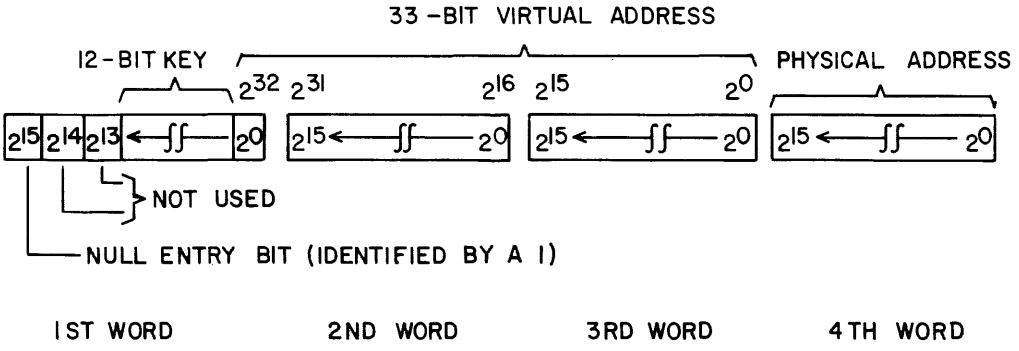


Figure 2-23. Memory Table Word Format

SCU SEARCH REQUESTS

The SCU may load as many as six 18-bit search request words into the IC logic which compares the request words against table entries from SBU memory. The SCU may issue several combinations of requests which may instruct the IC logic to search for a single key, two keys, or one or two keys and virtual address combinations as the objects of the search through memory. Special operations include a search backward through the table and delete key where a table entry is effectively deleted by setting the null bit (2^{15}) in the key. Typical request word formats are shown in Figure 2-24.

Bit 2^{13} of the first request word of request 0 must be set to perform a delete key operation. In this operation, the search through the memory table does not stop even though a satisfying condition is found. Instead, the search continues through the table for all specified keys matching the SCU's request until the end of the table is reached. The other conditions which may terminate a delete key operation prior to reaching the end of the table are a parity error or master or program clear. Entries temporarily stored in the IC logic buffers may be stored back in SBU memory exactly as entries are stored for the key search operations.

NORMAL CHANNEL BIT ASSIGNMENTS

All of the normal channel bit assignments used to control the IC logic are defined either in the following paragraphs or in Tables 2-20 and 2-21. The explanations of bit assignments given apply to the drum peripheral station. If the IC logic is used in other stations, bit assignments may be different. Appendix A contains a complete set of normal channel bit assignments for all STAR stations.

The SCU uses normal output channel 7 to transfer the following classes of control information to the IC logic.

Starting address
Terminating address
IC logic function bits
Search keys

Control information placed on NOC-7 must be accompanied by the appropriate strobing signal on NOC-6. The strobe signal is used to identify the class of information being issued and to transfer the information from NOC-7 into the IC logic.

TABLE 2-20. BIT DESCRIPTIONS FOR INDEX COMPARE/NOC-6 AND 7 (DRUM STATION)

Channel	Bit	Signal Name	Function
NOC-5	E	SCU key identifier	When set, this bit indicates that the first word of a request contains a 12-bit job identifier.
NOC-5	F	SCU request identifier	This bit identifies the request (0 or 1) to which each 18-bit request word belongs.
NOC-6	0	Starting address SBU	This bit gates the starting address on NOC-7 into the starting address register.
NOC-6	1	Terminating address SBU	This bit gates the terminating address on NOC-7 into the terminating address register.
NOC-6	2	Load request register	This bit is used for gating a request word from the SCU into the request register.
NOC-6	3	Program clear	This bit is interpreted as a master clear.
NOC-6	4	Start search	This bit enables the start of the search of the table in SBU memory.
NOC-6	5	Write buffers	This bit enables the transfer of data from the buffer registers of the compare interface to SBU memory.
NOC-6	6	Search backward	Use of this bit enables the index compare logic to search backward through the table in core memory.
NOC-6	7	One request	The set condition of this bit initiates the one request circuit in the index compare logic and causes it to search for a null list entry in addition to an entry equal to a single request.
NOC-6	B	Scanner select	This bit selects the scanner status bits on NIC-6.

TABLE 2-20. BIT DESCRIPTIONS FOR INDEX COMPARE/NOC-6 AND 7 (DRUM STATION) (Cont'd)

Channel	Bit	Signal Name	Function
NOC-6	C ↓ F	Connect Code 2^3 ↓ Connect Code 2^0	These bits are used by the SCU to connect the IC logic in the SBU with the SCU normal channels (refer to Table 2-1 for codes).
NOC-7	1 ↓ C	SA/TA/request bit 2^{14} ↓ SA/TA/request bit 2^3	These bits serve three purposes. 1. Starting address - This 12-bit word is sent to SBU memory via the IC logic as the beginning or starting address of a data block. 2. Terminating address - This 12-bit word is sent to the SBU via IC logic to indicate the end of a data block for which the IC logic was performing a compare operation. 3. Request bits - When NOC-7 is used to transmit request bits or a request word to the IC logic, all 16 bits may be used (0-F, 2^{15}-2^0).

TABLE 2-21. BIT DESCRIPTIONS FOR INDEX COMPARE/NIC-5, -6, AND -7

Channel	Bit	Name	Function
NIC-5	0	SBU parity error	This status bit indicates that a parity error occurred in SBU memory.
NIC-5	1 2 3	$\overline{\text{Bank ctr}}\ 2^2$ 2^1 2^0	When an SBU memory parity error is detected, the memory bank with the parity error is found by complementing the bank count status and then counting back four memory banks.
NIC-6	4	No compare parity error	This scanner status bit indicates whether or not a parity error occurred on data as it was read from SBU memory.
NIC-6	5	Compare request-1 hit	This scanner status bit is set if a match was made with request 1.
NIC-6	6	Compare end-of-table	This status bit indicates that the current address in the IC logic matches the terminating address and therefore means that the table search is complete.
NIC-6	7	Compare request-0 hit	This scanner status bit is set if a match was made with request 0.
NIC-6	D	Compare not busy	This scanner status bit indicates whether or not the IC logic has completed an address compare procedure.
NIC-7	6 F	Delete key count bit 2^9 2^0	These status bits indicate the total number of hits produced by altered table entries during a delete key operation (up to the limits of the counter).

PROGRAMMING SEQUENCES

The following procedures provide typical examples of the programming steps required to initiate and control address compare operations through the IC logic.

CONNECTING TO IC INTERFACE

1. Transmit the appropriate connect code (3_{16}) from the SCU to the IC logic using NOC-6, bits C through F.
2. Set and clear the program clear bit (NOC-6, bit 3).

TRANSMITTING KEY(S) FOR REQUEST(S)

1. Set or clear the request identifier bit (bit F of first word of request 0 or 1; refer to Figure 2-24). Set the key identifier bit.
2. Set the appropriate key bit (bit 2 for delete key operation or bit 1 for select key only search; refer to Figure 2-24). Set bit 0 for request 0, word 0 (start sequence).
3. Transmit the key bits (bits 2^1 through 2^{12} of first word of request 0 or 1) and bit 2^{32} of the virtual address to the IC logic via NOC-7.
4. Set and clear the load request register bit (NOC-6, bit 2).
5. Clear all bits set in step 2.
6. Repeat steps 1 through 5 to transmit a second request.

TRANSMITTING VIRTUAL ADDRESS PORTION(S) OF REQUEST(S)

1. Transmit second word of request via NOC-5, bits E and F, and all bits of NOC-7 to IC logic. Clear the key identifier bit via NOC-5.
2. Set and clear load request register bit via NOC-6, bit 2.
3. Repeat steps 1 and 2 for a second request (if used).
4. Transmit third word of request via NOC-5, bits E and F, and all bits of NOC-7 to IC logic.

Once the header information is completely read from the sector, the full status drops and the interface addresses a data page in memory (1 through 15) and transfers the entire data page from the sector to memory. The memory page addressed is specified by the starting address loaded during the initialization procedure.

Next, the interface does a check when the BCC is read from the sector. If the check fails, a read error status bit is sent to the SCU. If the check passes, a finished status bit is sent to the SCU.

After the software detects the finished status, it may read the next consecutive sector by sending a begin transfer command (provided header information was placed in SBU memory and a starting address was loaded when the full status dropped).

SBU MEMORY ADDRESSING

The SCU software must issue a starting address to the 844 interface at the time a read or write operation is initiated. The starting address specifies the location of the data page and also the location of the 32-word block of header information (address tags and preamble) for the data page. Since the data page is confined to only 2048 words of data, the software must reserve a separate page for the accompanying 32-word block of header information.

Hardwire connections on the interface main timing module allow selection of odd half banks, even half banks, or full banks addressing mode. When wired for odd banks, only odd memory banks (1, 3, 5, and 7) are selected. When wired for even banks, only even memory banks (0, 2, 4, and 6) are selected. Normally, the module is wired to select full banks (0 through 7). The software usually reserves page 0 for header information when full banks mode is selected. (Any page may be wired for the header information but the software must correspond.) Any one of the even pages (0, 2, 4, etc.) may be reserved for header information when even banks mode is selected or any one of the odd pages (1, 3, 5, etc.) when odd banks mode is selected. Figures 2-30 and 2-31 show the formats for full banks and half banks addressing.

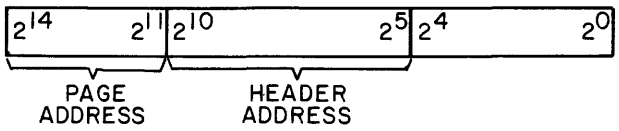


Figure 2-30. Full Banks Address Format, 844 Interface

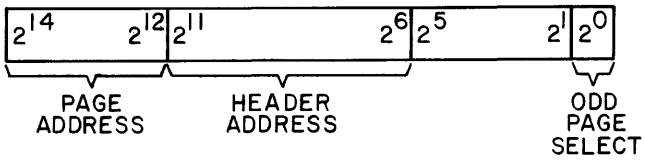


Figure 2-31. Half Banks Address Format, 844 Interface

The software places the starting address into the address register of the interface via the normal channels. Only page (whole sector) transfers take place between the interface and unit so that terminating addresses are not required. Bits 2^1 through 2^4 are hardwired to ground in the core control address register, and therefore, are always 0's. This condition restricts the starting address of the header to 32-word boundaries. During full banks mode, bit position 2^0 is forced clear, so that the boundaries would be 0000_{16}, 0020_{16}, 0040_{16}, etc.

When either odd or even half banks mode is hardwired in the main timing module, bit 2^0 is no longer used as part of the 32-word header address boundary. A 0 must be placed in bit position 2^5 to maintain the 32-word boundary. This shifts the header address one bit to the left, leaving only three bits for the page address. These three page address bits select one of eight odd pages (1, 3, 5, etc.) if a 1 is placed in bit position 2^0 or one of eight even pages (0, 2, 4, etc.) if a 0 is placed in bit position 2^0.

PARITY

A parity check is made by the interface on all data that is read from SBU memory. If the parity check fails, read error and transfer error status bits are sent to the SCU.

844 INTERFACE NORMAL CHANNEL SIGNALS

Tables 2-22 and 2-23 describe the normal input and output channel bits used with the 844 interface. Bit assignments in the table are for the 844 storage station. Interface bit assignments may be different in other stations. Refer to appendix A for a complete list of normal channel bit assignments for all stations.

The interface must remain connected to the SCU in order to receive control information from the SCU. The interface remains connected as long as the SCU holds the unique connect code, assigned to the interface, on output channel 6, bits C through F.

TABLE 2-22. NIC-6 AND -7 BIT DESCRIPTIONS FOR 844 INTERFACE

Channel	Bit	Name	Function
NIC-6	0	Unit busy	This status bit from the disk unit indicates that the unit selected by one of select unit bits (NOC-7) is reserved by the other 844 interface.
NIC-6	1 ↓ 9	Units 1 through 9 selected	Each of these status bits from the units indicates that the unit selected by one of select unit bits (NOC-7) is available and reserved.
NIC-6	A	Read error	This is a status bit from the interface that results from a parity error or a BCC error. The parity error may result on either the lower or upper half of a 16-bit word during a read operation from SBU memory. The BCC error results when the 16-bit BCC word read from the disk at the end of a page does not match the BCC word generated when the data page is read from the disk. The read error bit also sets the transfer error bit (NIC-7).
NIC-6	B	Tag BCC error	This interface status bit is used to indicate an address check code error when set in conjunction with the transfer error bit (NIC-7). The address check code error results when the 16-bit address check word read from the disk after the address tag word does not match the address check word generated when the address tag word is read from the disk.
NIC-6	C	Timing chain	This interface status bit indicates that it is too late to start a data transfer for the next consecutive disk sector. A retry should be attempted after a revolution of the disk. If a read error bit (NIC-6) occurs in conjunction with the timing chain bit, it indicates a parity error on the address tag word read from SBU memory.

TABLE 2-22. NIC-6 AND -7 BIT DESCRIPTIONS FOR 844 INTERFACE (Cont'd)

Channel	Bit	Name	Function
			If a read error bit (NIC-6) occurs without the timing chain bit, it indicates a BCC error on the data page read from the disk.
NIC-6	D ↓ F	$\overline{\text{SBU bank count}}$ 2^2 through 2^0	These three status bits give the not code of one of the eight SBU memory banks that was being accessed during a data transfer when a read error bit (NIC-6) was set. The memory bank with the error is found by complementing the bank count status code and counting back four memory banks.
NIC-7	0	Finished	This interface status bit indicates that the data transfer terminated normally.
NIC-7	1 ↓ 9	Units 1 through 9 on sector	Each of these status bits from the selected unit indicates that the addressed sector is one sector away from the heads. The signal is one sector in length.
NIC-7	A	Ready	This status bit from the disk unit indicates that the selected unit has completed its first seek. The unit does not accept seek commands until ready.
NIC-7	B	Transfer error	This interface status bit sets as a result of a read error (NIC-6), an address check code error (refer to tag BCC error, NIC-6), or an address tag compare error. The address tag compare error results when the address tag word read from SBU memory does not match the address tag word read from the disk.
NIC-7	C	On cylinder	This status bit from the disk unit indicates that the selected unit has positioned the read/write heads at the addressed cylinder.

TABLE 2-22. NIC-6 AND -7 BIT DESCRIPTIONS FOR 844 INTERFACE (Cont'd)

Channel	Bit	Name	Function
NIC-7	D	Seek error	This status bit from the disk unit indicates that the selected unit was unable to complete a move within 500 milliseconds or that the carriage has moved to a position outside the recording field.
NIC-7	E	Pack unsafe	This status bit from the disk unit indicates that the selected unit has a fault condition.
NIC-7	F	Full	This interface status bit indicates that new SBU memory address bits (NOC-7) and full bit (NOC-7) have been loaded into the interface address register. The software loads another address when the full status drops. It also indicates that a data page transfer has not yet begun. This marks a point of reference for determining whether an error occurred during address tag or data page transfer.

TABLE 2-23. NOC-6 AND -7 BIT DESCRIPTIONS FOR 844 INTERFACE

Channel	Bit	Name	Function
NOC-6	0 ↓ 6	Not used	
NOC-6	7	Load SBU address	This bit is used to gate the SBU memory starting address bits (NOC-7), write tag bit (NOC-7), write bit (NOC-7), full bit (NOC-7), and odd bit (NOC-7) into the interface address register.
NOC-6	8	Release	This bit in conjunction with function bit (NOC-6) enables a release signal to all units to clear the reserve status of the selected unit or units.
NOC-6	9	Function	This bit is used to gate the address and control bits 0 through 8 (NOC-7), difference select bit (NOC-7), clear fault bit (NOC-7), control select bit (NOC-7), sector select bit (NOC-7), and cylinder select bit (NOC-7) through the interface to the units.
NOC-6	A	Begin transfer	This bit initiates a read or write operation in the interface.
NOC-6	B	Not used	
NOC-6	C ↓ F	Connect code 2^3 through 2^0	These bits connect either 844-A or 844-B interface to the SCU. (Refer to Table 2-1 for 844 interface connect codes.)
NOC-7	0	Not used	
NOC-7	1	Select unit 1 †	This bit or one of select unit 2 through 9 bits (NOC-7) is used to select one of the nine units. The bit must be cleared to deselect the unit. Only one select unit bit should be set; otherwise, more than one unit would be selected.

See footnotes at end of table.

TABLE 2-23. NOC-6 AND -7 BIT DESCRIPTIONS FOR 844 INTERFACE (Cont'd)

Channel	Bit	Name	Function
NOC-7	2	Select unit 2 †	Refer to select unit 1 bit (NOC-7).
		or	
		Difference select † †	This bit is sent to all units and indicates that the address and control bits 0 through 8 (NOC-7) contain positioning information (difference between unit's present cylinder address and new interface address) for the selected unit.
		or	
		Write tag † † †	This bit enables the interface main timing to write address tags on the disk. The address tags include head gap, sync pattern, address tag word, and address check code. The write bit (NOC-7) must also be set for a write tags operation.
NOC-7	3	Select unit 3 †	Refer to select unit 1 bit (NOC-7).
		or	
		Clear fault † †	This bit is sent to all units and clears the fault condition in the selected unit.
		or	
		Write † † †	This set bit signals the interface to write an SBU memory data page onto the disk. A clear bit enables the interface to read a data page from the disk.
NOC-7	4	Select unit 4 †	Refer to select unit 1 bit (NOC-7).
		or	
		Control select † †	This bit is sent to all units and indicates that the address and control bits 0 through 8 (NOC-7) contain control information.
		or	
		Full † † †	This bit is sent to the interface address register along with the SBU memory address bits 2^5 through 2^{14} (NOC-7). It enables a full status in the interface. The full status clears in the interface when the page address is sent to the SBU memory.

See footnotes at end of table.

TABLE 2-23. NOC-6 AND -7 BIT DESCRIPTIONS FOR 844 INTERFACE (Cont'd)

Channel	Bit	Name	Function
NOC-7	5	Select unit 5†	Refer to select unit 1 bit (NOC-7).
		or	
		Sector select††	This bit is sent to all units and indicates that the address and control bits 0 through 8 (NOC-7) contain the address of the sector which generates the next on-sector signal. Only sectors 0, 8, and 16 are selected in order to divide the disk in three parts for full page data recording.
		or	
		Odd†††	This bit is used to select odd data pages (1, 3, 5, etc.) when set or even data pages (0, 2, 4, etc.) when clear. This function is applicable only during half banks mode (hardwire selection of odd or even banks on interface main timing module).
			NOTE The switch selects odd or even banks while the odd bit selects odd or even data pages.
NOC-7	6	Select unit 6†	Refer to select unit 1 bit (NOC-7).
		or	
		Cylinder select††	This bit is sent to all units and indicates that the address and control bits 0 through 8 (NOC-7) contain the new cylinder address.
		or	
		SBU memory address bit 2^{14}†††	This bit and SBU memory address bits 2^{13} through 2^{5} specify the starting address in SBU memory for a page of data and its accompanying header information.

See footnotes at end of table.

TABLE 2-23. NOC-6 AND -7 BIT DESCRIPTIONS FOR 844 INTERFACE (Cont'd)

Channel	Bit	Name	Function
NOC-7	7	Select unit 7†	Refer to select unit 1 bit (NOC-7).
		or	
		Address and control bit 8††	This bit and address and control bits 7 through 0 are sent to all units. Information for these bits is given in Table 2-24 and is determined by the accompanying difference select bit (NOC-7), control select bit (NOC-7), sector select bit (NOC-7), or cylinder select bit (NOC-7).
		or	
		SBU memory address bit 2^{13}†††	Refer to SBU memory address bit 2^{14} (NOC-7).
NOC-7	8	Select units 8 and 9†	Refer to select unit 1 bit (NOC-7).
	9	or	
		Address and control bits 7 and 6††	Refer to address and control bit 8 (NOC-7).
		or	
		SBU memory address bits 2^{12} and 2^{11}†††	Refer to SBU memory address bit 2^{14} (NOC-7).
NOC-7	A	Address and control bits 5 through 0††	Refer to address and control bit 8 (NOC-7).
	F	or	
		SBU memory address bits 2^{5} through 2^{0}†††	Refer to SBU memory address bit 2^{14} (NOC-7).

†This bit is set, provided the load SBU address bit (NOC-6) and function bit (NOC-6) are set.

††This bit is set, provided the load SBU address bit (NOC-6) is not set and function bit (NOC-6) is set.

†††This bit is set, provided the load SBU address bit (NOC-6) is set.

TABLE 2-25. NIC-6 AND -7 BIT DESCRIPTIONS FOR MDD INTERFACE

Channel	Bit	Name	Function
NIC-6	0 ↓ 8	Unit 0 selected through unit 8 selected	Each of these status bits from the MDD units indicates that the unit selected by the unit select and logic no. bits (NOC-5) is available and reserved NOTE When the standby unit replaces another unit on line, it takes the select code of the replaced unit but has its own unit selected status line.
NIC-6	9	Full	This interface status bit indicates that new SBU address bits (NOC-5) and full bit (NOC-5) have been loaded into the interface address register. The software loads another address when the full status bit drops. It also indicates that a data page transfer has not yet begun. This marks a point of reference for determining whether an error occurred during address tag or data page transfer.
NIC-6	A	Read error	This is a status bit from the interface that results from a parity error or a BCC error. The parity error may result on either the lower or upper half of a 16-bit word during a read operation from SBU memory. The BCC error results when the 16-bit BCC word read from the disk unit at the end of a data page does not match the BCC word generated when the data page is read from the disk. The read error bit also sets the MDD error bit (NIC-7).

TABLE 2-25. NIC-6 AND -7 BIT DESCRIPTIONS FOR MDD INTERFACE (Cont'd)

Channel	Bit	Name	Function
NIC-6	B	Tag BCC error	This interface status bit is used to indicate an address check code error when set in conjunction with the MDD error bit (NIC-7). The address check code error results when the 16-bit address check word read from the disk after the address tag word does not match the address check word generated when the address tag word is read from the disk.
NIC-6	C	End of page	This interface status bit indicates that the transfer of a data page between the SBU memory and disk unit (in either direction) has been completed and the interface is ready to process the next data page.
NIC-6	D ↓ F	SBU $\overline{\text{bank count}}$ 2^2 through 2^0	These three status bits give the not code of one of the eight SBU memory banks that was being accessed during a data transfer when a read error bit (NIC-6) was set. The memory bank with the error is found by complementing the bank count status code and counting back four memory banks.
NIC-7	0 ↓ 8	Unit 0 through 8 on sector or seek error	Each of these status bits from the MDD units indicates that the unit has completed the seek for the addressed sector (on sector) or is unable to complete the seek for the addressed sector (seek error). The on-sector signal is one sector in length, occurs immediately preceding the addressed sector, and is gated by the on-cylinder bit(NIC-7). The 1 pulse for an on sector occurs once per revolution of the disk pack until cleared.
NIC-7	9	Busy	This status bit from the MDD units indicates that the unit selected by unit select and logic number bits (NOC-5) is reserved by the other MDD interface.

TABLE 2-25. NIC-6 AND -7 BIT DESCRIPTIONS FOR MDD INTERFACE (Cont'd)

Channel	Bit	Name	Function
NIC-7	A	Ready	This status bit from the MDD units indicates that the unit selected by unit select and logic number bits (NOC-5) meets all conditions to transmit data.
NIC-7	B	Seek error	This status bit from the MDD units indicates that the selected unit was unable to complete a seek operation of the addressed sector in 600 milliseconds.
NIC-7	C	On cylinder	This status bit from the MDD units indicates that the selected unit has positioned the read/write heads at the addressed cylinder.
NIC-7	D	Pack unsafe	This status bit from the MDD units indicates that the selected unit has one or more fault conditions that inhibit write and erase currents to the heads.
NIC-7	E	MDD error	This status bit from the interface indicates a transfer error. The transfer error is the result of read error (NIC-6), address check code error (refer to tag BCC error, NIC-6), or address tag compare error. The address tag compare error results when the address tag word read from SBU memory does not match the address tag word read from the disk.
NIC-7	F	$\overline{\text{Finished}}$	This status bit from the interface indicates a not finished condition of the data transfer when set.

TABLE 2-26. NOC-5 AND -6 BIT DESCRIPTIONS FOR MDD INTERFACE

Channel	Bit	Name	Function
NOC-5	0	Release †	This bit is sent to all MDD units to release the selected unit by clearing the reserve status of the unit.
		or	
		Write tags † †	This bit enables the main timing in the interface to write address tags on the disk. The address words include head gap, sync pattern, address tag word, and address check code. The write bit (NOC-5) must also be set for a write tags operation.
NOC-5	1	Sector select †	This bit is sent to all MDD units and indicates that the address and control bits 0 through 7 (NOC-5) contain the address of the sector which generates the next on-sector signal. Only sectors 0 and 7 are selected in order to divide the disk in half for full-page data recording.
		or	
		Full † †	This bit is sent to the interface address register along with page and header address bits (NOC-5). It enables a full status in the interface. The full status clears in the interface when the page address is sent to the SBU memory.
NOC-5	2	Difference select †	This bit is sent to all MDD units and indicates that the address and control bits 0 through 7 (NOC-5) contain positioning information (difference between unit's present cylinder address and new interface address) for the selected unit.
		or	
		Proceed † †	This bit is sent to the interface address register along with page and header address bits (NOC-5). It is used in conjunction with the begin transfer bit (NOC-6) to initiate a read or write operation in the interface.

See footnotes at end of table.

TABLE 2-26. NOC-5 AND -6 BIT DESCRIPTIONS FOR MDD INTERFACE (Cont'd)

Channel	Bit	Name	Function
NOC-5	3	Clear †	This bit is sent to all MDD units and unreserves any unit previously selected by the interface regardless of present status.
		or	
		Odd † †	This bit is used to select odd data pages (1, 3, 5, etc.) when set or even data pages (0, 2, 4, etc.) when clear. This function is applicable only during half banks mode (ODD/EVEN/OFF banks switch, on interface main timing module, set to either ODD or EVEN). NOTE The switch selects odd or even banks while the odd bit selects odd or even data pages.
NOC-5	4	Logic number 2^2 †	This bit in conjunction with logic number 2^1 and 2^0 bits (NOC-5) provide a unit select code. They are sent to all MDD units along with unit select bit (NOC-5) to select a unit.
		or	
		Page address 2^{14} † †	This bit and page address 2^{13}, 2^{12}, and 2^{11} bits (NOC-5) are part of the starting address and specify 1 of 15 data page addresses in the SBU memory.
NOC-5	5	Logic number 2^1 †	Refer to logic number 2^2 (NOC-5).
		or	
		Page address 2^{13} † †	Refer to page address 2^{14} (NOC-5).
NOC-5	6	Logic number 2^0 †	Refer to logic number 2^2 (NOC-5).
		or	
		Page address 2^{12} † †	Refer to page address 2^{14} (NOC-5).

See footnotes at end of table.

TABLE 2-26. NOC-5 AND -6 BIT DESCRIPTIONS FOR MDD INTERFACE (Cont'd)

Channel	Bit	Name	Function
NOC-5	7	Unit select †	Refer to logic number 2^2 (NOC-5).
		or	
		Page address 2^{11} † †	Refer to page address 2^{14} (NOC-5).
NOC-5	8	Address and control bit 7 †	This bit along with address and control bits 6 through 0 (NOC-5) are sent to all MDD units. Information in the address and control bits is given in Table 2-24 and is determined by the accompanying sector select bit (NOC-5), control select bit (NOC-6), or difference select bit (NOC-5).
		or	
		Write † †	This set bit signals the interface to write an SBU memory data page onto the disk. A clear bit enables the interface to read a data page from the disk.
NOC-5	9	Address and control bit 6 †	Refer to address and control bit 7 (NOC-5).
NOC-5	A	Address and control bit 5 †	Refer to address and control bit 7 (NOC-5).
		or	
		Header address 2^{10} † †	This bit and header address bits 2^9 through 2^5 specify the address in page 0 of the header information that accompanies a data page.
NOC-5	B ↓ F	Address and control bits 4 through 0 †	Refer to address and control bit 7 (NOC-5).
		or	
		Header addresses 2^9 through 2^5 † †	Refer to header address 2^{10} (NOC-5).
NOC-6	0 ↓ 7	Not used	
NOC-6	8	Begin transfer	This bit, along with the proceed bit (NOC-5), initiates a read or write operation in the interface.

See footnotes at end of table.

TABLE 2-26. NOC-5 AND -6 BIT DESCRIPTIONS FOR MDD INTERFACE (Cont'd)

Channel	Bit	Name	Function
NOC-6	9	Clear end page	This bit is used to set a not end page status in the interface at the beginning of a read or write operation. After the read or write of a data page is completed, an end of page status bit (NIC-6) results.
NOC-6	A	Load address	This bit is used to gate the page and header address bits (NOC-5), write tags bit (NOC-5), full bit (NOC-5), proceed bit (NOC-5), odd bit (NOC-5), and write bit (NOC-5) into the interface.
NOC-6	B	Control select	This bit is sent to all MDD units and indicates that the address and control bits 0 through 7 (NOC-5) contains control information.
NOC-6	C	Function	This bit is used to gate the address and control bits 0 through 7 (NOC-5), release bit (NOC-5), sector select bit (NOC-5), difference select bit (NOC-5), clear bit (NOC-5), logic number bits (NOC-5), and unit select bit (NOC-7) through the interface to the units.
NOC-6	D ↓ F	Connect code 2^2 through 2^0	These bits connect either MDD-A or MDD-B interface to the SCU (refer to Table 2-1 for MDD interface connect codes).

†This bit is set, provided the function bit (NOC-6) is set.

††This bit is set, provided the load SBU address bit (NOC-6) is set.

ADDRESS AND CONTROL BUS

The address and control bus in the interface consists of eight lines which transmit normal channel information to the selected MDD unit. Information on these lines is determined by an accompanying normal channel tag line signal. Table 2-27 gives the relationship of the address and control bus and the tag line signals.

TABLE 2-27. ADDRESS AND CONTROL BUS FUNCTIONS

Address/ Control Bus	Tag Line			
	Difference Select	Sector Select	Control Select	
Bit 0 (NOC-5, bit F	1	1	Write gate –	A 1 input on this line enables the write drivers.
Bit 1 (NOC-5, bit E)	2	2	Read gate –	A 1 input on this line enables the digital read data lines.
Bit 2 (NOC-5, bit D)	4	4	Seek forward –	A 1 input on this line initiates forward carriage movement.
Bit 3 (NOC-5, bit C)	8	8	Not used	
Bit 4 (NOC-5, bit B)	16	Not used	Erase gate –	A 1 input on this line enables the erase driver to pass current through the head erase coil.
Bit 5 (NOC-5, bit A)	32	Not used	Seek reverse –	A 1 input on this line initiates reverse carriage movement.
Bit 6 (NOC-5, bit 9)	64	Not used	Return to zero –	A 1 input on this line initiates carriage movement to cylinder 00.
Bit 7 (NOC-5, bit 8)	128	Not used	Not used	

NETWORK TRUNK INTERFACE

The communications network trunk interface (NTI) is an SBU interface unlike all other SBU interfaces in that it is controlled by a remote terminal via modems (modulator/demodulator) rather than by the BC in the SCU. Figure 2-37 illustrates the relationship of the NTI to the SBU and remote terminal.

The NTI may transmit or receive up to 5 megabits per second to or from a modem, transceiver, or data set, depending upon the timing of the type of device used with the communications line. At the NTI/modem interface, data is in serial format and 16-bit parallel format at the SBU memory interface. The mode of operation in the NTI is governed completely by control information received from the remote terminal. There are no normal channel connections from the NTI to the SCU. This being the case, the information contained in the remaining paragraphs of this interface description explains some general communications procedures used and message sequences between the NTI and a remote terminal.

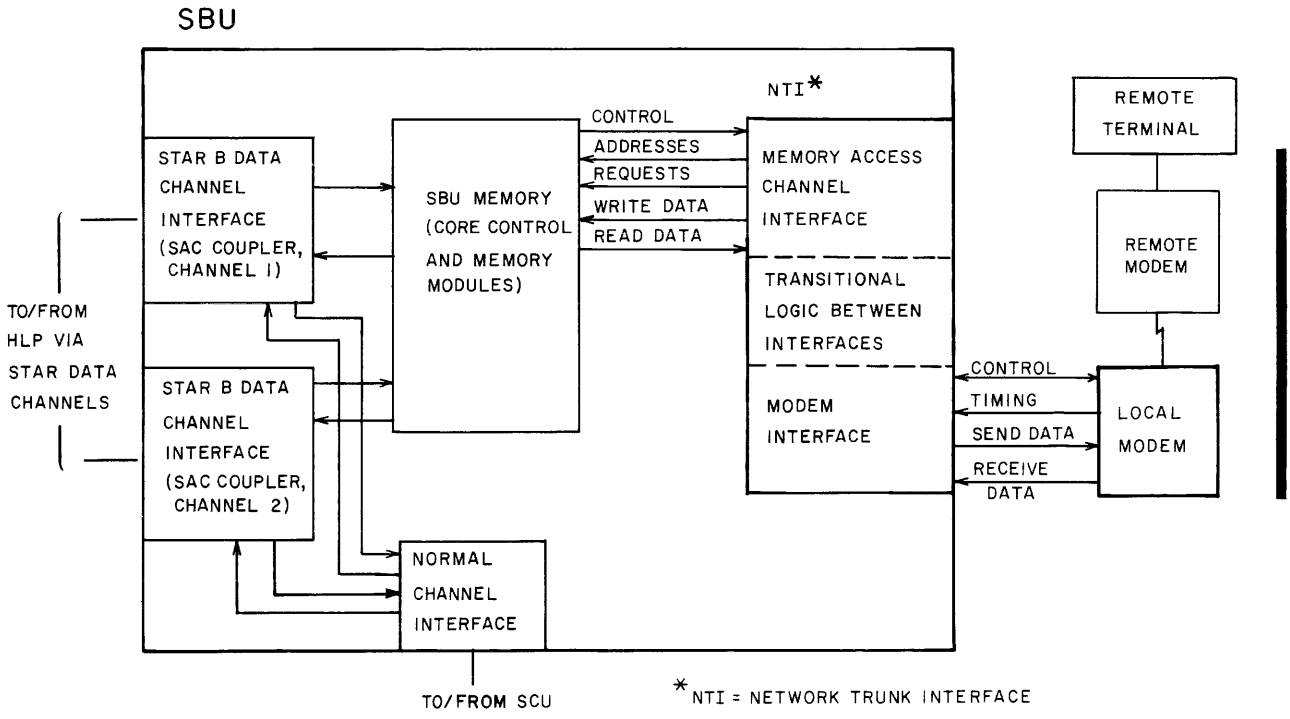


Figure 2-37. Network Trunk Interface System Relationship

ADCCP MESSAGE FORMATS

Message format conforms to USA Standard for Advanced Data Communication Control Procedures (ADCCP) with several exceptions. Serial data transmission from the modem starts with highest order bit first. The all parties address (00_{16}) is not implemented. On a party line, a terminal desiring to transmit a message after another terminal has been communicating with the NTI must wait between 50 and 300 microseconds after the carrier signal drops before initiating a request to send procedure. This delay allows the NTI time to generate the appropriate response.

All transmissions are in messages which conform to one of the formats shown in Figure 2-38.

FLAG	ADDRESS	CONTROL FIELD	INFO (DATA) FIELD	CRC†	FLAG

View A: Standard frame format

FLAG	ADDRESS	CONTROL FIELD	CRC†	FLAG

View B: Short frame format (used only when there is no information or data field)

†$\overline{\text{CRC}}$ = cyclic redundancy check

Figure 2-38. Message Frame Formats

Explanations of the various blocks of the message frame formats are as follows:

FLAG FIELD

All transfers start and end with a flag sequence. The flag sequence is one 0-bit, six 1-bits, and a 0-bit (0 11 11 11 0) and is used for synchronization purposes. All stations attached to the system data link continuously search for this sequence. The flag sequence is prohibited from occurring in all but the first and last fields of a frame so that transparent operation can be achieved and maintained in all other fields. Transparent operation simply means that information is transmitted exactly as it was received (even if in error). To achieve transparency within a block between starting and ending flags, the transmitting equipment inserts a 0-bit after five 1-bits and the receiving equipment deletes the 0-bit. If seven 1-bits are received, the receiving equipment interprets the condition as an abort and clears itself.

ADDRESS FIELD

Each terminal is assigned a unique address. The address field is eight bits and may contain the addresses of 0 to 255 terminals.

CONTROL FIELD

This is an 8-bit field used for functions, responses, and sequence numbers. The upper four bits contain either the function or response code. The lower four bits contain the sequence number. Function codes and response codes are defined in later paragraphs of this section. Sequence numbers are used to number transfers for each unique terminal address and to ensure that a transfer is not overlooked or duplicated. The NTI and the remote terminal must maintain the same sequence numbers. Each terminal generates a sequence number. In the NTI, logic circuits increment the sequence number after each message and store the number in SBU memory. Function and response bits are also stored in SBU memory. The upper eight bits of the memory location contain the terminal address.

INFORMATION (DATA) FIELD

This field is used only when data is to be transmitted. It is used for transmitting a bit stream of transparent data in which no specific character length is implied.

CRC FIELD

The cyclic redundancy check (CRC) field contains a 16-bit character used for data checking. Subsequent paragraphs in this section describe the CRC generator as it is used in the NTI.

NTI MESSAGE SEQUENCES

There are three types of message sequences used with the NTI excluding error conditions: read, write, and reset.

READ SEQUENCE

A read sequence means that the NTI must extract data from a specified location in SBU memory. The procedure is initiated by the remote terminal issuing a four-bit function code of 0101_2 (within the read request message sequence) to the NTI. After processing the read request, the NTI responds to the remote terminal with the read data message.

The order of events in a read request message sequence are given in Table 2-28 and occur as listed. When the read function and sequence number in the read message sequence has been received, the NTI then receives the SBU address information. At the end of the address field, both an even parity word and a CRC word are received from the remote terminal and are used to check all information received except the synchronizing flags. After the CRC character, a final flag character is received to indicate the end of the transmission.

After the NTI processes the read request, it begins transmitting synchronizing flags, and the remote terminal sends the read data message response which follows the sequence listed in Table 2-29.

TABLE 2-28. REMOTE TERMINAL READ REQUEST MESSAGE SEQUENCE

No. of Bits	Name	Definition or Function
8	Flag	Synchronizing character
8	Terminal address	Address of the remote terminal to receive the frame
4	Function	Read
4	Sequence number	A count of the number of transfers (messages) the NTI has processed for the given terminal address. This count in the incoming message is compared to the count in SBU memory. If they are not equal, a sequence error is recorded.
16	SBU starting address	Any address in SBU memory from which data is extracted
16	Complement of SBU starting address	Ones complement of the SBU starting address
16	Complement of SBU terminating address	Ones complement of the SBU terminating address
16	Even parity check	Checkword generated on the previous 64 bits by the remote terminal and checked in the NTI
16	CRC	Cyclic redundancy check generated by the remote terminal and checked in the NTI
8	Flag	Synchronizing character used to terminate the message

TABLE 2-29. READ DATA MESSAGE RESPONSE SEQUENCE

No. of Bits	Name	Definition or Function
8	Flag	Synchronizing character
8	Terminal address	Address of the remote terminal to receive the frame
4	Response	Answer the NTI sends to the remote terminal requesting data; it can be either an accept with data to follow or a reject
4	Sequence number	A count of the number of transfers (messages) the NTI has processed
16(n)	Data field	Data read from SBU memory and transmitted to remote terminal in 16-bit multiples, two words minimum and up to 2048 words, maximum
16	CRC	Cyclic redundancy checkword generated by the NTI and checked by the remote terminal
8	Flag	Synchronizing character used to terminate the message

WRITE SEQUENCE

A write sequence operation is initiated when a four-bit function code of 1101_2 is sent by the remote terminal to the NTI. The code is transferred to the NTI via the write request message sequence (Table 2-30). After processing the write request, the NTI responds to the remote terminal with the appropriate response sequence (Table 2-31).

After the NTI decodes the write function and sequence number, it receives SBU address location information and performs an even parity check on all information except the synchronizing flags. The data field follows the parity word and can be any size (in increments of 16-bit words) up to one page (2048 words). The 16-bit CRC character checks all information received from the remote terminal. The NTI then sends an accept to the remote terminal, provided no errors were detected in the data received. The accept (or control information) is followed by a 16-bit CRC character for all information transmitted (except synchronizing flags) plus a synchronizing flag to end the transmission.

For each write message received from the remote terminal, the NTI must send an appropriate response as to the status of the message. Table 2-31 lists the steps in order for a response sequence.

RESET SEQUENCE

If the remote terminal receives a sequence error or a reject from the NTI in response to a message, it issues the reset function (0110_2) to the NTI. Table 2-32 lists the steps in order for a reset message sequence.

After the NTI receives and decodes the reset function and sequence number, it receives SBU address information. The sequence number and address information are ignored and are only transmitted to comply with procedural requirements. At the end of the received information, the NTI performs an even parity check and a CRC character check. The flag is received to indicate the end of transmission. The NTI then transmits the accept response for the reset function, clears the sequence number, and sends a CRC character and a synchronizing flag to the remote terminal to end the transmission. Format of the acknowledgement message sent to the remote terminal in response to the reset function is listed in Table 2-33.

TABLE 2-30. REMOTE TERMINAL WRITE REQUEST MESSAGE SEQUENCE

No. of Bits	Name	Definition or Function
8	Flag	Synchronizing character
8	Terminal address	Address of the remote terminal sending the frame.
4	Function	Write
4	Sequence number	A count of the number of transfers (messages) the NTI has processed for the given terminal address. This count in the incoming message is compared to the count in SBU memory. If they are not equal, a sequence error is recorded.
16	SBU starting address	Any address in SBU memory where the data field is written.
16	Complement of SBU starting address	Ones complement of the SBU starting address.
16	Complement of SBU terminating address	Ones complement of the SBU terminating address.
16	Even-parity check	Checkword generated on the previous 64 bits by the remote terminal and checked in the NTI.
16	Data field	Multiples of 16-bit words up to 2048 words in length from the remote terminal.
16	CRC	Cyclic redundancy checkword generated by the remote terminal and checked by the NTI.
8	Flag	Synchronizing character used to terminate the message.

TABLE 2-31. NTI RESPONSE SEQUENCE TO WRITE REQUEST MESSAGE

No. of Bits	Name	Definition or Function
8	Flag	Synchronizing character
8	Terminal address	Address of the remote terminal receiving the acknowledgement
4	Response	Answer the NTI sends to the remote terminal sending the data; it can be either an accept or reject.
4	Sequence number	A count of the number of transfers (messages) the NTI has processed.
16	CRC	Cyclic redundancy checkword generated by the NTI and checked by the remote terminal
8	Flag	Synchronizing character used to terminate the message

TABLE 2-32. REMOTE TERMINAL RESET MESSAGE SEQUENCE

No. of Bits	Name	Definition or Function
8	Flag	Synchronizing character
8	Terminal address	Address of the remote terminal sending the frame
4	Function	Reset
4	Sequence number	A count of the number of transfers (messages) the NTI has processed for the given terminal address. This count in the incoming message is compared to the count in SBU memory. If they are not equal, a sequence error is recorded.
16	SBU starting address	Any address in SBU memory
16	Complemented SBU starting address	Ones complement of the SBU starting address
16	Complemented SBU terminating address	Ones complement of the SBU terminating address
16	Even parity check	Check performed on the previous 64 bits
16	CRC	Cyclic redundancy check generated by the remote terminal and checked in the NTI.
8	Flag	Synchronizing character used to terminate the message.

TABLE 2-33. NTI RESET ACKNOWLEDGE MESSAGE SEQUENCE

No. of Bits	Name	Definition or Function
8	Flag	Synchronizing character
8	Terminal address	Address of remote terminal to receive the frame
4	Response	Answer that the NTI sends to the connected terminal; it may be either an accept or a reject.
4	Sequence number	Reset to zero
16	CRC	Cyclic redundancy check generated by the NTI and checked by the remote terminal
8	Flag	Synchronizing character used to terminate the message

NTI RESPONSES

In response to a function, the NTI can respond with an accept code, an accept code with a data field to follow, or a reject code if an error was detected.

ACCEPT CODE (0001_2)

This response, when transmitted to the remote terminal, indicates that no error conditions were detected during the previous transmission from the remote terminal to the NTI.

ACCEPT WITH DATA FIELD CODE (1001_2)

This response is transmitted to the remote terminal during a read sequence. After the NTI receives the appropriate control information, it transmits this accept response followed by the transmission of serial data.

REJECT CODE (0011_2)

This response, when transmitted to the remote terminal, indicates that an error condition was detected during the previous transmissions from the remote terminal to the NTI. The seven error conditions which cause a reject are:

Illegal function

Memory parity error on read previous sequence

Sequence compare error

Starting address and complement starting address error

Header parity error

Page boundary reached on write function

Cyclic redundancy error

ERROR CONDITIONS

Although there are many possible error conditions that can cause the NTI to send a reject code or to terminate a transmission, 12 representative error conditions are listed and explained in Table 2-34. Since no status is available, detection of an error is confirmed only by a reject or no response at the terminal. No attempt is made by the hardware to differentiate between the types of errors.

TABLE 2-34. NTI ERROR CONDITIONS

Type of Error	Meaning	Response to Terminal
Illegal function	A function other than read, write, or reset was decoded from the four function bits.	Reject
Memory parity error on read previous sequence	A parity error was detected while reading the sequence number from memory for that terminal.	Reject
Sequence compare error	A lost message is indicated because the sequence number of the message and the sequence number in SBU core were not equal.	Reject
Starting address and complement starting address error	After the starting address is loaded into the SBU starting address register, it is returned to the NTI in ones complement form (return address). This complemented starting address is compared with the return address from the SBU. If they are not equal, an error has occurred.	Reject
Header parity error	This error occurs during an even parity check on the 64 serial data bits following the flag.	Reject
Page boundary reached on write function	This error occurs when a page boundary is reached before the current address equals the terminating address.	Reject
Cyclic redundancy error	This type of error occurs if data or a read or reset command is transferred incorrectly.	Reject
Carrier drop during address sequence	The address sequence contains the terminal and the SBU addresses both of which reside in the 64 bits following the synchronizing flag. If the carrier from the modem drops during this sequence, an error occurs.	No response, and NTI terminates operation
Insufficient data on write function	If the data stream stops or a flag is sensed before the current SBU address equals the terminating SBU address, an error occurs.	No response
Seven ones detected during an input operation	This error is caused by a malfunction at the transmitting terminal since seven 1's are never to be sent as data. The NTI clears its synchronized condition and timing chain.	No response

TABLE 2-34. NTI ERROR CONDITIONS (Cont'd)

Type of Error	Meaning	Response to Terminal
Memory parity error during read function	If an SBU memory parity error is detected while the NTI is transmitting data to a terminal, transmission is stopped immediately.	No response, and NTI terminates transmission
Page boundary reached on read function	Data field is limited to one page. If the read data field crosses a page boundary, transmission terminates with a CRC as if the terminating address was reached.	No response, and NTI terminates transmission

CYCLIC REDUNDANCY CHECK

Data checking procedures are based upon the transmission of redundant information with each transmission to enable the receiving party to detect errors. The CRC accumulation starts with the first bit following the flag sequence. All bits except the inserted 0-bit following the five one-bits are included in the accumulation. After the last information bit is received, the contents of the shift register represents the coefficient of the remainder polynomial. The checkword can be shifted out serially and appended to the data field. When data is received, data and the checkword are processed through the CRC generator. If the data is correct, the remainder is zero.

34 general purpose recording tracks, 1152† words/track		= 39,168
1 CRT refresher track, 648 words/track		= 648
1 autoload program track, 1152 words/track		= 1,152
36 addressable tracks	Total 16-bit words	40,968
2 spare tracks		
2 control tracks		
40 total tracks per microdrum		

Generally, the four principal functions of the microdrum are as follows:

- Provides auxiliary storage for the BC (34 tracks available).
- Provides an autoload track reserved for permanent storage of a program that can be automatically transferred to BC memory.
- Provides for the storage of diagnostic programs.
- Provides a CRT refresher track to enable a continuous display of data on the CRT.

The average access time is 8.4 milliseconds and the maximum access time is 16.7 milliseconds. The transfer rate is 1 megabit per second.

MICRODRUM/BC SIGNALS

The following signals or data bits are exchanged between the normal input and output channels of the BC, the drum and display logic, the microdrum, and the CRT display. Refer to Figure 3-2.

OUTPUT DATA

Sixteen bits of data are sent by the BC over NOC-0 to the drum and display logic and ultimately to the microdrum.

† Based on 18 sectors/track; 64 16-bit words/sector = 1152 words/track.

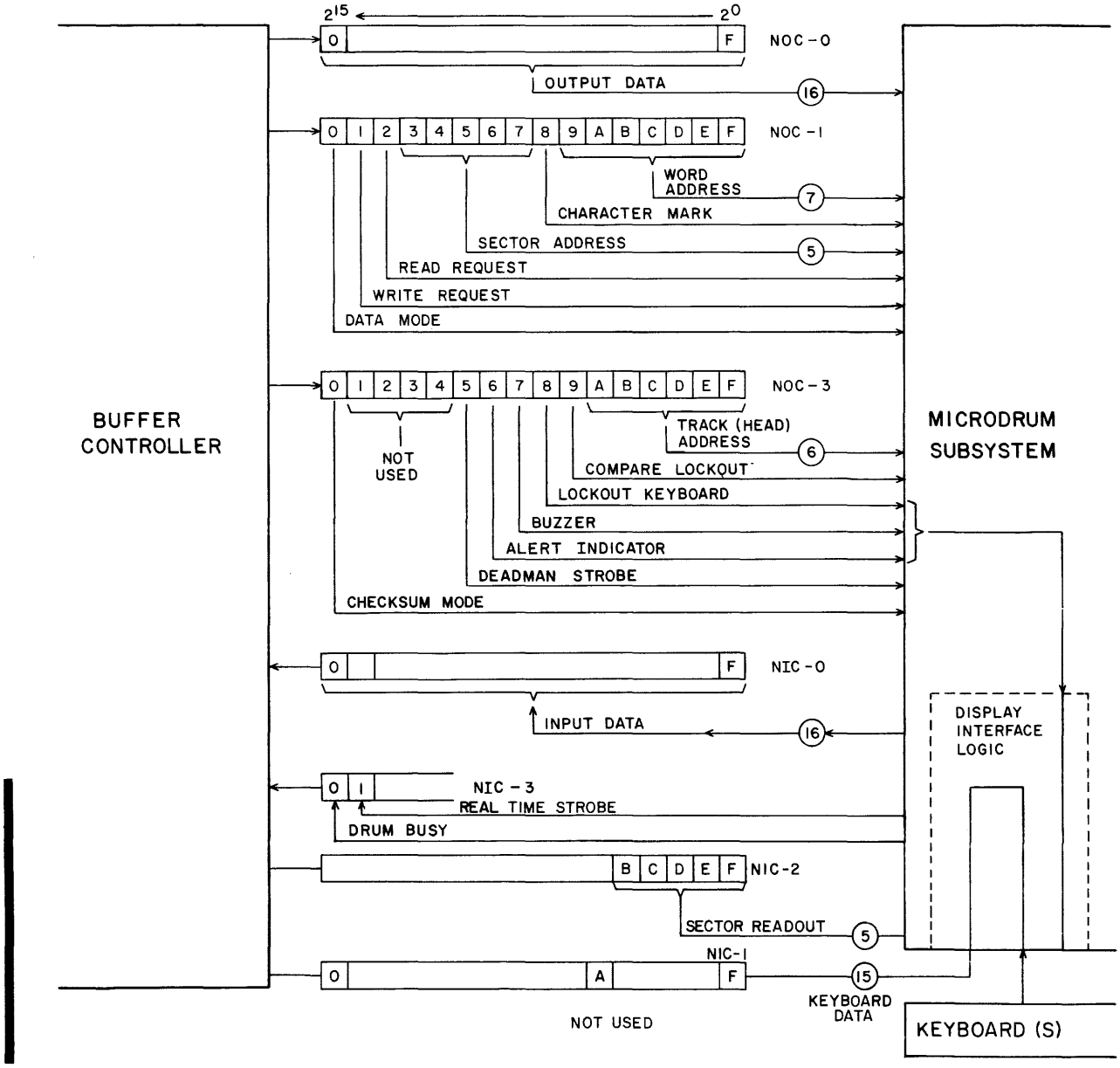


Figure 3-2. Word Formats Between the BC and Microdrum Subsystem and Keyboard(s)

COMPARE LOCKOUT

This signal (NOC-3, bit 9) disables the drum address compare circuits allowing continuous reading or writing on the microdrum. The BC must assume complete control during this mode of operation.

TRACK (HEAD) ADDRESS

These six bits (NOC-3, bits A through F) are sent by the BC to select any one of 36 tracks on the microdrum.

INPUT DATA

Sixteen bits of data are collected from the microdrum via NIC-0.

DRUM BUSY

This pulse, sent to the BC via NIC-3, bit 0, indicates that the microdrum is preparing to perform an operation such as read, write, or autoload; it, therefore, cannot accept additional commands until the current operation is completed. While this pulse is active, there must be no changes on any line from the BC to the drum and display logic. The drum busy pulse becomes active each time a new operation is begun.

REAL TIME STROBE

This bit (NIC-3, bit 1) switches states approximately every 8 milliseconds and can be used as a time clock for station software. It is bit 2^2 of the sector counter; therefore, each clock time equates to four sector times.

SECTOR READOUT

These five lines (NIC-2, bits B-F) indicate to the BC which sector is presently under the microdrum heads.

MICRODRUM OPERATIONS

The following operations can be performed under control of the BC.

WRITE

Records data from the BC into a specified sector or word location on the microdrum. The sector or word location is specified by an address sent from the BC at the beginning of the write operation.

A write lockout feature can be used to inhibit writing on 24 (00_8 through 27_8) of the 36 tracks, if desired. The procedure is initiated by the operator pressing the WRITE LOCKOUT switch on the SCU control panel.

The write operation can be performed in either the data or display mode. In the data mode, bits of information are packed (no spaces between words) on the microdrum and a full sector (64 16-bit words) is the smallest practical unit of data that is recorded.

In the display mode two spaces equal to six characters each form a parenthesis around each word. Therefore, a single 16-bit word can be stored within a sector without disturbing the remainder of the sector. The CRT refresher track is the only track that uses the display mode in a write operation.

Data cannot be recorded on the autoload track from the BC in the normal manner. A special procedure is used to write into this track from the paper tape reader on the portable maintenance console.

During a write operation, data is sent to the microdrum from the A register in the BC. A separate output-from-A instruction is executed to transfer each 16-bit word.

READ

This operation is the transfer of data from any sector or word on the microdrum to BC. In either the data or display mode, a read operation can be specified to begin at any word position within a sector.

During a read operation, input data flows to the A register in the BC. A separate input-to-A instruction is executed for each 16-bit word transferred.

In either a read or write operation, the BC must supply a starting address at the beginning of the operation. Words are then read or written from sequential locations beginning with the starting address supplied by the BC.

AUTOLOAD

The microdrum subsystem provides two methods for autoloading its host station; local or remote. In the local autoload mode, data is read from track 0 on the microdrum and loaded into the first 1152 locations (0000 through 480_{16}) of BC memory. In remote

DISPLAY SETUP

1. Select display track (NOC-3, bits A through F).
2. Reset current head selected. If desired head is same as current head selected, proceed to Establishing Starting Sector and Word Address for Data Transfer.
3. Transfer sector address (NOC-1, bits 3 through 7), word address (NOC-1, bits 9 through F, and character mark (NOC-1, bit 8) to microdrum.
4. Exit to program that originated display request.

ENTRY KEYBOARD

The keyboard used in the SCU is illustrated in Figure 3-4, and generates character codes for the 64 characters in columns 2, 3, 4, and 5 (refer to Table 3-1) of the ASCII character coding set. Figure 3-4 also lists the normal channels used for the transfer of each bit.

The keyboard also generates function codes for the function keys listed in Table 3-2. Either character or function codes are transferred to the BC via NIC-1, bits 1 through 7. Codes for characters sent to the BC are accompanied by the data strobe signal (NIC-1, bit B).

KEYBOARD CONTROL KEYS

Each of the keyboard control keys places an octal code on the character/function lines when pressed, and each key is used for a specific purpose in program control. Table 3-2 lists each key, its hexadecimal equivalent, and an application pertaining to program control.

KEYBOARD INTERFACE SIGNALS (TO NIC) (Refer to Figure 3-4)

CHARACTER FUNCTION/CODES

These seven lines (bits 1 through 7) are used to carry the function codes or character codes from the keyboard to normal input channel 1.

ALARM DISABLE (ALERT)

This signal is transmitted when the ALERT pushbutton switch is pressed.

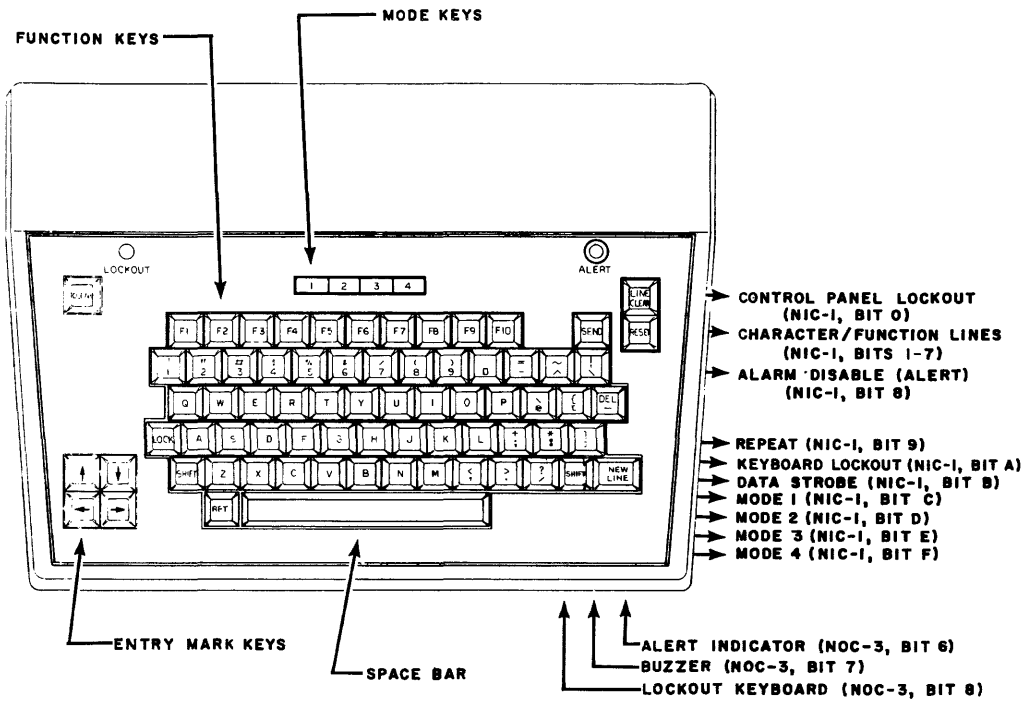


Figure 3-4. SCU Keyboard and I/O Signals

TABLE 3-1. ASCII CODING SET FOR KEYBOARD

b7 →						0	0	0	0	1	1	1	1
b6 →						0	0	1	1	0	0	1	1
b5 →						0	1	0	1	0	1	0	1
Bits	b4	b3	b2	b1	Column	0	1	2	3	4	5	6	7
	0	0	0	0	0	NUL	DLE	SP	0	@	P		p
	0	0	0	1	1	SOH	DC1	!	1	A	Q	a	q
	0	0	1	0	2	STX	DC2	"	2	B	R	b	r
	0	0	1	1	3	ETX	DC3	#	3	C	S	c	s
	0	1	0	0	4	EOT	DC4	$	4	D	T	d	t
	0	1	0	1	5	ENQ	NAK	%	5	E	U	e	u
	0	1	1	0	6	ACK	SYN	&	6	F	V	f	v
	0	1	1	1	7	BEL	ETB	'	7	G	W	g	w
	1	0	0	0	8	BS	CAN	(	8	H	X	h	x
	1	0	0	1	9	HT	EM	)	9	I	Y	i	y
	1	0	1	0	10	LF	SUB	*	:	J	Z	j	z
	1	0	1	1	11	VT	ESC	+	;	K	[	k	{
	1	1	0	0	12	FF	FS	,	<	L	/	l	¦
	1	1	0	1	13	CR	CS	-	=	M	]	m	}
	1	1	1	0	14	SO	RS	.	>	N	^	n	~
	1	1	1	1	15	SI	US	/	?	O	—	o	DEL

Not Used — Not Used

TABLE 3-2. KEYBOARD CONTROL KEY FUNCTION CODES

Function	Hex Code	Software Application
CLEAR	00	Clears display and places entry marker in first character position of line without affecting displayed area.
LINE CLEAR	03	Clears an entry line and places entry marker in first character position of line without affecting displayed area.
INTER (Interrupt)	02	Signals BC to read active lines on display and to remove active marks.
NEW LINE	0A	Signals the software that the keyboard entry is complete.
RESET	1C	Places entry marker in first character position of data field without affecting display data.
Entry mark keys		
↑	08	No response
→	0B	These keys position the cursor one character left or right without affecting the displayed area.
←	11	
↓	12	No response
Function keys		
F1	71	Functions unassigned; however, functions such as insert, delete, etc., can be used.
F2	72	
F3	73	
F4	74	
F5	75	
F6	76	
F7	77	
F8	78	
F9	79	
F0	70	
Mode switches 1 2 3 4		Functions unassigned; however, modes such as off-line, on-line, etc., could be assigned.

In SCU-only stations (such as the unit record station), the B coupler provides a bi-directional data path to an HLP as shown in Figure 3-6. This arrangement allows the SCU to read or write memory in the HLP.

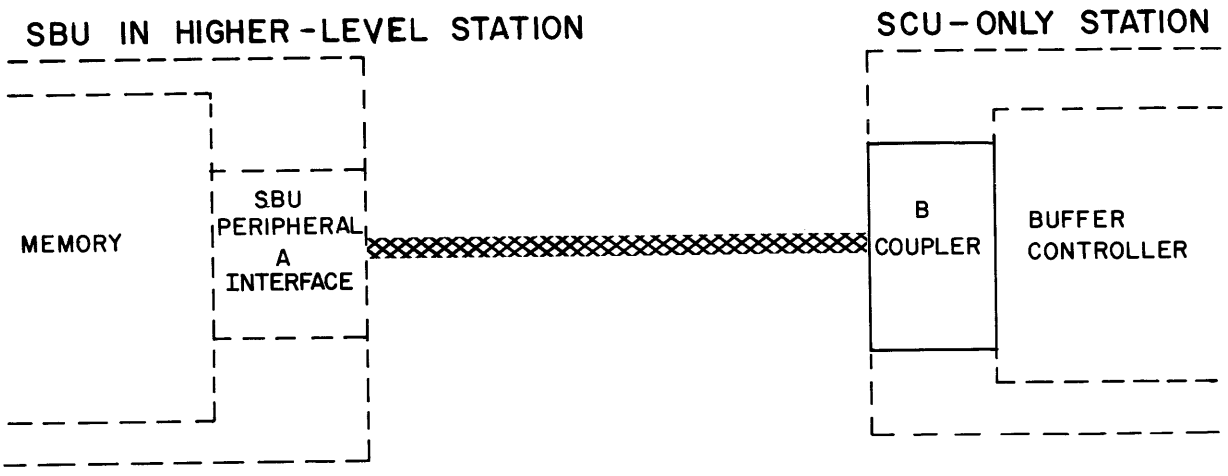


Figure 3-6. B Coupler Used in SCU-Only Station

In SCU/SBU stations (examples: paging station, disk station) the B coupler provides a path to the SBU that allows the SCU to write into or read from SBU memory. Figure 3-7 shows this arrangement.

One or more B couplers are present in all SCUs. Up to four B couplers can be installed in a SCU, however, only one can transfer data at a given time. A select code, issued on the normal channels, allows the BC, in the SCU, to select one of the couplers.

In SCU-only stations a secondary function of the B coupler is to allow autoloading of the SCU memory across the STAR data channel.

Operation of the B coupler is controlled by the BC via normal channel bits. The main control responsibilities of the SCU are:

- Issue a memory address to the A end of the channel. This address specifies the beginning of the area in A memory that the SCU wishes to read or write.
- Issue a function code which specifies the type of transfer operation (read or write).
- Initiate data transfer by executing a block transfer instruction.
- Monitor status conditions.

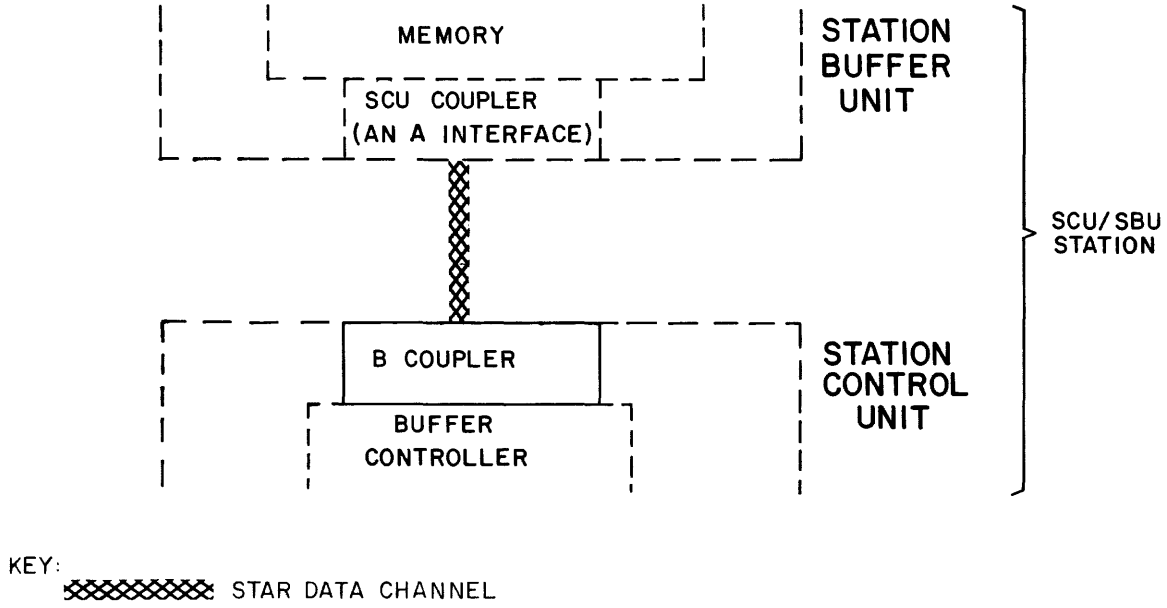


Figure 3-7. B Coupler Used in SCU/SBU Station

DATA TRANSFER OPERATIONS

The B coupler together with an A interface at the distant end of the channel, can perform the following data transfer operations.

• Write	Transfer a block of 32-bit data words (two 16-bit data words) from SCU memory to memory at the A end of the channel.
• Block read	Transfer a block of 32-bit words from A memory to the SCU memory.

- Special function† — Transfer one 32-bit word from a specified location in A memory to SCU memory, then store all zeros in this location in A memory.

All transfers on the STAR data channel must be multiples of 32-bit words. Each 32-bit word consists of two consecutive 16-bit words.

Data transfers on the STAR data channel must be initiated by the B end of the channel. To prepare the A end of the channel for a data transfer operation the BC sends the following information to A via the B coupler.

1. A function code that specifies the type of operation to be performed (write, block read, or destructive read).
2. A 21-bit starting address (sent as two 16-bit words) that specifies the beginning of the source or destination area in memory at the A end of the channel.

Then, the BC must execute an input-block transfer instruction or output-block transfer instruction to begin the data transfer.

For write and block read operations, the number of words transferred is determined by the word count of the block transfer instruction. The operation ends when the block transfer instruction terminates.

The sequence of programming steps required to initiate a data transfer are described later in this section.

FUNCTION CODES

Two types of function codes control activities on the STAR channel:

1. Operation function codes, sent from the B coupler to the A end of the channel.
2. System control functions, sent from A to the B coupler.

OPERATION FUNCTION CODES

The BC issues function codes (Table 3-3) to the B coupler via normal channel bits. The coupler forwards all function codes to the A end of the channel.

† Some A interfaces cannot perform this operation.

TABLE 3-3. B COUPLER OPERATION FUNCTION CODES

Name	Bits		
	D	E	F
Write	0	1	0
Block read	1	0	1
Read	0	0	1
Special function	0	1	1
Data	1	0	0
End of operation	1	1	1
Null	0	0	0
Illegal code	1	1	0

Write (010_2)

This code conditions the A end of the channel for transfer of a block of words from B to A.

Block read (101_2)

This code conditions the A end of the channel for transfer of a block of words from A to B.

Read (001_2)

This code is redundant. Its effect is identical in all respects to that of block read (101_2).

Special function (011_2)

This code causes the B end of the channel to perform a predetermined special function other than normal input/output. Not all A interfaces can perform this operation.

Data (100_2)

This code must be issued after a write (010_2) function code. It is transmitted along with the upper half of an output (write) data word.

End of operation (111_2)

This code should be issued at the end of a data transfer operation to inform the A end of the channel that the operation is complete (clears the A end of the channel).

Null (000_2)

This code does not specify an operation. It is transmitted along with the lower half of an address or output (write) data word to inform A that the lower part of a 32-bit word is on the channel. The B coupler automatically transmits this code. From a programming standpoint, it is transparent.

Illegal code (110_2)

This code should not be used. If issued, no operation results and the A end of the channel returns an illegal response bit that sets a status bit that can be sensed by the BC.

Some types of A interfaces also treat code 011_2 (destructive read) as an illegal code.

SYSTEM CONTROL CODES

The codes listed in Table 3-4 provide a means for the A end of the channel to send control information back to the B coupler.

TABLE 3-4. B COUPLER SYSTEM CONTROL CODES

Name	Code	
	Bit D	Bit E
Channel flag	0	1
External flag	1	0
Suspend	1	1
Invalid	0	0

NOTE

When the B coupler is used for the path between the SCU and SBU in SBU/SCU stations, these codes do not apply. The A interface in the SBU (the SCU coupler) cannot send system control codes.

Channel flag (01_2)

This code informs the B end of the channel that the system software has placed a message for B in a predetermined area in SBU memory at the A end of the channel. B normally responds to this code by initiating a block read operation to read in the message.

External flag (10_2)

This code directs B to master clear and then autoload from the microdrum.

Suspend (11_2)	This code causes B to terminate a write or block read operation.
Invalid (00_2)	The service station SCU should not transmit this code. It appears on the channel only as the result of a transmission fault. The B end of the channel should assume that a suspend code was intended. It should terminate the data transfer operation in progress and then send an interrupt to A to signal the malfunction.

In addition to setting individual status bits, all of the system function codes, except channel flag (01_2), also set the B coupler fault status bit. All of these status bits can be sensed by the BC on one of the normal input channels.

STARTING ADDRESS FORMAT

Before the start of a data transfer operation the SCU must issue a 21-bit starting address (Figure 3-8) by performing a two-word output-block transfer operation. The B coupler forwards the two address words to the A end of the channel. The starting address is the lowest address of the area in A memory read or written during the data transfer operation.

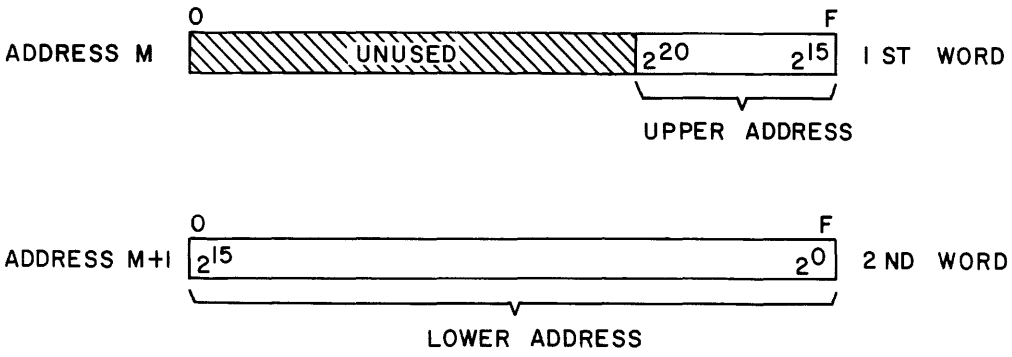


Figure 3-8. B Coupler Starting Address Word Formats

SCU CONTROL OF THE B COUPLER

Figure 3-9 shows the normal channel bits available to the BC for control of the B coupler. The bit assignments shown apply to all of the STAR stations.

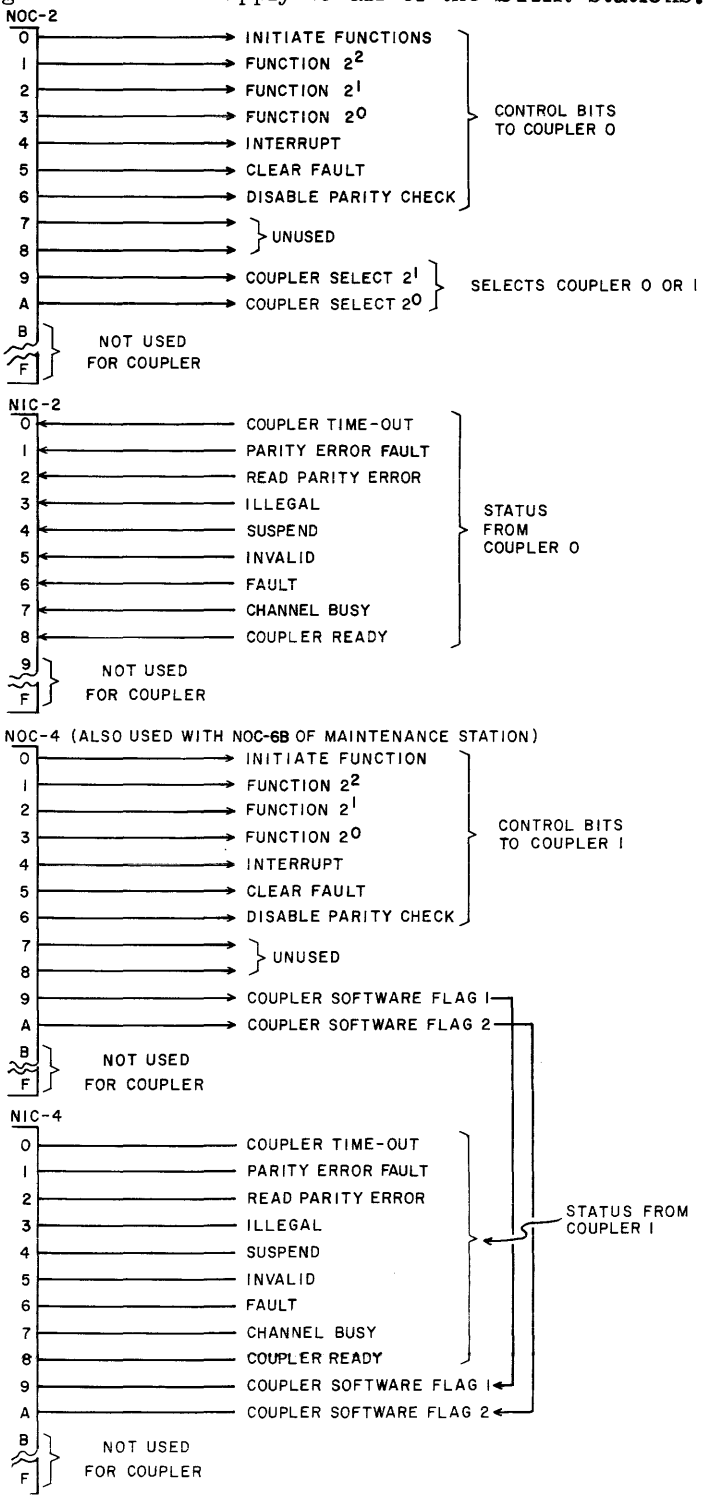


Figure 3-9. Coupler Normal Channel Bits

Table 3-5 lists and explains the functions of the normal channel bits used with the SCU B coupler.

TABLE 3-5. NORMAL CHANNEL BIT DESCRIPTIONS, SCU B COUPLER

Channel	Bit	Name	Function
NOC-2,-4	0	Initiate functions	When 1, this bit gates the function code (NOC-2,-4, bits 1, 2, and 3) into the B coupler. It must be used to issue all operation function codes, except the data code (100_2). It should be set at the beginning of a data transfer operation and cleared after the two starting address words are issued.
NOC-2,-4 NOC-2,-4 NOC-2,-4	1 2 3	Function bit 2^2 2^1 2^0	These bits are used to issue operation function codes.
NOC-2,-4	4	Interrupt	Setting this bit sends an interrupt signal to the A end of the channel. The bit may be cleared immediately after it is set.
NOC-2,-4	5	Clear fault	Setting and clearing this bit clears the following status bits. • Coupler time-out status • Parity error fault status • Read parity error status • Illegal status • Suspend status • Invalid status • Fault status

TABLE 3-5. NORMAL CHANNEL BIT DESCRIPTIONS, SCU B COUPLER (Cont'd)

Channel	Bit	Name	Function
NOC-2,-4	6	Disable parity check	When set, this bit disables the transmission parity check that the B coupler performs on data sent from A. It also prevents the fault bit from setting as a result of other parity errors detected.
NOC-2 NOC-2	9 A	Coupler select 2^1 Coupler select 2^0	These bits carry the coupler select code. Bit 9 | Bit A 0 | 0 — Selects B coupler 0 0 | 1 — Selects B coupler 1 1 | 0 — Unused 1 | 1 — Standard stations The select code must remain on the normal channels continuously to keep a coupler selected.
NOC-4 NOC-4	9 A	Coupler software flag 1 Coupler software flag 2	These two bits do not affect operation of the B coupler in any way. They are simply wired directly back to NIC-4, bits 9 and A. They are available for use by the software to record which coupler is selected.
NIC-2,-4	0	Coupler timeout status	When set, this bit indicates that the B coupler failed to transfer a starting address or data in response to an input or output block transfer instruction. This condition is the result of a hardware malfunction at either end of the STAR channel.
NIC-2,-4	1	Parity error fault status	When set, this bit indicates that the A end of the channel has detected: 1. A parity error in a function code sent by the B coupler, or 2. A parity error in data read from A memory during block read.

TABLE 3-5. NORMAL CHANNEL BIT DESCRIPTIONS, SCU B COUPLER (Cont'd)

Channel	Bit	Name	Function
NIC-2,-4	2	Read parity error status	When set, this bit indicates that a transmission fault has occurred on the STAR channel during a block read operation.
NIC-2,-4	3	Illegal status	When set, this bit indicates that the A end of the channel has: 1. Received an illegal control function code from the B coupler. 2. Detected a parity error in a control function code sent from the B coupler.
NIC-2,-4	4	Suspend status	When set, this bit indicates that the A end of the channel has sent a suspend control function code.
NIC-2,-4	5	Invalid status	When set, this bit indicates that an invalid code has appeared on the control function lines from A.
NIC-2,-4	6	Fault	When set, this bit indicates that one of the following conditions has occurred. • Coupler timeout • Transmission parity error during read • Control function parity error • A memory parity error during read • Illegal operation function code to A • Suspend control function code from A • External flag control function code from A
NIC-2,-4	7	Channel busy status	When set, this bit indicates that the B coupler is transferring a data or address word. The bit sets each time the B coupler requests a half-word from A. The bit clears each time transfer of a word is completed.

5. Recovery sequence

   a. Clear function select bits (NOC-2, bits 1, 2, and 3) and function initiate bit (NOC-2, bit 0).

   b. Place end-of-operation function code (111_2) on NOC-2, bits 1, 2,and 3.

   c. Set function initiate bit (NOC-2, bit 0).

   d. Set and clear fault bit (NOC-2, bit 5).

   e. Check coupler time-out status (NIC-2, bit 0).

      1) If time-out status = 1, a nonrecoverable hardware fault has occurred. Exit to calling program with an abort indication.

      2) If time-out status = 0, go to step 5f.

   f. Test status bits (NIC-2) for errors.

      1) If errors exist after third retry, exit to calling program with abort indication.

   g. Retry starting at step 1.

3000 SCU INTERFACE

The 3000 SCU interface connects CDC 3000 peripheral controllers to SCU normal channels. Figure 3-10 shows the relationship between the 3000 interface and other elements in the system.

The 3000 interface is limited to very basic data transfer operations. Each 12-bit data byte transferred to or from a 3000 controller requires a separate input-to-A or output-from-A instruction. Data is transferred through the interface without modification; no code conversion or assembly/disassembly takes place.

Control signals from the 3000 peripheral controllers are routed through the 3000 interface and terminate at normal channel bits. The BC controls peripheral devices by monitoring and manipulating these control signals. The 3000 interface performs only minor control functions; most of the control must be supplied by the driving software.

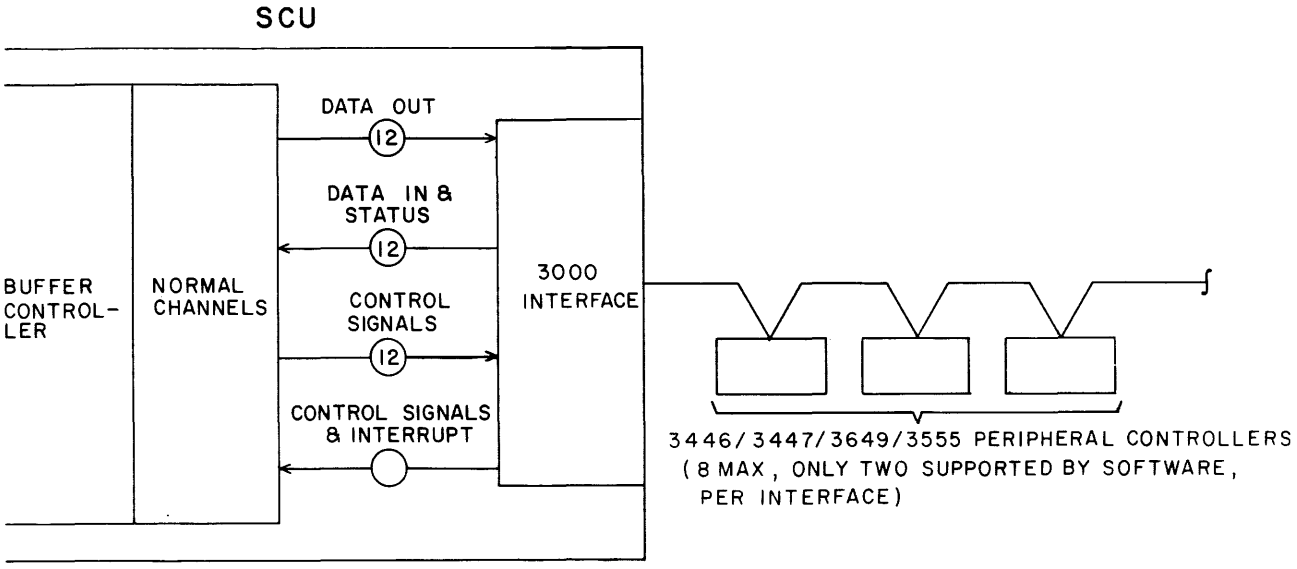


Figure 3-10. 3000 SCU Interface System Relationship

Two 3000 interfaces can be installed in the same SCU. The two interfaces are completely independent and are capable of transferring data concurrently, subject to software limitations.

This section describes the programming characteristics and function of the 3000 interface. To fully understand this material, the reader should be familiar with 3000 I/O programming conventions and the 3000 I/O channel interface specifications.†

3000 INTERFACE OPERATIONS

The 3000 interface and supporting software performs the following operations.

- Connect operation — Transmits a 12-bit connect code from a NOC to the peripheral controllers.

  This code activates one of the eight possible controllers linked to the 3000 interface. It may also select one of several peripheral units subordinate to the controller.

† Refer to the 3000 I/O specification manual.

- **Function operation**

  Transmits a 12-bit function code from a normal channel to the previously connected peripheral controller.

  Function codes are commands that condition a peripheral controller for I/O operations.

- **Write operation**

  Transmits a series of 12-bit data bytes from an NOC to the previously connected peripheral controller.

  An output-from-A instruction is required to transmit each 12-bit byte. The data byte comes from the lower 12 bits of the A register.

  An odd parity bit must accompany each output data byte. The 3000 interface does not automatically generate the required parity bit. It is the responsibility of the driver software to generate an odd parity bit and place it in the NOC along with the data byte.

- **Read operation**

  Transfers a series of 12-bit data bytes from a peripheral controller to the BC via a NIC.

  A separate input-to-A instruction is required to read in each 12-bit byte. The input byte appears on the lower 12 bits of the input channel.

  An odd parity bit, generated by the 3000 peripheral controller, accompanies each input data byte. It appears on the NIC along with the 12 data bits. The 3000 interface does not check parity. If a parity check is desired, the driver software must be written to analyze each data byte and associated parity bit to determine if a parity error occurred during transmission from the peripheral controller to the 3000 interface.

- **Read status**

  Transfers a 12-bit status word from a peripheral controller to the BC via a NIC.

  An input-to-A instruction is required to read in the status word.

3000 INTERFACE NORMAL CHANNEL SIGNALS

Figure 3-11 shows the normal channel signals used by the SCU to control the 3000 interface. Channel and bit assignments given here are for the unit record station. 3000 SCU interface bit assignments may be different in other stations. Refer to appendixes A and B of this manual for a complete list of normal channel bit assignments for all stations.

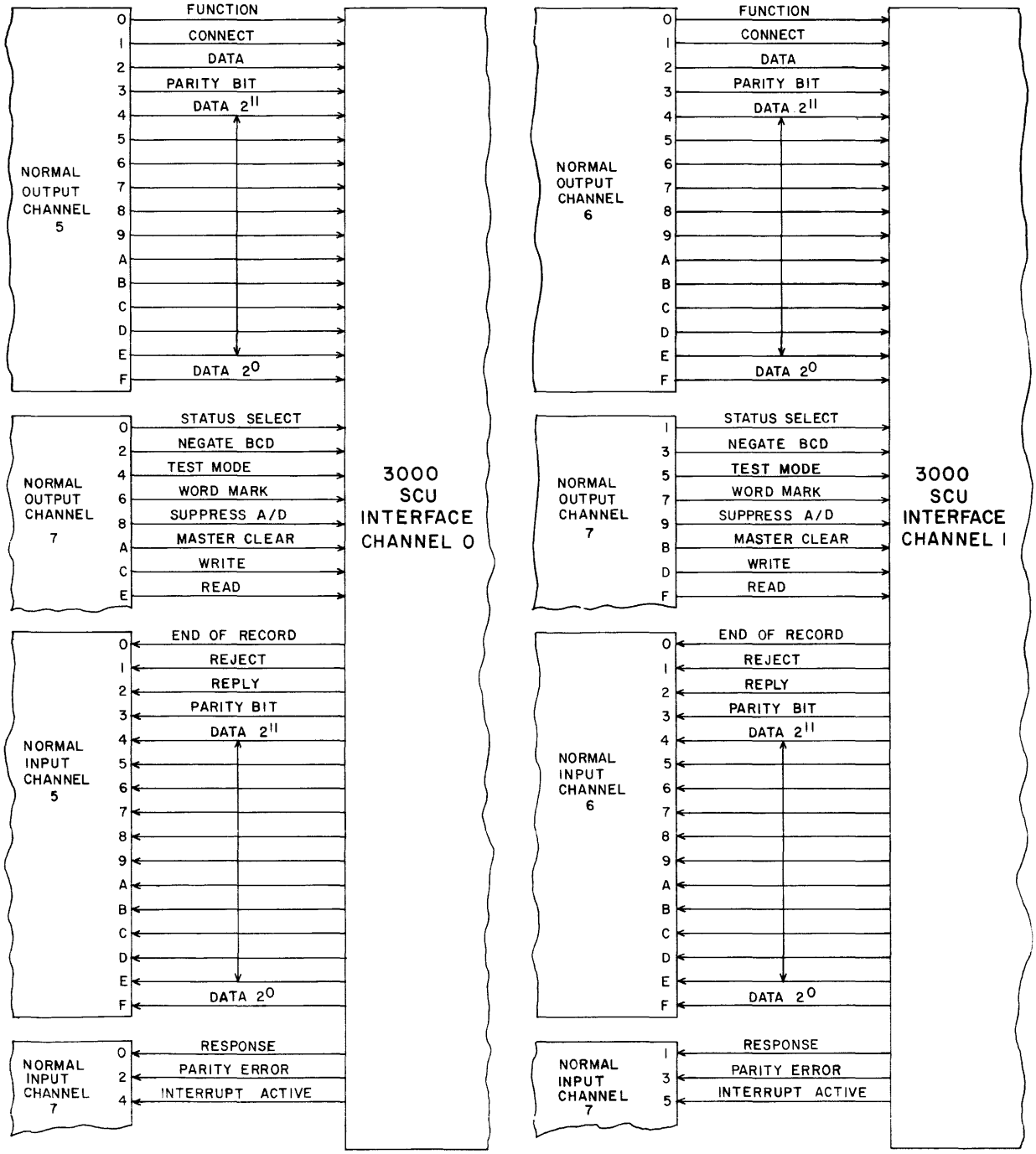


Figure 3-11. 3000 SCU Normal Channel Signals

Table 3-6 describes each of the normal channel bits used to control the 3000 interface.

TABLE 3-6. NORMAL CHANNEL BIT DEFINITIONS, 3000 SCU INTERFACE

Channel	Bit	Name	Function
NOC-5 and -6	0	Function	Setting this bit causes the 3000 interface to transmit a 12-bit function code and parity bit from the lower 13 bits of the output channel to the peripheral controller.
NOC-5 and -6	1	Connect	Setting this bit causes the 3000 interface to transmit a 12-bit connect code and parity bit from the lower 13 bits of the output channel to the peripheral controller.
NOC-5 and -6	2	Data signal	This bit acts as a data request to the peripheral controller. 1. Write operation; setting this bit causes the 3000 interface to transmit a 12-bit data byte and parity bit from the lower 13 bits of NOC-5 or -6. The data signal bit must remain set until the controller returns a reply (NIC-5 or -6, bit 2) 2. Read operation; setting this bit requests the controller to send a data byte. This bit must remain set until the controller returns a reply (NIC-5 or -6, bit 2) indicating that data byte is available for read-in.

TABLE 3-6. NORMAL CHANNEL BIT DEFINITIONS, 3000 SCU INTERFACE (Cont'd)

Channel	Bit	Name	Function
NOC-5 and -6	3	Output parity bit	This bit is an odd parity bit associated with the 12-bit connect code, function code, or output data byte that occupies the lower 12 bits of the output channel. It is the responsibility of the driver software to generate the odd parity bit for each code or data byte transmitted to the peripheral controller.
NOC-5 and -6	4	Output data/code bit 2^0	These 12 bits hold a connect code, function code, or output data byte that is transmitted to the peripheral controller.
NOC-5 and -6	F	Output data/code bit 2^{11}	
NOC-7	0	Status select (Channel 0)	When set, this bit selects the 12-bit status word, available from the peripheral controller, for input on NIC-5. When this bit is 0, data from the peripheral controller is available on NIC-5.
NOC-7	1	Status select (Channel 1)	Same as above for channel 1. Selects status or data for NIC-6.
NOC-7	2	Negate BCD conversion (Channel 0)	When set, this bit signals the peripheral controller to suppress the internal/external BCD conversion performed by some 3000 controllers. 1. During a read operation, this bit directs the controller not to convert BCD codes from external to internal form. During a write operation, this bit directs the controller not to convert BCD codes from internal to external form.

TABLE 3-6. NORMAL CHANNEL BIT DEFINITIONS, 3000 SCU INTERFACE (Cont'd)

Channel	Bit	Name	Function
NOC-7	3	Negate BCD conversion (Channel 1)	Same as above for channel 1.
NOC-7	4	Test mode (Channel 0)	Setting this bit selects test mode. When test mode is in effect, data transmitted on NOC-5 is looped back to NIC-5. Also, each time the connect, function, or data signal bit (NOC-5, bit 0, 1, or 2) is set to transmit a data byte, the 3000 generates a pseudo reply that appears on NIC-5, bit 2. The reply indicates that data sent out on NOC-5 can be read back in on NIC-5.
NOC-7	5	Test mode (Channel 1)	Same as above for channel 1. Data transmitted from NOC-6 is looped back to NIC-6.
NOC-7	A	Master clear (Channel 0)	When set, this bit causes the 3000 interface to send a master clear signal to the peripheral controller. The master clear signal clears out any internal operating conditions previously set up with functions and disconnects the peripheral controller.
NOC-7	B	Master clear (Channel 1)	Same as above for channel 1.
NOC-7	C	Write (Channel 0)	When set, this bit conditions the 3000 interface and peripheral controller for a write (output) operation. The write bit must remain set throughout a write operation.
NOC-7	D	Write (Channel 1)	Same as above for channel 1.
NOC-7	E	Read (Channel 0)	When set, this bit conditions the 3000 interface and peripheral controller for a read (input) operation. The read bit must remain set throughout a read operation.

TABLE 3-6. NORMAL CHANNEL BIT DEFINITIONS, 3000 SCU INTERFACE (Cont'd)

Channel	Bit	Name	Function
NOC-7	F	Read (Channel 1)	Same as above for channel 1.
NOC-7	6	Word mark (Channel 0)	When set, this bit causes the 3000 interface to transmit a word mark signal to the 3000 controller. Standard 3000 I/O channels, which assemble two or four 12-bit data bytes into a 24-bit or 48-bit memory word, send a word mark signal to designate the low-order byte in each memory word. Certain controllers are designed to transmit or accept only data bytes that correspond to the lowest byte in a memory word. That is, they respond only when a word mark signal accompanies the request to send or receive a data byte. In programming the 3000 interface, a safe practice is to always set this bit along with the data signal bit (NOC-5 or -6, bit 2) which is set to transmit or receive each data byte.
NOC-7	7	Word mark (Channel 1)	Same as above for channel 1.
NOC-7	8	Suppress assembly/disassembly (Channel 0)	When set, this bit signals the peripheral controller to stop the normal 6-bit/12-bit assembly-disassembly performed by some controllers. 1. During a read operation, this bit causes the controller to stop assembling two 6-bit characters into each 12-bit byte. Each input byte contains a single 6-bit character in the lower six bit positions.

TABLE 3-6. NORMAL CHANNEL BIT DEFINITIONS, 3000 SCU INTERFACE (Cont'd)

Channel	Bit	Name	Function
			2. During a write operation, this bit causes the controller to assume that each output byte contains a single 6-bit character in the lower six bit positions. The controller does not use the upper six bits of the byte. This bit does not affect the operation of a controller that does not perform 6-bit/12-bit assembly-disassembly.
NOC-7	9	Suppress assembly/ disassembly (Channel 1)	Same as above for channel 1.
NIC-5 and -6	0	End of record	When set, this bit indicates that the peripheral controller has reached the end of a record during a read operation and will send no more data until a new read operation is initiated via the 3000 interface. When the last input data byte in a record appears on input channel 5 or 6, this status bit sets instead of the reply status bit.
NIC-5 and -6	1	Reject	When set, this bit indicates that the peripheral controller has rejected a connect code or function code. 1. A connect code can be rejected only by a dual-access peripheral controller that has been connected or reserved on the other access channel; the access channel is not linked to the 3000 interface. 2. A function code may be rejected: a. If it is not a valid code for the controller to which it is directed, or b. If the function code conflicts with an operation the peripheral controller is performing.

TABLE 3-6. NORMAL CHANNEL BIT DEFINITIONS, 3000 SCU INTERFACE (Cont'd)

Channel	Bit	Name	Function
NIC-5 and -6	2	Reply	When set, this bit indicates that: 1. The peripheral controller has accepted a connect code, a function code, or an output data byte. 2. During a read operation, this bit indicates that an input byte from the peripheral controller is available on NIC-5 or -6.
NIC-5 and -6	3	Input parity bit	An odd parity bit generated by the peripheral controller that accompanies an input data byte.
NIC-5 and -6	4	Input data/ status bit 2^{11}	Two types of information from the peripheral controller can be read in on these normal channel bits: 1. Input data 2. A 12-bit status word The status word is selected for input by one of the following normal channel bits. 1. Status select bit (NOC-7, bit 0 or 1) = 1 2. Connect bit (NOC-5 or -6, bit 1) = 1 3. Function bit (NOC-5 or -6, bit 0) = 1 If all three of these select bits are 0, bits 4 through F_{16} can be used to read in data.
	F	Input data/ status bit 2^{0}	
NIC-7	0	Response (Channel 0)	Indicates that the peripheral controller has sent a reply, reject, or end of record signal to the 3000 interface. The individual status bits for these signals (NIC-5 and -6, bits 0, 1, and 2) can be checked to determine the type of response.

TABLE 3-6. NORMAL CHANNEL BIT DEFINITIONS, 3000 SCU INTERFACE (Cont'd)

Channel	Bit	Name	Function
NIC-7	1	Response (Channel 1)	Same as above for channel 1.
NIC-7	2	Output parity error (Channel 0)	When set, this bit indicates that the peripheral controller has detected a parity error in a function code or output data byte sent from the 3000 interface. This bit drops only if the 3000 interface master clears the controller.
NIC-7	3	Output parity error (Channel 1)	Same as above for channel 1.
NIC-7	4	Interrupt active (Channel 0)	When set, this bit indicates that one of the eight possible peripheral controllers is sending an interrupt signal to the 3000 interface. To determine the source of the interrupt, the 3000 interface must connect each controller and check the controller status word.
NIC-7	5	Interrupt active (Channel 1)	Same as above for channel 1.

PROGRAMMING SEQUENCES

The following sequences outline the programming steps required to drive a peripheral controller through the 3000 interface.

MAJOR STEPS

The steps required in a driver program depend, to a large extent, on the type of peripheral controller being driven. The order of steps suggested is a basic sequence that could be used with a number of standard 3000 controllers.

1. Connect peripheral controller

   This activates one of the controllers linked to the 3000 interface. Connect must always be the first step in any I/O operation. A peripheral controller cannot respond to any command from the 3000 interface unless connected.

2. Issue function codes

   This step usually follows connect. Most peripheral controllers must be prepared for an I/O operation with one or more function codes before data transfer can begin.

3. Read controller status word

   This step is often used after function codes are issued to determine if the connected peripheral controller is ready for a read or write operation. A 12-bit status word is always available from the connected peripheral controller. The 3000 interface can read in the status word any time data is not being read in.

4. Read or write operation

   Transmit or read in a series of 12-bit data bytes.

5. Read controller status word

   Status can be checked at the end of an operation to determine the reason for termination.

PROCEDURES

1. Connect peripheral controller

   a. Load lower 12 bits of A register, with connect code for controller to be activated.

   b. Generate parity bit for connect code and deposit in A register, bit 3.

   c. Set connect bit (A register, bit 1).

   d. Output-from-A to NOC-5.

   e. Wait for reply bit (NIC-5, bit 1).

      1) When reply bit = 1, go to step 1f.

      2) Absence of reply indicates that no controller connected. Repeat connect operation or go to an error routine.

   f. Clear connect bit (NOC-5, bit 1). The connect code can also be dropped.

5. Read controller status word

   A 12-bit status word is available from the connected peripheral controller at all times.

   a. Set status select bit (NOC-7, bit 0).

   b. Input-to-A from NIC-4.

      (The 12-bit status word is in the lower 12 bits of the A register.)

   c. Clear status select bit.

854 INTERFACE

The 854 interface controls data transfers between the 854 disk units and the SCU memory. The interface controls up to three units but can transfer data to only one unit at a time. Software supports only three units per interface. The interface is used only with the maintenance control units. Figure 3-12 shows the relationship between the interface and system elements with which it communicates.

Operation of the interface is controlled by the SCU through bits on normal channels 5, 6, and 7. Principle control responsibilities of the SCU in relation to the interface are as follows:

- Selects unit, cylinder, head, and sector.
- Controls read and write operations.
- Monitors status conditions.

DISK STORAGE DRIVE DESCRIPTION

The 854 disk storage drive is a high-speed, random access, disk storage device. Data is recorded on removable disk packs. Up to three 854 units are used with the 854 interface in the maintenance station.

Each unit contains six disks mounted on a common vertical spindle. Recording is done on only 10 surfaces of the six disks. The top side of the upper disk and bottom side of the lower disk are not used. The access mechanism for each unit consists of 10 arms mounted on a movable carriage. A read/write head is mounted on the end of each arm.

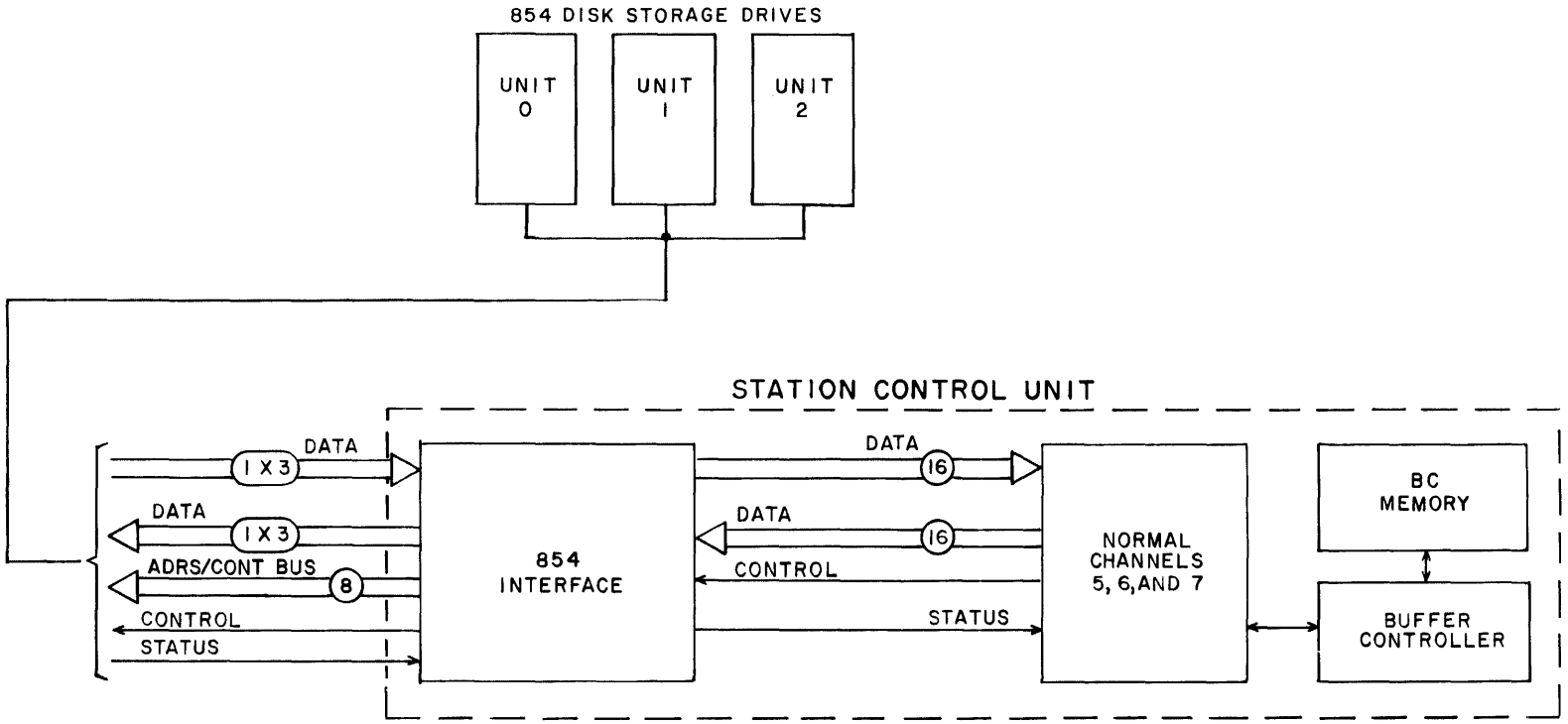


Figure 3-12. 854 Interface System Relationship

WRITE OPERATION

A selected write operation occurs immediately following the events previously described in Initial Procedure.

The software transfers the head gap, second sync pattern, and data field to the interface in 16-bit words. This information is written in serial fashion after the address tag checkword in the sector. As each 16-bit word is transferred from the interface to the sector, a flag status is returned to the software. Each time flag status comes up, the software must place another 16-bit word on the normal channels within 6.2 microseconds.

After the last word of the data field is written in the sector, a software-generated data checkword is written after the data field. The interface then writes the end of record after the data checkword.

READ OPERATION

A selected read operation occurs immediately following the events previously described in Initial Procedure.

The software then times out the 80 bits of the head gap and sends a zeros search signal to the interface. The interface then reads the second sync pattern from the disk in search for the sync bit.

After the interface detects the sync bit, it reads the first data word from the sector. When the 16-bit word is assembled in the interface, a flag status is sent to the software. Each time a word is read and flag status comes up, the software must transfer the word on the normal channels within 6.2 microseconds.

After the data field is read, the data checkword is read from the sector. The software compares the checkword with the data field just read. If the compare fails, a read error results.

854 INTERFACE NORMAL CHANNEL SIGNALS

Tables 3-7 and 3-8 describe the normal input and output channel bits used with the 854 interface. Bit assignments in the table are for the STAR-100 maintenance control unit. Refer to appendix A of this manual for a complete list of normal channel bit assignments for all stations.

TABLE 3-7. NIC-6A, -7 BIT DESCRIPTIONS FOR 854 INTERFACE

Channel	Bit	Name	Function
NIC-6A	0 ▼ 7	Selected units 0 through 7	These status bits from the units are used to check if more than one unit is selected.
NIC-6A	8	Flag	During a read operation this bit indicates that a 16-bit data word, data checkword, or a header address word is available on NIC-7. The BC must read in the word within 6.2 microseconds. The flag bit status clears normally after 6.2 microseconds from the time it set but may be cleared early by setting the reset flag bit (NOC-6A, bit 8). During a write operation this bit indicates that the interface is ready to accept a 16-bit data word, checkword, or header address word, on NOC-7. The BC must supply a data word within 6.2 microseconds, after flag status comes up.
NIC-6A	9	Sector mark	This status bit indicates detection of a sector reference mark from the selected unit. The bit remains set for 60 microseconds.
NIC-6A	A	Index mark	This status bit indicates detection of an index reference mark from the selected unit. The bit remains set for 60 microseconds, occurs once per revolution of the disk, and is in sync with sector mark status for sector 15.

TABLE 3-7. NIC-6A, -7 BIT DESCRIPTIONS FOR 854 INTERFACE (Cont'd)

Channel	Bit	Name	Function
NIC-6A	B	Ready	This status bit from the units indicates that the unit selected by unit select 2^0, 2^1, and 2^2 bits (NOC-6A) is available. Not ready conditions are: 1. Heads not loaded and motor not up to speed. 2. A disk pack not in the unit. 3. The unit ON LINE/OFF LINE switch in OFF LINE position.
NIC-6A	C	Seek error	This status bit from the units indicates that a direct seek in the selected unit has gone beyond the cylinder limits.
NIC-6A	D	On cylinder	This status bit from the units indicates that the selected unit has positioned the read/write heads at the addressed cylinder.
NIC-6A	E	On sector	This status bit from the units indicates that the addressed sector of the selected unit is one sector away from the recording head. The on sector status is a 1-millisecond pulse.
NIC-6A	F	Fault	This status bit from the units indicates that the selected unit has a fault condition. The fault condition must be manually cleared.
NIC-7	0 ↓ F	Input data bits 0 through F	These bits comprise the 16-bit data word that is read serially from the disk and assembled in the interface.

TABLE 3-8. NOC-5, -6A, -7 BIT DESCRIPTIONS FOR 854 INTERFACE

Channel	Bit	Name	Function
NOC-5	0 ↓ 7	Not used	
NOC-5	8	Channel switch† 2^1	This bit is used in conjunction with channel switch 2^0 bit (NOC-5) to select 854 interface, printer interface, or coupler B for transfer of NIC-6 and NOC-6 bits. If both bits are clear, NIC-6A and NOC-6A (854 interface) are selected.
NOC-5	9	Channel switch† 2^0	Refer to channel switch 2^1 bit (NOC-5).
NOC-5	A	Not used	
NOC-5	B	Not used	
NOC-5	C	Head select	This bit is sent to the selected unit and indicates that the address and control bits 0 through 3 (NOC-6A, bits 7 through 4) contain the head address.
NOC-5	D	Difference select	This bit is sent to the selected unit and indicates that the address and control bits 0 through 7 (NOC-6A, bits 7 through 0) contain positioning information (difference between unit's present cylinder address and new cylinder address.)
NOC-5	E	Control select	This bit is sent to the selected unit and indicates that the address and control bits 0 through 7 (NOC-6A, bits 7 through 0) contain control information.
NOC-5	F	Sector select	This bit is sent to the selected unit and indicates that the address and control bits 0 through 3 (NOC-6A, bits 7 through 4) contain the sector address.

† These two bits are inputs to the normal channel switch interface and are given here for reference.

TABLE 3-8. NOC-5, -6A, -7 BIT DESCRIPTIONS FOR 854 INTERFACE (Cont'd)

Channel	Bit	Name	Function
NOC-6A	0 ↓ 7	Address and control bits 7 through 0	These bits are sent to the selected unit. Information in these bits is determined by the accompaning head select, difference select, control select, or sector select bit (NOC-5). Information on the address and control bits is given in Table 3-9.
NOC-6A	8	Reset flag	This bit clears the flag status bit (NIC-6A) in the interface.
NOC-6A	9	Hold sector mark	This bit must be held at a constant 0 to enable the sector mark status bit (NIC-6A) to clear.
NOC-6A	A	Hold index mark	This bit is held at a constant 0 to enable the index mark status bit (NIC-6A) to clear.
NOC-6A	B	Write	This bit when set signals the interface to write data onto the disk. This bit when clear enables the interface to read data from the disk.
NOC-6A	C	Zeros search	This bit is set when address tag information is being read from the sector. It enables the flag status bit (NIC-6A) to set after the sync bit is read.
NOC-6A	D ↓ F	Unit select 2^2 through 2^0	These three bits provide a code that enables the interface to select one of the units. The code must be held to keep the unit selected.
NOC-7	0 ↓ F	Output data bits 0 through F	These bits comprise the 16-bit data word that is transferred serially from the interface shift register and written on the disk. The data is written in complement form. These bits must be all 1's during a read operation.

ADDRESS AND CONTROL BUS

The address and control bus in the interface consists of eight lines which transmit normal channel information to the selected unit. Information on these lines is determined by an accompaning normal channel tag line signal. Table 3-9 gives the relationship of the address and control bus and the tag line signals.

TABLE 3-9. ADDRESS AND CONTROL BUS FUNCTIONS

Address/ Control Bus	Tag Line			
	Difference Select	Sector Select	Head Select	Control Select
Bit 0 (NOC-6A, bit 7)	1	1	1	Write gate; a 1 input on this line enables the write drivers.
Bit 1 (NOC-6A, bit 6)	2	2	2	Read gate; a 1 input on this line enables the digital read data lines.
Bit 2 (NOC-6A, bit 5)	4	4	4	Seek forward; a 1 input on this line initiates forward carriage movement.
Bit 3 (NOC-6A, bit 4)	8	8	8	Not used
Bit 4 (NOC-6A, bit 3)	16	Not used	Not used	Erase gate; a 1 input on this line enables the erase driver to pass current through the head erase coil.
Bit 5 (NOC-6A, bit 2)	32	Not used	Not used	Seek reverse; a 1 input this line initiates reverse carriage movement.

NOTE

A timeout of each flag bit (6.2 microseconds) should be included in the program to eliminate the possibility of the program hanging up while waiting for the flag status to occur.

5. Input and verify the address tag on NIC-7, bits 0 through F.
6. Wait for the leading edge of next flag status (NIC-6A, bit 8).
7. Input and verify the address tag checkword (complement of address tag) on NIC-7, bits 0 through F.
8. If next operation is a read operation, leave all 1's in NOC-7. For a write operation, clear all bits of NOC-7.

READ OPERATION

1. Wait 45 microseconds to allow for the gap between read/write and erase heads.
2. Set and clear zeros search bit (NOC-6A, bit C).
3. Wait for leading edge of flag status (NIC-6A, bit 8).
4. Input and store 104 data words and one data checkword on NIC-7, bits 0 through F. Each word is read on the leading edge of the flag status (NIC-6A, bit 8) which occurs every 12.4 microseconds.
5. Verify that the half added sum of the data equals the data checkword shifted left around eight places.
6. If in half tracking mode, return to step 9 of Sector and Head Selection within 1.6 milliseconds and repeat the procedure.

WRITE OPERATION

1. Set write bit (NOC-6A, bit B).
2. Set erase gate bit (NOC-6A, bit 3).
3. Set write gate bit (NOC-6A, bit 7).
4. Set control select bit (NOC-5, bit E).
5. Wait for leading edge of flag status (NIC-6A, bit 8).
6. Output the following data on NOC-7, bits 0 through F.

5 words of all 1's (head gap)
3 words of all 0's, except last bit a 1 (second sync pattern)
104 words of data (data field)
1 word (data checkword)
1 word of all 0's except last bit a 1 (end of record)

Each output word must be conditioned by the leading edge of flag status (NIC-6A, bit 8).

7. Clear write bit (NOC-6A, bit B), erase gate bit (NOC-6A, bit 3). Write gate bit (NOC-6A, bit 7), and control select bit (NOC-5, bit E).

8. If in half tracking mode, return to step 9 of Sector and Head Selection within 1.6 milliseconds and repeat the procedure.

WRITE TAG OPERATION

Repeat the steps in the Write Operation, except in step 6 output the following data on NOC-7, bits 0 through F.

5 words of all 1's (tolerance gap no. 1)
2 words of all 0's, except last bit a 1 (sync pattern)
1 word (address tag)
1 word (address tag checkword, complement of address tag)

STAR-100 MAINTENANCE INTERFACE

NOTE

Since the maintenance, SAC coupler, and control interfaces of the maintenance control unit operate in such interlocking detail with the STAR-100 Computer, it is imperative that the reader be familiar with STAR-100 operation and its programming conventions to fully understand the following material.

The maintenance interface in the maintenance control unit acts as a special control area for the multiple access lines between the maintenance control unit and a STAR-100 Computer mainframe (refer to Figure 3-15). Normal input and output channels 8 through F receive status information from the computer and carry function commands to the computer. Normal input and output channels 0 through 7 carry information between the various peripheral devices and the MCU.

The BC in the MCU controls the flow of function commands to the computer and orders status checks to be made. Normal channel bit definitions for the maintenance interface are given in Tables 3-10 and 3-11.

TABLE 3-10. NIC-8 THROUGH NIC-F BIT DESCRIPTIONS FOR MAINTENANCE INTERFACE (Cont'd)

Channel	Bit	Name	Function
NIC-F (CPU chan ATB8)	2	Multiple match	This bit indicates that a CPU fault in a lock-virtual page address combination occurred in the page table.
NIC-F (CPU chan ATB8)	3	Absolute sword bounds hit	This bit indicates that the memory reference the maintenance interface has made is within the limits of a specified block of memory.
NIC-F (CPU chan ATB8)	4	Event stop	This bit indicates that the CPU stopped in response to the stop counter A or B lines being set previously.
NIC-F	5	Not used	
NIC-F	6	Not used	
NIC-F (CPU chan ATB8)	7	Monitor mode	This bit indicates that CPU software is operating in the monitor mode.
NIC-F	8	Temperature/dewpoint alarm	This bit indicates that either the temperature or relative humidity in the computer have exceeded allowable limits.
NIC-F	9	MG1 power failure	This bit indicates that 60 Hz source power to the primary MG set has failed.
NIC-F	A	Section power fail	This bit indicates that a particular section, but not all, of the computer has experienced a power failure.
NIC-F	B	System power margin (+5%)	This bit indicates that system power levels have exceeded the positive tolerance figure.

TABLE 3-10. NIC-8 THROUGH NIC-F BIT DESCRIPTIONS FOR MAINTENANCE INTERFACE (Cont'd)

Channel	Bit	Name	Function
NIC-F	C	System power margin (-5%)	This bit indicates that system power levels have become more negative than allowable.
NIC-F	D	MG2 power failure	This bit indicates that 60 Hz source power to the standby MG set has failed.
NIC-F	E	CPU idle	This bit indicates that the computer's CPU is in the idle state.
NIC-F	F	CPU stopped	This bit indicates that the computer's CPU is stopped due to some abnormal condition or due to some external influence (such as the MCU issuing a bit to stop the CPU under specified conditions).

TABLE 3-11. NOC-8 THROUGH NOC-F BIT DESCRIPTIONS FOR MAINTENANCE INTERFACE

Channel	Bit	Name	Function
NOC-8 (CPU chan BTA1)	0	Master clear	This signal is sent to SAC and central memory modules of the computer. It clears the SAC I/O channels and the devices connected to those I/O channels.
NOC-8	1	Stop	Issuing this signal will stop the computer before the next instruction is issued.

TABLE 3-11. NOC-8 THROUGH NOC-F BIT DESCRIPTIONS FOR MAINTENANCE INTERFACE (Cont'd)

Channel	Bit	Name	Function
NOC-8	2	Step†	Issuing this signal permits the execution of one instruction. (Any faults must be cleared before the computer can be stopped.)
NOC-8	3	Run†	Issuing this signal permits starting the computer from a manual stop or fault stop. (Faults must be cleared before computer can be started.)
NOC-8	4	Store associative register†	Issuing this signal permits storing the associative registers and register file in CPU central memory. Associative registers are stored starting at absolute address 4000_{16}. The register file is stored starting at absolute address 0000_{16} in monitor mode and at virtual address 0000_{16} in job mode. After this operation both must be reloaded by executing a load associative register command.
NOC-8	5	Load associative register†	Issuing this signal permits loading the associative registers and register file from CPU central memory. Associative registers are loaded starting from absolute address 4000_{16}. The register file is loaded starting at absolute address 0000_{16} in monitor mode and at virtual address 0000_{16} in job mode.

† Computer must be stopped before issuing these commands.

TABLE 3-11. NOC-8 THROUGH NOC-F BIT DESCRIPTIONS FOR MAINTENANCE INTERFACE (Cont'd)

Channel	Bit	Name	Function
NOC-8 (CPU chan BTA1)	6	Stream/FP master clear	Issuing this signal sends a master clear to the streaming and floating point modules of the computer. SAC and central memory modules are not included. This signal must be set at minimum of 1 microsecond.
NOC-8	7	Clear faults	Issuing this signal clears the following conditions and allows the computer to be restarted with a run signal (NOC-8, bit 3). 1. Memory parity fault 2. Microcode memory parity fault 3. Multiple match 4. Absolute sword bounds hit 5. Parity fault address register and bounds hit address register
NOC-8	8	Not used	
NOC-8	9	Sync	This signal is used by the CPU to gate CPU data back to the MCU. When reading display registers, the sync signal must be set after the read signal is set.
NOC-8	A	Not used	
NOC-8	B	Read	This signal transfers the selected register and CIAR into the MCU's display register.

TABLE 3-11. NOC-8 THROUGH NOC-F BIT DESCRIPTIONS FOR MAINTENANCE INTERFACE (Cont'd)

<table>
<tr><th>Channel</th><th>Bit</th><th>Name</th><th>Function</th></tr>
<tr><td>NOC-8
↓</td><td>C
D
E
F</td><td>Register select 2^3
2^2
2^1
2^0</td><td>These bits represent a 4-bit code sent by the MCU to the HLP to select one of several CPU registers for inputs to the maintenance interface. (Refer to Table 3-12.)</td></tr>
<tr><td>NOC-9
(CPU chan BTA2)</td><td>0</td><td>Sweep mode</td><td>Issuing this bit causes all instructions to act as passes.</td></tr>
<tr><td></td><td>1</td><td>Interrupt gate</td><td>When this signal is a 1, time interrupts and external interrupts will only be processed between instruction.</td></tr>
<tr><td></td><td>2</td><td>Block instruction execution overlap</td><td>This signal will allow only one register instruction to be execution at any time.</td></tr>
<tr><td></td><td>3</td><td>Channel register select 2^1</td><td rowspan="2">These two bits form a code which permits the selection of any of three CPU registers via NOC-A. The code is:
<table>
<tr><th>bit 3(2^1)</th><th>bit 4(2^0)</th><th>CPU Reg. Sel.</th></tr>
<tr><td>0</td><td>0</td><td>None</td></tr>
<tr><td>0</td><td>1</td><td>Channel register A1</td></tr>
<tr><td>1</td><td>0</td><td>Channel register A2</td></tr>
<tr><td>1</td><td>1</td><td>Channel register A3</td></tr>
</table></td></tr>
<tr><td></td><td>4</td><td>Channel register select 2^0</td></tr>
<tr><td></td><td>5</td><td>Clock adjust</td><td>Setting this bit enables adjustment of the CPU clocks.</td></tr>
<tr><td>↓</td><td>6</td><td>Decrease clock frequency</td><td>This bit is used to decrease clock frequency.</td></tr>
</table>

TABLE 3-11. NOC-8 THROUGH NOC-F BIT DESCRIPTIONS FOR MAINTENANCE INTERFACE (Cont'd)

Channel	Bit	Name	Function
NOC-9 (CPU chan BTA2)	7	Increase clock frequency	This bit used to increase clock frequency.
	8	Delay trailing edge	This bit is used to delay the trailing edge of all of the clocks on the CPU panel which is specified by NOC-9, bits B through F. If bit 8 and bit 9 are set, only the odd or even clocks on a panel are moved depending on bit A.
	9	Delay leading edge	This bit is used to delay the leading edge of all of the clocks on the panel which is specified by NOC-9, bits B through F. If bits 8 and 9 are set, only the odd or even clocks on a panel are moved depending on bit A.
	A	Move clocks	0, move even clocks (refer to description for bit 8 or 9). 1, move odd clocks.
NOC-9 (CPU chan BTA2)	B C D E F	Panel designators	These bits are used in hex codes to identify panel designators for clock margins. Bit B is the leftmost bit of the designator. They are defined as follows:

Designator Hex Code	CPU Panel(s)
00	All panels
01	All floating point panels
02	All SAC panels
03	All stream and string panels
04	Not used
05	Direct access channel

TABLE 3-11. NOC-8 THROUGH NOC-F BIT DESCRIPTIONS FOR MAINTENANCE INTERFACE (Cont'd)

Channel	Bit	Name	Function		
NOC-9 (CPU chan BTA2)			Designator Hex Code	CPU Panel(s)	
			06	Panel AA	Floating point module
			07	Panel AB	
			08	Panel BA	
			09	Panel BB	
			0A	Panel CA	
			0B	Panel CB	
			0C	Panel DA	
			0D	Panel DB	
			0E	Panel EA	
			0F	Panel EB	
			10	Panel KA	SAC module
			11	Panel KB	
			12	Panel LA	
			13	Panel LB	
			14	Panel NA	
			15	Panel NB	
			16	Panel PA	Stream, string module
			17	Panel PB	
			18	Panel FA	
			19	Panel FB	
			1A	Panel GA	
			1B	Panel GB	
			1C	Panel HA	
			1D	Panel HB	
			1E	Panel JA	
			1F	Panel JB	
NOC-A1 (CPU chan BTA3-1)	0	Not used			
	1	Disable channel 1	These bits are transmitted to the SAC module in the computer. Whichever bit is set disables the corresponding channel and no central memory references will be allowed from that channel.		
	2	2			
	3	3			
	4	4			
	5	5			

TABLE 3-11. NOC-8 THROUGH NOC-F BIT DESCRIPTIONS FOR MAINTENANCE INTERFACE (Cont'd)

Channel	Bit	Name	Function
NOC-A1	6	Disable channel 6	
(CPU chan BTA3-1)	7	7	
↓	8	8	
	9	9	
	A	10	
	B	11	
	C	12	
	D	Not used	
	E	Not used	
	F	Not used	
NOC-A2	0	Select memory group 2^1	For maintenance purposes the memory strobe on CPU memory may be advanced or delayed by setting either bit 2 or 3, as appropriate. Memory is divided into four-section groups (16 banks per group) of which one group is selected for margin tests. The four-section groups correspond to a memory wing. Thus a program can be written to run in a portion of memory not experiencing strobe margin failures and test a portion of memory experiencing strobe margin failures. The code used by bits 0 and 1 to select a memory group is:
(CPU chan BTA3-2)	1	Select memory group 2^0	
	2	Delay memory strobe	
	3	Advance memory strobe	

bit 0	bit 1	
0	0	Selects sections MA-MD
0	1	Selects sections ME-MH
1	0	Selects sections MJ-MM
1	1	Selects sections MN-MR

TABLE 3-11. NOC-8 THROUGH NOC-F BIT DESCRIPTIONS FOR MAINTENANCE INTERFACE (Cont'd)

Channel	Bit	Name	Function
NOC-A2 (CPU chan BTA3-2)	4 5 6 7	Disable memory Parity check	CPU memory is divided into 262K blocks each of which may have its parity check disabled. This procedure facilitates troubleshooting a section of memory while the CPU continues normal job execution with minimum interference. Setting the appropriate bit disables the parity check on memory addresses as follows: Bit 4; addresses 0 through 0 FFF FFF Bit 5; addresses 1 000 000 through 1 FFF FFF Bit 6; addresses 2 000 000 through 2 FFF FFF Bit 7; addresses 3 000 000 through 3 FFF FFF These are absolute addresses and correspond to physical addresses only if no swaps have been made or if phase 16 is in effect.
NOC-A2 (CPU chan BTA3-2)	8	Stop on I/O parity fault	Setting this bit enables the CPU to stop whenever a central memory parity fault is found in data going to I/O logic.
NOC-A2	9	Not used	
NOC-A2	A	Not used	
NOC-A2	B	Not used	
NOC-A2	C	Swap 131K	Setting this bit causes bit 40 of central memory address to be toggled and facilitates testing that part of memory where the memory test is located. The effect is to swap alternate 131K word blocks.

TABLE 3-11. NOC-8 THROUGH NOC-F BIT DESCRIPTIONS FOR MAINTENANCE INTERFACE (Cont'd)

Channel	Bit	Name	Function
NOC-A2 (CPU chan BTA3-2)	D	Phase 16	Setting this bit, one of the memory degradation lines, causes sequential memory addresses to sweep through 16 banks rather than 32. This is accomplished by interchanging specified memory address bits in computer memory. When phase 16 is set, a time penalty is unavoidable on certain instructions due to the lower order of bank interleaving.
NOC-A2	E	Swap 262K	Setting this bit causes memory address bit 50 to be toggled. If phase 16 bit is clear, alternate 128-word blocks are exchanged. If phase 16 bit is set, the effect is to interchange upper and lower 262K of memory.
NOC-A2	F	Swap 524K	Setting this bit causes memory address bit 38 to be toggled. The effect is to interchange upper and lower 524K.
NOC-A3 (CPU chan BTA3-3)	0	Absolute addressing	Setting this bit forces all central memory references to be absolute addresses.
NOC-A3	1	Test associative registers	Setting this bit toggles bit 30 (2K select) of central memory address when storing the associative registers. The associative registers are then stored at absolute bit address $24,000_{16}$. Therefore, the associative registers may be repeatedly loaded with a fixed pattern and stored in memory for inspection.

TABLE 3-11. NOC-8 THROUGH NOC-F BIT DESCRIPTIONS FOR MAINTENANCE INTERFACE (Cont'd)

Channel	Bit	Name	Function
NOC-A3 (CPU chan BTA3-3)	2	Test data paths	Setting this bit toggles bit 30 when storing the register file and forces a register file store during an initial load. The register file is stored at absolute bit address $20,000_{16}$ and loaded from address 0. Testing of the data paths to and from central memory is facilitated using this procedure and absolute addressing.
NOC-A3	3	Test invisible package	Setting this bit toggles bit 30 when storing the invisible package. The invisible package is stored 2048_{10} words ahead or behind where it is loaded. Therefore, the test mode can be used starting with a given initial invisible package to see the result of CPU activity on the invisible package.
NOC-A3	4 ↓ F	Not used	
NOC-B	0	Not used	
(CPU chan BTA4)	1	External flag chan 1	These bits are sent to the computer which in turn sends them on to the appropriate device via an I/O channel. They are used to initiate an autoloading sequence in the BC of the MCU.
↓	2	2	
	3	3	
	4	4	
	5	5	
	6	6	
	7	7	
	8	8	
	9	9	
	A	10	
	B	11	
	C	12	

TABLE 3-11. NOC-8 THROUGH NOC-F BIT DESCRIPTION FOR MAINTENANCE INTERFACE (Cont'd)

Channel	Bit	Name	Function
NOC-B (CPU chan BTA4)	D	Not used	
	E	1 upper bounds	Setting this bit identifies the bits on NOC-C as the upper bounds sword address.
		0 lower bounds	Clearing this bit identifies the bits on NOC-C as the lower bounds sword address.
	F	1 bounds in upper 524K	When bit F is set, this bit identifies the address on NOC-C as being in the upper 524K of memory.
		0 bounds in lower 524K	When bit F is clear, this bit identifies the address on NOC-C as being in the lower 524K of memory.
NOC-C (CPU chan BTA5)	0	Bounds sword Address bit 00	These bits represent either the upper or lower bounds sword address as determined by the state of bit E of NOC-B. Bit 0 of this word is the leftmost bit of the sword address in 524K memory. (Refer to bit F of NOC-B.)
	F	Address bit 15	
NOC-D (CPU chan BTA6)	0	Check bounds on memory reads	When set, bits 0 through 4 provide the means for the MCU to selectively test various categories of requests for inbounds conditions of memory references. Any combination of classes may be selected. If the CPU has been stopped by a bounds hit (bit 4), the maintenance interface must set bit 7 (clear fault) of NOC-8 before the CPU can be restarted. The CPU can then be restarted by
	1	Check bounds on memory writes	
	2	Check bounds on CPU references	
	3	Check bounds on channel references	
	4	Stop CPU on bounds hit	

TABLE 3-11. NOC-8 THROUGH NOC-F BIT DESCRIPTIONS FOR MAINTENANCE INTERFACE (Cont'd)

Channel	Bit	Name	Function
NOC-D (CPU chan BTA6)			setting bit 3 (run) of NOC-8, and it will execute the next instruction in sequence. To identify a second bounds hit, the maintenance interface must set bit 7 (clear fault) of NOC-8 so that another bounds hit can be detected on NIC-F, bit 3.
	5	Enable bounds check	Setting this bit enables the particular bounds checking bit(s) (bits 0 through 4) to perform their intended function(s). The conditions desired in bits 0 through 4 must be set before setting this bit.
	6	Count A	Setting this bit initiates operation of counter A. The proper counter specification (bit F) and bits 8 through E of this channel must be set up before this count line is enabled.
	7	Count B	Same explanation as counter A but applied to counter B.
	8	Clear counter overflow bits	Setting this bit clears only the upper bit of each 32- or 16-bit counter. If the bit is cleared, both A & B counters are cleared after the read signal (NOC-8, bit B) is received and after both counters are transferred into the maintenance interface's display registers.
	9 A	Stop counter A Stop counter B	Setting either of these bits causes the event incrementing either of the 16-bit counter pairs to stop the CPU. Clear fault (NOC-8, bit 7) clears the condition.

TABLE 3-11. NOC-8 THROUGH NOC-F BIT DESCRIPTIONS FOR MAINTENANCE INTERFACE (Cont'd)

Channel	Bit	Name	Function
NOC-D (CPU chan BTA6)	B C D E	Carry into A1 Carry into A2 Carry into B1 Carry into B2	These bits are used for reconfiguring CPU counter word size during monitoring functions. Setting bit B enables the carry into counter A1 from counter A2. Clearing both A1 and A2 allows counters to operate as two 16-bit counters. To obtain a 32-bit count, clear A1 and set A2. If both lines of a counter pair are set and NOC-D, bit 8 is set, undefined results occur when the counters are cleared.
NOC-D	F	1 Counter B specifications 0 Counter A specifications	Setting this bit selects counting specifications on NOC-E, bits 0 through F for counter B. Clearing this bit selects counting specifications on NOC-E, bits 0 through F for counter A.
NOC-E (CPU chan BTA7)	0 ↓ 9	Counter A1/B1 event select codes ↓ Counter A2/B2 event select codes	Setting the desired bit(s) in this group determines which counter pair and event will be selected by the maintenance interface for monitoring purposes. Bits 0 through 4 apply to counter pair A1/B1, and bits 5 through 9 apply to A2/B2. (Refer to Table 3-13).
	A	Not used	
	B	All jobs enable	Setting this mask bit enables the counters to be incremented for any selected event.

TABLE 3-11. NOC-8 THROUGH NOC-F BIT DESCRIPTIONS FOR MAINTENANCE INTERFACE (Cont'd)

Channel	Bit	Name	Function
NOC-E (CPU chan BTA7)	C	Monitor mode mask	Setting this bit enables counters to be incremented only when the CPU is in monitor mode.
	D	Job mode mask	Setting this masking bit enables a count to be made during CPU selected jobs only.
	E	Data flag bit 56 mask	Setting bit E enables counters to be incremented for sword address on NOC-C and CPU selected functions on NOC-D, bits 0 through F.
	F	Data flag bit 57 mask	Setting bit F enables counters to be incremented for sword address on NOC-C and CPU selected events and masks on NOC-E, bits 0 through F.
NOC-F (CPU chan BTA8) ↓	0	Function select bit 2^7	These 8 bits constitute a function select code which determines the count condition sent to the CPU. If the select code and the corresponding hex code (refer to hex code 12, Table 3-13) bits are equal, wherever there is a 1 in the mask, the counter will be incremented. If the mask contains all zeros, all instructions will be counted. Bit 0 is the leftmost bit of the code.
	1	↓ 2^6	
	2	↓ 2^5	
	3	↓ 2^4	
	4	↓ 2^3	
	5	↓ 2^2	
	6	↓ 2^1	
	7	↓ 2^0	
↓	8	Mask bit 2^7	These 8 bits constitute a mask for the function code used with the function select bits (bits 0 through 7) to define the masking to be used. Bit 8 is the leftmost bit of the code.
	9	↓ 2^6	
	A	↓ 2^5	
	B	↓ 2^4	
	C	↓ 2^3	
	D	↓ 2^2	
	E	↓ 2^1	
	F	↓ 2^0	

MAINTENANCE INTERFACE MONITORING ACTIVITIES

The maintenance interface of the MCU performs all the system monitoring functions required for computer system operation. The maintenance interface monitors the outputs of its two display registers as its main medium of evaluating system activity, monitors four 16-bit counters in the CPU, and can request microcode memory status and selected CPU status.

DISPLAY REGISTER MONITORING

Two maintenance interface display registers are used for this function; one always contains the output of the current instruction address register (CIAR) in the CPU and the other contains the output of a register selected by a 4-bit code sent to the CPU by the maintenance interface. The code used for register selection is transmitted to the CPU via NOC-8, bits C through F. The maintenance interface must also set NOC-8, bit 8 (read) to enable the CPU to transfer data from its CIAR and data from the selected register to the maintenance interface display registers. Note that the maintenance interface must set up the register select code before issuing the read signal to the CPU. The CIAR is received at the maintenance interface via the bits of NIC-8, NIC-9, and NIC-A. Data from the code-selected register is received via the bits of NIC-B through NIC-E. Select codes and their corresponding registers are listed in Table 3-12.

TABLE 3-12. MAINTENANCE INTERFACE SELECT CODES

Hex Code	Register(s) Selected	Bits
0	Current instruction address register (CIAR)	0-63
1	Data flag register	0-63
2	Invisible package address (absolute bit address)	0-31
	Page zero address (absolute bit address)	32-63
3	External interrupt register	17-31
	Channel 1	17
	2	18
	3	19
	4	20
	5	21
	6	22
	7	23

The control interface in the MCU is connected to the microcode memory module of an HLP such as the STAR-100 or STAR-65 via an I/O channel similar to a STAR data channel. The control interface connects to the block transfer channel of the BC and is programmed as the SAC coupler except that different normal channels are used for control. The microcode memory (or HLP) end of the channel is like a standard A coupler with channel control and fanin/fanout logic between the channel and the 224-bit microcode words. The A coupler in the HLP does not use the following lines normally used in a STAR data channel:

1. Parity error from A (PEFA)

   The A coupler does not check parity on any function sent by the control interface or does not send a parity error to the control interface on a microcode parity error. The MCU checks for microcode parity errors via the normal channel lines between the MCU and the CPU just as it would for any other CPU parity error.

2. Illegal from A (IFA)
3. Interrupt from B (IFB)
4. System control [such as control strobe from A (CSFA) or control from A (CFA)]
5. No parity is sent with data on a read operation

Refer to publication number 60429400 for a complete description of a STAR data channel.

The BC in the MCU uses the block transfer channel for data transfers through the control interface and normal channel 6C for function codes and control of the control interface.

CONTROL INTERFACE TO A COUPLER FUNCTION CODES

The control interface in the MCU sends function codes via the I/O channel as directed by the BC. These codes are sent to the A coupler (or microcode memory module) via NOC-6C, bits 1, 2, and 3 and are defined in Table 3-14.

TABLE 3-14. FUNCTION CODES FOR CONTROL INTERFACE/MICROCODE MEMORY INTERFACE

Bit $3(2^0)$	Bit $2(2^1)$	Bit $1(2^2)$	Name	Function
0	0	0	Null	Automatically sent by control interface as the second half of any function.
0	0	1	Read memory	Read a block of microcode memory from the current microcode address.
0	1	0	Write memory	Write a block of microcode memory from the current microcode address.
0	1	1		Not normally used, but performs the same as an EOP in computer.
1	0	0	Data	Automatically sent with data during a write microcode memory operation.
1	0	1	Read status	Read the current microcode status (explained in detail later in this section).
1	1	0	Write switch	Switches that provide control of microcode execution (explained in detail later in this section).
1	1	1	EOP	End of operation clears microcode memory interface of all previous functions and also clears counter that controls data fanin/fanout to and from the I/O channel.

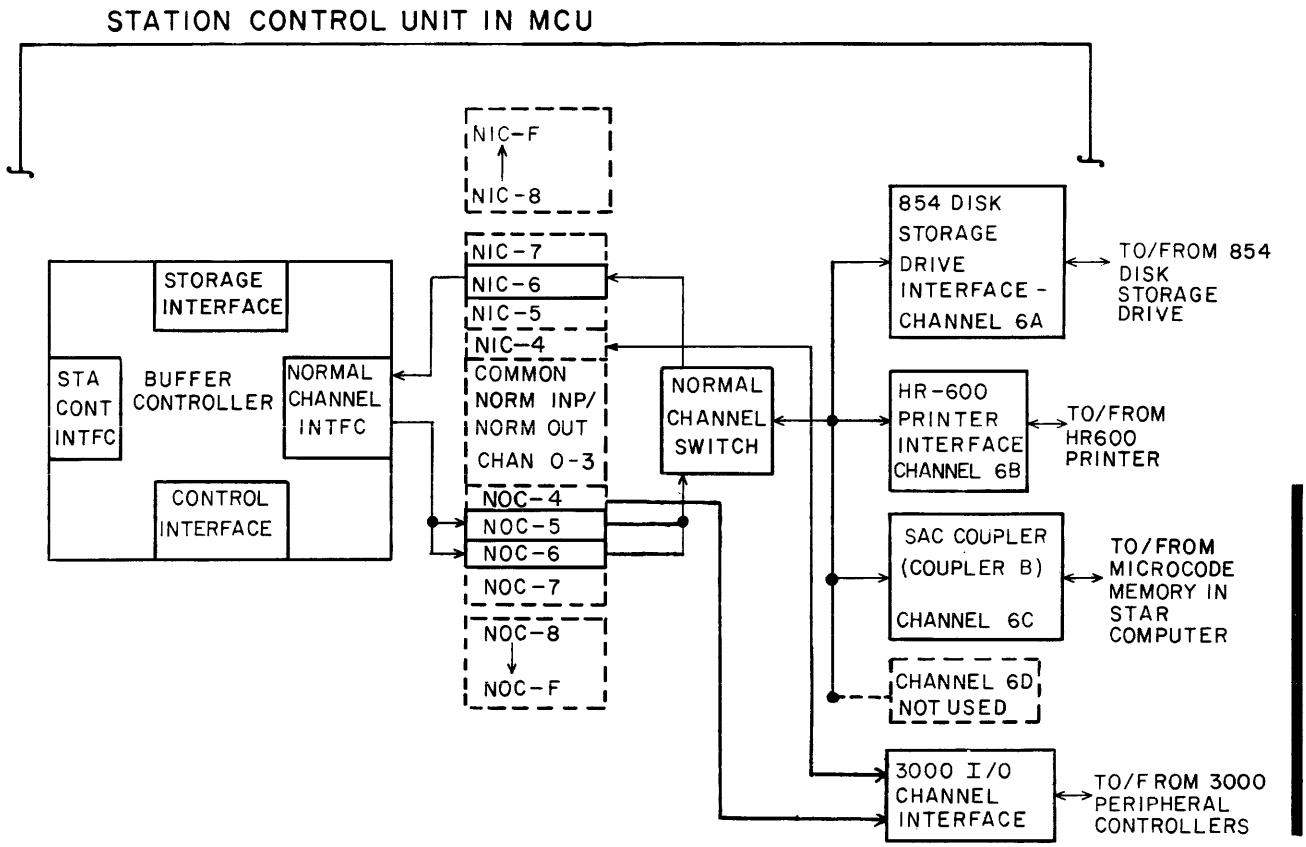


Figure 3-18. Normal Channel Switch/Normal Channel 6 Relationship

PROGRAMMING SEQUENCES

Since the HR600 printer is completely controlled by software, only a general sequence of events is included in the following paragraphs.

1. Initially, the software initiates the following bits.

   Sets advance ribbon bit (NOC-6B, bit 2)
   Selects 6/8 lines per inch printing density (NOC-6B, bit 1)
   Tests status for the start bit (NIC-3, bit 7)
   Tests the start indicator (NOC-6B, bit 0)
   Sets status for index pulse (NIC-3, bit 4) to establish drum synchronism at a drum speed of 800 rpm. At this speed an index pulse occurs every 75 milliseconds.

2. Following the index pulse, software checks for a drum row pulse (NIC-3, bit 5). There are 63 drum row pulses between each index pulse. Since a drum row pulse corresponds to a character row, the software must match the character to be printed with the correct drum row pulse.

3. When the correct drum row pulse is determined, the hammer address(es) (NOC-6B, bits 8-F) is sent to the printer to specify which of the 136 hammers are to be fired.

4. The compare bit (NOC-6B, bit 5) strobes the hammer address to the printer.

5. The hammer enable bit (NOC-6B, bit 4) causes all hammers previously addressed for the specified drum row pulse to fire. From the initial sensing of the drum row pulse, the software has 1.17 milliseconds to print the character.

6. Steps 2 through 5 are repeated until all characters on that line are printed.

7. After all characters for one line are printed, the software advances the paper (NOC-6B, bit 3) to print the next line and continues printing subsequent lines.

TABLE 4-3. NOC-5 KEYBOARD INDICATOR SELECT BITS FOR SDU COUPLER INTERFACE

Bit 0	Selects LOCKOUT light group 0	Selects LOCKOUT light group 2
1	Selects LOCKOUT light group 1	Selects LOCKOUT light group 3
2	Selects ALERT light group 0	Selects ALERT light group 2
3	Selects ALERT light group 1	Selects ALERT light group 3
4	Selects ALERT alarm group 0	Selects ALERT alarm group 2
5	Selects ALERT alarm group 1	Selects ALERT alarm group 3
6	Not used	Not used
7	Not used	Not used
8	Not used	Not used
9	Selects keyboard 1 or 8	Selects keyboard 15 or 22
A	Selects keyboard 2 or 9	Selects keyboard 16 or 23
B	Selects keyboard 3 or 10	Selects keyboard 17 or 24
C	Selects keyboard 4 or 11	Selects keyboard 18 or 25
D	Selects keyboard 5 or 12	Selects keyboard 19 or 26
E	Selects keyboard 6 or 13	Selects keyboard 20 or 27
F	Selects keyboard 7 or 14	Selects keyboard 21 or 28
	Bit A of NOC-6 used to strobe selects bits to SDU.	Bit 9 of NOC-6 used to strobe selects bits to SDU.

NOTE

Group 0 is keyboards 1-7
Group 1 is keyboards 8-14
Group 2 is keyboards 15-21
Group 3 is keyboards 22-28

MEMORY MAP

Figure 4-11 shows the assignment of buffer areas and cursor address areas within a 4K segment of SDU memory. The SDU can contain up to four 4K segments. Each one serves a group of seven display units. Memory allocation is the same within each of the four segments.

SDU Memory Address				
X000-X1FF	512 words	monitor unit 1	A Field	Buffer Areas
X200-X3FF	512 words	monitor unit 2		
X400-X5FF	512 words	monitor unit 3		
X600-X7FF	512 words	monitor unit 4		
X800-X9FF	512 words	monitor unit 5		
XA00-XBFF	512 words	monitor unit 6		
XC00-XDFF	512 words	monitor unit 7		
XE00-XE3F	64 words	monitor unit 1	B Field	
XE40-XE7F	64 words	monitor unit 2		
XE80-XEBF	64 words	monitor unit 3		
XECO-XEFF	64 words	monitor unit 4		
XF00-XF3F	64 words	monitor unit 5		
XF40-XF7F	64 words	monitor unit 6		
XF80-XFBF	64 words	monitor unit 7		
XFC0-XFC7	8 words	monitor unit 1	A Field	Cursor Address Area
XFC8-XFCF	8 words	monitor unit 2		
XFD-XFD7	8 words	monitor unit 3		
XFD8-XFDF	8 words	monitor unit 4		
XFE0-XFE7	8 words	monitor unit 5		
XFE8-XFEF	8 words	monitor unit 6		
XFF0-XFF7	8 words	monitor unit 7		
XFF8	1 word	monitor unit 1	B Field	
XFF9	1 word	monitor unit 2		
XFFA	1 word	monitor unit 3		
XFFB	1 word	monitor unit 4		
XFFC	1 word	monitor unit 5		
XFFD	1 word	monitor unit 6		
XFFE	1 word	monitor unit 7		
XFFF	1 word	unused		

Figure 4-11. SDU Memory Map

NORMAL CHANNEL CONTROL BITS

Figure 4-12 shows the normal channel bits associated with the SDU coupler, SDU, and keyboards. Each of these bits is described on the following pages in Tables 4-4 and 4-5.

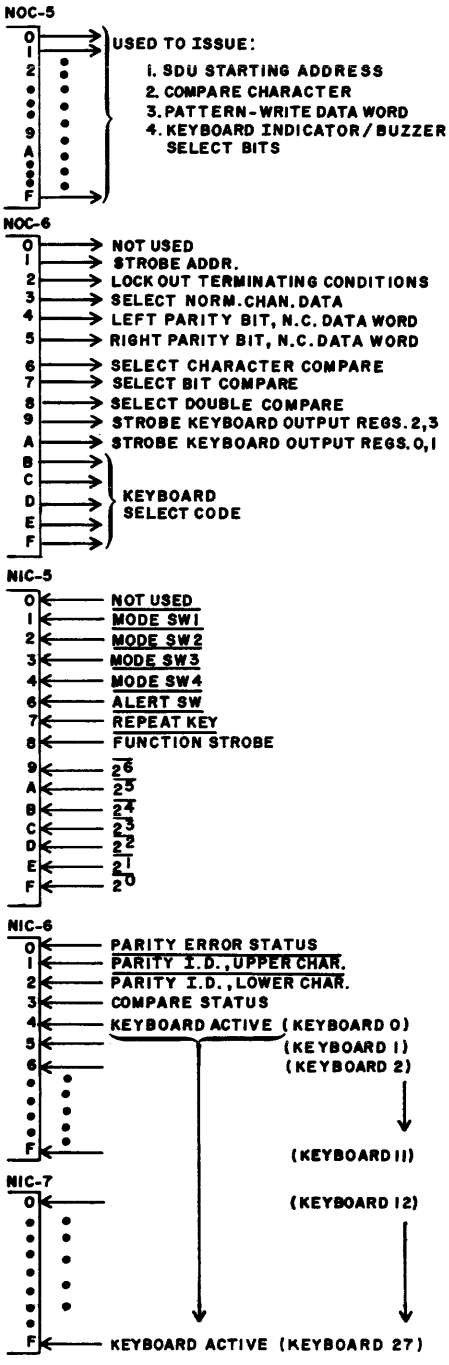


Figure 4-12. SDU and SDU Coupler Normal Channel Bits

USES OF NORMAL OUTPUT CHANNEL 5

Normal output channel 5 is used to issue four different types of information. Bits on normal output channel 6 are used to identify the type of information being transmitted on NOC-5.

1. SDU starting address

   A 15 bit starting address (Figure 4-13) must be issued to the SDU via NOC-5 before the start of a block-input, block-output, or pattern-write operation. NOC-6, bit 3 (select normal channel data) must also be set to prepare the coupler to issue an address. Setting, then immediately clearing NOC-6, bit 1 (strobe address) transfers the address to the SDU.

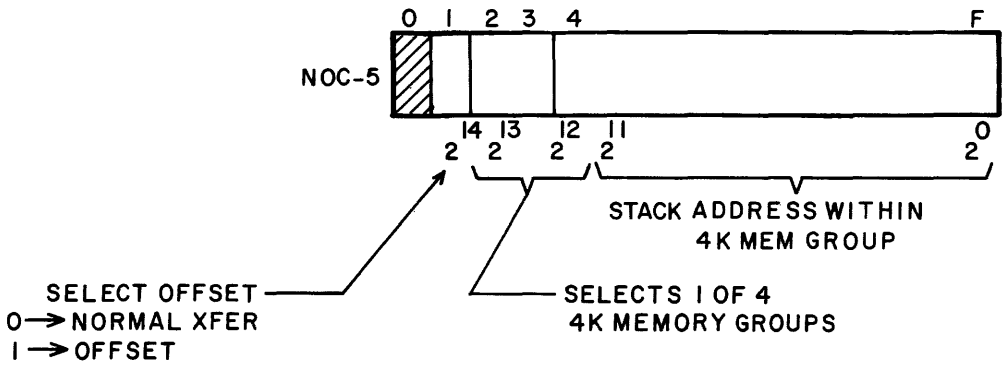


Figure 4-13. Address Format

2. Compare character

   When the character compare or double compare terminating conditions are selected, a compare character must be held in NOC-5 throughout a block-input or block-output operation. NOC-6, bit 6 (select character compare) or NOC-6, bit 8 (select double compare) must also be set. As shown in Figure 4-14, the same compare character must be repeated in the upper and lower halves of NOC-5.

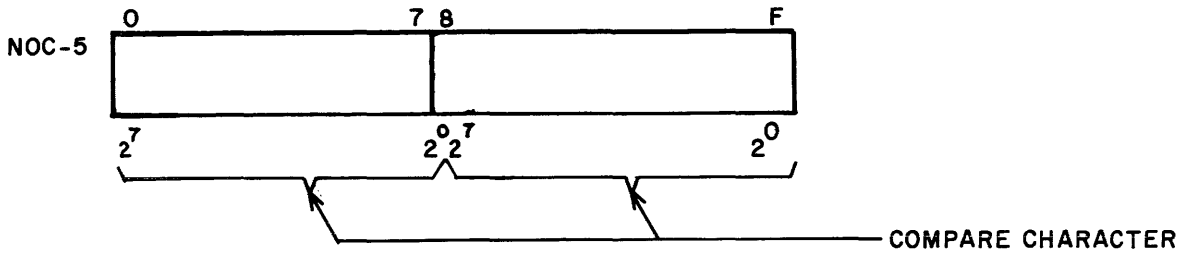


Figure 4-14. Compare Character Format

If character compare is selected, any 7-bit character can be issued on NOC-5. If double compare is selected, either the end-of-file code ($1C_{16}$) or end-of-record code ($1F_{16}$) must be placed in NOC-5. It makes no difference which of these codes is issued; if one of them is present in NOC-5, the coupler terminates a block-input or block-output operation if either code appears in the data stream.

3. Pattern - write data word

   During a pattern-write operation, the pattern word to be written repetitively in SDU memory must be held in NOC-5 throughout the operation. Also, NOC-6, bit 3 (select normal channel data) must be set throughout the operation to gate the pattern word from NOC-5 to the SDU data lines.

4. Keyboard indicator/buzzer select bits

   The bits listed in Table 4-3 are used to turn on keyboard indicator lights and alarm buzzers. One of two keyboard output register strobe bits (NOC-6,bit 9 or bit A) must be set, then cleared to transfer the select bits from NOC-5 to the keyboard output registers. Also, NOC-6,bit 3 (select normal channel data) must be set.

TABLE 4-4. NOC-6 BIT DESCRIPTIONS FOR SDU COUPLER INTERFACE

Channel	Bit	Name	Function
NOC-6	1	Strobe address	This set/clear† bit strobes the starting address on NOC-5 into SDU memory prior to a block transfer operation.
NOC-6	2	Lockout terminate	Normally, a compare hit or parity error terminates a block transfer operation. When set, this bit causes the coupler to overlook these terminating conditions. This bit is used primarily as a maintenance aid.
NOC-6	3	Select NC data	When set, this bit connects NOC-5, bits 0-F, to the SDU data lines. The normal path from the BC block transfer channel to the SDU data lines is disconnected. This bit must be set (1) when a starting address is issued to the SDU via NOC-5, (2) during a pattern-write operation, or (3) during an output operation of the keyboard output register. It must be clear during a normal output-block transfer operation.
NOC-6	4	NC data PBL (parity bit, left character)	This bit is used to add the proper parity to the left half of a 16-bit word when NOC-5 is used for data in a pattern-write operation.
NOC-6	5	NC data PBR (parity bit, right character)	This bit is used similar to that described in bit 4, above, except it is used with the right half of the 16-bit pattern word.

† A set/clear bit must be set and then immediately cleared to initiate its function.

TABLE 4-4. NOC-6 BIT DESCRIPTIONS FOR SDU COUPLER INTERFACE (Cont'd)

<table>
<tr><th>Channel</th><th>Bit</th><th>Name</th><th>Function</th></tr>
<tr><td>NOC-6</td><td>6</td><td>Select character compare</td><td>While set, this bit selects the character compare terminating condition.</td></tr>
<tr><td>NOC-6</td><td>7</td><td>Select bit compare</td><td>While set, this bit selects the bit compare terminating condition.</td></tr>
<tr><td>NOC-6</td><td>8</td><td>Select double compare</td><td>While set, this bit selects the double compare terminating condition.</td></tr>
<tr><td>NOC-6</td><td>9</td><td>Strobe keyboard output register 2, 3</td><td>Setting this bit gates NOC-5 data into the group 2 or 3 keyboard output register. Each bit in the keyboard output register controls an indicator light or buzzer on one of the keyboards.</td></tr>
<tr><td>NOC-6</td><td>A</td><td>Strobe keyboard output register 0, 1</td><td>Setting this bit gates NOC-5 data into the group 0 or 1 keyboard output register.</td></tr>
<tr><td>NOC-6</td><td>B
↓
F</td><td>Select keyboard input</td><td>(2^4)
↓
(2^0)
Bits 2^3 and 2^4 are used to select one of four groups of keyboards, and bits 2^0, 2^1, and 2^2 are used to select one of seven keyboards within a group.
<table>
<tr><th>Bit 2^4</th><th>Bit 2^3</th><th>Group selected</th><th>Bit 2^2</th><th>Bit 2^1</th><th>Bit 2^0</th><th>Keyboard selected</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>2</td></tr>
<tr><td>1</td><td>0</td><td>2</td><td>0</td><td>1</td><td>1</td><td>3</td></tr>
<tr><td>1</td><td>1</td><td>3</td><td>1</td><td>0</td><td>0</td><td>4</td></tr>
<tr><td></td><td></td><td></td><td>1</td><td>0</td><td>1</td><td>5</td></tr>
<tr><td></td><td></td><td></td><td>1</td><td>1</td><td>0</td><td>6</td></tr>
<tr><td></td><td></td><td></td><td>1</td><td>1</td><td>1</td><td>7</td></tr>
</table></td></tr>
</table>

TABLE 4-5. NIC -5, -6, AND -7 BIT DESCRIPTIONS FOR SDU COUPLER INTERFACE

Channel	Bit	Name	Function
NIC-5	2 ↓ 5	Not mode switch 1 2 3 4	These four bits, sent over four lines to the SCU, indicate one of the four mode switches on the selected keyboard that was pressed. A 0 indicates the switch is ON.
NIC-5	6	Not ALERT switch	This status bit indicates the state of the ALERT switch on the selected keyboard. A 0 indicates the switch is ON.
NIC-5	7	Not repeat key	When 0, this bit indicates that the operator is pressing the repeat key on the selected keyboard. No keyboard data accompanies the repeat bit; it is up to the software to repeat the previously typed character in the next character position in SCU memory.
NIC-5	8	Not function strobe	When a 0, this status bit indicates that bits 9 through F of NIC-5 contain a function code from the function keys of a selected keyboard rather than an ASCII-coded data character. A 1 indicates ASCII data.
NIC-5	9 ↓ F	Not keyboard data 2^6 ↓ 2^0	These input bits carry one of two types of information from the selected keyboard. 1. An ASCII-coded data character each time one of the ASCII character keys are pressed. 2. A hexadecimal function code each time one of the function keys is pressed.

STATION NORMAL CHANNEL BIT ASSIGNMENTS A

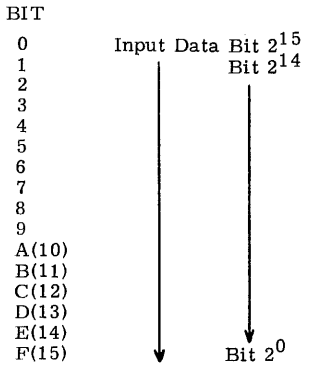
This appendix identifies the normal channel bit assignments for each STAR peripheral station. Bit assignments for channels 0 through 4 are common to all stations except for the maintenance station. Bit assignments for normal channels 5, 6, and 7 and for all channels of the maintenance station follow the listings for channel 4. In those instances where functions are not given for particular bits, the bits are unassigned. Use the index below to find the beginning page for the desired station.

Refer to appendix B for a listing of bit assignments arranged by interface.

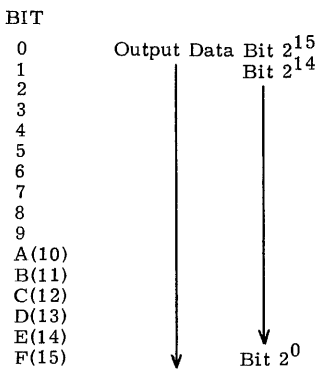
COMMON NORMAL CHANNEL BIT ASSIGNMENTS

The following bit assignments for channels 0 through 4 are common to all stations except for the maintenance control units.

INPUT CHANNEL 0
Microdrum



OUTPUT CHANNEL 0
Microdrum



COMMON NORMAL CHANNEL BIT ASSIGNMENTS

INPUT CHANNEL 1
Keyboard

BIT	
0	Control Panel Lockout
1	Character Code 2^6
2	↓
3	↓
4	↓
5	↓
6	↓
7	2^0
8	Alarm Disable (alert)
9	Repeat Key
A(10)	Keyboard Lockout Switch
B(11)	Data Strobe
C(12)	Mode 1
D(13)	Mode 2
E(14)	Mode 3
F(15)	Mode 4

OUTPUT CHANNEL 1
Microdrum

BIT	
0	Data Mode
1	Write Request
2	Read Request
3	Sector Address 2^4
4	2^3
5	2^2
6	2^1
7	2^0
8	Character Mark
9	Word Address 2^6
A(10)	2^5
B(11)	2^4
C(12)	2^3
D(13)	2^2
E(14)	2^1
F(15)	2^0

INPUT CHANNEL 2
Coupler A/Microdrum

BIT	
0	Coupler Time-out Status
1	Parity Error Fault Status
2	Read Parity Error Status
3	Illegal Status
4	Suspend Status
5	Invalid Status
6	Fault Status
7	Channel Busy Status
8	Coupler Ready Status
9	
A(10)	
B(11)	Sector Readout 2^4
C(12)	2^3
D(13)	2^2
E(14)	2^1
F(15)	2^0

OUTPUT CHANNEL 2
Coupler A

BIT	
0	Initiate Functions
1	Function 2^2 B0
2	Function 2^1 B1
3	Function 2^0 B2
4	Interrupt
5	Clear Fault
6	Disable Parity Check
7	
8	
9	Coupler Select 2^1
A(10)	Coupler Select 2^0
B(11)	
C(12)	
D(13)	
E(14)	
F(15)	

COMMON NORMAL CHANNEL BIT ASSIGNMENTS

INPUT CHANNEL 3
Scanner High Priority

BIT	
0	Microdrum Busy
1	Real-Time Strobe
2	Flag Coupler A
3	Flag Coupler B
4	
5	
6	
7	
8	
9	
A(10)	
B(11)	
C(12)	
D(13)	
E(14)	
F(15)	

OUTPUT CHANNEL 3
Microdrum/Keyboard

BIT	
0	Checksum Mode
1	
2	
3	
4	
5	Deadman Strobe
6	Alert Indicator
7	Buzzer
8	Lockout Keyboard
9	Compare Lockout (Drum)
A(10)	Head Address 2^5
B(11)	2^4
C(12)	2^3
D(13)	2^2
E(14)	2^1
F(15)	2^0

INPUT CHANNEL 4
Coupler B

BIT	
0	Coupler Time-out Status
1	Parity Error Fault Status
2	Read Parity Error Status
3	Illegal Status
4	Suspend Status
5	Invalid Status
6	Fault Status
7	Channel Busy Status
8	Coupler Ready Status
9	Coupler Software Flag 1
A(10)	Coupler Software Flag 2
B(11)	
C(12)	
D(13)	
E(14)	
F(15)	

OUTPUT CHANNEL 4
Coupler B

BIT	
0	Initiate Functions
1	Function 2^2
2	Function 2^1
3	Function 2^0
4	Interrupt
5	Clear Fault
6	Disable Parity Check
7	
8	
9	Coupler Software Flag 1
A(10)	Coupler Software Flag 2
B(11)	
C(12)	
D(13)	
E(14)	
F(15)	

PAGING (DRUM) STATION
OUTPUT CHANNEL 6

Bit 0

SAC-1	SBU Starting Address
7000-0	SBU Starting Address
7000-1	SBU Starting Address
Index Compare	SBU Starting Address

Bit 1

SAC-1	SBU Terminating Address
7000-0	SBU Terminating Address
7000-1	SBU Terminating Address
Index Compare	SBU Terminating Address

Bit 2

SAC-1	Function
7000-0	Function
7000-1	Function
Index Compare	Load Request Register

Bit 3

SAC-1	Program Clear
7000-0	Program Clear
7000-1	Program Clear
Index Compare	Program Clear

Bit 4

SAC-1	Request
7000-0	Disable Error
7000-1	Disable Error
Index Compare	Start Search

Bit 5

SAC-1	Accept
7000-0	
7000-1	
Index Compare	Write Buffers

Bit 6

SAC-1	Select Status
7000-0	
7000-1	
Index Compare	Search Backward

Bit 7

SAC-1	Set Interrupt
7000-0	
7000-1	
Index Compare	One Request

Bit 8

Index Compare	NOC-7 Select
	Norm Chan 6, Bit 8 Fanout

Bit 9

Index Compare	NOC-5 Select
	Norm Chan 6, Bit 9 Fanout

Bit A

Index Compare	NOC-6 Select
	Norm Chan 6, Bit A Fanout

Bit B

Scanner Select
Norm Chan 6, Bit B Fanout

Bit C

Connect Code 2^3
Norm Chan 6, Bit C Fanout

Bit D

Connect Code 2^2
Norm Chan 6, Bit D Fanout

Bit E

Connect Code 2^1
Norm Chan 6, Bit E Fanout

Bit F

Connect Code 2^0
Norm Chan 6, Bit F Fanout

PAGING (DRUM) STATION
INPUT CHANNEL 7

Bit 0		
SAC-1	SCU Data/RA Bit 2^{15}†	
7000-0		
7000-1		
Compare		
Bit 1		
SAC-1	SCU Data/RA Bit 2^{14}	
7000-0		
7000-1		
Compare		
Bit 2		
SAC-1	SCU Data/RA Bit 2^{13}	
7000-0		
7000-1		
Compare		
Bit 3		
SAC-1	SCU Data/RA Bit 2^{12}	
7000-0		
7000-1		
Compare		
Bit 4		
SAC-1	SCU Data/RA Bit 2^{11}	
7000-0		
7000-1		
Compare		
Bit 5		
SAC-1	SCU Data/RA Bit 2^{10}†	
7000-0		
7000-1		
Compare		
Bit 6		
SAC-1	SCU Data/RA Bit 2^{9}	
7000-0		
7000-1		
Compare	Delete Key Count Bit 2^{9}	
Bit 7		
SAC-1	SCU Data/RA Bit 2^{8}	
7000-0		
7000-1		
Compare	Delete Key Count Bit 2^{8}	
Bit 8		
SAC-1	SCU Data/RA Bit 2^{7}	
7000-0		
7000-1		
Compare	Delete Key Count Bit 2^{7}	
Bit 9		
SAC-1	SCU Data/RA Bit 2^{6}	
7000-0		
7000-1		
Compare	Delete Key Count Bit 2^{6}	
Bit A		
SAC-1	SCU Data/RA Bit 2^{5}	
7000-0		
7000-1		
Compare	Delete Key Count Bit 2^{5}	
Bit B		
SAC-1	SCU Data/RA Bit 2^{4}†	
7000-0		
7000-1		
Compare	Delete Key Count Bit 2^{4}	
Bit C		
SAC-1	SCU Data/RA Bit 2^{3}	
7000-0		
7000-1		
Compare	Delete Key Count Bit 2^{3}	
Bit D		
SAC-1	SCU Data/RA Bit 2^{2}	
7000-0		
7000-1		
Compare	Delete Key Count Bit 2^{2}	
Bit E		
SAC-1	SCU Data/RA Bit 2^{1}	
7000-0		
7000-1		
Compare	Delete Key Count Bit 2^{1}	
Bit F		
SAC-1	SCU Data/RA Bit 2^{0}	
7000-0		
7000-1		
Compare	Delete Key Count Bit 2^{0}	

†RA = Return address

HCD STATION NORMAL CHANNEL BIT ASSIGNMENTS

HCD STATION
INPUT CHANNEL 5

Bit 0	
SAC-1	SBU Parity Error
SAC-2	SBU Parity Error
7000-0	SBU Parity Error
7000-1	SBU Parity Error

Bit 1	
SAC-1	$\overline{\text{Bank Counter}}\ 2^2$
SAC-2	$\overline{\text{Bank Counter}}\ 2^2$
7000-0	$\overline{\text{Bank Counter}}\ 2^2$
7000-1	$\overline{\text{Bank Counter}}\ 2^2$

Bit 2	
SAC-1	$\overline{\text{Bank Counter}}\ 2^1$
SAC-2	$\overline{\text{Bank Counter}}\ 2^1$
7000-0	$\overline{\text{Bank Counter}}\ 2^1$
7000-1	$\overline{\text{Bank Counter}}\ 2^1$

Bit 3	
SAC-1	$\overline{\text{Bank Counter}}\ 2^0$
SAC-2	$\overline{\text{Bank Counter}}\ 2^0$
7000-0	$\overline{\text{Bank Counter}}\ 2^0$
7000-1	$\overline{\text{Bank Counter}}\ 2^0$

Bit 4	
SAC-1	Transmission Parity Error
SAC-2	Transmission Parity Error
7000-0	Disk Status 2^{11}
7000-1	Disk Status 2^{11}

Bit 5	
SAC-1	SAC Parity Error
SAC-2	SAC Parity Error
7000-0	Disk Status 2^{10}
7000-1	Disk Status 2^{10}

Bit 6	
SAC-1	Illegal
SAC-2	Illegal
7000-0	Disk Status 2^9
7000-1	Disk Status 2^9

Bit 7	
SAC-1	Busy
SAC-2	Busy
7000-0	Disk Status 2^8
7000-1	Disk Status 2^8

Bit 8	
SAC-1	Term. Address Compare
SAC-2	Term. Address Compare
7000-0	Disk Status 2^7
7000-1	Disk Status 2^7

Bit 9	
SAC-1	First Rank Full
SAC-2	First Rank Full
7000-0	Disk Status 2^6
7000-1	Disk Status 2^6

Bit A	
SAC-1	Last Rank Full
SAC-2	Last Rank Full
7000-0	Disk Status 2^5
7000-1	Disk Status 2^5

Bit B	
SAC-1	Control Function 2^1
SAC-2	Control Function 2^1
7000-0	Disk Status 2^4
7000-1	Disk Status 2^4

Bit C	
SAC-1	Control Function 2^0
SAC-2	Control Function 2^0
7000-0	Disk Status 2^3
7000-1	Disk Status 2^3

Bit D	
SAC-1	Control Function Strobe
SAC-2	Control Function Strobe
7000-0	Disk Status 2^2
7000-1	Disk Status 2^2

Bit E	
SAC-1	NU
SAC-2	NU
7000-0	Disk Status 2^1
7000-1	Disk Status 2^1

Bit F	
SAC-1	NU
SAC-2	NU
7000-0	Disk Status 2^0
7000-1	Disk Status 2^0

HCD STATION
OUTPUT CHANNEL 5

Bit 0

SAC-1	SCU Addr/Data Bit 2^{15}
SAC-2	SCU Addr/Data Bit 2^{15}
7000-0	EDS/SDS/Software Bit 2^{2} †
Ch. 5 Fanout	

Bit 1

SAC-1	SBU TA/SCU Addr/Data Bit 2^{14}
SAC-2	SBU TA/SCU Addr/Data Bit 2^{14}
7000-0	SBU SA/TA Bit 2^{14}/Data Sequence
Ch. 5 Fanout	

Bit 2

SAC-1	SBU TA/SCU Addr/Data Bit 2^{13}
SAC-2	SBU TA/SCU Addr/Data Bit 2^{13}
7000-0	SBU SA/TA Bit 2^{13}/Software Bit 2^{1}
Ch. 5 Fanout	

Bit 3

SAC-1	SBU TA/SCU Addr/Data Bit 2^{12}
SAC-2	SBU TA/SCU Addr/Data Bit 2^{12}
7000-0	SBU SA/TA Bit 2^{12}/Software Bit 2^{0}
Ch. 5 Fanout	

Bit 4

SAC-1	SBU TA/SCU Addr/Data Bit 2^{11}
SAC-2	SBU TA/SCU Addr/Data Bit 2^{11}
7000-0	SBU SA/TA/Function Bit 2^{11}
Ch. 5 Fanout	

Bit 5

SAC-1	SBU TA/SCU Addr/Data Bit 2^{10}
SAC-2	SBU TA/SCU Addr/Data Bit 2^{10}
7000-0	SBU SA/TA/Function Bit 2^{10}
Ch. 5 Fanout	

Bit 6

SAC-1	SBU TA/SCU Addr/Data Bit 2^{9}
SAC-2	SBU TA/SCU Addr/Data Bit 2^{9}
7000-0	SBU SA/TA/Function Bit 2^{9}
Ch. 5 Fanout	

Bit 7

SAC-1	SBU TA/SCU Addr/Data Bit 2^{8}
SAC-2	SBU TA/SCU Addr/Data Bit 2^{8}
7000-0	SBU SA/TA Function Bit 2^{8}
Ch. 5 Fanout	

Bit 8

SAC-1	SBU TA/SCU Addr/Data Bit 2^{7}
SAC-2	SBU TA/SCU Addr/Data Bit 2^{7}
7000-0	SBU SA/TA/Function Bit 2^{7}
Ch. 5 Fanout	

Bit 9

SAC-1	SBU TA/SCU Addr/Data Bit 2^{6}
SAC-2	SBU TA/SCU Addr/Data Bit 2^{6}
7000-0	SBU SA/TA/Function Bit 2^{6}
Ch. 5 Fanout	

Bit A

SAC-1	SBU TA/SCU Addr/Data Bit 2^{5}
SAC-2	SBU TA/SCU Addr/Data Bit 2^{5}
7000-0	SBU SA/TA/Function Bit 2^{5}
Ch. 5 Fanout	

Bit B

SAC-1	SBU TA/SCU Addr/Data Bit 2^{4}
SAC-2	SBU TA/SCU Addr/Data Bit 2^{4}
7000-0	SBU SA/TA/Function Bit 2^{4}
Ch. 5 Fanout	

Bit C

SAC-1	SBU TA/SCU Addr/Data Bit 2^{3}
SAC-2	SBU TA/SCU Addr/Data Bit 2^{3}
7000-0	SBU SA/TA/Function Bit 2^{3}
Ch. 5 Fanout	

Bit D

SAC-1	SBU TA/SCU Addr/Data Bit 2^{2}
SAC-2	SBU TA/SCU Addr/Data Bit 2^{2}
7000-0	SBU SA/TA/Function Bit 2^{2}
Ch. 5 Fanout	

Bit E

SAC-1	SBU TA/SCU Addr/Data Bit 2^{1}
SAC-2	SBU TA/SCU Addr/Data Bit 2^{1}
7000-0	SBU SA/TA/Function Bit 2^{1}
Ch. 5 Fanout	

Bit F

SAC-1	SBU TA/SCU Addr/Data Bit 2^{0}
SAC-2	SBU TA/SCU Addr/Data Bit 2^{0}
7000-0	SBU SA/TA/Function Bit 2^{0}
Ch. 5 Fanout	

†EDS/SDS = End data sequence/start data sequence

HCD STATION
INPUT CHANNEL 6

Bit 0

Scanner	7000-0 Disk On-Cylinder Interrupt
SCU Int.	NU
Ch. 5 Fanin	Bit 0
Ch. 7 Fanin	Bit 0

Bit 1

Scanner	7000-0 Disk Error
SCU Int.	NU
Ch. 5 Fanin	Bit 1
Ch. 7 Fanin	Bit 1

Bit 2

Scanner	7000-0 Disk EOT Bit 2^1*
SCU Int.	NU
Ch. 5 Fanin	Bit 2
Ch. 7 Fanin	Bit 2

Bit 3

Scanner	7000-0 Disk EOT 2^0
SCU Int.	NU
Ch. 5 Fanin	Bit 3
Ch. 7 Fanin	Bit 3

Bit 4

Scanner	7000-1 Disk On-Cylinder Interrupt
SCU Int.	NU
Ch. 5 Fanin	Bit 4
Ch. 7 Fanin	Bit 4

Bit 5

Scanner	7000-1 Disk Error
SCU Int	$\overline{\text{Bank Counter } 2^2}$
Ch. 5 Fanin	Bit 5
Ch. 7 Fanin	Bit 5

Bit 6

Scanner	7000-1 Disk EOT 2^1
SCU Int	$\overline{\text{Bank Counter } 2^1}$
Ch. 5 Fanin	Bit 6
Ch. 7 Fanin	Bit 6

Bit 7

Scanner	7000-1 Disk EOT 2^0
SCU Int	$\overline{\text{Bank Counter } 2^0}$
Ch. 5 Fanin	Bit 7
Ch. 7 Fanin	Bit 7

Bit 8

Scanner	SAC-1 Not Busy
Ch. 6 Fanin	Bit 8
Ch. 5 Fanin	Bit 8
Ch. 7 Fanin	Bit 8

Bit 9

Scanner	SAC-2 Not Busy
Ch. 6 Fanin	Bit 9
Ch. 5 Fanin	Bit 9
Ch. 7 Fanin	Bit 9

Bit A

Scanner	SAC-1 Flag
Ch. 6 Fanin	Bit A
Ch. 5 Fanin	Bit A
Ch. 7 Fanin	Bit A

Bit B

Scanner	SAC-2 Flag
Ch. 6 Fanin	Bit B
Ch. 5 Fanin	Bit B
Ch. 7 Fanin	Bit B

Bit C

Scanner	NU
Ch. 6 Fanin	Bit C
Ch. 5 Fanin	Bit C
Ch. 7 Fanin	Bit C

Bit D

Scanner	NU
Ch. 6 Fanin	Bit D
Ch. 5 Fanin	Bit D
Ch. 7 Fanin	Bit D

Bit E

Scanner	NU
Ch. 6 Fanin	Bit E
Ch. 5 Fanin	Bit E
Ch. 7 Fanin	Bit E

Bit F

Scanner	NU
Ch. 6 Fanin	Bit F
Ch. 5 Fanin	Bit F
Ch. 7 Fanin	Bit F

*EOT = End of Transfer

HCD STATION
OUTPUT CHANNEL 6

Bit 0

SAC-1	SBU Starting Address
SAC-2	SBU Starting Address
7000-0	SBU Starting Address
7000-1	SBU Starting Address

Bit 1

SAC-1	SBU Term. Address
SAC-2	SBU Term. Address
7000-0	SBU Term. Address
7000-1	SBU Term. Address

Bit 2

SAC-1	Function
SAC-2	Function
7000-0	Function
7000-1	Function

Bit 3

SAC-1	Program Clear
SAC-2	Program Clear
7000-0	Program Clear
7000-1	Program Clear

Bit 4

SAC-1	Request
SAC-2	Request
7000-0	Disable Error
7000-1	Disable Error

Bit 5

SAC-1	Accept
SAC-2	Accept
7000-0	NU
7000-1	NU

Bit 6

SAC-1	Select Status
SAC-2	Select Status
7000-0	NU
7000-1	NU

Bit 7

SAC-1	Set Interrupt
SAC-2	Set Interrupt
7000-0	NU
7000-1	NU

Bit 8

SAC-1	NU
SAC-2	NU
7000-0	NOC-7 Select
7000-1	NOC-7 Select
Ch. 6 Fanout	Bit 8

Bit 9

SAC-1	NU
SAC-2	NU
7000-0	NOC-5 Select
7000-1	NOC-5 Select
Ch. 6 Fanout	Bit 9

Bit A

SAC-1	NU
SAC-2	NU
7000-0	NOC-6 Select
7000-1	NOC-6 Select
Ch. 6 Fanout	Bit A

Bit B

SAC-1	Scanner Select
SAC-2	Scanner Select
7000-0	Scanner Select
7000-1	Scanner Select
Ch. 6 Fanout	Bit B

Bit C

	Connect Code 2^3
	NC Bit C Fanout

Bit D

	Connect Code 2^2
	NC Bit D Fanout

Bit E

	Connect Code 2^1
	NC Bit E Fanout

Bit F

	Connect Code 2^0
	NC Bit F Fanout

†NC = Normal Channel

HCD STATION
INPUT CHANNEL 7

Bit 0		
	SAC-1	SCU Data 2^{15}
	SAC-2	SCU Data 2^{15}
	7000-0	Return Function 2^{2}
	7000-1	Return Function 2^{2}
Bit 1		
	SAC-1	SCU Data/SBU RA 2^{14} †
	SAC-2	SCU Data/SBU RA 2^{14}
	7000-0	NU
	7000-1	NU
Bit 2		
	SAC-1	SCU Data/SBU RA 2^{13}
	SAC-2	SCU Data/SBU RA 2^{13}
	7000-0	Return Function 2^{1}
	7000-1	Return Function 2^{1}
Bit 3		
	SAC-1	SCU Data/SBU RA 2^{12}
	SAC-2	SCU Data/SBU RA 2^{12}
	7000-0	Return Function 2^{0}
	7000-1	Return Function 2^{0}
Bit 4		
	SAC-1	SCU Data/SBU RA 2^{11}
	SAC-2	SCU Data/SBU RA 2^{11}
	7000-0	NU
	7000-1	NU
Bit 5		
	SAC-1	SCU Data/SBU RA 2^{10}
	SAC-2	SCU Data/SBU RA 2^{10}
	7000-0	NU
	7000-1	NU
Bit 6		
	SAC-1	SCU Data/SBU RA 2^{9}
	SAC-2	SCU Data/SBU RA 2^{9}
	7000-0	NU
	7000-1	NU
Bit 7		
	SAC-1	SCU Data/SBU RA 2^{8}
	SAC-2	SCU Data/SBU RA 2^{8}
	7000-0	NU
	7000-1	NU
Bit 8		
	SAC-1	SCU Data/SBU RA 2^{7}
	SAC-2	SCU Data/SBU RA 2^{7}
	7000-0	
	7000-1	
Bit 9		
	SAC-1	SCU Data/SBU RA 2^{6}
	SAC-2	SCU Data/SBU RA 2^{6}
	7000-0	NU
	7000-1	NU
Bit A		
	SAC-1	SCU Data/SBU RA 2^{5}
	SAC-2	SCU Data/SBU RA 2^{5}
	7000-0	NU
	7000-1	NU
Bit B		
	SAC-1	SCU Data/SBU RA 2^{4}
	SAC-2	SCU Data/SBU RA 2^{4}
	7000-0	NU
	7000-1	NU
Bit C		
	SAC-1	SCU Data/SBU RA 2^{3}
	SAC-2	SCU Data/SBU RA 2^{3}
	7000-0	NU
	7000-1	NU
Bit D		
	SAC-1	SCU Data/SBU RA 2^{2}
	SAC-2	SCU Data/SBU RA 2^{2}
	7000-0	NU
	7000-1	NU
Bit E		
	SAC-1	SCU Data/SBU RA 2^{1}
	SAC-2	SCU Data/SBU RA 2^{1}
	7000-0	NU
	7000-1	NU
Bit F		
	SAC-1	SCU Data/SBU RA 2^{0}
	SAC-2	SCU Data/SBU RA 2^{0}
	7000-0	NU
	7000-1	NU

†RA = Return address

HCD STATION
OUTPUT CHANNEL 7

Bit 0

SAC-1	NU
SAC-2	NU
7000-1	EDS/SDS/Software Bit 2^2 †
Ch. 7 Fanout	Bit 2^{15}

Bit 1

SAC-1	SBU SA Bit 2^{14}
SAC-2	SBU SA Bit 2^{14}
7000-1	SBU SA/TA Bit 2^{14}/Data Sequence
Ch. 7 Fanout	Bit 2^{14}

Bit 2

SAC-1	SBU SA Bit 2^{13}
SAC-2	SBU SA Bit 2^{13}
7000-1	SBU SA/TA Bit 2^{13}/Software Bit 2^1
Ch. 7 Fanout	Bit 2^{13}

Bit 3

SAC-1	SBU SA Bit 2^{12}
SAC-2	SBU SA Bit 2^{12}
7000-1	SBU SA/TA Bit 2^{12}/Software Bit 2^0
Ch. 7 Fanout	Bit 2^{12}

Bit 4

SAC-1	SBU SA Bit 2^{11}
SAC-2	SBU SA Bit 2^{11}
7000-1	SBU SA/TA/Func Bit 2^{11}
Ch. 7 Fanout	Bit 2^{11}

Bit 5

SAC-1	SBU SA Bit 2^{10}
SAC-2	SBU SA Bit 2^{10}
7000-1	SBU SA/TA/Func Bit 2^{10}
Ch. 7 Fanout	Bit 2^{10}

Bit 6

SAC-1	SBU SA Bit 2^9
SAC-2	SBU SA Bit 2^9
7000-1	SBU SA/TA/Func Bit 2^9
Ch. 7 Fanout	Bit 2^9

Bit 7

SAC-1	Clear P.E./SBU SA Bit 2^8
SAC-2	Clear P.E./SBU SA Bit 2^8
7000-1	SBU SA/TA/Func Bit 2^8
Ch. 7 Fanout	Bit 2^8

Bit 8

SAC-1	Clear Illegal/SBU SA Bit 2^7
SAC-2	Clear Illegal/SBU SA Bit 2^7
7000-1	SBU SA/TA/Func Bit 2^7
Ch. 7 Fanout	Bit 2^7

Bit 9

SAC-1	Clear Cont Func/SBU SA Bit 2^6
SAC-2	Clear Cont Func/SBU SA Bit 2^6
7000-1	SBU SA/TA/Func Bit 2^6
Ch. 7 Fanout	Bit 2^6

Bit A

SAC-1	M.C./SBU SA Bit 2^5
SAC-2	SA/M.C./SBU SA Bit 2^5
7000-1	SBU SA/TA/Func Bit 2^5
Ch. 7 Fanout	Bit 2^5

Bit B

SAC-1	SBU SA Bit 2^4
SAC-2	SBU SA Bit 2^4
7000-1	SBU SA/TA/Func Bit 2^4
Ch. 7 Fanout	Bit 2^4

Bit C

SAC-1	Select SAC + $\overline{\text{SCU}}$/SBU SA Bit 2^3
SAC-2	Select SAC + $\overline{\text{SCU}}$/SBU SA Bit 2^3
7000-1	SBU SA/TA/Func Bit 2^3
Ch. 7 Fanout	Bit 2^3

Bit D

SAC-1	Func Code/SBU SA Bit 2^2
SAC-2	Func Code/SBU SA Bit 2^2
7000-1	SBU SA/TA/Func Bit 2^2
Ch. 7 Fanout	Bit 2^2

Bit E

SAC-1	Func Code/SBU SA Bit 2^1
SAC-2	Func Code/SBU SA Bit 2^1
7000-1	SBU SA/TA/Func Bit 2^1
Ch. 7 Fanout	Bit 2^1

Bit F

SAC-1	Func Code/SBU SA Bit 2^0
SAC-2	Func Code/SBU SA Bit 2^0
7000-1	SBU SA/TA/Func Bit 2^0
Ch. 7 Fanout	Bit 2^0

† EDS/SDS = End data sequence/start data sequence

844 SERVICE STATION
OUTPUT CHANNEL 5

Bit 0		
	SAC-1	SBU TA/SCU Addr/Data Bit 2^{15}†
	SAC-2	SBU TA/SCU Addr/Data Bit 2^{15}
Bit 1		
	SAC-1	SBU TA/SCU Addr/Data Bit 2^{14}
	SAC-2	SBU TA/SCU Addr/Data Bit 2^{14}
Bit 2		
	SAC-1	SBU TA/SCU Addr/Data Bit 2^{13}
	SAC-2	SBU TA/SCU Addr/Data Bit 2^{13}
Bit 3		
	SAC-1	SBU TA/SCU Addr/Data Bit 2^{12}
	SAC-2	SBU TA/SCU Addr/Data Bit 2^{12}
Bit 4		
	SAC-1	SBU TA/SCU Addr/Data Bit 2^{11}
	SAC-2	SBU TA/SCU Addr/Data Bit 2^{11}
Bit 5		
	SAC-1	SBU TA/SCU Addr/Data Bit 2^{10}
	SAC-2	SBU TA/SCU Addr/Data Bit 2^{10}
Bit 6		
	SAC-1	SBU TA/SCU Addr/Data Bit 2^{9}
	SAC-2	SBU TA/SCU Addr/Data Bit 2^{9}
Bit 7		
	SAC-1	SBU TA/SCU Addr/Data Bit 2^{8}
	SAC-2	SBU TA/SCU Addr/Data Bit 2^{8}
Bit 8		
	SAC-1	SBU TA/SCU Addr/Data Bit 2^{7}
	SAC-2	SBU TA/SCU Addr/Data Bit 2^{7}
Bit 9		
	SAC-1	SBU TA/SCU Addr/Data Bit 2^{6}
	SAC-2	SBU TA/SCU Addr/Data Bit 2^{6}
Bit A		
	SAC-1	SBU TA/SCU Addr/Data Bit 2^{5}
	SAC-2	SBU TA/SCU Addr/Data Bit 2^{5}
Bit B		
	SAC-1	SBU TA/SCU Addr/Data Bit 2^{4}
	SAC-2	SBU TA/SCU Addr/Data Bit 2^{4}
Bit C		
	SAC-1	SBU TA/SCU Addr/Data Bit 2^{3}
	SAC-2	SBU TA/SCU Addr/Data Bit 2^{3}
Bit D		
	SAC-1	SBU TA/SCU Addr/Data Bit 2^{2}
	SAC-2	SBU TA/SCU Addr/Data Bit 2^{2}
Bit E		
	SAC-1	SBU TA/SCU Addr/Data Bit 2^{1}
	SAC-2	SBU TA/SCU Addr/Data Bit 2^{1}
Bit F		
	SAC-1	SBU TA/SCU Addr/Data Bit 2^{0}
	SAC-2	SBU TA/SCU Addr/Data Bit 2^{0}

† TA = Terminating Address

844 SERVICE STATION
INPUT CHANNEL 6

Bit 0		
Scanner	Memory P.E. I/O Channel	
844	Unit Busy	
Bit 1		
Scanner	NU	
844	Unit 1 Selected	
Bit 2		
Scanner	SAC-1 Not Busy	
844	Unit 2 Selected	
Bit 3		
Scanner	SAC-2 Not Busy	
844	Unit 3 Selected	
Bit 4		
Scanner	SAC-1 Flag	
844		
Bit 5		
Scanner	SAC-2 Flag	
844		
Bit 6		
Scanner	NU	
844		
Bit 7		
Scanner	NU	
844		
Bit 8		
Scanner	I/O Interrupt Channel 1	
844		
Bit 9		
Scanner	I/O Interrupt Channel 2	
844		
Bit A		
Scanner	I/O Interrupt Channel 3	
844	Read Error	
Bit B		
Scanner	I/O Interrupt Channel 4	
844	Tag BCC Error*	
Bit C		
Scanner	NU	
844	Timing Chain	
Bit D		
Scanner	NU	
844	SBU $\overline{\text{Bank Counter}}$ 2^2	
Bit E		
Scanner	NU	
844	SBU $\overline{\text{Bank Counter}}$ 2^1	
Bit F		
Scanner	NU	
844	SBU $\overline{\text{Bank Counter}}$ 2^0	

*BCC = Block Check Code

844 SERVICE STATION
OUTPUT CHANNEL 6

Bit 0		
	SAC-1	SBU Starting Address
	SAC-2	SBU Starting Address
	STAR A	
Bit 1		
	SAC-1	SBU Terminating Address
	SAC-2	SBU Terminating Address
	STAR A	
Bit 2		
	SAC-1	Function
	SAC-2	Function
	STAR A	
Bit 3		
	SAC-1	Program Clear
	SAC-2	Program Clear
	STAR A	
Bit 4		
	SAC-1	Request
	SAC-2	Request
	STAR A	I/O Chan 4 Select
Bit 5		
	SAC-1	Accept
	SAC-2	Accept
	STAR A	I/O Chan 3 Select
Bit 6		
	SAC-1	Select Status
	SAC-2	Select Status
	STAR A	I/O Chan 2 Select
Bit 7		
	SAC-1	Set Interrupt
	SAC-2	Set Interrupt
	844	Load SBU Address
	STAR A	I/O Chan 1 Select
Bit 8		
	844	Release
	STAR A	Select SCU Coupler
Bit 9		
	844	Function
Bit A		
	844	Begin Transfer
Bit B		
		Scanner Select
Bit C		
	All Interfaces	Connect Code 2^3
Bit D		
	All Interfaces	Connect Code 2^2
Bit E		
	All Interfaces	Connect Code 2^1
Bit F		
	All Interfaces	Connect Code 2^0

844 SERVICE STATION
INPUT CHANNEL 7

Bit 0		
SAC-1	SCU Data/RA 2^{15}†	
SAC-2	SCU Data/RA 2^{15}	
844	Finished	
Bit 1		
SAC-1	SCU Data/RA 2^{14}	
SAC-2	SCU Data/RA 2^{14}	
844	Unit 1 On Sector/Seek Error	
Bit 2		
SAC-1	SCU Data/RA 2^{13}	
SAC-2	SCU Data/RA 2^{13}	
844	Unit 2 On Sector/Seek Error	
Bit 3		
SAC-1	SCU Data/RA 2^{12}	
SAC-2	SCU Data/RA 2^{12}	
844	Unit 3 On Sector/Seek Error	
Bit 4		
SAC-1	SCU Data/RA 2^{11}	
SAC-2	SCU Data/RA 2^{11}	
844	NU	
Bit 5		
SAC-1	SCU Data/RA 2^{10}	
SAC-2	SCU Data/RA 2^{10}	
844	NU	
Bit 6		
SAC-1	SCU Data/RA 2^{9}	
SAC-2	SCU Data/RA 2^{9}	
844	NU	
Bit 7		
SAC-1	SCU Data/RA 2^{8}	
SAC-2	SCU Data/RA 2^{8}	
844	NU	
Bit 8		
SAC-1	SCU Data/RA 2^{7}	
SAC-2	SCU Data/RA 2^{7}	
844	NU	
Bit 9		
SAC-1	SCU Data/RA 2^{6}	
SAC-2	SCU Data/RA 2^{6}	
844	NU	
Bit A		
SAC-1	SCU Data/RA 2^{5}	
SAC-2	SCU Data/RA 2^{5}	
844	Ready	
Bit B		
SAC-1	SCU Data/RA 2^{5}	
SAC-2	SCU Data/RA 2^{4}	
844	Transfer Error	
Bit C		
SAC-1	SCU Data/RA 2^{3}	
SAC-2	SCU Data/RA 2^{3}	
844	On Cylinder	
Bit D		
SAC-1	SCU Data/RA 2^{2}	
SAC-2	SCU Data/RA 2^{2}	
844	Seek Error	
Bit E		
SAC-1	SCU Data/RA 2^{1}	
SAC-2	SCU Data/RA 2^{1}	
844	Pack Unsafe	
Bit F		
SAC-1	SCU Data/RA 2^{0}	
SAC-2	SCU Data/RA 2^{0}	
844	Full	

†RA = Return address

844 STORAGE/MAGNETIC TAPE STATION
OUTPUT CHANNEL 5

Bit 0

SAC-1	SBU TA/SCU Addr Bit 2^{15}
SAC-2	SBU TA/SCU Addr Bit 2^{15}
3000-0	Compare Bit/Binary/Coded
3000-1	Compare Bit/Binary/Coded

Bit 1

SAC-1	SBU TA/SCU Addr Bit 2^{14}
SAC-2	SBU TA/SCU Addr Bit 2^{14}
3000-0	SBU SA/TA/TBA/Read/Write †
3000-1	SBU SA/TA/TBA/Read/Write

Bit 2

SAC-1	SBU TA/SCU Addr Bit 2^{13}
SAC-2	SBU TA/SCU Addr Bit 2^{13}
3000-0	SBU SA/TA/TBA/Connect/Function
3000-1	SBU SA/TA/TBA/Connect/Function

Bit 3

SAC-1	SBU TA/SCU Addr Bit 2^{12}
SAC-2	SBU TA/SCU Addr Bit 2^{12}
3000-0	SBU SA/TA/TBA/Odd/Even
3000-1	SBU SA/TA/TBA/Odd/Even

Bit 4

SAC-1	SBU TA/SCU Addr Bit 2^{11}
SAC-2	SBU TA/SCU Addr Bit 2^{11}
3000-0	SBU SA/TA/TBA/Fctn Code/Conn Code/Disable Request
3000-1	SBU SA/TA/TBA/Fctn Code/Conn Code/Disable Request

Bit 5

SAC-1	SBU TA/SCU Addr Bit 2^{10}
SAC-2	SBU TA/SCU Addr Bit 2^{10}
3000-0	SBU SA/TA/TBA/Fctn Code/Conn Code/Halt On Error
3000-1	SBU SA/TA/TBA/Fctn Code/Conn Code/Halt On Error

Bit 6

SAC-1	SBU TA/SCU Addr Bit 2^{9}
SAC-2	SBU TA/SCU Addr Bit 2^{9}
3000-0	SBU SA/TA/TBA/Fctn Code/Conn Code/Read Bckwrds
3000-1	SBU SA/TA/TBA/Fctn Code/Conn Code/Read Bckwrds

Bit 7

SAC-1	SBU TA/SCU Addr Bit 2^{8}
SAC-2	SBU TA/SCU Addr Bit 2^{8}
3000-0	SBU SA/TA/TBA/Fctn Code/Conn Code
3000-1	SBU SA/TA/TBA/Fctn Code/Conn Code

Bit 8

SAC-1	SBU TA/SCU Addr Bit 2^{7}
SAC-2	SBU TA/SCU Addr Bit 2^{7}
3000-0	SBU SA/TA/Fctn Code/Conn Code
3000-1	SBU SA/TA/Fctn Code/Conn Code

Bit 9

SAC-1	SBU TA/SCU Addr Bit 2^{6}
SAC-2	SBU TA/SCU Addr Bit 2^{6}
3000-0	SBU SA/TA/Fctn Code/Conn Code
3000-1	SBU SA/TA/Fctn Code/Conn Code

Bit A

SAC-1	SBU TA/SCU Addr Bit 2^{5}
SAC-2	SBU TA/SCU Addr Bit 2^{5}
3000-0	SBU SA/TA/Fctn Code/Conn Code
3000-1	SBU SA/TA/Fctn Code/Conn Code

Bit B

SAC-1	SBU TA/SCU Addr Bit 2^{4}
SAC-2	SBU TA/SCU Addr Bit 2^{4}
3000-0	SBU SA/TA/Fctn Code/Conn Code
3000-1	SBU SA/TA/Fctn Code/Conn Code

Bit C

SAC-1	SBU TA/SCU Addr Bit 2^{3}
SAC-2	SBU TA/SCU Addr Bit 2^{3}
3000-0	SBU SA/TA/Fctn Code/Conn Code
3000-1	SBU SA/TA/Fctn Code/Conn Code

Bit D

SAC-1	SBU TA/SCU Addr Bit 2^{2}
SAC-2	SBU TA/SCU Addr Bit 2^{2}
3000-0	SBU SA/TA/Fctn Code/Conn Code
3000-1	SBU SA/TA/Fctn Code/Conn Code

Bit E

SAC-1	SBU TA/SCU Addr Bit 2^{1}
SAC-2	SBU TA/SCU Addr Bit 2^{1}
3000-0	SBU SA/TA/Fctn Code/Conn Code
3000-1	SBU SA/TA/Fctn Code/Conn Code

Bit F

SAC-1	SBU TA/SCU Addr Bit 2^{0}
SAC-2	SBU TA/SCU Addr Bit 2^{0}
3000-0	SBU SA/TA/Fctn Code/Conn Code
3000-1	SBU SA/TA/Fctn Code/Conn Code

† TBA = Table Address

844 STORAGE/MAGNETIC TAPE STATION
INPUT CHANNEL 6

Bit 0		
	Scanner F	3000-0 TA Empty
	844-A	Unit Busy
	844-B	Unit Busy
	MT STAT*	Write Parity Error
Bit 1		
	Scanner F	3000-1 TA Empty
	844-A	Unit 1 Selected
	844-B	Unit 1 Selected
	MT STAT	End of Record
Bit 2		
	Scanner F	SAC-1 Flag
	844-A	Unit 2 Selected
	844-B	Unit 2 Selected
	MT STAT	Reject
Bit 3		
	Scanner F	SAC-2 Flag
	844-A	Unit 3 Selected
	844-B	Unit 3 Selected
	MT STAT	Reply
Bit 4		
	Scanner F	SAC-1 Not Busy
	844-A	Unit 4 Selected
	844-B	Unit 4 Selected
	MT STAT	Reserved
Bit 5		
	Scanner F	SAC-2 Not Busy
	844-A	Unit 5 Selected
	844-B	Unit 5 Selected
	MT STAT	Vert or Long Parity Error
Bit 6		
	Scanner F	3000-0 Response Line
	844-A	Unit 6 Selected
	844-B	Unit 6 Selected
	MT STAT	End of Operation
Bit 7		
	Scanner F	3000-0 Address Compare
	844-A	Unit 7 Selected
	844-B	Unit 7 Selected
	MT STAT	Lost Data
Bit 8		
	Scanner F	3000-1 Response Line
	844-A	Unit 8 Selected
	844-B	Unit 8 Selected
	MT STAT	800 BPI
Bit 9		
	Scanner F	3000-1 Address Compare
	844-A	Unit 9 Selected
	844-B	Unit 9 Selected
	MT STAT	556 BPI
Bit A		
	Scanner F	NU
	844-A	Read Error
	844-B	Read Error
	MT STAT	End of Tape
Bit B		
	Scanner F	NU
	844-A	Tag BCC Error†
	844-B	Tag BCC Error
	MT STAT	Load Point
Bit C		
	Scanner F	NU
	844-A	Timing Chain
	844-B	Timing Chain
	MT STAT	File Mark
Bit D		
	Scanner F	NU
	844-A	SBU $\overline{\text{Bank Counter}}\ 2^2$
	844-B	SBU $\overline{\text{Bank Counter}}\ 2^2$
	MT STAT	Write Enable
Bit E		
	Scanner F	NU
	844-A	SBU $\overline{\text{Bank Counter}}\ 2^1$
	844-B	SBU $\overline{\text{Bank Counter}}\ 2^1$
	MT STAT	Busy
Bit F		
	Scanner F	NU
	844-A	SBU $\overline{\text{Bank Counter}}\ 2^0$
	844-B	SBU $\overline{\text{Bank Counter}}\ 2^0$
	MT STAT	Ready

*MT STAT denotes magnetic tape status word 1 only.
†BCC = Block Check Code

844 STORAGE/MAGNETIC TAPE STATION
OUTPUT CHANNEL 6

Bit 0

SAC-1	SBU SA
SAC-2	SBU SA
3000-0	SBU SA
3000-1	SBU SA

Bit 1

SAC-1	SBU TA
SAC-2	SBU TA
3000-0	SBU TA
3000-1	SBU TA

Bit 2

SAC-1	Function
SAC-2	Function
3000-0	Internal Function
3000-1	Internal Function

Bit 3

SAC-1	Program Clear
SAC-2	Program Clear
3000-0	Program Clear
3000-1	Program Clear

Bit 4

SAC-1	Request (SCU Write)
SAC-2	Request (SCU Write)
3000-0	Channel Function
3000-1	Channel Function

Bit 5

SAC-1	Accept (SCU Read)
SAC-2	Accept (SCU Read)
3000-0	SBU TBA
3000-1	SBU TBA

Bit 6

SAC-1	Select Status
SAC-2	Select Status
3000-0	SBU Current Address
3000-1	SBU Current Accress

Bit 7

SAC-1	Set Interrupt
SAC-2	Set Interrupt
844-A	Load SBU Address
844-B	Load SBU Address

Bit 8

SAC-1	NU
SAC-2	NU
844-A	Release
844-B	Release

Bit 9

SAC-1	NU
SAC-2	NU
844-A	Function
844-B	Function

Bit A

SAC-1	NU
SAC-2	NU
844-A	Begin Transfer
844-B	Begin Transfer

Bit B

SAC-1	NU
SAC-2	NU
844-A	NU
844-B	NU

Bit C

All Interfaces	Connect Code 2^3

Bit D

All Interfaces	Connect Code 2^2

Bit E

All Interfaces	Connect Code 2^1

Bit F

All Interfaces	Connect Code 2^0

844 STORAGE/MAGNETIC TAPE STATION
INPUT CHANNEL 7

Bit 0		
	SAC-1	SCU Data/SBU RA Bit 2^{15}
	SAC-2	SCU Data/SBU RA Bit 2^{15}
	844-A	Finished
	844-5	Finished
Bit 1		
	SAC-1	SCU Data/SBU RA Bit 2^{14}
	SAC-2	SCU Data/SBU RA Bit 2^{14}
	844-A	Unit 1 On Sector
	844-B	Unit 1 on Sector
Bit 2		
	SAC-1	SCU Data/SBU RA Bit 2^{13}
	SAC-2	SCU Data/SBU RA Bit 2^{13}
	844-A	Unit 2 On Sector
	844-B	Unit 2 On Sector
Bit 3		
	SAC-1	SCU Data/SBU RA Bit 2^{12}
	SAC-2	SCU Data/SBU RA Bit 2^{12}
	844-A	Unit 3 On Sector
	844-B	Unit 3 On Sector
Bit 4		
	SAC-1	SCU Data/SBU RA Bit 2^{11}
	SAC-2	SCU Data/SBU RA Bit 2^{11}
	844-A	Unit 4 On Sector
	844-B	Unit 4 On Sector
Bit 5		
	SAC-1	SCU Data/SBU RA Bit 2^{10}
	SAC-2	SCU Data/SBU RA Bit 2^{10}
	844-A	Unit 5 On Sector
	844-B	Unit 5 On Sector
Bit 6		
	SAC-1	SCU Data/SBU RA Bit 2^{9}
	SAC-2	SBU Data/SBU RA Bit 2^{9}
	844-A	Unit 6 On Sector
	844-B	Unit 6 On Sector
Bit 7		
	SAC-1	SCU Data/SBU RA Bit 2^{8}
	SAC-2	SCU Data/SBU RA Bit 2^{8}
	844-A	Unit 7 On Sector
	844-B	Unit 7 On Sector
Bit 8		
	SAC-1	SCU Data/SBU RA Bit 2^{7}
	SAC-2	SCU Data/SBU RA Bit 2^{7}
	844-A	Unit 8 On Sector
	844-B	Unit 8 On Sector
Bit 9		
	SAC-1	SCU Data/SBU RA Bit 2^{6}
	SAC-2	SCU Data/SBU RA Bit 2^{6}
	844-A	Unit 9 On Sector
	844-B	Unit 9 On Sector
Bit A		
	SAC-1	SCU Data/SBU RA Bit 2^{5}
	SAC-2	SCU Data/SBU RA Bit 2^{5}
	844-A	Ready
	844-B	Ready
Bit B		
	SAC-1	SCU Data/SBU RA Bit 2^{4}
	SAC-2	SCU Data/SBU RA Bit 2^{4}
	844-A	Transfer Error
	844-B	Transfer Error
Bit C		
	SAC-1	SCU Data/SBU RA Bit 2^{3}
	SAC-2	SCU Data/SBU RA Bit 2^{3}
	844-A	On Cylinder
	844-B	On Cylinder
Bit D		
	SAC-1	SCU Data/SBU RA Bit 2^{2}
	SAC-2	SCU Data/SBU RA Bit 2^{2}
	844-A	Seek Error
	844-B	Seek Error
Bit E		
	SAC-1	SCU Data/SBU RA Bit 2^{1}
	SAC-2	SCU Data/SBU RA Bit 2^{1}
	844-A	Pack Unsafe
	844-B	Pack Unsafe
Bit F		
	SAC-1	SCU Data/SBU RA Bit 2^{0}
	SAC-2	SCU Data/SBU RA Bit 2^{0}
	844-A	Full
	844-B	Full

DISPLAY/EDIT STATION NORMAL CHANNEL BIT ASSIGNMENTS

Input Channel 5

Bit	
0	
1	
2	Not mode switch 1
3	Not mode switch 2
4	Not mode switch 3
5	Not mode switch 4
6	Not alert switch
7	Not repeat key
8	Not function strobe
9	Not keyboard data 2^6
A (10)	Not keyboard data 2^5
B (11)	Not keyboard data 2^4
C (12)	Not keyboard data 2^3
D (13)	Not keyboard data 2^2
E (14)	Not keyboard data 2^1
F (15)	Not keyboard data 2^0

Output Channel 5

Bit	
0	Not used
1	Select offset
2	Group select bit 2^1
3	Group select bit 2^0
4	SDU starting address 2^{11}
5	SDU starting address 2^{10}
6	SDU starting address 2^9
7	SDU starting address 2^8
8	SDU starting address 2^7
9	SDU starting address 2^6
A (10)	SDU starting address 2^5
B (11)	SDU starting address 2^4
C (12)	SDU starting address 2^3
D (13)	SDU starting address 2^2
E (14)	SDU starting address 2^1
F (15)	SDU starting address 2^0

Output Channel 5

Bit	
0	Compare character 2^7/SDU write data 2^{15}
1	Compare character 2^6/SDU write data 2^{14}
2	Compare character 2^5/SDU write data 2^{13}
3	Compare character 2^4/SDU write data 2^{12}
4	Compare character 2^3/SDU write data 2^{11}
5	Compare character 2^2/SDU write data 2^{10}
6	Compare character 2^1/SDU write data 2^9
7	Compare character 2^0/SDU write data 2^8
8	Compare character 2^7/SDU write data 2^7
9	Compare character 2^6/SDU write data 2^6
A	Compare character 2^5/SDU write data 2^5
B	Compare character 2^4/SDU write data 2^4
C	Compare character 2^3/SDU write data 2^3
D	Compare character 2^2/SDU write data 2^2
E	Compare character 2^1/SDU write data 2^1
F	Compare character 2^0/SDU write data 2^0

Output Channel 5

Bit	
0	Select lockout light group 0/select lockout light group 2
1	Select lockout light group 1/select lockout light group 3
2	Select alert light group 0/select alert light group 2
3	Select alert light group 1/select alert light group 3
4	Select alert alarm group 0/select alert alarm group 2
5	Select alert alarm group 1/select alert alarm group 3
6	Not used/ not used
7	Not used/ not used
8	Not used/
9	Select keyboard 1 or 8/select keyboard 15 or 22
A	Select keyboard 2 or 9/select keyboard 16 or 23
B	Select keyboard 3 or 10/select keyboard 17 or 24
C	Select keyboard 4 or 11/select keyboard 18 or 25
D	Select keyboard 5 or 12/select keyboard 19 or 26
E	Select keyboard 6 or 13/select keyboard 20 or 27
F	Select keyboard 7 or 14/select keyboard 21 or 28

Input Channel 6

Bit	
0	**Parity error status**
1	**Not Parity Bit Left**
2	**Not Parity Bit Right**
3	**Compare status**
4	Keyboard interrupt monitor 1
5	Keyboard interrupt monitor 2
6	Keyboard interrupt monitor 3
7	Keyboard interrupt monitor 4
8	Keyboard interrupt monitor 5
9	Keyboard interrupt monitor 6
A (10)	Keyboard interrupt monitor 7
B (11)	Keyboard interrupt monitor 8
C (12)	Keyboard interrupt monitor 9
D (13)	Keyboard interrupt monitor 10
E (14)	Keyboard interrupt monitor 11
F (15)	Keyboard interrupt monitor 12

Output Channel 6

Bit	
0	
1	Strobe Address
2	**Lockout terminate**
3	Select NC data
4	NC data **Parity Bit Left**
5	NC data **Parity Bit Right**
6	Select character compare
7	Select bit compare
8	Select double compare
9	Strobe keyboard output register (2, 3)
A (10)	Strobe keyboard output register (0, 1)
B (11)	Select keyboard input 2^4
C (12)	Select keyboard input 2^3
D (13)	Select keyboard input 2^2
E (14)	Select keyboard input 2^1
F (15)	Select keyboard input 2^0

Input Channel 7

Bit	
0	Keyboard interrupt monitor 13
1	Keyboard interrupt monitor 14
2	Keyboard interrupt monitor 15
3	Keyboard interrupt monitor 16
4	Keyboard interrupt monitor 17
5	Keyboard interrupt monitor 18
6	Keyboard interrupt monitor 19
7	Keyboard interrupt monitor 20
8	Keyboard interrupt monitor 21
9	Keyboard interrupt monitor 22
A (10)	Keyboard interrupt monitor 23
B (11)	Keyboard interrupt monitor 24
C (12)	Keyboard interrupt monitor 25
D (13)	Keyboard interrupt monitor 26
E (14)	Keyboard interrupt monitor 27
F (15)	Keyboard interrupt monitor 28

Output Channel 7

Bit	
0	Not used
1	Not used
2	Not used
3	Not used
4	Not used
5	Not used
6	Not used
7	Not used
8	Not used
9	Not used
A (10)	Not used
B (11)	Not used
C (12)	Not used
D (13)	Not used
E (14)	Not used
F (15)	Not used

STAR-1B SERVICE STATION
OUTPUT CHANNEL 6

Bit 0	
SAC-1	SBU starting address
SAC-2	SBU starting address
Index Compare	SBU starting address
STAR A	NU
Bit 1	
SAC-1	SBU terminating address
SAC-2	SBU terminating address
Index Compare	SBU terminating address
STAR A	Select SCU coupler
Bit 2	
SAC-1	Function
SAC-2	Function
Index Compare	Load request register
STAR A	I/O Channel 6 Select
Bit 3	
SAC-1	Program clear
SAC-2	Program clear
Index Compare	Program clear
STAR A	I/O Channel 5 Select
Bit 4	
SAC-1	Request (SCU write)
SAC-2	Request (SCU write)
Index Compare	Start search
STAR A	I/O Channel 4 Select
Bit 5	
SAC-1	Accept (SCU read)
SAC-2	Accept (SCU read)
Index Compare	Write buffers
STAR A	I/O Channel 3 Select
Bit 6	
SAC-1	Select status
SAC-2	Select status
Index Compare	Search backward
STAR A	I/O Channel 2 Select
Bit 7	
SAC-1	Set interrupt
SAC-2	Set interrupt
Index Compare	One request
STAR A	I/O Channel 1 Select

Bit 8	
SAC-1	
SAC-2	
MDD A	Begin transfer
MDD B	Begin transfer
Bit 9	
SAC-1	
SAC-2	
MDD A	Clear end page
MDD B	Clear end page
Bit A	
SAC-1	
SAC-2	
MDD A	Load address
MDD B	Load address
Bit B	
SAC-1	
SAC-2	
MDD A	Control select
MDD B	Control select
Bit C	
SAC-1	
SAC-2	
MDD A	Function
MDD B	Function
Bit D	
All Interfaces	Connect code 2^2
Bit E	
All Interfaces	Connect code 2^1
Bit F	
All Interfaces	Connect code 2^0

Bit 0

SAC-1	SCU data/SBU RA bit 2^{15}
SAC-2	SCU data/SBU RA bit 2^{15}
MDD A	Unit 0 on sector/seek error
MDD B	Unit 0 on sector/seek error

Bit 1

SAC-1	SCU data/SBU RA bit 2^{14}
SAC-2	SCU data/SBU RA bit 2^{14}
MDD A	Unit 1 on sector/seek error
MDD B	Unit 1 on sector/seek error

Bit 2

SAC-1	SCU data/SBU RA bit 2^{13}
SAC-2	SCU data/SBU RA bit 2^{13}
MDD A	Unit 2 on sector/seek error
MDD B	Unit 2 on sector/seek error

Bit 3

SAC-1	SCU data/SBU RA bit 2^{12}
SAC-2	SCU data/SBU RA bit 2^{12}
MDD A	Unit 3 on sector/seek error
MDD B	Unit 3 on sector/seek error

Bit 4

SAC-1	SCU data/SBU RA bit 2^{11}
SAC-2	SCU data/SBU RA bit 2^{11}
MDD A	Unit 4 on sector/seek error
MDD B	Unit 4 on sector/seek error

Bit 5

SAC-1	SCU data/SBU RA bit 2^{10}
SAC-2	SCU data/SBU RA bit 2^{10}
MDD A	Unit 5 on sector/seek error
MDD B	Unit 5 on sector/seek error

Bit 6

SAC-1	SCU data/SBU RA bit 2^{9}
SAC-2	SCU data/SBU RA bit 2^{9}
MDD A	Unit 6 on sector/seek error
MDD B	Unit 6 on sector/seek error

Bit 7

SAC-1	SCU data/SBU RA bit 2^{8}
SAC-2	SCU data/SBU RA bit 2^{8}
MDD A	Unit 7 on sector/seek error
MDD B	Unit 7 on sector/seek error

Bit 8

SAC-1	SCU data/SBU RA bit 2^{7}
SAC-2	SCU data/SBU RA bit 2^{7}
MDD A	Unit 8 on sector/seek error
MDD B	Unit 8 on sector/seek error

Bit 9

SAC-1	SCU data/SBU RA bit 2^{6}
SAC-2	SCU data/SBU RA bit 2^{6}
MDD A	Busy
MDD B	Busy

Bit A (10)

SAC-1	SCU data/SBU RA bit 2^{5}
SAC-2	SCU data/SBU RA bit 2^{5}
MDD A	Ready
MDD B	Ready

Bit B (11)

SAC-1	SCU data/SBU RA bit 2^{4}
SAC-2	SCU data/SBU RA bit 2^{4}
MDD A	Seek error
MDD B	Seek error

Bit C (12)

SAC-1	SCU data/SBU RA bit 2^{3}
SAC-2	SCU data/SBU RA bit 2^{3}
MDD A	On cylinder
MDD B	On cylinder

Bit D (13)

SAC-1	SCU data/SBU RA bit 2^{2}
SAC-2	SCU data/SBU RA bit 2^{2}
MDD A	Pack unsafe
MDD B	Pack unsafe

Bit E (14)

SAC-1	SCU data/SBU RA bit 2^{1}
SAC-2	SCU data/SBU RA bit 2^{1}
MDD A	MDD error
MDD B	MDD error

Bit F (15)

SAC-1	SCU data/SBU RA bit 2^{0}
SAC-2	$\overline{\text{SCU data}}$/SBU RA bit 2^{0}
MDD A	$\overline{\text{Finished}}$
MDD B	$\overline{\text{Finished}}$

STAR-100 SERVICE STATION
OUTPUT CHANNEL 6

Bit 0

SAC-1	SBU Starting Address
SAC-2	SBU Starting Address
7000	SBU Starting Address
STAR A	I/O Chan 8 Select

Bit 1

SAC-1	SBU Terminating Address
SAC-2	SBU Terminating Address
7000	SBU Terminating Address
STAR A	I/O Chan 7 Select

Bit 2

SAC-1	Function
SAC-2	Function
7000	Function
STAR A	I/O Chan 6 Select

Bit 3

SAC-1	Program Clear
SAC-2	Program Clear
7000	Program Clear
STAR A	I/O Chan 5 Select

Bit 4

SAC-1	Request
SAC-2	Request
7000	Disable Error
STAR A	I/O Chan 4 Select

Bit 5

SAC-1	Accept
SAC-2	Accept
7000	
STAR A	I/O Chan 3 Select

Bit 6

SAC-1	Select Status
SAC-2	Select Status
7000	
STAR A	I/O Chan 2 Select

Bit 7

SAC-1	Set Interrupt
SAC-2	Set Interrupt
7000	
STAR A	I/O Chan 1 Select

Bit 8

	Norm Chan 7 Select
STAR A	Select SCU coupler
	Norm Chan 6, Bit 8 Fanout

Bit 9

Norm Chan 5 Select
Norm Chan 6, Bit 9 Fanout

Bit A

Norm Chan 6 Select
Norm Chan 6, Bit A Fanout

Bit B

Scanner Select
Norm Chan 6, Bit B Fanout

Bit C

Connect Code 2^3
Norm Chan 6, Bit C Fanout

Bit D

Connect Code 2^2
Norm Chan 6, Bit D Fanout

Bit E

Connect Code 2^1
Norm Chan 6, Bit E Fanout

Bit F

Connect Code 2^0
Norm Chan 6, Bit F Fanout

STAR-100 SERVICE STATION
INPUT CHANNEL 7

Bit 0		
	SAC-1	SCU Data/SBU RA Bit 2^{15}
	SAC-2	SCU Data/SBU RA Bit 2^{15}
Bit 1		
	SAC-1	SCU Data/SBU RA Bit 2^{14}
	SAC-2	SCU Data/SBU RA Bit 2^{14}
Bit 2		
	SAC-1	SCU Data/SBU RA Bit 2^{13}
	SAC-2	SCU Data/SBU RA Bit 2^{13}
Bit 3		
	SAC-1	SCU Data/SBU RA Bit 2^{12}
	SAC-2	SCU Data/SBU RA Bit 2^{12}
Bit 4		
	SAC-1	SCU Data/SBU RA Bit 2^{11}
	SAC-2	SCU Data/SBU RA Bit 2^{11}
Bit 5		
	SAC-1	SCU Data/SBU RA Bit 2^{10}
	SAC-2	SCU Data/SBU RA Bit 2^{10}
Bit 6		
	SAC-1	SCU Data/SBU RA Bit 2^{9}
	SAC-2	SCU Data/SBU RA Bit 2^{9}
Bit 7		
	SAC-1	SCU Data/SBU RA Bit 2^{8}
	SAC-2	SCU Data/SBU RA Bit 2^{8}
Bit 8		
	SAC-1	SCU Data/SBU RA Bit 2^{7}†
	SAC-2	SCU Data/SBU RA Bit 2^{7}
Bit 9		
	SAC-1	SCU Data/SBU RA Bit 2^{6}
	SAC-2	SCU Data/SBU RA Bit 2^{6}
Bit A		
	SAC-1	SCU Data/SBU RA Bit 2^{5}
	SAC-2	SCU Data/SBU RA Bit 2^{5}
Bit B		
	SAC-1	SCU Data/SBU RA Bit 2^{4}
	SAC-2	SCU Data/SBU RA Bit 2^{4}
Bit C		
	SAC-1	SCU Data/SBU RA Bit 2^{3}
	SAC-2	SCU Data/SBU RA Bit 2^{3}
Bit D		
	SAC-1	SCU Data/SBU RA Bit 2^{2}
	SAC-2	SCU Data/SBU RA Bit 2^{2}
Bit E		
	SAC-1	SCU Data/SBU RA Bit 2^{1}
	SAC-2	SCU Data/SBU RA Bit 2^{1}
Bit F		
	SAC-1	SCU Data/SBU RA Bit 2^{0}
	SAC-2	SCU Data/SBU RA Bit 2^{0}

†RA = Return address

INPUT CHANNEL 1
KEYBOARD

BIT	
0	Control Panel Lockout
1	Character Code 2^6
2	
3	
4	
5	
6	
7	2^0
8	Alarm Disable (alert)
9	Repeat
A	Lockout Switch
B	Data Strobe
C	Mode 1
D	Mode 2
E	Mode 3
F	Mode 4

OUTPUT CHANNEL 1
DRUM

BIT	
0	Data Mode
1	Write Request
2	Read Request
3	Sector Address 2^4
4	2^3
5	2^2
6	2^1
7	2^0
8	Character Mark
9	Word Address 2^6
A	2^5
B	2^4
C	2^3
D	2^2
E	2^1
F	2^0

INPUT CHANNEL 2
Coupler A/Microdrum

BIT	
0	Coupler Time-out Status
1	Parity Error Fault Status
2	Not used
3	Illegal Status
4	Suspend Status
5	Invalid Status
6	Fault Status
7	Channel Busy Status
8	Coupler Ready Status
9	
A	
B	Sector Address 2^4
C	2^3
D	2^2
E	2^1
F	2^0

OUTPUT CHANNEL 2
Coupler A

BIT	
0	Initiate Functions
1	Function 2^2 B0
2	Function 2^1 B1
3	Function 2^0 B2
4	Interrupt
5	Clear Fault
6	Disable Parity Check
7	Block Clear
8	
9	Coupler Select 2^1
A	Coupler Select 2^0
B	
C	
D	
E	
F	

INPUT CHANNEL 3

BIT	
0	Microdrum Busy
1	Real-Time Strobe
2	Flag Coupler A
3	Flag Coupler B
4	Index Pulse (Printer)
5	Row Pulse (Printer)
6	Paper Strobe (Printer)
7	Start (Printer)
8	Page Eject (Printer)
9	
A	
B	
C	
D	
E	
F	

OUTPUT CHANNEL 3
Microdrum/Keyboard

BIT	
0	Checksum Mode
1	
2	
3	
4	
5	Deadman Strobe
6	Alert Indicator
7	Buzzer
8	Lockout Keyboard
9	Compare Lockout (Drum)
A	Head Address 2^5
B	2^4
C	2^3
D	2^2
E	2^1
F	2^0

INPUT CHANNEL 4

BIT	
0	End of Record
1	Reject
2	Reply
3	Parity Bit
4	Input Data Bit 2^{11}
5	2^{10}
6	2^9
7	2^8
8	2^7
9	2^6
A	2^5
B	2^4
C	2^3
D	2^2
E	2^1
F	2^0

OUTPUT CHANNEL 4

BIT	
0	Function
1	Connect
2	Data Signal
3	Parity Bit
4	Output Data Bit 2^{11}
5	2^{10}
6	2^9
7	2^8
8	2^7
9	2^6
A	2^5
B	2^4
C	2^3
D	2^2
E	2^1
F	2^0

INPUT CHANNEL 5

BIT	
0	Respond Line Active
1	Transmit Parity Error
2	Interrupt Active
3	
4	
5	
6	
7	
8	
9	
A	
B	
C	
D	
E	
F	

OUTPUT CHANNEL 5

BIT	
0	Status Select
1	Negate BCD
2	Test Mode
3	Word Mark
4	Suppress Assy/Disassy
5	Master Clear
6	Write
7	Read
8	Channel Switch 2^1
9	Channel Switch 2^0
A	
B	
C	Head Select
D	Difference Select
E	Control Select
F	Sector Select

INPUT CHANNEL 6A
854 Disk Storage Drive

BIT	
0	Selected Unit 0
1	Selected Unit 1
2	Selected Unit 2
3	Selected Unit 3
4	Selected Unit 4
5	Selected Unit 5
6	Selected Unit 6
7	Selected Unit 7
8	Flag
9	Sector Mark
A	Index Mark
B	Ready
C	Seek Error
D	On Cylinder
E	On Sector
F	Fault

OUTPUT CHANNEL 6A
854 Disk Storage Drive

BIT	
0	Address and Control Bit 7
1	Address and Control Bit 6
2	Address and Control Bit 5
3	Address and Control Bit 4
4	Address and Control Bit 3
5	Address and Control Bit 2
6	Address and Control Bit 1
7	Address and Control Bit 0
8	Reset Flag
9	Hold Sector Mark
A	Hold Index Mark
B	Write
C	Zero Search
D	Unit Select 2^2
E	Unit Select 2^1
F	Unit Select 2^0

INPUT CHANNEL 6B
Printer

BIT	
0	
1	
2	
3	
4	
5	
6	
7	
8	
9	
A	
B	
C	
D	Out of Paper
E	Drum Latch Switch
F	29V Alarm

OUTPUT CHANNEL 6B
Printer

BIT	
0	Start Indicator
1	Select 8 Lines/inch
2	Advance Ribbon
3	Advance Paper
4	Hammer Enable
5	Compare
6	
7	
8	Hammer Address 7
9	Hammer Address 6
A	Hammer Address 5
B	Hammer Address 4
C	Hammer Address 3
D	Hammer Address 2
E	Hammer Address 1
F	Hammer Address 0

INPUT CHANNEL 6C
Coupler B

BIT	
0	Coupler Time-Out Status
1	Parity Error Fault Status
2	Read Parity Error Status
3	Illegal Status
4	Suspend Status
5	Invalid Status
6	Fault Status
7	Channel Busy Status
8	Coupler Ready Status
9	
A	
B	
C	Disable Parity Check
D	
E	
F	

OUTPUT CHANNEL 6C
Coupler B

BIT	
0	Initiate Functions
1	Function 2^2
2	Function 2^1
3	Function 2^0
4	Interrupt
5	Clear Fault
6	Disable Parity Check
7	
8	
9	
A	
B	
C	
D	
E	
F	

INTERFACE NORMAL CHANNEL BIT ASSIGNMENTS B

Appendix B lists normal channel bit assignments by interface for several of the most common interfaces in the SBU. For a listing of all bits used in any particular station, refer to appendix A.

TABLE B-1. SAC-1 AND SAC-2 SBU INTERFACE NIC BIT ASSIGNMENTS

		Paging (Drum) Station†	HCD Station	844 Storage Magnetic Tape Station	STAR-1B Service Station	STAR-100 Service Station	Storage (Media) Station	844 Service Station
NIC-5, Bit	0	SBU Parity Error						
	1	Bank Counter 2^2	(Same as Drum Station)	(Same as Drum Station)	(Same as Drum Station)	(Same as Drum Station)	(Same as Drum Station)	(Same as Drum Station)
	2	2^1						
	3	2^0						
	4	Transmission Parity Error						
	5	SAC Parity Error						
	6	Illegal						
	7	Busy						
	8	Term Addr Compare						
	9	First Rank Full						
	A	Last Rank Full						
	B	Control Function 2^1						
	C	Control Function 2^0						
	D	Control Function Strobe						
	E	NU						
	F	NU						
NIC-6, Bit	0							
	1							
	2			SAC-1 Flag	(Same as 844 Storage Station)	SAC-1 Not Busy	(Same as 844 Storage Station)	(Same as STAR-100 Service Station)
	3			SAC-2 Flag		SAC-2 Not Busy		
	4			SAC-1 Not Busy		SAC-1 Flag		
	5			SAC-2 Not Busy		SAC-2 Flag		
	6							
	7							
	8		SAC-1 Not Busy					
	9		SAC-2 Not Busy					
	A		SAC-1 Flag					
	B	SAC-1 Not Busy	SAC-2 Flag					
	C	SAC-1 Flag						
	D							
	E							
	F							
NIC-7, Bit	0	SCU Data/SBU RA Bit 2^{15}	SCU Data Bit 2^{15}	(Same as Drum Station)	(Same as Drum Station)	(Same as Drum Station)	(Same as Drum Station)	(Same as Drum Station)
	1		SCU Data/SBU RA Bit 2^{14}					
	2							
	3							
	4							
	5							
	6							
	7							
	8							
	9							
	A							
	B							
	C							
	D							
	E							
	F	2^0	2^0					

NU = not used
RA = return address
† Paging station uses SAC-1 interface only

TABLE B-2. SAC-1 AND SAC-2 SBU INTERFACE NOC BIT ASSIGNMENTS

	Paging (Drum) Station†		844 Storage Magnetic Tape Station	844 Service Station	STAR-1B Service Station	STAR-100 Service Station	Storage (Media) Station
NOC-5, Bit 0	SBU TA/SCU Addr/Data Bit 2^{15}	SCU Addr/Data Bit 2^{15}	(Same as Drum Station)	SBU TA/Data Bit 2^{15}	(Same as Drum Station)	(Same as Drum Station)	(Same as Drum Station)
1		SBU TA/SCU Addr/Data Bit 2^{14}					
2							
3							
4							
5							
6							
7							
8							
9							
A							
B							
C							
D							
E							
F	2^0	2^0		2^0			
NOC-6, Bit 0	SBU Starting Address	(Same as Drum Station)	(Same as Drum Station)	(Same as Drum Station)	SBU Starting address	(Same as Drum Station)	(Same as Drum Station)
1	SBU Terminating Address				SBU TA		
2	Function				Function		
3	Program Clear				Program Clear		
4	Request				Request		
5	Accept				Accept		
6	Select Status				Select Status		
7	Set Interrupt				Set Interrupt		
8							
9							
A							
B							
C	Connect Code 2^3				Connect Code 2^3		
D							
E							
F	2^0				2^0		
NOC-7, Bit 0	SBU SA Bit 2^{15}	NU	(Same as Drum Station)	(Same as Drum Station)	(Same as Drum Station)	(Same as Drum Station)	(Same as Drum Station)
1							
2							
3							
4							
5							
6	2^9						
7	Clear Parity Error/ SBU SA Bit 2^8	Clear Parity Error					
8	Clear Illegal/SBU SA Bit 2^7	Clear Illegal					
9	Clear Cont. Func./SBU SA Bit 2^6	Clear Cont. Func.					
A	Master Clear/SBU SA Bit 2^5	Master Clear					
B	SBU SA Bit 2^4	NU					
C	Select SAC + $\overline{\text{SCU}}$/SBU SA Bit 2^3	Select SAC+$\overline{\text{SCU}}$					
D	Function Code/SBU SA Bit 2^2	Function Code Bit 2^2					
E	2^1						
F	2^0	2^0					

Addr = address
SA = starting address
TA = terminating address
† Paging station uses SAC-1 interface only

TABLE B-3. 7000-0 AND 7000-1 SBU INTERFACE NIC BIT ASSIGNMENTS

		Paging (Drum) Station	HCD Station	STAR-100 Service Station †
NIC-5, Bit	0	SBU Parity Error	SBU Parity Error	(Same as Drum Station)
	1	Bank Counter 2^2	Bank Counter 2^2	
	2	2^1	2^1	
	3	2^0	2^0	
	4	Drum Sector Count 2^6	Disk Status 2^{11}	
	5	2^5		
	6	2^4		
	7	2^3		
	8	2^2		
	9	2^1		
	A	2^0		
	B	Drum Sector Stable		
	C	Drum EOT Bit 2^1		
	D	Drum Abnormal		
	E	Drum Parity Error		
	F	Drum Not Ready	2^0	
NIC-6, Bit	0	7000-1 Drum SC Bit 2^0	7000-0 Disk on Cylinder	
	1	7000-1 Drum EOT Bit 2^0	7000-0 Disk Error	Drum SC 2^0
	2	7000-0 Drum SC Bit 2^0	7000-0 Disk EOT Bit 2^1	
	3	7000-0 Drum EOT Bit 2^0	7000-0 Disk EOT Bit 2^0	
	4		7000-1 Disk on Cylinder	
	5		7000-1 Disk Error	
	6		7000-1 Disk EOT 2^1	Drum EOT 2^0
	7		7000-1 Disk EOT 2^0	Drum Error
	8		NU	
	9	7000-1 Drum Error		
	A	7000-0 Drum Error		
	B			
	C			
	D			
	E			
	F			
NIC-7, Bit	0	NU	Return Function 2^2	NU
	1			
	2		Return Function 2^1	
	3		Return Function 2^0	
	4		NU	
	5			
	6			
	7			
	8			
	9			
	A			
	B			
	C			
	D			
	E			
	F			

EOT = end of transfer
NU = not used
SC = sector count
† Only one 7000 interface used

TABLE B-4. 7000-0 AND 7000-1 SBU INTERFACE NOC BIT ASSIGNMENTS

		Paging (Drum) Station	HCD Station	STAR-100 Service Station
NOC-5, Bit	0	EDS/SDS	EDS/SDS/Software Bit 2^2	(Same as Drum Station)
	1	SBU SA/TA/Function Bit 2^{14}	SBU SA/TA Bit 2^{14}/Data Sequence	
	2		SBU SA/TA Bit 2^{13}/Software Bit 2^1	
	3		SBU SA/TA Bit 2^{12}/Software Bit 2^0	
	4		SBU SA/TA/Function Bit 2^{11}	
	5			
	6			
	7			
	8			
	9			
	A			
	B			
	C			
	D			
	E			
	F	2^0	2^0	
NOC-6, Bit	0	SBU Starting Address	(Same as Drum Station)	SBU Starting Address
	1	SBU Terminating address		SBU Terminating Addr
	2	Function		Function
	3	Program Clear		Program Clear
	4	Disable Error		Disable Error
	5	NU		
	6	NU		
	7	NU		
	8	NOC-7 Select		
	9	NOC-5 Select		
	A	NOC-6 Select		
	B	Scanner Select		
	C	Connect Code 2^3		Connect Code 2^3
	D			
	E	2^0		2^0
	F			
NOC-7, Bit	0	NU	(Same as NOC-5, above)	NU
	1			
	2			
	3			
	4			
	5			
	6			
	7			
	8			
	9			
	A			
	B			
	C			
	D			
	E			
	F			

NU = not used
SA = starting address
TA = terminating address
EDS/SDS = end data sequence/start data sequence

TABLE B-5. 3000-0 AND 3000-1 SBU INTERFACE NIC BIT ASSIGNMENTS

	844 Storage/Mag Tape Station	Storage (Media) Station
NIC-5, Bit 0	NU	(Same as Mag Tape Station)
1	NU	
2	Interrupt Active	
3	SBU Parity Error	
4	Read Parity Error	
5	Current Addr 2^{10}/Int Line 3	
6	2^{9} 2	
7	2^{8} 1	
8	2^{7} 0	
9	2^{6}/Byte Counter Rank 3	
A	2^{5} 2	
B	2^{4} 1	
C	2^{3} 0	
D	2^{2}/$\overline{\text{Phase}}$ $\overline{\text{Counter}}$ 2^{2}	
E	2^{1} 2^{1}	
F	2^{0} 2^{0}	
NIC-6, Bit 0	Write Parity Error/TA Empty 0	(Same as Mag Tape Station)
1	End of Record/TA Empty 1	
2	Reject	
3	Reply	
4	Reserved	
5	Vert or Long Parity Error	
6	End of Operation/Response, 3000-0	
7	Lost Data/Adrs Comp, 3000-0	
8	800 BPI/Response, 3000-1	
9	556 BPI/Adrs Comp, 3000-1	
A	End of Tape	
B	Load Point	
C	File Mark	
D	Write Enable	
E	Busy	
F	Ready	
NIC-7, Bit 0	NU	NU
1		
2		
3		
4		
5		
6		
7		
8		
9		
A		
B		
C		
D		
E		
F		

Addr = address
BPI = bits per inch
C1 = channel 1
Err = error
Int = interrupt
Vert or Long = vertical or longitudinal
NU = not used

TABLE B-6. 3000-0 AND 3000-1 SBU INTERFACE NOC BIT ASSIGNMENTS

	844 Storage/Mag Tape Station	Storage (Media) Station
NOC-5, Bit 0	Compare Bit/Binary/Coded	(Same as Mag Tape Station)
1	SBU SA/TA/TBA/Read/Write	
2	SBU SA/TA/TBA/CONN/FCTN	
3	/Odd/Even SEL	
4	/FCTN Code/Dis Req/Conn Code/	
5	/HOE	
6	/RE BA	
7		
8		
9		
A		
B		
C		
D		
E		
F		
NOC-6, Bit 0	SBU SA	(Same as Mag Tape Station)
1	SBU TA	
2	**Internal Function**	
3	Program Clear	
4	Channel Function	
5	SBU TBA	
6	SBU Current Address	
7	NU	
8		
9		
A		
B		
C	Connect Code 2^{3}	
D		
E	2^{0}	
F	2^{0}	
NOC-7, Bit 0	NU	NU
1		
2		
3		
4		
5		
6		
7		
8		
9		
A		
B		
C		
D		
E		
F		

C1 = channel 1
HOE = halt on error
CONN = connect
DIS Req = disable request
FCTN = function
RE BA = Read backward
SA = starting address
SEL = select
TA = terminating address
TBA = table address

TABLE B-7. INDEX COMPARE SBU INTERFACE NIC BIT ASSIGNMENTS

	Paging (Drum) Station	STAR-1B Service Station
NIC-5, Bit 0	SBU Parity Error	Null Hit
1	Bank Counter 2^2	Bank Counter 2^2
2	2^1	2^1
3	2^0	2^0
4		Request One Hit
5		Request Zero Hit
6		Delete Key Count 2^9
7		
8		
9		
A		
B		
C		
D		
E		
F		2^0
NIC-6, Bit 0		
1		No Compare Parity Error
2		
3		
4	No Compare Parity Error	
5	Compare Req-1 Hit	
6	Compare End of Table	Compare End of Table
7	Compare Req-0 Hit	Compare Not Busy
8		
9		
A		
B		
C		
D	Compare Not Busy	
E		
F		
NIC-7, Bit 0		NU
1		
2		
3		
4		
5		
6	Delete Key Count Bit 2^9	
7		
8		
9		
A		
B		
C		
D		
E		
F	2^0	

NU = not used
REQ = request

TABLE B-8. INDEX COMPARE SBU INTERFACE NOC BIT ASSIGNMENTS

	Paging (Drum) Station	STAR-1B Service Station
NOC-5, Bit 0		Key ID
1		Request ID
2		
3		
4		
5		
6		
7		
8		
9		
A		
B		
C		
D		
E	Key ID	
F	Request ID	
NOC-6, Bit 0	SBU Starting Address	(Same as Drum Station)
1	SBU Terminating Address	
2	Load Request Register	
3	Program Clear	
4	Start Search	
5	Write Buffers	
6	Search Backward	
7	One Request	
8		
9		
A		
B		
C	Connect Code 2^3	
D	2^2	
E	2^1	
F	2^0	
NOC-7, Bit 0	Request Bit 2^{15}	(Same as Drum Station)
1	SBU SA/TA/Request Bit 2^{14}	
2		
3		
4		
5		
6		
7		
8		
9		
A		
B		
C		
D		
E		
F	2^0	

ID = identification bit
SA and TA = starting and terminating address, respectively

TABLE B-9. STAR A SBU INTERFACE NIC BIT ASSIGNMENTS

	844 Service Station	STAR-1B Service Station	STAR-100 Service Station
NIC-5, Bit 0	MEM P. E. /SCU Chan	MEM P.E. - SCU Coupler	MEM P. E. /SCU Chan
1	STA INT X Bank CTR 2^2	STA INT X Bank Count 22	STA INT X Bank CTR 2^2
2	2^1	2^1	2^1
3	2^0	2^0	2^0
4		MEM P.E. I/O Chan 6	
5		5	
6		4	
7		3	
8	MEM P. E. I/O Chan 1	2	MEM P. E. I/O Chan 1
9	2	1	2
A	3		3
B	4		4
C			5
D			6
E			7
F			8
NIC-6, Bit 0	MEM P. E. I/O Chan	MEM P. E. I/O Chan	MEM P. E. I/O Chan
1			
2			
3			
4			
5			
6			
7			
8	I/O Interrupt-Chan 1	I/O Int-Chan 1	I/O Interrupt-Chan 1
9	2	1	2
A	3	2	3
B	4	3	4
C		4	5
D		5	6
E		6	7
F			8
NIC-7, Bit 0	NU	NU	NU
1			
2			
3			
4			
5			
6			
7			
8			
9			
A			
B			
C			
D			
E			
F			

CTR = counter
I/O = input/output
MEM P. E. = memory parity error
NU = not used
STA INT = station interface

TABLE B-10. STAR A SBU INTERFACE NOC BIT ASSIGNMENTS

	844 Service Station	STAR-1B Service Station	STAR-100 Service Station
NOC-5, Bit 0	NU		NU
1			
2			
3			
4			
5			
6			
7			
8			
9			
A			
B		Clear Interrupt	
C		Program Clear	
D		Control Function 2^1	
E		Control Function 2^0	
F		Cont Fctn Strobe	
NOC-6, Bit 0			I/O Chan 8 Select
1		I/O Chan 6 Select	7
2		5	6
3		4	5
4	I/O Chan 4 Select	3	4
5	3	2	3
6	2	1	2
7	1		1
8			
9			
A			
B			
C	Connect Code 2^3	Connect Code 2^3	Connect Code 2^3
D	2^2	2^2	2^2
E	2^1	2^1	2^1
F	2^0	2^0	2^0
NOC-7, Bit 0		NU	
1			
2			
3			
4			
5			
6			
7			
8			
9			
A			
B	Clear Interrupt		Clear Interrupt
C	Program Clear		Program Clear
D	Control Function 2^1		Control Function 2^1
E	Control Function 2^0		Control Function 2^0
F	Cont Fctn Strobe		Cont Fctn Strobe

I/O = input/output
NU = not used
Cont Fctn = control function

TABLE B-11. 844 SBU INTERFACE NIC BIT ASSIGNMENTS

	844 Service Station	844 Storage Station
NIC-5, Bit 0	NU	NU
1		
2		
3		
4		
5		
6		
7		
8		
9		
A		
B		
C		
D		
E		
F		
NIC-6, Bit 0	Unit Busy	Unit Busy
1	Unit 1 Selected	Unit 1 Selected
2	2	2
3	3	3
4	NU	4
5		5
6		6
7		7
8		8
9		9
A	Read Error	Read Error
B	Tag BCC Error	Tag BCC Error
C	Timing Chain	Timing Chain
D	SBU Bank Counter 2^2	SBU Bank CTR 2^2
E	2^1	2^1
F	2^0	2^0
NIC-7, Bit 0	Finished	Finished
1	Unit 1 on Sector/Seek Error	Unit 1 on Sector
2	2	2
3	3	3
4	NU	4
5		5
6		6
7		7
8		8
9		9
A	Ready	Ready
B	Transfer Error	Transfer Error
C	On Cylinder	On Cylinder
D	Seek Error	Seek Error
E	Pack Unsafe	Pack Unsafe
F	Full	Full

BCC = block check code
CTR = counter
NU = not used

TABLE B-12. 844 SBU INTERFACE NOC BIT ASSIGNMENTS

	844 Service Station	844 Storage Station
NOC-5, Bit 0	NU	NU
1		
2		
3		
4		
5		
6		
7		
8		
9		
A		
B		
C		
D		
E		
F		
NOC-6, Bit 0		
1		
2		
3		
4		
5		
6		
7	Load SBU Address	Load SBU Address
8	Release	Release
9	Function	Function
A	Begin Transfer	Begin Transfer
B	NU	NU
C	Connect Code 2^3	Connect Code 2^3
D	2^2	2^2
E	2^1	2^1
F	2^0	2^0
NOC-7, Bit 0	NU	NU
1	Select Unit 1	Select Unit 1
2	2/Write Tag/Diff Sel	2/Write Tag/DIFF SELECT
3	3/Write/Clear Fault	3/Write/Clear Fault
4	Full/Control Select	4/Full/Control Select
5	Odd Bank/Sector Select	5/Odd/Sector Select
6	SBU MEM Address/Cylinder Select	6/SBU MEM ADDR 2^{14}/ Cylinder Sel
7		7/SBU MEM ADDR 2^{13}/ DSU ADDR and CONT 2^8
8	Address/Control Bit 8	8/SBU MEM ADDR 2^{12}/ DSU ADDR and CONT 2^7
9		9/SBU MEM ADDR 2^{11}/ DSU ADDR and CONT 2^6
A		SBU MEM ADDR 2^{10}/DSU ADDR and CONT 2^5
B		2^9 2^4
C		2^8 2^3
D		2^7 2^2
E		2^6 2^1
F	Bit 0	2^5 2^0

DIFF SEL = difference select
DSU ADDR and CONT = disk storage unit address and control
MEM ADDR = memory address NU = not used

TABLE B-13. MDD (841) SBU INTERFACE NIC BIT ASSIGNMENTS

	STAR-1B Service Station	Storage (Media) Station
NIC-5, Bit 0	NU	NU
1		
2		
3		
4		
5		
6		
7		
8		
9		
A		
B		
C		
D		
E		
F		
NIC-6, Bit 0	Unit 0 Selected	(Same as STAR-1B Service Station)
1	1	
2	2	
3	3	
4	4	
5	5	
6	6	
7	7	
8	8	
9	Full	
A	Read Error	
B	Tag BCC Error	
C	End of Page	
D	SBU Bank Counter 2^2	
E	2^1	
F	2^0	
NIC-7, Bit 0	Unit 0 on Sector/Seek Error	(Same as STAR-1B Service Station)
1	1	
2	2	
3	3	
4	4	
5	5	
6	6	
7	7	
8	8	
9	Busy	
A	Ready	
B	Seek Error	
C	On Cylinder	
D	Pack Unsafe	
E	MDD Error	
F	Finished	

BCC = block check code
MDD = multiple disk drive
NU = not used

TABLE B-14. MDD (841) SBU INTERFACE NOC BIT ASSIGNMENTS

	STAR-1B Service Station	Storage (Media) Station
NOC-5, Bit 0	Release/Write Tags	Release/Write Tags
1	Sector Select/Full	Sector Select/Full
2	Diff Select/Proceed	Diff Select/Proceed
3	Clear/Odd	Clear/Odd
4	Logic No. 2^2/Page Addr 2^{14}	Logic No. 2^2/Page Address 2^{14}
5	2^1/ 2^{13}	2^1/ 2^{13}
6	2^0/ 2^{12}	2^0/ 2^{12}
7	Unit Select/ 2^{11}	Unit Select/ 2^{11}
8	Addr and Cont Bit 7/Write	Addr and Cont Bit 7/Write
9	6	6
A	5/HDR ADDR 2^{10}	5/Hdr Addr 2^{10}
B	4/ 2^9	4/ 2^9
C	3/ 2^8	3/ 2^8
D	2/ 2^7	2/ 2^7
E	1/ 2^6	1/ 2^6
F	0/ 2^5	0/ 2^5
NOC-6, Bit 0		
1		
2		
3		
4		
5		
6		
7		Load Address
8	Begin Transfer	Control Select
9	Clear End Page	Function
A	Load Address	Begin Transfer
B	Control Select	Clear End Page
C	Function	Connect Code 2^3
D	Connect Code 2^2	2^2
E	2^1	2^1
F	2^0	2^0
NOC-7, Bit 0	NU	NU
1		
2		
3		
4		
5		
6		
7		
8		
9		
A		
B		
C		
D		
E		
F		

ADDR and CONT = address and control
DIFF = difference
NU = not used
HDR = header

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