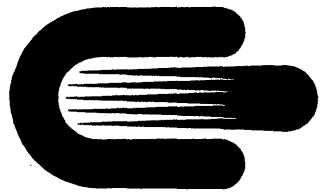

CLEARPOINT INC.

Q-RAM 22B

USER INFORMATION MANUAL

106 South Street
Hopkinton, MA 01748
(617) 435-5395
Telex: 298281

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CHAPTER 1

GENERAL DESCRIPTION AND SPECIFICATIONS

1.1 INTRODUCTION

This manual supplies user information for the Q-RAM 22(B) family of memory modules. Q-RAM 22(B) modules (see Table 1) provide high density, low cost per bit storage for systems which utilize the Digital Equipment Corporation (hereafter referred to as DEC*) Q-BUS. 64K MOS RAMS are used as individual storage devices to provide up to 1 mbyte on a single quad-height board. Features available on Q-RAM 22(B) are:

- Up to 1 MB memory capacity
- Jumper selectable 18 or 22(B) bit addressing
- Parity generation and checking on board
- Complete DEC software-hardware compatible, parity control and status register on board locatable at any of 8 assigned I/O page address
- Battery back-up support
- Single 5 volt power supply
- Starting address programmable at any 64K boundary
- Parity error LED provides visual indication of board failure

Table-1 Q-RAM Products

Designation	Description
Q-RAM 22(B)	1 MB board with parity
Q-RAM 22(B)-1	1 MB board no parity
Q-RAM 22(B)-2	512 KB board with parity
Q-RAM 22(B)-3	512 KB board no parity

*Registered trademark of Digital Equipment Corporation

1.2 GENERAL DESCRIPTION

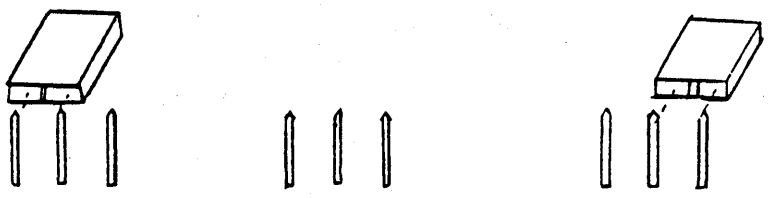
The Q-RAM 22(B) is a single quad-height memory module which interfaces to the LSI-11 Q-BUS. All timing and control logic for the memory, refresh circuitry, parity control, and status register are contained on board.

The MOS memory array consists of up to eight rows of 65,536 X 1 bit dynamic RAM devices with 18 devices per row. Each row will accept 65,536 18 bit words consisting of (two) eight bit bytes and two parity bits (one per byte). Circuitry for refresh of the MOS memory devices is provided on board and operates transparently to the user.

The Q-RAM 22(B) module's starting address is selectable using program plugs P0 to P4 (see figure 1 and 2) to any 64K boundary within the Q-BUS 22 or 18 bit address space. Program plug P7 is used to select 18 bit or 22 bit addressing. BDAL 18, BDAL 19, BDAL 20, and BDAL 21 are ignored if 18 bit addressing is selected.

The module will not respond to BBS7 transfers to allow the top 4K addresses to be reserved for I/O peripherals. P8 is provided on board which allows the user to reclaim 2K of the I/O page for system memory (see figure 2).

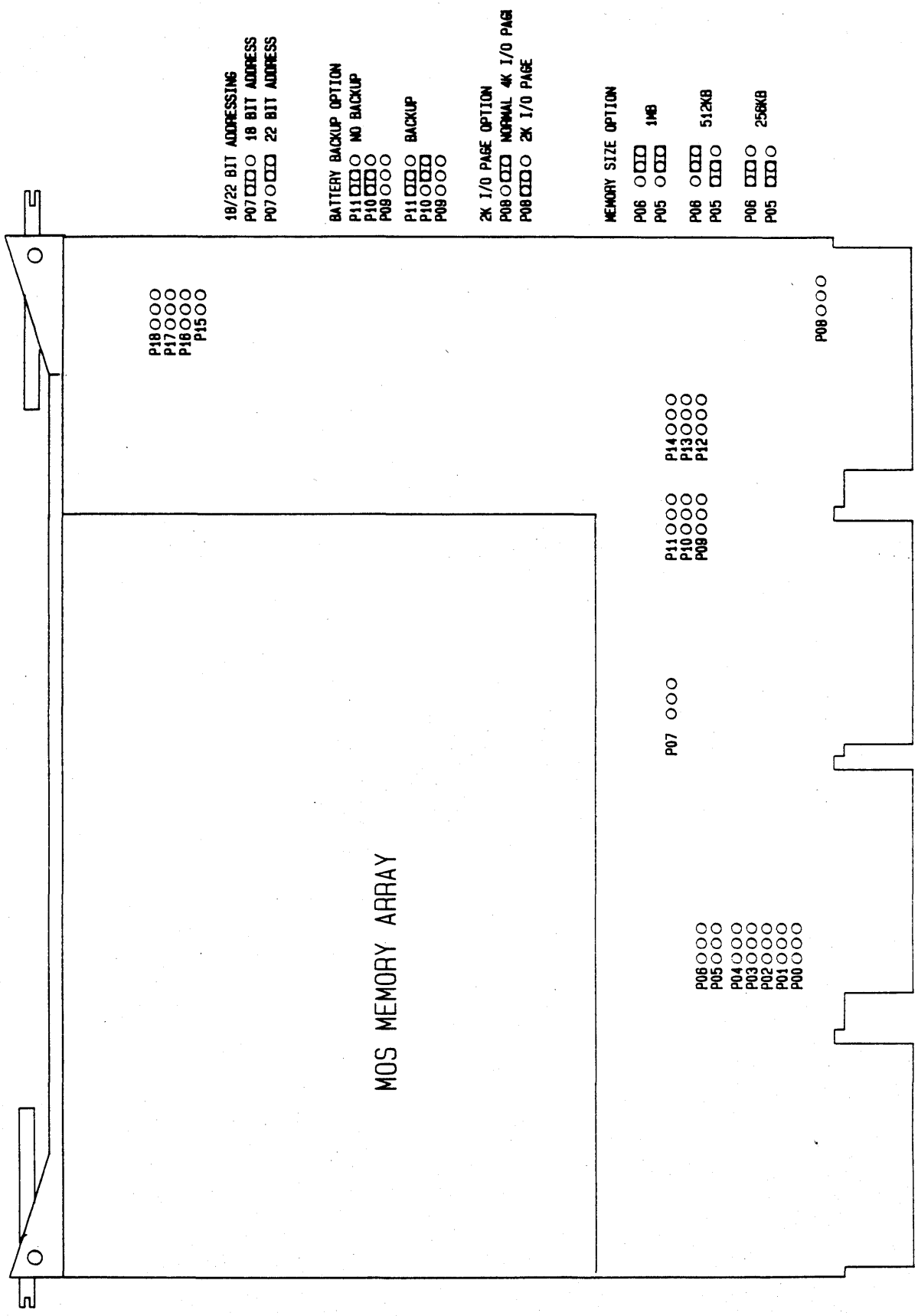
FIGURE 1 PROGRAM PLUG DESCRIPTION



ON OUT OFF

When holding board fingers down, program plugs positioned to left are defined as "ON". Those positioned to right are "OFF".

FIGURE 2 Q-RAM 22, Q-RAM 22B



When any byte of data is written to Q-RAM 22(B) boards which contain parity, a parity bit is generated which is stored along with the byte of data in the memory array. Whenever a byte of data is read the parity logic checks it against the stored parity bit. If parity is bad, an error has occurred and data is asumed to be bad.

In order to utilize the parity generation and checking circuitry in the Q-RAM 22(B), a control and status register is provided on board which is both hardware and software compatible with LSI-11 systems.

The control and status register is used to enable the board to interrupt if an error has occurred, latch the upper address bits of the location with bad data, set the parity error flag on error, and force bad parity writing for diagnostic purposes.

1.3 BACKPLANE PIN UTILIZATION

Table 2 contains backplane power pins required for Q-RAM 22(B). Table 3 designates pins used for other signals. Board finger designations shown in figure 2 are equivalent to backplane pin designations.

Table-2 Backplane Power Pins Required

Voltage	Pin
+5 normal	BV1
	AA2
	BA2
ground	AT1
	BT1
	AC2
	BC2
+5 battery (if used)	AV1
+5 Battery spare (if used)	AS1
	AE1

Table-3 Backplane I/O Signal Pins

Signal	Pin
AC1	BDAL 16 L
AD1	BDAL 17 L
BA1	BDCOK H
BC1	BDAL 18 L
BD1	BDAL 19 L
BE1	BDAL 20 L
BF1	BDAL 21 L
AE2	BDOUT L
AF2	BRPLY L
AH2	BDIN L
AJ2	BSYNC L
AK2	BWTBT L
AM2	BIAKI L
AN2	BIAKO L
AP2	BBS7 L
AR2	BDMGI L
AS2	BSMGO L
AU2	BDAL 00 L
AV2	BDAL 01 L
BE2	BDAL 02 L
BF2	BDAL 03 L
BH2	BDAL 04 L
BJ2	BDAL 05 L
BK2	BDAL 06 L
BL2	BDAL 07 L
BM2	BDAL 08 L
BN2	BDAL 09 L
BP2	BDAL 10 L
BR2	BDAL 11 L
BS2	BDAL 12 L
BT2	BDAL 13 L
BU2	BDAL 14 L
BV2	BDAL 15 L

1.4 SPECIFICATIONS

CHARACTERISTICS	SPECIFICATIONS
memory device type	MOS dynamic RAM (65,536 X 1)
read access time	200 ns typ.
write access time	50 ns typ.
memory cycle time	450 typ.
operating temperature	0 to +65 C
storage temperature	-40 to +85 C
relative humidity	0 to 90% (non-condensing
voltages required	+5V ±5% pins BU1,AA2,BA2
battery backup voltage	+5V ±5% pins AV1,AS1*,AE1
+5V operating current	2 amp typ.
+5V standby current	2 amp typ.
+5V battery backup current	.9 amp typ.

* optional spares available on backplane

CHAPTER 2

HARDWARE INSPECTION, INSTALLATION, AND CHECKOUT

2.1 INTRODUCTION

This chapter provides information for configuring the Q-RAM 22(B) programmable plug options prior to system installation followed by installation and checkout procedures.

2.2 CONFIGURING THE Q-RAM 22(B) PROGRAM PLUGS

Figure 2 provides the locations of the various Q-RAM 22(B) option jumpers and Figure 1 illustrates how they are used. The module should be inspected prior to installation to assure that it has been properly configured. Sections 2.3 through 2.6 describe the various Q-RAM 22(B) program plug options.

2.3 ADDRESSING OPTIONS

Q-RAM 22(B) addressing logic is capable of either 22 or 18 bit operation. P7 is used to select the desired addressing mode as follows:

P7 - ON	18 Bit Address Mode
P7 - OFF	22 Bit Address Mode

BDAL 18, BDAL 19, BDAL 20, and BDAL 21 are ignored if 18 bit addressing mode is selected and the board may not be configured to respond to addresses above 128K.

The memory starting address may be programmed at any 64K boundary using jumpers P0 through P4. Depending on the size of the board, the memory will utilize up to 524,288 contiguous word addresses in the address space beginning at

the selected starting address. Q-RAM 22(B) board size options are described in section 2-4.

To program the starting address of memory, BDAL 21 through BDAL 17 must be reflected by the following program plug configurations:

BDAL 21 1	P4 ON
BDAL 21 0	P4 OFF
BDAL 20 1	P3 ON
BDAL 20 0	P3 OFF
BDAL 19 1	P2 ON
BDAL 19 0	P2 OFF
BDAL 18 1	P1 ON
BDAL 18 0	P1 OFF
BDAL 17 1	P0 ON
BDAL 17 0	P0 OFF

Appendix A may be used to determine starting addresses if the Q-RAM 22(B) is to placed over existing resident memory. Table 4 may be used as an illustration of the above described formula. Table 4 may also be used to directly configure systems with multiple Q-RAM 22(B) 1 MB boards.

Table-4 Multiple Q-RAM 22(B) Starting Addresses

BRD	STARTING ADDRESS							PLUG CONFIGURATIONS				
#	A21	A20	A19	A18	A17	A16	A15	P4	P3	P2	P1	P0
1	0	0	0	0	0	0	0	OFF	OFF	OFF	OFF	OFF
2	0	1	0	0	0	0	0	OFF	ON	OFF	OFF	OFF
3	1	0	0	0	0	0	0	ON	OFF	OFF	OFF	OFF
4	1	1	0	0	0	0	0	ON	ON	OFF	OFF	OFF

The BBS7 signal is used during the address portion of a data transfer cycle on the Q-BUS. It indicates that the bus master is requesting a data transfer with one of the I/O devices in the 4K I/O page space. BBS7 is asserted whenever an I/O page transfer is requested. The memory board should ignore all transfers requested within the I/O

space. If, however, there are few peripherals on the system and it is desired by the user to reserve only 2K of the I/O page space, plug P8 may be used as follow:

P8 - OFF	Normal 4K I/O Page
P8 - ON	Reserve Only 2K I/O Page

2.4 BOARD SIZE CONFIGURATION PLUGS

Plugs P5 and P6 are used to configure the board size. Q-RAM 22(B) boards have up to eight rows of 65,536 X 1 bit dynamic RAM devices with 18 devices per row. Each row will accept 65,536 (64K) 18 bit words. A Q-RAM 22(B) may have 2, 4, or 8 rows of memory chips corresponding to 128K, 256K, or 512K words respectively. P5 and P6 must be configured, as shown in Table 5, to match the size of the memory array on board.

Table-5 Memory Size Jumpers

Board memory capacity	P5	P6
128K words	ON	ON
256K words (1/2 MB)	ON	OFF
512K words (1 MB)	OFF	OFF

2.5 CSR OPTION PLUG CONFIGURATION

The parity control and status register (hereafter referred to as CSR) has an I/O page address in the top 4K of memory. This address may be any one of eight specified locations reserved by DEC for this purpose. Program plugs P12, P13, and P14 are used to select one of the reserved addresses. Table 6 illustrates the use of these plugs. Note that each memory board used in a system must be configured to a different address.

Table-6 CSR Address Selection

CSR Address	P14	P13	P12
772100	ON	ON	ON
772102	ON	ON	OFF
772104	ON	OFF	ON
772106	ON	OFF	OFF
772110	OFF	ON	ON
772112	OFF	ON	OFF
772114	OFF	OFF	ON
772116	OFF	OFF	OFF
No CSR or Parity*	OUT	OUT	OUT

*To disable parity, remove P12, P13, and P14 plugs

2.6 BATTERY BACKUP OPTION PLUGS

The MOS memory, unlike core memory, requires the 5 volt supply to retain data. If the 5V power is removed from the board, system memory data is lost.

The battery backup option is used if battery power is available to maintain system memory data during power failures. Battery backup 5V must be available on backplane pin AV1. AS1 or AE1 may be used as an additional battery backup 5V input pin. Table 7 shows the various configurations of the battery backup mode select plugs P9, P10, and P11.

Table-7 Battery Backup Mode Options

Battery Backup Mode	P11	P10	P9
No Backup	ON	ON	OUT
Battery Backup +5 AV1 (AS1, AE1 unused)	OFF	OFF	OUT
Battery Backup +5 AV1,AS1	OFF	OFF	ON
Battery Backup +5 AV1,AE1	OFF	OFF	OFF

2.7 INSTALLATION PROCEDURE

The following procedure should be followed when a Q-RAM 22(B) board is received.

1. Visually inspect the module to make sure that it has arrived in good condition.

2. Set up program plug options for required operation.

3. Verify that the required power connections are available on the backplane (see Table 2).

4. Power down the system. Make sure that the system is powered off before plugging in the module.

5. Plug the module into the QBUS. Memories should be installed in sequential slots following the CPU. Make sure that the module is not being inserted backwards. The component side must face in the same direction as other modules in the system.

6. Power up the system and run any DEC memory diagnostic as an initial test. If available, use the following diagnostics:

   MAINDEC-11 CVMSA (22(B) bit system diagnostic)
   MAINDEC-11 CZKMA (18 bit system diagnostic)

CHAPTER 3

CSR DESCRIPTION

3.1 INTRODUCTION

When any byte is written to Q-RAM 22(B) boards with parity option, a parity bit is generated which is stored along with the byte of data in the memory array. Whenever a byte of data is read, the parity logic checks it against the stored parity bit. If parity is bad, an error has occurred and data is assumed to be bad.

In order for software to utilize the parity generation and checking circuitry in the Q-RAM 22(B), a control and status register (CSR) is provided.

The CSR is assigned an address in the I/O page (see Table 6) which may be accessed by software. When a parity error is detected, the upper address bits of the bad memory location (A11 to A21) are latched in the CSR. Control bits are provided in the CSR to enable interrupt on error and write of bad parity for diagnostic purposes.

3.2 CSR BIT ASSIGNMENT

The CSR is a 16 bit register located in the I/O page. The function of the 16 bits in the CSR are as follows:

Bit 0 — Parity error interrupt enable

If set to 1, the memory board will interrupt the processor on error, by setting bits BDAL 17 and BDAL 16 along with the data bits BDAL 0 to BDAL 15. This will result in an LSI-11 processor trap to location 114. BUS INIT clears this bit.

Bit 1 UNUSED

Bit 2 Write wrong parity

If this bit is set to 1, any word or byte written to the array will be stored along with an incorrect parity bit. This is for maintenance purposes. It enables didagnostics to check the boards ability to detect parity errors and interrupt when enabled. This bit is cleared by BUS INIT.

Bit 3 UNUSED

Bit 4 UNUSED

Bit 5 - 11 Latch address bits

When a parity error is detected, the upper address bits of the failing location are latched. These bits are not cleared by BUS INIT, but are writeable, as well as readable. When an error is detected, address bits 11 to 21 are displayed in these bits. Since there are only 7 bits and there are 11 latched address bits, they are multiplexed. Bit 14 in the CSR controls which of the latched address bits are on display. (see Table 8).

Bit 12 UNUSED

Bit 13 UNUSED

Bit 14 Extended CSR read enable

(See Table 8.) This bit is used to multiplex the extended latched address bits A18 to A21 into the CSR bits 5 to 11. This bit is cleared by BUS INIT. Program plug P17 may be used to disable setting of bit 14. If plug P17 is on, CSR bit 14 is always 0.

Bit 15 Parity error flag

This bit is set if a parity error is detected and remains set until cleared by being written or by BUS INIT.

Table-8 CSR Bits 5 to 11

CSR Bit	If CSR Bit 14-0	If CSR Bit 14-1
05	Latched A11	Latched A18
06	Latched A12	Latched A19
07	Latched A13	Latched A20
08	Latched A14	Latched A21
09	Latched A15	0
10	Latched A16	0
11	Latched A17	0

APPENDIX A

MEMORY STARTING ADDRESS CHART

Resident memory in K words	Starting Address A21	A20	A19	A18	A17
0K	0	0	0	0	0
64K	0	0	0	0	1
128K (1/4 MB)	0	0	0	1	0
192K	0	0	0	1	1
256K (1/2 MB)	0	0	1	0	0
320K	0	0	1	0	1
384K (3/4 MB)	0	0	1	1	0
448K	0	0	1	1	1
512K (1 MB)	0	1	0	0	0
576K	0	1	0	0	1
640K (1 1/4 MB)	0	1	0	1	0
704K	0	1	0	1	1
768K (1 1/2 MB)	0	1	1	0	0
832K	0	1	1	0	1
896K (1 3/4 MB)	0	1	1	1	0
960K	0	1	1	1	1
1024K (2 MB)	1	0	0	0	0

If starting address is greater than 2MB, subtract 2MB from the total. Set A21-1 and use table to determine state of 1A5 through A20 by finding remainder in table.

APPENDIX B

BANK SELECTION

The bank select feature designed into the Q-RAM 22(B) products is used essentially to increase the available main memory which is addressable in a Q-BUS* system. With Clearpoint bank select memory, up to 32 megabytes may be used in a single Q-BUS system with no hardware modifications required.

To enable the Q-RAM 22(B), bank selectability jumpers P15, P16, P17, and P18 (see figure 2) are used. If all of these jumpers are "out" (see figure 1), the bank select feature is disabled. To use this feature, P16, P17, and P18 must be installed. P15 may be installed as shown below (see table).

Any board which has jumpers P18, P17, and P16 installed will respond to writes (DOUT cycles) to I/O page CSR address 7775100 in one of the following two ways:

1. If P15 is not installed, the board will latch bank select bits provided by D5,D6, and D7 in the word being written.
2. If P16,P17, and P18 are all on (see figure 1) and P15 is installed; the board will respond with BREPLY L to any write to address 177775100 and latch bank select bits from D5, D6, and D7 in the word being written.

Since 7775100 is a write only address the memory boards will not respond to read (DIN cycles) using 7775100 at all.

To verify data being written into bits 5, 6, and 7 of the bank select control status register, data written will be displayed in bits 5 - 11 of the parity control status register for each board.

*Q-BUS is a registered trademark of Digital Equipment Corporation.

Bank selectable boards have unique parity CSR addresses as well. Boards which are not enabled for bank select have registers as described in Table 6. Parity CSR addressing for boards configured for bank select is described below.

Table 6 CSR Address Selection for Boards Enabled for Bank Select

CSR Address	P14	P13	P12
772120	ON	ON	ON
772122	ON	ON	OFF
772124	ON	OFF	ON
772126	ON	OFF	OFF
772130	OFF	ON	ON
772132	OFF	ON	OFF
772134	OFF	ON	ON
772136	OFF	OFF	OFF
No CSR or Parity*	OUT	OUT	OUT

*Parity may not be disables for bank selectable boards.

All memory boards in the system must have a unique parity CSR address. Parity must be enabled to use bank select.

The data bits written into CSR 7775100 bits 5, 6, and 7 select which page of memory will be accessible in bank selectable address space and up to eight pages may be available. The following table shows how jumpers P16, P17, and P18 correspond to the selection bits written into 7775100.

Table-7 Page Selection Options

Bank Select Page	CSR Bit 7	CSR Bit 6	CSR Bit 5	P18	P17	P16
0	0	0	0	ON	ON	ON
1	0	0	1	ON	ON	OFF
2	0	1	0	ON	OFF	ON
3	0	1	1	ON	OFF	OFF
4	1	0	0	OFF	ON	ON
5	1	0	1	OFF	ON	OFF
6	1	1	0	OFF	OFF	ON
7	1	1	1	OFF	OFF	OFF

APPENDIX C

The Q-RAM 22B Block Mode DMA Memory Board

The Q-RAM 22B is designed to implement the block mode DMA protocols on the Q-BUS. Block Mode DMA reduces the "handshaking" necessary to transfer data and thereby increases the transfer rate by a factor of nearly 2. From the user's perspective there is no difference in the operation or configuration of the Q-RAM 22B since the board will operate transparently using whatever form of DMA is invoked by other devices on the bus.

What is Block Mode DMA?

Under conventional direct memory access (DMA), direct data transfers between I/O devices and memory occur one (16 bit) word at a time or one byte at a time using DATI, DATO or DATO (B) bus cycles. Under block mode DMA, the starting address is followed not only by data for that address, but by data for up to 16 consecutive addresses. By eliminating the assertion of the address for each data word, the transfer rate is nearly doubled.

The Q-RAM 22B can also be used in system configurations with non-block mode DMA memory boards (either above or below). Most new Q-BUS peripheral controllers will be supporting block mode protocols and take advantage of the improved bus bandwidth using DATBI and DATBO type bus cycles. For devices already designed that do not use these block mode bus cycles, bus operation is unaffected.

For a complete technical description of these protocols, refer to the 1983 PDP-11 Micro/PDP-11 Handbook published by Digital Equipment Corporation.