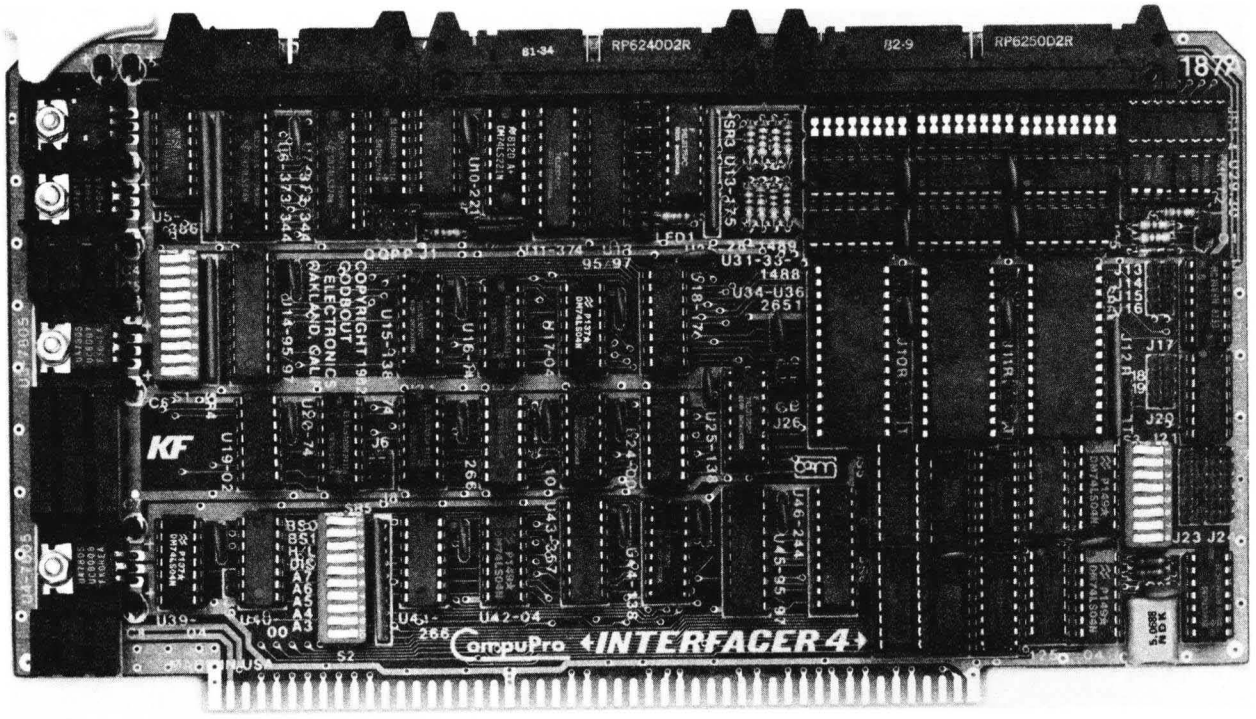
‹INTERFACER 4›™

TECHNICAL MANUAL



IEEE 696 / S-100

3 CHANNEL SERIAL I/O BOARD

with CENTRONICS and Universal Parallel Ports

187C

mac

CompuPro®

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Document #11877

DISCLAIMER

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How to Get Your INTERFACER 4 Board Up and Running in a CompuPro System in Five Minutes or Less Without Reading the Manual

This section allows the user to configure an **INTERFACER 4** in a standard **CompuPro** system running CP/M-80 or CP/M-86 so that the **INTERFACER 4** DRIVES the console, list and UL1 devices. If, after reading and following the directions in this section, your board appears not to function, or if you are planning to use this board in other than a standard **CompuPro** system, DON'T CALL!!! READ THE MANUAL FIRST!!!

SWITCHES

DIP SWITCH S1

This switch is not used by either the CP/M-80 or the CP/M-86 BIOS, so we recommend that you turn all positions "OFF".

DIP SWITCH S2

This switch controls the port addressing and board selection number for the board. It should be set as described in the table below. These settings will put the INTERFACER 4 at ports 10-17H as users 4-7.

POSITION	LABELED	HOW TO SET IT
1	BS0	ON
2	BS1	ON
3	H/L	OFF
4	DIS	OFF
5	A7	ON
6	A6	ON
7	A5	ON
8	A4	OFF
9	A3	ON
10	-	ON (NOT USED)

DIP SWITCH S3

This switch should be set with positions 1-4 "ON", and positions 5-8 "OFF".

JUMPER SOCKETS

The jumper sockets should have either an 8 position shunt or an 8 position DIP header as indicated below.

JUMPER SOCKET

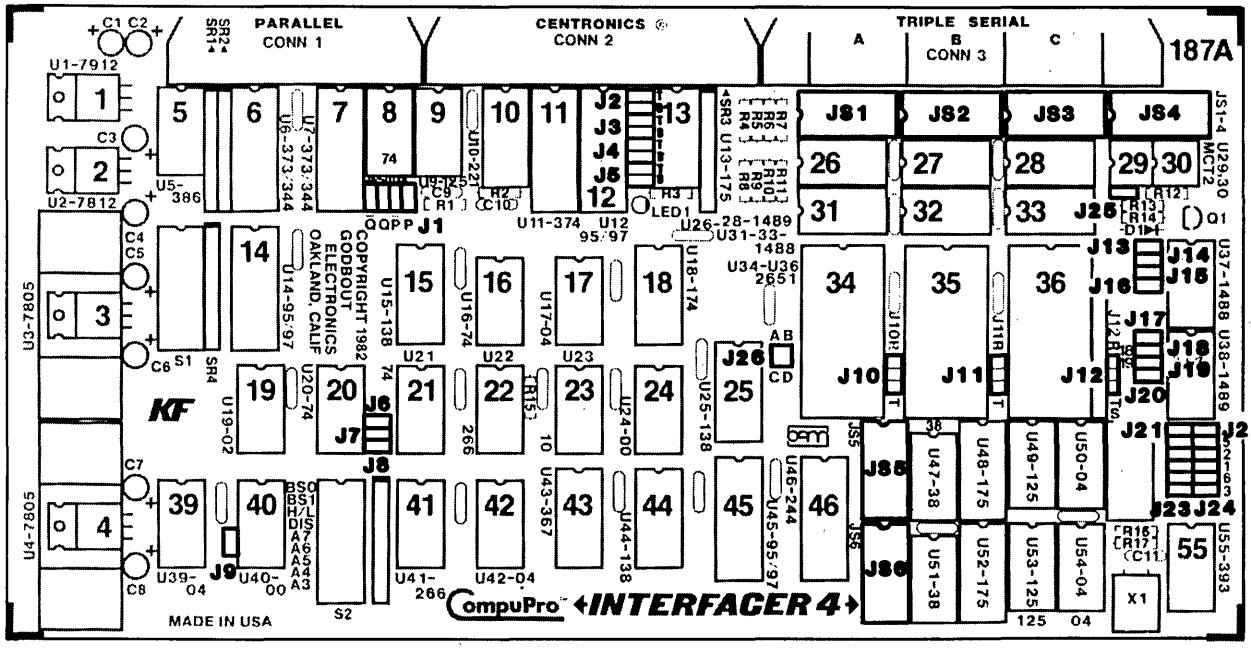
```
JS1 ---------- SHUNT INSTALLED
JS2 ---------- SHUNT INSTALLED
JS3 ---------- SHUNT INSTALLED
JS4 ---------- HEADER INSTALLED WITH NO WIRES
JS5 ---------- HEADER INSTALLED WITH NO WIRES
JS6 ---------- HEADER INSTALLED WITH NO WIRES
```

JUMPERS

The pin shunt jumpers should be installed or removed as indicated.

JUMPER	CONDITION
J1	NO PINS NEED TO BE INSTALLED
J2	BOTTOM INSTALLED WITH EPSON / NO SHUNT OTHERWISE
J3	TOP INSTALLED WITH EPSON / NO SHUNT OTHERWISE
J4	BOTTOM INTSALLED WITH BOTH EPSON AND CENTRONICS
J5	REMOVED
J6	INSTALLED FOR 1 WAIT STATE / REMOVED OTHERWISE
J7	INSTALLED FOR 2 WAIT STATES / REMOVED OTHERWISE
J8	INSTALLED FOR 3 WAIT STATES / REMOVED OTHERWISE
J9	NO JUMPER
J10-J25	REMOVED
J26	JUMPER A-B and C-D for the CENTRONICS CHANNEL as USER 4. JUMPER A-C and B-D for the CENTRONICS CHANNEL as USER 6.

DIAGRAM - JUMPER AND JUMPER SOCKET LAYOUT



NOTE: Under MP/M 8-16 or an interrupt driven mode, J26 MUST be jumpered A-B and C-D.

HARDWARE SECTION

ABOUT INTERFACER 4

Congratulations on your decision to purchase the INTERFACER 4 multi-purpose I/O board. INTERFACER 4 has been designed to be the most flexible and highest performance I/O interface available that fully complies with the IEEE 696/S-100 bus standard. Due to its provision for ready expansion and modification as the state of the computing art improves, the S-100 bus is the professional level choice for commercial, industrial, and scientific applications. We believe that this board, along with the rest of the S-100 portion of the CompuPro family, is one of the best boards available for that bus.

The INTERFACER 4 boasts several innovative features not found on currently available I/O boards. The primary innovation stems from its full software compatibility with the INTERFACER 3 as well as the ability to intermix INTERFACER 3 and 4 boards at the same port addresses. Additional features include 3 fully programmable asynchronous serial channels, 2 of which are capable of high speed synchronous transmission and one capable of current loop operation, five RS-232 handshaking lines per channel plus bi-directional clock drivers on both the synchronous channels, a pin compatible CENTRONICS parallel interface port with the full complement of handshaking lines, a universal parallel port with 16 data and 3 handshaking lines, expandability to 32 users with eight boards using only 8 port addresses, a flexible interrupt structure with full maskability and pending status on both transmit and receive interrupts, and conservative design for operation with most CPUs operating to beyond 10 MHz. Other features standard to all CompuPro boards include thorough bypassing of all supply lines to suppress transients, on-board regulators, and low power Schottky TTL and MOS technology integrated circuits for reliable, cool operation. All this and sockets for all IC's go onto a double sided, solder masked printed circuit board with a complete component legend.

TECHNICAL OVERVIEW

The INTERFACER 4 was designed for efficient operation in interrupt driven/ multi-user microcomputer systems as well as polled mode single user systems. Eight distinct interrupts are generated on-board by the three USARTs and two parallel ports, and these are brought out for jumpering by the user to the eight vectored interrupt lines on the S-100 bus. Since these interrupt lines are open collector, they may be configured to interrupt on any or all of the vectored interrupt lines. In addition, a transmit and receive interrupt mask port is provided for inhibiting unwanted interrupts.

The INTERFACER 4 provides multi-user operation with a minimum number of I/O ports by incorporating a user select register to activate the required I/O channel. This five bit register is used to select a particular channel, which allows up to 32 users (up to eight boards) on the same 8 port addresses. When a particular user is selected, the four USART registers associated with that specific serial channel or the parallel registers are made available for examination and alteration by the host processor or other temporary bus master. In addition, whenever a particular channel is selected, the interrupt registers on that particular board as well as the registers on another board in the same group of eight users are available for examination and alteration.

The typical sequence of operation would require all channels on the INTERFACER 4 to be mode initialized and the interrupt mask registers set for operation. All parameters of the USART or parallel ports may be altered by selecting that particular channel and writing a new set of mode and command words to the proper registers. If running in a non-interrupt environment, the interrupt status registers may be polled and checked in roughly the same manner as a standard single channel serial board.

All three of the serial channels on the INTERFACER 4 are designed for direct connection to DATA TERMINAL EQUIPMENT (DTE) or DATA COMMUNICATION EQUIPMENT (DCE) in asynchronous mode without alteration of the cables. This allows direct connection to all types of RS-232 equipment including modems. In addition, two channels are capable of high speed synchronous operation using internal or external clocks and one channel may be connected to current loop devices.

The CENTRONICS parallel channel was designed for direct connection to printers using standard ribbon cable connectors. In addition, all handshaking lines have been implemented for maximum flexibility and ease of interfacing.

PORT MAP

The INTERFACER 4 interface uses a block of eight port addresses for communication between it and the host processor. The address of the first port is switch selectable to any address which is a multiple of eight. The ports will be referred to as RELATIVE PORTS 0 - 7.

RELATIVE PORT	FUNCTION
0	USART / CENTRONICS / DIPSWITCH DATA-C Register (R/W)
1	USART / CENTRONICS STATUS-C Register (R) SYN1/SYN2/DLE Register / CENTRONICS CONTROL-C Reg. (W)
2	USART Mode Register / Parallel DATA-P Register (R/W)
3	USART Command Register / Parallel STATUS-P Register (R/W)
4	Transmit Interrupt Status Register (R) Transmit Interrupt Mask Register (W)
5	Receive Interrupt Status Register (R) Receive Interrupt Mask Register (W)
6	Not used
7	User Select Register (write only)

PORT ADDRESSING

DIP switch S2, positions 4 thru 9 are used to select the base address of the eight port block in a binary fashion as shown in the following table:

SWITCH POSITION	ADDRESS BIT	
4	PORT DISABLE WHEN "ON"	
5	A7	
6	A6	"ON" = "0"
7	A5	"OFF" = "1"
8	A4	
9	A3	

EXAMPLE: To address this board at addresses 10H thru 17H for the CompuPro CP/M-80 or CP/M-86 operating system or the Phase 1 OASIS operating system, position 4 and 8 would be "OFF" and positions 5 thru 7 and positions 9 would be "ON".

USER/BOARD SELECTION

To select a particular channel and to select which board that channel will be on (when running more than 4 users), requires the use of the User Select Port and three board select switches. The five bit User Select Register determines which of 32 possible users will be selected at a particular time. The two board select switches (S2-1 and S2-2) determine whether a board will respond to users 0 thru 7, 8 thru 15, 16 thru 23, and 24 thru 31 and the HIGH/LOW select switch (S2-3) determines whether the board is the high or low 4 users in a particular block of eight. A particular user (0-31) is selected by outputting the five bit number that represents that user. The diagram shown below describes the relation between the board select switches and the User Select Register.

USER SELECT REGISTER

DATA BIT	NAME	FUNCTION
D0	US0	USER SELECT 0 (LSB)
D1	US1	USER SELECT 1
D2	H/LS	HIGH/LOW SELECT
D3	BS0	BOARD SELECT 0 (LSB)
D4	BS1	BOARD SELECT 1 (MSB)
D5		NOT USED
D6		NOT USED
D7		NOT USED

Since each INTERFACER 4 will support 4 users, we will refer to these 4 as RELATIVE USERS 0-3. These 4 ports are physically configured with RELATIVE USER 0 as the CENTRONICS and Universal Parallel ports, RELATIVE USER 1 as the far right serial channel with current loop capabilities (CONN 3 C), RELATIVE USER 2 is the middle channel (CONN 3 C), and RELATIVE USER 3 as the far left channel (CONN 3 A).

To determine the EXACT USER number, the RELATIVE USER number must be added to the USER OFFSET number. The RELATIVE USER number corresponds to the 2 bits above called USER SELECT 0-1, and the USER OFFSET number corresponds to the 3 bits above called BOARD SELECT 0 and 1, and HIGH/LOW SELECT. These 5 bits determine the exact user number.

US1	US0	RELATIVE USER NUMBER	STANDARD CONFIGURATION
0	0	USER 0	CENTRONICS / PARALLEL
0	1	USER 1	RIGHT SERIAL CHANNEL
1	0	USER 2	MIDDLE SERIAL CHANNEL
1	1	USER 3	LEFT SERIAL CHANNEL

BOARD SELECT SWITCHES			BOARD SELECT BITS			USER
S2-3	S2-2	S2-1	H/LS	BS1	BS0	OFFSET
ON	ON	ON	0	0	0	0
OFF	ON	ON	1	0	0	4
ON	ON	OFF	0	0	1	8
OFF	ON	OFF	1	0	1	12
ON	OFF	ON	0	1	0	16
OFF	OFF	ON	1	1	0	20
ON	OFF	OFF	0	1	1	24
OFF	OFF	OFF	1	1	1	28

DATA BUS SELECT SWITCH S3

Switch S3 is used to steer either the high (D4-D7) or the low (D0-D3) nibble of status/control information to and from the interrupt logic on the INTERFACER 4. This switch was designed in to provide software compatibility with the INTERFACER 3 board.

When the INTERFACER 4 is addressed as EXACT USERS 0-3 + N, (where N is 0, 8, 16, or 24) we would like the low nibble (D0-D3) of status and control information to be used. This would require switch S3 to have positions 1-4 "OFF" and positions 5-8 "ON".

When the INTERFACER 4 is addressed as EXACT USERS 4-7 + N, (where N is 0, 8, 16, or 24) we would like the high nibble (D4-D7) of status and control information to be used. This would require switch S3 to have positions 1-4 "ON" and positions 5-8 "OFF".

NOTE!: SETTING SWITCH S3 DIFFERENTLY THAN DESCRIBED ABOVE WILL CAUSE IMPROPER BOARD OPERATION AND POSSIBLE BOARD DAMAGE!

EXAMPLE: To address the INTERFACER 4 to respond to EXACT USERS 4 thru 7 (the CompuPro standard), switches S2-1 and S2-2 would be "ON", and S2-3 would be "OFF". To select a particular user in the group from 4 to 7, BS1 (D4) and BS0 (D3) of the User Select Register must be "0", and H/LS (D2) must be "1" for the board to respond. Switch S3 must have positions 1-4 "ON" and 5-8 "OFF". To select EXACT USER 5, a 05H must be sent to the USER SELECT REGISTER.

EXAMPLE: To address the INTERFACER 4 to respond to users 16 thru 19, switch S2-1 and S2-3 would be "ON", and switch S2-2 would be "OFF". Switch S3 must have positions 1-4 "OFF" and 5-8 "ON". To select a particular user in the group from 16 to 19, BS1 must be a "1" , BS0 must be "0", and H/LS must be a "0" for the board to respond. To select EXACT USER 18, a 12H must be sent to the USER SELECT REGISTER.

RELATIVE USER 0 - 2 SWAP OPTION

The INTERFACER 4 may be configured so that RELATIVE USERS 0 and 2 may be swapped by re-jumpering J26. This will configure the CENTRONICS and UNIVERSAL Parallel channels as RELATIVE USER 2 instead of 0, and the middle serial channel as RELATIVE USER 0 instead of 2. This option allows EXACT USER 6 to be either a serial channel or the CENTRONICS channel for compatibility with the standard CompuPro CP/M BIOS. (This allows the LPT LIST device to be either serial or parallel without changing the BIOS.)

The standard configuration has "A" connected to "B", and "C" connected to "D" on J26. This provides the CENTRONICS as RELATIVE USER "0". To swap this, jumper "A" to "C", and "B" to "D" on J26, and the CENTRONICS channel will be RELATIVE USER 2 and the middle serial channel will be RELATIVE USER 0.

WAIT STATE SELECTION

The INTERFACER 4 was designed to run in very fast microcomputer systems by allowing up to three wait states to be added when accessing the USART/PARALLEL registers. Since the user select and interrupt control registers are capable of higher speed operation than the USART registers, no wait states are inserted even when they are enabled on the board.

The 3 sets of vertical pins (J6, J7, and J8) control the enabling of one, two, or three wait states. With the black pin shunt on J6, one wait state will be inserted. With the pin shunt on J7, two wait states will be inserted. With the pin shunt on J8, three wait states will be inserted. If the pin shunt is left removed, no wait states will be inserted.

NOTE: If multiple INTERFACER 4 boards are inserted, they should be set to the same number of wait states.

CABLES

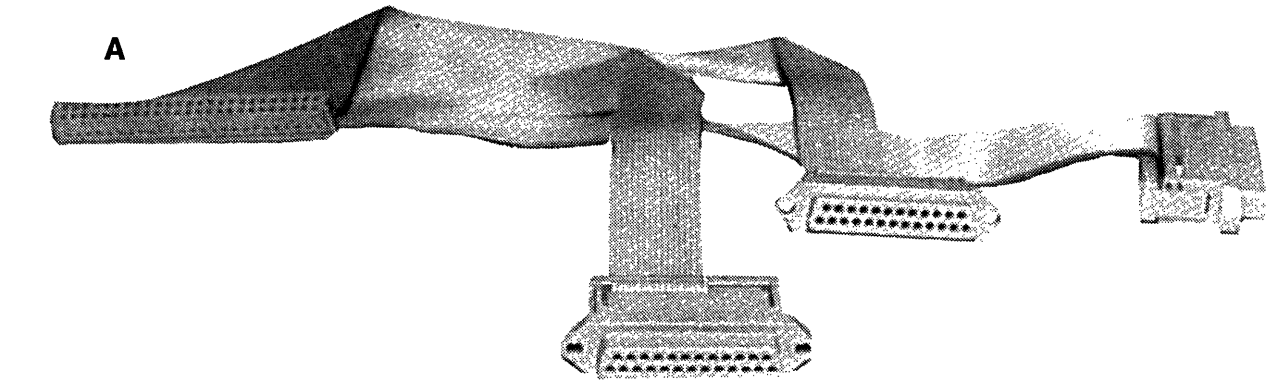
The INTERFACER 4 is designed to use 3 different cable assemblies. The serial channels use a custom 50 conductor cable that splits into three DB-25S connectors. The Universal Parallel channel uses a standard 26 conductor cable identical to those used on the INTERFACER 1 and INTERFACER 2, and the CENTRONICS Parallel channel uses a custom 40 pin cable that mates to a 36 pin "D" Shell connector for interfacing to the printer.

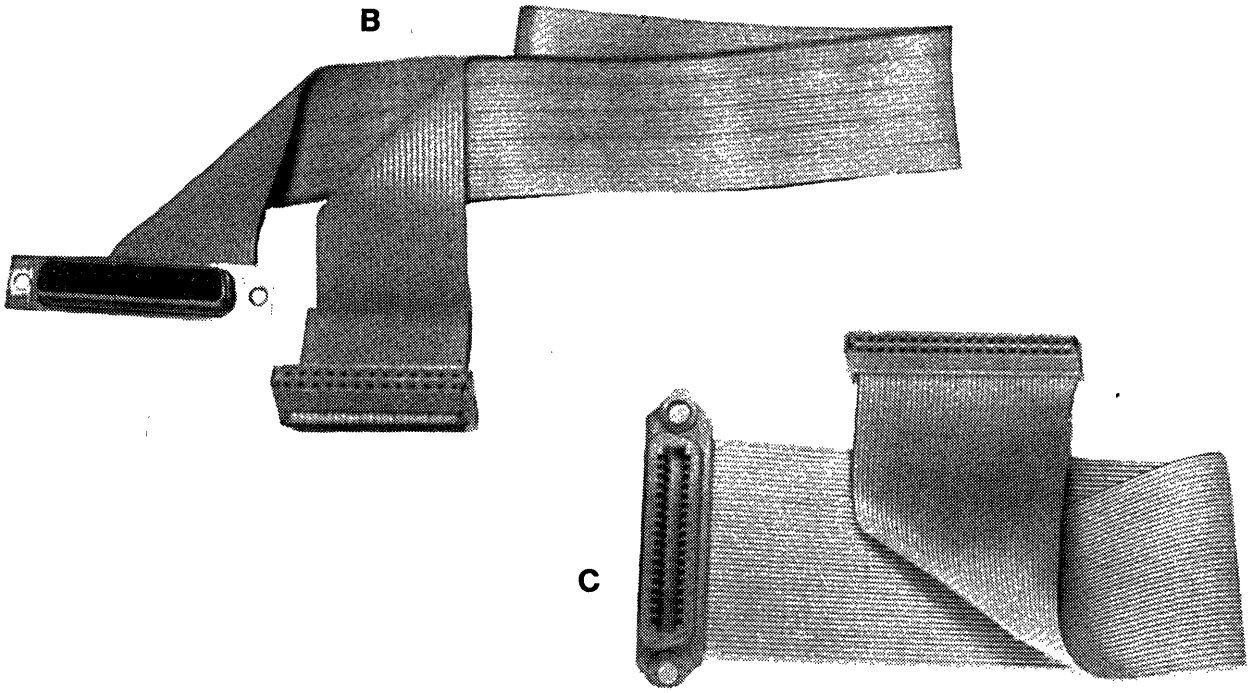
The serial channels (CONN 3, 50 pin connector on the far right) use a custom 3 user cable (see photo A page 12). This cable consists of a female 50 pin insulation displacement connector that splits into thirds and connects to three female DB-25 connectors. The actual cable has positions 1-16 (pin 1 on the far left side of the connector) on the first DB-25, positions 17-32 on the second DB-25, and positions 33-50 on the third DB-25. **NOTE:** The pin numbers on the circuit diagram show the pin numbers on the DB-25 connector and not the 50 pin connector.

The Universal Parallel channel (CONN 1, 26 pin connector on the far left) uses the CompuPro standard RS-232 I/O cables (see photo B page 12). This cable consists of a female 26 pin insulation displacement connector that mates to a

female DB-25 (the 26th conductor is not used). **NOTE:** The pin numbers on the circuit diagram show the pin numbers on the DB-25 connector and not the 26 pin connector.

The CENTRONICS Parallel channel (CONN 2, 40 pin connector in the middle of the board) uses another custom cable (see photo C page 12). This cable consists of a 40 pin female transition connector that mates with a 36 pin female "D" shell connector identical to those on the back of CENTRONICS interface printers. **NOTE:** The pin numbers on the circuit diagram show the pin numbers on the D-36 connector and not the 40 pin connector, and that pin 1 of the 40 pin connector does not correspond to pin 1 of the D-36 connector. If the user wishes to make this cable, the 36 conductors from the D-36 connector should be centered in the 40 pin connector, with 2 unused pins on each edge.





USING INTERRUPTS

The INTERFACER 4 has a simple but elegant interrupt structure that allows considerable flexibility. Each USART generates both a transmit and receive interrupt. The CENTRONICS Channel generates an interrupt upon receiving an ACKNOWLEDGE from the printer, and the Universal Parallel channel generates an interrupt after being STROBED by an external device for a total of 8 distinct interrupts for the board. A transmit interrupt indicates that the USART or the CENTRONICS transmit register is empty and it is ready to accept a character. A receive interrupt indicates that data is available from the receiver data register on either the USART or the Universal Parallel channel. Each of these interrupts may be masked "OFF" or "ON" by altering the INTERRUPT CONTROL REGISTERS as described below. Each of these interrupts are open collector, and may be individually tied to any of the 8 vectored interrupt lines (VI0-VI7). The status of each interrupt line may be sampled by reading the INTERRUPT STATUS REGISTERS as described below.

Since each of the 8 interrupts generated on the INTERFACER 4 may be tied to any of the 8 vectored lines, almost any type of priority scheme may implemented. All transmit interrupts are brought out twice on one side of jumper socket JS5, and all receive interrupts are brought out twice on one side of jumper socket JS6. On the opposite side of each socket, each of the 8 vectored interrupt lines are brought out. By using the provided headers, any USART interrupt may be connected to any VI line. The pin-out of JS5 and JS6 are shown below.

INTERRUPT	JS5		VI LINE	JS6		INTERRUPT
TxINT 0 -----	9	8	--- VI0 ---	8	9	----- RxINT 0
TxINT 1 -----	10	7	--- VI1 ---	7	10	----- RxINT 1
TxINT 2 -----	11	6	--- VI2 ---	6	11	----- RxINT 2
TxINT 3 -----	12	5	--- VI3 ---	5	12	----- RxINT 3
TxINT 0 -----	13	4	--- VI4 ---	4	13	----- RxINT 0
TxINT 1 -----	14	3	--- VI5 ---	3	14	----- RxINT 1
TxINT 2 -----	15	2	--- VI6 ---	2	15	----- RxINT 2
TxINT 3 -----	16	1	--- VI7 ---	1	16	----- RxINT 3

EXAMPLE: If we wish to generate an interrupt on vectored interrupt line VI3 when data becomes available from RELATIVE USER 3, a wire should be soldered between pins 5 and 12 of JS6.

EXAMPLE: If we wish to generate an interrupt on vectored interrupt line VI6 when data becomes available from RELATIVE USERS 0, 1, 2, and 3, a wire should be soldered to connect pins 1, 13,14,15, and 16 of JS6.

EXAMPLE: If we wish to generate an interrupt on vectored interrupt line VI0 when RELATIVE USER 2 is ready to accept a character, a wire should be soldered to connect pins 8 and 11 of JS5.

All serial channels are capable of generating a third interrupt called TxEMT/DSCHG*. This interrupt occurs when the transmitter has completed serialization of the last character loaded or a change has occurred in the state of the DSR or DCD RS-232 status lines. Additional information on this line may be found in the 2651 data sheet in this manual.

The TxEMT/DSCHG* output from the 2651 may be jumpered to generate either a transmit or receive interrupt. Due to the wire-OR capability of the interrupt outputs from the 2651, when jumpered, the transmit interrupt will become TxRDY OR TxEMT/DSCHG* or the receive interrupt will become RxRDY OR TxRDY/DSCHG*. Therefore, when jumpered, the user must check the status register to determine what condition caused the interrupt.

The following table will demonstrate where to install the shorting plug to generate the appropriate interrupt.

CHANNEL NUMBER	TO CAUSE A TxEMT/DSCHG TxRDY LINE	INTERRUPT ON THE: RxRDY LINE
1	INSTALL J10T	INSTALL J10R
2	INSTALL J11T	INSTALL J11R
3	INSTALL J12T	INSTALL J12R

INTERRUPT CONTROL REGISTERS

Two registers are provided for individually masking the transmit and receive interrupts from the bus. On power-up or reset, all interrupts are disabled on the INTERFACER 4. Alteration of the interrupt registers may be accomplished in groups of eight users for compatibility with the INTERFACER 4. To gain access to these registers, a user channel must be enabled in the particular group of 8 users. (You cannot alter any interrupt register on a pair of boards set for users 0 thru 7 unless you have selected one of those 8 users)

If an INTERFACER 4 is installed in a system where it is selected as EXACT USERS 0-3 + "N", where "N" is 0, 8, 16, or 24 (i.e. users 0-3, 8-11, etc.), a Transmit or Receive interrupt may be enabled by outputting a "1" to the proper bit of the appropriate register. The registers are configured so that Data Bit 0 will mask RELATIVE USER 0, D1 will mask RELATIVE USER 1, D2 will mask RELATIVE USER 2, and D3 will mask RELATIVE USER 3.

If an INTERFACER 4 is installed in a system where it is selected as EXACT USERS 4-7 + "N", where "N" is 0, 8, 16, or 24 (i.e. users 4-7, 12-15, etc.), a Transmit or Receive interrupt may be enabled by outputting a "1" to the proper bit of the appropriate register. The registers are configured so that Data Bit 4 will mask RELATIVE USER 4, D5 will mask RELATIVE USER 5, D6 will mask RELATIVE USER 6, and D7 will mask RELATIVE USER 7. This is true for both the Transmit Interrupt Control Register (relative port 4) and the Receive Interrupt Control Register (relative port 5).

EXAMPLE: To enable all Transmit Interrupts on a particular INTERFACER 4, you should send to relative port 4 either a 0FH if the board is selected as a 0-3 group or send a 0F0H if the board is selected as a 4-7 group.

EXAMPLE: To enable the Transmit Interrupt on relative users 1, 4 and 6 in a pair of INTERFACER 4 boards configured as a group of eight users, you should send a 52H to relative port 4.

EXAMPLE: To disable all Receive Interrupts on a particular INTERFACER 4 selected as a 4-7 group, you should send a 0FH to relative port 5.

EXAMPLE: To enable the Receive Interrupt on relative users 2, 3 and 7 in a pair of INTERFACER 4 boards, you should send a 8CH to relative port 5.

INTERRUPT STATUS REGISTERS

Two registers are provided for checking the status of pending transmit and receive interrupts. To gain access to these registers, a user channel must be enabled on the particular board or pair of boards in a group of eight users to be altered. The INTERFACER 4 board has the intelligence to allow you to read the interrupt status from a pair of boards simultaneously. (You cannot read any interrupt register on a pair of boards set for users 0 thru 7 unless you have selected one of those 8 users).

If a Transmit or Receive interrupt is pending, a "1" will be present in the proper bit of the status register. The registers are configured so that Data Bit 0 contains the status of EXACT USER 0+N, D1 contains the status of EXACT USER 1+N, and so on with D7 containing the status of EXACT USER 7+N, where N is 0, 8, 16, or 24. This is true for both the Transmit Interrupt Status Register (relative port 4) and the Receive Interrupt Status Register (relative port 5). Remember, these status registers are read only! Writing into these registers will alter the Interrupt Control Mask. In addition, the status of a channel's interrupts are available even if those interrupts are masked "OFF". The Interrupt Control Register does not affect the reading of the status from a register.

EXAMPLE: If all Transmit Interrupts on a particular pair of INTERFACER 4 boards are asserted, you will read a 0FFH at relative port 4.

EXAMPLE: If Transmit Interrupts are pending on EXACT USERS 1, 4 and 6 (+N), you will read a 52H from relative port 4.

EXAMPLE: If there are no Receive Interrupts pending on a single INTERFACER 4 in a system, (no data available), you will read either a 0F0H from relative port 5 if the board is set for EXACT USERS 0-3 (+N), or you will read a 0FH if the board is set for EXACT USERS 4-7 (+N). The reason for the nibble of value "F" is the processor will read binary "1"s from non-driven lines.

EXAMPLE: If Receive Interrupts are pending on EXACT USERS 2 and 3 (+N) with a single INTERFACER 4 in the system, you will read a 0FCH from relative port 5.

SERIAL INFORMATION SECTION

USART INITIALIZATION

The serial channels on the INTERFACER 4 are implemented with a 2651 type USART from either National Semiconductor or Signetics. Several of the USART parameters and channel control functions are programmed by writing into or reading from certain registers in the 2651. They are:

1. The baud rate.
2. The word length.
3. Whether or not a parity bit is generated.
4. Whether the parity is even or odd (if generated).
5. The number of stop bits.
6. Enabling and disabling the transmitter and receiver.
7. Setting and testing the RS-232 handshake lines.
8. Synchronous or asynchronous operation.

In addition, the normal status indication and data transfer functions are also handled through the USART's registers.

A table of the various registers and where they appear in the I/O port map is shown in a previous section and in the following tables.

"READ" or "INPUT" Ports

Relative Port Address	UART Register Function
00 hex	Data Port, read received data.
01 hex	Status Port, read UART status info.
02 hex	Mode Registers, read current UART mode.
03 hex	Command Register, read current command.

"WRITE" or "OUTPUT" Ports

Relative Port Address	UART Register Function
00 hex	Data port, write transmit data.
01 hex	SYN1/SYN2/DLE register, write sync bytes.
02 hex	Mode registers, write mode bytes.
03 hex	Command register, write command byte.

USART INITIALIZATION SEQUENCE

When bringing up the USART in asynchronous mode, the following sequence of events must occur:

1. Set Mode Register 1
2. Set Mode Register 2
3. Set Command Register
4. Begin normal USART operation

When bringing up the USART in transparent synchronous mode, all of the following sequence of events must occur. If bringing up the USART in non-transparent synchronous mode, step 5 may be omitted.

1. Set Mode Register 1
2. Set Mode Register 2
3. Set SYN1 Register
4. Set SYN2 Register
5. Set DLE Register
6. Set Command Register
7. Begin normal USART operation

DATA REGISTERS

The USART data registers are straight-forward in their operation. You write a byte to the data register when you want to transmit that byte to an external serial device and you read the byte in the data register to receive a byte from an external serial device. The USART will automatically add the proper start and stop bits when transmitting and will remove them when receiving.

STATUS REGISTER

The status register is used to determine the current state of the USART. Each bit of the status register has a different meaning depending on whether it is high or low. (High means a logic one or high level and low means a logic zero or low level.) The following table describes the meaning of the status bits:

STATUS REGISTER FORMAT TABLE

STATUS REGISTER FORMAT

BIT NUMBERS							
SR-7	SR-6	SR-5	SR-4	SR-3	SR-2	SR-1	SR-0
DATA SET READY 0 = $\overline{DSR}$ INPUT IS HIGH 1 = $\overline{DSR}$ INPUT IS LOW	DATA CARRIER DETECT 0 = DCD INPUT IS HIGH 1 = DCD INPUT IS LOW	FE/SYN DETECT ASYN: 0 = NORMAL 1 = FRAMING ERROR SYNC: 0 = NORMAL 1 = SYN CHARACTER DETECTED	OVERRUN 0 = NORMAL 1 = OVERRUN ERROR	PE/DLE DETECT ASYNC: 0 = NORMAL 1 = PARITY ERROR SYNC: 0 = NORMAL 1 = PARITY ERROR OR DLE CHARACTER RECEIVED	TxEMT/DSCHG 0 = NORMAL 1 = CHANGE IN $\overline{DSR}$ OR $\overline{DCD}$, OR TRANSMIT SHIFT REGISTER IS EMPTY	RxRDY 0 = RECEIVE HOLDING REGISTER EMPTY 1 = RECEIVE HOLDING REGISTER HAS DATA	TxRDY 0 = TRANSMIT HOLDING REGISTER BUSY 1 = TRANSMIT HOLDING REGISTER EMPTY

NOTE 1. BAUD RATE FACTOR IN ASYNCHRONOUS MODE APPLIES ONLY IF EXTERNAL CLOCK IS SELECTED. FACTOR IS 16x IF INTERNAL CLOCK IS SELECTED.

MODE REGISTERS

When bringing up the USART, its two mode registers must be set with various bit patterns that will determine the operating modes. Although there are two registers, they occupy only one I/O port address. This is accomplished with internal sequencing logic that allows you to write the first register (Mode Register 1) and then the second register (Mode Register 2). It is important to write to Mode Register 1 first.

The meanings of the various bits in the mode registers are described in the following tables:

MODE REGISTER 1 AND 2 FORMAT TABLES

MODE REGISTER 1 FORMAT

BIT NUMBERS

MR1-7	MR1-6	MR1-5	MR1-4	MR1-3	MR1-2	MR1-1	MR1-0
SYNC: NO. OF SYN CHARACTERS 0 = DOUBLE SYN 1 = SINGLE SYN ASYNC: STOP BIT LENGTH 00 = INVALID 01 = 1 STOP BIT 10 = 1½ STOP BITS 11 = 2 STOP BITS	SYNC: TRANSPARENCY CONTROL 0 = NORMAL 1 = TRANSPARENT	PARITY TYPE 0 = ODD 1 = EVEN	PARITY CONTROL 0 = DISABLED 1 = ENABLED	CHARACTER LENGTH 00 = 5 BITS 01 = 6 BITS 10 = 7 BITS 11 = 8 BITS		MODE AND BAUD RATE FACTOR[1] 00 = SYNCHRONOUS 1x RATE 01 = ASYNCHRONOUS 1x RATE 10 = ASYNCHRONOUS 16x RATE 11 = ASYNCHRONOUS 64x RATE	

MODE REGISTER 2 FORMAT

BIT NUMBERS

MR2-7	MR1-6	MR2-5	MR2-4	MR2-3	MR2-2	MR2-1	MR2-0
NOT USED		TRANSMITTER CLOCK 0 = EXTERNAL 1 = INTERNAL	RECEIVER CLOCK 0 = EXTERNAL 1 = INTERNAL	BAUD RATE SELECTION 0000 = 50 BAUD 0001 = 75 BAUD 0010 = 110 BAUD 0011 = 134.5 BAUD 0100 = 150 BAUD 0101 = 300 BAUD	0110 = 600 BAUD 0111 = 1200 BAUD 1000 = 1800 BAUD 1001 = 2000 BAUD 1010 = 2400 BAUD 1011 = 3600 BAUD	1100 = 4800 BAUD 1101 = 7200 BAUD 1110 = 9600 BAUD 1111 = 19200 BAUD	

That completes the description of the Mode Registers. Remember that you must always write both mode registers, with Mode Register 1 first.

COMMAND REGISTER

The Command Register is used to set the operating mode (sync or async), enable or disable the receiver and/or transmitter, force a "break" condition, reset the error flags and control the state of the RTS and DTR outputs.

COMMAND REGISTER TABLE

COMMAND REGISTER FORMAT

BIT NUMBERS

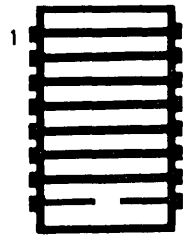
CR-7	CR-6	CR-5	CR-4	CR-3	CR-2	CR-1	CR-0
OPERATING MODE 00 = NORMAL OPERATION 01 = ASYNC: AUTOMATIC ECHO MODE SYNC: SYN AND/OR DLE STRIPPING MODE 10 = LOCAL LOOP BACK 11 = REMOTE LOOP BACK		REQUEST TO SEND 0 = FORCES $\overline{RTS}$ OUTPUT HIGH 1 = FORCES $\overline{RTS}$ OUTPUT LOW	RESET ERROR 0 = NORMAL 1 = RESET ERROR FLAG IN STATUS REGISTER (FE, OE, PE/DLE DETECT)	ASYNC: FORCE BREAK 0 = NORMAL 1 = FORCE BREAK SYNC: SEND DLE 0 = NORMAL 1 = SEND DLE	RECEIVE CONTROL (RxEN) 0 = DISABLE 1 = ENABLE	DATA TERMINAL READY 0 = FORCES $\overline{DTR}$ OUTPUT HIGH 1 = FORCES $\overline{DTR}$ OUTPUT LOW	TRANSMIT CONTROL 0 = DISABLE 1 = ENABLE

SERIAL MODE JUMPERS

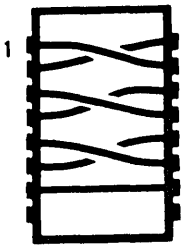
The **INTERFACER 4** board with its serial programming jumpers allows the user to adapt all three channels to all standard RS-232 pin configurations and Relative User 1 to standard current loop configurations. In RS-232 mode, these jumpers may be set so that this board operates in a "master" mode where it behaves as the Data Terminal Equipment (DTE), or it may be set so that the board operates in a "slave" mode where it behaves as the Data Communication Equipment (DCE). With almost all CRT terminals and serial interface printers, the **INTERFACER 4** serial mode jumpers (JS1-JS3) must be set in the "slave" or DCE mode. When connected to a Modem, the serial mode jumpers (JS1-JS3) of the **INTERFACER 4** should be set in the "master" mode as shown on the following table. In current loop mode on Relative User 1, JS3 should be removed and JS4 and J25 installed. The proper configuration of JS4 depends on whether the on-board or an off-board 20mA current source is used. The wiring of the mating DB-25 connector should have pins 14 and 15 as the + and - inputs, and 16 and 17 as the + and - outputs. For special applications, pins 18 and 19 of the DB-25 are TTL IN and OUT if pin 7 and 10, and 8 and 9 of JS4 are shorted.

PROGRAMMING JUMPERS

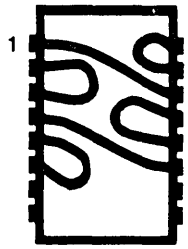
SLAVE MODE, JS1-JS3: for connections to CRT terminals, printers, etc.



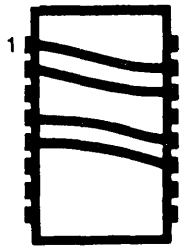
MASTER MODE, JS1-JS3: for connection to MODEMS.



CURRENT LOOP - on board current source, JS4: Example TTY.



CURRENT LOOP - external current source, JS4.



RS-232C CONTROL LINES

The RS-232 control and data lines are defined as shown below. The EIA RS-232 standard defines a signal line at greater than +3V (+12V typical) to be "SPACING" and a signal line at less than -3V (-12V typical) to be "MARKING".

PIN#	CIRCUIT	DIR.	NAME	DESCRIPTION
1	AA			PROTECTIVE GROUND
2	BA	TO DCE	TxD	TRANSMITTED DATA
3	BB	TO DTE	RxD	RECEIVED DATA
4	CA	TO DCE	RTS	REQUEST TO SEND
5	CB	TO DTE	CTS	CLEAR TO SEND
6	CC	TO DTE	DSR	DATA SET READY
7	AB			SIGNAL GROUND
8	CF	TO DTE	DCD	REC'D LINE SIGNAL DET.
15	DB	DCE SOURCE	TSET	TRANS. SIG. ELE. TIMING
17	DD	DCE SOURCE	RSET	REC'D SIG. ELE. TIMING
20	CD	TO DCE	DTR	DATA TERMINAL READY

Five RS-232 handshaking signals are provided for interfacing to equipment needing these lines as shown below. Output lines may be set either "MARKING" or "SPACING" and their state may be altered by software commands as described in the USART INITIALIZATION Section under Command Register.

USART HANDSHAKING LINES

	NAME	RS-232 LINE	DB25 PIN CONNECTION
OUTPUT LINES ---	DTR	CD	20 OR 6 *
	RTS	CA	4 OR 5 *
INPUT LINES ---	NAME	RS-232 LINE	DB25 PIN CONNECTION
	DSR	CC	6 OR 20 *
	CTS	CB	5 OR 4 *
	DCD	CF	8

* **NOTE:** Pin numbers with no asterisk indicate the DB25 pin number when the Serial Mode Jumpers are set for "master" mode. Pin numbers with an asterisk indicate the DB25 pin number when the Serial Mode Jumpers are set for "slave" mode.

SYNCHRONOUS MODE CLOCK DRIVER/RECEIVERS

RELATIVE CHANNELS 2 and 3 can either transmit or receive the synchronous timing element signals. The typical configuration requires that the DATA COMMUNICATION EQUIPMENT (DCE) be the source of the of the synchronous transmit and receive clocks. The INTERFACER 4 is capable of independently transmitting or receiving the sync clocks in either DCE or DTE modes.

For using either channel in a synchronous mode, there are two major options. The first option is whether or not you will be using the USART internal baud rate generator or the on-board high speed baud rate generators. The second option is whether you will be transmitting the sync clocks to the external device or receiving them from the external device. The following table will describe how each pin shunt should be set.

RELATIVE USER 2 SYNCHRONOUS MODE JUMPERS

INTERNAL BAUD RATE USE - LOW SPEED OPERATION

TRANSMITTING SYNC CLOCKS	RECEIVING SYNC CLOCKS
INSTALL J13, J16	INSTALL J15, J21

EXTERNAL BAUD RATE USE - HIGH SPEED OPERATION

TRANSMITTING SYNC CLOCKS	RECEIVING SYNC CLOCKS
INSTALL J13, J14 , J16 INSTALL J23 FOR DESIRED RATE	INSTALL J15, J21

RELATIVE USER 3 SYNCHRONOUS MODE JUMPERS

INTERNAL BAUD RATE USE - LOW SPEED OPERATION

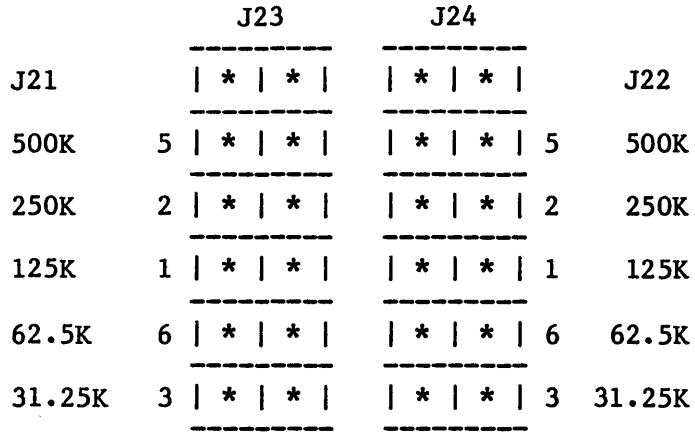
TRANSMITTING SYNC CLOCKS	RECEIVING SYNC CLOCKS
INSTALL J17, J20	INSTALL J19, J22

EXTERNAL BAUD RATE USE - HIGH SPEED OPERATION

TRANSMITTING SYNC CLOCKS	RECEIVING SYNC CLOCKS
INSTALL J17, J18 , J20 INSTALL J24 FOR DESIRED RATE	INSTALL J19, J22

SELECTING THE RATE OF THE ON-BOARD BAUD RATE GENERATOR

Either or both of the synchronous channels may use the on-board high speed baud rate generator for communication at rates greater than that available from the USART. The rates available on-board include 31.25K, 62.50K, 125K, 250K, and 500K baud, however, it is unlikely that 500K baud will be usable in most applications due to the slew rate limitations of the RS-232 drivers and receivers. The table below describes the jumper block that allows selection of these rates.



For relative user 2, jumper the proper rate across on J23.
For relative user 3, jumper the proper rate across on J24.

UNIVERSAL PARALLEL CHANNEL

TECHNICAL OVERVIEW

The UNIVERSAL PARALLEL section of the INTERFACER 4 consists of a full duplex latched parallel port for I/O data and one port for status. The use of TTL latches rather than a MOS parallel interface chip eliminates the need for mode selection and initialization, and allows the port to have strobe, attention and enable bits, an input interrupt, and 16 true data lines.

I/O ADDRESS ASSIGNMENT

The UNIVERSAL PARALLEL channel on the INTERFACER 4 board is addressed as the MODE and CONTROL registers of RELATIVE USER 0. The DATA-P register of the channel is addressed at the PORT BASE + 2 (USART equivalent is the MODE register), and the STATUS-P register is addressed at PORT BASE + 3 (USART equivalent is the CONTROL register). In the STATUS-P register only data bits 0 and 1 are significant.

STATUS-P REGISTER BIT ASSIGNMENT

Inputs to the processor from the STATUS-P register are defined as follows:

DATA BIT	NAME	SIGNAL
D0	DAV0	DATA AVAILABLE CHANNEL
D1	TKN0	DATA TAKEN CHANNEL
D2-D7	NOT USED	

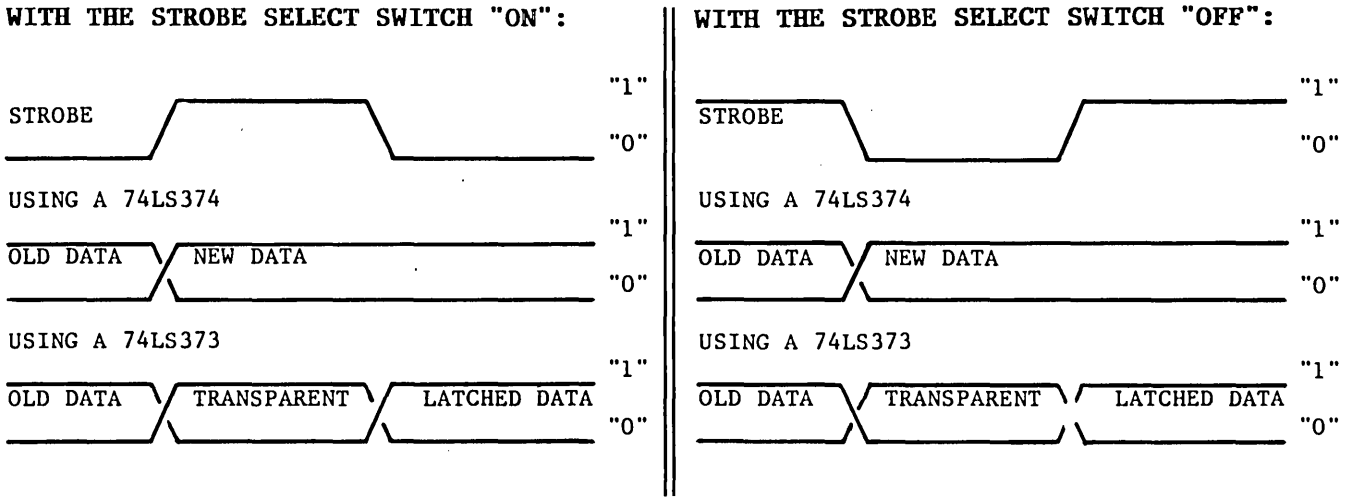
PORT CONTROL LINES - INPUT STROBE LINE

The STROBE line on the input Channel is used to latch the data into the input register when a 74LS374 or 74LS373 latch is used. This line also sets the status flag so that the processor can tell if data has been entered.

If a 74LS374 is used as the input register, a transition on the strobe line latches the data and sets the status flag. The strobe polarity select switch should be set as described below so that your data is valid during the transition. With the select switch (S1-2) ON, a low to high transition on strobe will latch the data. With the select switch OFF, a high to low transition on strobe will latch the data.

If a 74LS373 is used as the input register, the strobe line can assume two different modes. The first mode is similar to the latched mode of the 74LS374 described above except that during the strobe pulse the data is transparent through the latch to the processor. At the end of the strobe pulse, the data will be latched and stable for the processor to access. With the strobe select switch (S1-2) "ON", a positive going strobe pulse will latch the data at the end of the pulse. With the select switch "OFF", a negative going strobe pulse will latch the data at the end of the pulse. The second mode is the fully transparent mode where the data is never latched but is available for inputting at any time by the processor. This mode is useful whenever the data has no strobe

bit associated with it. This mode is entered when the strobe line is left open with the strobe select switch "ON". See the table below for strobing data.



INPUT EXAMPLES

Some examples of typical applications might include connecting a ASCII keyboard or a set of sense switches to the input Channel of the INTERFACER 4. A keyboard usually has a strobe line to indicate that it has current valid data on its lines. Therefore, using one of the 74LS374 latches would be best. The keyboard data lines would be connected accordingly to input data lines, and the strobe line would be connected, and the strobe select switch would be "ON" for a positive keyboard strobe, and "OFF" for a negative keyboard strobe. If connecting some sense switches to the input lines, a 74LS373 would be the best choice because there are usually no strobe lines associated with switches. The switches should be connected to the input lines so that they ground the inputs (no pullup resistors are needed since they are supplied on the board) and the STROBE LINE should be left floating with the strobe select switch "ON". This allows the processor to input the data from the switches at any time.

- OUTPUT ENABLE LINE

The OUTPUT ENABLE LINE on the Channel serves two functions depending on the user's configuration. In handshaking operations, it is used to enable the output of the DATA-P register which is normally tri-stated. This line also resets the ATTENTION bit and informs the processor, through the status port, that the data has been taken from the latch. In strobed operations, the OUTPUT ENABLE LINE is used to enable the output of the register at all times. When the select switch (S1-1) is "ON", the OUTPUT ENABLE LINE must be low to enable the outputs. With the select switch "OFF", the OUTPUT ENABLE LINE must be high to enable the output.

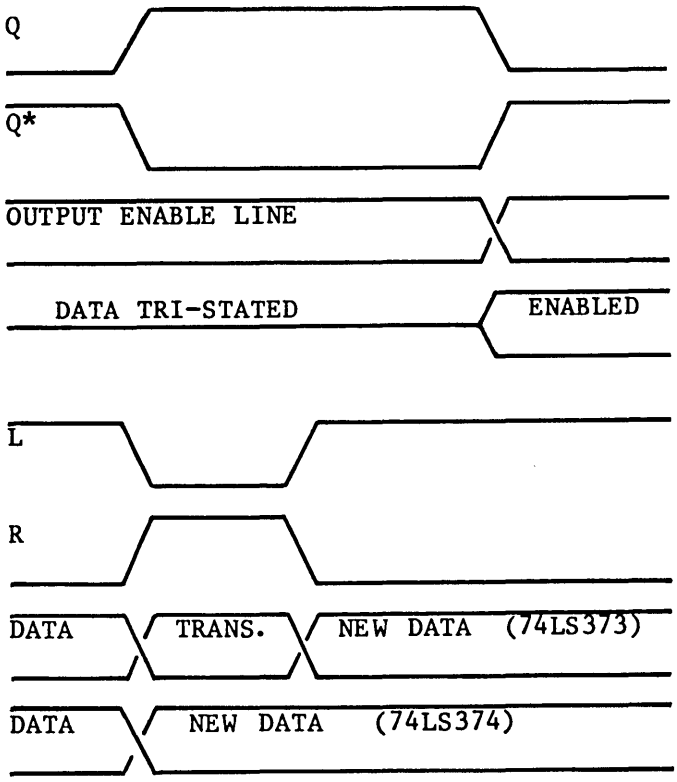
- ATTENTION LINE

The ATTENTION LINE is used to inform an external device that new data is now available for it. This line may be jumpered (J1) to provide any one of four different outputs. With the Common (top row of four pins) jumpered to either Q or Q*, and the OUTPUT ENABLE LINE set so that the output of the register is Tri-Stated, then the ATTENTION LINE will go high (Q) or low (Q*) when data is

strobed into the output register. When the OUTPUT ENABLE LINE level is changed to enable the data, then the ATTENTION LINE will return to its original level. In this mode, the OUTPUT ENABLE LINE is used to transfer the data out of the register and reset the attention flag. Since the level of the ATTENTION LINE may be sampled by the processor through the status port, a high speed handshaking data transfer can occur.

With the Common tied to either the "P" or the "P*", the ATTENTION LINE becomes a positive (P) or negative (P*) going strobe pulse with a width of the system pWR* strobe (between 150 and 1000ns). In this mode, the state of the OUTPUT ENABLE LINE should be set so that the data is enabled at all times. This mode is best used when the external device needs the data strobed into it. See the diagrams below for the output data timing using either a 74LS373 or a 74LS374 as an output register.

OUTPUT DATA TIMING



- OUTPUT EXAMPLES

Some examples of typical applications might include connecting an A to D converter or some LED's to the output lines. An A to D converter will probably require 8 data lines be connected in addition to a strobe line. In many cases, the strobe (P or P*) connected to the ATTENTION LINE will be sufficiently long for the converter and can be connected directly with the proper polarity for correct operation. If only 7 data lines are required for the converter, then the eighth data line may be used.

CENTRONICS STYLE PARALLEL CHANNEL

TECHNICAL OVERVIEW

The CENTRONICS PARALLEL section of the INTERFACER 4 consists of an 8 bit latched output port for data and a full complement of status and control lines. The output STROBE line timing conforms with the timing specifications of all known CENTRONICS interface printers, and power-up programming of the control lines allows flexible initialization procedures.

I/O ADDRESS ASSIGNMENT

The CENTRONICS PARALLEL channel on the INTERFACER 4 board is addressed as the DATA and STATUS registers of RELATIVE USER 0. The DATA-C register of the channel is addressed at the PORT BASE + 0 and the STATUS-C / CONTROL-C register is addressed at PORT BASE + 1.

STATUS-C REGISTER BIT ASSIGNMENT

Inputs to the processor from the STATUS-C register are defined as follows:

DATA BIT	NAME	SIGNAL
D0	PBMT	PRINTER BUFFER EMPTY - READY FOR CHARACTER WHEN HIGH
D1	NOT USED	ALWAYS LOGIC "0"
D2	ACKNLG	TRANSFER ACKNOWLEDGE - 10uS LOW PULSE
D3	PE	PAPER ERROR - PRINTER OUT OF PAPER WHEN HIGH
D4	ERROR	PRINTER ERROR WHEN HIGH
D5	ERROR	PRINTER ERROR WHEN HIGH
D6	SLCT	PRINTER SELECTED "ON" WHEN HIGH
D7	BUSY*	PRINTER BUSY WHEN LOW

The status register bit assignment was designed to minimize the amount of software alteration required to use a parallel printer. As configured, the status word should be compatible with most currently available BIOS routines. With this channel selected as EXACT USER 6, it is 100% compatible with standard CompuPro software.

CONTROL-C REGISTER BIT ASSIGNMENTS

Outputs to the CONTROL-C register from the processor are defined as follows:

DATA BIT	NAME	SIGNAL
D0	AFX	AUTO FEED EXTERNAL - AUTO LINE FEED AFTER RETURN
D1	INIT	INITIALIZE - INITIALIZE PRINTER
D2	SLCTIN	SELECT INPUT - PRINTER SELECT INPUT
D3	LED	LIGHT EMITTING DIODE - HIGH = ON
D4-D7	NC	NOT USED

CENTRONICS TRANSMIT INTERRUPT

The INTERFACER 4 comes configured to generate an interrupt upon receiving an ACKNOWLEDGE pulse from the printer indicating that it is ready to accept another byte of data. Provisions have been made to generate an interrupt upon the printer's change from BUSY to NOT BUSY. This may be accomplished by cutting the shorting trace at jumper J5 TOP, and installing a shorting plug on J5 BOTTOM.

CENTRONICS INTERFACE SIGNAL DESIGNATIONS

The following table describes the CENTRONICS cable pinout designations as defined by EPSON. There exist several minor differences between the CENTRONICS signal designations and those of EPSON. The EPSON designations are shown here because they are somewhat more complete. All differences will be marked with a "*" and explained below.

SIGNAL PIN #	GROUND PIN #	SIGNAL NAME	SIGNAL DESCRIPTION	
1	19	STROBE*	ACTIVE LOW DATA STROBE PULSE	
2	20	DATA 1	DATA BIT 1	
3	21	DATA 2	DATA BIT 2	
4	22	DATA 3	DATA BIT 3	
5	23	DATA 4	DATA BIT 4	
6	24	DATA 5	DATA BIT 5	
7	25	DATA 6	DATA BIT 6	
8	26	DATA 7	DATA BIT 7	
9	27	DATA 8	DATA BIT 8	
10	28	ACKNLG*	ACKNOWLEDGE PULSE ACTIVE LOW	
11	29	BUSY	PRINTER BUSY ACTIVE HIGH	
12	30	PE	PAPER ERROR ACTIVE HIGH	
13	--	SLCT	PRINTER "ON" WHEN HIGH	
14	--	AUTO FEED XT*	AUTO LINE FEED WHEN LOW	*
15	--	NC	NOT USED	*
16	--	0V	LOGIC GROUND LEVEL	
17	--	CHASGND	PRINTER CHASSIS GROUND	
18	--	NC	NOT USED	*
19-30	--	GND	GROUND RETURN LINES	
31	--	INIT*	PRINTER INITIALIZE WHEN LOW > 50 uS	
32	--	ERROR*	PRINTER ERROR WHEN LOW	
33	--	GND	GROUND	
34	--	NC	NOT USED	*
35	--	NC	NOT USED	*
36	--	SLCT IN*	PRINTER SELECT INPUT WHEN LOW	*

SIGNAL DIFFERENCES BETWEEN EPSON AND CENTRONICS

LINE 14 This line is defined as 0V or signal ground by CENTRONICS. J2 should be removed when used with a CENTRONICS Printer.

LINE 15 This line is designated as OSCXT by CENTRONICS. This is not a conflict.

LINE 18 This line is designated as +5V by CENTRONICS. This is not a conflict.

LINE 34 This line is designated LINE COUNT PULSE by CENTRONICS. This is not a conflict.

LINE 35 This line is designated as a ground return by CENTRONICS. This is not a conflict.

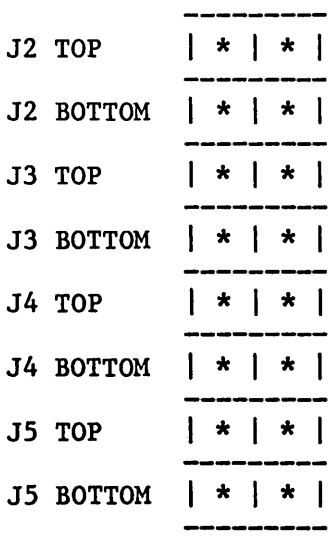
LINE 36 This line is not used by CENTRONICS, however, J3 should be removed when used with a CENTRONICS Printer.

NOTE: The user should always refer to the interface specifications of his printer before connecting it to the INTERFACER 4.

CENTRONICS CONTROL-C LINE JUMPERING

The printer control lines handled by the CONTROL-C register may be set to power-up either high or low by the proper setting of jumpers J2-J4. This allows the user to select the power-up condition of the printer independent of the initialization procedure used. Jumper J5 is not a CONTROL-C jumper, but controls whether the interrupt is generated on ACKNLG* or BUSY. It is included in this section because it is located in the same block of jumpers. The following section describes the position of the jumpers and their effects.

Jumpers J2-J5 are located in between U13 and U14, and above LED1, and are arranged in the following format.



JUMPER DESCRIPTION

J2 AUTO FEED XT* This signal controls whether the printer does an automatic line feed after receiving a "return".

J2 TOP Low on power-up when jumpered.
J2 BOTTOM High on power-up when jumpered.

J3	SLCT IN*	This signal enables the printer to receive data when Low. Printer disabled when High.
	J3 TOP	Low on power-up when jumpered.
	J3 BOTTOM	High on power-up when jumpered.
J4	INIT*	This signal initializes the printer controller when low for more than 50 uS. High normally.
	J4 TOP	Low on power-up when jumpered.
	J4 BOTTOM	High on power-up when jumpered.
J5	INTERRUPT	This jumper determines whether the CENTRONICS interrupt is generated from ACKNLG* or BUSY.
	J5 TOP	Interrupt on ACKNLG* - shorted as shipped on board.
	J5 BOTTOM	Interrupt on BUSY - MUST CUT TOP SHORT!

LIGHT EMITTING DIODE

LIGHT EMITTING DIODE LED1 is controlled by the CONTROL-C register bit D3, and may be turned "ON" or "OFF" when outputting to this port. The LED will always be "OFF" upon power-up or RESET, and may be turned "ON" by outputting a logic "1" to D3.

SENSE DIP SWITCH

By reading the DATA-C register, the state of DIP switch S1, positions 3-10 may be determined under program control. When read, an "ON" position will read as a "0", and an "OFF" position will be read as a "1". Positions 3 thru 10 correspond to DATA bits 7 thru 0 when read.

EXAMPLE: If a 0Fh is read, positions 3-6 are "ON", and positions 7-10 are "OFF".

NOTE: Maximum allowable length for the Centronics cable from enclosure to printer is six feet.

THEORY OF OPERATION

The INTERFACER 4 can be roughly divided into 9 subsections for describing its operation. These sections include: The S-100 Bus Drivers, the I/O Port Decode Logic, the Strobe Generation Logic, the Wait State Logic, the Interrupt Control/Status Logic, the USART, the RS-232/CURRENT LOOP Level Conversion Logic, The CENTRONICS Parallel Logic, and the Universal Parallel Logic.

S-100 BUS DRIVERS

The separate data input and output data buses of the S-100 bus are converted to a bi-directional data bus by octal drivers U45 and U46. Data from the S-100 bus is driven onto the internal data bus by U45 only when sOUT goes high, indicating an output operation. The internal data bus is driven onto the S-100 bus either as a high or low nibble, or as a full byte. When DOEN* goes low, indicating that valid board select (SEL) and pDBIN are high (NAND-U40), and A2 is low, both DOENL* and DOENH* go low and enable a full byte onto the bus. When A2 is high, either the high or low nibble is gated out onto the bus depending on the state of HSEL (U5, U24). This allows the interrupt status to be read from 2 boards at the same time, each suppling the proper nibble of data.

All S-100 bus signals are buffered onto the board if the line would otherwise have more than 1 LSTTL load. Address lines A0, A1, A2, and pDBIN are buffered onto the board by 2/3 of hex buffer U43, and the lines sOUT, sINP, pWR*, 0, and pSTVAL* are inverted using portions of U42

I/O PORT DECODE LOGIC

The eight port block that the INTERFACER 4 occupies is decoded by 6 open collector X-OR gates (U22 and U41). 5 of these gates decode address lines A3-A7 by comparing against positions 5-9 of switch S2, and the last section compares sOUT and sINP* to determine if an I/O operation is occurring. When all compare conditions are satisfied, ASEL goes high. Closing position 4 of S2 will ground ASEL and disable the board completely.

A valid board select (SEL*) is generated (by 1/3 of U23), when ASEL goes high along with USEL (indicating that this boards select number is active) and A1 and A2 are not both high (indicating the USER SELECT PORT is not selected). SEL* is disabled by 1/3 of U23 when the USER SELECT PORT is enabled so that conflicts between up to eight boards do not occur.

A USER SELECT write occurs when ASEL, A1, A2, sOUT, and STROBE go high. This generates OUT7* (U23) which clocks the least significant 5 bits on the bus (D0-D4) into hex latch U18. The 2 low order bits of U18 are decoded into 4 chip enables (CE0* - CE3*) by U25 when SEL is high, A2 and ESTROBE* are low, and SH/L* is low. Bit D2 (H/L*), is either buffered or inverted by X-OR U5 and S2-3. This signal is low if the board is selected and also indicates that a high or low nibble is to be read. The 2 high order bits of U18 are compared to switch positions 1 and 2 of S2 by 1/2 of U22 (X-NOR) to decode a current user board select signal USEL. Access to registers on the board requires that USEL be high before access is gained.

The four interrupt read and write strobes are generated by decoder U44 when A2 is high and SEL* and STROBE* are low. A0, A1, and sINP* determine which output becomes active at the proper time.

STROBE GENERATION LOGIC

In order to gain additional access time in an I/O cycle for the 2651 USARTs, the INTERFACER 4 generates early strobes based on valid status. S-100 bus strobes pDBIN and pWR* are gated together (U19) and inverted to generate STROBE and STROBE*. These signals indicate that a bus strobe is occurring. The interrupt registers and user select port have their data gated by STROBE because they are TTL and capable of very high speed operation. Since the 2651 type USART is a MOS device and has an access time of approximately 250 nS, an early strobe is generated so that wait states are avoided whenever possible. A status valid signal, ESTATVAL*, is generated whenever pSYNC is high and pSTVAL* is low. ESTATVAL* clears "D" flop U16a to generate ESTROBE*, which becomes one term of the USART chip enable decoder U25. The termination of STROBE* causes a "1" to be clocked into U16a and terminate ESTROBE*.

WAIT STATE LOGIC

To allow operation with high speed processors, a wait state generator allows the addition of 1, 2, or 3 wait cycles. U20a and U21 forms a 3 bit shift register clocked by ϕ*. A wait state is left pending after STROBE goes low, and when STALL1*, STALL2* or STALL3* and A2 are low (U19), and SEL is high (U40), WAIT* is generated. STALL1* is clocked out on the next rising edge of ϕ* after STROBE goes high, STALL2* is clocked out the following cycle and STALL3* is clocked out on the 3rd cycle. The pRDY* line is pulled low by U43 when WAIT* goes low. When neither J6, J7, OR J8 is connected, no wait states will be generated.

INTERRUPT CONTROL/STATUS LOGIC

The interrupt logic consists of two 4 bit latches for enabling interrupts onto the bus, two 4 bit buffers for reading current interrupt status, and eight 2 input open collector NAND buffers for driving the interrupts on the bus.

Two 4 bit latches (U48, U52) are used for generating the interrupt enable mask. The Q outputs become the RxINTENx and TxINTENx interrupt enables for selectively masking "OFF" individual interrupts. Upon power-up or reset, these latches are cleared by CLR* so that all interrupts are disabled.

The TxRDY and RxRDY interrupt outputs from the 2651 USARTs are inverted to form active high interrupt signals. The CENTRONICS Parallel and Universal Parallel channels generate active high interrupts automatically. These interrupt signals are fed to one input of the open collector NAND buffer (U47, U51), with the corresponding interrupt enable fed to the other input. The resulting interrupt outputs (TxINTx and RxINTx) are capable of driving the VIO-7 lines directly, and are brought out to JS5 and JS6 for jumpering to the appropriate line.

Two 4 bit buffers are formed from two quad tri-state buffers (U49, U53) for

gating the current USART and parallel interrupts (TxRDYx and RxRDYx) onto the bus as status information. Since the buffers use Tx and Rx RDY instead of Tx and Rx INT lines, the status of disabled as well as enabled interrupts are displayed.

Relative channels 1, 2, and 3 allow jumpering the TxEMT/DSCHG interrupt from the USART to either the TxRDY or RxRDY interrupt outputs. This is possible since the outputs from the 2651 are open drain and may be wire-ORed.

USARTS

The 2651 type USART is quite sophisticated in that it can run in both asynchronous as well as synchronous modes. In addition, the part has an internal baud rate generator, RS-232 status and control bits, up to 3 interrupt outputs, and the capability of transmitting as well as receiving baud clocks.

The chip enable (CE) and read/write (R*/W) lines are operated by initially determining whether a read or a write will occur (sINP* to R*/W) and then strobing the part with CE*. Address lines A0 and A1 determine which of four registers will be selected and CLR resets the USART.

The baud rate clock BAUDCLK is generated by a 5.0688 MHz crystal oscillator formed from 3 inverters (U54) and crystal X1.

RS-232/CURRENT LOOP LEVEL CONVERSION LOGIC

Each USART has a full complement of RS-232 handshaking lines for devices that require them. Industry standard 1488 and 1489 receivers and transmitters are used throughout for highest performance. In addition to the data lines TxD and RxD, each channel has a RTS and DTR output and a CTS, DSR, and DCD input. All three RS-232 status lines have pullup resistors to +12V so that floating inputs are pulled high.

Relative Users 2 and 3 are capable of sending and receiving both the transmit and receive baud clocks for running in synchronous mode. An RS-232 driver and a receiver are provided for RxC and TxC, and either one may be jumpered in. In addition, a dual 4 bit counter (U55) is used to divide the 2 MHz bus clock down to 31.25 KHz to 500 KHz for running the USARTs faster than their internal baud rate generators provide. Flexible jumpering allows either or both channels to run at the higher rates.

Relative user 1 may be set to run in current loop mode by appropriately jumpering JS4. Optical isolators U29 and U30 are used if isolation is required. R4 provides the current source for U29, whose output is inverted (U54), and then converted to RS-232 by the free section of U33. This output may be jumpered to pin 2 of JS3 by J25. Transmit data (TxD) is inverted (U54), isolated (U30), and buffered by Q1 for which R8 is the current source.

CENTRONICS Parallel Logic

The CENTRONICS Parallel logic consists of an octal data latch, a quad control latch, an octal status buffer, an octal status buffer with a DIP switch,

a strobe one-shot, and a control strobe decoder. Decoder (U15) generates eight separate control strobes for both the CENTRONICS parallel logic and the Universal parallel logic. Depending on A0, A1, and sINP*, the 8 strobes are generated when STROBE* and CPE* are low. The output data register (U11) is clocked by inverted DWR* and latches 8 data bits off the internal data bus. The data strobe is provided by dual one-shot U10, which when strobed by DWR*, generates a 1 uS delay and then a 1 uS data strobe to accommodate all known data set-up and strobe length times. Printer status is gated onto the internal data bus by octal buffer U12 when SRD* strobes low. The status word is arranged similarly to the status register of the 2651 USART to facilitate software compatibility. Quad control register U13 latches the 4 low order data bits off the internal data bus when SWR* strobes low, and is cleared on reset for a known power-up state. Jumpers J2, J3, and J4 allow either Q or Q* to control the printers AUTO FEED XT*, INIT*, and SLCT IN* lines for any power-up state that can be altered under software control. The LED is controlled by bit D3 and Q* so that it is off after reset. Sense DIP switch S1 positions 3-10 are buffered (U14) onto the internal data bus when DRD* is strobed low. The CENTRONICS interrupt TxI0 is generated at the end of an ACKNLG* pulse from the printer, and is cleared when new data is written to the data register (DWR*). Jumper J5 allows the interrupt to be generated by BUSY if required.

Universal Parallel Logic

The Universal Parallel logic consists of 2 octal data registers, 2 "D" type flip flops, 3 X-OR gates and 2 status buffers. Output data is latched from the internal data bus by U7 when MWR* strobes low. MWR* also sets flop U8b which with J1 provides the attention level or pulse, and the DNTKN status bit 1 flag. When the data register is brought active by ENABLE through U5, the attention level and DNTKN flag are cleared. Input data is latched into U6 when STROBE is pulsed through U5. This also clocks a "1" into U8b, which generates the RxI0 interrupt, and sets the DAV status bit 0 flag. Input data is gated onto the internal data bus when MRD* strobes low, and the interrupt and DAV status is cleared.

SOFTWARE SECTION

SAMPLE PROGRAM FOR USING THE INTERFACER 4 AS THE CP/M CONSOLE

```
;       CompuPro INTERFACER 4 support routines

GBI3:   EQU     10h             ;INTERFACER 4 Base address
GBI3D:  EQU     GBI3+0          ;Uart data location
GBI3S:  EQU     GBI3+1          ;Uart status
GBI3M:  EQU     GBI3+2          ;Uart mode register
GBI3C:  EQU     GBI3+3          ;Uart command register
GBI3U:  EQU     GBI3+7          ;Uart select register

GBI3DV: EQU     00000010b       ;INTERFACER 4 Data Available
GBI3MT: EQU     00000001b       ;INTERFACER 4 Transmit Buffer Empty
GBI3DS: EQU     10000000b       ;INTERFACER 4 Data Set Ready
CON:    EQU     7               ;INTERFACER 4 Console Select
PRN:    EQU     6               ;INTERFACER 4 Printer Select
ULS:    EQU     5               ;INTERFACER 4 UL1 Select

;       C O N S O L E   I N I T I A L I Z A T I O N
;
;       This routine performs the initialization required by the INTERFACER 4.
;

I3INIT:
        MVI     A,CON           ;Console select
        OUT     GBI3U           ;Select Uart 7
        MVI     A,11101110b     ;Async, 16x, 8 bits, no parity, even, 2 stops
        OUT     GBI3M           ;Set up mode register 1
        MVI     A,01111110b     ;9600 baud
        OUT     GBI3M           ;Set up mode register 2
        MVI     A,00100111b     ;Trans. on, dtr low, rec. on, no break,
                                ;       no reset, rts low
        OUT     GBI3C           ;Set up command port

        MVI     A,PRN           ;Printer Select
        OUT     GBI3U           ;Select Uart 0
        MVI     A,11101110b     ;Async, 16x, 8 bits, no parity, even, 2 stops
        OUT     GBI3M           ;Set up mode register 1
        MVI     A,01111110b     ;9600 baud
        OUT     GBI3M           ;Set up mode register 2
        MVI     A,00100111b     ;Trans. on, dtr low, rec. on, no break,
                                ;       no reset, rts low
        OUT     GBI3C           ;Set up command port

        MVI     A,ULS           ;User list 1 Select
        OUT     GBI3U           ;Select Uart 0
        MVI     A,11101110b     ;Async, 16x, 8 bits, no parity, even, 2 stops
        OUT     GBI3M           ;Set up mode register 1
        MVI     A,01111110b     ;9600 baud
        OUT     GBI3M           ;Set up mode register 2
        MVI     A,00100111b     ;Trans. on, dtr low, rec. on, no break,
                                ;       no reset, rts low
```

```
        OUT     GBI3C           ;Set up command port
        RET

;       C O N S O L E   S T A T U S
;
;       This routine samples the Console status and returns the following
;       values in the A register.
;
;       EXIT    A = 0 (zero), means no character
;               currently ready to read.
;
;               A = FFh (255), means character
;               currently ready to read.

I3CONST:
        MVI     A,CON
        OUT     GBI3U
        IN      GBI3S           ;Input from port
        ANI     GBI3DV          ;Mask data available
        RZ                      ;If data not available
        ORI     0FFH
        RET


;       C O N S O L E   I N P U T
;
;       Read the next character into the A register, clearing the high
;       order bit.  If no character currently ready to read then wait for a
;       character to arrive before returning.
;
;       EXIT    A = character read from terminal.

I3CONIN:
        MVI     A,CON
        OUT     GBI3U
        IN      GBI3S           ;Get status from uart
        ANI     GBI3DV
        JZ      I3CONIN
        IN      GBI3D
        ANI     7Fh
        RET


;       C O N S O L E   O U T P U T
;
;       Send a character to the console.  If the console is not ready to
;       receive a character wait until the console is ready.
;
;       ENTRY   C = ASCII character to output to console.

I3CONOUT:
        MVI     A,CON
        OUT     GBI3U
        IN      GBI3S           ;Get uart status
        ANI     GBI3MT          ;Test if buffer empty
```

```
        JZ      I3CONOUT
        MOV     A,C
        OUT     GBI3D
        RET
;
;       L i s t   O u t p u t.
;
;       Send a character to the list device.  If the list device is not ready
;       to receive a character wait until the device is ready.
;
;       ENTRY   C = ASCII character to be output.

I3LIST: LDA     IOBYTE          ;Get IOBYTE status
        ANI     0C0H            ;Check for UL1:
        SUI     0C0H
        MVI     A,ULS
        JZ      I3UL1
        MVI     A,PRN
I3UL1:  OUT     GBI3U
I3LST1: IN      GBI3S
        ANI     GBI3MT+GBI3DS
        SUI     GBI3MT+GBI3DS
        JNZ     I3LST1
        MOV     A,C
        OUT     GBI3D
        RET
;
;       L i s t   S t a t u s.
;
;       Return the ready status for the list device.
;
;       EXIT    A = 0 (zero), list device is not ready to
;               accept another character.
;               A = FFh (255), list device is ready to accept
;               a character.

I3LST:  LDA     IOBYTE
        ANI     0C0H            ;Check for UL1:
        SUI     0C0H
        MVI     A,ULS
        JZ      I3LS1
        MVI     A,PRN
I3LS1:  OUT     GBI3U
        IN      GBI3S
        ANI     GBI3MT+GBI3DS
        SUI     GBI3MT+GBI3DS
        MVI     A,0FFH
        RZ
        XRA     A
        RET
```

CENTRONICS TEST PROGRAM

```
; 3/25/82

;*              CENTRONICS TEST PROGRAM
;*
;*   This program will output all standard ASCII characters to the printer
;*   along with the EPSON graphics characters controlled by bit 8.  The
;*   program will stop when any key is hit on the console.  The printer
;*   is required to be USER 4 at ports 10-17.  J2, J3, and J4 should be on
;*   the top pair of pins with an EPSON.  J2 and J3 should be removed
;*   entirely with a CENTRONICS printer.
;*
base    equ     10h
udata   equ     BASE+0h ;data port in and out
ustat   equ     BASE+1h ;status register port
mode    equ     BASE+2h ;mode register port
commr   equ     BASE+3h ;command register port
txreg   equ     BASE+4h ;tx int register
rxreg   equ     BASE+5h ;rx int register
user    equ     BASE+7h ;port to select user
exit    equ     0       ;CP/M reentry point
tbmt    equ     01h     ;transmitter buffer empty
dav     equ     02h     ;data available
cr      equ     0dh     ;carr. return
lf      equ     0ah     ;line feed
*
*
*
        org     100h
start1  call    setup   ;setup message area
start2  call    start   ;init user
line1   lxi     h,msg1  ;point to message
        call    print   ;print message
        lxi     h,msg3  ;point
        call    print   ;print
        lxi     h,msg4  ;point
        call    print   ;print
        lxi     h,msg5  ;point graphics
        call    print   ;print graphics
        mvi     c,0bh   ;check
        call    0005h   ;  console
        cpi     00h     ;    status
        jz      start2  ;for entry
        jmp     0       ;exit

Start   mvi     a,04H   ;init CENTRONICS
        out     user    ;select uart
        mvi     a,0ffh  ;interrupts enable
        out     txreg   ;transmit int enabled
        out     rxreg   ;receive enabled
        mvi     a,0bh   ;init centronics
        out     ustat   ;out
        ret
```

```
setup   lxi     h,msg3  ;point to buffer
        mvi     a,20h   ;init
sloop   mov     m,a     ;put byte
        inr     a       ;next up
        inx     h       ;next loc
        cpi     40h     ;beyond last char
        jz      done1   ;
        jmp     sloop   ;again
done1   mvi     a,cr    ;carrage return
        mov     m,a     ;
        inx     h       ;
        mvi     a,1f    ;line feed
        mov     m,a     ;
        inx     h       ;
        mvi     a,0     ;null
        mov     m,a     ;place
setup1  lxi     h,msg4  ;point to buffer
        mvi     a,40h   ;init
sloop1  mov     m,a     ;put byte
        inr     a       ;next up
        inx     h       ;next loc
        cpi     7eh     ;beyond last char
        jz      done2   ;
        jmp     sloop1  ;again
done2   mvi     a,cr    ;carrage return
        mov     m,a     ;
        inx     h       ;
        mvi     a,1f    ;line feed
        mov     m,a     ;
        inx     h       ;
        mvi     a,0     ;null
        mov     m,a     ;place
setup2  lxi     h,msg5  ;point to buffer
        mvi     a,0A0h  ;init
sloop2  mov     m,a     ;put byte
        inr     a       ;next up
        inx     h       ;next loc
        cpi     0E0h    ;beyond last char
        jz      done3   ;
        jmp     sloop2  ;again
done3   mvi     a,cr    ;carrage return
        mov     m,a     ;
        inx     h       ;
        mvi     a,1f    ;line feed
        mov     m,a     ;
        inx     h       ;
        mvi     a,0     ;null
        mov     m,a     ;place
        ret
print   call    start   ;select user
        call    instat  ;check status
        mov     a,m     ;get byte
        cpi     0       ;is it a null?
        rz              ;done
        out     udata   ;output data
```

```
        inx     h       ;next byte
        jmp     print   ;again

instat  in      ustat   ;get status
        cpi     0c5h    ;check all ok?
        jnz     instat  ;loop not ready
        ret
msg1    db      cr,lf,lf
        db      'This is a test of the INTERFACER 4 CENTRONICS port'
        db      cr,lf,lf
        db      0
msg2    db      cr,lf,lf
        db      0
msg3    ds      100h
msg4    ds      100h
msg5    ds      100h
        end
```

INTERFACER 4 SERIAL TEST PROGRAM

```
;*              INTERFACER 4 SERIAL TEST PROGRAM
;*
;*     This program will initialize 2651s for asynchronous operation at
;*     9600 baud with 8 data bits, one stop bit, no parity.  If the sense
;*     switch position 10 is "ON", RELATIVE USER 1 will run at 110 baud for
;*     current loop testing.  This program will echo all characters
;*     received on any user channel (from 0 to 31 except the CENTRONICS
;*     PORT) and if any user sends a ^C, the program will terminate and
;*     return back to CP/M.
;*
base    equ     10h
udata   equ     BASE+0h ;data port in and out
ustat   equ     BASE+1h ;status register port
mode    equ     BASE+2h ;mode register port
commr   equ     BASE+3h ;command register port
txreg   equ     BASE+4h ;tx int register
rxreg   equ     BASE+5h ;rx int register
user    equ     BASE+7h ;port to select user
exit    equ     0       ;CP/M reentry point
tbmt    equ     01h     ;transmitter buffer empty
dav     equ     02h     ;data available
*
*
*
        org     100h
fs      mvi     a,0     ;first board
        out     user    ;select
        mvi     a,0ffh  ;interrupts on
        out     txreg   ;enable transmit int
        out     rxreg   ;enable receive int
Start   mvi     a,0ffh  ;init user
Loop    inr     a       ;next user
        cpi     20H     ;check for final uart
        jz      echo    ;start echo routine
usel    out     user    ;select uart
        mov     b,a     ;save user in b
        ani     3       ;mask for centronics
        cz      cinit   ;sense I-loop
        call    init    ;init the uart
        mov     a,b     ;restore user
        jmp     loop    ;next
Cinit   in      udata   ;get sense switch
        ani     1       ;bit 0
        jz      iloop   ;110 baud
        mvi     e,7Eh   ;9600 baud
nu      mov     a,b     ;resore user
        inr     a       ;next user
        mov     b,a     ;save user
        out     user    ;select next user
        ret             ;init usart 9600
iloop   mvi     e,72h   ;110 baud
```

```
        jmp     nu      ;next user
Init    mvi     a,0CEh  ;set up the 2651
        out     mode    ;send to mode register 1
        mov     a,e     ;get baud value
        out     mode    ;SEND BYTE TO M.R. 2
        mvi     a,27h   ;could be 07h (no 1420)
        out     commr
        mvi     e,7eh   ;reset 9600
        ret
Echo    mvi     a,0FFh  ;mask value
        out     txreg   ;set tx int reg
        out     rxreg   ;set rx int reg
Loop1   inr     a       ;next user
        out     user    ;select uart
        mov     b,a     ;save user in b
        call    cstat   ;check for data
        cpi     0AAh    ;data if aa
        cz      ok      ;do echo loop
        mov     a,b     ;restore user
        jmp     loop1   ;next
Ok      call    inloop  ;get data
        call    oloop   ;output data
        ret
Cstat   in      ustat   ;look for key entry
        ani     dav     ;check status
        jz      nodat   ;no data
        mvi     a,0AAh  ;data char
        ret
Nodat   mvi     a,0     ;no data char
        ret
Inloop  in      ustat   ;look for key entry
        ani     dav     ;check the status
        jz      inloop  ;wait for key entry
        in      udata   ;get key entry
        ani     7Fh     ;mask parity off
        cpi     03h     ;has a ^c been hit?
        jz      done    ;return to CP/M
        mov     e,a     ;save input in E reg.
        ret
Oloop   in      ustat   ;check ready for output
        ani     tbmt    ;check status
        jz      oloop   ;wait for ready
        mov     a,e     ;get data
        out     udata   ;output character
        ret
Done    jmp     exit    ;return to cp/m
        end
```

INS2651 PROGRAMMABLE COMMUNICATIONS INTERFACE

National Semiconductor

October 1980

INS2651 Programmable Communications Interface

General Description

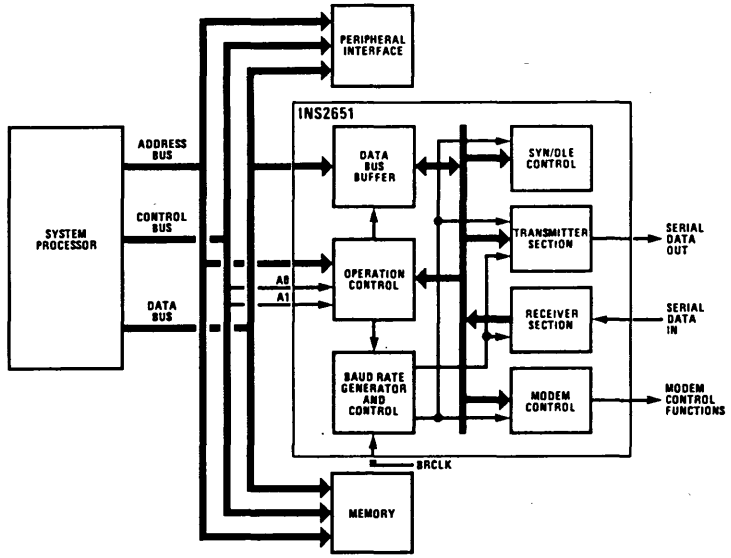
The INS2651 is a programmable Universal Synchronous/Asynchronous Receiver/Transmitter (USART) chip contained in a standard 28-pin dual-in-line package. The chip, which is fabricated using N-channel silicon gate MOS technology, functions as a serial data input/output interface in a bus structured system. The functional configuration of INS2651 is programmed by the system software for maximum flexibility, thereby allowing the system to receive and transmit virtually any serial data communications signal presently in use.

The INS2651 can be programmed to receive and transmit either synchronous or asynchronous serial data. The INS2651 performs serial-to-parallel conversion on data characters received from an input/output device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the INS2651 at any time during the functional operation. Status information reported includes the type and the condition of the transfer operations being performed by the INS2651, as well as error conditions (parity, overrun, or framing).

Features

- Synchronous and Asynchronous Full Duplex or Half Duplex Operations
- Synchronous Mode Capabilities
  - Selectable 5- to 8-Bit Characters
  - Selectable 1 or 2 SYNC Characters
  - Transparent or Non-Transparent Mode
  - Automatic SYNC or DLE-SYNC Insertion
  - SYNC or DLE Stripping
- Asynchronous Mode Capabilities
  - Selectable 5- to 8-Bit Characters
  - 3 Selectable Clock Rates (1x, 16x, or 64x the Baud Rate)
  - Line Break Detection and Generation
  - 1-, 1½-, or 2-Stop Bit Detection and Generation
  - False Start Bit Detection
- Baud Rates
  - DC to 0.8 M Baud (Synchronous)
  - DC to 0.8 M Baud (1x, Asynchronous)
  - DC to 50 k Baud (16x, Asynchronous)
  - DC to 12.5 k Baud (64x, Asynchronous)
- Internal or External Baud Rate Clock
  - 16 Internal Rates (50 to 19,200 Baud)
- Double Buffering of Data
- TTL Compatible
- No System Clock Required
- Direct Plug-In Replacement for Signetics 2651

INS2651 General System Configuration



Absolute Maximum Ratings

Operating Ambient Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Voltages with Respect to Ground	−0.5 V to +6.0 V

Note: *Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC Electrical Characteristics.*

DC Electrical Characteristics

$T_A = 0°C$ to $+70°C$; $V_{CC} = +5.0\,V \pm 5\%$, GND = 0 V

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage		0.25	0.45	V	$I_{OL} = 1.6\,mA$
V_{OH}	Output High Voltage	2.4	2.8		V	$I_{OH} = -100\,\mu A$
I_{IL}	Input Load Current			10	μA	$V_{IN} = 0\,V$ to $5.5\,V$
I_{LD}	Data Bus Leakage Current			10	μA	$V_{OUT} = 4.0\,V$
I_{LO}	Open Drain Leakage Current			10	μA	$V_{OUT} = 4.0\,V$
I_{CC}	Power Supply Current		65	150	mA	

Capacitance

$T_A = +25°C$; V_{CC} = GND = 0 V

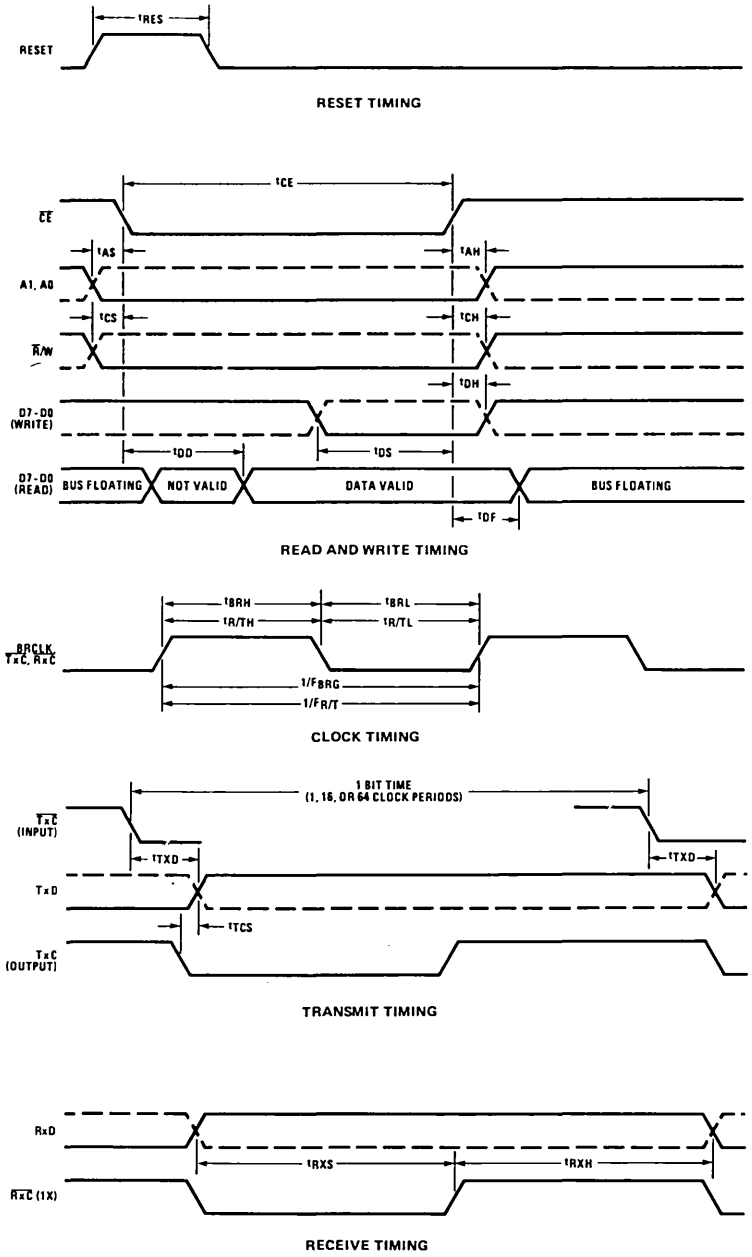
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
C_{IN}	Input Capacitance			20	pF	$f_c = 1\,MHz$
C_{OUT}	Output Capacitance			20	pF	Unmeasured pins
$C_{I/O}$	I/O Capacitance			20	pF	to ground

AC Electrical Characteristics

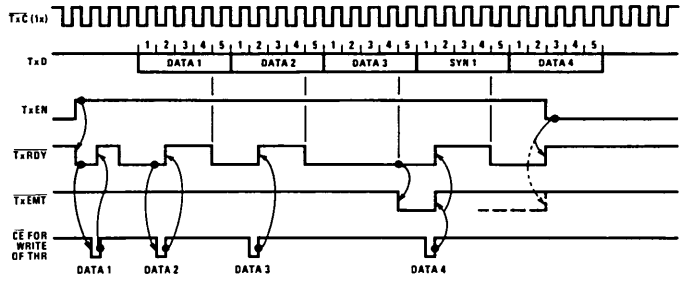
T_A = 0°C to +70°C; V_{CC} = +5.0 V ± 5%, GND = 0 V

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
BUS PARAMETERS						
t_{CE}	Chip Enable Pulse Width	300			ns	
t_{AS}	Address Setup Time	20			ns	
t_{AH}	Address Hold Time	20			ns	
t_{CS}	R/W Control Setup Time	20			ns	
t_{CH}	R/W Control Hold Time	20			ns	
t_{DS}	Data Setup Time for Write	225			ns	
t_{DH}	Data Hold Time for Write	50			ns	
t_{DD}	Data Delay Time for Read			250	ns	C_L = 100pF
t_{DF}	Data Bus Floating Time for Read			150	ns	C_L = 100pF
OTHER TIMINGS						
t_{RES}	RESET Pulse Width	1000			ns	
f_{BRG}	Baud Rate Generator Input Clock Frequency	1.0	5.0688	5.073	MHz	
t_{BRH}	Baud Rate Clock High State	70			ns	
t_{BRL}	Baud Rate Clock Low State	70			ns	
$f_{R/T}$	$\overline{TxC}$ or $\overline{RxC}$ Input Clock Frequency	DC		0.769	MHz	
$t_{R/TH}$	$\overline{TxC}$ or $\overline{RxC}$ Clock High State	650			ns	
$t_{R/TL}$	$\overline{TxC}$ or $\overline{RxC}$ Clock Low State	650			ns	
t_{TxD}	TxD Delay from Falling Edge of $\overline{TxC}$			650	ns	C_L = 100pF
t_{TCS}	Skew Between TxD Changing and Falling Edge of $\overline{TxC}$ Output		0	0	ns	C_L = 100pF
t_{RxS}	Rx Data Setup Time	300			ns	
t_{RxH}	Rx Data Hold Time	300			ns	

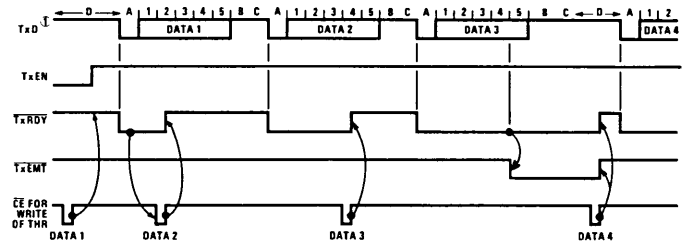
Timing Waveforms



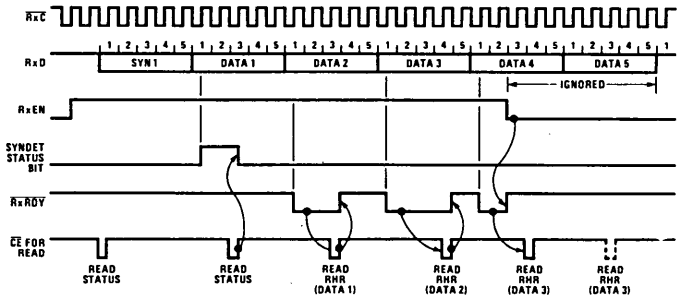
Timing Waveforms (cont'd.)



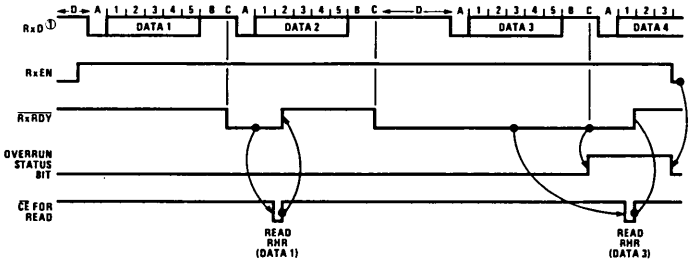
SYNCHRONOUS MODE



ASYNCHRONOUS MODE



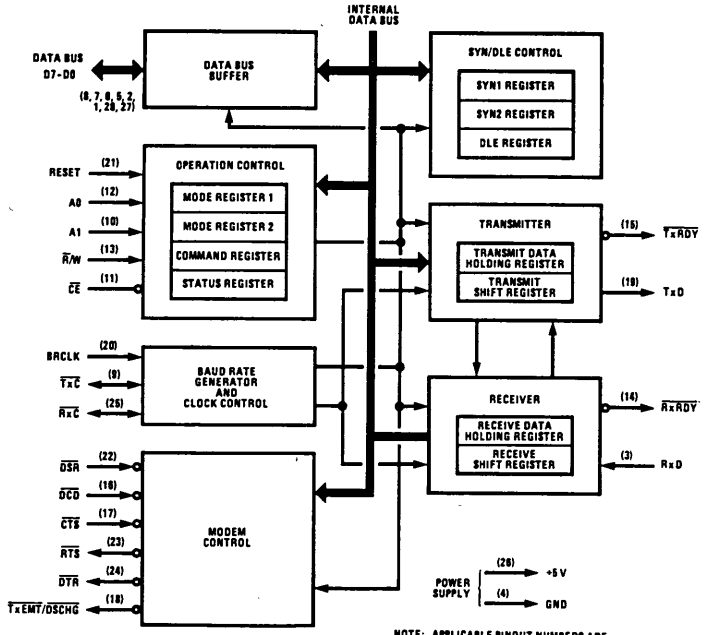
SYNCHRONOUS MODE



ASYNCHRONOUS MODE

TxRDY, TxEMT TIMING (SHOWN FOR 5-BIT CHARACTERS, NO PARITY, 2-STOP BITS (IN SYNCHRONOUS MODE).
RxRDY TIMING (SHOWN FOR 5-BIT CHARACTERS, NO PARITY, 2-STOP BITS (IN ASYNCHRONOUS).
NOTE 1: A – START BIT, B – STOP BIT 1, C – STOP BIT 2,
D – TxD MARKING CONDITION.

INS2651 Block Diagram



NOTE: APPLICABLE PINOUT NUMBERS ARE INCLUDED WITHIN PARENTHESES.

INS2651 Functional Pin Definitions

The following describes the function of all the INS2651 input/output pins. Some of these descriptions reference internal circuits.

INPUT SIGNALS

Reset (RESET), Pin 21: When high, performs a master reset on the INS2651. This signal asynchronously terminates any device activity and clears the Mode, Command, and Status Regsiters. The device assumes the idle state and remains in this mode until initialized with the appropriate control words.

Address Lines (A1-A0), Pins 10, 12: Address lines used to select internal Mode and Command registers.

Read/Write ($\overline{R}$/W), Pin 13: Controls the direction of data bus transfers. A high input allows data from the CPU to be loaded into the addressed register. A low input causes the contents of the addressed register to be present on the data bus.

Chip Enable ($\overline{CE}$), Pin 11: When low, indicates that control and data lines to the device are valid and that the specified operation should be performed. When high, places the device in the TRI-STATE® condition.

Baud Rate Generator Clock (BRCLK), Pin 20: 5.0688 MHz clock input to the internal Baud Rate Generator. Not required if external receiver and transmitter ($\overline{TxC}$ and $\overline{RxC}$) clocks are used.

Receiver Data (RxD), Pin 3: Serial data input to the receiver.

Data Set Ready ($\overline{DSR}$), Pin 22: General-purpose input which, when low, indicates either the Data Set Ready or Ring condition. Its complement is stored as Status Register bit 7. A change in state of this input causes a low output on $\overline{TXEMT/DSCHG}$.

Data Carrier Detect ($\overline{DCD}$), Pin 16: When low, enables the receiver to operate. The complement of this input is stored as Status Register bit 6, and an input change in state causes a low output on $\overline{TXEMT/DSCHG}$.

Clear to Send ($\overline{CTS}$), Pin 17: When low, enables the transmitter to operate. When high, holds the $\overline{TxD}$ output in MARK condition.

V_{CC}, Pin 26: +5-volt supply.

Ground, Pin 4: 0-volt reference.

OUTPUT SIGNALS

Transmitter Ready ($\overline{TxRDY}$), Pin 15: A low on this output, which is open-drain, indicates that Transmit Holding Register (THR) is ready to accept a data character from the CPU. This output, which is the complement of Status Register bit 0, goes high when the data character is loaded and is valid only when the transmitter is enabled. The $\overline{TxRDY}$ output can be used as an interrupt to the system.

Receiver Ready ($\overline{RxRDY}$), Pin 14: A low on this output, which is open-drain, indicates that the Receive Holding Register (RHR) has a character ready for input to the CPU. This output, which is the complement of Status Register bit 1, goes high either when the Receiver Holding Register is read by the CPU or when the receiver is disabled. The $\overline{RxRDY}$ output can be used as an interrupt to the system.

Transmitter Empty or Data Set Change ($\overline{TxEMT/DSCHG}$), Pin 18: A low on this output, which is open-drain, indicates that either the transmitter has completed serialization of the last character loaded by the CPU or that a change of state of the $\overline{DSR}$ or $\overline{DCD}$ inputs has occurred. If the TxEMT condition does not exist, this output goes high when the Status Register is read by the CPU. Otherwise, the Transmit Holding Register must be loaded by the CPU for this line to go high. The $\overline{TxEMT/DSCHG}$ output can be used as an interrupt to the system. This output is the complement of Status Register bit SR2.

Transmitter Data ($\overline{TxD}$), Pin 19: Composite serial data output to a MODEM or input/output device. The TxD output is held in the marking state (logic 1) when the transmitter is disabled.

Data Terminal Ready ($\overline{DTR}$), Pin 24: General-purpose output normally used to indicate Data Terminal Ready. The $\overline{DTR}$ output is the complement of Command Register bit 1.

Request to Send ($\overline{RTS}$), Pin 23: General-purpose output normally used to indicate Request to Send. The $\overline{RTS}$ output is the complement of Command Register bit 5.

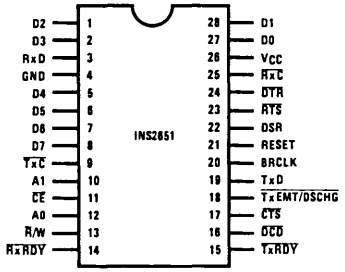
INPUT/OUTPUT SIGNALS

Data (D7-D0) Bus, Pins 28, 27, 8, 7, 6, 5, 2, 1: This bus comprises eight TRI-STATE input/output lines. The bus provides bidirectional communications between the INS2651 and the CPU. Data, control words, and status information are transferred via the Data Bus.

Receiver Clock ($\overline{RxC}$), Pin 25: If external receiver clock is programmed, this input controls the rate at which a data character is received. The frequency of the $\overline{RxC}$ input is a multiple (1x, 16x, or 64x) of the Baud Rate. Data is sampled on the rising edge of the clock. If internal receiver clock is programmed, this pin becomes an output at 1x the programmed Baud Rate.

Transmitter Clock ($\overline{TxC}$), Pin 9: If external transmitter clock is programmed, this input controls the rate at which a data character is transmitted. The frequency of the $\overline{TxC}$ input is a multiple (1x, 16x, or 64x) of the Baud Rate. Transmitter Data is clocked out of the INS2651 on the falling edge of the $\overline{TxC}$ input. If internal transmitter clock is programmed, this pin becomes an output at 1x the programmed Baud Rate.

Pin Configuration



INS2651 Programming

The system software determines the operative conditions (mode selection, clock selection, data format, and so forth) of the INS2651 via internal Mode Registers 1 and 2, and the Command Register. Prior to initiating data communications, the INS2651 operational mode must be programmed by performing write operations to these 8-bit registers via the Data Bus. The device can be reprogrammed at any time during program execution. However, the receiver and transmitter should be disabled if the change has an effect on the reception or transmission of a character.

The internal registers of the INS2651 are accessed by applying signals to the $\overline{CE}$, R/W, A1, and A0 inputs as specified in table 1.

Table 1. Guess My Name

$\overline{CE}$	A1	A0	R/W	Function
1	X	X	X	TRI-STATE Data Bus
0	0	0	0	Read Receive Holding Register
0	0	0	1	Write Transmit Holding Register
0	0	1	0	Read Status Register
0	0	1	1	Write SYN1/SYN2/DLE Registers
0	1	0	0	Read Mode Registers 1 and 2
0	1	0	1	Write Mode Registers 1 and 2
0	1	1	0	Read Command Register
0	1	1	1	Write Command Register

In the case of multiple registers (SYN1/SYN2/DLE Registers and Mode Registers 1 and 2), successive read or write operations will access the next higher register. For example, if A1 equals 0, A2 equals 1, and R/W equals 1, the first write operation loads SYN1 Register. The next write operation loads SYN2 Register, and the third loads the DLE Register. Read and write operations are performed on the Mode Registers in a similar manner. If more than the required numbet of accessses is made, the internal register pointer returns to the first register. The pointers are reset to the first registers either by a RESET input or by performing a "Read Command Register" operation, but are unaffected by any other read or write operation.

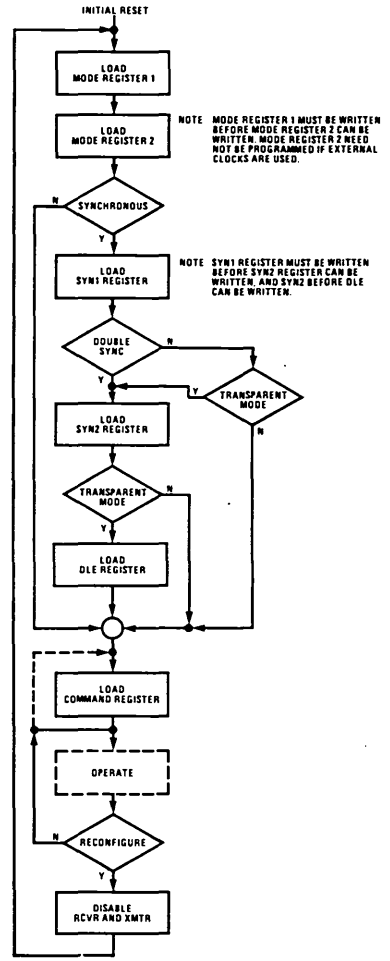


Figure 1. Initialization Flowchart

MODE REGISTER 1 FORMAT

BIT NUMBERS

MR1-7	MR1-6	MR1-5	MR1-4	MR1-3	MR1-2	MR1-1	MR1-0
SYNC: NO. OF SYN CHARACTERS 0 = DOUBLE SYN 1 = SINGLE SYN	SYNC: TRANSPARENCY CONTROL 0 = NORMAL 1 = TRANSPARENT	PARITY TYPE 0 = ODD 1 = EVEN	PARITY CONTROL 0 = DISABLED 1 = ENABLED	CHARACTER LENGTH 00 = 5 BITS 01 = 6 BITS 10 = 7 BITS 11 = 8 BITS		MODE AND BAUD RATE FACTOR[1] 00 = SYNCHRONOUS 1x RATE 01 = ASYNCHRONOUS 1x RATE 10 = ASYNCHRONOUS 16x RATE 11 = ASYNCHRONOUS 64x RATE	

ASYNC:
STOP BIT LENGTH
00 = INVALID
01 = 1 STOP BIT
10 = 1½ STOP BITS
11 = 2 STOP BITS

MODE REGISTER 2 FORMAT

BIT NUMBERS

MR2-7	MR1-6	MR2-5	MR2-4	MR2-3	MR2-2	MR2-1	MR2-0
NOT USED		TRANSMITTER CLOCK 0 = EXTERNAL 1 = INTERNAL	RECEIVER CLOCK 0 = EXTERNAL 1 = INTERNAL	BAUD RATE SELECTION 0000 = 50 BAUD 0001 = 75 BAUD 0010 = 110 BAUD 0011 = 134.5 BAUD 0100 = 150 BAUD 0101 = 300 BAUD	0110 = 600 BAUD 0111 = 1200 BAUD 1000 = 1800 BAUD 1001 = 2000 BAUD 1010 = 2400 BAUD 1011 = 3600 BAUD	1100 = 4800 BAUD 1101 = 7200 BAUD 1110 = 9600 BAUD 1111 = 19200 BAUD	

COMMAND REGISTER FORMAT

BIT NUMBERS

CR-7	CR-6	CR-5	CR-4	CR-3	CR-2	CR-1	CR-0
OPERATING MODE 00 = NORMAL OPERATION 01 = ASYNC: AUTOMATIC ECHO MODE SYNC: SYN AND/OR DLE STRIPPING MODE 10 = LOCAL LOOP BACK 11 = REMOTE LOOP BACK		REQUEST TO SEND 0 = FORCES $\overline{RTS}$ OUTPUT HIGH 1 = FORCES $\overline{RTS}$ OUTPUT LOW	RESET ERROR 0 = NORMAL 1 = RESET ERROR FLAG IN STATUS REGISTER (FE, OE, PE/DLE DETECT)	ASYNC: FORCE BREAK 0 = NORMAL 1 = FORCE BREAK SYNC: SEND DLE 0 = NORMAL 1 = SEND DLE	RECEIVE CONTROL (RxEN) 0 = DISABLE 1 = ENABLE	DATA TERMINAL READY 0 = FORCES $\overline{DTR}$ OUTPUT HIGH 1 = FORCES $\overline{DTR}$ OUTPUT LOW	TRANSMIT CONTROL 0 = DISABLE 1 = ENABLE

STATUS REGISTER FORMAT

BIT NUMBERS

SR-7	SR-6	SR-5	SR-4	SR-3	SR-2	SR-1	SR-0
DATA SET READY 0 = $\overline{DSR}$ INPUT IS HIGH 1 = $\overline{DSR}$ INPUT IS LOW	DATA CARRIER DETECT 0 = DCD INPUT IS HIGH 1 = DCD INPUT IS LOW	FE/SYN DETECT ASYN: 0 = NORMAL 1 = FRAMING ERROR SYNC: 0 = NORMAL 1 = SYN CHARACTER DETECTED	OVERRUN 0 = NORMAL 1 = OVERRUN ERROR	PE/DLE DETECT ASYNC: 0 = NORMAL 1 = PARITY ERROR SYNC: 0 = NORMAL 1 = PARITY ERROR OR DLE CHARACTER RECEIVED	TxEMT/DSCHG 0 = NORMAL 1 = CHANGE IN $\overline{DSR}$ OR $\overline{DCD}$, OR TRANSMIT SHIFT REGISTER IS EMPTY	RxRDY 0 = RECEIVE HOLDING REGISTER EMPTY 1 = RECEIVE HOLDING REGISTER HAS DATA	TxRDY 0 = TRANSMIT HOLDING REGISTER BUSY 1 = TRANSMIT HOLDING REGISTER EMPTY

NOTE 1: BAUD RATE FACTOR IN ASYNCHRONOUS MODE APPLIES ONLY IF EXTERNAL CLOCK IS SELECTED. FACTOR IS 16x IF INTERNAL CLOCK IS SELECTED.

Table 2. Baud Rate Generator Characteristics (Crystal Frequency = 5.0688 MHz)

Baud Rate	Theoretical Frequency 16x Clock (kHz)	Actual Frequency 16x Clock (kHz)	Percent Error	Duty Cycle (%)	Divisor
50	0.8	0.8	–	50/50	6336
75	1.2	1.2	–	50/50	4224
110	1.76	1.76	–	50/50	2880
134.5	2.152	2.1523	0.016	50/50	2355
150	2.4	2.4	–	50/50	2112
300	4.8	4.8	–	50/50	1056
600	9.6	9.6	–	50/50	528
1200	19.2	19.2	–	50/50	264
1800	28.8	28.8	–	50/50	176
2000	32.0	32.081	0.253	50/50	158
2400	38.4	38.4	–	50/50	132
3600	57.6	57.6	–	50/50	88
4800	76.8	76.8	–	50/50	66
7200	115.2	115.2	–	50/50	44
9600	153.6	153.6	–	48/52	33
19200	307.2	316.8	3.125	50/50	16

Note: 16x clock is used in asynchronous mode. In synchronous mode, clock multiplier is 1x and duty cycle is 50%/50% for any baud rate.

INS2651 Operation

GENERAL

The transmitter section of the INS2651 performs parallel-to-serial conversion of data supplied to it from the system data bus.

The receiver section of the INS2651 performs serial-to-parallel conversion of data received from the MODEM or input/output device. Both the transmitter and receiver are double buffered, allowing a full character time in which to service Transmit Ready ($\overline{TxRDY}$) and Receive Ready ($\overline{RxRDY}$) interrupts.

The character size (5, 6, 7, or 8 bits) is program selectable. Parity check/generation and the baud rate may also be defined by the program. Note that the character size is exclusive of the start/stop and parity bits.

SYNCHRONOUS MODE

The transmitter starts transmitting a continuous bit stream once the transmitter is enabled and the Clear to Send ($\overline{CTS}$) input is low. If the system is late in supplying a character to the transmitter, then the transmitter will send the SYN character (or SYN1, two characters if in double SYNC mode) as an idle fill in the Non-Transparent mode, or the DLE-SYN1 character pair as an idle fill in the Transparent mode. If this condition occurs, the $\overline{TxEMT/DSCHG}$ output goes low.

The receiver enters a character synchronization mode as soon as the receiver is enabled and the Data Carrier Detect ($\overline{DCD}$) input goes low. Either one or two consecutive SYN characters must be recognized by the receiver. The number of SYN characters is program selectable, and data is sent to the processor only after synchronization. The SYN character(s) in the Transparent mode (or DLE-SYN1 characters in the Non-Transparent mode) are stripped off the data stream after synchronization. This feature is program selectable.

An overrun error will occur if the processor is late in servicing the received character. When this condition occurs, the character in the receiver buffer is written over by the character causing the overrun, and the overrun status bit is set.

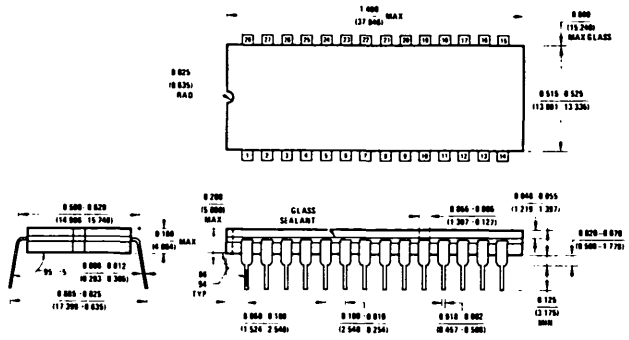
ASYNCHRONOUS MODE

Once transmission is initiated, the transmitter supplies the start bit, odd, even, or no parity bit, and the proper number of stop bits as specified by the program. If the next character is presented to the transmitter, it is sent immediately after transmission of the stop bit of the present character. Otherwise the Mark (logic high) condition is sent. The transmitter can be programmed to send a Space (logic low) condition instead of the Mark condition.

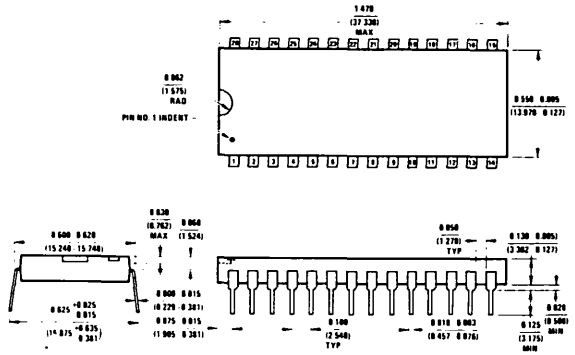
Once the receiver is enabled, reception of a character is initiated by recognition of the start bit. The Start/Stop and Parity bits are stripped off while assembling the serial input into a parallel character. If a break condition is detected then the receiver sends a character of all zero bits and a Framing Error status bit to the processor.

Succeeding all-zero or break characters are not assembled and presented to the system. The Receive Data (RxD) input must return to a marking condition before character assembly is resumed. The overrun condition is checked in the same manner as in the Synchronous mode.

Physical Dimensions



28-Lead Ceramic Dual-In-Line Package [Cer Dip (J)]
Order Number INS2651J



28-Lead Plastic Dual-In-Line Package (N)
Order Number INS2651N

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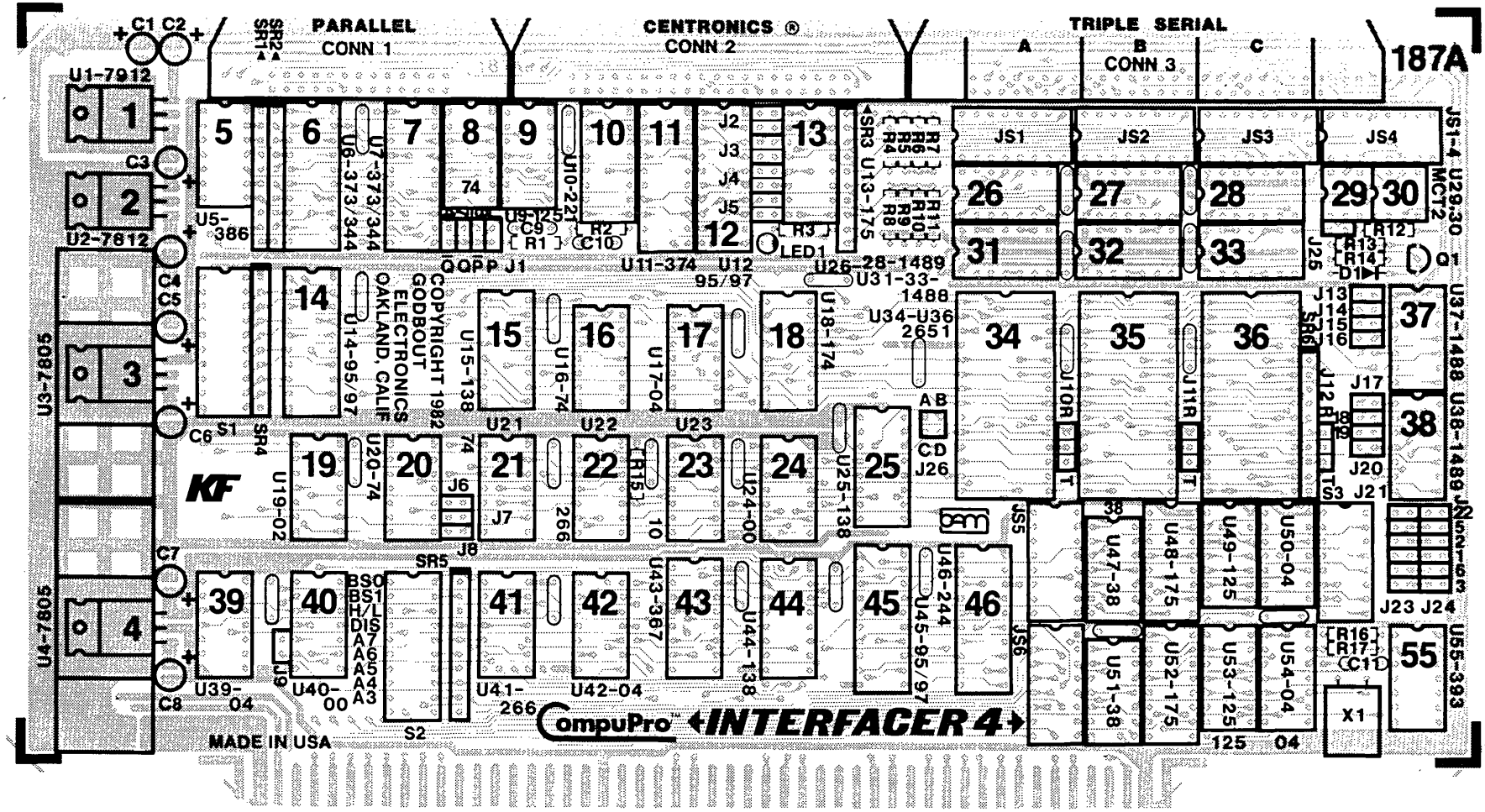
Cnr Stud Rd & Mtn Highway
Bayswater, Victoria 3153
Australia
Tel 03-729-6333
Telex 32096

PARTS LIST

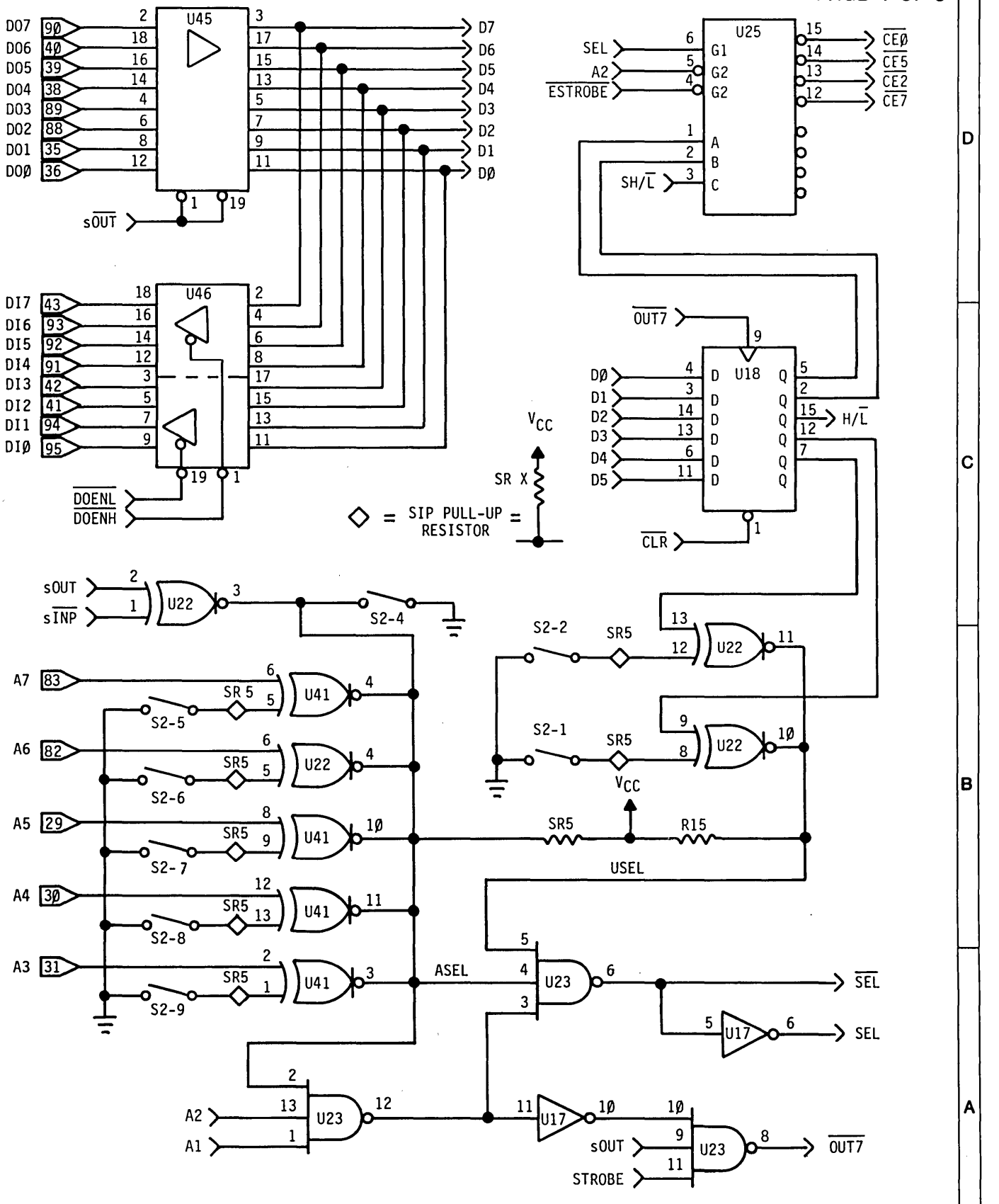
INTEGRATED CIRCUITS	
U1	7912
U2	7812
U3-U4	7805
U5	74LS386
U6	74LS373/374
U7	74LS373/374
U8	74LS74
U9	74LS125
U10	74LS221
U11	74LS374
U12	81LS95/97
U13	74LS175
U14	81LS95/97
U15	74LS138
U16	74LS74
U17	74LS04
U18	74LS174
U19	74LS02
U20-U21	74LS74
U22	74LS266
U23	74LS10
U24	74LS00
U25	74LS138
U26-U28	1489
U29-U30	4N28
U31-U33	1488
U34-U36	2651
U37	1488
U38	1489
U39	74LS04
U40	74LS00
U41	74LS266
U42	74LS04
U43	74LS367
U44	74LS138
U45	81LS95/97

INTERGRATED CIRCUITS	
U46	74LS244
U47	74LS38
U48	74LS175
U49	74LS125
U50	74LS04
U51	74LS38
U52	74LS175
U53	74LS125
U54	74LS04
U55	74LS393
RESISTORS	
R1-R2	10K OHM
R3	330 OHM
R4	560 OHM
R5-R7	5.1K OHM
R8	560 OHM
R9-R11	5.1K OHM
R12	2.7K OHM
R13	4.7K OHM
R14	470 OHM
R15	5.1K OHM
R16-R17	1.0K OHM
SR1-SR6	4.7K OHM
CAPACITORS	
C1-C8	DIPPED TANT 20V
C9-C10	220PF MICA
C11	.01UF CERAMIC
(25)	BYPASS CAPS
CRYSTAL	
X1	5.0688 MHz

TRANSISTOR	
Q1	2N3904
DIODES	
D1	SIGNAL DIODE
LED1	RED LED
SWITCHES	
S1	10 POSITION
S2	10 POSITION
S3	8 POSITION
SHUNTS	
JS1-JS3	8 POS. SHUNT
JS4-JS6	8 POS. HEADER
(10)	PIN SHUNTS



COMPONENT LAYOUT



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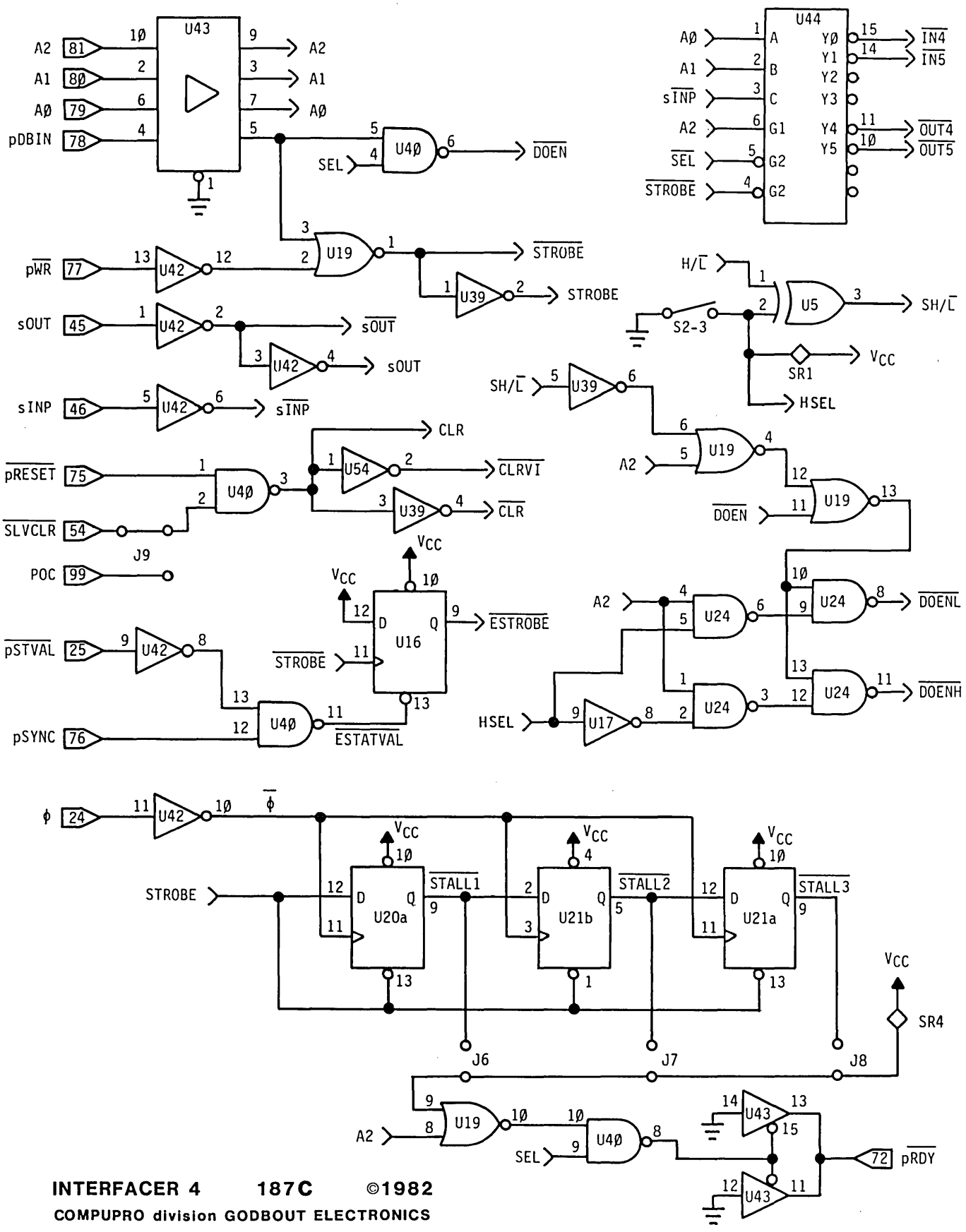
U43
A2
A1
AØ
pDBIN
U44
AØ
A1
sINP
A2
SEL
STROBE
IN4
IN5
OUT4
OUT5
U4Ø
DOEN
U19
STROBE
pWR
U42
U39
sOUT
sINP
H/L
S2-3
U5
SH/L
VCC
SR1
HSEL
CLR
pRESET
SLVCLR
U54
CLRVI
J9
POC
U16
ESTROBE
pSTVAL
pSYNC
ESTATVAL
U24
DOENL
DOENH
U17
HSEL
φ
U20a
U21b
U21a
STALL1
STALL2
STALL3
SR4
J6
J7
J8
pRDY
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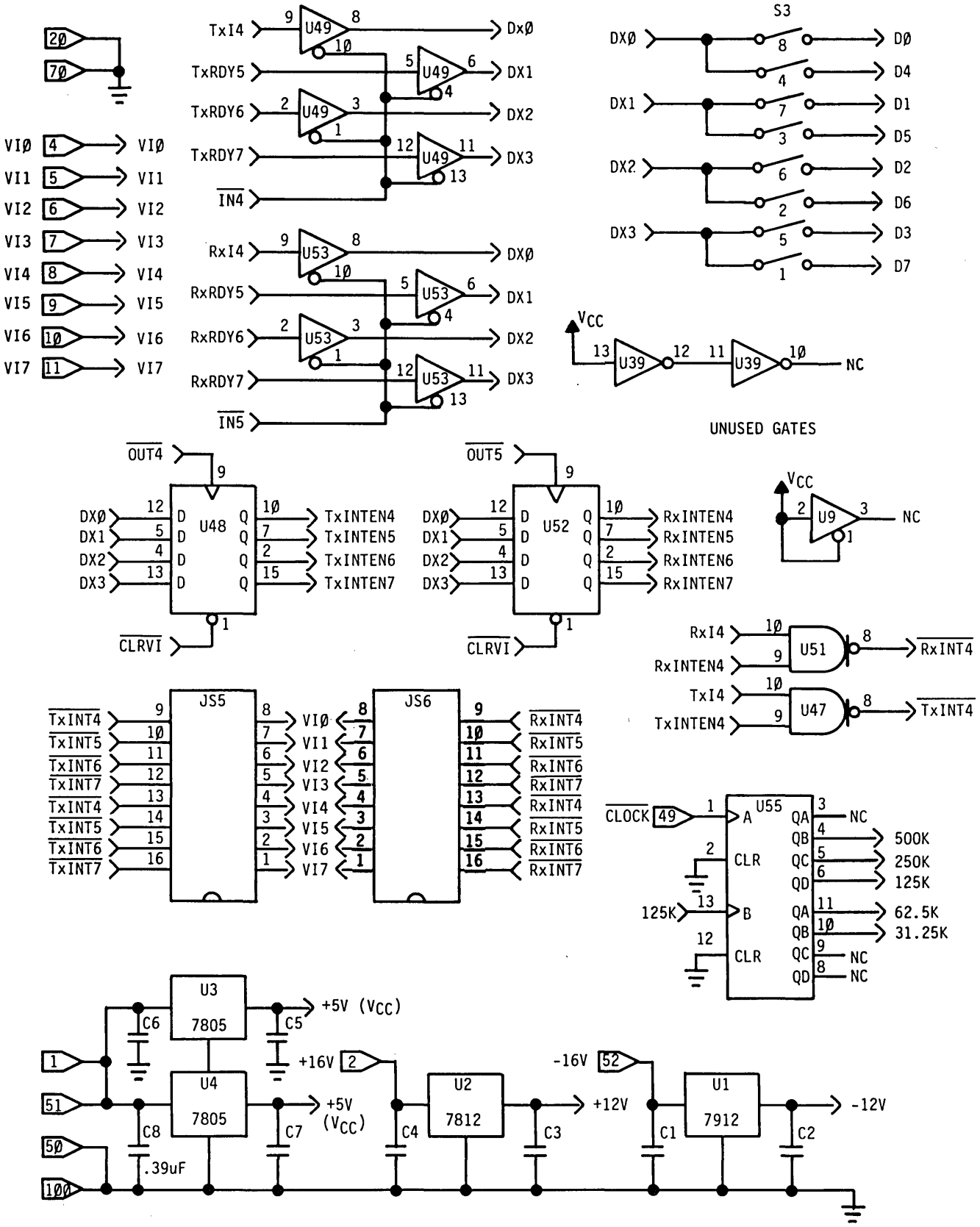

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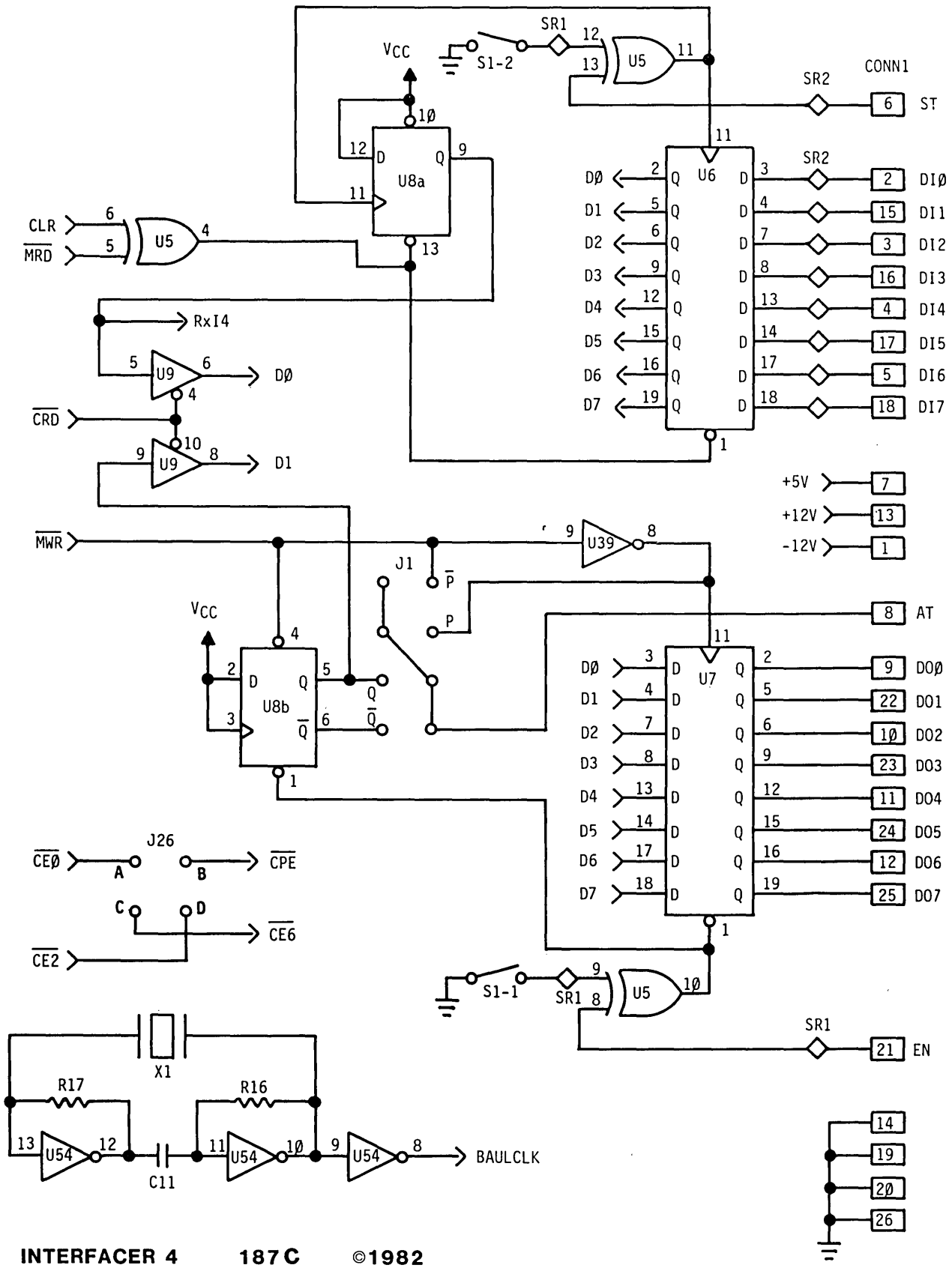

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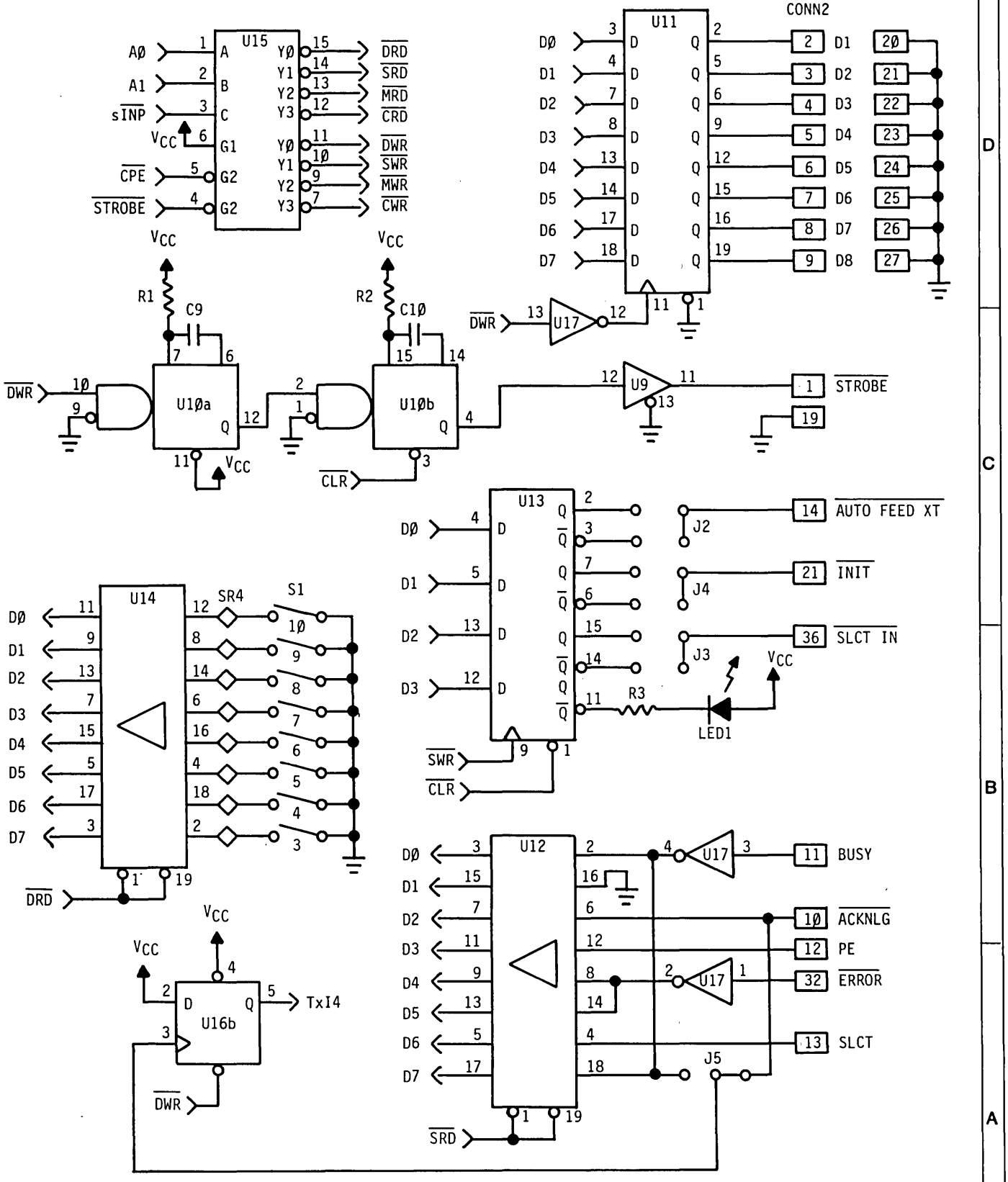

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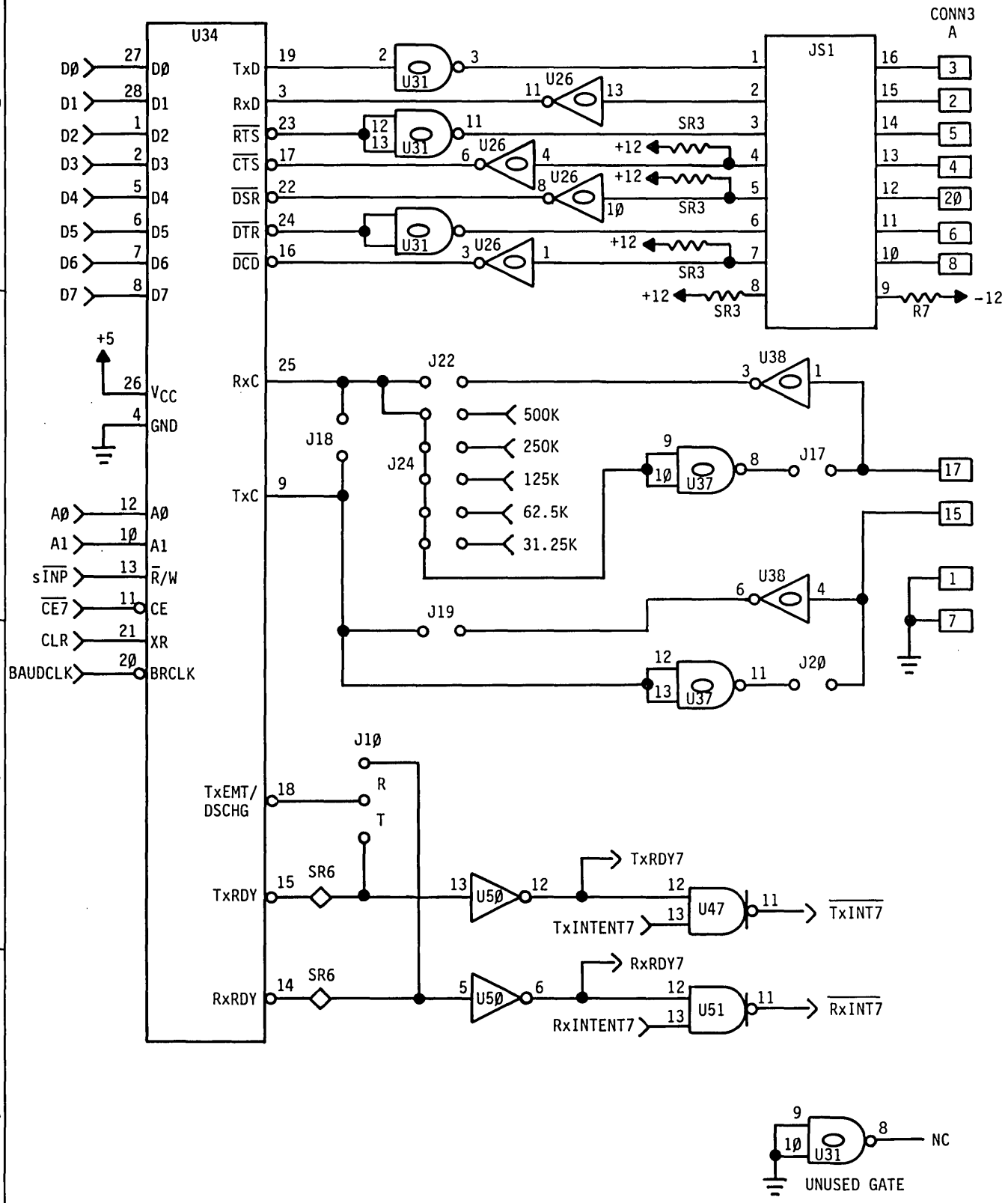

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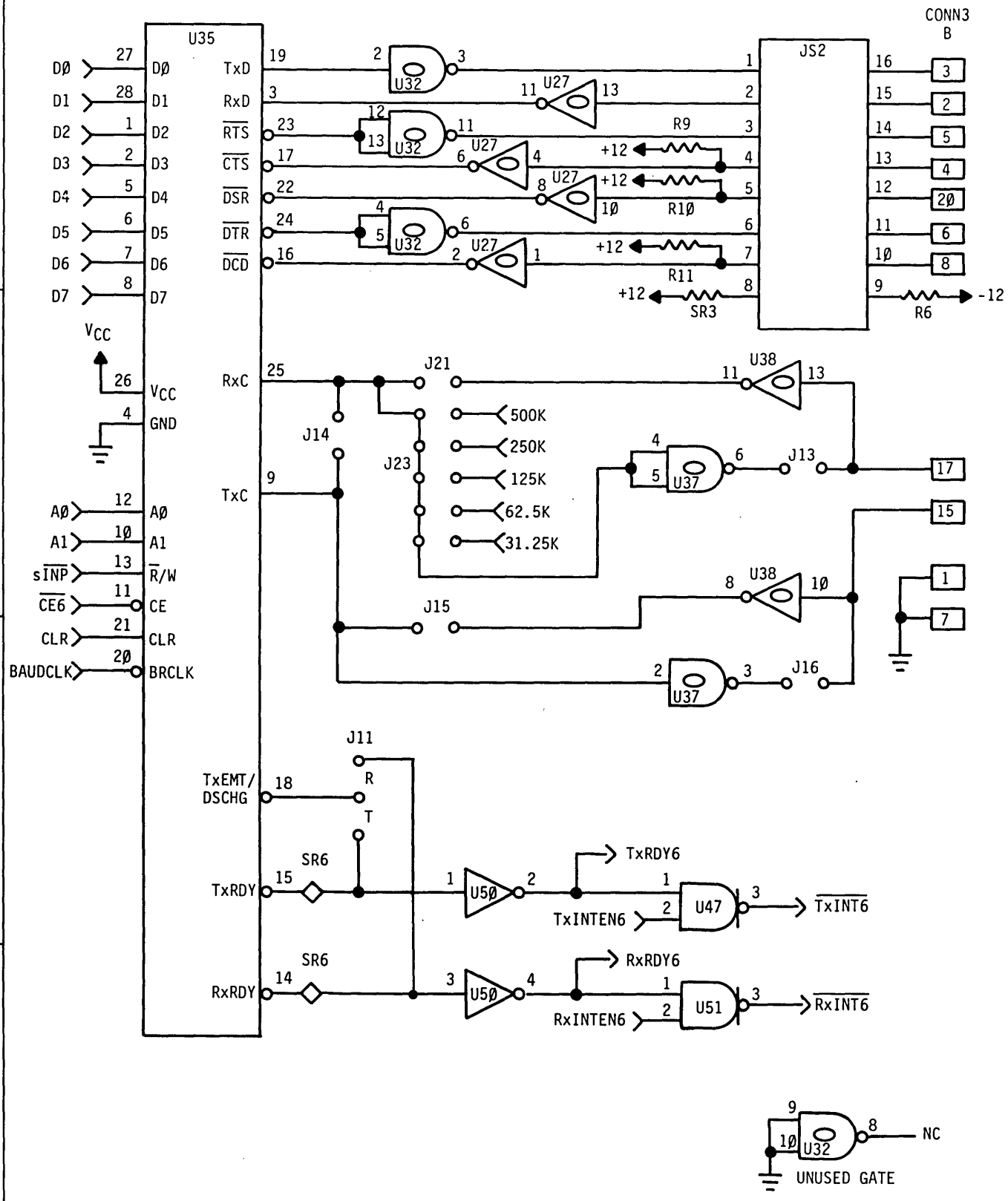

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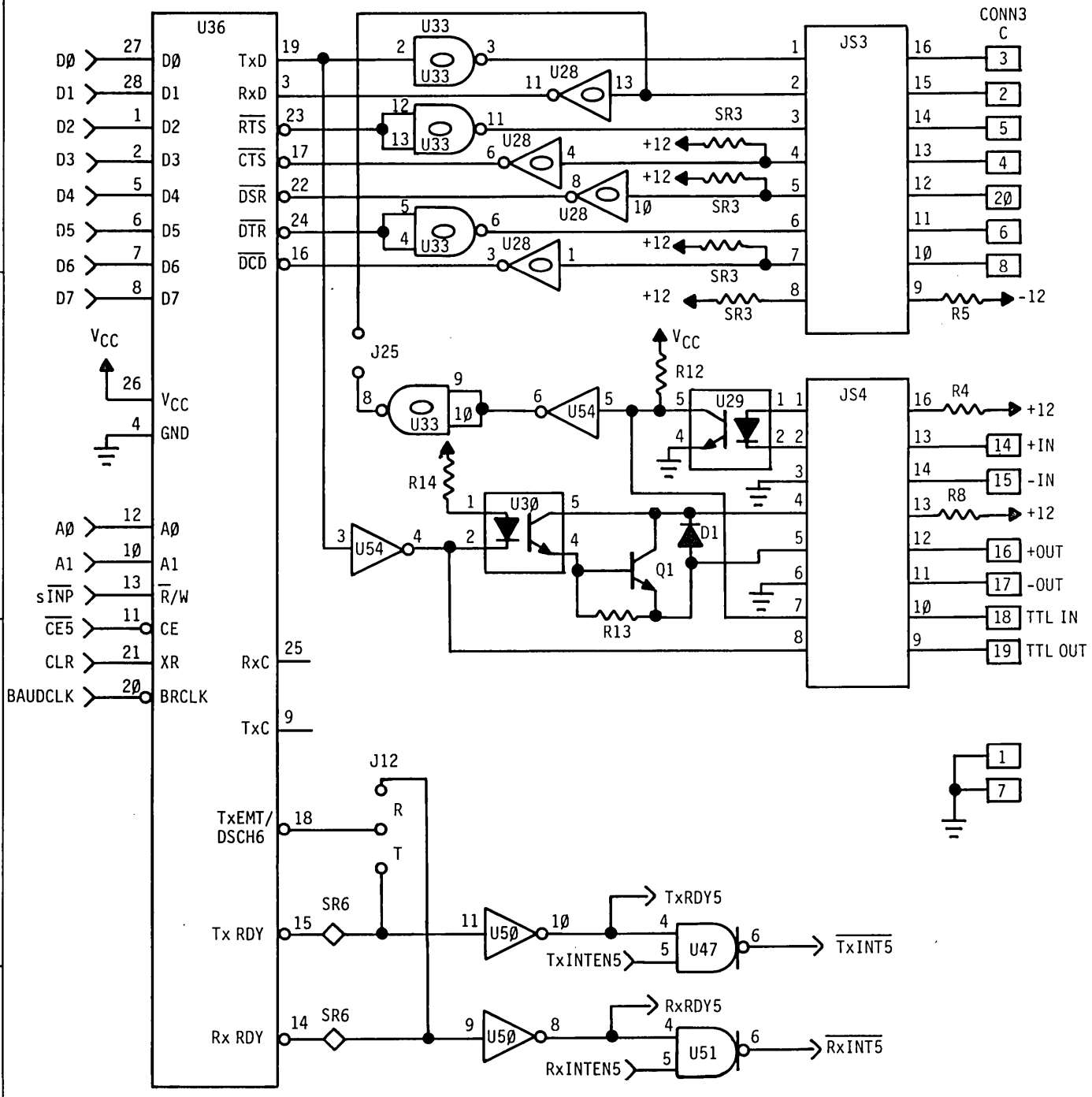

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JUMPER AND SWITCH INDEX

IF YOU NEED ASSISTANCE ALWAYS CONTACT
YOUR **COMPUPRO DEALER FIRST**

CUSTOMER SERVICE INFORMATION

Our paramount concern is that you be satisfied with any Godbout CompuPro product. If this product fails to operate properly, it may be returned to us for service; see warranty information below.

If you need further information feel free to write us at:

Box 2355, Oakland Airport, CA 94614-0355

LIMITED WARRANTY INFORMATION

Godbout Electronics will repair or replace, at our option, any parts found to be defective in either materials or workmanship for a period of 1 year from date of invoice. Defective parts *MUST* be returned for replacement.

If a defective part causes a Godbout Electronics product to operate improperly during the 1 year warranty period, we will service it free (original owner only) if delivered and shipped at owner's expense to and from Godbout Electronics. If improper operation is due to an error or errors on the part of the purchaser, there may be a repair charge. Purchaser will be notified if this charge exceeds $50.00.

We are not responsible for damage caused by the use of solder intended for purposes other than electronic equipment construction, failure to follow printed instructions, misuse or abuse, unauthorized modifications, use of our products in applications other than those intended by Godbout Electronics, theft, fire, or accidents.

Return to purchaser of a fully functioning unit meeting all advertised specifications in effect as of date of purchase is considered to be complete fulfillment of all warranty obligations assumed by Godbout Electronics. This warranty covers only products marketed by Godbout Electronics and does not cover other equipment used in conjunction with said products. We are not responsible for incidental or consequential damages.

Prices and specifications are subject to change without notice, owing to the volatile nature and pricing structure of the electronics industry.

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