ANSI EIA/TIA-530-A

In this report:

Note: The content of this report has been reviewed and revalidated. It is being published with a new date to indicate that the information is current.

Datapro Summary

ANSI EIA/TIA-530-A (hereafter EIA-530-A) defines the mechanical interface characteristics between Data Termination Equipment (DTE) and Data Circuit-Terminating Equipment (DCE). It operates in conjunction with RS-422-A and RS-423-A, which define the electrical operation of the individual interchange circuits for balanced and unbalanced operation, respectively. EIA-530-A complements RS-232-D for data rates above 20K bps and replaces RS-449 for data rates above 20K bps.

A revision of EIA-530, EIA-530-A was approved in May 1992 and includes several relatively minor modifications to the previous standard. The most significant change accounts for the alternative 26-position interface connector (Alt A). Other revisions comprise the following:

- Addition of Circuits CJ (Ready for Receiving), CE (Ring Indicator), and AC (Signal Common).
- Use of Circuit CB (Clear to Send) for hardware flow control.
- Use of Local Loopback for "Busy Out."
- Change of Circuits CC (DCE Ready) and CD (DTE Ready) to Category II Circuits.

The new standard is compatible with EIA-530, but applications connecting versions of RS-449 or EIA-530 (with Category I Circuits CC and CD) with EIA-530-A (with Category II Circuits CC and CD) require an unbalanced/balanced converter between the interfaces (see Table *"Interconnecting EIA RS-530-A With EIA RS-449"* for circuitry connections).

In 1977 the Electronic Industries Assn. (EIA) developed the RS-449, RS-422, and RS-423 standards to eventually replace RS-232-C. RS-449, however, never really caught on and, in March 1987, EIA-530 was introduced as its intended replacement. RS-422 and RS-423 remain in the revised forms of RS-422-A and RS-423-A. RS-232-C also outlasted RS-449 and, in January 1987, the EIA issued RS-232-D, a revision for RS-232-C.

EIA-530-A governs the mechanical and electrical characteristics of the interface between Data Terminal Equipment (DTE) and Data Circuit-Terminating Equipment (DCE). The standard defines DTE as the hardware on the business machine side of the interface (teleprinters, display terminals, front-end processors, central processing units, etc.), and DCE as the modem, signal converter, or other device between the DTE and the communications line.

This report compares EIA-530-A with RS-232-D, RS-449, and CCITT V.35. It also discusses the mechanical and electrical characteristics and looks at the general classification of interchange circuits and outlines interchange circuit details.

Copies of EIA-530-A, RS-422-A, and RS-423-A can be obtained from the Electronic Industries Assn., 2001 I Street NW, Washington, DC 20006.

Analysis

EIA-530-A operates in conjunction with either of two standards specifying electrical characteristics: RS-422-A, for balanced circuits; and RS-423-A, for unbalanced circuits. When each interface circuit has its own ground lead, the circuit is balanced. When an interface uses a common or shared grounding technique, it is unbalanced.

EIA-530-A is used for data communications systems with the following characteristics:

- DTE serializes data bits, and the DCE puts no restrictions on the DTE's bit sequence arrangements.
- Communication is binary, serial, synchronous, or asynchronous, and control information is exchanged on separate circuits.
- Equipment on one side of the DTE/DCE interface connects directly to equipment on the other side without additional technical considerations.
- Communication is in half- and/or full-duplex modes in point-to-point or multipoint configurations over two- or four-wire facilities with data rates ranging from 20K bps to a nominal upper limit of 2.1M bps. Point-to-point arrangements may operate on either switched or dedicated facilities. Dedicated lines connect multipoint arrangements.

Applications in which cable termination, signal wave shaping, interconnection cable distance, and the interface's mechanical configurations must be tailored to meet specific user needs are not precluded, but are generally not within the standard's scope. The EIA-530-A connector, also used for RS-232-D, uses electrical characteristics that, if improperly connected to some silicon devices designed to meet the RS-422-A and RS-423-A electrical characteristics specified in this recommendation, could damage those devices.

EIA-530-A/RS-232-D

These standards include a specification of the D-shaped 25-pin interface connector, which RS-232-C had only referenced in an appendix and never included as part of the standard. Both standards support testing of both local and remote DCEs through the Local Loopback, Remote Loopback, and Test Mode circuits. Circuit names for the first 8 pins in both standards are the same, but differ on pins 9, 10, and 11, which are not used in RS-232-D.

RS-530-A achieves higher data rates than RS-232-D (greater than 20K bps) by specifying the use of balanced signals, while sacrificing some secondary signals and the Ring Indicator. The Ring Indicator's elimination indicates that EIA-530-A is not for use in dial-up applications.

EIA-530-A/RS-449

The EIA-530-A standard has officially replaced RS-449 but, while both standards are in use, EIA-530-A can be interconnected with RS-449 devices through a connecting cable or adapter. Table *"Interconnecting EIA RS-530-A With EIA RS-449"* lists the circuit name and mnemonic, and connector contact pin for each interface.

EIA-530-A/CCITT V.35

EIA-530-A provides balanced (EIA-422-A) generators and receivers on interchange Circuits CA (Request to Send), CB (Clear to Send), and CF (Receive Line Signal Detector). The corresponding interchange circuits in a V.35 interface utilize CCITT V.28 (EIA-232-E) electrical characteristics. In applications connecting an EIA-422-A balanced generator with an EIA-232-E unbalanced receiver, a special balanced/unbalanced converter must be employed between the interfaces. Otherwise, EIA-530-A and CCITT V.35 are fully compatible.

Mechanical Characteristics

The point of demarcation between the DTE and the DCE is at connector plugs on the DCE or at an interface point no further than ten feet (three meters) from the DCE. A 25-position connector was specified for all interchange circuits in EIA-530. EIA-530-A's alternative 26-position "Alt A" connector is specified for use when a smaller physical connector is required (it is approximately 3/4" × 1/4"). In all cases, the DTE provides the cable (up to 200 feet), which has male (pin) contacts and a female shell (plug connector); the DCE has a female connector. The connectors are equipped with a block that permits latching and unlatching without a tool. The latching block also permits the use of screws to fasten the connectors together. The mechanical configuration for connections of the interface cable at points other than the demarcation point is not specified.

When additional functions are offered in a separate unit that is inserted between the DTE and DCE, the female connector is associated with the DTE interface, while the male connector is a DCE interface.

Functional Description of Interchange Circuits

Interchange circuits fall into four general classifications: ground (or common return), data circuits, control circuits, and timing circuits. Table *"EIA RS-530-A Interchange Circuits"* outlines a list of EIA-530-A interchange circuits showing circuit mnemonic, circuit name, circuit direction, and circuit type. Table *"RS-530 and Nearest Equivalent CCITT V.35"* compares the connector pin assignments and the functional interchange circuits along with an equivalency table showing the nearest equivalent CCITT V.35 functions in relation to each EIA-530-A function. A functional description of each of the EIA-530-A interchange circuits follows.

Ground or Common Return Circuits

Circuit AB and AC (Signal Commons) connects the DTE circuit ground (signal common) to the DCE circuit ground (signal common) to provide a conductive route between the DTE and DCE signal commons.

Data Circuits

Circuit BA (Transmitted Data) transfers the data signals originated by the DTE to the DCE. The DTE holds Circuit BA in the binary ONE (marking) condition unless an ON condition is present on all of the following circuits: CA (Request to Send), CB (Clear to Send), CC (DCE Ready), and CD (DTE Ready). The DCE disregards any signal appearing on Circuit BA when an OFF condition exists on one or more of these circuits. While an ON condition is maintained on each of the circuits, the DCE sends all data signals transmitted across the interface on Circuit BA to the communications channel. The term "data signals" includes the binary ONE (marking) condition, reversals, and other sequences, such as SYN coded characters that maintain timing synchronization.

Circuit BB (Received Data) transfers DCE-generated data signals to the DTE in response to line signals from a remote station. Circuit BB is held in the binary ONE (marking) condition while Circuit CF (Receive Line Signal Detector) is in the OFF condition. On half-duplex channels, Circuit BB is held in the marking condition when Circuit CA is ON and for a brief interval when Circuit CA makes the transition from ON to OFF. This allows for the completion of the transmission and for the decay of channel reflections.

Timing Circuits

Circuit DA (Transmit Signal Element Timing—DTE Source) provides the DCE with transmit signal element timing data. The ON to OFF transition nominally indicates the center of each signal element on Circuit BA. When Circuit DA is implemented in the DTE, the DTE provides timing data on it whenever the DTE is

Interconnecting EIA RS-530-A With EIA RS-449

	EIA-530-A		EIA-RS-449		
Circuit Name	**Mnemonic**	**Contact**	**Contact**	**Mnemonic**	**Circuit Name**
Shield	None	1	1	None	Shield
Transmitted Data	BA (A) BA (B)	2 14	4 22	SD (A) SD (B)	Send Data
Received Data	BB (A) BB (B)	3 16	6 24	RD (A) RD (B)	Receive Data
Request to Send	CA (A) CA (B)	4 19	7 25	RS (A) RS (B)	Request to Send
Clear to Send	CB (A) CB (B)	5 13	9 27	CS (A) CS (B)	Clear to Send
DCE Ready	CC	6	11 29	DM (A) DM (B)	Data Mode *(1)*
DTE Ready	CD	20	12 30	TR (A) TR (B)	Terminal Ready *(2)*
Signal Common	AB	7	19	SG	Signal Ground *(2)*
Received Line Signal Detector	CF (A) CF (B)	8 10	13 31	RR (A) RR (B)	Receiver Ready
Transmit Signal Element Timing (DCE Source)	DB (A) DB (B)	15 12	5 23	ST (A) ST (B)	Send Timing
Receiver Signal Element Timing (DCE Source)	DD (A) DD (B)	17 9	8 26	RT (A) RT (B)	Receive Timing
Local Loopback	LL	18	10	LL	Local Loopback
Remote Loopback	RL	21	14	RL	Remote Loopback
Transmit Signal Element Timing (DTE Source)	DA (A) DA (B)	24 11	17 35	TT (A) TT (B)	Terminal Timing
Test Mode	TM	25	18	TM	Test Mode
Ring Indicator	CD	22	15	IC	Incoming Call
Signal Common	AC	23	20	RC	Receive Common *(1)*
			37	SC	Send Common *(2)*

(1) For proper operation with an EIA-449 DTE, connect contacts 20 and 29.

(2) For proper operation with an EIA-449 DCE, connect contacts 19, 30, and 37.

EIA RS-530-A Interchange Circuits

Circuit Mnemonic	Circuit Name	Circuit Direction	Circuit Type
AB	Signal Common	Does not apply	Common
AC	Signal Common	Does not apply	Common
BA	Transmitted Data	To DCE	Data
BB	Received Data	From DCE	Data
DA	Transmit Signal Element Timing (DTE Source)	To DCE	Timing
DB	Transmit Signal Element Timing (DCE Source)	From DCE	Timing
DD	Receiver Signal Element Timing (DCE Source)	From DCE	Timing
CA	Request to Send	To DCE	Control
CB	Clear to Send	From DCE	Control
CF	Received Line Signal Detector	From DCE	Control
CJ	Ready for Receiving	To DCE	Control
CE	Ring Indicator	From DCE	Control
CC	DCE Ready	From DCE	Control
CD	DTE Ready	To DCE	Control
LL	Local Loopback	To DCE	Timing
RL	Remote Loopback	To DCE	Timing
TM	Test Mode	From DCE	Timing

in a POWER ON condition. The DTE can withhold timing data on this circuit for short periods as long as Circuit CA is in the OFF condition.

Circuit DB (Transmit Signal Element Timing—DCE Source) provides the DTE with transmit element timing data. The DTE provides a data signal on Circuit BA in which the transitions between signal elements occur at the time of the transitions from OFF to ON condition of the signal on Circuit DB. The DCE provides timing data on Circuit DB whenever the DCE is in a POWER ON condition. The DCE can withhold timing data on this circuit if Circuit CC is in the OFF condition.

Circuit DD (Receiver Signal Element Timing—DCE Source) provides the DTE with receive signal element timing data. The DCE provides timing data on this circuit whenever the DCE is in a POWER ON condition. The DCE can withhold timing data on this circuit for short periods as long as Circuit CC is in the OFF condition.

Control Circuits

Circuit CA (Request to Send) controls the transmit function of the local DCE and, on half-duplex channels, the direction of data transmission. On one-way-only (duplex) channels, the ON condition holds the DCE in the transmit mode; the OFF condition suppresses transmission. On a half-duplex channel, the ON condition holds the DCE in the transmit mode and suppresses the receive mode. The OFF condition holds the DCE in the receive mode. A transition from OFF to ON instructs the DCE to enter the transmit mode. The DCE responds by taking any necessary action and indicating completion of such action by turning ON Circuit CB (Clear to Send), thereby permitting the DTE to transfer data across Circuit BA. A transition from ON to OFF instructs the DCE to complete transmission of all data previously transferred across the interface on Circuit BA (Transmitted Data) and then to assume a nontransmit, or receive mode, as appropriate. The DCE responds to this instruction by turning OFF Circuit CB.

When Circuit CA is turned OFF, it is not turned ON again until Circuit CB has been turned OFF by the DCE. An ON condition is required on Circuit CA, as well as on Circuits CB and CC, whenever data is transferred across the interface on Circuit BA by the DTE. Circuit CA may be turned ON at any time when Circuit CB is OFF, regardless of the status of any other interface circuit.

Circuit CB (Clear to Send) indicates that the DCE has been conditioned to transmit data over the communications channel. The ON condition, together with the ON on Circuit CA (Request to Send) and Circuit CC (DCE Ready), indicates to the DTE that signals on Circuit BA (Transmitted Data) will be transmitted to the communication channel. The OFF condition indicates that the DTE should not transfer data across the interface on Circuit BA, since this data will not be transmitted to the line. The ON condition of Circuit CB is a response to the occurrence of concurrent ON conditions on Circuits CC and CA, delayed as appropriate by the DCE, to allow the establishment of a data communications channel to a remote DTE. Circuit CB may be turned OFF during the data transfer or test phase, independent of Circuit CA's condition, to signal the DTE to interrupt the transfer of data on Circuit BA for a finite period of time. This capability, added in EIA-530-A, provides for DCE flow control or DCE/DCE resynchronization.

Circuit CF (Received Line Signal Detector) indicates whether the receiver in the DCE is ready to receive data signals from the communication channel, but does not indicate the relative quality of the data signals received. An equalizer's condition

RS-530 and Nearest Equivalent CCITT V.35

Circuit Name	EIA-530-A Mnemonic	Contact	CCITT V.35 Contact	Circuit Name	Mnemonic
Shield	None	1	A	Shield	None
Transmitted Data	BA (A)	2	P	Transmitted Data	103 (A)
Transmitted Data	BA (B)	14	S	Transmitted Data	103 (B)
Received Data	BB (A)	3	R	Received Data	104 (A)
Received Data	BB (B)	16	T	Received Data	104 (A)
Request to Send	CA (A)	4	C	Request to Send	105 (A)
Request to Send	CA (B)	19	C	(1)	
Clear to Send	CB (A)	5	D	Clear to Send	106
Clear to Send	CB (B)	13			
DCE Ready	CC	6	E	Data Set Ready	107
DTE Ready	CD	20	H	Data Terminal Ready	108/1, /2 *(2)*
Signal Common	AB	7	B	Signal Common	102
Received LineSignal Detector	CF (A)	8	F	Data Channel Received Line Signal Detector	109 *(1)*
Received LineSignal Detector	CF (B)	10	F		
Transmit Signal Element Timing (DCE Source)	DB (A)	15	Y	Transmitter Signal	114 (A)
Transmit Signal Element Timing (DCE Source)	DB (B)	12	AA	Transmitter Signal	114 (B)
Receiver Signal Element Timing (DCE Source)	DD (A)	17	V	Receiver Signal Element Timing	115 (A)
Receiver Signal Element Timing (DCE Source)	DD (B)	9	X	Receiver Signal Element Timing	115 (B)
Local Loopback	LL	18	L	Local Loopback	141 *(2)*
Remote Loopback	RL	21	N	Loopback/ Maintenance *(2)*	140
Transmit Signal Element Timing (DTE Source)	DA (A)	24	U	Transmitter Signal Element Timing	113 (A) *(2)*
Transmit Signal Element Timing (DTE Source)	DA (B)	11	W	Transmitter Signal Element Timing	113 (B) *(2)*

RS-530 and Nearest Equivalent CCITT V.35 (Continued)

Circuit Name	EIA-530-A Mnemonic	Contact	CCITT V.35 Contact	Circuit Name	Mnemonic
Test Mode	TM	25	NN	Test Indicator	142
Ring Indicator	CE	22	J	Calling Indicator	125 *(2)*
Signal Common	AC	23	B	Signal Common	102

(1) Special balanced/unbalanced circuitry required between these interfaces.

(2) Not included in CCITT V.35, but are provided in ISO 2593 as optional.

in a DCE does not affect Circuit CF. The ON condition indicates that the DCE is receiving a signal that meets its criteria, which the DCE manufacturer establishes. The OFF condition indicates that no signal is being received. Circuit CF's OFF condition causes Circuit BB (Received Data) to be clamped to the binary ONE (marking) condition.

On half-duplex channels, Circuit CF is held in the OFF condition whenever Circuit CA (Request to Send) is in the ON condition and for a brief interval of time following Circuit CA's transition from ON to OFF.

Circuit CC (DCE Ready) indicates the status of the local DCE; the ON condition does not indicate that a communication channel has been established to a remote data station nor does it indicate the status of any remote station equipment. The OFF condition indicates that the DTE should ignore signals appearing on all other interchange circuits with the exception of Circuit TM (Test Mode). Circuit CC remains in the OFF condition for DCE tests not completed through the DTE/DCE interface. The circuit responds normally (i.e., not clamped OFF) for DCE tests conducted through the DTE/DCE interface.

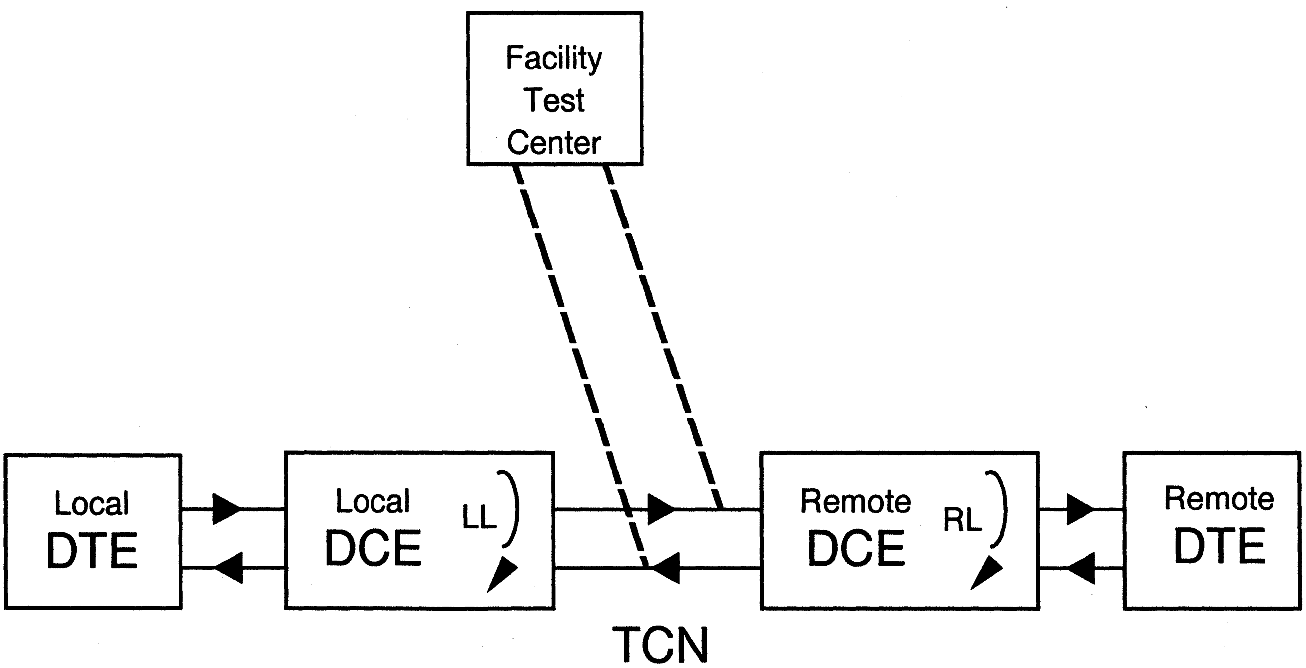
Circuit CD (DTE Ready) controls DCE switching to and from the communications channel. The ON condition prepares the DCE for connection to a communications channel and maintains the connection. The OFF condition removes the DCE from the communication channel following the completion of any "in process" transmission.

Circuit CJ (Ready for Receiving) controls data transfer (flow control) on Circuit BB (Received Data) when an intermediate function, such as error control, is being used in the DCE. The DTE is capable of receiving data when Circuit CJ is ON. When Circuit CJ is implemented, Circuit CA must be considered to be permanently in the ON condition.

Circuit CE (Ring Indicator) indicates when a ringing signal is being received on the communications channel. The ON condition appears approximately coincident with the audible ringing. Furthermore, the DCE may be configured to only respond to specific ringing signals in those systems employing custom ring patterns.

Circuit LL (Local Loopback) controls the local loopback test condition in the local DCE. (See Figure *"Loopback Tests"* for

Figure
Loopback Tests



Local loopback and remote loopback tests as seen from the local DTE.

Circuit Requirements

DTE Control Interchange Circuits	DCE Control Interchange Circuits
CA (Request to Send)	CB (Clear to Send)
LL (Local Loopback)	CF (Receive Line Signal Detector)
RL (Remote Loopback)	TM (Test Mode)
CD (DTE Ready)	CC (DCE Ready)

details.) The ON condition instructs the DCE to transfer its output to its receive signal converter to check local operation. After establishing the LL test condition, the local DTE turns ON Circuit TM. Once TM is ON, the DTE may operate in a duplex mode, using all the circuits in the interface. OFF causes the DCE to release the LL test condition. The LL test does not disable Circuit IC.

Circuit RL (Remote Loopback) controls the remote loopback test function (see Figure *"Loopback Tests"*). This circuit's ON condition causes the local DCE to initiate the RL test on the remote DCE. After turning RL ON and detecting an ON condition on the TM (Test Mode) circuit, the local DTE can operate in a duplex mode using local and remote DCE circuitry. An OFF condition releases the RL condition. While a unit is in RL test condition, communications is out-of-service to the remote DTE. When RL is activated, the DCE presents an OFF condition on Circuit DM and an ON condition on Circuit TM to the DTE. The local DCE presents an ON condition on Circuit TM and allows Circuit DM to respond normally.

Circuit TM (Test Mode) indicates that local DCE is in test condition. ON indicates a test condition, and OFF indicates normal operation. When testing (either LL or RL) is conducted through the local DTE/DCE interface, Circuit CC responds normally; when testing is not conducted through this interface, Circuit CC is held in an OFF condition.

Electrical Characteristics

RS-422-A (balanced operation) and RS-423-A (unbalanced operation) specify the individual interchange circuits' electrical characteristics. EIA-530-A, like RS-449, specifies the mechanical configuration of the connector and the pin assignments and functions of the entire interface, including the timing and interrelationships of the various circuits.

For the purpose of assigning electrical characteristics to the interchange circuits (defined functionally earlier in this report), EIA-530-A has defined two separate categories of circuits. Category I Circuits are as follows:

- Circuit BA (Transmitted Data)
- Circuit BB (Received Data)
- Circuit DA (Transmit Signal Element Timing, DTE Source)
- Circuit DB (Transmit Signal Element Timing, DCE Source)
- Circuit DD (Receiver Signal Element Timing, DCE Source)
- Circuit CA (Request to Send)
- Circuit CB (Clear to Send)
- Circuit CF (Received Line Signal Detector)

The individual Category I Circuits use the balanced electrical characteristics of 422-A. Each circuit has two leads through the interface connector; each interchange circuit contains a pair of wires interconnecting a balanced generator and a differential receiver.

Category II Circuits are as follows:

- Circuit CC (DCE Ready)
- Circuit CD (DTE Ready)
- Circuit LL (Local Loopback)
- Circuit RL (Remote Loopback)
- Circuit TM (Test Mode)

Category II Circuits use the unbalanced electrical characteristics of RS-423-A. Each circuit contains one wire interconnecting an unbalanced generator and a differential receiver. The RS-423-A generators use wave shaping that allows operation over an interface cable length of up to 200 feet (60 meters). The common return for Category II interchange circuits is Circuit AB (Signal Ground).

Certain control interchange circuits require that an ON or OFF voltage be applied to them at all times for proper operation. If the circuit is not associated with an operation generator, a dummy generator must be provided. The circuits involved are as presented in the *"Circuit Requirements"* table.

A dummy generator must meet the appropriate open-circuit, test termination, and short-circuit generator requirements of RS-422-A or RS-423-A. It is implemented using a 2-watt, 47-ohm resistor connected to a DC source of between 4 and 6 volts. A single dummy generator can signal over more than one interchange circuit. Therefore, only two dummy generators are required for both ON and OFF (positive and negative) circuit conditions. The DTE's interface cable must provide separate conductors for each circuit requiring a dummy generator. Two conductors may be used, however: one for the positive dummy generator and the other for the negative dummy generator. An RS-422-A or RS-423-A POWER OFF requirement is required when any of the following circuits uses a dummy generator:

- Circuit CC (DCE Ready),
- Circuit DC (DTE Ready), and
- Circuit CA (Request to Send).

The RS-422-A standard describes the relationship between signaling rate and interface cable distance for balanced interchange circuits. The guidelines specify that operation over 200 feet of cable limits the maximum signaling rate of balanced interchange circuits to 2 million bps. Operation over cable distances greater than 200 feet is possible, but viewed as a tailored application.

In DTEs and DCEs, protective ground is a point that is electrically bonded to the equipment frame. It can also be connected to external grounds through the third wire of the power cord. It should be noted that protective ground (frame ground) is not an

Connector Contact Assignments

Contact Number	Circuit	Interchange Points	Circuit Category	Direction to DCE	Direction from DCE
1	Shield	None	None	Does not apply	Does not apply
2	BA	A-A'	I	X	
3	BB	A-A'	I		X
4	CA/CJ *(1)*	A-A'	I	X	
5	CB	A-A'	I		X
6	CC *(2)*	A-A'	II		X
7	AB	C-C'	None	Does not apply	Does not apply
8	CF	A-A'	I		X
9	DD	B-B'	I		X
10	CF	B-B'	I		X
11	DA	B-B'	I	X	
12	DB	B-B'	I		X
13	CB	B-B'	I		X
14	BA	B-B'	I	X	
15	DB	A-A'	I		X
16	BB	B-B'	I		X
17	DD	A-A'	I		X
18	LL	A-A'	II	X	
19	CA/CJ *(1)*	B-B'	I	X	
20	CD *(2)*	A-A'	II	X	
21	RL	A-A'	II	X	
22	CE	A-A'	II		X
23	AC	C-C'	None	Does not apply	Does not apply
24	DA	A-A'	I	X	
25	TM	A-A'	II		X
26	*(3)*				

(1) When hardware flow control is required, Circuit CA may take on the functionality of Circuit CJ.

(2) Interoperation between Category I and II circuits requires balanced/unbalanced conversion circuitry.

(3) Contact 26 is contained on the Alt A connector only. No connection is to be made to this contact.

interchange circuit in EIA-530-A. If the DCE and DTE equipment frames must be bonded, a separate conductor that conforms to the appropriate national or local electrical codes should be used.

Interface connector pin number 1 facilitates the use of shield interconnecting cable, permitting the DTE cable to carry tandem connectorized sections with shield continuity. The DCE does not connect to pin 1, except in some applications requiring electromagnetic interference (EMI) suppression. While additional provisions may be necessary, they are beyond the scope of this standard.

Proper operation of the interchange circuits requires a path between the DTE circuit ground (circuit common) and the DCE circuit ground, which is provided by Circuit AB (Signal Ground). Normally, both the DTE and DCE should have their circuit grounds connected to protective grounds (frame grounds), which, in turn, may be connected to an external ground, usually associated with the power line plug.

For fail-safe operation, the receivers can detect a POWER OFF condition in the equipment across the interface or a disconnected cable. Detection of either of these conditions is interpreted as an OFF on any of the following interchange circuits:

- Circuit CC (DCE Ready)
- Circuit CA (Request to Send)
- Circuit CD (DTE Ready)

The receiver for each control circuit, except those control circuits specified above, interprets the situation in which the conductor is not implemented in the interconnecting cable as an OFF condition.

Standard Interfaces for Selected Communication System Configuration

Interchange Circuit	Configuration Type SR	Configuration Type SO	Configuration Type RO	Configuration Type DT
AB Signal Ground	M	M	M	M
BA Transmitted Data	M	M	M	M
BB Received Data	M		M	M
DA Transmit Signal Element Timing (DTE Source)	O	O		O
DB Transmit Signal Element Timing (DCE Source)	T	T		T
DD Receiver Signal Element Timing (DCE Source)	T		T	T
CA Request to Send	M	M		
CB Clear to Send	M	M		
CF Received Line Signal Detector	M		M	
CC DCE Ready	M	M	M	
CD DTE Ready	S	S	S	
LL Local Loopback	O			
RL Remote Loopback	O			
TM Test Mode	M	M	M	

M—Mandatory interchange circuits for a given configuration.

T—Additional interchange circuits required for synchronous operation.

S—Additional interchange circuit required for switched service.

O—Optional interchange circuits.

General Signal Characteristics

Interchange circuits transferring data signals across the interface point hold the mark (binary ONE) and space (binary ZERO) conditions for the total nominal duration of each signal element. EIA-334-A, "Signal Quality at Interface Between Data Processing Terminal Equipment and Synchronous Data Communication Equipment for Serial Data Transmission," defines distortion tolerances for synchronous systems. EIA-363, "Standard for Specifying Signal Quality for Transmitting and Receiving Data Processing Terminal Equipment Using Serial Data Transmission at the Interface with Non-Synchronous Communication Equipment," states standard naming procedures for specifying signal quality for nonsynchronous systems. Distortion tolerances for nonsynchronous systems are stated in EIA-404-A, "Standard for Start-Stop Signal Quality Between Data Terminal Equipment and Non-Synchronous Data Communication Equipment." Interchange circuits sending timing signals across the interface point keep ON and OFF conditions for nominally equal amounts of time, in keeping with the acceptable tolerances specified in EIA-334-A.

The accuracy and stability of the timing data on Circuit DD (Receiver Signal Element Timing) are needed only when Circuit CF (Received Line Signal Detector) is ON. During the OFF condition of Circuit CF, drift is acceptable; however, once the OFF to ON transition of Circuit CF occurs, resynchronization of the timing data on Circuit DD must occur as quickly as possible.

Transfer of timing information across the interface is necessary whenever the timing source is capable of generating data, and it should not be restricted only to periods of actual data transmission. When timing data is not provided on a timing interchange circuit, the interchange circuit is clamped in the OFF condition. Tolerances on the relationship between data and associated timing signals follow the EIA-334-A recommendation.

EIA-530-A Interchange Circuit Details

Listed below are details of EIA-530-A's additional functions.

Use of Circuits for Testing

Three interchange circuits permit fault isolation testing done under DTE control: Circuit LL (Local Loopback), Circuit RL (Remote Loopback), and Circuit TM (Test Mode) (see Figure *"Loopback Tests"*).

The EIA considers the (Circuit TM) and test control (Circuit LL and Circuit RL) status circuits a desirable step toward uniform methods of fault isolation. These circuits assist DTE and DCE users in tracking down a defective unit.

Local Loopback (LL Test): This test condition is equivalent to CCITT test loop #3. It provides a way in which a DTE can check the functioning of a DTE-to-DCE interface and the transmit and receive sections of the local DCE. One may also test the local DCE with a test set instead of through the DTE. The output of the transmitting portion of the DCE is returned to the receiving station in the LL test through circuitry that is required for proper operation. In many DCEs, the signal transmitted is unsuitable for direct connection to the receiver. In such cases, an appropriate signal shaping or conversion in the loop-around circuitry may be included so that any element used in normal operations is checked in the test condition.

Remote Loopback (RL Test): This test, equivalent to CCITT test loop #2, allows a DTE or a facility test center to check the transmission path through the remote DCE to the DTE interface and the corresponding return path. In this test, Circuit SD and Circuit RD are either isolated or disconnected from the remote DTE at the interface and then connected to each other at the remote DCE. In synchronous DCEs, a suitable transmit clock may be necessary when the RL test condition is initiated. In some instances, buffer storage may be required between Circuit RD and Circuit SD.

Remote control of the RL test permits the automation of end-to-end testing of any circuit from a central location. Primarily, test control is suitable in point-to-point applications, but may also be used in multipoint arrangements with the addition of an address detection feature in the DCE. Test RL enables circuit verification without the aid of a distant DCE, supported by an inherent remote loopback capability in many modern DCEs.

The ON states of Circuit RL and Circuit LL are mutually exclusive, because the two test conditions may not function simultaneously.

Equalizers

Equalization is a process whereby a circuit's frequency and phase distortions are reduced to compensate for differences in time delay and attenuation of the varying frequencies in the transmission band. An equalizer associated with the DCE may require training, a process that produces a fixed number of equally spaced reference signals.

RS-449 outlines the procedures for equalizer training. The following example outlines a typical training sequence. DCE ″E″ (East) has an equalizer that requires training. DCE ″W″ (West) is transmitting toward DCE ″E″. Initial training of DCE ″Es″ equalizer occurs during the interval between the ON condition of Circuit RS and the ON condition of Circuit CS of DCE ″W″. Initial training in the DCE ″Es″ receiver occurs prior to the ON condition of Circuit RR of DCE ″E″. Circuit SQ is placed in the ON condition no later than the OFF-to-ON transition of Circuit RR if the initial training is successful. Circuit SQ's state is undefined when Circuit RR is OFF.

If the equalizer requires a unique training signal from DCE ″W″ to achieve equalization, the states of specific interchange circuits are controlled during this process. When the normal flow of data toward DCE ″W″ is interrupted in order to cause DCE ″W″ to transmit this unique sequence, Circuit CS of DCE ″E″ is held in the OFF condition while the command signal is being sent. In this situation, Circuit SQ of DCE ″W″ should be placed in the OFF condition while receiving the command signal. Circuit RD of DCE ″W″ may be clamped to the marking condition while the command signal is received. In the reverse direction, Circuit CS of DCS ″W″ is in the OFF condition while the unique training signal is sent. Circuit RD of DCE ″E″ may be clamped to the marking condition when the unique training signal is received. When the equalizer attains proper adjustment, DCE ″E″ places Circuit SQ in the ON condition.

Standard Interfaces for Selected Configurations

Standard sets of interchange circuits for data transmission configurations are defined as follows: Type SR (Send-Receive), Type SO (Send-Only), Type RO (Receive-Only), and Type DT (Data and Timing only). Table ″*Standard Interfaces for Selected Communication System Configuration*″ lists the interchange circuits that must be provided for each data transmission configuration. For a given type of interface, generators and receivers must be provided for every interchange circuit designated M (Mandatory) in Table ″*Standard Interfaces for Selected Communication System Configuration.*″ In addition, generators and receivers are necessary for all interchange circuits designated S and T, where the service is switched and synchronous, respectively. ■

ANSI EIA/TIA-530-A

In this report:

Note: In June 1992 the Electronic Industries Assn. published ANSI EIA/TIA-530-A (1992), which is a revision of ANSI EIA-530 (1987).

Datapro Summary

ANSI EIA/TIA-530-A (hereafter EIA-530-A) defines the mechanical interface characteristics between Data Termination Equipment (DTE) and Data Circuit-Terminating Equipment (DCE). It operates in conjunction with RS-422-A and RS-423-A, which define the electrical operation of the individual interchange circuits for balanced and unbalanced operation, respectively. EIA-530-A complements RS-232-D for data rates above 20K bps and replaces RS-449 for data rates above 20K bps.

A revision of EIA-530, EIA-530-A was approved in May 1992 and includes several relatively minor modifications to the previous standard. The most significant change accounts for the alternative 26-position interface connector (Alt A). Other revisions comprise the following:

- Addition of Circuits CJ (Ready for Receiving), CE (Ring Indicator), and AC (Signal Common).
- Use of Circuit CB (Clear to Send) for hardware flow control.
- Use of Local Loopback for "Busy Out."
- Change of Circuits CC (DCE Ready) and CD (DTE Ready) to Category II Circuits.

The new standard is compatible with EIA-530, but applications connecting versions of RS-449 or EIA-530 (with Category I Circuits CC and CD) with EIA-530-A (with Category II Circuits CC and CD) require an unbalanced/balanced converter between the interfaces (see Table 1 for circuitry connections).

In 1977 the Electronic Industries Assn. (EIA) developed the RS-449, RS-422, and RS-423 standards to eventually replace RS-232-C. RS-449, however, never really caught on and, in March 1987, EIA-530 was introduced as its intended replacement. RS-422 and RS-423 remain in the revised forms of RS-422-A and RS-423-A. RS-232-C also outlasted RS-449 and, in January 1987, the EIA issued RS-232-D, a revision for RS-232-C.

EIA-530-A governs the mechanical and electrical characteristics of the interface between Data Terminal Equipment (DTE) and Data Circuit-Terminating Equipment (DCE). The standard defines DTE as the hardware on the business machine side of the interface (teleprinters, display terminals, front-end processors, central processing units, etc.), and DCE as the modem, signal converter, or other device between the DTE and the communications line.

This report compares EIA-530-A with RS-232-D, RS-449, and CCITT V.35. It also discusses the mechanical and electrical characteristics and looks at the general classification of interchange circuits and outlines interchange circuit details.

Copies of EIA-530-A, RS-422-A, and RS-423-A can be obtained from the Electronic Industries Assn., 2001 I Street NW, Washington, DC 20006.

—By Vance Macdonald
Research Analyst

Analysis

EIA-530-A operates in conjunction with either of two standards specifying electrical

Table 1. Interconnecting EIA RS-530-A With EIA RS-449

EIA-530-A			EIA-RS-449		
Circuit Name	**Mnemonic**	**Contact**	**Contact**	**Mnemonic**	**Circuit Name**
Shield	None	1	1	None	Shield
Transmitted Data	BA (A) BA (B)	2 14	4 22	SD (A) SD (B)	Send Data
Received Data	BB (A) BB (B)	3 16	6 24	RD (A) RD (B)	Receive Data
Request to Send	CA (A) CA (B)	4 19	7 25	RS (A) RS (B)	Request to Send
Clear to Send	CB (A) CB (B)	5 13	9 27	CS (A) CS (B)	Clear to Send
DCE Ready	CC	6	11 29	DM (A) DM (B)	Data Mode *(1)*
DTE Ready	CD	20	12 30	TR (A) TR (B)	Terminal Ready *(2)*
Signal Common	AB	7	19	SG	Signal Ground *(2)*
Received Line Signal Detector	CF (A) CF (B)	8 10	13 31	RR (A) RR (B)	Receiver Ready
Transmit Signal Element Timing (DCE Source)	DB (A) DB (B)	15 12	5 23	ST (A) ST (B)	Send Timing
Receiver Signal Element Timing (DCE Source)	DD (A) DD (B)	17 9	8 26	RT (A) RT (B)	Receive Timing
Local Loopback	LL	18	10	LL	Local Loopback
Remote Loopback	RL	21	14	RL	Remote Loopback
Transmit Signal Element Timing (DTE Source)	DA (A) DA (B)	24 11	17 35	TT (A) TT (B)	Terminal Timing
Test Mode	TM	25	18	TM	Test Mode
Ring Indicator	CE	22	15	IC	Incoming Call
Signal Common	AC	23	20	RC	Receive Common *(1)*
			37	SC	Send Common *(2)*

(1) For proper operation with an EIA-449 DTE, connect contacts 20 and 29.
(2) For proper operation with an EIA-449 DCE, connect contacts 19, 30, and 37.

Source: Electronic Industries Assn. EIA/TIA-530-A, 1992.

characteristics: RS-422-A, for balanced circuits; and RS-423-A, for unbalanced circuits. When each interface circuit has its own ground lead, the circuit is balanced. When an interface uses a common or shared grounding technique, it is unbalanced.

EIA-530-A is used for data communications systems with the following characteristics:

- DTE serializes data bits, and the DCE puts no restrictions on the DTE's bit sequence arrangements.
- Communication is binary, serial, synchronous, or asynchronous, and control information is exchanged on separate circuits.
- Equipment on one side of the DTE/DCE interface connects directly to equipment on the other side without additional technical considerations.
- Communication is in half- and/or full-duplex modes in point-to-point or multipoint configurations over two- or four-wire facilities with data rates ranging from 20K bps to a nominal upper limit of 2.1M bps. Point-to-point arrangements may operate on either switched or dedicated facilities. Dedicated lines connect multipoint arrangements.

Applications in which cable termination, signal wave shaping, interconnection cable distance, and the interface's mechanical configurations must be tailored to meet specific user needs are not precluded, but are generally not within the standard's scope. The EIA-530-A connector, also used for RS-232-D, uses electrical characteristics that, if improperly connected to some silicon devices designed to meet the RS-422-A and RS-423-A electrical characteristics specified in this recommendation, could damage those devices.

EIA-530-A/RS-232-D

These standards include a specification of the D-shaped 25-pin interface connector, which RS-232-C had only referenced in an appendix and never included as part of the standard. Both standards support testing of both local and remote DCEs through the Local Loopback, Remote Loopback, and Test Mode circuits. Circuit names for the first 8 pins in both standards are the same, but differ on pins 9, 10, and 11, which are not used in RS-232-D.

RS-530-A achieves higher data rates than RS-232-D (greater than 20K bps) by specifying the use of balanced signals, while sacrificing some secondary signals and the Ring Indicator. The Ring Indicator's elimination indicates that EIA-530-A is not for use in dial-up applications.

EIA-530-A/RS-449

The EIA-530-A standard has officially replaced RS-449 but, while both standards are in use, EIA-530-A can be interconnected with RS-449 devices through a connecting cable or adaptor. Table 1 lists the circuit name and mnemonic, and connector contact pin for each interface.

EIA-530-A/CCITT V.35

EIA-530-A provides balanced (EIA-422-A) generators and receivers on interchange Circuits CA (Request to Send), CB (Clear to Send), and CF (Receive Line Signal Detector). The corresponding interchange circuits in a V.35 interface utilize CCITT V.28 (EIA-232-E) electrical characteristics. In applications connecting an EIA-422-A balanced generator with an EIA-232-E unbalanced receiver, a special balanced/unbalanced converter must be employed between the interfaces. Otherwise, EIA-530-A and CCITT V.35 are fully compatible.

Mechanical Characteristics

The point of demarcation between the DTE and the DCE is at connector plugs on the DCE or at an interface point no further than ten feet (three meters) from the DCE. A 25-position connector was specified for all interchange circuits in EIA-530. EIA-530-A's alternative 26-position "Alt A" connector is specified for use when a smaller physical connector is required (it is approximately ¾" x ¼"). In all cases, the DTE provides the cable (up to 200 feet), which has male (pin) contacts and a female shell (plug connector); the DCE has a female connector. The connectors are equipped with a block that permits latching and unlatching without a tool. The latching block also permits the use of screws to fasten the connectors together. The mechanical configuration for connections of the interface cable at points other than the demarcation point is not specified.

When additional functions are offered in a separate unit that is inserted between the DTE and DCE, the female connector is associated with the DTE interface, while the male connector is a DCE interface.

Functional Description of Interchange Circuits

Interchange circuits fall into four general classifications: ground (or common return), data circuits, control circuits, and timing circuits. Table 2 outlines a list of EIA-530-A interchange circuits showing mnemonic name, circuit identification, circuit direction, and circuit type. Table 3 compares the connector pin assignments and the functional interchange circuits along with an equivalency table showing the nearest equivalent CCITT V.35 functions in relation to each EIA-530-A function. A functional description of each of the EIA-530-A interchange circuits follows.

Ground or Common Return Circuits

Circuit AB and AC (Signal Commons) connects the DTE circuit ground (signal common) to the DCE circuit ground (signal common) to provide a conductive route between the DTE and DCE signal commons.

Data Circuits

Circuit BA (Transmitted Data) transfers the data signals originated by the DTE to the DCE. The DTE holds Circuit BA in the binary ONE (marking) condition unless an ON condition is present on all of the following circuits: CA (Request to Send), CB (Clear to Send), CC (DCE Ready), and CD (DTE Ready). The DCE disregards any signal appearing on Circuit BA when an OFF condition exists on one or more of these circuits. While an ON condition is maintained on each of the circuits, the DCE sends all data signals transmitted across the interface on Circuit BA to the communications channel. The term "data signals" includes the binary ONE (marking) condition, reversals, and other sequences, such as SYN coded characters that maintain timing synchronization.

Circuit BB (Received Data) transfers DCE-generated data signals to the DTE in response to line signals from a remote station. Circuit BB is held in the binary ONE (marking) condition while Circuit CF (Receive Line Signal Detector) is in the OFF condition. On half-duplex channels, Circuit BB is held in the marking condition when Circuit CA is ON and for a brief interval when Circuit CA

Table 2. EIA RS-530-A Interchange Circuits

Circuit Mnemonic	Circuit Name	Circuit Detection	Circuit Type
AB	Signal Common	Does not apply	Common
AC	Signal Common	Does not apply	Common
BA	Transmitted Data	To DCE	Data
BB	Received Data	From DCE	Data
DA	Transmit Signal Element Timing (DTE Source)	To DCE	Timing
DB	Transmit Signal Element Timing (DCE Source)	From DCE	Timing
DD	Receiver Signal Element Timing (DCE Source)	From DCE	Timing
CA	Request to Send	To DCE	Control
CB	Clear to Send	From DCE	Control
CF	Received Line Signal Detector	From DCE	Control
CJ	Ready for Receiving	To DCE	Control
CE	Ring Indicator	From DCE	Control
CC	DCE Ready	From DCE	Control
CD	DTE Ready	To DCE	Control
LL	Local Loopback	To DCE	Timing
RL	Remote Loopback	To DCE	Timing
TM	Test Mode	From DCE	Timing

Source: Electronic Industries Assn. EIA/TIA-530-A, 1992.

makes the transition from ON to OFF. This allows for the completion of the transmission and for the decay of channel reflections.

Timing Circuits

Circuit DA (Transmit Signal Element Timing—DTE Source) provides the DCE with transmit signal element timing data. The ON to OFF transition nominally indicates the center of each signal element on Circuit BA. When Circuit DA is implemented in the DTE, the DTE provides timing data on it whenever the DTE is in a POWER ON condition. The DTE can withhold timing data on this circuit for short periods as long as Circuit CA is in the OFF condition.

Circuit DB (Transmit Signal Element Timing—DCE Source) provides the DTE with transmit element timing data. The DTE provides a data signal on Circuit BA in which the transitions between signal elements occur at the time of the transitions from OFF to ON condition of the signal on Circuit DB. The DCE provides timing data on Circuit DB whenever the DCE is in a POWER ON condition. The DCE can withhold timing data on this circuit if Circuit CC is in the OFF condition.

Circuit DD (Receiver Signal Element Timing—DCE Source) provides the DTE with receive signal element timing data. The DCE provides timing data on this circuit whenever the DCE is in a POWER ON condition. The DCE can withhold timing data on this circuit for short periods as long as Circuit CC is in the OFF condition.

Control Circuits

Circuit CA (Request to Send) controls the transmit function of the local DCE and, on half-duplex channels, the direction of data transmission. On one-way-only (duplex) channels, the ON condition holds the DCE in the transmit mode; the OFF condition suppresses transmission. On a half-duplex channel, the ON condition holds the DCE in the transmit mode and suppresses the receive mode. The OFF condition holds the DCE in the receive mode. A transition from OFF to ON instructs the DCE to enter the transmit mode. The DCE responds by taking any necessary action and indicating completion of such action by turning ON Circuit CB (Clear to Send), thereby permitting the DTE to transfer data across Circuit BA. A transition from ON to OFF instructs the DCE to complete transmission of all data previously transferred across the interface on Circuit BA (Transmitted Data) and then to assume a nontransmit, or receive mode, as appropriate. The DCE responds to this instruction by turning OFF Circuit CB.

When Circuit CA is turned OFF, it is not turned ON again until Circuit CB has been turned OFF by the DCE. An ON condition is required on Circuit CA, as well as on Circuits CB and CC, whenever data is transferred across the interface on Circuit BA by the DTE. Circuit CA may be turned ON at any time when Circuit CB is OFF, regardless of the status of any other interface circuit.

Circuit CB (Clear to Send) indicates that the DCE has been conditioned to transmit data over the communications channel. The ON condition, together with the ON on Circuit CA (Request to Send) and Circuit CC (DCE Ready), indicates to the DTE that signals on Circuit BA (Transmitted Data) will be transmitted to the communication channel. The OFF condition indicates that the DTE should not transfer data across the interface on Circuit BA, since this data will not be transmitted to the line. The ON condition of Circuit CB is a response to the occurrence of concurrent ON conditions on Circuits CC and CA, delayed as appropriate by the DCE, to allow the establishment of a data communications channel to a remote DTE. Circuit CB may be turned OFF during the data transfer or test phase, independent of Circuit CA's condition, to signal the DTE to interrupt the transfer of data on Circuit BA for a finite period of time. This capability, added in EIA-530-A, provides for DCE flow control or DCE/DCE resynchronization.

Circuit CF (Received Line Signal Detector) indicates whether the receiver in the DCE is ready to receive data

Table 3. RS-530 and Nearest Equivalent CCITT V.35

EIA-530-A			CCITT V.35		
Circuit Name	**Mnemonic**	**Contact**	**Contact**	**Circuit Name**	**Mnemonic**
Shield	None	1	A	Shield	None
Transmitted Data	BA (A)	2	P	Transmitted Data	103 (A)
Transmitted Data	BA (B)	14	S	Transmitted Data	103 (B)
Received Data	BB (A)	3	R	Received Data	104 (A)
Received Data	BB (B)	16	T	Received Data	104 (A)
Request to Send	CA (A)	4	C	Request to Send	105 (A)
Request to Send	CA (B)	19	C	*(1)*	
Clear to Send	CB (A)	5	D	Clear to Send	106
Clear to Send	CB (B)	13			
DCE Ready	CC	6	E	Data Set Ready	107
DTE Ready	CD	20	H	Data Terminal Ready	108/1, /2 *(2)*
Signal Common	AB	7	B	Signal Common	102
Received Line Signal Detector	CF (A)	8	F	Data Channel Received Line Signal Detector	109 *(1)*
Received Line Signal Detector	CF (B)	10	F		
Transmit Signal Element Timing (DCE Source)	DB (A)	15	Y	Transmitter Signal	114 (A)
Transmit Signal Element Timing (DCE Source)	DB (B)	12	AA	Transmitter Signal	114 (B)
Receiver Signal Element Timing (DCE Source)	DD (A)	17	V	Receiver Signal Element Timing	115 (A)
Receiver Signal Element Timing (DCE Source)	DD (B)	9	X	Receiver Signal Element Timing	115 (B)
Local Loopback	LL	18	L	Local Loopback	141 *(2)*
Remote Loopback	RL	21	N	Loopback/ Maintenance *(2)*	140

signals from the communication channel, but does not indicate the relative quality of the data signals received. An equalizer's condition in a DCE does not affect Circuit CF. The ON condition indicates that the DCE is receiving a signal that meets its criteria, which the DCE manufacturer establishes. The OFF condition indicates that no signal is being received. Circuit CF's OFF condition causes Circuit BB (Received Data) to be clamped to the binary ONE (marking) condition.

On half-duplex channels, Circuit CF is held in the OFF condition whenever Circuit CA (Request to Send) is in the ON condition and for a brief interval of time following Circuit CA's transition from ON to OFF.

Table 3. RS-530 and Nearest Equivalent CCITT V.35 (Continued)

EIA-530-A			CCITT V.35		
Circuit Name	**Mnemonic**	**Contact**	**Contact**	**Circuit Name**	**Mnemonic**
Transmit Signal Element Timing (DTE Source)	DA (A)	24	U	Transmitter Signal Element Timing	113 (A) *(2)*
Transmit Signal Element Timing (DTE Source)	DA (B)	11	W	Transmitter Signal Element Timing	113 (B) *(2)*
Test Mode	TM	25	NN	Test Indicator	142
Ring Indicator	CE	22	J	Calling Indicator	125 *(2)*
Signal Common	AC	23	B	Signal Common	102

(1) Special balanced/unbalanced circuitry required between these interfaces.
(2) Not included in CCITT V.35, but are provided in ISO 2593 as optional.

Source: Electronic Industries Assn. EIA/TIA-530-A, 1992.

Circuit CC (DCE Ready) indicates the status of the local DCE; the ON condition does not indicate that a communication channel has been established to a remote data station nor does it indicate the status of any remote station equipment. The OFF condition indicates that the DTE should ignore signals appearing on all other interchange circuits with the exception of Circuit TM (Test Mode). Circuit CC remains in the OFF condition for DCE tests not completed through the DTE/DCE interface. The circuit responds normally (i.e., not clamped OFF) for DCE tests conducted through the DTE/DCE interface.

Circuit CD (DTE Ready) controls DCE switching to and from the communications channel. The ON condition prepares the DCE for connection to a communications channel and maintains the connection. The OFF condition removes the DCE from the communication channel following the completion of any "in process" transmission.

Circuit CJ (Ready for Receiving) controls data transfer (flow control) on Circuit BB (Received Data) when an intermediate function, such as error control, is being used in the DCE. The DTE is capable of receiving data when Circuit CJ is ON. When Circuit CJ is implemented, Circuit CA must be considered to be permanently in the ON condition.

Circuit CE (Ring Indicator) indicates when a ringing signal is being received on the communications channel. The ON condition appears approximately coincident with the audible ringing. Furthermore, the DCE may be configured to only respond to specific ringing signals in those systems employing custom ring patterns.

Circuit LL (Local Loopback) controls the local loopback test condition in the local DCE. (See Figure 1 for details.) The ON condition instructs the DCE to transfer its output to its receive signal converter to check local operation. After establishing the LL test condition, the local DTE turns ON Circuit TM. Once TM is ON, the DTE may operate in a duplex mode, using all the circuits in the interface. OFF causes the DCE to release the LL test condition. The LL test does not disable Circuit IC.

Circuit RL (Remote Loopback) controls the remote loopback test function (see Figure 1). This circuit's ON condition causes the local DCE to initiate the RL test on the remote DCE. After turning RL ON and detecting an ON condition on the TM (Test Mode) circuit, the local DTE can operate in a duplex mode using local and remote DCE circuitry. An OFF condition releases the RL condition. While a unit is in RL test condition, communications is out-of-service to the remote DTE. When RL is activated, the DCE presents an OFF condition on Circuit DM and an ON condition on Circuit TM to the DTE. The local DCE presents an ON condition on Circuit TM and allows Circuit DM to respond normally.

Circuit TM (Test Mode) indicates that local DCE is in test condition. ON indicates a test condition, and OFF indicates normal operation. When testing (either LL or RL) is conducted through the local DTE/DCE interface, Circuit CC responds normally; when testing is not conducted through this interface, Circuit CC is held in an OFF condition.

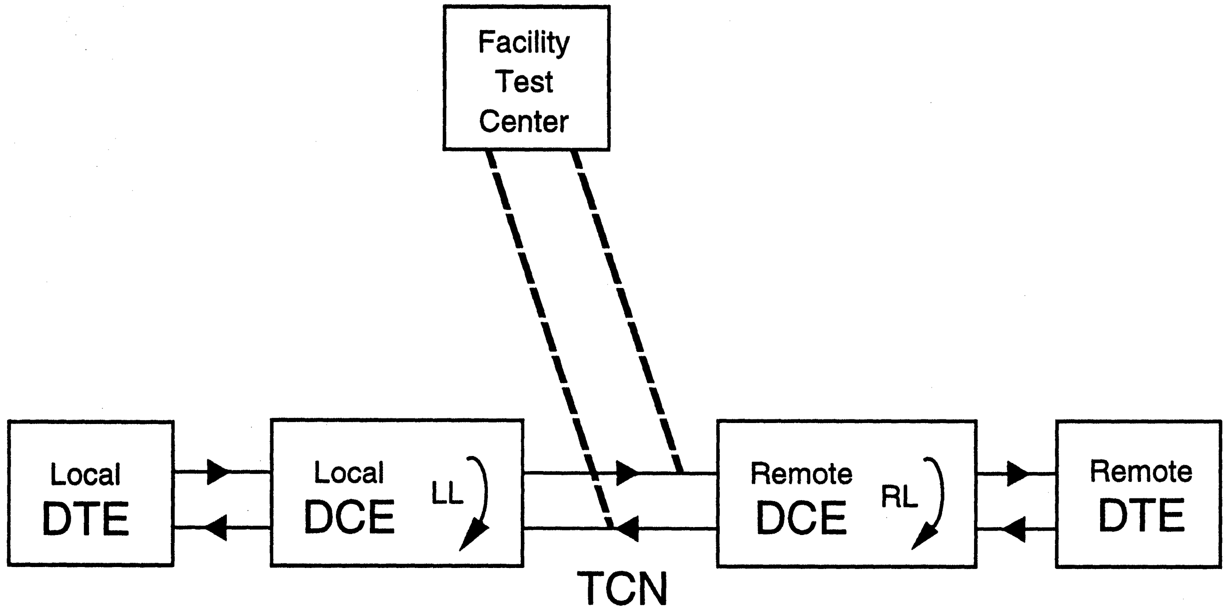
Electrical Characteristics

RS-422-A (balanced operation) and RS-423-A (unbalanced operation) specify the individual interchange circuits' electrical characteristics. EIA-530-A, like RS-449, specifies the mechanical configuration of the connector and the pin assignments and functions of the entire interface, including the timing and interrelationships of the various circuits.

For the purpose of assigning electrical characteristics to the interchange circuits (defined functionally earlier in this report), EIA-530-A has defined two separate categories of circuits. *Category I Circuits* are as follows:

- Circuit BA (Transmitted Data)
- Circuit BB (Received Data)
- Circuit DA (Transmit Signal Element Timing, DTE Source)

Figure 1.
Loopback Tests



Local loopback and remote loopback tests as seen from the local DTE.

- Circuit DB (Transmit Signal Element Timing, DCE Source)
- Circuit DD (Receiver Signal Element Timing, DCE Source)
- Circuit CA (Request to Send)
- Circuit CB (Clear to Send)
- Circuit CF (Received Line Signal Detector)

The individual Category I circuits use the balanced electrical characteristics of 422-A. Each circuit has two leads through the interface connector; each interchange circuit contains a pair of wires interconnecting a balanced generator and a differential receiver.

Category II Circuits are as follows:

- Circuit CC (DCE Ready)
- Circuit CD (DTE Ready)
- Circuit LL (Local Loopback)
- Circuit RL (Remote Loopback)
- Circuit TM (Test Mode)

Category II Circuits use the unbalanced electrical characteristics of RS-423-A. Each circuit contains one wire interconnecting an unbalanced generator and a differential receiver. The RS-423-A generators use wave shaping that allows operation over an interface cable length of up to 200 feet (60 meters). The common return for Category II interchange circuits is Circuit AB (Signal Ground).

Certain control interchange circuits require that an ON or OFF voltage be applied to them at all times for proper operation. If the circuit is not associated with an operation generator, a dummy generator must be provided. The circuits involved are as presented here:

DTE Control Interchange Circuits	DCE Control Interchange Circuits
CA (Request to Send)	CB (Clear to Send)
LL (Local Loopback)	CF (Received Line Signal Detector)
RL (Remote Loopback)	TM (Test Mode)
CD (DTE Ready)	CC (DCE Ready)

A dummy generator must meet the appropriate open-circuit, test termination, and short-circuit generator requirements of RS-422-A or RS-423-A. It is implemented using a 2-watt, 47-ohm resistor connected to a DC source of between 4 and 6 volts. A single dummy generator can signal over more than one interchange circuit. Therefore, only two dummy generators are required for both ON and OFF (positive and negative) circuit conditions. The DTE's interface cable must provide separate conductors for each circuit requiring a dummy generator. Two conductors may be used, however: one for the positive dummy generator and the other for the negative dummy generator. An RS-422-A or RS-423-A POWER OFF requirement is required when any of the following circuits uses a dummy generator:

- Circuit CC (DCE Ready),
- Circuit DC (DTE Ready), and
- Circuit CA (Request to Send).

The RS-422-A standard describes the relationship between signaling rate and interface cable distance for balanced interchange circuits. The guidelines specify that operation over 200 feet of cable limits the maximum signaling rate of balanced interchange circuits to 2 million bps. Operation over cable distances greater than 200 feet is possible, but viewed as a tailored application.

Table 4. Connector Contact Assignments

Contact Number	Circuit	Interchange Points	Circuit Category	Direction to DCE	Direction from DCE
1	Shield	None	None	Does not apply	Does not apply
2	BA	A-A'	I	X	
3	BB	A-A'	I		X
4	CA/CJ *(1)*	A-A'	I	X	
5	CB	A-A'	I		X
6	CC *(2)*	A-A'	II		X
7	AB	C-C'	None	Does not apply	Does not apply
8	CF	A-A'	I		X
9	DD	B-B'	I		X
10	CF	B-B'	I		X
11	DA	B-B'	I	X	
12	DB	B-B'	I		X
13	CB	B-B'	I		X
14	BA	B-B'	I	X	
15	DB	A-A'	I		X
16	BB	B-B'	I		X
17	DD	A-A'	I		X
18	LL	A-A'	II	X	
19	CA/CJ *(1)*	B-B'	I	X	
20	CD *(2)*	A-A'	II	X	
21	RL	A-A'	II	X	
22	CE	A-A'	II		X
23	AC	C-C'	None	Does not apply	Does not apply
24	DA	A-A'	I	X	
25	TM	A-A'	II		X
26	*(3)*				

(1) When hardware flow control is required, Circuit CA may take on the functionality of Circuit CJ.
(2) Interoperation between Category I and II circuits requires balanced/unbalanced conversion circuitry.
(3) Contact 26 is contained on the Alt A connector only. No connection is to be made to this contact.

Source: Electronic Industries Assn. EIA/TIA-530-A, 1992.

In DTEs and DCEs, protective ground is a point that is electrically bonded to the equipment frame. It can also be connected to external grounds through the third wire of the power cord. It should be noted that protective ground (frame ground) is not an interchange circuit in EIA-530-A. If the DCE and DTE equipment frames must be bonded, a separate conductor that conforms to the appropriate national or local electrical codes should be used.

Interface connector pin number 1 facilitates the use of shield interconnecting cable, permitting the DTE cable to carry tandem connectorized sections with shield continuity. The DCE does not connect to pin 1, except in some applications requiring electromagnetic interference (EMI) suppression. While additional provisions may be necessary, they are beyond the scope of this standard.

Proper operation of the interchange circuits requires a path between the DTE circuit ground (circuit common) and the DCE circuit ground, which is provided by Circuit AB (Signal Ground). Normally, both the DTE and DCE should have their circuit grounds connected to protective grounds (frame grounds), which, in turn, may be connected to an external ground, usually associated with the power line plug.

For fail-safe operation, the receivers can detect a POWER OFF condition in the equipment across the interface or a disconnected cable. Detection of either of these conditions is interpreted as an OFF on any of the following interchange circuits:

Table 5. Standard Interfaces for Selected Communication System Configuration

Interchange Circuit	Configuration Type SR	Configuration Type SO	Configuration Type RO	Configuration Type DT
AB Signal Ground	M	M	M	M
BA Transmitted Data	M	M	M	M
BB Received Data	M		M	M
DA Transmit Signal Element Timing (DTE Source)	O	O		O
DB Transmit Signal Element Timing (DCE Source)	T	T		T
DD Receiver Signal Element Timing (DCE Source)	T		T	T
CA Request to Send	M	M		
CB Clear to Send	M	M		
CF Received Line Signal Detector	M		M	
CC DCE Ready	M	M	M	
CD DTE Ready	S	S	S	
LL Local Loopback	O			
RL Remote Loopback	O			
TM Test Mode	M	M	M	

M—Mandatory interchange circuits for a given configuration.
T—Additional interchange circuits required for synchronous operation.
S—Additional interchange circuit required for switched service.
O—Optional interchange circuits.

- Circuit CC (DCE Ready)
- Circuit CA (Request to Send)
- Circuit CD (DTE Ready)

The receiver for each control circuit, except those control circuits specified above, interprets the situation in which the conductor is not implemented in the interconnecting cable as an OFF condition.

General Signal Characteristics

Interchange circuits transferring data signals across the interface point hold the mark (binary ONE) and space (binary ZERO) conditions for the total nominal duration of each signal element. EIA-334-A, "Signal Quality at Interface Between Data Processing Terminal Equipment and Synchronous Data Communication Equipment for Serial Data Transmission," defines distortion tolerances for synchronous systems. EIA-363, "Standard for Specifying Signal Quality for Transmitting and Receiving Data Processing Terminal Equipment Using Serial Data Transmission at the Interface with Non-Synchronous Communication Equipment," states standard naming procedures for specifying signal quality for nonsynchronous systems. Distortion tolerances for nonsynchronous systems are stated in EIA-404-A, "Standard for Start-Stop Signal Quality Between Data Terminal Equipment and Non-Synchronous Data Communication Equipment." Interchange circuits sending timing signals across the interface point keep ON and OFF conditions for nominally equal amounts of time, in keeping with the acceptable tolerances specified in EIA-334-A.

The accuracy and stability of the timing data on Circuit DD (Receiver Signal Element Timing) are needed only when Circuit CF (Received Line Signal Detector) is ON. During the OFF condition of Circuit CF, drift is acceptable; however, once the OFF to ON transition of Circuit CF occurs, resynchronization of the timing data on Circuit DD must occur as quickly as possible.

Transfer of timing information across the interface is necessary whenever the timing source is capable of generating data, and it should not be restricted only to periods of actual data transmission. When timing data is not provided on a timing interchange circuit, the interchange circuit is clamped in the OFF condition. Tolerances on the relationship between data and associated timing signals follow the EIA-334-A recommendation.

EIA-530-A Interchange Circuit Details

Listed below are details of EIA-530-A's additional functions.

Use of Circuits for Testing

Three interchange circuits permit fault isolation testing done under DTE control: Circuit LL (Local Loopback), Circuit RL (Remote Loopback), and Circuit TM (Test Mode) (see Figure 1).

The EIA considers the (Circuit TM) and test control (Circuit LL and Circuit RL) status circuits a desirable step toward uniform methods of fault isolation. These circuits assist DTE and DCE users in tracking down a defective unit.

Local Loopback (LL Test): This test condition is equivalent to CCITT test loop #3. It provides a way in which a DTE can check the functioning of a DTE-to-DCE interface and the transmit and receive sections of the local DCE. One may also test the local DCE with a test set instead of through the DTE. The output of the transmitting portion of the DCE is returned to the receiving station in the LL test through circuitry that is required for proper operation. In many DCEs, the signal transmitted is unsuitable for direct connection to the receiver. In such cases, an appropriate signal shaping or conversion in the loop-around circuitry may be included so that any element used in normal operations is checked in the test condition.

Remote Loopback (RL Test): This test, equivalent to CCITT test loop #2, allows a DTE or a facility test center to check the transmission path through the remote DCE to the DTE interface and the corresponding return path. In this test, Circuit SD and Circuit RD are either isolated or disconnected from the remote DTE at the interface and then connected to each other at the remote DCE. In synchronous DCEs, a suitable transmit clock may be necessary when the RL test condition is initiated. In some instances, buffer storage may be required between Circuit RD and Circuit SD.

Remote control of the RL test permits the automation of end-to-end testing of any circuit from a central location. Primarily, test control is suitable in point-to-point applications, but may also be used in multipoint arrangements with the addition of an address detection feature in the DCE. Test RL enables circuit verification without the aid of a distant DCE, supported by an inherent remote loopback capability in many modern DCEs.

The ON states of Circuit RL and Circuit LL are mutually exclusive, because the two test conditions may not function simultaneously.

Equalizers

Equalization is a process whereby a circuit's frequency and phase distortions are reduced to compensate for differences in time delay and attenuation of the varying frequencies in the transmission band. An equalizer associated with the DCE may require training, a process that produces a fixed number of equally spaced reference signals.

RS-449 outlines the procedures for equalizer training. The following example outlines a typical training sequence. DCE "E" (East) has an equalizer that requires training. DCE "W" (West) is transmitting toward DCE "E". Initial training of DCE "Es" equalizer occurs during the interval between the ON condition of Circuit RS and the ON condition of Circuit CS of DCE "W". Initial training in the DCE "Es" receiver occurs prior to the ON condition of Circuit RR of DCE "E". Circuit SQ is placed in the ON condition no later than the OFF-to-ON transition of Circuit RR if the initial training is successful. Circuit SQ's state is undefined when Circuit RR is OFF.

If the equalizer requires a unique training signal from DCE "W" to achieve equalization, the states of specific interchange circuits are controlled during this process. When the normal flow of data toward DCE "W" is interrupted in order to cause DCE "W" to transmit this unique sequence, Circuit CS of DCE "E" is held in the OFF condition while the command signal is being sent. In this situation, Circuit SQ of DCE "W" should be placed in the OFF condition while receiving the command signal. Circuit RD of DCE "W" may be clamped to the marking condition while the command signal is received. In the reverse direction, Circuit CS of DCS "W" is in the OFF condition while the unique training signal is sent. Circuit RD of DCE "E" may be clamped to the marking condition when the unique training signal is received. When the equalizer attains proper adjustment, DCE "E" places Circuit SQ in the ON condition.

Standard Interfaces for Selected Configurations

Standard sets of interchange circuits for data transmission configurations are defined as follows: Type SR (Send-Receive), Type SO (Send-Only), Type RO (Receive-Only), and Type DT (Data and Timing only). Table 5 lists the interchange circuits that must be provided for each data transmission configuration. For a given type of interface, generators and receivers must be provided for every interchange circuit designated M (Mandatory) in Table 5. In addition, generators and receivers are necessary for all interchange circuits designated S and T, where the service is switched and synchronous, respectively. ■

EIA RS-530

[redacted]

In this report:

Note: The subject of this report is considered as a mature standard. No significant developments are anticipated, but because of its importance in the industry, coverage is being continued.

EIA RS-530, approved in March 1987, defines the mechanical interface characteristics between Data Termination Equipment (DTE) and Data Circuit-Terminating Equipment (DCE). It operates in conjunction with RS-422-A and RS-423-A, which define the electrical operation of the individual interchange circuits for balanced and unbalanced operation, respectively. EIA RS-530 complements EIA RS-232-D for data rates above 20K bps and will gradually replace RS-449 for data rates above 20K bps.

Highlights

In 1977, the Electronic Industries Association (EIA) developed the RS-449, RS-422, and RS-423 standards to eventually replace RS-232-C. RS-449, however, never really caught on and, in March 1987, EIA RS-530 was introduced as its intended replacement. RS-422 and RS-423 remain in the revised forms of RS-422-A and RS-423-A. RS-232-C also outlasted RS-449 and, in January 1987, the EIA issued RS-232-D, a revision for RS-232-C.

EIA RS-530 governs the mechanical and electrical characteristics of the interface between Data Terminal Equipment (DTE) and Data Circuit Terminating Equipment (DCE). The standard defines DTE as the hardware on the business machine side of the interface (teleprinters, display terminals, front-end processors, central processing units, etc.), and DCE as the modem, signal converter, or other device between the DTE and the communications line.

This report compares EIA RS-530 with RS-232-D and RS-449. It also discusses the mechanical and electrical characteristics and looks at the general classification of interchange circuits and outlines interchange circuit details.

Copies of EIA RS-530, 422-A, and 423-A can be obtained from the Electronic Industries Association, 2001 I Street, NW, Washington, DC 20006.

Analysis

EIA RS-530 operates in conjunction with either of two standards specifying electrical characteristics: RS-422-A, for balanced circuits; and RS-423-A, for unbalanced circuits. When each interface circuit has its own ground lead, the circuit is balanced. When an interface uses a common or shared grounding technique, it is unbalanced.

RS-530 is used for data communications systems with the following characteristics:

- DTE serializes data bits, and the DCE puts no restrictions on the DTE's bit sequence arrangements.
- Communication is binary, serial, synchronous, or asynchronous, and control information is exchanged on separate circuits.
- Equipment on one side of the DTE/DCE interface connects directly to equipment on the other side without additional technical considerations.
- Communication is in half- and/or full-duplex modes in point-to-point or multipoint configurations over two- or four-wire facilities with data rates ranging from 20K bps to a nominal upper limit of 2M bps. Point-to-point arrangements may operate on either switched or dedicated facilities. Dedicated lines connect multipoint arrangements.

Applications in which cable termination, signal wave shaping, interconnection cable distance, and the interface's mechanical configurations must be tailored to meet specific user needs are not precluded, but are generally not within the standard's scope. The EIA RS-530 connector, also used for EIA RS-232-D, uses electrical characteristics that, if improperly connected to some silicon devices designed to

Table 1. Interconnecting EIA RS-530 with EIA RS-449

EIA-530			EIA-RS-449		
Circuit, Name, and Mnemonic		**Contact**	**Contact**	**Circuit, Name, and Mnemonic**	
Shield	—	1	1	—	Shield
Transmitted Data	BA (A) BA (B)	2 14	4 22	SD (A) SD (B)	Send Data
Received Data	BB (A) BB (B)	3 16	6 24	RD (A) RD (B)	Receive Data
Request to Send	CA (A) CA (B)	4 19	7 25	RS (A) RS (B)	Request to Send
Clear to Send	CB (A) CB (B)	5 13	9 27	CS (A) CS (B)	Clear to Send
DCE Ready	CC (A) CC (B)	6 22	11 29	DM (A) DM (B)	Data Mode
DTE Ready	CD (A) CD (B)	20 23	12 30	TR (A) TR (B)	Terminal Ready
Signal Ground	AB	7	19	SG	Signal Ground
Received Line Signal Detector	CF (A) CF (B)	8 10	13 31	RR (A) RR (B)	Receiver Ready
Transmit Signal Element Timing (DCE Source)	DB (A) DB (B)	15 12	5 23	ST (A) ST (B)	Send Timing
Receiver Signal Element Timing (DCE Source)	DD (A) DD (B)	17 9	8 26	RT (A) RT (B)	Receive Timing
Local Loopback	LL	18	10	LL	Local Loopback
Remote Loopback	RL	21	14	RL	Remote Loopback
Transmit Signal Element Timing (DTE Source)	DA (A) DA (B)	24 11	17 35	TT (A) TT (B)	Terminal Timing
Test Mode	TM	25	18	TM	Test Mode

meet the RS-422-A and RS-423-A electrical characteristics specified in this recommendation, could damage those devices.

An RS-530/RS-232-D Comparison

These standards include a specification of the D-shaped 25-pin interface connector, which RS-232-C had only referenced in an appendix and never included as part of the standard. Both standards support testing of both local and remote DCEs through the Local Loopback, Remote Loopback, and Test Mode circuits. Circuit names for the first 8 pins in both standards are the same, but differ on pins 9, 10, and 11, which are not used in RS-232-D.

EIA RS-530 achieves higher data rates than RS-232-D (greater than 20K bps) by specifying the use of balanced signals, while sacrificing some secondary signals and the Ring Indicator. The Ring Indicator's elimination indicates that EIA RS-530 is not for use in dial-up applications.

An EIA RS-530/RS-449 Comparison

The RS-530 standard will one day replace RS-449 but, while both standards are in use, RS-530 can be interconnected with devices using RS-449 through a connecting cable or device. Table 1 lists the Circuit Name and Mnemonic, and connector contact pin for each interface.

Mechanical Characteristics

The point of demarcation between the DTE and the DCE is at connector plugs on the DCE or at an interface point no further than 10 feet (three meters) from the DCE. A 25-position connector is specified for all interchange circuits. In all cases, the DTE provides the cable (up to 200 feet), which has male (pin) contacts and a female shell (plug connector); the DCE has a female connector. The connectors are equipped with a block that permits latching and unlatching without a tool. The latching block also permits the use of screws to fasten the connectors together. The mechanical configuration for connections of the interface cable at points other than the demarcation point is not specified.

When additional functions are offered in a separate unit that is inserted between the DTE and DCE, the female connector is associated with the DTE interface, while the male connector is a DCE interface.

Functional Description of Interchange Circuits

Interchange circuits fall into four general classifications: ground (or common return), data circuits, control circuits, and timing circuits. Table 2 outlines a list of EIA RS-530 interchange circuits showing mnemonic name, circuit

Table 2. EIA RS-530 Interchange Circuits

Circuit Mnemonic	Circuit Name	Circuit Detection	Circuit Type
AB	Signal Ground	—	—
BA	Transmitted Data	To DCE	Data
BB	Received Data	From DCE	Data
DA	Transmit Signal Element Timing (DTE Source)	To DCE	Timing
DB	Transmit Signal Element Timing (DCE Source)	From DCE	Timing
DD	Receiver Signal Element Timing (DCE Source)	From DCE	Timing
CA	Request to Send	To DCE	Control
CB	Clear to Send	From DCE	Control
CF	Received Line Signal Detector	From DCE	Control
CC	DCE Ready	From DCE	Control
CD	DTE Ready	To DCE	Control
LL	Local Loopback	To DCE	Control
RL	Remote Loopback	To DCE	Control
TM	Test Mode	From DCE	Control

identification, circuit direction, and circuit type. Table 3 compares the connector pin assignments and the functional interchange circuits along with an equivalency table showing the nearest equivalent EIA RS-232-D and CCITT V.24 functions in relation to each EIA RS-530 function. A functional description of each of the EIA RS-530 interchange circuits follows.

Ground or Common Return Circuits

Circuit AB (Signal Ground) connects the DTE circuit ground (circuit common) to the DCE circuit ground (circuit common) to provide a conductive route between the DTE and DCE signal commons.

Data Circuits

Circuit BA (Transmitted Data) transfers the data signals originated by the DTE to the DCE. The DTE holds Circuit BA in the binary ONE (marking) condition unless an ON condition is present on all of the following circuits: CA (Request to Send), CB (Clear to Send), CC (DCE Ready), and CD (DTE Ready). The DCE disregards any signal appearing on Circuit BA when an OFF condition exists on one or more of these circuits. While an ON condition is maintained on each of the circuits, the DCE sends all data signals transmitted across the interface on Circuit BA to the communications channel. The term "data signals" includes the binary ONE (marking) condition, reversals, and other sequences, such as SYN coded characters that maintain timing synchronization.

Circuit BB (Received Data) transfers DCE-generated data signals to the DTE in response to line signals from a remote station. Circuit BB is held in the binary ONE (marking) condition while Circuit CF (Receive Line Signal Detector) is in the OFF condition. On half-duplex channels, Circuit BB is held in the marking condition when Circuit CA is ON and for a brief interval when Circuit CA makes the transition from ON to OFF. This allows for the completion of the transmission and for the decay of channel reflections.

Timing Circuits

Circuit DA (Transmit Signal Element Timing—DTE Source) provides the DCE with transmit signal element timing data. The ON to OFF transition nominally indicates the center of each signal element on Circuit BA. When Circuit DA is implemented in the DTE, the DTE provides timing data on it whenever the DTE is in a POWER ON condition. The DTE can withhold timing data on this circuit for short periods as long as Circuit CA is in the OFF condition.

Circuit DB (Transmit Signal Element Timing—DCE Source) provides the DTE with transmit element timing data. The DTE provides a data signal on Circuit BA in which the transitions between signal elements occur at the time of the transitions from OFF to ON condition of the signal on Circuit DB. The DCE provides timing data on Circuit DB whenever the DCE is in a POWER ON condition. The DCE can withhold timing data on this circuit if Circuit CC is in the OFF condition.

Circuit DD (Receiver Signal Element Timing—DCE Source) provides the DTE with receive signal element timing data. The DCE provides timing data on this circuit whenever the DCE is in a POWER ON condition. The DCE can withhold timing data on this circuit for short periods as long as Circuit CC is in the OFF condition.

Control Circuits

Circuit CA (Request to Send) controls the transmit function of the local DCE and, on half-duplex channels, the direction of data transmission. On one-way-only (duplex) channels, the ON condition holds the DCE in the transmit mode; the OFF condition suppresses transmission. On a half-duplex channel, the ON condition holds the DCE in the transmit mode and suppresses the receive mode. The OFF condition holds the DCE in the receive mode. A transition from OFF to ON instructs the DCE to enter the transmit mode. The DCE responds by taking any necessary action and indicating completion of such action by turning ON Circuit CB (Clear to Send), thereby permitting the DTE to transfer data across Circuit BA. A transition from ON to OFF instructs the DCE to complete transmission of all data previously transferred across the interface on Circuit BA (Transmitted Data) and then to assume a nontransmit, or receive mode, as appropriate. The DCE responds to this instruction by turning OFF Circuit CB.

When Circuit CA is turned OFF, it is not turned ON again until Circuit CB has been turned OFF by the DCE. An ON condition is required on Circuit CA, as well as on Circuits CB and CC, whenever data is transferred across the interface on Circuit BA by the DTE. Circuit CA may be turned ON at any time when Circuit CB is OFF, regardless of the status of any other interface circuit.

Table 3. RS-530 and Nearest Equivalent RS-232-C and CCITT V.24

EIA RS-530 Circuit	EIA RS-530 Description	25 Pin	CCITT V.24 Circuit	EIA RS-232-D Circuit	EIA RS-232-D Description
—	Shield	1	—	—	Shield
BA	Transmitted Data	2	103	BA	Transmitted Data
BB	Received Data	3	104	BB	Received Data
CA	Request to Send	4	105	CA	Request to Send
CB	Clear to Send	5	106	CB	Clear to Send
CC	DCE Ready	6	107	CC	DCE Ready
AB	Signal Ground	7	102	AB	Signal Ground
CF	Received Line Signal Detector	8	109	CF	Received Line Signal Detector
DD	Receiver Signal Element timing (DCE)	9	—	—	Reserved for Testing
CF	Received Line Signal Detector	10	—	—	Reserved for Testing
DA	Transmit Signal Element Timing (DTE)	11	—	—	Unassigned
DB	Transmit Signal Element Timing (DCE)	12	122/112	SCF/CI	Secondary Received Line Signal Detector/Data Signal Rate Selector (DCE)
CB	Clear to Send	13	121	SCB	Secondary Clear to Send
BA	Transmitted Data	14	118	SBA	Secondary Transmitted Data
DB	Transmitter Signal Element Timing (DCE)	15	114	DB	Transmitter Signal Element Timing (DCE)
BB	Received Data	16	119	SBB	Secondary Received Data
DD	Receiver Signal Element Timing (DCE)	17	115	DD	Receiver Signal Element Timing (DCE)
LL	Local Loopback	—	—	—	—

Circuit CB (Clear to Send) indicates that the DCE has been conditioned to transmit data over the communications channel. The ON condition, together with the ON on Circuit CA (Request to Send) and Circuit CC (DCE Ready), indicates to the DTE that signals on Circuit BA (Transmitted Data) will be transmitted to the communication channel. The OFF condition indicates that the DTE should not transfer data across the interface on Circuit BA, since this data will not be transmitted to the line. The ON condition of Circuit CB is a response to the occurrence of concurrent ON conditions on Circuits CC and CA, delayed as appropriate by the DCE, to allow the establishment of a data communications channel to a remote DTE.

Circuit CF (Received Line Signal Detector) indicates whether the receiver in the DCE is ready to receive data signals from the communication channel, but does not indicate the relative quality of the data signals received. An equalizer's condition in a DCE does not affect Circuit CF. The ON condition indicates that the DCE is receiving a signal that meets its criteria, which the DCE manufacturer establishes. The OFF condition indicates that no signal is being received. Circuit CF's OFF condition causes Circuit BB (Received Data) to be clamped to the binary ONE (marking) condition.

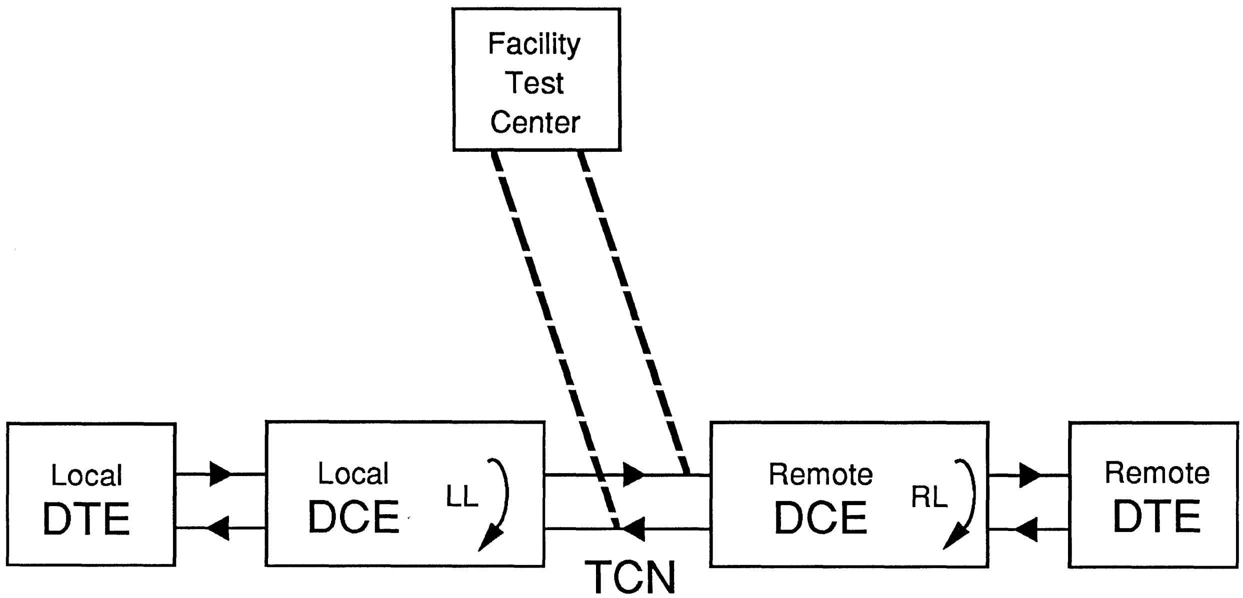
On half-duplex channels, Circuit CF is held in the OFF condition whenever Circuit CA (Request to Send) is in the ON condition and for a brief interval of time following Circuit CA's transition from ON to OFF.

Circuit CC (DCE Ready) indicates the status of the local DCE; the ON condition does not indicate that a communication channel has been established to a remote data station nor does it indicate the status of any remote station equipment. The OFF condition indicates that the DTE should ignore signals appearing on all other interchange circuits with the exception of Circuit TM (Test Mode). Circuit CC remains in the OFF condition for DCE tests not completed through the DTE/DCE interface. The circuit responds normally (i.e., not clamped OFF) for DCE tests conducted through the DTE/DCE interface.

Circuit CD (DTE Ready) controls DCE switching to and from the communications channel. The ON condition prepares the DCE for connection to a communications channel and maintains the connection. The OFF condition removes the DCE from the communication channel following the completion of any "in process" transmission.

Circuit LL (Local Loopback) controls the local loopback test condition in the local DCE. (See Figure 1 for details.) The ON condition instructs the DCE to transfer its output to its receive signal converter to check local operation. After establishing the LL test condition, the local DTE turns ON Circuit TM. Once TM is ON, the DTE may operate in a duplex mode, using all the circuits in the interface. OFF

Figure 1.
Loopback Tests



Local loopback and remote loopback tests as seen from the local DTE.

causes the DCE to release the LL test condition. The LL test does not disable Circuit IC.

Circuit RL (Remote Loopback) controls the remote loopback test function (see Figure 1). This circuit's ON condition causes the local DCE to initiate the RL test on the remote DCE. After turning RL ON and detecting an ON condition on the TM (Test Mode) circuit, the local DTE can operate in a duplex mode using local and remote DCE circuitry. An OFF condition releases the RL condition. While a unit is in RL test condition, communications is out-of-service to the remote DTE. When RL is activated, the DCE presents an OFF condition on Circuit DM and an ON condition on Circuit TM to the DTE. The local DCE presents an ON condition on Circuit TM and allows Circuit DM to respond normally.

Circuit TM (Test Mode) indicates that local DCE is in test condition. ON indicates a test condition, and OFF indicates normal operation. When testing (either LL or RL) is conducted through the local DTE/DCE interface, Circuit CC responds normally; when testing is not conducted through this interface, Circuit CC is held in an OFF condition.

Electrical Characteristics

RS-422-A (balanced operation) and RS-423-A (unbalanced operation) specify the individual interchange circuits' electrical characteristics. EIA RS-530, like RS-449, specifies the mechanical configuration of the connector and the pin assignments and functions of the entire interface, including the timing and interrelationships of the various circuits.

For the purpose of assigning electrical characteristics to the interchange circuits (defined functionally earlier in this report), EIA RS-530 has defined two separate categories of circuits. *Category I Circuits* are as follows:

- Circuit BA (Transmitted Data)
- Circuit BB (Received Data)
- Circuit DA (Transmit Signal Element Timing, DTE Source)
- Circuit DB (Transmit Signal Element Timing, DCE Source)
- Circuit DD (Receiver Signal Element Timing, DCE Source)
- Circuit CA (Request to Send)
- Circuit CB (Clear to Send)
- Circuit CF (Received Line Signal Detector)
- Circuit CC (DCE Ready)
- Circuit CD (DTE Ready)

The individual Category I circuits use the balanced electrical characteristics of EIA-422-A. Each circuit has two leads through the interface connector; each interchange circuit contains a pair of wires interconnecting a balanced generator and a differential receiver.

Category II Circuits are as follows:

- Circuit LL (Local Loopback)
- Circuit RL (Remote Loopback)
- Circuit TM (Test Mode)

Category II Circuits use the unbalanced electrical characteristics of EIA-423-A. Each circuit contains one wire interconnecting an unbalanced generator and a differential receiver. The EIA-423-A generators use wave shaping that allows operation over an interface cable length of up to 200 feet (60 meters). The common return for Category II interchange circuits is Circuit AB (Signal Ground).

Certain control interchange circuits require that an ON or OFF voltage be applied to them at all times for proper operation. If the circuit is not associated with an operation

Table 4. Connector Contact Assignments

Contact Number	Circuit	Interchange Points	Circuit Category	Direction to DCE	Direction from DCE
1	Shield	—			
2	BA	A-A1	I	X	
3	BB	A-A1	I		X
4	CA	A-A1	I	X	
5	CB	A-A1	I		X
6	CC	A-A1	I		X
7	AB	C-C1	—		X
8	CF	A-A1	I		X
9	DD	B-B1	I		X
10	CF	B-B1	I		X
11	DA	B-B1	I	X	
12	DB	B-B1	I		X
13	CB	B-B1	I		X
14	BA	B-B1	I	X	
15	DB	A-A1	I		X
16	BB	B-B1	I		X
17	DD	A-A1	I		X
18	LL	A-A1	II	X	
19	CA	B-B1	I	X	
20	CD	A-A1	I	X	
21	RL	A-A1	II	X	
22	CC	B-B1	I		X
23	CD	B-B1	I	X	
24	DA	A-A1	I	X	
25	TM	A-A1	II		X

Note:
Interchange Points A-A1, B-B1 for each Category I circuit should be assigned twisted pairs in interconnecting cables to minimize cross-talk.

generator, a dummy generator must be provided. The circuits involved are:

DTE Control Interchange Circuits	DCE Control Interchange Circuits
CA (Request to Send)	CB (Clear to Send)
LL (Local Loopback)	CF (Received Line Signal Detector)
RL (Remote Loopback)	TM (Test Mode)
CD (DTE Ready)	CC (DCE Ready)

A dummy generator must meet the appropriate open-circuit, test termination, and short-circuit generator requirements of EIA-422-A or EIA-423-A. It is implemented using a 2-watt, 47-ohm resistor connected to a DC source of between 4 and 6 volts. A single dummy generator can signal over more than one interchange circuit. Therefore, only two dummy generators are required for both ON and OFF (positive and negative) circuit conditions. The DTE's interface cable must provide separate conductors for each circuit requiring a dummy generator. Two conductors may be used, however, one for the positive dummy generator and the other for the negative dummy generator. An RS-422-A or RS-423-A POWER OFF requirement is required when any of the following circuits uses a dummy generator:

- Circuit CC (DCE Ready),
- Circuit DC (DTE Ready), and
- Circuit CA (Request to Send)

The RS-422-A standard describes the relationship between signaling rate and interface cable distance for balanced interchange circuits. The guidelines specify that operation over 200 feet of cable limits the maximum signaling rate of balanced interchange circuits to 2 million bps. Operation over cable distances greater than 200 feet is possible, but viewed as a tailored application.

In DTEs and DCEs, protective ground is a point that is electrically bonded to the equipment frame. It can also be connected to external grounds through the third wire of the power cord. It should be noted that protective ground (frame ground) is not an interchange circuit in EIA RS-530. If the DCE and DTE equipment frames must be bonded, a separate conductor that conforms to the appropriate national or local electrical codes should be used.

Interface connector pin number 1 facilitates the use of shield interconnecting cable, permitting the DTE cable to carry tandem connectorized sections with shield continuity. The DCE does not connect to pin 1, except in some applications requiring electromagnetic interference (EMI) suppression. While additional provisions may be necessary, they are beyond the scope of this standard.

Proper operation of the interchange circuits requires a path between the DTE circuit ground (circuit common) and the DCE circuit ground, which is provided by Circuit AB (Signal Ground). Normally, both the DTE and DCE should have their circuit grounds connected to protective grounds (frame grounds), which, in turn, may be connected to an external ground, usually associated with the power line plug.

For fail-safe operation, the receivers can detect a POWER OFF condition in the equipment across the interface or a disconnected cable. Detection of either of these conditions is interpreted as an OFF on any of the following interchange circuits:

- Circuit CC (DCE Ready)
- Circuit CA (Request to Send)
- Circuit CD (DTE Ready)

The receiver for each control circuit, except those control circuits specified above, interprets the situation in which the conductor is not implemented in the interconnecting cable as an OFF condition.

General Signal Characteristics

Interchange circuits transferring data signals across the interface point hold the mark (binary ONE) and space (binary ZERO) conditions for the total nominal duration of each signal element. EIA-334-A, "Signal Quality at Interface Between Data Processing Terminal Equipment and Synchronous Data Communication Equipment for Serial Data Transmission" defines distortion tolerances for synchronous systems. EIA-363, "Standard for Specifying Signal Quality for Transmitting and Receiving Data Processing Terminal Equipment Using Serial Data Transmission at the Interface with Non-Synchronous Communication Equipment," states standard naming procedures for specifying signal quality for nonsynchronous systems. Distortion tolerances for nonsynchronous systems are stated in EIA-404-A, "Standard for Start-Stop Signal Quality Between Data Terminal Equipment and Non-Synchronous Data Communication Equipment." Interchange circuits sending timing signals across the interface point keep ON and OFF conditions for nominally equal amounts of time, in keeping with the acceptable tolerances specified in EIA-334-A.

The accuracy and stability of the timing data on Circuit DD (Receiver Signal Element Timing) are needed only when Circuit CF (Received Line Signal Detector) is ON. During the OFF condition of Circuit CF, drift is acceptable; however, once the OFF to ON transition of Circuit CF occurs, resynchronization of the timing data on Circuit DD must occur as quickly as possible.

Transfer of timing information across the interface is necessary whenever the timing source is capable of generating data, and it should not be restricted only to periods of actual data transmission. When timing data is not provided on a timing interchange circuit, the interchange circuit is clamped in the OFF condition. Tolerances on the relationship between data and associated timing signals follow the EIA-334-A recommendation.

EIA RS-530 Interchange Circuit Details

Listed below are details of RS-530's additional functions.

Use of Circuits for Testing

Three interchange circuits permit fault isolation testing done under DTE control: Circuit LL (Local Loopback), Circuit RL (Remote Loopback), and Circuit TM (Test Mode) (see Figure 1).

The EIA considers the (Circuit TM) and test control (Circuit LL and Circuit RL) status circuits a desirable step toward uniform methods of fault isolation. These circuits assist DTE and DCE users in tracking down a defective unit.

Local Loopback (LL Test): This test condition is equivalent to CCITT test loop #3. It provides a way in which a DTE can check the functioning of a DTE-to-DCE interface and the transmit and receive sections of the local DCE. One may also test the local DCE with a test set instead of through the DTE. The output of the transmitting portion of the DCE is returned to the receiving station in the LL test through circuitry that is required for proper operation. In many DCEs, the signal transmitted is unsuitable for direct connection to the receiver. In such cases, an appropriate signal shaping or conversion in the loop-around circuitry may be included so that any element used in normal operations is checked in the test condition.

Remote Loopback (RL Test): This test, equivalent to CCITT test loop #2, allows a DTE or a facility test center to check the transmission path through the remote DCE to the DTE interface and the corresponding return path. In this test, Circuit SD and Circuit RD are either isolated or disconnected from the remote DTE at the interface and then connected to each other at the remote DCE. In synchronous DCEs, a suitable transmit clock may be necessary when the RL test condition is initiated. In some instances, buffer storage may be required between Circuit RD and Circuit SD.

Remote control of the RL test permits the automation of end-to-end testing of any circuit from a central location. Primarily, test control is suitable in point-to-point applications, but may also be used in multipoint arrangements with the addition of an address detection feature in the DCE. Test RL enables circuit verification without the aid of a distant DCE, supported by an inherent remote loopback ability in many modern DCEs.

The ON states of Circuit RL and Circuit LL are mutually exclusive, because the two test conditions may not function simultaneously.

Equalizers

Equalization is a process whereby a circuit's frequency and phase distortions are reduced to compensate for differences in time delay and attenuation of the varying frequencies in the transmission band. An equalizer associated with the DCE may require training, a process that produces a fixed number of equally spaced reference signals.

RS-449 outlines the procedures for equalizer training. The following example outlines a typical training sequence. DCE "E" (East) has an equalizer that requires training. DCE "W" (West) is transmitting toward DCE "E". Initial training of DCE "Es" equalizer occurs during the interval between the ON condition of Circuit RS and

Table 5. Standard Interfaces for Selected Communication System Configuration

Interchange Circuit	Configuration Type SR	Configuration Type SO	Configuration Type RO	Configuration Type DT
AB Signal Ground	M	M	M	M
BA Transmitted Data	M	M	M	M
BB Received Data	M		M	M
DA Transmit Signal Element Timing (DTE Source)	O	O		O
DB Transmit Signal Element Timing (DCE Source)	T	T		T
DD Receiver Signal Element Timing (DCE Source)	T		T	T
CA Request to Send	M	M		
CB Clear to Send	M	M		
CF Received Line Signal Detector	M		M	
CC DCE Ready	M	M	M	
CD DTE Ready	S	S	S	
LL Local Loopback	O			
RL Remote Loopback	O			
TM Test Mode	M	M	M	

M—Mandatory interchange circuits for a given configuration.
T—Additional interchange circuits required for synchronous operation.
S—Additional interchange circuit required for switched service.
O—Optional interchange circuits.

the ON condition of Circuit CS of DCE "W". Initial training in the DCE "Es" receiver occurs prior to the ON condition of Circuit RR of DCE "E". Circuit SQ is placed in the ON condition no later than the OFF-to-ON transition of Circuit RR if the initial training is successful. Circuit SQ's state is undefined when Circuit RR is OFF.

If the equalizer requires a unique training signal from DCE "W" to achieve equalization, the states of specific interchange circuits are controlled during this process. When the normal flow of data toward DCE "W" is interrupted in order to cause DCE "W" to transmit this unique sequence, Circuit CS of DCE "E" is held in the OFF condition while the command signal is being sent. In this situation, Circuit SQ of DCE "W" should be placed in the OFF condition while receiving the command signal. Circuit RD of DCE "W" may be clamped to the marking condition while the command signal is received. In the reverse direction, Circuit CS of DCS "W" is in the OFF condition while the unique training signal is sent. Circuit RD of DCE "E" may be clamped to the marking condition when the unique training signal is received. When the equalizer attains proper adjustment, DCE "E" places Circuit SQ in the ON condition.

Standard Interfaces for Selected Configurations

Standard sets of interchange circuits for data transmission configurations are defined as follows: Type SR (Send-Receive), Type SO (Send-Only), Type RO (Receive-Only), and Type DT (Data and Timing only). Table 5 lists the interchange circuits that must be provided for each data transmission configuration. For a given type of interface, generators and receivers must be provided for every interchange circuit designated M (Mandatory) in Table 5. In addition, generators and receivers are necessary for all interchange circuits designated S and T, where the service is switched and synchronous, respectively. ■

EIA RS-530

In this report:

Synopsis

Editor's Note
EIA RS-530, approved in March 1987, defines the mechanical interface characteristics between Data Termination Equipment (DTE) and Data Circuit-Terminating Equipment (DCE). It operates in conjunction with RS-422-A and RS-423-A, which define the electrical operation of the individual interchange circuits for balanced and unbalanced operation, respectively. EIA RS-530 complements EIA RS-232-D for data rates above 20K bps and will gradually replace RS-449 for data rates above 20K bps.

Report Highlights
In 1977, the Electronic Industries Association (EIA) developed the RS-449, RS-422, and RS-423 standards to eventually replace RS-232-C. RS-449, however, never really caught on and, in March 1987, EIA RS-530 was introduced as its intended replacement. RS-422 and RS-423 remain in the revised forms of RS-422-A and RS-423-A. RS-232-C also outlasted RS-449 and, in January 1987, the EIA issued RS-232-D, a revision for RS-232-C.

EIA RS-530 governs the mechanical and electrical characteristics of the interface between Data Terminal Equipment (DTE) and Data Circuit Terminating Equipment (DCE). The standard defines DTE as the hardware on the business machine side of the interface (teleprinters, display terminals, front-end processors, central processing units, etc.), and DCE as the modem, signal converter, or other device between the DTE and the communications line.

This report compares EIA RS-530 with RS-232-D and RS-449. It also discusses the mechanical and electrical characteristics and looks at the general classification of interchange circuits and outlines interchange circuit details.

Copies of EIA RS-530, 422-A, and 423-A can be obtained from the Electronic Industries Association, 2001 I Street, NW, Washington, DC 20006.

Analysis

EIA RS-530 operates in conjunction with either of two standards specifying electrical characteristics: RS-422-A, for balanced circuits; and RS-423-A, for unbalanced circuits. When each interface circuit has its own ground lead, the circuit is balanced. When an interface uses a common or shared grounding technique, it is unbalanced.

RS-530 is used for data communications systems with the following characteristics:

- DTE serializes data bits, and the DCE puts no restrictions on the DTE's bit sequence arrangements.
- Communication is binary, serial, synchronous, or asynchronous, and control information is exchanged on separate circuits.
- Equipment on one side of the DTE/DCE interface connects directly to equipment on the other side without additional technical considerations.
- Communication is in half- and/or full-duplex modes in point-to-point or multipoint configurations over two- or four-wire facilities with data rates ranging from 20K bps to a nominal upper limit of 2M bps. Point-to-point arrangements may operate on either switched or dedicated facilities. Dedicated lines connect multipoint arrangements.

Applications in which cable termination, signal wave shaping, interconnection cable distance, and the interface's mechanical configurations must be tailored to meet specific user needs are not precluded, but are generally not within the standard's scope. The EIA RS-530 connector, also used for EIA R-232-D, uses electrical characteristics that, if improperly connected to some silicon devices designed to meet the RS-422-A and RS-423-A electrical characteristics specified in this recommendation, could damage those devices.

An RS-530/RS-232-D Comparison

These new standards include a specification of the D-shaped 25-pin interface connector, which RS-232-C had only referenced in an appendix and never included as part of the standard. Both standards support testing of both local and remote DCEs through the Local Loopback, Remote Loopback, and Test Mode circuits. Circuit names for the first 8 pins in both standards are the same, but differ on pins 9, 10, and 11, which are not used in RS-232-D.

EIA RS-530 achieves higher data rates than RS-232-D (greater than 20K bps) by specifying the use of balanced signals, while sacrificing some secondary signals and the Ring Indicator. The Ring Indicator's elimination indicates that EIA RS-530 is not for use in dial-up applications.

An EIA RS-530/RS-449 Comparison

The RS-530 standard will one day replace RS-449 but, while both standards are in use, RS-530 can be interconnected with devices using RS-449 through a connecting cable or device. Table 1 lists the Circuit Name and Mnemonic, and connector contact pin for each interface.

Mechanical Characteristics

The point of demarcation between the DTE and the DCE is at connector plugs on the DCE or at an interface point no further than 10 feet (three meters) from the DCE. A 25-position connector is specified for all interchange circuits. In all cases, the DTE provides the cable (up to 200 feet), which has male (pin) contacts and a female shell (plug connector); the DCE has a female connector. The connectors are equipped with a block that permits latching and unlatching without a tool. The latching block also permits the use of screws to fasten the connectors together. The mechanical configuration for connections of the interface cable at points other than the demarcation point is not specified.

When additional functions are offered in a separate unit that is inserted between the DTE and DCE, the female connector is associated with the DTE interface, while the male connector is a DCE interface.

Table 1. Interconnecting EIA RS-530 with EIA RS-449

EIA-530			EIA-RS-449		
Circuit, Name, and Mnemonic		Contact	Contact	Circuit, Name, and Mnemonic	
Shield	—	1	1	—	Shield
Transmitted Data	BA (A) BA (B)	2 14	4 22	SD (A) SD (B)	Send Data
Received Data	BB (A) BB (B)	3 16	6 24	RD (A) RD (B)	Receive Data
Request to Send	CA (A) CA (B)	4 19	7 25	RS (A) RS (B)	Request to Send
Clear to Send	CB (A) CB (B)	5 13	9 27	CS (A) CS (B)	Clear to Send
DCE Ready	CC (A) CC (B)	6 22	11 29	DM (A) DM (B)	Data Mode
DTE Ready	CD (A) CD (B)	20 23	12 30	TR (A) TR (B)	Terminal Ready
Signal Ground	AB	7	19	SG	Signal Ground
Received Line Signal Detector	CF (A) CF (B)	8 10	13 31	RR (A) RR (B)	Receiver Ready
Transmit Signal Element Timing (DCE Source)	DB (A) DB (B)	15 12	5 23	ST (A) ST (B)	Send Timing
Receiver Signal Element Timing (DCE Source)	DD (A) DD (B)	17 9	8 26	RT (A) RT (B)	Receive Timing
Local Loopback	LL	18	10	LL	Local Loopback
Remote Loopback	RL	21	14	RL	Remote Loopback
Transmit Signal Element Timing (DTE Source)	DA (A) DA (B)	24 11	17 35	TT (A) TT (B)	Terminal Timing
Test Mode	TM	25	18	TM	Test Mode

Functional Description of Interchange Circuits

Interchange circuits fall into four general classifications: ground (or common return), data circuits, control circuits, and timing circuits. Table 2 outlines a list of EIA RS-530 interchange circuits showing mnemonic name, circuit identification, circuit direction, and circuit type. Table 3 compares the connector pin assignments and the functional interchange circuits along with an equivalency table showing the nearest equivalent EIA RS-232-D and CCITT V.24 functions in relation to each EIA RS-530 function. A functional description of each of the EIA RS-530 interchange circuits follows.

Ground or Common Return Circuits

Circuit AB (Signal Ground) connects the DTE circuit ground (circuit common) to the DCE circuit ground (circuit common) to provide a conductive route between the DTE and DCE signal commons. See Figure 3 for grounding arrangements.

Data Circuits

Circuit BA (Transmitted Data) transfers the data signals originated by the DTE to the DCE. The DTE holds Circuit BA in the binary ONE (marking) condition unless an ON condition is present on all of the following circuits: CA (Request to Send), CB (Clear to Send), CC (DCE Ready), and CD (DTE Ready). The DCE disregards any signal appearing on Circuit BA when an OFF condition exists on one or more of these circuits. While an

Table 2. EIA RS-530 Interchange Circuits

Circuit Mnemonic	Circuit Name	Circuit Detection	Circuit Type
AB	Signal Ground	—	—
BA	Transmitted Data	To DCE	Data
BB	Received Data	From DCE	Data
DA	Transmit Signal Element Timing (DTE Source)	To DCE	Timing
DB	Transmit Signal Element Timing (DCE Source)	From DCE	Timing
DD	Receiver Signal Element Timing (DCE Source)	From DCE	Timing
CA	Request to Send	To DCE	Control
CB	Clear To Send	From DCE	Control
CF	Received Line Signal Detector	From DCE	Control
CC	DCE Ready	From DCE	Control
CD	DTE Ready	To DCE	Control
LL	Local Loopback	To DCE	Control
RL	Remote Loopback	To DCE	Control
TM	Test Mode	From DCE	Control

ON condition is maintained on each of the circuits, the DCE sends all data signals transmitted across the interface on Circuit BA to the communications channel. The term "data signals" includes the binary ONE (marking) condition, reversals, and other sequences, such as SYN coded characters that maintain timing synchronization.

Circuit BB (Received Data) transfers DCE-generated data signals to the DTE in response to line signals from a remote station. Circuit BB is held in the binary ONE (marking) condition while Circuit CF (Receive Line Signal Detector) is in the OFF condition. On half-duplex channels, Circuit BB is held in the marking condition when Circuit CA is ON and for a brief interval when Circuit CA makes the transition from ON to OFF. This allows for the completion of the transmission and for the decay of channel reflections.

Timing Circuits

Circuit DA (Transmit Signal Element Timing—DTE Source) provides the DCE with transmit signal element timing data. The ON to OFF transition nominally indicates the center of each signal element on Circuit BA. When Circuit DA is implemented in the DTE, the DTE provides timing data on it whenever the DTE is in a POWER ON condition. The DTE can withhold timing data on this circuit for short periods as long as Circuit CA is in the OFF condition.

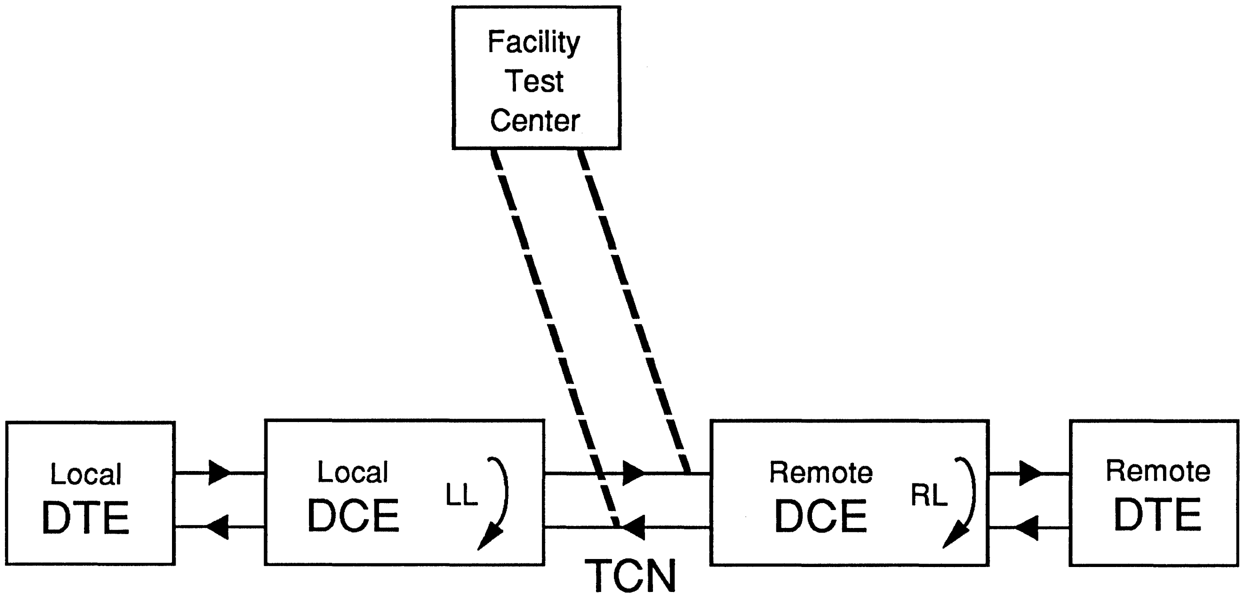
Circuit DB (Transmit Signal Element Timing—DCE Source) provides the DTE with transmit element timing data. The DTE provides a data signal on Circuit BA in which the transitions between signal elements occur at the time of the transitions from OFF to ON condition of the signal on Circuit DB. The DCE provides timing data on Circuit DB whenever the DCE is in a POWER ON condition. The DCE can withhold timing data on this circuit if Circuit CC is in the OFF condition.

Circuit DD (Receiver Signal Element Timing—DCE Source) provides the DTE with receive signal element timing data. The DCE provides timing data on this circuit whenever the DCE is in a POWER ON condition. The DCE can withhold timing data on this circuit for short periods as long as Circuit CC is in the OFF condition.

Control Circuits

Circuit CA (Request to Send) controls the transmit function of the local DCE and, on half-duplex channels, the direction of data transmission. On one-way-only (duplex) channels, the ON condition holds the DCE in the transmit mode; the OFF condition suppresses transmission. On a half-duplex channel, the ON condition holds the DCE in the transmit mode and suppresses the receive mode. The OFF condition holds the DCE in the receive mode. A transition from OFF to ON instructs the DCE to enter the transmit mode. The DCE responds by taking any necessary action and indicating completion of such action by turning ON Circuit CB (Clear to Send), thereby permitting the DTE to transfer data across Circuit BA. A transition from ON to OFF instructs the DCE to complete transmission of all data previously transferred across the interface on Circuit BA

Figure 1.
Loopback Tests



Local loopback and remote loopback tests as seen from the local DTE.

(Transmitted Data) and then to assume a nontransmit, or receive mode, as appropriate. The DCE responds to this instruction by turning OFF Circuit CB.

When Circuit CA is turned OFF, it is not turned ON again until Circuit CB has been turned OFF by the DCE. An ON condition is required on Circuit CA, as well as on Circuits CB and CC, whenever data is transferred across the interface on Circuit BA by the DTE. Circuit CA may be turned ON at any time when Circuit CB is OFF, regardless of the status of any other interface circuit.

Circuit CB (Clear to Send) indicates that the DCE has been conditioned to transmit data over the communications channel. The ON condition, together with the ON on Circuit CA (Request to Send) and Circuit CC (DCE Ready), indicates to the DTE that signals on Circuit BA (Transmitted Data) will be transmitted to the communication channel. The OFF condition indicates that the DTE should not transfer data across the interface on Circuit BA, since this data will not be transmitted to the line. The ON condition of Circuit CB is a response to the occurrence of concurrent ON conditions on Circuits CC and CA, delayed as appropriate by the DCE, to allow the establishment of a data communications channel to a remote DTE.

Circuit CF (Received Line Signal Detector) indicates whether the receiver in the DCE is ready to receive data signals from the communication channel, but does not indicate the relative quality of the data signals received. An equalizer's condition in a DCE does not affect Circuit CF. The ON condition indicates that the DCE is receiving a signal that meets its criteria, which the DCE manufacturer establishes. The OFF condition indicates that no signal is being received. Circuit CF's OFF condition causes Circuit BB (Received Data) to be clamped to the binary ONE (marking) condition.

On half-duplex channels, Circuit CF is held in the OFF condition whenever Circuit CA (Request to Send) is in the ON condition and for a brief interval of time following Circuit CA's transition from ON to OFF.

Circuit CC (DCE Ready) indicates the status of the local DCE; the ON condition does not indicate that a communication channel has been established to a remote data station nor does it indicate the status of any remote station equipment. The OFF condition indicates that the DTE should ignore signals appearing on all other interchange circuits with the exception of Circuit TM (Test Mode). Circuit CC remains in the OFF condition for DCE tests not completed through the DTE/DCE interface. The circuit responds normally (i.e.,

Table 3. RS-530 and Nearest Equivalent RS-232-C and CCITT V.24

EIA RS-530 Circuit	EIA RS-530 Description	25 Pin	CCITT V.24 Circuit	EIA RS-232-D Circuit	EIA RS-232-D Description
—	Shield	1	—	—	Shield
BA	Transmitted Data	2	103	BA	Transmitted Data
BB	Received Data	3	104	BB	Received Data
CA	Request to Send	4	105	CA	Request to Send
CB	Clear to Send	5	106	CB	Clear to Send
CC	DCE Ready	6	107	CC	DCE Ready
AB	Signal Ground	7	102	AB	Signal Ground
CF	Received Line Signal Detector	8	109	CF	Received Line Signal Detector
DD	Receiver Signal Element timing (DCE)	9	—	—	Reserved for Testing
CF	Resceived Line Signal Detector	10	—	—	Reserved for Testing
DA	Transmit Signal Element Timing (DTE)	11	—	—	Unassigned
DB	Transmit Signal Element Timing (DCE)	12	122/112	SCF/CI	Secondary Received Line Signal Detector/Data Signal Rate Selector (DCE)
CB	Clear to Send	13	121	SCB	Secondary Clear to Send
BA	Transmitted Data	14	118	SBA	Secondary Transmitted Data
DB	Transmitter Signal Element Timing (DCE)	15	114	DB	Transmitter Signal Element Timing (DCE)
BB	Received Data	16	119	SBB	Secondary Received Data
DD	Receiver Signal Element Timing (DCE)	17	115	DD	Receiver Signal Element Timing (DCE)
LL	Local Loopback	—	—	—	—

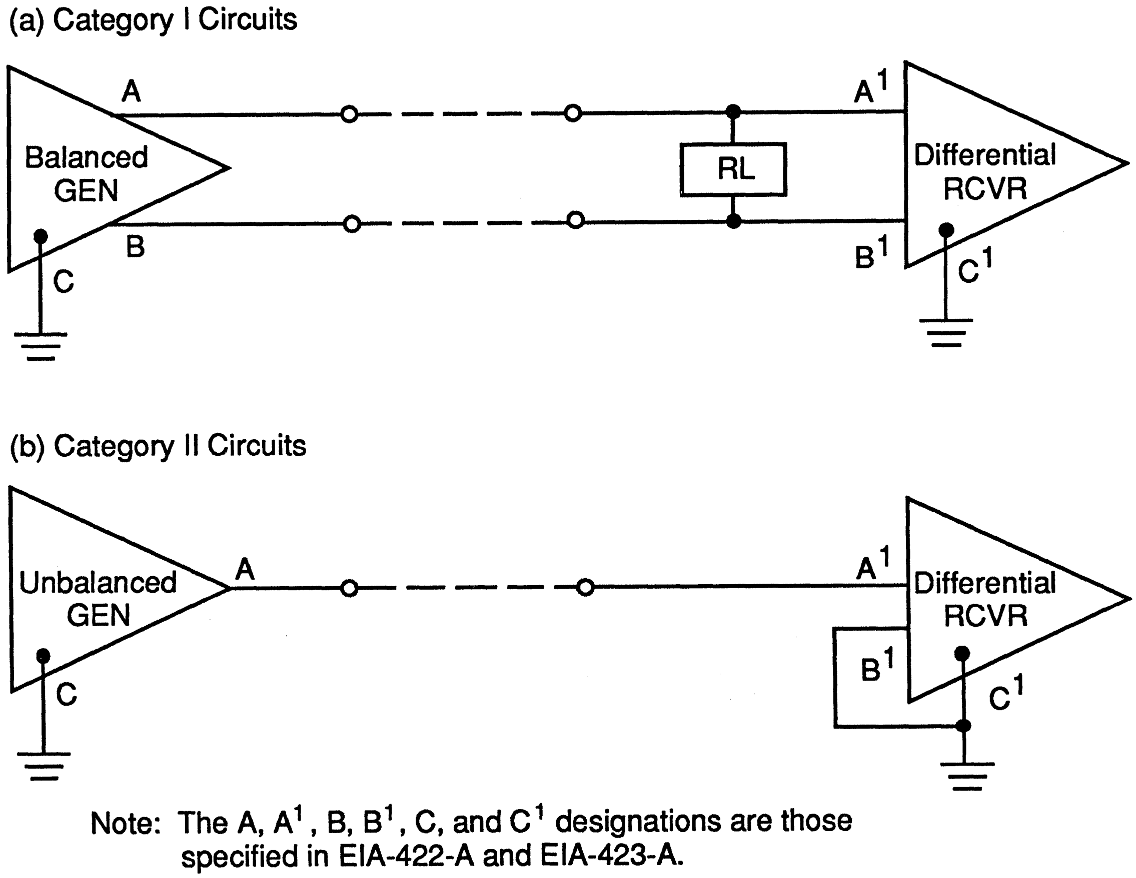
not clamped OFF) for DCE tests conducted through the DTE/DCE interface.

Circuit CD (DTE Ready) controls DCE switching to and from the communications channel. The ON condition prepares the DCE for connection to a communications channel and maintains the connection. The OFF condition removes the DCE from the communication channel following the completion of any "in process" transmission.

Circuit LL (Local Loopback) controls the local loopback test condition in the local DCE. (See Figure 1 for details.) The ON condition instructs the DCE to transfer its output to its receive signal converter to check local operation. After establishing the LL test condition, the local DTE turns ON Circuit TM. Once TM is ON, the DTE may operate in a duplex mode, using all the circuits in the interface. OFF causes the DCE to release the LL test condition. The LL test does not disable Circuit IC.

Circuit RL (Remote Loopback) controls the remote loopback test function (see Figure 1). This circuit's ON condition causes the local DCE to initiate the RL test on the remote DCE. After turning RL ON and detecting an ON condition on the TM (Test Mode) circuit, the local DTE can operate in a duplex mode using local and remote DCE circuitry. An OFF condition releases the RL condition. While a unit is in RL test condition, communications is out-of-service to the remote DTE. When RL is activated, the DCE presents an OFF condition on Circuit DM and an ON condition on Circuit TM to the DTE. The local DCE

Figure 2.
Generator and Receiver Connections at Interface



Category I circuits use the balanced electrical characteristics of EIA-422-A, while Category II circuits use the unbalanced electrical characteristics of EIA-422-A.

presents an ON condition on Circuit TM and allows Circuit DM to respond normally.

Circuit TM (Test Mode) indicates that local DCE is in test condition. ON indicates a test condition, and OFF indicates normal operation. When testing (either LL or RL) is conducted through the local DTE/DCE interface, Circuit CC responds normally; when testing is not conducted through this interface, Circuit CC is held in an OFF condition.

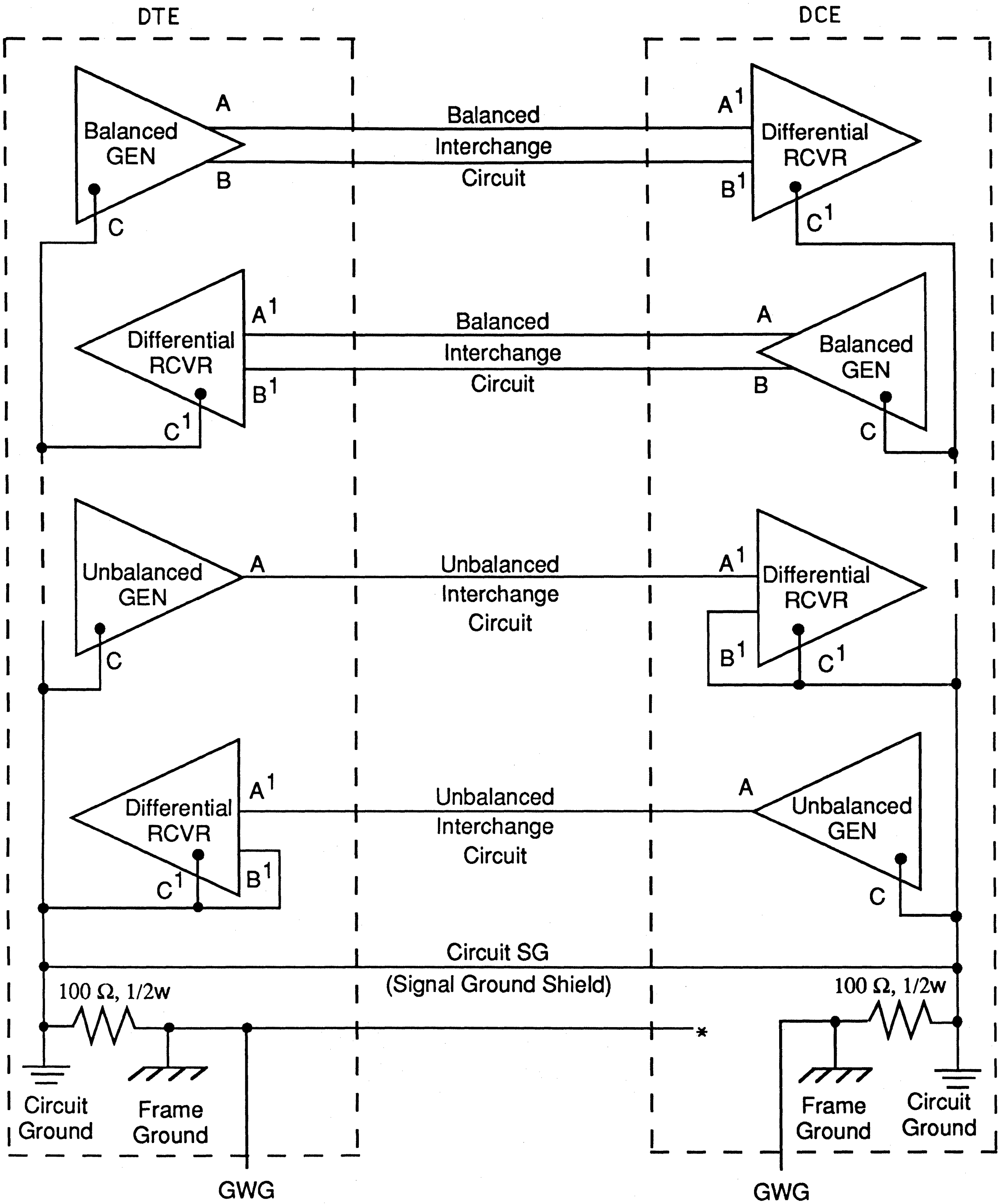
Electrical Characteristics

RS-422-A (balanced operation) and RS-423-A (unbalanced operation) specify the individual interchange circuits' electrical characteristics. EIA RS-530, like RS-449, specifies the mechanical configuration of the connector and the pin assignments and functions of the entire interface, including the timing and interrelationships of the various circuits.

For the purpose of assigning electrical characteristics to the interchange circuits (defined functionally earlier in this report), EIA RS-530 has defined two separate categories of circuits. *Category I Circuits* are as follows:

- Circuit BA (Transmitted Data)
- Circuit BB (Received Data)
- Circuit DA (Transmit Signal Element Timing, DTE Source)
- Circuit DB (Transmit Signal Element Timing, DCE Source)
- Circuit DD (Receiver Signal Element timing, DCE Source)

Figure 3.
Grounding Arrangements



**Normally no connection to shield in DCE.*

Notes: GWG is green wire ground of power system.

Grounding provides a conductive route between the DTE and DCE signal commons.

Table 4. Connector Contact Assignments

Contact Number	Circuit	Interchange Points	Circuit Category	Direction to DCE	Direction From DCE
1	Shield	—			
2	BA	A-A¹	I	X	
3	BB	A-A¹	I		X
4	CA	A-A¹	I	X	
5	CB	A-A¹	I		X
6	CC	A-A¹	I		X
7	AB	C-C¹	—		X
8	CF	A-A¹	I		X
9	DD	B-B¹	I		X
10	CF	B-B¹	I		X
11	DA	B-B¹	I	X	
12	DB	B-B¹	I		X
13	CB	B-B¹	I		X
14	BA	B-B¹	I	X	
15	DB	A-A¹	I		X
16	BB	B-B¹	I		X
17	DD	A-A¹	I		X
18	LL	A-A¹	II	X	
19	CA	B-B¹	I	X	
20	CD	A-A¹	I	X	
21	RL	A-A¹	II	X	
22	CC	B-B¹	I		X
23	CD	B-B¹	I	X	
24	DA	A-A¹	I	X	
25	TM	A-A¹	II		X

Note:
Interchange Points A-A¹, B-B¹ for each Category I circuit should be assigned twisted pairs in interconnecting cables to minimize cross-talk.

- Circuit CA (Request to Send)
- Circuit CB (Clear to Send)
- Circuit CF (Received Line Signal Detector)
- Circuit CC (DCE Ready)
- Circuit CD (DTE Ready)

The individual Category I circuits use the balanced electrical characteristics of EIA-422-A. Each circuit has two leads through the interface connector; each interchange circuit contains a pair of wires interconnecting a balanced generator and a differential receiver.

Category II Circuits are as follows:

- Circuit LL (Local Loopback)
- Circuit RL (Remote Loopback)
- Circuit TM (Test Mode)

Category II Circuits use the unbalanced electrical characteristics of EIA-423-A. Each circuit contains one wire interconnecting an unbalanced generator and a differential receiver. The EIA-423-A generators use wave shaping that allows operation over an interface cable length of up to 200 feet (60 meters). The common return for Category II interchange circuits is Circuit AB (Signal Ground).

Certain control interchange circuits require that an ON or OFF voltage be applied to them at all times for proper operation. If the circuit is not associated with an operation generator, a dummy generator must be provided. The circuits involved are:

Table 5. Standard Interfaces for Selected Communication System Configuration

Interchange Circuit	Configuration Type SR	Configuration Type SO	Configuration Type RO	Configuration Type DT
AB Signal Ground	M	M	M	M
BA Transmitted Data	M	M	M	M
BB Received Data	M		M	M
DA Transmit Signal Element Timing (DTE Source)	O	O		O
DB Transmit Signal Element Timing (DCE Source)	T	T		T
DD Receiver Signal Element Timing (DCE Source)	T		T	T
CA Request to Send	M	M		
CB Clear to Send	M	M		
CF Received Line Signal Detector	M		M	
CC DCE Ready	M	M	M	
CD DTE Ready	S	S	S	
LL Local Loopback	O			
RL Remote Loopback	O			
TM Test Mode	M	M	M	

M—Mandatory interchange circuits for a given configuration.
T—Additional interchange circuits required for synchronous operation.
S—Additional interchange circuit required for switched service.
O—Optional interchange circuits.

DTE Control Interchange Circuits	DCE Control Interchange Circuits
CA (Request to Send)	CB (Clear to Send)
LL (Local Loopback)	CF (Received Line Signal Detector)
RL (Remote Loopback)	TM (Test Mode)
CD (DTE Ready)	CC (DCE Ready)

A dummy generator must meet the appropriate open-circuit, test termination, and short-circuit generator requirements of EIA-422-A or EIA-423-A. It is implemented using a 2-watt, 47-ohm resistor connected to a DC source of between 4 and 6 volts. A single dummy generator can signal over more than one interchange circuit. Therefore, only two dummy generators are required for both ON and OFF (positive and negative) circuit conditions. The DTE's interface cable must provide separate conductors for each circuit requiring a dummy generator. Two conductors may be used, however, one for the positive dummy generator and the other for the negative dummy generator. An RS-422-A or RS-423-A POWER OFF requirement is required when any of the following circuits uses a dummy generator:

- Circuit CC (DCE Ready),
- Circuit DC (DTE Ready), and
- Circuit CA (Request to Send)

The RS-422-A standard describes the relationship between signaling rate and interface cable distance for balanced interchange circuits. The guidelines specify that operation over 200 feet of cable limits the maximum signaling rate of balanced interchange circuits to 2 million bps. Operation over cable distances greater than 200 feet is possible, but viewed as a tailored application.

In DTEs and DCEs, protective ground is a point that is electrically bonded to the equipment frame. It can also be connected to external grounds through the third wire of the power cord. It should be noted that protective ground (frame ground) is not an interchange circuit in EIA RS-530. If the DCE and DTE equipment frames must be bonded, a separate conductor that conforms to the appropriate national or local electrical codes should be used.

Interface connector pin number 1 facilitates the use of shield interconnecting cable, permitting the DTE cable to carry tandem connectorized sections with shield continuity. The DCE does not connect to pin 1, except in some applications requiring electromagnetic interference (EMI) suppression. While additional provisions may be necessary, they are beyond the scope of this standard.

Proper operation of the interchange circuits requires a path between the DTE circuit ground (circuit common) and the DCE circuit ground, which is provided by Circuit AB (Signal Ground). Normally, both the DTE and DCE should have their circuit grounds connected to protective grounds (frame grounds), which, in turn, may be connected to an external ground, usually associated with the power line plug. The grounding arrangement is shown in Figure 3.

For failsafe operation, the receivers can detect a POWER OFF condition in the equipment across the interface or a disconnected cable. Detection of either of these conditions is interpreted as an OFF on any of the following interchange circuits:

- Circuit CC (DCE Ready)
- Circuit CA (Request to Send)
- Circuit CD (DTE Ready)

The receiver for each control circuit, except those control circuits specified above, interprets the situation in which the conductor is not implemented in the interconnecting cable as an OFF condition.

General Signal Characteristics

Interchange circuits transferring data signals across the interface point hold the mark (binary ONE) and space (binary ZERO) conditions for the total nominal duration of each signal element. EIA-334-A, "Signal Quality at Interface Between Data Processing Terminal Equipment and Synchronous Data Communication Equipment for Serial Data Transmission" defines distortion tolerances for synchronous systems. EIA-363, "Standard for Specifying Signal Quality for Transmitting and Receiving Data Processing Terminal Equipment Using Serial Data Transmission at the Interface with Non-Synchronous Communication Equipment," states standard naming procedures for specifying signal quality for nonsynchronous systems. Distortion tolerances for nonsynchronous systems are stated in EIA-404-A, "Standard for Start-Stop Signal Quality Between Data Terminal Equipment and Non-Synchronous Data Communication Equipment." Interchange circuits sending timing signals across the interface point keep ON and OFF conditions for nominally equal amounts of time, in keeping with the acceptable tolerances specified in EIA-334-A.

The accuracy and stability of the timing data on Circuit DD (Receiver Signal Element Timing) is needed only when Circuit CF (Received Line Signal Detector) is ON. During the OFF condition of Circuit CF, drift is acceptable; however, once the OFF to ON transition of Circuit CF occurs, resynchronization of the timing data on Circuit DD must occur as quickly as possible.

Transfer of timing information across the interface is necessary whenever the timing source is capable of generating data, and it should not be restricted only to periods of actual data transmission. When timing data is not provided on a timing interchange circuit, the interchange circuit is clamped in the OFF condition. Tolerances on the relationship between data and associated timing signals follow the EIA-334-A recommendation.

EIA RS-530 Interchange Circuit Details

Listed below are details of RS-530's additional functions.

Use of Circuits for Testing

Three interchange circuits permit fault isolation testing done under DTE control: Circuit LL (Local Loopback), Circuit RL (Remote Loopback), and Circuit TM (Test Mode) (see Figure 1).

The EIA considers the (Circuit TM) and test control (Circuit LL and Circuit RL) status circuits a desirable step toward uniform methods of fault isolation. These circuits assist DTE and DCE users in tracking down a defective unit.

Local Loopback (LL Test): This test condition is equivalent to CCITT test loop #3. It provides a way in which a DTE can check the functioning of a DTE-to-DCE interface and the transmit and receive sections of the local DCE. One may also test the local DCE with a test set instead of through the DTE. The output of the transmitting portion of the DCE is returned to the receiving station in the LL test through circuitry that is required for proper operation. In many DCEs, the signal transmitted is unsuitable for direct connection to the receiver. In such cases, an appropriate signal shaping or conversion in the loop-around circuitry may be included so that any element used in normal operations are checked in the test condition.

Remote Loopback (RL Test): This test, equivalent to CCITT test loop #2, allows a DTE or a facility test center to check the transmission path through the remote DCE to the DTE interface and the corresponding return path. In this test, Circuit SD and Circuit RD are either isolated or disconnected from the remote DTE at the interface and then connected to each other at the remote DCE. In synchronous DCEs, a suitable transmit clock may be necessary when the RL test condition is initiated. In some instances, buffer storage may be required between Circuit RD and Circuit SD.

Remote control of the RL test permits the automation of end-to-end testing of any circuit from a central location. Primarily, test control is suitable in point-to-point applications, but may also be used in multipoint arrangements with the addition of an address detection feature in the DCE. Test RL enables circuit verification without the aid of a distant DCE, supported by an inherent remote loopback ability in many modern DCEs.

The ON states of Circuit RL and Circuit LL are mutually exclusive, because the two test conditions may not function simultaneously.

Equalizers

Equalization is a process whereby a circuit's frequency and phase distortions are reduced to compensate for differences in time delay and attenuation of the varying frequencies in the transmission band. An equalizer associated with the DCE may require training, a process that produces a fixed number of equally spaced reference signals.

RS-449 outlines the procedures for equalizer training. The following example outlines a typical training sequence. DCE "E" (East) has an equalizer that requires training. DCE "W" (West) is transmitting toward DCE "E". Initial training of DCE "Es" equalizer occurs during the interval between the ON condition of Circuit RS and the ON condition of Circuit CS of DCE "W". Initial training in the DCE "Es" receiver occurs prior to the ON condition of Circuit RR of DCE "E". Circuit SQ is placed in the ON condition no later than the OFF-to-ON transition of Circuit RR if the initial training is successful. Circuit SQ's state is undefined when Circuit RR is OFF.

If the equalizer requires a unique training signal from DCE "W" to achieve equalization, the states of specific interchange circuits are controlled during this process. When the normal flow of data toward DCE "W" is interrupted in order to cause DCE "W" to transmit this unique sequence, Circuit CS of DCE "E" is held in the OFF condition while the command signal is being sent. In this situation, Circuit SQ of DCE "W" should be placed in the OFF condition while receiving the command signal. Circuit RD of DCE "W" may be clamped to the marking condition while the command signal is received. In the reverse direction, Circuit CS of DCS "W" is in the OFF condition while the unique training signal is sent. Circuit RD of DCE "E" may be clamped to the marking condition when the unique training signal is received. When the equalizer attains proper adjustment, DCE "E" places Circuit SQ in the ON condition.

Standard Interfaces for Selected Configurations

Standard sets of interchange circuits for data transmission configurations are defined as follows: Type SR (Send-Receive), Type SO (Send-Only), Type RO (Receive-Only), and Type DT (Data and Timing only). Table 5 lists the interchange circuits that must be provided for each data transmission configuration. For a given type of interface, generators and receivers must be provided for every interchange circuit designated M (Mandatory) in Table 5. In addition, generators and receivers are necessary for all interchange circuits designated S and T, where the service is switched and synchronous, respectively. ■