EY-D2055-WB-001

RK05 Subsystem Maintenance SPI Course

Student Workbook

digital

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Student Workbook

A Portion Of Course
EY-D2079-SP-001

Prepared by Educational Services
Digital Equipment Corporation

First Edition, June 1981

Printed in U.S.A.

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RKØ5 DISK SUBSYSTEM MAINTENANCE

Student Guide

COURSE DESCRIPTION

This self-paced instruction (SPI) course describes both the RK11/RKØ5 and RK8-E/RKØ5 disk subsystems. The course consists of ten modules, each of which includes a test that you must successfully complete before you can advance to the next module. Six of these tests are written, and the remaining four are laboratory projects.

Following is a detailed outline of the tasks an RK-trained Field Service engineer should be able to perform.

FIELD SERVICE JOB ANALYSIS OF RK DISK SUBSYSTEM MAINTENANCE

- Install a drive
    - Cable a drive to a subsystem
    - Mount the drive into a rack
    - Run diagnostics on an RK subsystem
        - Use conversational mode
        - Interpret error printouts
        - Interpret normal printouts
        - Loop on sub-test of diagnostics
- Perform preventive maintenance procedures
    - Change filters
        - Open covers
        - Insert and remove cartridge
        - Remove front panel
        - Use operator control panel
    - Clean an RK drive
    - Check adjustments
- Perform Corrective Maintenance
    - Make modules accessible
    - Write manual-entry programs to aid troubleshooting
    - Correct any adjustment on an RK subsystem drive
        - Positioner servo
        - Data separator
        - Heads
        - Power supply
    - Remove and replace the failing field replaceable unit (FRU)

SUMMARY OF MODULE TOPICS

- Introduction/Physical Description
- RK11 Subsystem Registers and Commands
- RK11 Theory of Operation
- RK8-E Subsystem Registers and Commands
- RK8-E Theory of Operation
- RKØ5 Theory of Operation
- Adjustments and Alignments
- Component Location
- Preventive Maintenance
- Diagnostics
- Troubleshooting

This course has five laboratory projects in which you will perform the tasks listed below.

- Perform all preventive maintenance procedures
- Perform servo adjustments
- Perform head alignment
- Perform sector/index timing adjustment
- Locate the components on the following list and then remove and replace those components identified on the list with an asterisk (*)

    - Linear positioner*
    - Control and indicators
    - Read/write heads*
    - Sector transducer
    - Carriage bearings
    - Front door interlock
    - Logic chassis
    - Spindle*
    - Blower motor
    - Duckbill
    - Spindle drive motor and belt*
    - Absolute filter
    - Linear positioner transducer
    - Power supply regulators; +5, -5, and -15 vdc

- Load, run and use the diagnostics
- Troubleshoot administrator-inserted problems

PREREQUISITES

Prior to taking this course on the RKØ5, you must have taken the courses on the following list or have equivalent experience and knowledge.

- Introduction to the PDP-11 A/V course (11-family students only)
- 8E/8A Systems Training (8-family students only)
- Basic Disk Principles A/V course
- Magnetic Recording Techniques A/V course

The knowledge you have from this training should include the topics listed below.

- 11-family students
  - Programming UNIBUS peripherals
  - UNIBUS signal transmissions
- 8-family students
  - OMNIBUS signal transmissions
  - Programming OMNIBUS peripherals
- All students
  - General care of disk packs
  - Frequency modulation magnetic recording technique
  - Basic disk drive terminology

PREREQUISITE TEST DESCRIPTION

Take the prerequisite test to demonstrate your knowledge in the prerequisite areas. There are separate questions on the prerequisite test for the 11-family and 8-family trained students.

SMALL DISK SPECIALIST CURRICULUM

This course, the RK05 Disk Subsystem Maintenance course, is part of the small disk specialist curriculum. The other two courses in the curriculum are the RX01/RX02 Disk Subsystem Maintenance course and the RL01/RL02 Disk Subsystem Maintenance course.

Figure 1-1 shows the small disk specialist curriculum map. Note that both the Basic Disk Principles course and the Magnetic Recording Techniques course must be completed before beginning the RK05, RX01/RX02, or RL01/RL02 courses.

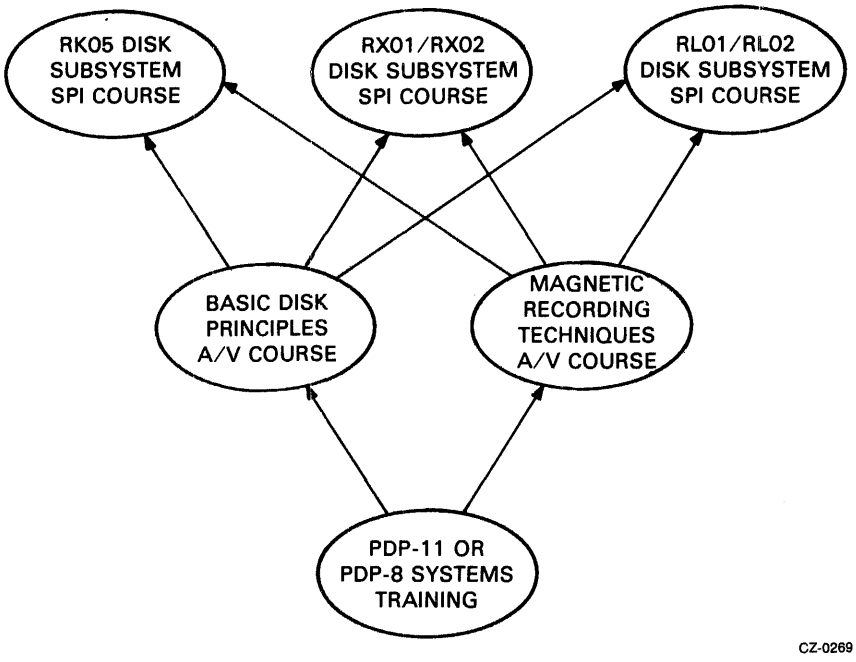


Figure 1-1 Curriculum Map

COURSE NON-GOALS

This course does not use any field maintenance print sets to explain individual circuit operation. The print sets may be followed, however, as you study the block diagrams in the text. Each block within a diagram contains a mnemonic referencing a field maintenance print set page to correlate the diagram to the print sets.

MAINTENANCE PHILOSOPHY

The primary maintenance philosphy is to isolate RK11/RK05 or RK8-E/RK05 subsystem malfunctions to the failing field replaceable unit (FRU) level, and then to replace the FRU.

COURSE OUTLINE

Each major heading corresponds to a course module title.

Introduction/Physical Description

Introduction and physical description of the items listed below

- RK05/05J/05F Disk Drive description
- RK05 controls and indicators
- RK11/RK05 Subsystem
  - RK11 options
  - RK11 module functions
- RK8-E/RK05 Subsystem
  - RK8-E module functions

RK11 Subsystem Registers and Commands

Use and description of the registers listed below

- RKDS
- RKER
- RKCS
- RKWC
- RKBA
- RKDA
- RKDB

Use and description of the commands listed below

- Control reset
- Seek
- Drive reset
- Write lock
- Write
- Read
- Write check
- Read check

RK11 Theory of Operation

Description of the major circuit elements on the modules listed below

- Status and control
- Disk control
- Data path
- Bus control

Description of the data path for the commands listed below

- Write
- Read
- Write check

RK8-E Subsystem Registers and Commands

Use and description of the registers listed below

- Command register
- Current address
- Disk address
- Status register
- Four-word data buffer
- Major state register
- Module 12 and 16-bit counters
- Module 128 or 256-word counters

Use and description of the commands listed below

- Read data
- Read all
- Set write protect
- Seek only
- Write data
- Write all

RK8-E Theory of Operation

Description of the major circuit elements on the modules listed below

- Data buffer and status
- Major register module
- Control module

RKØ5 Theory of Operation

Use and description of the interface signals between the RK11/RK8-E and the disk drive

Use and description of the items listed below

- Read/write module
- Cylinder address and difference module
- Positioner and servo module
- Index and sector module
- Control panel
- Power supply

Description of the circuits listed below

- Sector/index pulse generator
- Cylinder addressing circuit
- Servo system
- Positioner control system
- Read/write control system

RKØ5 Component Removal/Replacement

Laboratory exercise to give practice in locating drive components

Laboratory exercise to give practice in removing and replacing the components listed below

- Linear positioner
- Carriage
- Spindle
- Spindle drive motor and belt

RKØ5 Adjustments/Alignments

- Servo adjustments
- Head alignments
- Sector/index timing adjustments
- Data separator adjustment

Subsystem Diagnostics

Description of the items listed below

- RK11/RKØ5 Subsystem diagnostics
- RK8-E/RKØ5 Subsystem diagnostics
- Switch register options
- Use of the subsystem diagnostics

Administrator-inserted problems will be isolated by the student.

COURSE ORGANIZATION

Course Map

Figure 1-2 shows the course map. Each oval on the map corresponds to a different course module. The course starts at the bottom of the map and should be completed in the sequence illustrated. No new modules should be started until all modules whose arrows lead into it are completed.

NOTE

- **PDP-11 trained students need only complete the "RK11 Subsystem Registers/Commands" and "RK11 Theory of Operation" modules prior to starting the "RKØ5 Theory of Operation" module.**
- **PDP-8 trained students need only complete "RK8-E Subsystem Registers/Commands" and "RK8-E Theory of Operation" modules prior to starting the "RKØ5 Theory of Operation" module.**

Module Contents

Each module consists of five parts. The first part is the introduction to the module. The introduction describes what is in the module. Following this are one or more objectives which state what you must be able to do to complete the module. The next part is the text of the module. At the end of the text is a summary of the text. The last part of the module is the test.

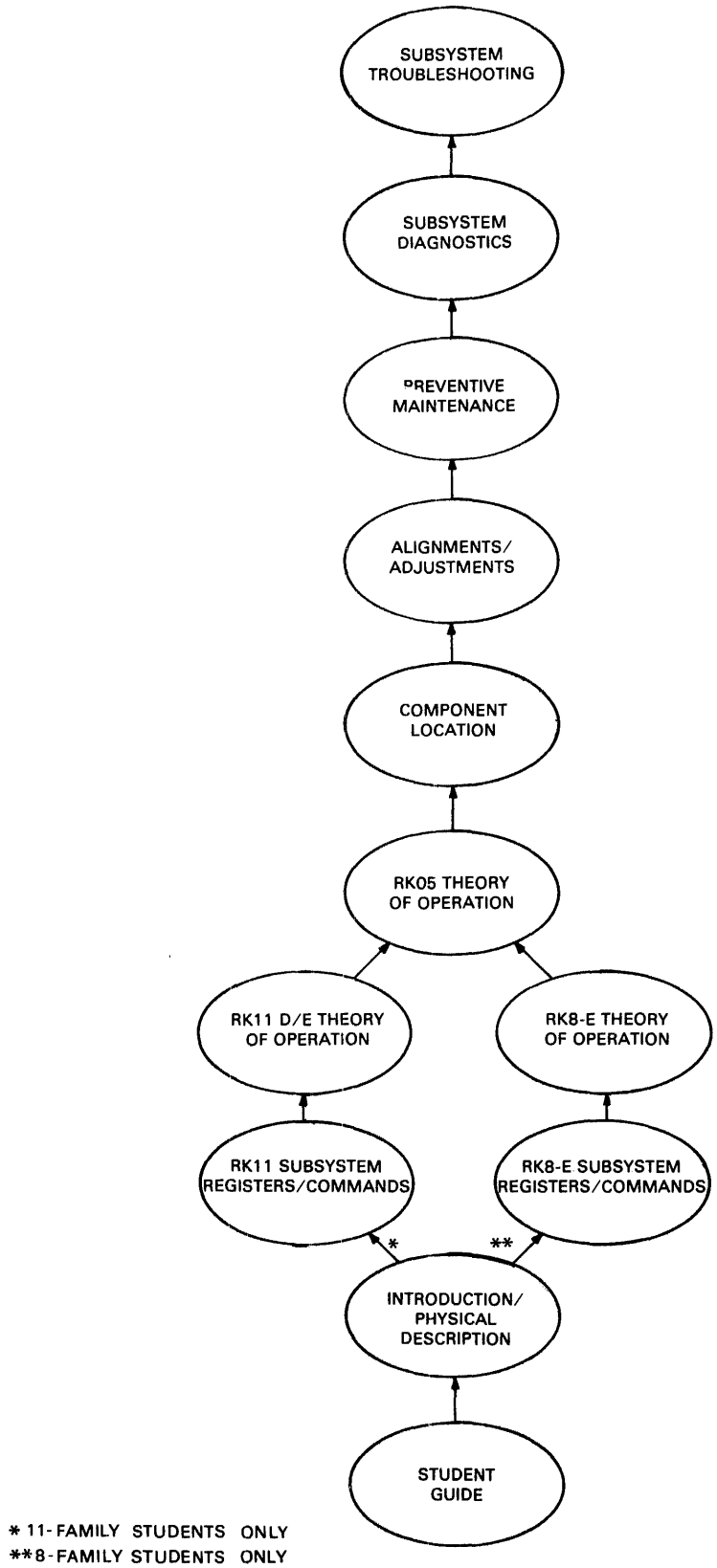


Figure 1-2 Course Map

Testing

The first six modules include a written module test. These tests cover the material defined in the objectives. Three of these modules also contain a module exercise which must be completed prior to taking the module test.

The last four modules do not have a written test, but have laboratory worksheets which cover the material defined in the objectives.

To complete each module satisfactorily, you must meet the criteria stated in each module objective.

Evaluation

As you complete each module test, the course administrator will check your answers and review the material with you. As you satisfactorily complete each module, the course administrator will update the master Progress Plotter and your Personal Progress Plotter (below) to keep a record of your progress.

If you do not satisfactorily complete a module, assistance from the course administrator and/or peers may be necessary so that you will understand the material, and be able to re-take the test. All tests and answers to the test are packaged separately.

Extra Illustrations

Several of the illustrations used in this course are also packaged separately from the course workbook itself. This is so you can read the text and refer to these illustrations without having to turn pages back and forth. Your course administrator has these extra illustrations. Before starting the course ask your administrator for these illustrations.

COURSE RESOURCES

There are three types of course resources. The first type of resource is the group of materials that come with the course itself and are yours to keep. The second type of resource is the group of materials that you must use to complete the course, but which are only available from the course administrator. These resources stay in the classroom. The third type of resource is the group of materials that you might want to refer to while taking this course. The materials in the third group include other Field Service documentation that pertain to the drives and controllers, and documentation pertaining to host-system CPUs and instruction sets.

Resources to Keep

Student Workbook	EY-D2Ø55-WB
Laboratory Projects Workbook	EY-D2Ø67-WB
PDP-11 DECdisk Subsystem Quick Reference Card	EH-18955

Resources Necessary for Course Completion

RK11-D Disk Drive Controller Print Set	MP-ØRK11-DØ
RK8-E Disk Drive Controller Print Set	MP-ØRK8J-EØ
RKØ5/Ø5J/Ø5F Disk Drive Maintenance Manual	EK-RK5JF-MM
RKØ5J/F Disk Drive Print Set	MP-ØRKØ5-JØ
PDP8-E Maintenance Manual (Volumes 1 and 2)	
RK11/RKØ5 diagnostics and listings	
RK8-E/RKØ5 diagnostics and listings	
PDP-11 Programming Card	EH-Ø5185
PDP-8 Programming Card	
PDP-11 Processor Handbook	EH-17716

Resources for Additional Studying

RK11D/E Controller User's Manual	EK-RK11D-OP
RK11D/E Controller Manual	RK-RK11D-MM
PDP-8/E Maintenance Manual (Volume 3)	DEC-8E-HMM3A-C-D
RKØ5 Disk Drive User's Manual	EK-RKØ5-OP
PDP-11 Peripherals Handbook	EB-Ø7667

Now you may take the prerequisite test. The course administrator has the answers and the test.

PERSONAL PROGRESS PLOTTER

Modules	Date Achieved	Initials
Introduction/Physical Description		
RK11 Subsystem Registers/Commands		
RK11 Theory of Operation		
RK8-E Subsystem Registers/Commands		
RK8-E Theory of Operation		
RKØ5 Theory of Operation		
Component Location		
Alignments/Adjustments		
Subsystem Diagnostics		
Subsystem Troubleshooting		

RKØ5 DISK SUBSYSTEM MAINTENANCE

Introduction/Physical Description

INTRODUCTION/PHYSICAL DESCRIPTION

INTRODUCTION

The RKØ5 Disk Drive is one of the smaller disk drives in the DIGITAL family of mass storage devices. Even though you are a newly-hired DIGITAL Field Service Engineer, you will find RKØ5 Disk Drive maintenance easy to learn. This course will give you the knowledge required to intelligently maintain and repair this drive. This module introduces the RKØ5 drive and the RK11D/E and RK8-E Controllers that are used with the various DIGITAL central processors. The text will describe the physical structure of each subsystem and present an overall block diagram of those subsystems.

OBJECTIVES

At the completion of this module you will be able to define the function of the major components of each device listed below.

- RK11 D/E Controllers
- RK8-E Controller
- RKØ5 Disk Drive

To demonstrate your ability to do this, you will be required to answer 12 out of 15 multiple-choice questions correctly within 2Ø minutes. You may use any reference material.

OPTIONAL RESOURCES

RK11D/E Moving Head Controller Manual	EK-RK11D-MM-ØØ2
RKØ5 Disk Drive User's Manual	EK-RKØ5-OP-ØØ1
PDP8-E/F/M Maintenance Manual, Vol. 3, Chapter 11	DEC-8E-HMM3A-C-D
RKØ5/RKØ5J/RKØ5F Disk Drive Maintenance Manual	EK-RK5JF-MM-ØØ1

DISK SUBSYSTEM CONFIGURATIONS

The RKØ5 Disk Drive is a random-access data storage device that is suited for use in small or medium size computer systems. There are actually three different versions of this drive, the RKØ5, the RKØ5J and the RKØ5F. The differences between these drives are described later in this module.

Any of these drives can be used with the 11-family, 15-family or 8-family computer systems. The central processor used determines which of the three controllers (RK11D, RK11E or RK8-E) is used. Table 2-1 shows the possible subsystem configurations for this device.

Table 2-1 Subsystem Configurations

Controller	Processor
RK11D (16 bit word)	PDP-11/04/05/34/40/45/60/70
RK11E (18 bit word)	PDP-15
RK8-E (12 bit word)	PDP-8A/8E/8F/8M

RK11D/RK11E SUBSYSTEMS

The RK11D/RK11E subsystems consist of one of the two RK11 Controllers and one or more disk drives.

Either RK11 Controller can control up to eight disk drives. This configuration will be some combination of RK05, RK05J and/or RK05F drives. Table 2-2 shows several possible configurations.

Table 2-2 Typical RK11D/RK11E Subsystem Configurations

Controller	Drives
RK11D	1 RK05, 1 RK05J
RK11D	8 RK05J
RK11E	1 RK05J, 3 RK05F
RK11E	4 RK05J, 2 RK05F
RK11D	4 RK05F

Figure 2-1 shows the largest possible configuration of an RK11 Controller with RK05J drives.

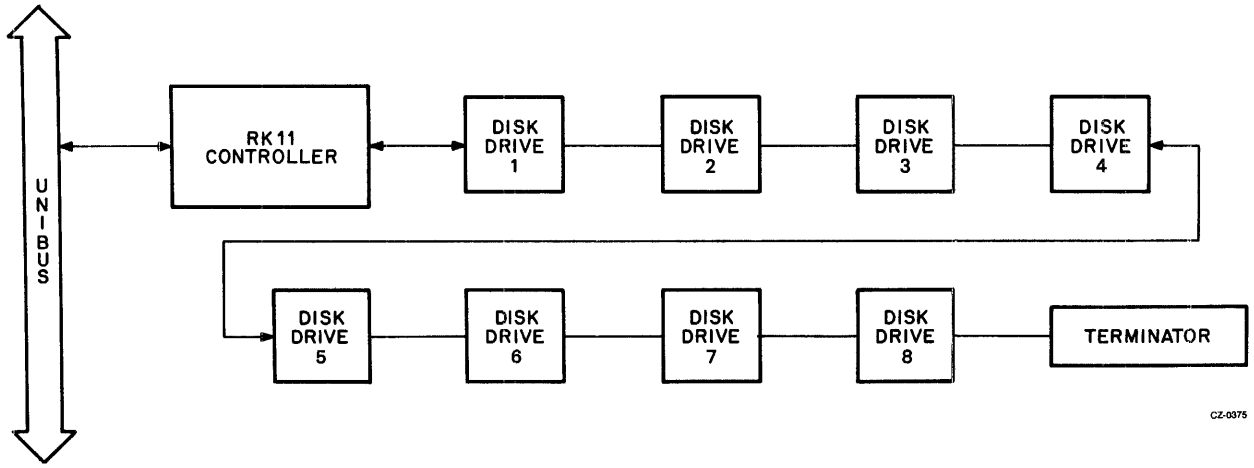


Figure 2-1 RK11/RK05J Disk Drive Subsystem

RK11D/RK11E Controllers

The RK11 Controller will be either an RK11D or an RK11E. The RK11D transfers 16-bit data words while the RK11E transfers 18-bit data words. Jumpers on the controller determine whether the RK11 is configured as an RK11D or RK11E.

RK11D Functional Description - The RK11D Controller is the interface between the drives and a PDP-11 processor via the UNIBUS. Figure 2-2 shows that the RK11D consists of four modules (M7254, M7255, M7256 and M7257). The interface with the disk drive is accomplished via a drive bus cable (DR BUS).

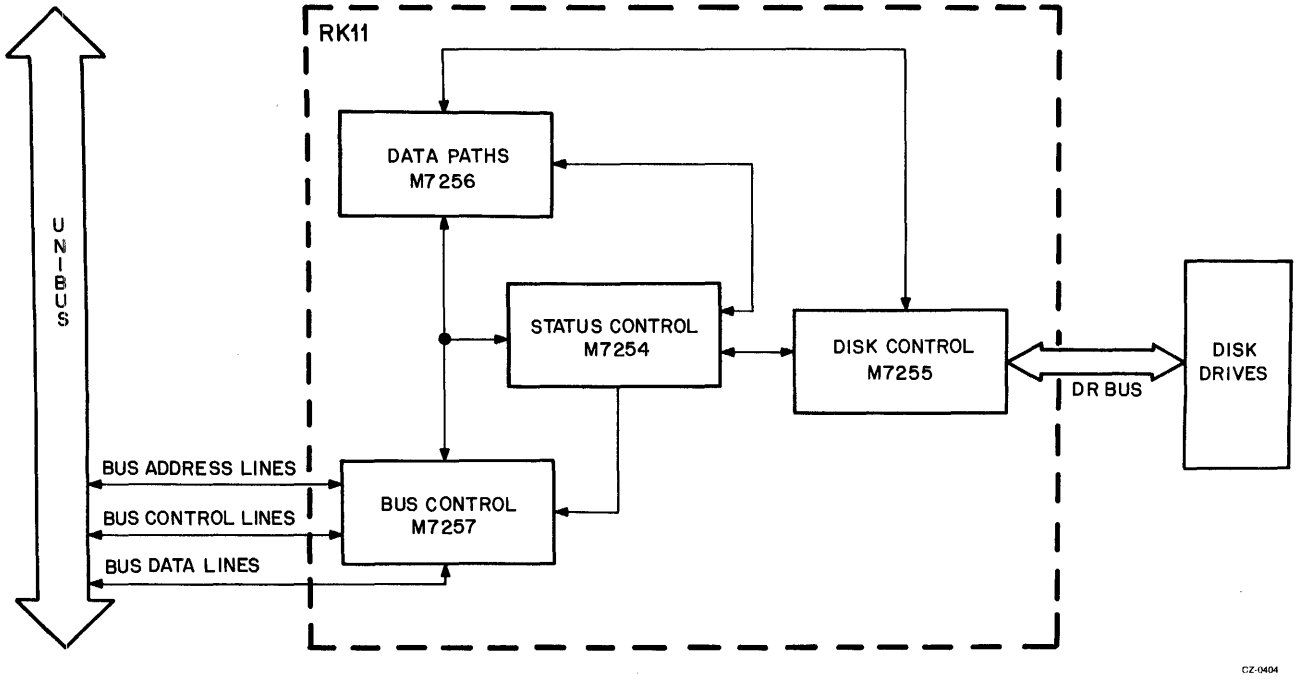


Figure 2-2 RK11 Controller Functional Block Diagram

The functions of the modules and drive bus are listed below.

- Status control (M7254) - initiates the programmable RK11 subsystem commands and monitors logic status conditions
- Disk control (M7255) - monitors drive status conditions and controls all drive functions
- Data paths (M7256) - transfer parallel data to and from the UNIBUS, and serial data to and from the drive

- Bus control (M7257) - interfaces the RK11 with the UNIBUS for address selection, NPR data transfers, and interrupt sequences

- DR BUS (Drive bus) - transmits interface signals between the RK11 and the RKØ5

RK11E Functional Description - The RK11E Controller consists of the same modules performing the same functions as those modules in the RK11D. There are differences in the module jumpers and crystal oscillator. The RK11E oscillator establishes a higher internal clocking rate than the RK11D to handle the longer word lengths used with the PDP-15 CPU.

RK8-E/RKØ5 SUBSYSTEM

The RK8-E Controller is the interface between the PDP-8 OMNIBUS and the drives. The RK8-E Controller can control up to four disk drives. This configuration will be some combination of RKØ5, RKØ5J and RKØ5F drives. Table 2-3 shows several possible configurations.

NOTE

The system containing a PDP-8 central processor can accomodate two RK8-E Controllers, for a maximum configuration of eight disk drives.

Table 2-3 Typical RK8-E Subsystem Configurations

Controller	Drives
RK8-E	2 RKØ5
RK8-E	4 RKØ5J
RK8-E	1 RKØ5J, 1 RKØ5F
RK8-E	2 RKØ5F

RK8-E Functional Description

The RK8-E Controller is the interface between the drives and a PDP-8 processor via the OMNIBUS. Figure 2-3 shows that the RK8-E consists of three modules (M71Ø4, M71Ø5 and M71Ø6). They are joined with H851 top connectors and inserted into the OMNIBUS. The RK8-E is connected to the drives by a 7Ø-Ø9Ø26 (BC11A) I/O cable.

NOTE

The M71Ø5 module can be accidentally inserted upside down into the OMNIBUS. If the subsystem is cabled up and powered on when this module is upside down, the module will be destroyed.

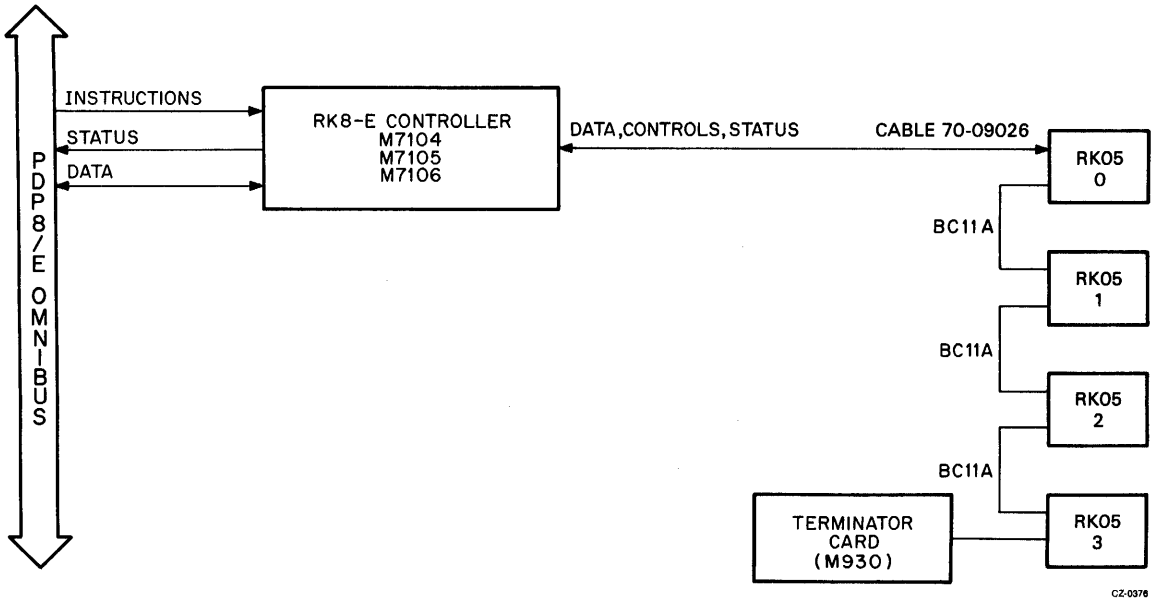


Figure 2-3 RK8-E Controller and RKØ5 Disk Drive Subsystem Block Diagram

The basic function of each RK8-E module is listed below.

- Data buffer register and status module (M71Ø4) - contain the data buffer and monitors status.
- Major registers module (M71Ø5) - contains the major registers.
- Control module (M71Ø6) - contains the control logic for the RK8-E.

Jumpers on the M71Ø4 module select the proper device code and priority.

Now that you have seen the basic configurations for the various controllers, read the following text, which describes the physical make-up of the drives themselves.

DISK DRIVES

As previously stated, the RKØ5, RKØ5J and RKØ5F Disk Drives are random-access data storage devices that are used on small- or medium-sized computer systems.

Data Cartridge

These drives use a single-disk cartridge as the storage medium. A 12 sectors/track cartridge is used with PDP-11 and PDP-15 computer systems. A 16 sectors/track cartridge is used with PDP-8 computer systems.

There is one movable head for each of the two surfaces of the disk platter. Data is read from or recorded on the surfaces, using the frequency modulated encoding technique. In all three drives, the platter turns at 1500 revolutions per minute.

RK05 Disk Drive

This drive represents the original design effort by DIGITAL engineering. The drive can store up to 25 million bits of on-line data (1.24 million PDP-11 words) on 203 cylinders.

RK05J Disk Drive

This drive is an updated version of the original RK05. It includes all the engineering changes that the RK05 has incurred throughout the years of use. One typical change is in the design of the cartridge receiver.

RK05F Disk Drive

This drive is a double density version of the RK05J. It is also a fixed-media device in that the cartridge cannot be removed by the operator. The cartridge contains 406 cylinders and must be logically addressed by the controller as two physical RK05J drives. This addressing scheme eliminated the need for redesigning the controllers.

Combinations of RK05, RK05J, and RK05F Disk Drives on the same subsystem are possible, as long as any one RK05F drive has a drive select number that is even (0, 2, 4 or 6). For example, the controller will recognize a drive with a drive select number of "4" as logical units "4" AND "5".

MAJOR ASSEMBLIES AND SYSTEMS

All the RK05 drives include the major assemblies and systems listed below.

- Linear positioner
- Spindle and drive motor
- Cartridge handling system
- Logic assembly
- Air supply system
- Power supply
- Read/write heads
- Controls and indicators

Figures 2-4, 2-5, and 2-6 show the location of these major assemblies for the RK05, RK05J and RK05F. The text below gives a brief description of the functions of each major assembly. There are also several detailed figures to accompany these descriptions.

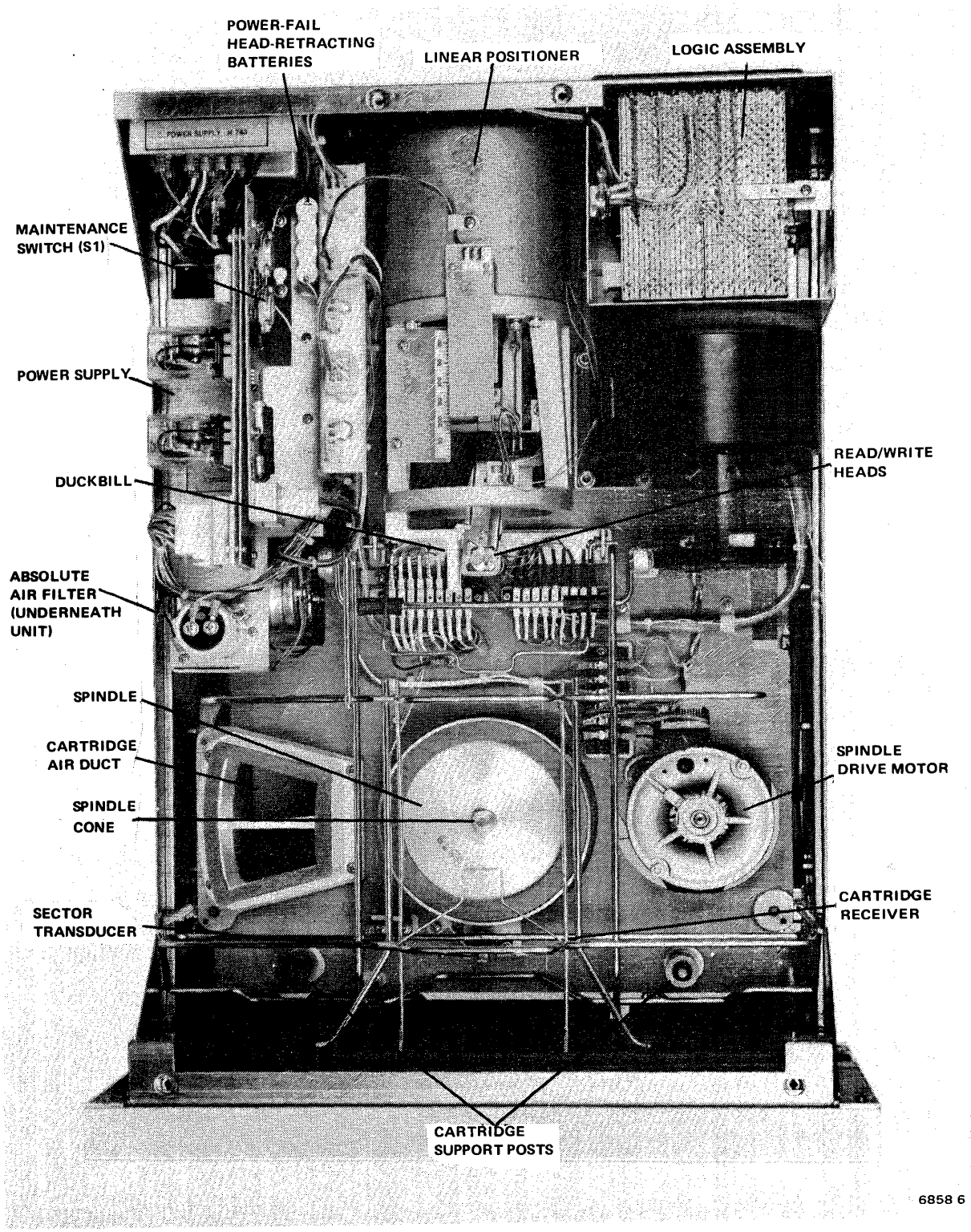


Figure 2-4 Location of Major Assemblies and Systems (RKØ5)

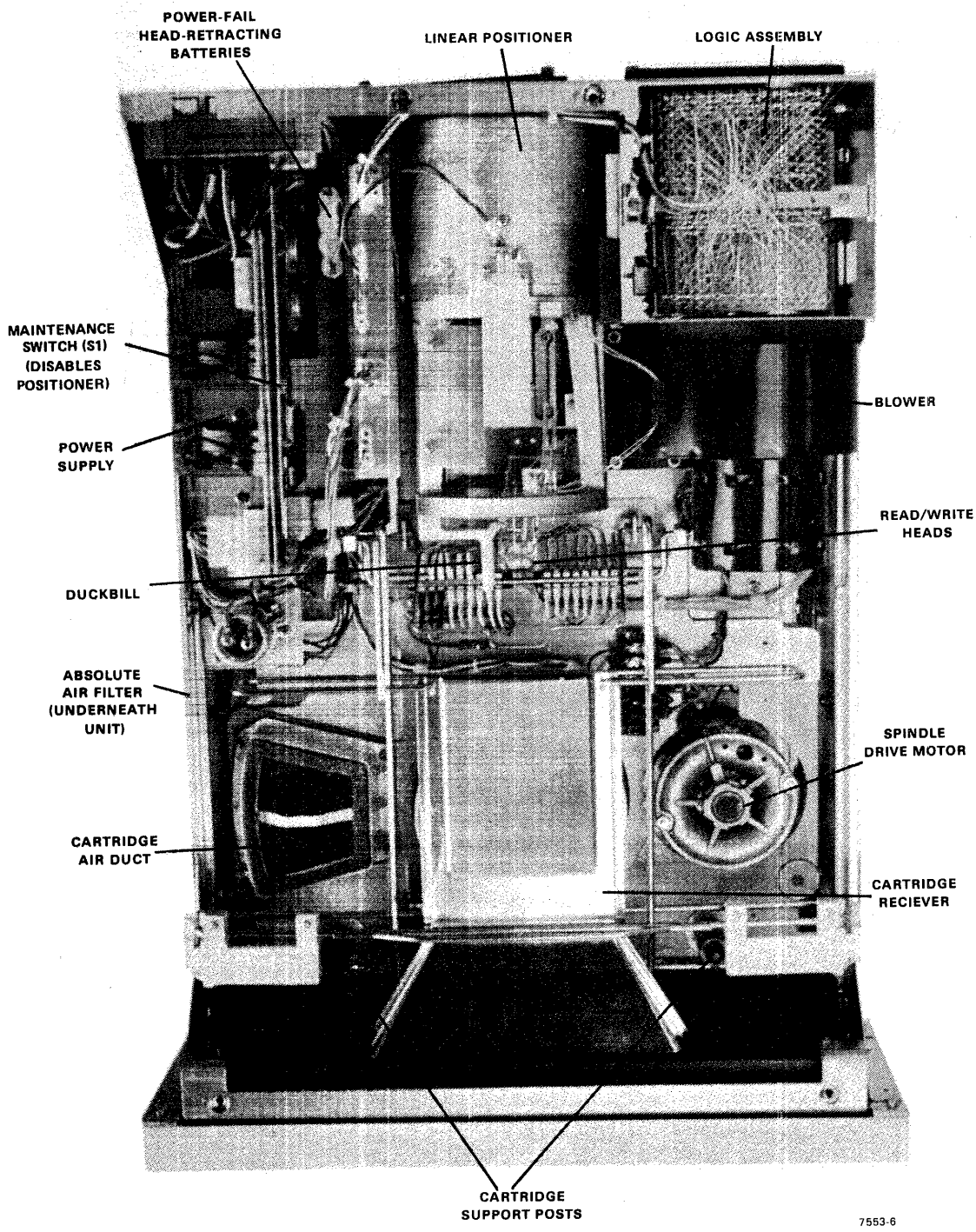


Figure 2-5 Location of Major Assemblies and Systems (RKØ5J)

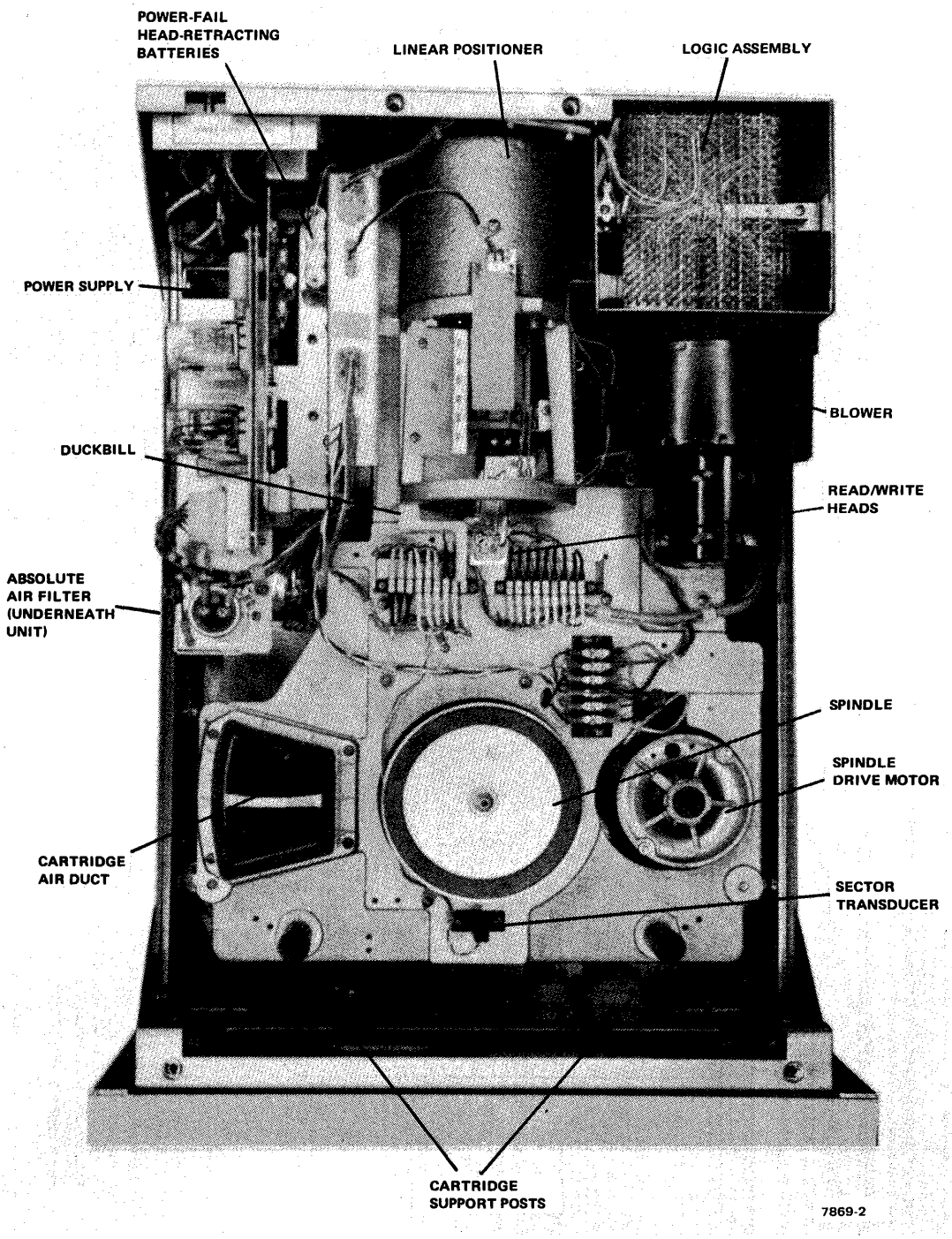


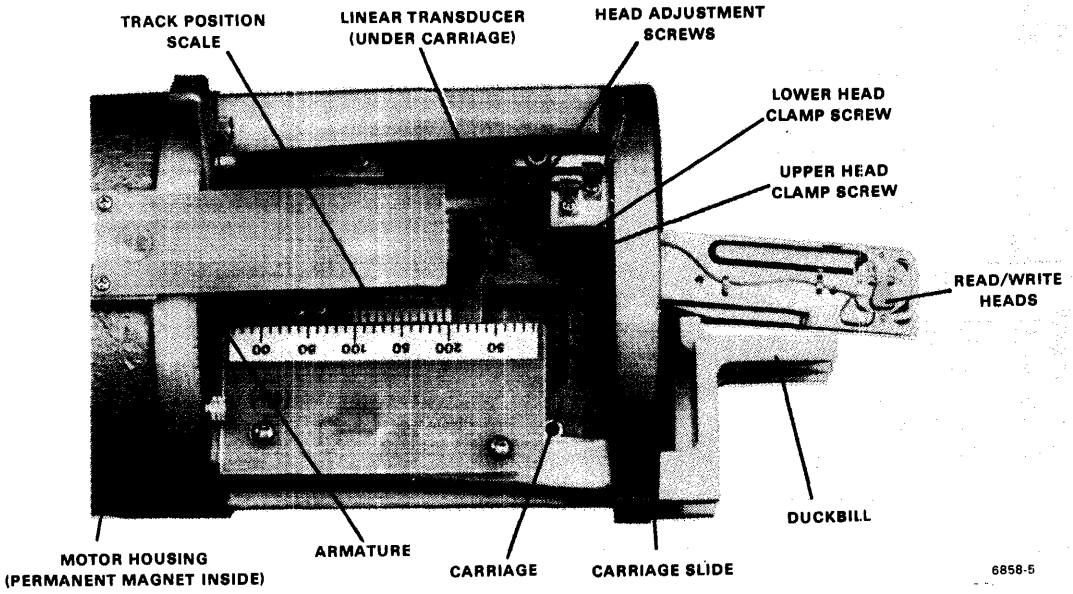
Figure 2-6 Location of Major Assemblies and Systems (RKØ5F)

Linear Positioner Assembly

The linear positioner assembly consists of the linear motor, the carriage, the read/write heads and the linear positioner transducer. The read/write heads (attached to the carriage) move across the surface of the disk when the motor moves the carriage.

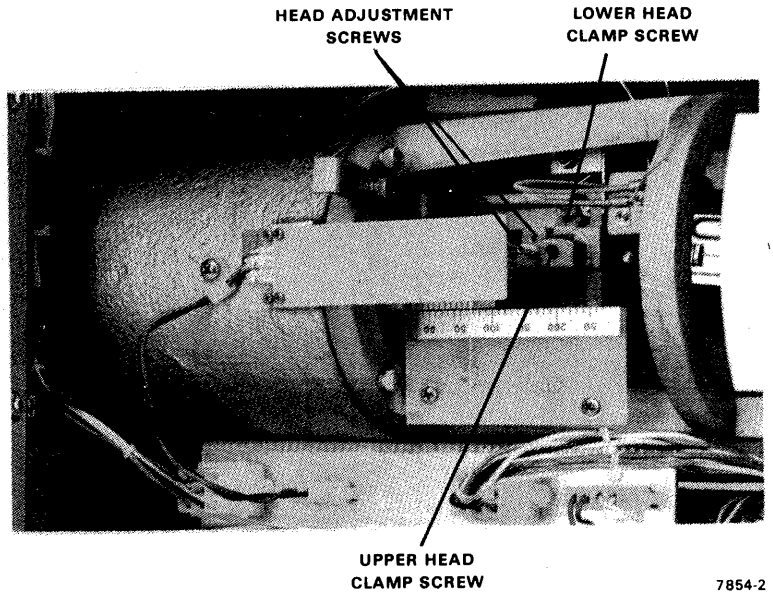
The linear positioner transducer, located under the carriage, detects carriage movement. The control logic uses the transducer output to determine the cylinder position of the heads, and the servo logic uses the same output to control the speed of carriage travel.

Figures 2-7a and 2-7b show the differences between the older style and newer style carriages. The major difference is the placement of the adjustment and clamping screws for the read/write heads.



a Older Style Carriage

Figure 2-7 Carriage Styles



b Newer Style Carriage

Figure 2-7 Carriage Styles (Cont.)

Spindle and Drive Motor System

The spindle and drive motor system (Figure 2-8) consists of the spindle, the spindle drive motor and the recording disk. A 50/60 hertz, split-phase ac motor transfers torque (via the drive belt) to the spindle drive pulley. Belt tension is maintained by a tension spring anchored to the baseplate.

The spindle speed is monitored by a circuit that measures the interval between index pulses. When the interval increases to approximately 45 milliseconds, indicating the spindle is moving too slowly, the drive cycles down. If the RUN/LOAD switch is placed in the LOAD position, ac power is removed from the motor, and the spindle coasts to a halt.

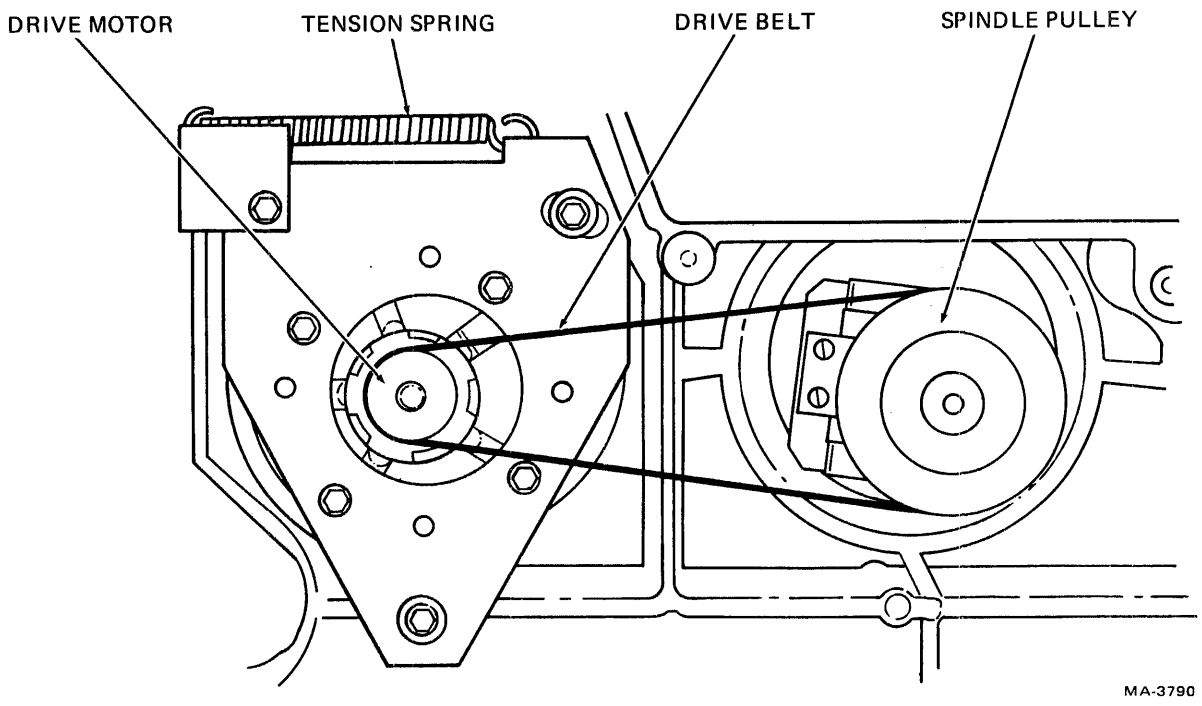


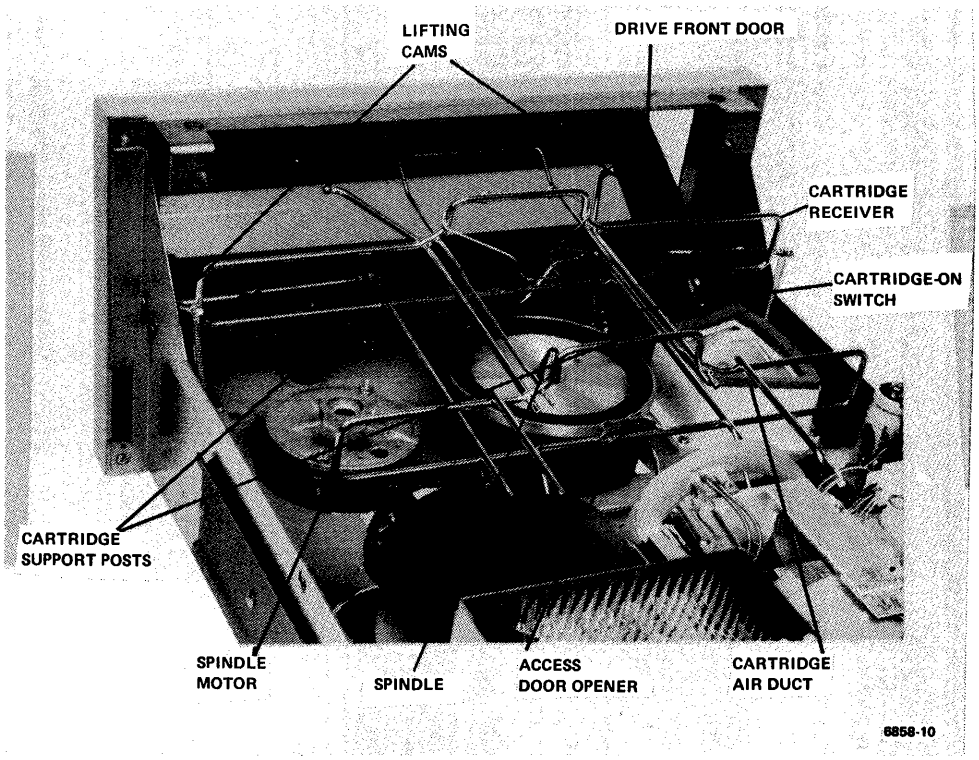
Figure 2-8 Spindle and Drive Motor System

Cartridge-Handling Systems

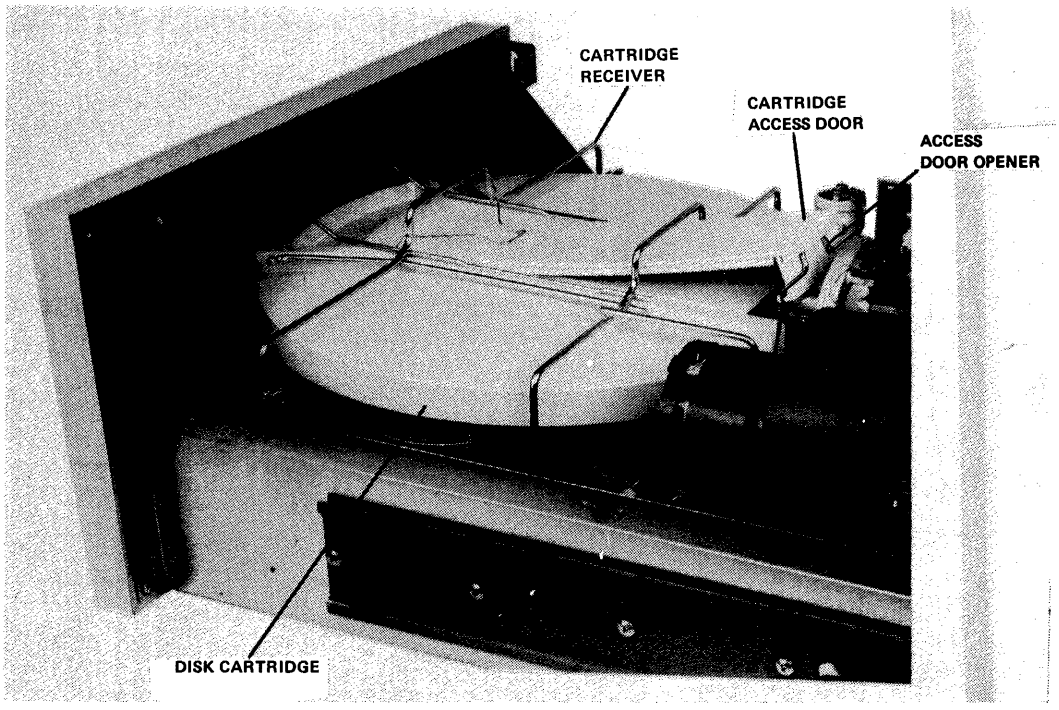
There is a different cartridge-handling system in each of the three types of RKØ5 drives. The three different systems are described below.

RKØ5 Cartridge-Handling System - This system (Figure 2-9) consists of a cartridge receiver, two receiver lifting cams, an access door opener, a duckbill, and cartridge-support posts.

The cartridge receiver guides the cartridge into an operating position. The duckbill and support posts hold the cartridge in place to allow the recording disk to rotate with the spindle. The rotating spindle drives the disk by magnetic coupling at the disk hub.



a Cartridge Removed



b Cartridge Inserted

Figure 2-9 RKØ5 Cartridge-Handling System

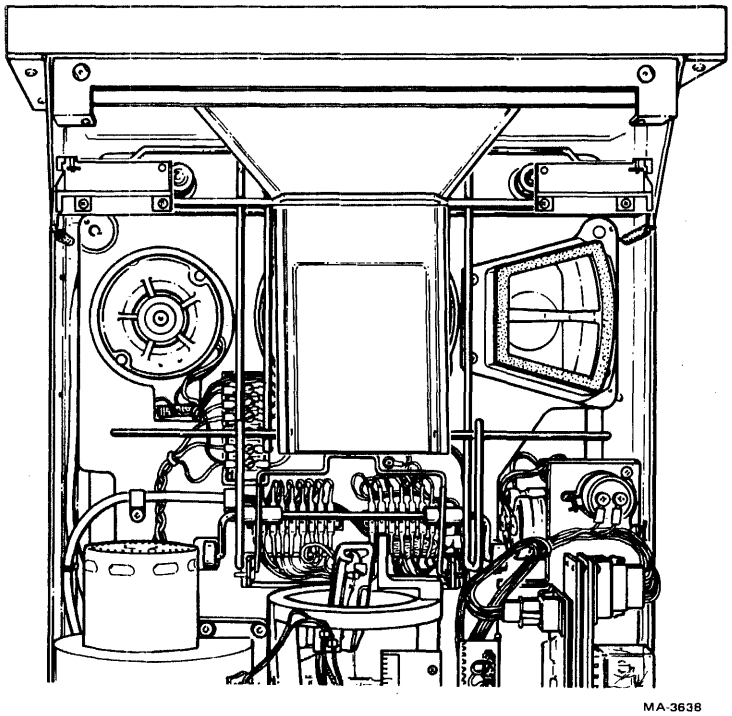
The operator opens the front door to insert a cartridge. When the door is pulled down, lifting cams linked to the front door rotate, elevating the receiver to a slanted position. When the operator inserts a cartridge into the receiver, the access door opener opens the access door in the rear of the cartridge cover. The read/write heads can then enter the cartridge.

As the operator closes the door, the lifting cams lower the receiver to the operating position and magnetic coupling holds the disk hub to the spindle. When the cartridge is in the operating position, the plastic case pushes the cartridge-on switch, indicating to the logic that a cartridge is present.

RKØ5J Cartridge-Handling System - This system (Figure 2-1Ø) is similar to the RKØ5 system, with the addition of two cartridge clamps to provide more positive cartridge seating. As the door is closed, the receiver is lowered, and the cartridge clamps are brought down to the upper surface of the cartridge. This ensures proper cartridge seating on the support posts.

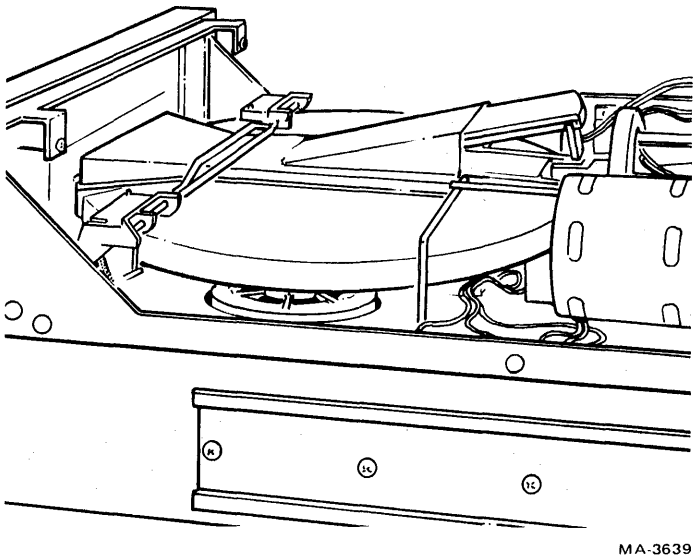
As the operator opens the door, the lifting cams rotate to elevate the cartridge receiver and lift the cartridge clamps away from the cartridge. The cartridge can then be removed.

In all other functional aspects, the RKØ5 and RKØ5J cartridge-handling systems are the same.



a Cartridge Removed

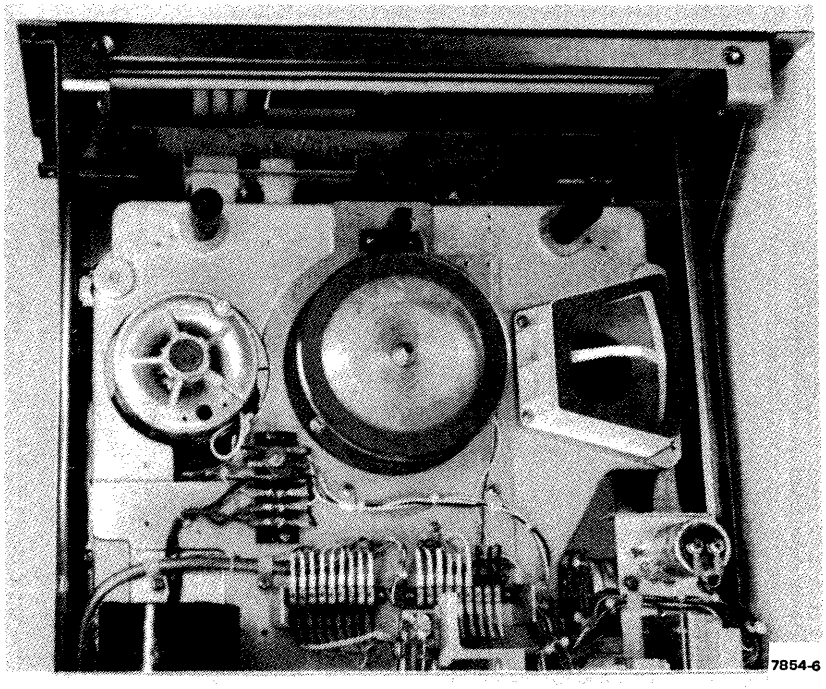
Figure 2-1Ø RKØ5J Cartridge-Handling System



b Cartridge Inserted

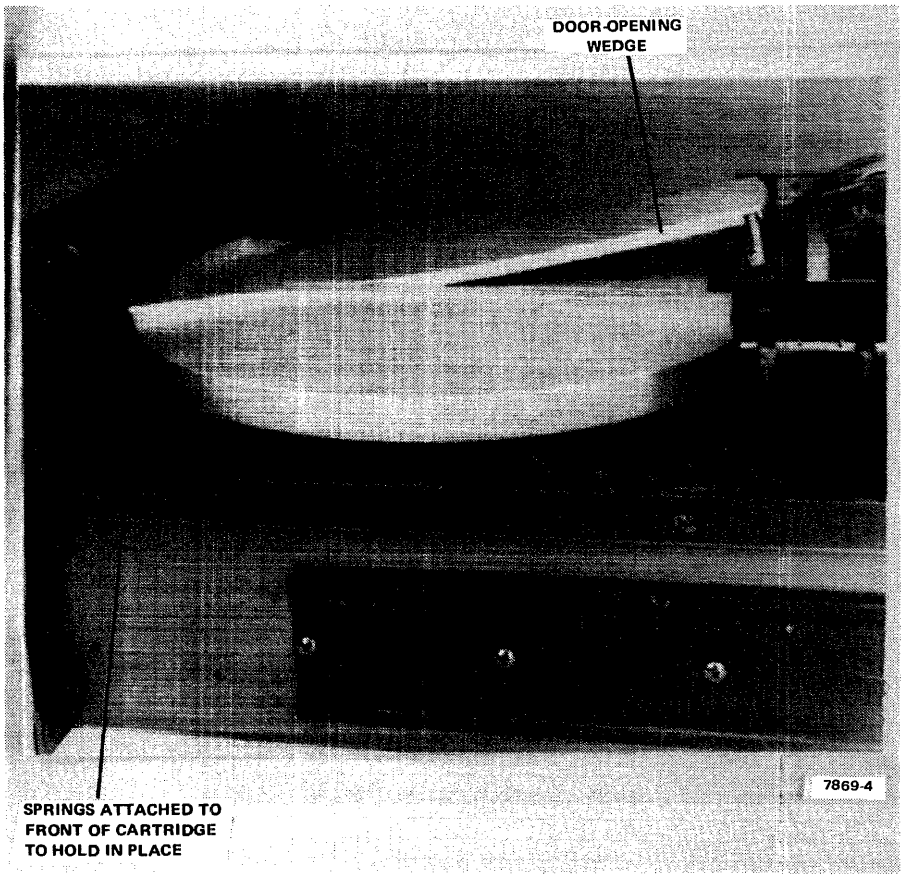
Figure 2-10 RK05J Cartridge-Handling System

RK05F Cartridge-Handling System - Because the RK05F has a fixed cartridge, its cartridge-handling system (Figure 2-11) is considerably simpler. This system consists of a duckbill, a door-opening wedge, two cartridge-support posts, two cartridge-retaining springs, and a cartridge-guide bracket.



a Cartridge Removed

Figure 2-11 RK05F Cartridge-Handling System



b Cartridge Inserted

Figure 2-11 RKØ5F Cartridge-Handling System

When the drive is installed, the cartridge is lowered through the top of the drive and onto the spindle and support posts. The cartridge is then secured with the cartridge-retaining springs, and a door-opening wedge is inserted to hold the access door open for the heads.

Figures 2-12 and 2-13 show the position of the holddown springs when the RKØ5F cartridge is installed.

Logic Assembly

The logic assembly is located in the right-rear portion of the disk drive, and has eight slots for printed circuit modules. Three of the slots contain the drive functional logic and the read/write modules. Two of the slots contain positioner servo logic modules. One slot is for the cable connector that interfaces the drive electronics with the positioner and other physical components. The remaining two slots are used for controller-to-drive interface cables and/or terminators.

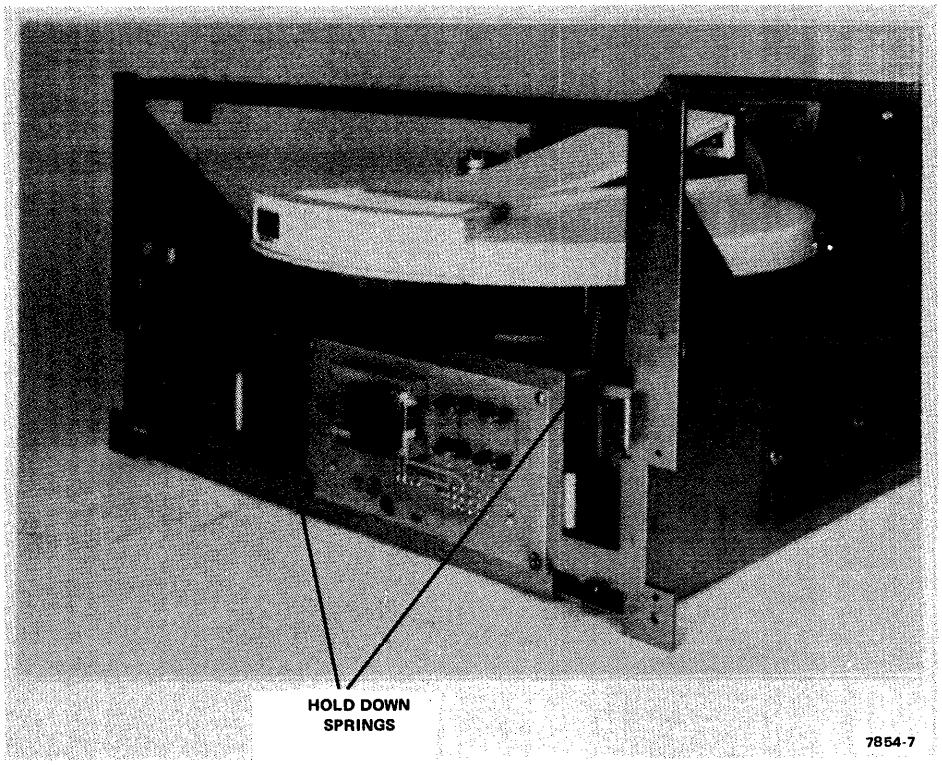


Figure 2-12 RKØ5F Cartridge Installed

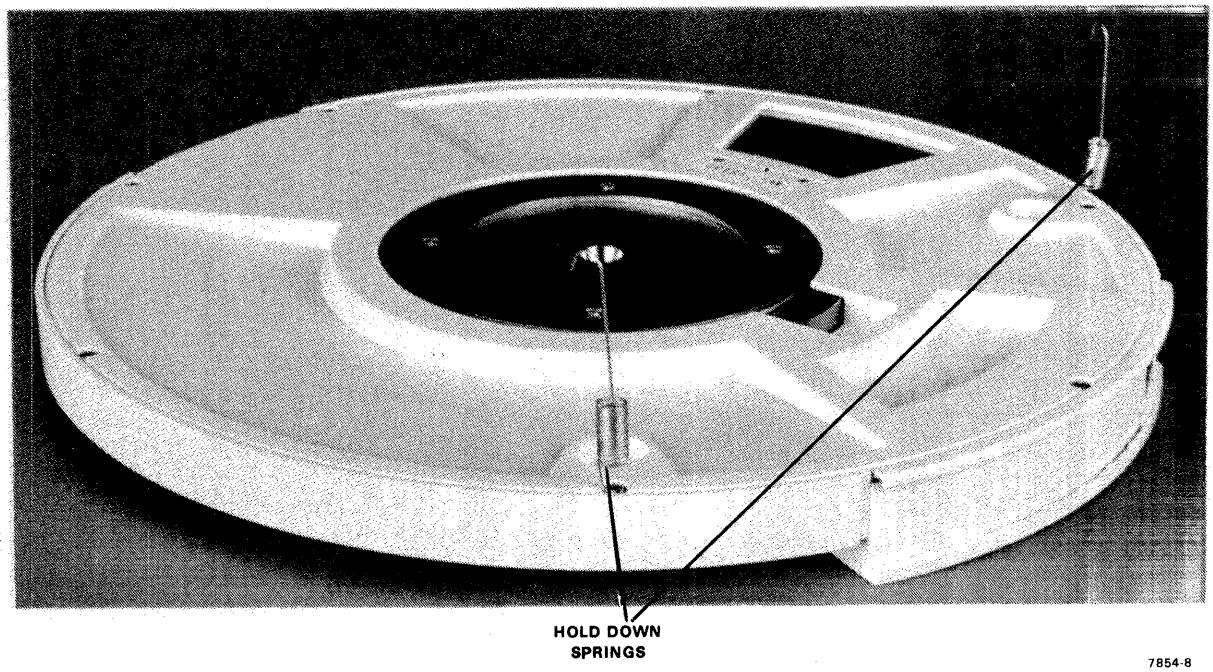


Figure 2-13 RKØ5F Cartridge

Air Supply System

Figure 2-14 shows the air supply system which consists of the prefilter, blower, cooling duct, inlet port, absolute filter, outlet port and air duct.

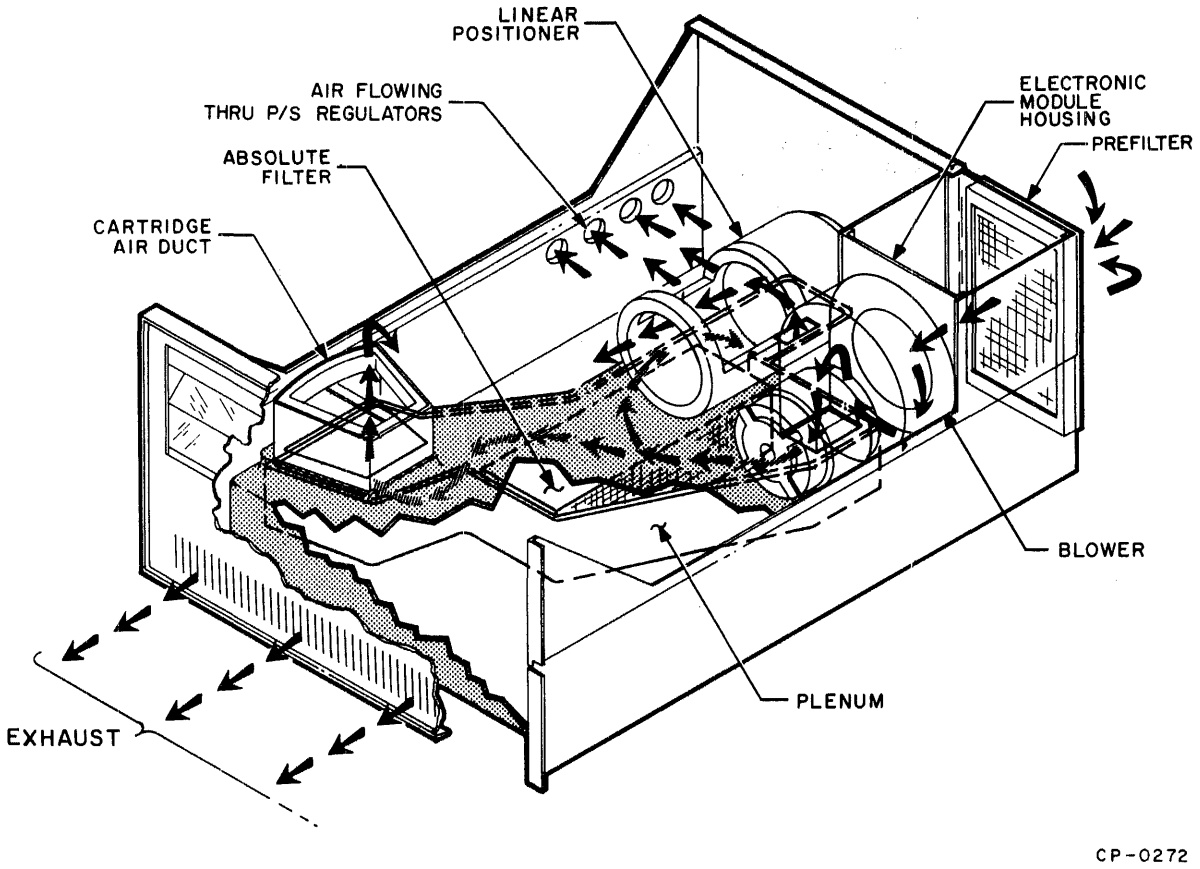


Figure 2-14 Air System

The blower draws unfiltered air through the prefilter, which removes large particles from the air. The filtered air is then drawn across the logic assembly and through the blower. Upon leaving the blower, some of the air is channeled through the cooling duct and directed onto the power supply. The remaining air from the blower is routed via the inlet port into the absolute filter, where minute contamination is removed.

The cleaned air is then routed to the disk cartridge via the filter outlet port and the air duct. This air passes through the disk cartridge, exiting through the access door, and is circulated across the linear positioner and drive baseplate. The air then exits the drive through exhaust louvers in the front panel and in the chassis next to the power supply.

Power Supply

The power supply is located in the left-rear portion of the disk drive. This supply furnishes all dc voltages for the drive. The power supply can operate with a 110-120 or 220-240 Vac, 50 or 60 Hz line voltage input.

Read/Write Heads

Figure 2-15 shows the two ramp-loaded read/write heads used in all of the RK05 drives. One head reads and writes on the top surface of the recording disk, and the other one does the same on the bottom surface. The heads are mounted on suspension arms. Springs connect the suspension arms to the head slider. When there is no cartridge in the drive, the suspension arms rest on a plastic cam block on the duckbill.

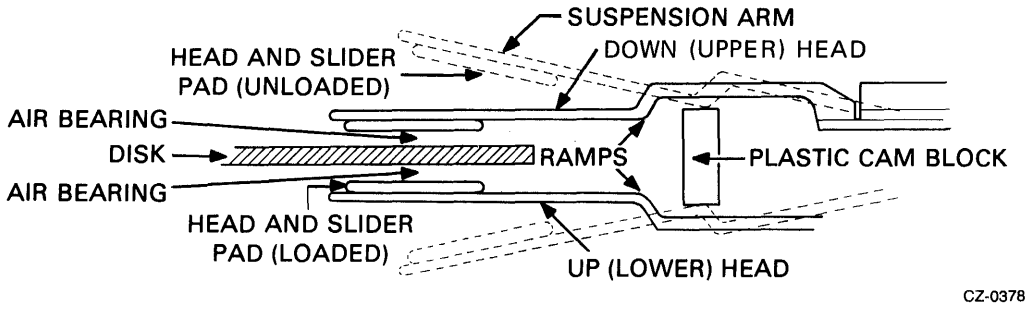


Figure 2-15 Head Loading

When the drive is placed in RUN mode, the positioner moves the heads forward ("loads" the heads) toward cylinder zero. When the entire head slider has passed the edge of the disk, a ramp on the suspension arm slides down the edge of the plastic cam block, allowing the heads to move closer to the disk surface. When completely loaded, the heads "fly" 80 to 100 microinches from the disk surface.

CONTROLS AND INDICATORS

Figure 2-16 shows the controls and indicators used during normal drive operation. They are on the front of the drive cabinet.

Figure 2-16 Controls and Indicators

Table 2-4 gives the function of each switch and indicator on the front panel of the RKØ5, RKØ5J, and RKØ5F Disk Drives.

Table 2-4 Controls and Indicators for the RKØ5, RKØ5J and RKØ5F

Controls and Indicators	Description
RUN/LOAD (rocker switch)	When this switch is placed in the RUN position, the actions listed below occur. 1. The drive locks its front door. 2. The logic enables the drive motor to accelerate the disk to operating speed. 3. The drive turns off the LOAD indicator. 4. The drive enables the logic to load the read/write heads when the disk is at operating speed.
RUN/LOAD (Cont)	When this switch is placed in the LOAD position, the actions listed below are performed. 1. The drive unloads the read/write heads. 2. The disk stops rotating. 3. The drive unlocks its front door when the disk has stopped. 4. The drive lights the load indicator. **CAUTION** **Do not switch to the LOAD position during a write operation. This will result in erroneous data being recorded.**
WT PROT (rocker switch normally off)	When this momentary contact switch is placed in the WT PROT position, the drive lights the WT PROT indicator and prevents a write operation. It also turns off the FAULT indicator, if that is lit. When the switch is depressed a second time, the drive turns off the WT PROT indicator and allows a write operation to occur.
PWR (indicator)	This indicator lights when operating power is present. It goes off when operating power is removed.

Table 2-4 Controls and Indicators for the RKØ5, RKØ5J and RKØ5F (Cont)

Controls and Indicators	Description
RDY (indicator)	This indicator lights when all the conditions listed below have occurred. 1. The disk is rotating at the correct operating speed. 2. The heads are loaded. 3. No other conditions are present to prevent a seek, read, or write operation. The indicator goes off when the RUN/LOAD switch is set to LOAD.
ON CYL (indicator)	This indicator lights when both of the conditions listed below have occurred. • The drive is ready. • The read/write heads are positioned and settled. The indicator goes off during a seek or restore operation.
FAULT (indicator)	This indicator lights when any of the conditions listed below have occurred. • Erase or write current is present without a WRITE GATE. • The linear positioner transducer lamp is out. • Any or all of +15, -15 or +5 Vdc are low. The indicator goes off when the WT PROT switch is pressed, or when the drive is cycled through a RUN/LOAD sequence.
WT PROT (indicator)	This indicator lights when either of the conditions listed below have occurred. 1. The WT PROT switch is pressed. 2. The operating system sends a write protect command.

Table 2-4 Controls and Indicators for the RKØ5, RKØ5J and RKØ5F (Cont)

Controls and Indicators	Description
WT PROT (Cont)	The indicator goes off when the WT PROT switch is pressed a second time, or when the drive is cycled through a RUN/LOAD sequence.
LOAD (indicator)	This indicator lights when the read/write heads are fully retracted and the spindle has stopped rotating. At this point, the cartridge can be removed (if the drive is an RKØ5 or RKØ5J).
WT (indicator)	This indicator lights when a write operation occurs. The indicator goes off when the write operation terminates.
RD (indicator)	Lights when a read operation occurs. Goes off when the read operation terminates.

Figure 2-17 shows a basic block diagram for the drive. The function of each block within the diagram is described below.

- Read/write logic performs reading and writing of data from the disk surface.
- Linear positioner control provides the electromechanical positioning of the read/write heads.
- Control and sequencing logic provides the interface between the drive and controller, decodes the cylinder address information, and sends drive status to the controller.
- Spindle control provides the control for the rotation of the disk.

OTHER DISK DRIVES

Figure 2-18 compares the RKØ5 drives with other DIGITAL disk drives.

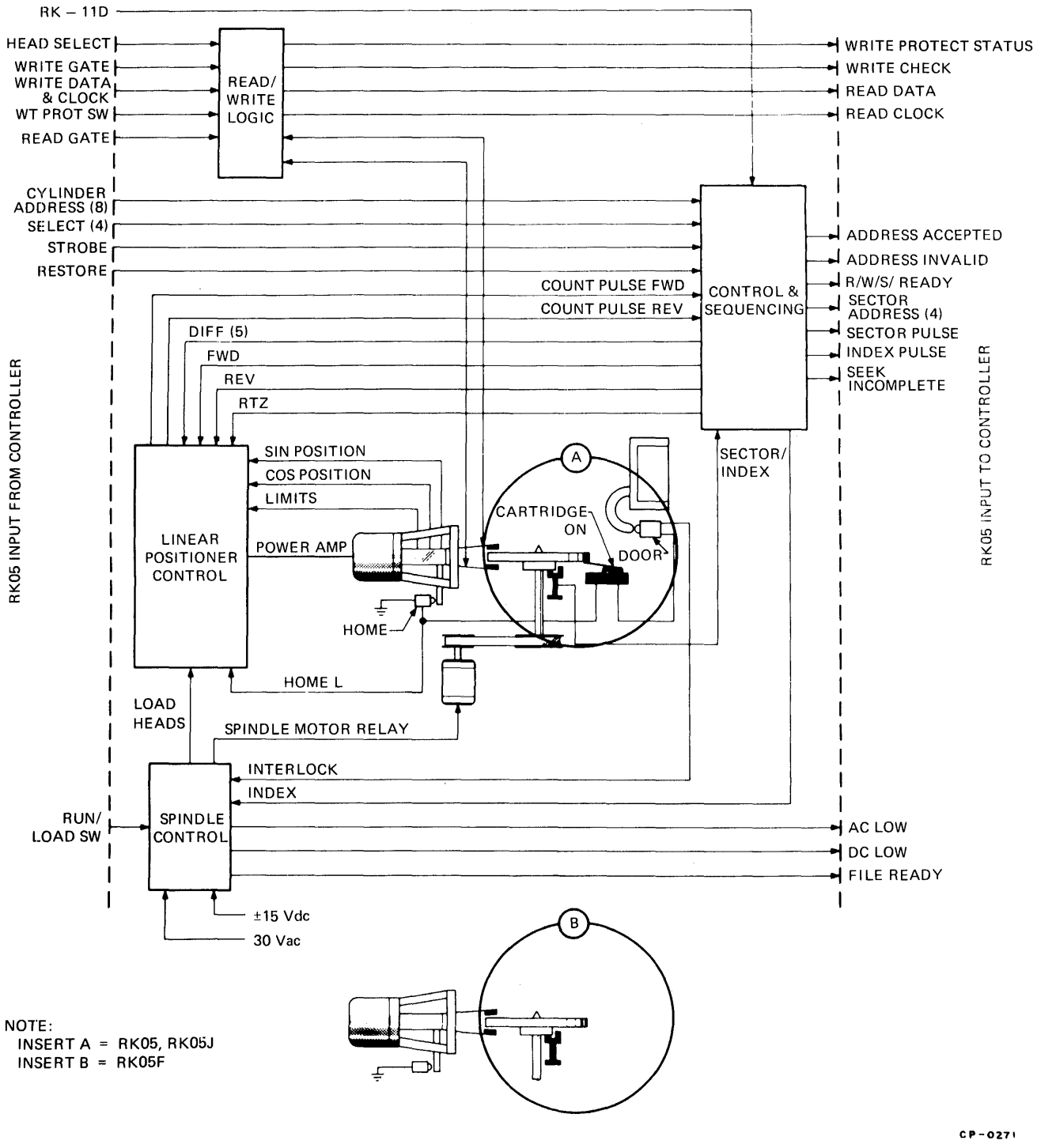


Figure 2-17 RKØ5 Basic Block Diagram

DRIVE	RX01	RX02	RK05 RK05J	RK05F	RK06	RK07	RP02 RPR02	RP02S	RP03	RP04	RP05	RP06	RM02	RM03	RM05	RM80	RL01	RL02
CONT-ROLLER	RX11	RX211	RK11C RK11D RK11E	RK11D RK11E	RK611	→	RP11 RP11-A RP11-E	RP11-A RP11-C	RP11-C	RH11 RH70 RH780	→	→	RH11 RH70 RH780	RH780 RH70	→	RH780	RL11 RLV11	→
MEDIA USED	REMOVABLE IBM DISKETTE	→	IBM 2315-TYPE CARTRIDGE	FIXED CARTRIDGE	RK06-DC CARTRIDGE	RK07-DC CARTRIDGE	IBM 2316 TYPE DISK PACK	→	→	IBM 3336-TYPE DISK PACK	→	IBM 3336-11-TYPE DISK PACK	CDC 9876 DISK PACK	→	CDC 883-91 DISK PACK	FIXED HDA	RL01-K CARTRIDGE	RL02-K CARTRIDGE
CAPACITY OF ONE DRIVE	256 KB	512KB	2.4 MB	4.8 MB	14 MB	26MB	20MB	→	40MB	88MB	→	174 MB	67MB	→	256 MB	124 MB	5MB	10MB
VENDOR NAME	CALCOMP	→	DIGITAL	→	→	→	MEMOREX (660-1)	ISS (714 DEC)	ISS (715 DEC)	ISS (733 DEC)	MEMOREX (677-51)	MEMOREX (677-01)	CONTROL DATA (BK585-G16)	→	CONTROL DATA (BK7B1-E1F)	DIGITAL	HERTRICH DEVELOPMENT AND DIGITAL	→
MAX # DRIVES/ CONTROL	2	→	8	3 PHYSICAL UNITS, 8 LOGICAL	8	→	→	→	→	→	→	→	→	→	→	→	4	→
# BYTES PER SECTOR	128	→	512	→	→	→	→	→	→	→	→	→	→	→	→	→	256	→
# SECTORS PER TRACK	26	→	12	→	22	→	10	→	→	22	→	→	32	→	→	31	40	→
# TRACKS PER SURFACE	77	→	203	406	411	815	203	→	→	411	→	815	823	→	→	1118	256	512
# DATA SURFACES	1	2	→	→	3	→	20	→	→	19	→	→	5	→	19	7	2	→
BIT CELL TIME	4μS	→	880NS	→	232NS	→	400NS	→	→	156NS	→	→	155NS	103NS	→	→	244NS	→
BYTE XFER RATE	18μS	→	5.55μS	→	1.96μS	→	3.7μS	→	→	1.25μS	→	→	1.25μS	.825μS	→	→	1.96μS	→
MAX ACCESS TIME	1000MS	→	85MS	→	67MS	→	60MS	55MS	→	52MS	53MS	→	56MS	→	→	50MS	100MS	→
MAX BIT DENSITY	3200 BPI	→	2200 BPI	→	4040 BPI	→	2200 BPI	→	→	4040 BPI	→	→	6000 BPI	→	→	6339 BPI	3725 BPI	→
ENCODING METHOD	FM	MODIFIED MFM	FM	→	MFM	→	FM	→	→	MFM	→	→	MFM	→	→	→	→	→
SERVO TRACKS USED	SOFT SECTOR	→	NONE	→	TRACK FOLLOWING SERVO	→	NONE	→	→	TRACK FOLLOWING SERVO	→	→	→	→	→	→	IMBEDDED SERVO	→
MOTOR SPEED	360 R/MIN	→	1500 R/MIN	→	2400 R/MIN	→	→	→	→	3600 R/MIN	→	→	2400 R/MIN	3600 R/MIN	→	→	2400 R/MIN	→
TYPE OF POSITIONING SYSTEM	STEPPING MOTOR; ELECTRONIC DETENT	→	LINEAR MOTOR, ELECTRONIC DETENT	→	→	→	LINEAR MOTOR, MECHANICAL DETENT	LINEAR MOTOR ELECTRONIC DETENT	→	→	→	→	→	→	→	ROTARY POSITIONER, ELECTRONIC DETENT	DC MOTOR, ELECTRONIC DETENT	→

CZ-3043

Figure 2-18 PDP-11 Disk Drive Comparison Chart

INTRODUCTION/PHYSICAL DESCRIPTION

SUMMARY

The RKØ5 Disk Drive is used with both the 11-family and 8-family processors.

The RK11D/E Controller can control up to eight RKØ5 Drives.

- Can be eight RKØ5 or RKØ5J Drives
- Can be a combination of RKØ5, RKØ5J and RKØ5F Drives

The RK11D/E Controller can be used with PDP-11 or PDP-15 computer systems.

- RK11D is used to transfer 16-bit data words (PDP-11)
- RK11E is used to transfer 18-bit data words (PDP-15)
- Jumpers determine if the controller is an RK11D or RK11E

The RK11D/E consists of four modules.

- M7254 - status control
- M7255 - disk control
- M7256 - data paths
- M7257 - bus control

The RK8-E Controller can control up to four RKØ5 Drives.

- Can be four RKØ5 or RKØ5J Drives
- Can be a combination of RKØ5, RKØ5J and RKØ5F Drives

The RK8-E Controller consists of three modules.

- M71Ø4 - data buffer and status
- M71Ø5 - major registers
- M71Ø6 - control logic

The RKØ5 family of disk drives consists of the RKØ5, RKØ5J and RKØ5F Drives.

- Compact, single-platter disk drives
- RKØ5 and RKØ5J use removable disk cartridges
  - 12 sector cartridge (PDP-11 or PDP-15 processors)
  - 16 sector cartridge (PDP-8 processor system)
  - 4Ø6 data tracks - 2Ø3 with each head
- RKØ5F uses a non-removable disk cartridge
  - Cartridge fixed in RKØ5F - held in place with two springs
  - 812 data tracks - 4Ø6 with each head
  - Physically, one drive but is addressed as two drives
  - Drive select switch must be set to an even-number; i.e., Ø, 2, 4 or 6 - for example, drive number "2" is recognized by the software as logical units "2" AND "3"

There are several major assemblies in an RKØ5 Drive.

- Linear positioner moves the read/write heads to desired position on disk surface.
- Spindle and drive motor rotate the disk platter.
- Cartridge handling system guides the cartridge into position inside the drive (RKØ5 and RKØ5J Drives only).
- Logic assembly contains the logic for reading, writing, positioning and interface cabling.
- Air system filters the external air.
- Power supply provides dc voltages for the drive.
- Read/write heads read and write data from the disk.
- Front panel controls the drive and displays drive operational status.

Now that you have finished this module, take the module test. The course administrator has the answers to the test.

RKØ5 DISK SUBSYSTEM MAINTENANCE

RK11 Subsystem Registers/Commands

RK11 SUBSYSTEM REGISTERS/COMMANDS

INTRODUCTION

The RK11 Controller is the interface between a PDP-11 processor and an RKØ5 Disk Drive. Like any other peripheral device, the drive must be able to communicate with the processor. The RK11 performs this communication with the registers and commands described in this module.

The topics covered in this module are listed below.

- Register use and bit definition
- Command categories
- Command functions
- Data format

While studying this module, don't try to memorize what each bit in every register does. Instead, learn the function of each register, and see which registers are used to control the various commands the subsystem can perform.

OBJECTIVES

At the completion of this module, you will be able to perform the tasks listed below.

- Complete a partially written program designed to transfer data to and from the drive
- Define the function of each register
- Define the commands the device can execute

To demonstrate your ability to perform these tasks, you will be asked to perform the exercises listed below.

- Given a short program write in the remarks as to what each instruction is doing. Time allowed to complete this exercise is 2Ø minutes.
- Given a list of both registers and commands and a list of their definitions, match the registers and commands with the proper definition. You must match 1Ø out of the 12 possible definitions within 1Ø minutes.

You may use any reference material you have available.

OPTIONAL RESOURCES

PDP11 Processor Handbook	EB-17716
RK11D/E Moving Head Disk Drive Controller Manual	EK-RK11D-MM-002

REQUIRED RESOURCES

PDP-11 Subsystem Register Quick Reference Card	EH-18955
PDP-11 Programming Card	

RK11 SUBSYSTEM REGISTERS/COMMANDS

INTRODUCTION

The RK11 Controller (either the RK11D or the RK11E) contains seven 16-bit programmable registers. These registers are addressed via the UNIBUS. They provide the software interface between the RK11 and the host CPU. Table 3-1 lists these registers and their addresses.

Table 3-1 RK11 Registers

Name	Abbreviation	Address
Drive status register	RKDS	777400
Error register	RKER	777402
Control status register	RKCS	777404
Word count register	RKWC	777406
Bus address register (Current memory address)	RKBA	777410
Disk address register	RKDA	777412
Data buffer register	RKDB	777416

REGISTER DESCRIPTIONS

All RK11 software control is accomplished by the seven device registers listed in Table 3-1. These registers are assigned UNIBUS addresses and can be read or written into (except as noted) using instructions that refer to the respective register addresses.

The seven device registers, their UNIBUS addresses and their bit assignments are described below. Note that unassigned and write-only bits are always read as zeros. Also, any attempt to manipulate an unassigned or read-only bit will not affect the bit. Finally, the INIT signal refers to the initialization signal issued by the processor.

Drive Status Register (RKDS) (777400)

This register is shown in Figure 3-1, and is described below in Table 3-2.

NOTE

This register is a read-only register, and contains the status of the selected drive, including the current sector address.

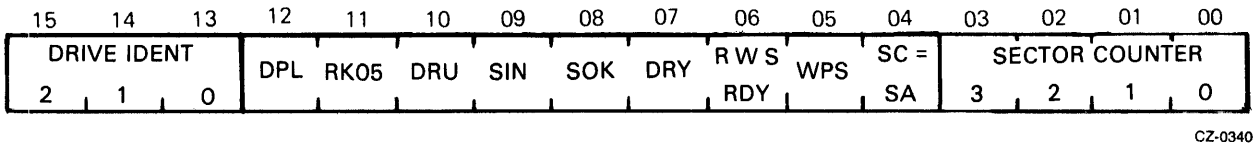


Figure 3-1 Drive Status Register

Table 3-2 Drive Status Register

Bit(s)	Name	Description and Operation
ØØ-Ø3	Sector counter (SC)	Indicates the current sector address of the selected drive. Sector address ØØ is defined as the sector following the index pulse.
Ø4	Sector counter equals sector address (SC=SA)	Indicates that the disk heads are positioned over the address that is currently in the sector address register.
Ø5	Write protect status (WPS)	Indicates the selected drive is write protected.
Ø6	Read/write/seek ready (R/W/S/RDY)	Indicates that the selected drive positioner is not moving, and that the drive is ready to accept a new command.
Ø7	Drive ready (DRY)	Indicates that the selected drive has met the conditions listed below. • The drive is properly supplied with power. • The drive is loaded with a disk cartridge. • The cartridge access door is closed. • The LOAD/RUN switch is set to RUN. • The disk is rotating at proper speed. • The heads are loaded. • Bit 1Ø of RKDS is cleared, indicating the drive has no unsafe conditions.
Ø8	Sector counter OK (SOK)	Indicates that the current sector address of the selected drive (bits ØØ-Ø3) is not in the process of changing and can be used for determining the present sector location of the heads.

Table 3-2 Drive Status Register (Cont)

Bit(s)	Name	Description and Operation
Ø9	Seek incomplete (SIN)	Indicates that a seek command did not complete, due to some malfunction.
1Ø	Drive unsafe (DRU)	Indicates that an unusual condition has occurred in the disk drive, and the drive cannot properly perform any operations. Drive unsafe turns on the FAULT lamp on the drive front panel. The faults that cause this are listed below. • Erase or write current without write gate • Linear positioner transducer lamp burned out • Any or all of +15, -15, or +5 Vdc low
11	RKØ5 disk on line (RKØ5)	Indicates that the selected disk drive is an RKØ5.
12	Drive power low (DPL)	Indicates that there is a loss of power to one of the disk drives.
13-15	Identification of drive (ID)	Indicates to the software the drive that caused the interrupt.

Error Register (RKER) (777402)

This register is shown in Figure 3-2, and is described below in Table 3-3.

NOTE
This is a read-only register and indicates all subsystem errors.

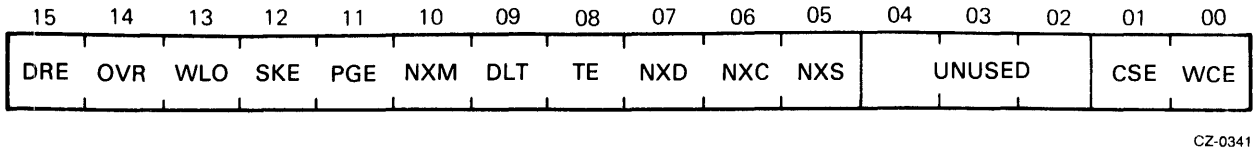


Figure 3-2 Error Register

Table 3-3 Error Register

Bit(s)	Name	Description and Operation
ØØ	Write check error (WCE)	Indicates that an error was encountered during a write check function as a result of a faulty bit comparison between disk data and memory data.
Ø1	Checksum error (CSE)	Indicates a faulty recalculation of the checksum, while performing a read or read check command.
Ø2-Ø4	Unused	
Ø5	Nonexistent sector (NXS)	Indicates that an attempt was made to initiate a transfer to a sector address larger than 13 (octal).
Ø6	Nonexistent cylinder (NXC)	Indicates that an attempt was made to initiate a transfer to a cylinder address larger than 312 (octal).
Ø7	Nonexistent disk (NXD)	Indicates that an attempt was made to initiate a function on a nonexistent drive.
Ø8	Timing error (TE)	Indicates that no timing pulses have been detected for at least five microseconds. The timing pulses could be from the crystal oscillator in the controller (during a write data command), or the read clock from the disk drive read circuits (during a read data command).
Ø9	Data late (DLT)	Indicates that an error occurred during one of the three commands listed below. • Write or write check - the output buffer of the four word file emptied, failing to supply a word to the disk. If this occurs, the disk will attempt to remove a word from an empty file.

Table 3-3 Error Register (Cont)

Bit(s)	Name	Description and Operation
Ø9 (cont)	Data late	• Read - The input buffer of the four word file filled, indicating the UNIBUS is unable to move words to memory fast enough. If this occurs, the disk will attempt to read another word into an already full file.
1Ø	Nonexistent memory (NXM)	Indicates that MSYN was transmitted and that memory did not respond with a SSYN within the allotted time of 2Ø microseconds.
11	Programming error (PGE)	Indicates that bit 1Ø of the RKCS register (format) was set while initiating a function other than read or write.
12	Seek error (SKE)	Indicates that the positioner was not over the correct cylinder while executing a read, write, read check, or write check command.
13	Write lockout violation (WLO)	Indicates that an attempt was made to write on a disk which is write-protected (bit 5 of RKDS is set).
14	Overrun (OVR)	Indicates that, during any data transfer command, the word count has not yet overflowed, and that the last sector of the last cylinder on surface 1 has been accessed.
15	Drive error (DRE)	Indicates that one of the drives in the system senses a loss of either ac or dc power, and a function is either initiated or in process.

NOTE
Bits Ø5 through 15 of the RKER indicate hard errors, and can only be cleared by a BUS INIT or a control reset function.

Control Status Register (RKCS) (777404)

This register is shown in Figure 3-3, and is described below in Table 3-4.

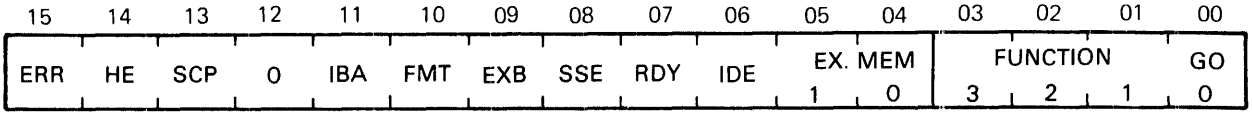


Figure 3-3 Control Status Register

Table 3-4 Control Status Register

Bit(s)	Name	Description and Operation
00	GO (write-only)	Indicates that the device is to initiate the command that is specified by the function code in bits 1, 2 and 3 of this register.
01-03	Function (read/write)	Indicates the function (command) to be performed by the device. The binary coding for each function is listed below. **Function Bit 3 / Bit 2 / Bit 1 / Go / Command** 0 0 0 1 Control reset 0 0 1 1 Write 0 1 0 1 Read 0 1 1 1 Write check 1 0 0 1 Seek 1 0 1 1 Read check 1 1 0 1 Drive reset 1 1 1 1 Write lock
04, 05	Memory extension (MEX) (r/w)	Indicates use of extended bus addressing. This device is capable of using memory addresses of up to 18 bits.

Table 3-4 Control Status Register (Cont)

Bit(s)	Name	Description and Operation
Ø6	Interrupt on done enable (IDE) (r/w)	Indicates that the device is to issue a bus request and interrupt to vector address 22Ø for any of the reasons listed below. • A command is completed • A hard error is encountered • A soft error is encountered and bit Ø8 of the RKCS (SSE) is set • RKCS Ø7 (RDY) is set and GO is not set
Ø7	Control ready (RDY) (read-only)	Indicates that the RK11 Controller is ready to perform a function (i.e., controller is not busy).
Ø8	Stop on soft error (SSE) (r/w)	Commands the logic to take one of the two courses of action listed below when a soft error is encountered. • All control action will stop at the end of the current sector if RKCS Ø6 (IDE) is reset. • All control action will stop and a bus request will occur at the end of the current sector if RKCS Ø6 (IDE) is set.
Ø9	Extra bit (EXB)	This bit is unused.
1Ø	Format (FMT) (r/w)	Commands the controller logic to take one of the two courses of action listed below, depending upon the function code found in RKCS bits 1, 2 and 3. • Write - formats a disk cartridge. Used to recreate the headers on any or all disk sectors.

Table 3-4 Control Status Register (Cont)

Bit(s)	Name	Description and Operation
		• Read - reads header words and transfers them to memory. No data out of the data field of any sector is sent to memory in this mode of operation.
11	Inhibit incrementing the RKBA (IBA) (r/w)	Inhibits the RKBA from incrementing during normal data transfer commands.
12	Unused	
13	Search complete (SCP) (SCP) (r/w)	Indicates that the previous interrupt was the result of a seek or drive reset command.
14	Hard error (HE) (read-only)	Indicates that any of the error register bits Ø5-15 are set.
15	Error (ERR) (read-only)	Indicates that any of the error register bits are set.

Word Count Register (RKWC) (777406)

This register is shown in Figure 3-4, and is described below in Table 3-5.

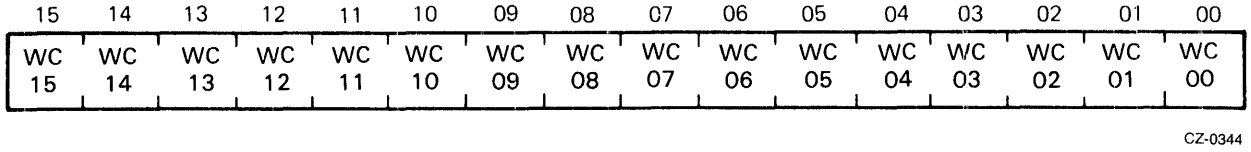


Figure 3-4 Word Count Register

Table 3-5 Word Count Register

Bit(s)	Name	Description and Operation
Ø0-15	WCØØ-WC15 (r/w)	Contains the 2's complement of the total number of words to be transferred by a data transfer command. This register is incremented after each word transfer.

Current Bus Address Register (RKBA) (777410)

This register is shown in Figure 3-5, and is described below in Table 3-6.

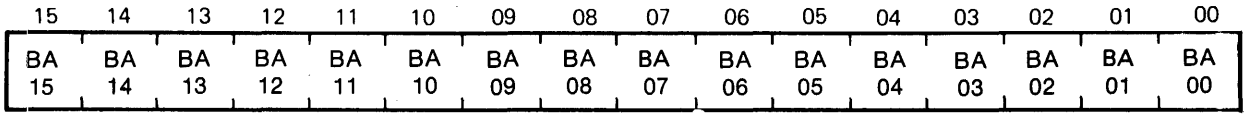


Figure 3-5 Current Bus Address Register

Table 3-6 Current Bus Address Register

Bit(s)	Name	Description and Operation
00-15	BA00-BA15 (r/w)	Contains the UNIBUS memory address to or from which data will be transferred. This register is incremented at the end of each transfer, unless bit 11 of the control status register is set. If the system has extended memory, the RKBA will overflow to the EX MEM (bits 04 and 05 of the RKCS) to reflect the extended bus addresses.

Disk Address Register (RKDA) (777412)

This register is shown in Figure 3-6, and is described below in Table 3-7.

NOTE

This register will not respond to commands while the controller is busy. Therefore, RKDA bits are loaded from the bus data lines only in the control ready state (RDY - bit 07 of the RKCS), and are cleared by BUS INIT and control reset. The RKDA is incremented automatically at the end of each disk sector.

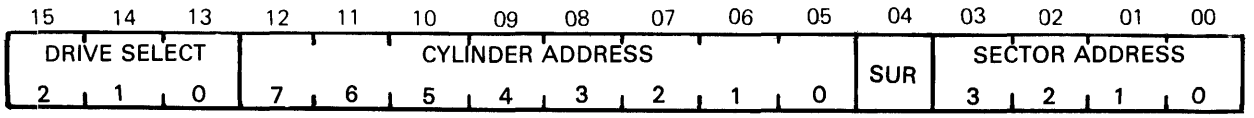


Figure 3-6 Disk Address Register

Table 3-7 Disk Address Register

Bit(s)	Name	Description and Operation
ØØ-Ø3	Sector address (SA) (r/w)	Binary representation of the disk sector to be addressed for the next function.
Ø4	Surface (SUR) (r/w)	When set, head Ø is selected. When cleared, head 1 is selected.
Ø5-12	Cylinder address (CYL ADDR) (r/w)	Binary representation of the cylinder address currently being selected. The largest valid cylinder address is 312 (octal).
13-15	Drive select (DR SEL) (r/w)	Binary representation of the logical drive number currently being selected.

Data Buffer Register (RKDB) (777416)

This register is shown in Figure 3-7, and is described below in Table 3-8.

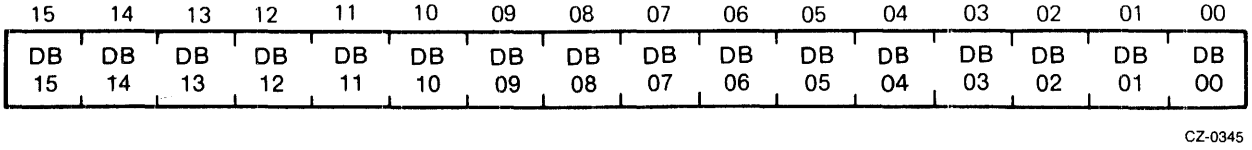


Figure 3-7 Data Buffer Register

Table 3-8 Data Buffer Register

Bit(s)	Name	Description and Operation
ØØ-15	DBØØ-DB15 (read only)	The data buffer register serves the three functions listed below. • In NPR write data transfers, the data buffer serializes the data word for transmission to the drive. • In NPR read data transfers, the data buffer contains the word to be transferred to memory. • In diagnostic testing, the output of the four-word file can be checked with a MOV instruction.

These seven progammable registers not only give status and error indication, but, when properly programmed, they allow the drive to perform the eight functions or commands the device is capable of executing. These functions and commands are divided into the two categories listed below.

- Control functions
- Data transfer functions

CONTROL FUNCTIONS

Through software control, the RK11 can perform the four control functions listed below.

- Control reset
- Seek
- Drive reset
- Write lock

Control Reset

This function initializes all internal registers and clears most of the bits in the seven programmable registers. The exceptions are bit 7 of RKCS (READY), which sets, and bits Ø1 through 11 of RKDS, which are not affected.

Seek Command

This command directs the selected disk drive to move its positioner to the cylinder address specified by bits Ø5 through 12 of RKDA. After directing the drive to seek, the controller returns to the ready state (RKCS bit Ø7 is set) so that other commands may be performed.

The selected drive completes the seek by moving its positioner to the desired cylinder. Then, the controller sets bit Ø6 of RKDS (R/W/S RDY).

Drive Reset Command

This command directs the selected disk drive to move its positioner to cylinder address ØØØ and to reset all active errors. The RK11 performs this command in the same manner as a seek command.

Write Lock Command

This command write-protects a selected disk drive until the condition is overridden by operation of the write protect (WT PROT) switch on the front panel of the drive. The drive is automatically write-enabled when power is first applied, or when the disk drive RUN/LOAD switch is set to RUN.

DATA TRANSFER FUNCTIONS

In addition to the four control functions, the RK11 can perform the four data transfer functions listed below.

- Write
- Read
- Write check
- Read check

Write Command

This command causes data to be written on the disk cartridge, starting with the sector specified in the disk address register (RKDA). First, the controller commands the drive to perform a normal seek (if necessary). When the seek is completed, the next available header word is read to verify the location of the positioner. If the header is correct, the controller begins the write operation when the sector count (bits ØØ through Ø3 of the RKDS) equals the sector address (RKDS bits ØØ through Ø3), referred to as SC=SA.

Read Command

This command causes data to be read from the disk cartridge with the sector specified in the disk address register (RKDA). First, the controller commands the drive to perform a normal seek (if necessary). When the seek is completed, the controller waits for SC=SA. The controller then reads and checks the header word. If the cylinder address is correct, the controller continues reading the sector and transfers the data words to memory.

Write Check Command

This command compares the contents of memory to the contents of a continuous block of data on the cartridge. The controller first performs a seek and then reads and checks the next available header word. If the cylinder address is correct, the controller waits for SC=SA, then begins reading the rest of the sector (data and checksum). Each data word from the disk drive is compared, bit by bit, with memory data from the UNIBUS. The disk drive checksum, in turn, is compared with the checksum calculated by the controller.

If any bit is found to be in error, RKER bit ØØ (write check error) is set. Controller reaction depends on bit Ø6 of RKCS (IDE) and bit Ø8 of RKCS (SSE).

The write check function may be performed on a short sector (less than 256 data words) as long as the number of words checked is equal to the number of words previously written into the sector.

Read Check Command

This command causes the drive to read data from the disk so the controller can calculate the checksum and compare it to the checksum read from the disk. No NPRs occur during this command. This command allows the software to determine if a given block of data is readable and error free.

You have seen that the RK11 can execute any of eight different commands using seven registers. When the RK11 executes any of the four data transfer commands, the data on the disk pack is written or read in a certain format. This format is identical for all sectors on all cylinders.

SECTOR FORMAT

Data is stored on the disk cartridge in groups of 12 sectors per track for both the 16-bit (RK11D) and 18-bit (RK11E) controllers. Each sector contains 256 data words, and each sector is defined by a sector mark. The five basic segments of each sector are listed below.

- Preamble
- Header
- Data
- Checksum
- Postamble

Each of these sector segments corresponds to a logic "major state".

Figure 3-8 shows the sector format.

PREAMBLE	SYNC BIT	HEADER	DATA	CHECKSUM	POSTAMBLE
13_{10} (15_8) WORDS OF ZEROS	1	CYLINDER ADDRESS (1 WORD)	256_{10} (400_8) WORDS (16-BIT OR 18-BIT)	SECTOR CHECKSUM (1 WORD)	1 WORD OF ZEROS

CZ-0347

Figure 3-8 Sector Format

The preamble and postamble areas of a sector serve as boundaries before and after the information major states (header, data, and checksum).

Preamble

This sector area consists of 15 (octal) 16-bit words of zeros, to allow adequate time for RD GATE to turn on during a known zero data field. The read logic then waits for the first one bit to occur (sync bit), and begins to read at the first bit of the header word. For a write function, the hardware writes the 15 (octal) words of zeros and then the sync bit.

There is a 5.8 microsecond gap between the sensing of the sector mark and the actual start of the preamble. This gap is caused by the write amps being turned on without any data to write. The controller logic allows time for the write current to stabilize and then starts writing the preamble.

Sync Bit

This part of the sector consists of a single one bit following the all-zero preamble. Its purpose is to synchronize the logic major state register and counting circuits to the sector being read. When the sync bit is read, the logic knows that the next bit that follows is the start of the header.

Header

This sector area consists of a single 16-bit word containing the actual cylinder address. Before a data transfer function is performed, the header word is read and checked against the cylinder address portion of the RKDA (bits Ø5-12, desired cylinder address) to ensure that the heads are at the proper cylinder. The write function rewrites the header each time data is written on a sector using the cylinder address in the RKDA.

Data

This is the area of the sector that contains the actual user information. The data area consists of 256 (decimal) data words. These words are 16 bits long when written by an RK11D, and 18 bits long when written by an RK11E.

Short portions (less than 256 data words) of a sector may be read or written as determined by the word count. When a short sector is written, logic in the controller automatically writes the remainder of the sector with zeros. The write check function may be performed on a short sector as long as the number of words write-checked is equal to the number of words previously written into the sector.

Checksum

This area of the sector consists of a single 16-bit word that is the checksum of all 256 data words. The controller compares this checksum to the controller-calculated checksum whenever a write check, read, or read check function is performed on a sector. For a write function, the controller calculates the checksum from the words being written and appends it to the sector following the last data word. The checksum is created by serially adding each bit of a sector as it is transferred to the disk for writing.

Postamble

This sector area consists of a single 16-bit word of zeros used as a buffer area following the checksum. This area exists so that write current can be turned off without affecting any data.

There is an area following the postamble that contains no written information. This tolerance gap allows for timing differences in spindle motor speeds and the physical sector length differences between the RK11D and RK11E Controllers (16-bit words versus 18-bit words).

As you learn about other DIGITAL disk drives you will learn that the sector formats are different from drive family to drive family. The data format just described is for RKØ5 drives only.

SUMMARY

The RK11 contains seven programmable registers.

- **RKDS (drive status)** contains the selected drive status and current sector address.
- **RKER (error register)** contains error indications for the subsystem.
- **RKCS (control and status)** contains the function code and GO bit which allow the subsystem to execute the desired command, and contains other information as well.
- **RKWC (word count)** contains the number of words to be transferred in 2's complement form.
- **RKBA (bus address)** contains the bus (memory) address to or from which data is to be transferred.
- **RKDA (disk address)** contains the sector address, surface number, cylinder address, and drive number for the selected drive.
- **RKDB (data buffer)** is used in three functions.
  - Serializes data for the drive when writing.
  - Holds the data to be transferred to memory when reading.
  - Tests the data transfer integrity of the four-word file in the RK11D during diagnostic testing.

The RK11 performs four control and four data transfer functions.

- Control functions
  - **Control reset** initializes all internal registers and clears five of the seven programmable registers.

- **Seek** directs the drive to move its heads to the cylinder address specified by bits Ø5 through 12 of the RKDA register.
- **Drive reset** directs the drive to move its heads to cylinder zero, and resets all drive errors.
- **Write lock** write protects a selected drive until the condition of the write protect switch on the front panel is changed.

- Data transfer functions
  - **Write** causes data to be written on the disk cartridge starting with the sector specified by the disk address register.
  - **Read** causes data to be read from the disk cartridge starting with the sector specified by the disk address register.
  - **Write check** compares the data stored in memory with the contents of a written block of data from the disk (comparison is performed in the controller).
  - **Read check** causes data to be read from the disk so that the checksum can be checked (used to inform the program if a given block of data is readable and error-free).

An RKØ5 sector is divided into five sections.

- **Preamble** consists of 15 octal words of zeros used to ensure that read gate will turn on in a known area. A logic one bit follows the 15 words of zeros and is called the sync bit. The sync bit is used to synchronize the controller logic to the start of the header.
- **Header** consists of a 16-bit word containing the cylinder address.
- **Data** consists of 256 decimal words of data (16-bit words for RK11D and 18-bit words for RK11E).
- **Checksum** consists of a 16-bit word which is the checksum of all the words in the data area of the sector.
- **Postamble** consists of one zero-filled word where write current is turned off.

RK11 SUBSYSTEM REGISTERS/COMMANDS

MODULE EXERCISE

Using the program listed below, write in the remarks column what each instruction is doing. You may only use your PDP-11 programming card as a reference. You have 20 minutes to successfully complete this exercise.

Memory Location	Instruction	Remarks
1000	012737	move 177770 to address 177406
1002	177770	
1004	177406	
1006	012737	move 3000 to address 177410
1010	003000	
1012	177410	
1014	012737	move 10000 to address 177412
1016	010000	
1020	177412	
1022	012737	move 4003 to address 177404
1024	004003	
1026	177404	
1030	105737	test Byte of address 177404
1032	177404	
1034	100375	branch to 1030
1036	012737	move 177770 to address 177406
1040	177770	
1042	177406	
1044	012737	move 4000 to address 177410
1046	004000	
1050	177410	
1052	012737	move 10000 to address 177412
1054	010000	
1056	177412	
1060	012237	move what is in R2 and +1 to 177404
1062	000005	
1064	177404	
1066	000000	HALT
3000	052525	BIS
4000	000000	
4002	000000	
4004	000000	HALT
4006	000000	
4010	000000	
4012	000000	
4014	000000	
4016	000000	
4020	000000	
4022	000000	

MODULE EXERCISE SOLUTIONS

Memory Location	Instruction	Remarks
1000	012737	Set up word count
1002	177770	2's complement operand
1004	177406	Word count register address
1006	012737	Set up bus address
1010	003000	Starting memory location
1012	177410	Bus address register address
1014	012737	Set up disk address
1016	010000	Operand
1020	177412	Disk address register address
1022	012737	Set up control and status for
1024	004003	write and bus address incre-
1026	177404	ment inhibit
1030	105737	TSTB for ready
1032	177404	CSR
1034	100375	Branch to location 1030
1036	012737	Set up word count
1040	177770	2's complement operand
1042	177406	Word count register address
1044	012737	Set up bus address
1046	004000	Memory location for read data
1050	177410	Bus address register address
1052	012737	Set up disk address
1054	010000	Disk address operand
1056	177412	Disk address register address
1060	012737	Set up control and status for
1062	000005	read command
1064	177404	CSR address
1066	000000	Halt
3000	052525	Set up memory location 3000 with data to be used
4000	000000	Clear out memory locations
4002	000000	4000 through 4022 so they can
4004	000000	be used by the program to hold
4006	000000	data read from the disk
4010	000000	
4012	000000	
4014	000000	
4016	000000	
4020	000000	
4022	000000	

Now that you have completed the module exercise you may take the module test. The course administrator has the answers to the test.

RKØ5 DISK SUBSYSTEM MAINTENANCE

RK11D/E Theory of Operation

RK11D/E THEORY OF OPERATION

INTRODUCTION

In the previous module, you studied the registers in the RK11D/E Controller and learned what functions the subsystem can execute. Now you will use this information to learn how the controller itself works.

This module describes the theory of operation of the RK11D/E Controller. With the aid of block diagrams, this module describes the logic in the RK11D/E. The overall block diagram shows the major circuits on each circuit module. Each major circuit is described in terms of the function it performs. In addition, there are three block diagrams which show the various data paths taken for write, read, and write check commands.

Each block within a diagram contains a mnemonic which references a page of logic in the field maintenance print set. This way, you may correlate the circuit elements on a block diagram to a print set diagram, if you wish to do so.

OBJECTIVES

At the completion of this module, you will be able to perform the tasks listed below.

- Trace the portions of RK11D/E logic that is used during execution of each of the commands listed below.
  - Command initiation
  - Write
  - Read
  - Write check
- Describe the function of the major logic circuits in the overall controller block diagram.

To demonstrate your ability to meet these objectives, you will be given a module test where you will be required to match each logic circuit block with its definition. You must correctly match 8 out of 10 logic circuits with their definitions within 10 minutes. The second part of the module test will require you to use supplied diagrams to shade in the logic circuits used for each type of data path.

ADDITIONAL RESOURCES

RK11D/E Moving Head Disk Drive Controller Manual EK-RK11D-MM-002
RK11D/E Print Set

RK11D/E CONTROLLER

The RK11D/E Controller consists of the four modules listed below.

- M7254 status control (ST)
- M7255 disk control (DK)
- M7256 data paths (DA)
- M7257 bus control (BS)

Figure 4-1 is a simplified overall block diagram that shows the major circuits and on which module they reside. Use this figure as a reference while reading the following text. The RKDA is the only logic circuit represented that is not shown on the proper module.

M7254 STATUS CONTROL

The status control module (ST) initiates the programmable functions (read, write, etc.) of the controller and monitors logic status by means of the control status (RKCS), word count (RKWC) and error (RKER) registers.

RKCS Register

The RKCS register is loaded, from the processor, via the UNIBUS D lines with three bits (FØ-F2) representing the function code to be performed. This function is decoded and applied to the appropriate logic for execution. The software can also define to the logic whether or not the read or write command is to be a special format.

RKWC Register

The RKWC register is loaded, from the processor, via the UNIBUS D lines with the 2's complement of the number of data words to be transferred. Each time a word is transferred to or from the disk, this register is incremented with the signal Ø -> NPR.

RKER Register

The RKER register contains information on any errors that occur during the execution of an RK11 function. The output of RKER is multiplexed with the output of RKCS, RKWC and the drive status register (RKDS on the data paths module). This multiplexer is described in the next paragraph.

Four-To-One Multiplexer

This multiplexer takes the inputs from the RKCS, RKWC, RKER and RKDS registers and selects one for transmission on the internal bus A. Internal bus A is multiplexed with the output of a four-to-one multiplexer on the data paths module. This output is sent over the UNIBUS via the D lines to memory. The register decoding on the bus control module produces enabling signals for the multiplexer to determine which input (RKCS, RKWC, RKER or RKDS) is sent to memory via the internal bus A.

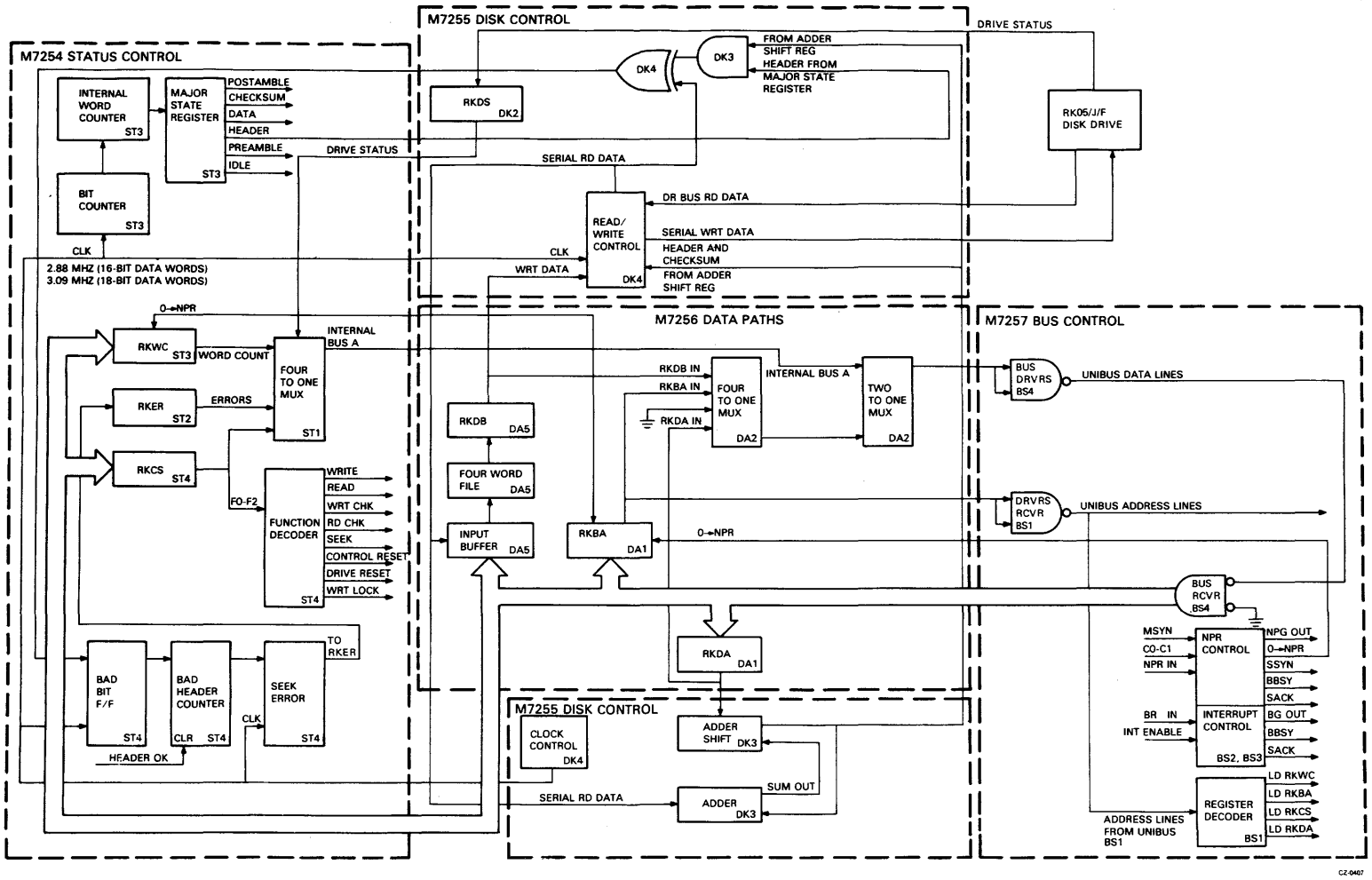


Figure 4-1 RK11D/E Controller Simplified Block Diagram

Bit Counter

The bit counter counts word lengths of 16 or 18 (decimal) bits. During write data operations, its input is CLK from the disk control module. CLK can be derived from either the 2.88 MHz crystal used for 16-bit word formatting (RK11D) or the 3.Ø9 MHz crystal used with 18-bit words (RK11E). During read data operations, the clock is derived from the drive logic. The drive separates read clocks from the data and sends both clock and data signals to the controller.

The bit counter sends its output to the internal word counter.

Internal Word Counter

The internal word counter counts the output of the bit counter. By doing this, the internal word counter keeps track of the sector length for the major state register.

Major State Register

The major state register controls each phase, or "major state", that the controller progresses through while performing a seek, read, or write operation. Each major state causes specific logic operations to be performed. The output of this register corresponds to each area of a sector.

The major state register uses the output of the internal word counter as one of the conditions to advance to another state. For example, after counting the 256 words of the data field, the major state register will advance to the checksum major state.

Not all of the major states are required for the completion of every command, so another input to the state register is the command that is being performed.

Header Check Circuitry

The header check circuitry consists of the bad bit flip-flop, bad header counter and seek error flip-flop. This logic is used to check the header word during data commands. The header word (cylinder address) is input from the RKDA via the adder shift register and is checked against the header word read from the disk drive. If the bad bit flip-flop sets due to a miscompare, it increments the bad header counter. The RK11 will then read the header words on the track another 15 (decimal) times. If the header word does not compare and the counter has incremented to 16 (decimal), the controller sets the seek error flip-flop.

The seek error flip-flop output is sent to the error register as a program flag. If a good header comparison is made during the time the counter is incrementing toward 15, the signal HEADER OK clears the counter and a seek error does not occur.

M7255 DISK CONTROL

The disk control module (DK) controls the functions of the drive according to commands received from the ST module. The DK module organizes information from, and sends information to, the other areas of logic.

RKDS Register

The RKDS register monitors status conditions of the selected drive and applies its output to the four-to-one multiplexer on the ST module. When the RKDS input on the four-to-one multiplexer is selected, the drive status data is sent via the internal bus A lines to the disk control module for transmission to the UNIBUS. The RKDS register is a read-only register.

Adder Shift Register

The adder shift register performs the four tasks listed below.

- The disk address register (RKDA) contents are serialized by the shift register, and are shifted to the read/write control logic. This enables the header word to be written on the disk during write data commands.
- The disk address contents are shifted to the status control logic. This enables the header word to be checked during read or write data commands.
- The shift register checksum contents are shifted to the status control logic. This enables the calculated checksum to be compared with the checksum read from the disk during read data or read check commands.
- The shift register checksum contents are shifted to the read/write control logic. This enables the calculated checksum to be written on the disk during write data commands.

Adder

The adder circuit performs the two tasks listed below.

- This circuit computes the checksum character for write data commands.
- This circuit also computes the checksum character for read data commands.

The checksum is calculated by serially adding each bit of the sector to be written with the existing contents of the adder shift register. As each word is added, the shift register contains a new checksum. At the completion of the sector, the accumulated checksum is sent to the read/write control circuits and written on the disk at the end of the data field.

For a read, read check or write check command, the checksum is calculated by adding the serial read data with the contents of the adder shift register. The result is compared to the checksum that is written on the disk, following the data field.

Read/Write Control

The read/write control logic controls the reading or writing of all data for each sector on the disk. Data read from the disk is clocked with a read clock supplied by the drive. The read data is shifted by the read/write control logic to the input buffer of the four-word file. Data to be written is combined with the output of the crystal oscillator and encoded by the read/write control logic into frequency-modulated data. This data is shifted to the disk for writing.

Clock

The clock control logic consists of a crystal oscillator and associated logic which outputs a frequency of 2.88 MHz for the RK11D Controller and 3.Ø9 MHz for the RK11E Controller. This crystal is used during write data commands.

There is an auto/manual switch on the DC module which is used with the crystal oscillator. When the switch is in auto position, the crystal oscillator is used to generate clocking. When the switch is in manual position, the crystal oscillator is bypassed, thus making it possible to use an external clock for timing. Under normal operating conditions, the switch must be in the auto position in order for the controller to operate.

During read data commands, the clocking originates from the disk drive. Logic in the drive separates the recorded data from the clocks and transmits both to the controller, then uses this clock to control the data and counting circuits.

M7256 Data Paths

The data path module (DA) controls the bidirectional data flow (read or write) between a selected drive and the UNIBUS. The central logic in the control of data flow is the four-word file and associated logic. The file is responsible for buffering, serialization and deserialization of data.

Additional logic on this module includes three registers and two multiplexers. Each of these are described in the following paragraphs.

Input Buffer

The input buffer consists of five shift register ICs that serve as the input to the four-word file. These ICs are configured to handle either 16-bit or 18-bit data words, depending on whether the RK11 is configured as an RK11D or an RK11E.

During a write or write check command, the input buffer is parallel-loaded with a data word from the UNIBUS data lines (BUS D). The status control negates READ during a write or write check operation to enable the register to load. The DATA STROBE 2 pulse from the bus control module clocks in the data word from the UNIBUS D lines. The data word is then parallel-loaded into the four-word file.

For a read command, READ is asserted, enabling the input buffer to shift. Each CLK IN BUFF pulse then shifts the input buffer one bit position toward bit ØØ. CLK IN BUFF also loads serial data from the read/write control logic (SER RD DATA) to either bit position 15 (for the RK11D) or bit 17 (for the RK11E). When the entire word has been assembled in the input buffer, it is then transferred to the four-word file.

GEN CLR from the status control clears the input buffer.

Data Buffer Register

This register (RKDB) consists of five shift register ICs that handle data between the four-word file and either the read/write control logic or the bus control logic (via a multiplexer). This buffer is the output of the four-word file and, during write operations, serializes the data for the read/write control logic. During read operations, NPR transfers will move the contents of the buffer to the four-to-one multiplexer and then to the two-to-one multiplexer on its way to the UNIBUS D lines.

Four-Word File

The four-word file consists of five register ICs intended to provide four 16-bit (RK11D) or 18-bit (RK11E) word locations of storage area. It is possible to read a word from one location while simultaneously writing another word into a different location.

The controlling logic for the file consists of the circuits listed below.

- Input counter
- Output counter
- Four-word file status flip-flops
- Input buffer full status flip-flop
- Output buffer full status flip-flop

Each time the file is accessed to store a word in it, the input counter is incremented. If the output buffer is empty, and the output counter is zero, this word will be transferred directly to the output buffer.

All successive words are placed in the file according to the location specified by the input counter. All words to be retrieved from the file are transferred to the output buffer. The word location in the file to be accessed for this transfer is determined by the output counter.

Bus Address Register

This register (RKBA) consists of four counter ICs. The RKBA is parallel-loaded from the UNIBUS D lines with bus address information when LOAD RKBA LO and LOAD RKBA HI are asserted by the bus control.

When the bus control asserts Ø -> NPR, the RKBA register is incremented. The Ø -> NPR pulse indicates completion of an NPR transfer. Thus, the RKBA is incremented twice for each transfer to the next sequential bus address (which will always be an even number).

RKDA Register

The RKDA register is loaded via the UNIBUS D lines, with the cylinder, sector and surface addresses necessary for seeks and header comparisons. The output of the disk address register goes to two places: the adder shift register and the four-to-one multiplexer on the DA module, as described below.

The adder shift register output is used in two places. The ST module uses it for header comparisons during read data operations. The read/write control logic uses it for rewriting of the header word during write data commands.

The multiplexer output enables the register to be read by the software. This multiplexer selects one of the three registers found on the DK module and outputs the contents of one of these registers to the two-to-one multiplexer. This path allows the program to examine the contents of any one of these registers (RKBA, RKDA or RKDB).

Two-To-One Multiplexer

This multiplexer allows one of two inputs to be placed on the UNIBUS data lines to be transferred back to memory. One of the inputs is from internal bus A lines (ST module). The other input is the output of the four-to-one multiplexer on the DA module.

Internal bus A contains the output of another four-to-one multiplexer which allows the program to read the RKWC, RKER, RKDS and RKCS registers.

M7257 BUS CONTROL

The bus control logic of the M7257 (BS) module serves as an interface between the UNIBUS and the RK11 Controller by generating all UNIBUS control signals. The bus control logic consists of register address selection, NPR control, interrupt control, and UNIBUS driver/receiver logic.

Register Decode Logic

The register decode logic determines which registers are to be addressed by, and loaded from, the UNIBUS. The multiplexers handle the reading of the registers directly. The multiplexers have inputs from the UNIBUS address lines to select one of the seven registers.

The input to the register decoder are bits 1, 2 and 3 of the UNIBUS address lines and are exclusive-ORed with a set of jumpers to determine if a register in the RK11 is being addressed. If the bits do not compare with an existing RK11 register, then the bus control logic assumes the software via the UNIBUS wants to communicate with some other device on the UNIBUS.

NPR Control Logic

The NPR control logic requests use of the UNIBUS by generating BUS NPR L for any data transfer function. Figure 4-2 shows the NPR timing for write or write check commands. Figure 4-3 shows the NPR timing for read commands.

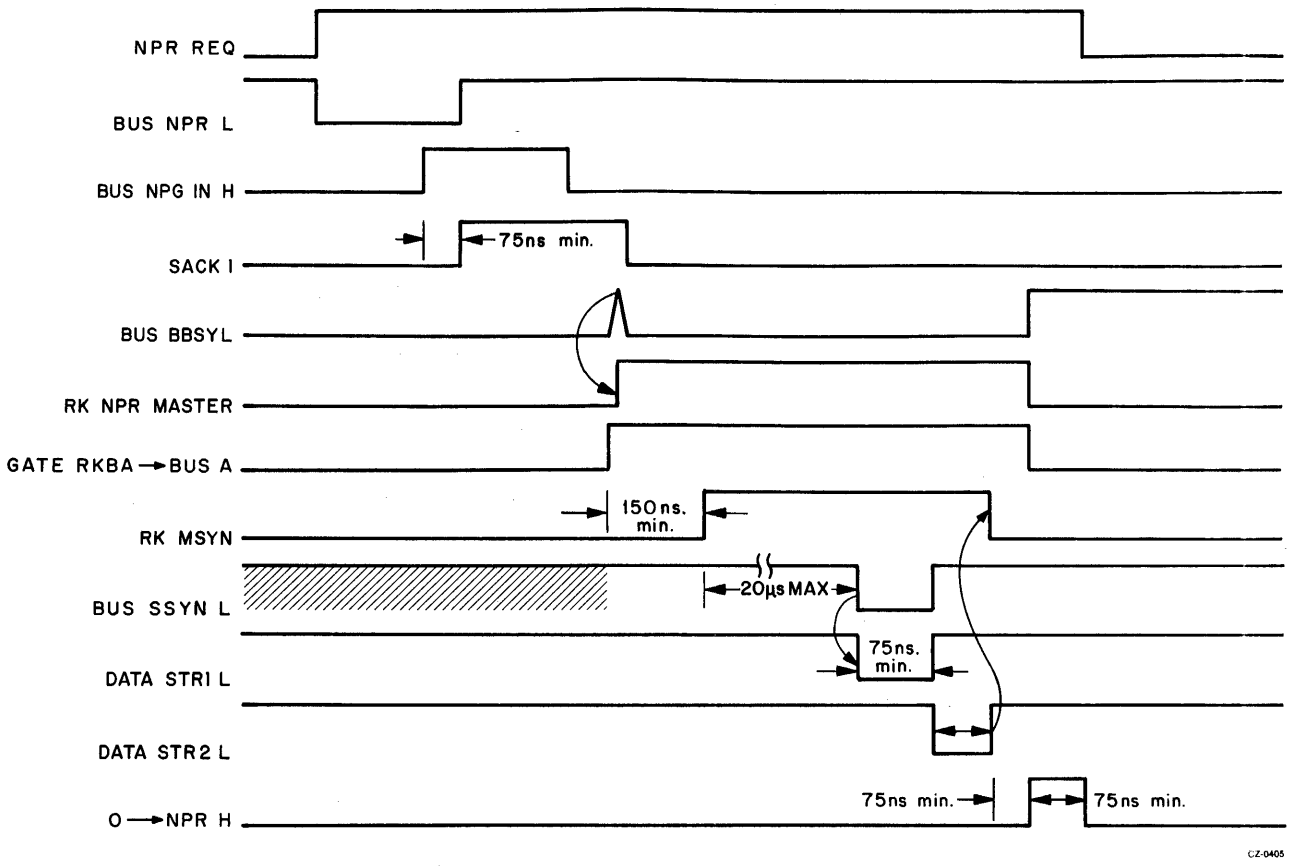


Figure 4-2 NPR Timing Diagram for RK11 Write or Write Check

Interrupt Control Logic

The interrupt control logic generates interrupt requests by the RK11. RK11 interrupts are initiated when the conditions listed below are met.

- Controller is ready.
- IDE bit is set in the control register.

The BR level of the RK11 Controller is usually five. Figure 4-4 shows the interrupt timing for the RK11 bus request.

This completes the description of the overall block diagram of the RK11 Controller. Each major logic circuit has been described to help you understand the concepts of its operation. The data paths will now be described, utilizing a separate block diagram for the read, write and write check commands. Each block diagram highlights the areas used by each of these commands, allowing you to see more clearly the circuits used by the command.

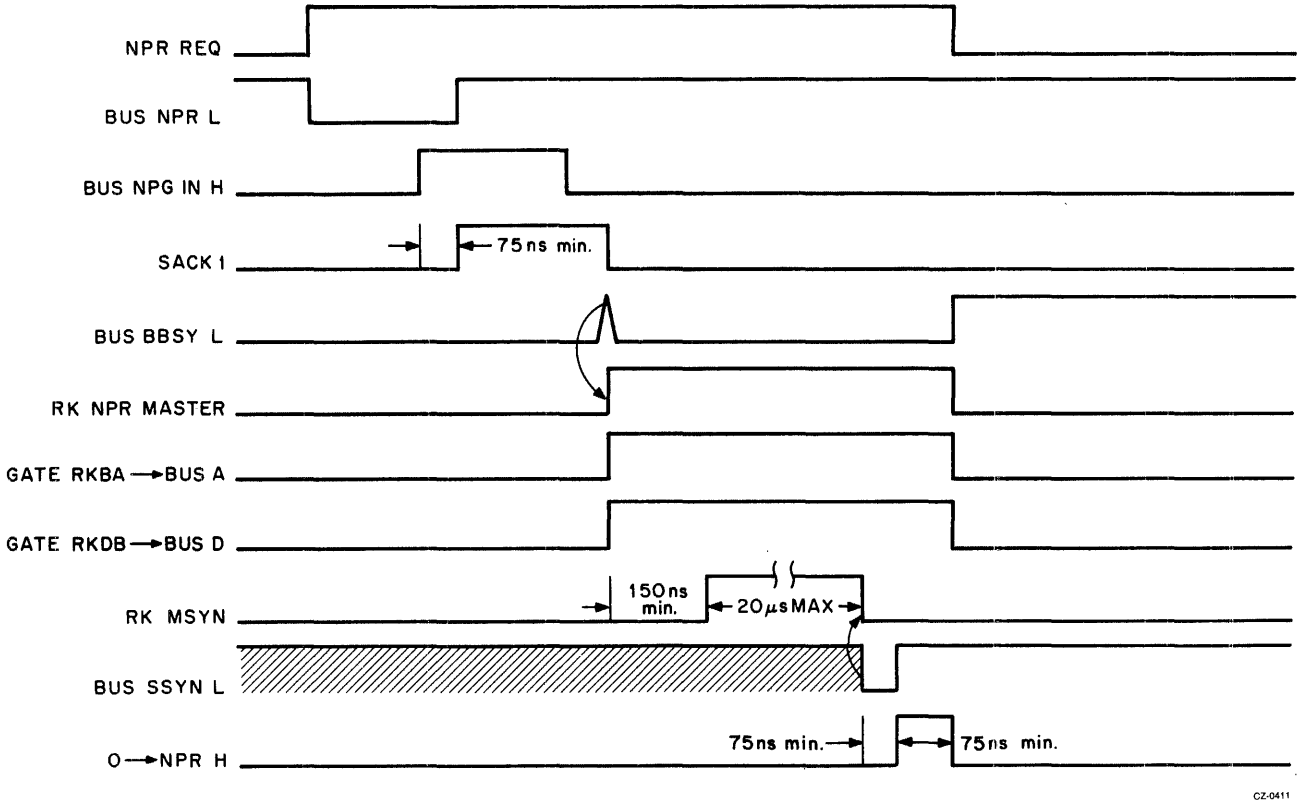


Figure 4-3 NPR Timing Diagram for RK11 Read

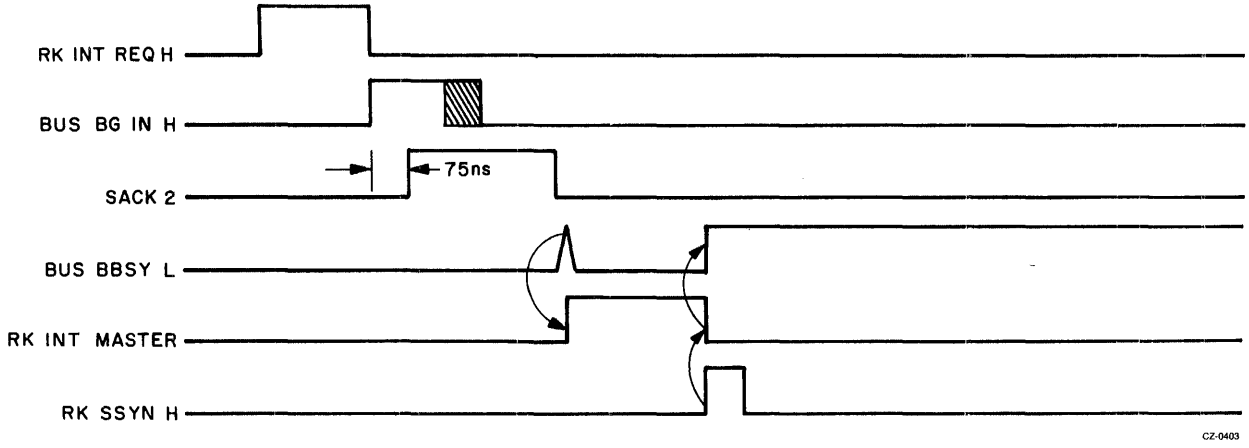


Figure 4-4 RK11 Bus Request Interrupt Timing Sequence

DATA PATHS GENERAL INFORMATION

This section describes the elements common to all the different data commands. Figure 4-5 indicates these elements as shaded areas or darkened lines.

For any command to be executed, the software must load the appropriate registers. The RKWC will be loaded with the number of whole PDP-11 words to be transferred between the RK11 Controller and memory. The RKBA will be loaded with the memory address that the RK11 Controller will access for any of the data transfer commands. The RKDA will be loaded with the address that the RK11 Controller will use to access the disk drive (i.e., cylinder, sector and head). The RKCS register will be loaded with the appropriate function code, GO bit, and other needed control bits. (See Figure 3-3.)

Once the GO bit has been loaded, the RK11 initiates the function. The first event to take place in all commands is that the disk address is sent to the disk drive. Control logic transfers the contents of the RKDA in parallel to the cylinder difference and detection logic of the drive. Upon reception of the new disk address, the drive computes the difference between the current location of the heads and the new disk address. If the two are different, the drive seeks to reposition the heads.

Upon completion of the seek, the controller must then verify the new location of the heads. This is done in two different ways, depending on the command being executed.

Read, Write Check or Read Check Header Verification

For these commands, the controller waits for the sector count from the drive to equal the sector address contained in the lower four bits of RKDA (SC=SA). When SC=SA, the controller knows the sector desired by the software is under the heads. At this time, the header on this sector is read and compared with the RKDA register.

To accomplish this header verification, bits Ø5-12 of RKDA are transferred to the adder shift register. They remain there until bits from the disk header are read. The serial read data line containing the header is strobed by the read clock to the XOR circuit on Page DK4 of the print set. Simultaneously, read clocks shift the output of the adder shift register to the same XOR circuit. Bit by bit, these two words, the actual cylinder address and the desired cylinder address are compared for equality. If the disk drive has positioned the heads properly, these two words will compare (RD data = WT data) and command execution will continue. If the disk drive has not positioned the heads to the proper cylinder, the two words will not compare and command execution terminates.

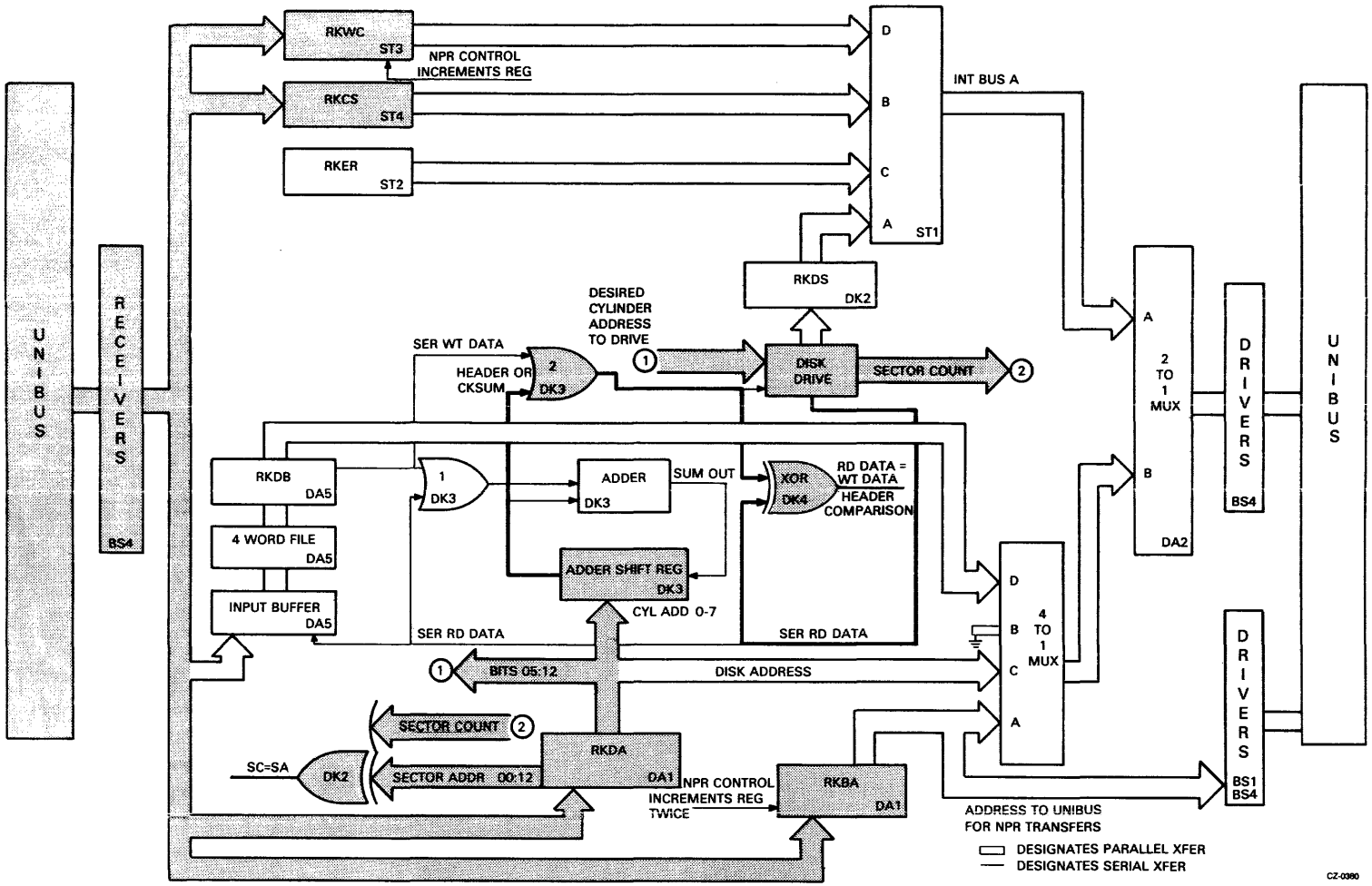


Figure 4-5 Command Initiation

In the event of a simple mis-read of the header due to a dropped or picked-up bit, the logic is capable of reading the header another fifteen times. Each header re-read occurs from SC=SA so that only the desired sector is read. If the header cannot be read after sixteen times, then a seek error is generated, setting bit 12 of RKER.

Write Data Header Verification

The write commands check the header differently than the read commands.

The header and data fields are adjacent to each other in the RKØ5/RK11 format. This requires the logic to rewrite the header each time the data within a sector is to be written.

To verify the header, the controller logic only waits for the occurrence of the next available sector pulse. (In the read commands, the logic waited for SC=SA.) When the sector pulse is detected, the header word in the sector following is read. The header data is sent to the XOR comparison logic via the serial read data line. Simultaneously, the desired header that was transferred out of RKDA and placed in the adder shift register is sent to the same XOR. The desired cylinder address that was in RKDA is compared with the header read from any sector on the disk.

If the disk drive has positioned the heads properly, the two words will match (RD data = WT data) and write command execution will begin.

The controller logic then waits for SC=SA. When the sector count from the drive matches the sector address stored in RKDA, the cylinder address portion of RKDA is transferred to the adder shift register. From the adder shift register, the cylinder address is shifted to the disk drive to be written. If the drive has <u>not</u> positioned the heads properly, the header will not verify and command execution terminates.

In the event of a simple mis-read of the header due to a dropped or picked-up bit, the logic is capable of reading the header another fifteen times. Each header re-read occurs on consecutive sectors. If the header cannot be read after sixteen times, then a seek error is generated, setting bit 12 of RKER.

WRITE DATA PATHS BLOCK DIAGRAM

Figure 4-6 shows the data path taken for a write data command. The text below gives the sequence of events that take place during the write operation.

NOTE

The field maintenance print set includes detailed flow charts for each RK11 command. The text below gives a condensed version of the commands.

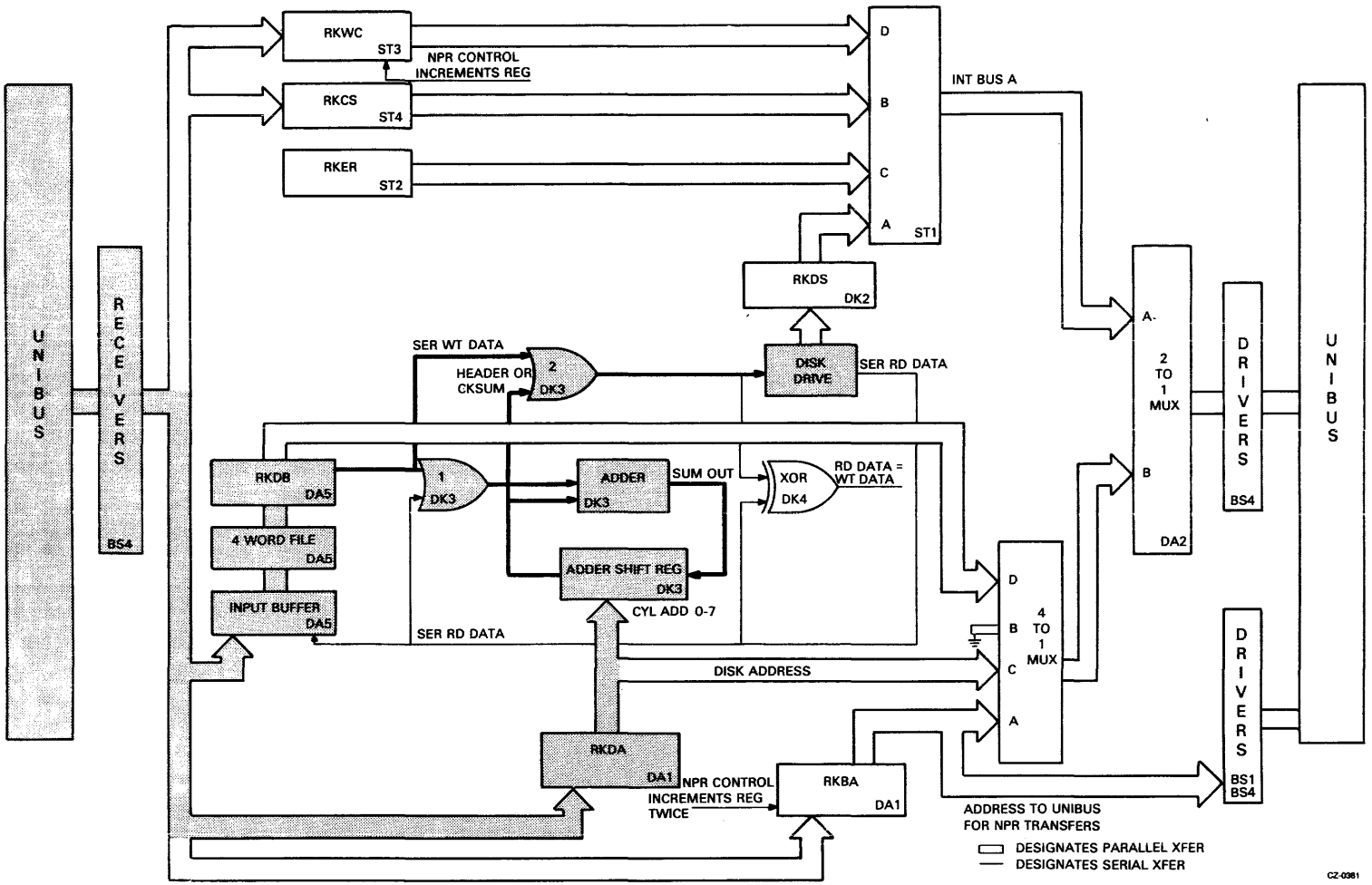


Figure 4-6 RK11 Data Path Block Diagram - Write

1. Major state register is in idle (command initiation; drive performs a seek).

   - RKWC is loaded with the number of words to be written on the disk.
   - RKDA is loaded with the sector, surface and cylinder addresses to be used on the disk.
   - RKBA is loaded with the starting address in memory where data is to be retrieved.
   - RKCS is loaded with the function code of write data and a GO bit.

     a. Control register logic decodes command.

     b. Seek is performed using address supplied by RKDA.

     c. Controller waits for R/W/S READY from drive (to indicate seek is complete).

     d. Controller waits for first available sector pulse.

2. Major state register shifts to preamble (logic prepares to compare header).

   - Read enable asserted to drive.
   - RKDA contents are transferred to adder shift register (desired cylinder address).
   - Preamble and sync bit are read.

3. Major state register shifts to header (logic compares header).

   - Header being read is compared with contents of RKDA.

4. Major state register shifts back to idle if header compares (RD data = WRT data).

   - Read gate negated to drive.
   - Controller waits for SC=SA (sector counter contents equals sector address in RKDA).

5. Major state register shifts to preamble (logic prepares to write header).

   - Write gate is asserted to disk.
   - RKDA contents are transferred to adder shift register.
   - Preamble and sync bit are written.

6. Major state register shifts to header (logic writes header).

   - Contents of adder shift register shifted to drive (via OR gate 2).

7. Major state register shifts to data (user's data written onto disk).

   - NPRs cause memory data to be transferred to input buffer using address supplied by RKBA.

   NOTE
   The initial NPRs occur as soon as function decoding determines that a write operation is to be performed.

   - Input buffer transfers words to four-word file.
   - Four-word file transfers words to output buffer.
   - Output buffer serializes data for read/write control logic (OR gate 2 in Figure 4-6).
   - Output buffer simultaneously sends serialized data to adder for checksum calculation (OR gate 1 in Figure 4-6).
   - RKWC increments as each word is retrieved from memory via NPRs.

8. Major state register shifts to checksum at an internal count of 256_{10} (logic writes checksum).

   - Checksum in adder shift register is shifted to drive logic (OR gate 2 in Figure 4-6).

9. Major state register shifts to postamble.

   - One word of zeros is written.

10. Major state register shifts to idle.

    - Write gate is negated.
    - Check for RKWC overflow (operation is completed).
    - RKDA is incremented (logic prepares for header verification of next sector).

      a. RKDA is checked for last sector on track (need head change to opposite surface, or seek to next cylinder).

b. RKDA is checked for last track on disk (no more room).

c. Continue if more words are to be written.

READ DATA

Figure 4-7 shows the data path taken for a read data command. The text below gives the sequence of events that takes place during the read operation.

1. Major state register is in idle (command initiation, drive performs a seek).

   - RKWC is loaded with the number of words to be read from disk.
   - RKDA is loaded with the sector, surface and cylinder addresses to be used on the disk.
   - RKBA is loaded with the starting address in memory where data is to be sent.
   - RKCS is loaded with the function code of read data and a GO bit.

     a. Command is decoded by control register logic.

     b. Seek is performed using addresses supplied by RKDA.

     c. Controller waits for R/W/S READY from disk (indicating the seek is complete).

     d. Controller waits for sector pulse.

     e. Controller waits for SC=SA (sector counter contents equals sector address stored in RKDA).

2. Major state register shifts to preamble (logic prepares to compare header).

   - Read enable is asserted to drive.
   - RKDA contents are transferred to adder shift register (desired cylinder address).
   - Preamble and sync bit are read.

3. Major state register shifts to header (logic compares header).

   - Header being read is compared with the contents of RKDA.

4. Major state register shifts to data if header compares (user's data read from disk).

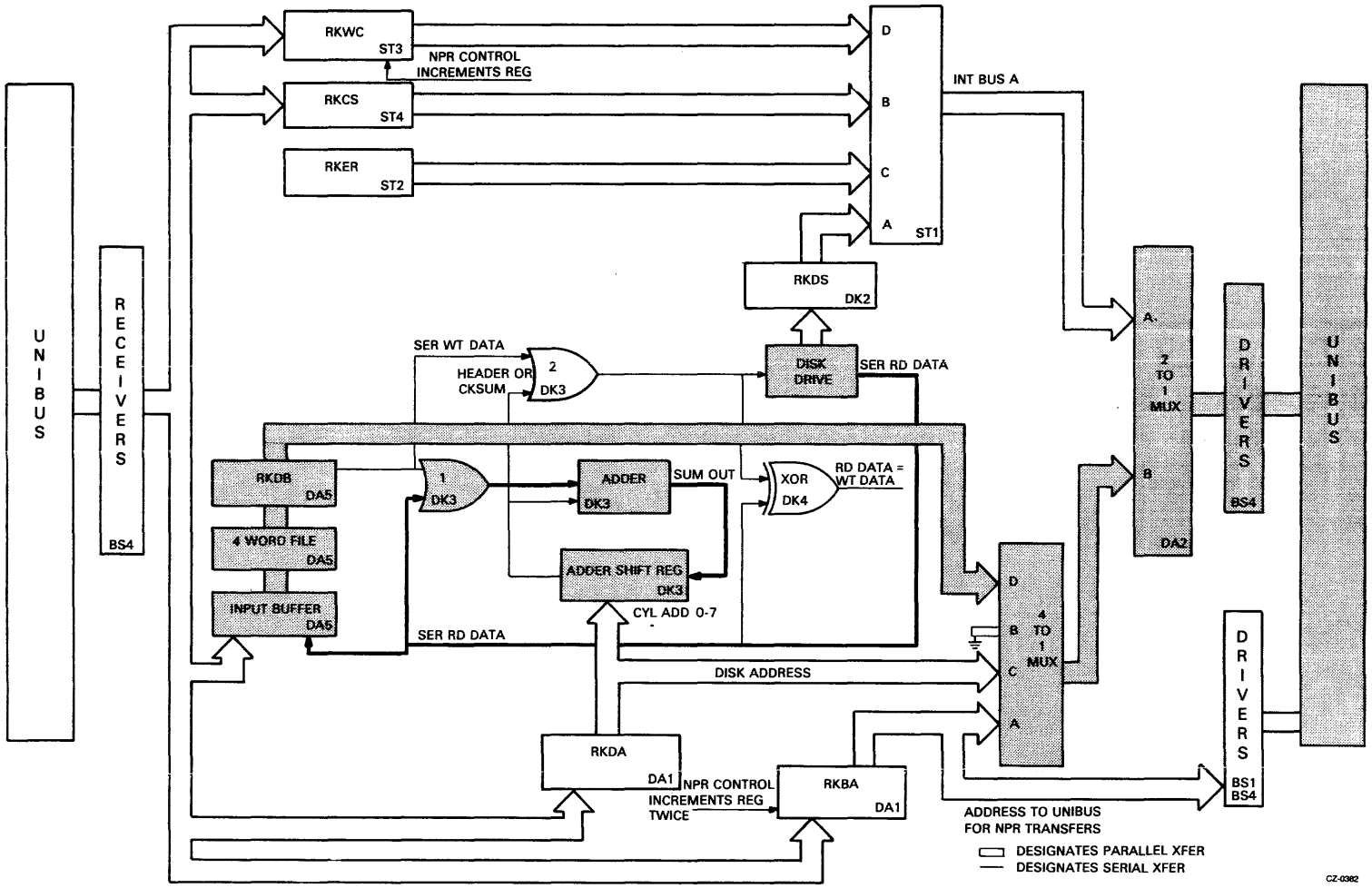


Figure 4-7 RK11 Data Path Block Diagram - Read

- Words being read are shifted into input buffer and adder (OR gate in Figure 4-7) for checksum calculation.
- Input buffer transfers words in parallel to four-word file.
- Four-word file transfers words to output buffer.
- Output buffer transfers words to four-to-one multiplexer.
- Four-to-one multiplexer transfers words to two-to-one multiplexer.
- NPRs transfer contents of two-to-one multiplexer to memory location specified by RKBA.
- RKWC increments as each word is transferred to memory.

5. Major state register shifts to checksum at internal word count of 256_{10}.
   - The checksum being read is exclusive-ORed with contents of adder shift register (OR gate 2 to XOR in Figure 4-7).
6. Major state register shifts to postamble.
   - Read enable negated to drive.
7. Major state register shifts to idle.
   - RKWC checked for overflow.
   - RKDA is incremented.
     a. RKDA is checked for last sector on track (need head change to opposite surface or seek to next cylinder).
     b. RKDA is checked for last track on disk (no more room).
     c. Continue if more words are to be read.

WRITE CHECK

Figure 4-8 shows the data path taken for a write check command. Basically, a write check is the same as a read data command, except that the data from the disk is not transferred to memory. Instead, the data read from the disk is compared with the data from memory. The data comparison is bit by bit and accomplished by the RK11 hardware logic.

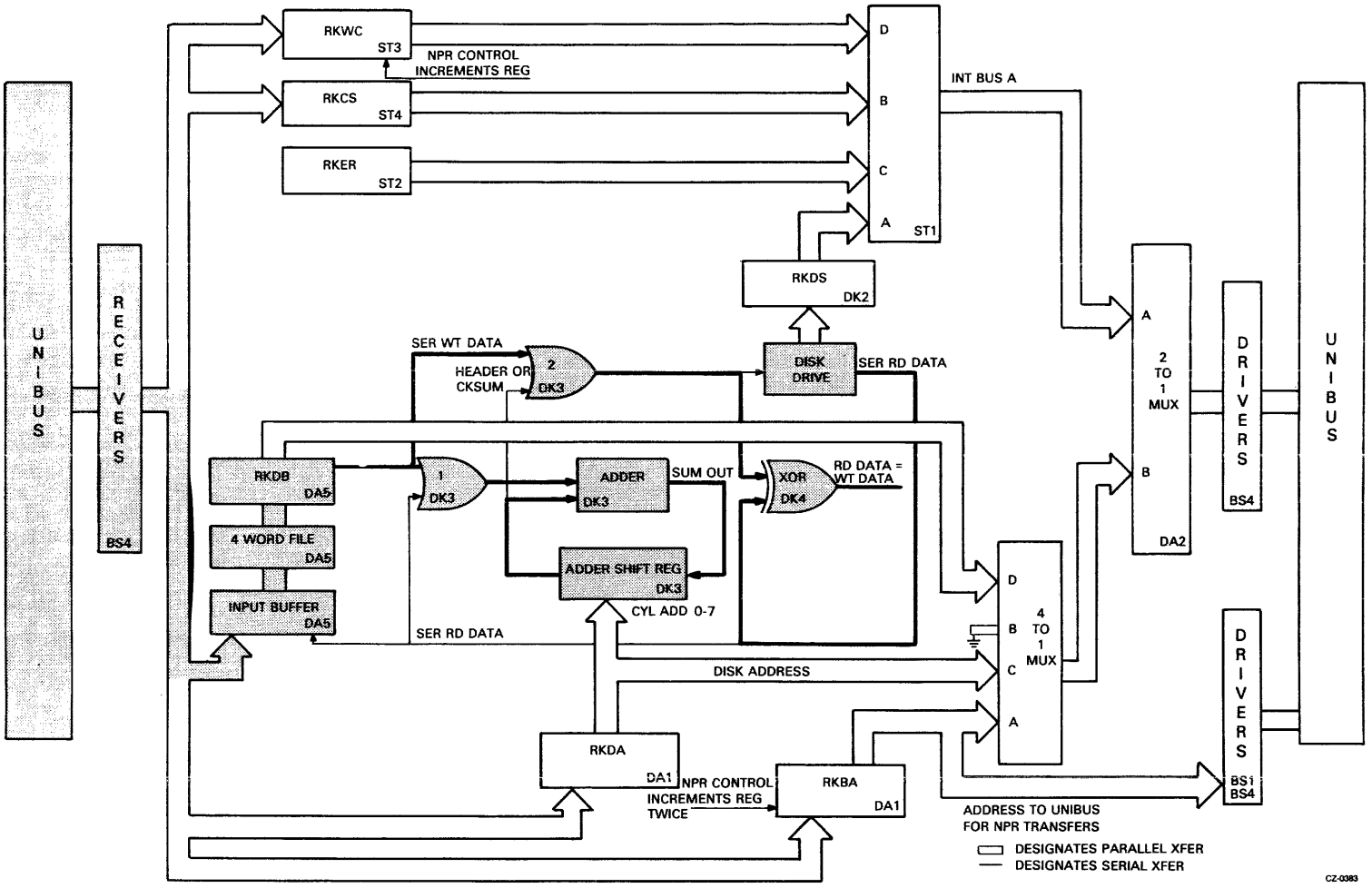


Figure 4-8 RK11 Data Path Block Diagram - Write Check

The text below gives the sequence of events that takes place during the write check operation.

1. Major state register is in idle (command initiation; drive performs a seek).

   - RKWC is loaded with the number of words to be checked.
   - RKDA is loaded with the disk address to be checked.
   - RKBA is loaded with the starting address in memory that data will be checked against.
   - RKCS is loaded with the function code of write check data and a GO bit.

     a. Command is decoded by control register logic.

     b. Seek is performed using addresses supplied by RKDA.

     c. Controller waits for R/W/S READY from drive (indicating that the seek is complete).

     d. Controller waits for first available sector pulse.

2. Major state register shifts to preamble (logic prepares to compare header).

   - Read enable is asserted to drive.
   - RKDA contents are transferred to adder shift register (desired cylinder address).
   - Preamble and sync bit are read.

3. Major state register shifts to header (logic compares header).

   - Header being read is compared with contents of RKDA.

4. Major state register shifts back to idle if header compares (RD data = WRT data).

   - Read gate negated to drive.
   - Controller waits for SC=SA (sector counter contents equals sector address stored in RKDA).

5. Major state register shifts to preamble.

   - Read gate asserted to drive.
   - RKDA contents are transferred to adder shift register.

- Preamble and sync bit are read.

6. Major state register shifts to header (logic compares header on first sector to be checked).

   - Header being read is compared with contents of RKDA.

7. Major state register shifts to data if header compares.

   - Data from memory is write checked with the data read from the disk (XOR).

     a. Read sector data.

        - Data is shifted to an exclusive-OR circuit from serial read data line.

        - Data is shifted to the adder for checksum calculation from serial read data line via OR gate 1 as shown in Figure 4-8.

     b. Obtain words from memory using addresses supplied by RKBA.

        NOTE

        The initial NPRs occur as soon as function decoding determines that a write check function is to be performed.

     c. NPRs cause data from memory to be transferred to the input buffer of the four-word file.

     d. Input buffer transfers words to the four-word file.

     e. Four-word file transfers words to the output buffer.

     f. Output buffer serializes data for write check comparison.

     g. OR gate 2 routes data from memory (output buffer) to XOR as shown in Figure 4-8.

   - RKWC increments as each word arrives from memory.

8. Major state register shifts to checksum at an internal word count of 256_{10}.

   - The contents of adder shift register are exclusive-ORed with the checksum being read (via OR gate 2 as shown in Figure 4-8).

9. Major state shifts to postamble.

   - Read enable negated to drive.

10. Major state register shifts to idle.

- Check for RKWC overflow.
- Increment RKDA.

  a. RKDA is checked for last sector on track (need head change to opposite surface or seek to next cylinder).

  b. RKDA is checked for last track on disk (no more room).

  c. Continue if more words are to be checked.

SUMMARY

The RK11 consists of four modules.

- M7254 status control module initiates the programmable functions of the controller and establishes the logic states. The logic circuits on this module are listed below.
  - RKCS register contains the function code which will indicate the function to be performed.
  - RKWC register contains the 2's complement of the number of words to be transferred to or from the disk during read, write or write check commands.
  - RKER register contains the error status of the controller and selected drive.
  - Four-to-one multiplexer allows gating of one of four registers to internal bus A for routing to the UNIBUS via the two-to-one multiplexer.
  - Bit counter is used to count the number of bits within a word that is being written or read for use by the major state register and internal word counter.
  - Internal word counter uses the overflow of the bit counter to determine the length of the data field within a sector. When 256_{10} words have been counted, the major state register will advance to the checksum major state.
  - Major state register determines the major state used by each function. The output of this register corresponds to each area of a sector (i.e., preamble, header, data, checksum and postamble).

- Header check circuits consist of a bad bit flip-flop, bad header counter and a seek error flip-flop. Used to compare the header word being read during data transfer commands with the contents of the RKDA.

- M7255 disk control module is used to control the functions of the drive according to commands received from the status control. It sends information to other areas of logic. The circuits on this module are listed below.

  - RKDS register is used to monitor the status condition of the selected drive and outputs its data to the UNIBUS.

  - RKDA register is loaded with cylinder sector and surface addesses. The addresses are used during seek and all data transfer commands.

  - Adder shift register is used in conjuction with the adder. Its output is either a 16-bit header or checksum character.

  - Adder is used to compute the checksum character for write data and read data commands.

  - Read/write control is used for controlling the reading and writing of all data within a sector. Contains a crystal oscillator used to generate the clocks used in the frequency modulation data encoding (during a write command).

  - AUTO/MANUAL operation control switch is used to allow the crystal oscillator to generate the internal clock pulses when in AUTO position. When in the MANUAL position, an external source can be used to generate the timing clocks.

- M7256 data paths module controls bidirectional data flow between a selected disk and the UNIBUS. The circuits contained on this module are listed below.

  - Input buffer is used to receive parallel data from the UNIBUS and to transfer the data to the four-word file (write and write check commands). The buffer also receives serial data from the disk and transfers parallel data to the four-word file during read data commands.

  - Four-word file provides four-word locations for buffering the data rate difference between the UNIBUS and the disk.

- Output buffer handles data between the four-word file and either the read/write control logic or the four-to-one multiplexer. This buffer serializes the data for write data commands and is the source of data for NPR reads to memory.

- RKBA register is used to indicate the starting memory address for all data transfer commands.

- Four-to-one multiplexer allows gating of one of three registers to be output to the two-to-one multiplexer.

- Two-to-one multiplexer allows gating of either the internal bus A (one of four registers) from the status control module, or the output of the four-to-one multiplexer (one of three registers) to be output to the UNIBUS.

- M7257 bus control module serves as an interface between the UNIBUS and the controller. Generates all UNIBUS control signals. The circuits on this module are listed below.

  - Register decoder is used to determine which RK11 registers are to be accessed and loaded by the UNIBUS.

  - NPR control logic is used to obtain control of the UNIBUS when requested by a data transfer command.

  - Interrupt control is used to initiate interrupts when requested by the RK11.

- Command initiation (read commands)

  - Registers are loaded.

  - Cylinder address to drive from RKDA bits Ø5-12.

  - Drive seeks to new cylinder address.

  - Sector count from drive compared with RKDA bits Ø8-Ø2 for SC=SA.

  - Compare header word at that sector location with RKDA bits Ø5-12 for RD data = WRT data (present cylinder address = desired cylinder address).

  - Continue with command.

- Command initiation (write commands)
  - Registers are loaded.
  - Cylinder address to drive from RKDA bits Ø5-12.
  - Drive seeks to new cylinder address.
  - Wait for sector pulse.
  - Compare header word at that sector location with RKDA bits Ø5-12 for RD data = WRT data (present cylinder address = desired cylinder address).
  - Sector count from drive compared with RKDA bits ØØ-Ø2 for SC=SA (present sector address = desired sector address).
  - Continue with command.
- Functional Block Diagrams
  - Write data path takes the data from the UNIBUS in parallel form and writes it onto the disk in serial form. Headers are checked on any sector to verify positioner cylinder location. Header is re-written on sector as part of the write operation.
  - Read data path takes the data from the disk in serial form and transfers it to memory via the UNIBUS in parallel form. Headers are checked at the sector from which the read operation is to start.
  - Write check takes data from the disk and data from memory and compares the two for equality. This command can follow a write data command to verify the integrity of the data being stored on the disk.

Now that you have completed this module, you can take the module test. The course administrator has the answers to the test.

RKØ5 DISK SUBSYSTEM MAINTENANCE

RK8-E Subsystem Registers/Commands

RK8-E SUBSYSTEM REGISTERS/COMMANDS

INTRODUCTION

In a previous module, you learned that the RK8-E Controller can control up to four RKØ5 Disk Drives.

The PDP-8 processor, in turn, must communicate with the RK8-E Controller. Like other 8-family peripherals, the RK8-E communicates with the CPU by the use of registers and instructions. The registers in the RK8-E transmit the software commands to the drive via the drive bus, directing the drive to perform several functions or commands.

This module describes the items listed below.

- Function of each register
- Bits in each register
- Functions and commands the RK8-E can perform
- Data format used with the RK8-E/RKØ5 subsystem

While studying this module, don't try to memorize what each bit in every register does. Instead, learn the function of each register, and how the registers are used to control the various commands the subsystem can execute.

OBJECTIVES

Upon completion of this module, you will be able to perform the tasks listed below.

- Define the function of each RK8-E register.

- Cause data to be transferred to the disk drive.

To demonstrate your ability to perform the first task, you will be required to correctly answer 8 out of 1Ø true-false questions within 1Ø minutes using any reference material.

To demonstrate your ability to perform the second task, you will be required to write a short program as a lab exercise which will allow the disk drive to write one complete sector with data. You will have two hours to complete this exercise.

ADDITIONAL RESOURCES

PDP-8 Programming Card
PDP-8E/F/M Maintenance Manual, Vol. III, Chapter 11

RK8-E SUBSYSTEM REGISTERS/COMMANDS

INTRODUCTION

Each RK8-E register falls into one of two categories: those that are loaded or read by user software and those that are transparent to user software. The first category includes the registers listed below.

- Command registers
- Current address register
- Disk address register
- Status register

The second category includes the registers listed below.

- Four-word data buffer
- CRC register
- Major state register
- Divide by 12 bit counter
- Divide by 16 bit counter
- Divide by 128 or 256 word counter

The major registers must be loaded from the processor accumulator (AC) by input/output transfer (IOT) instructions in the correct sequence before the RK8-E performs any control function. The individual flip-flops in the registers are set by bits from the AC.

INSTRUCTIONS

The following are the instructions used to program the RK8-E.

- **SKIP ON TRANSFER DONE OR ERROR (DSKP-6741)** causes the program to skip the next instruction if the transfer done or error flags are set.

- **CLEAR ALL (DCLR-6742)** transfers bits 10 and 11 from the AC to the logic in the RK8-E and clears the AC. See Table 5-1.

- **LOAD ADDRESS AND GO (DLAG-6743)** transfers the contents of the AC to the disk address register.

- **LOAD CURRENT ADDRESS (DLCA-6744)** transfers the contents of the AC to the current address register.

- **READ STATUS REGISTER (DRST-6745)** clears the AC and transfers the contents of the status register to the AC.

- **LOAD COMMAND REGISTER (DLDC-6746)** transfers the contents of the AC to the command register.

- **MAINTENANCE IOT (DMAN-6747)** transfers the contents of the AC to the maintenance logic of the RK8-E. See Table 5-2.

Table 5-1 Clear Operations Using the DCLR Instruction

AC Bit 10	AC Bit 11	Operation
Ø	Ø	DCLS; clears the AC and status register. This bit combination is normally used to clear program interrupts.
Ø	1	DCLC; clears the AC and all RK8-E control logic but does not clear the selected RKØ5 control logic. This bit combination is used only to simulate a power clear or if the controller does not respond to normal commands. Note that this instruction stops the control even if it is rewriting a header word. The status register contains all zeros after the DCLR instruction is executed with this bit combination in the AC.
1	Ø	DCLD; clears the AC and recalibrates the selected drive by forcing it to cylinder ØØØ (home position). This bit combination is used to recover from cylinder address errors (indicated by bit 11, status register).
1	1	Accomplishes same operation as Ø Ø.

NOTE

The instruction codes listed represent those codes executable by the first RK8-E controller on the OMNIBUS. To access the second controller, the "74" portion of each code should be "75". This will select the second possible set of RKØ5s on the system.

Table 5-2 Maintenance Functions

AC Bit	Function
Ø	Enables maintenance logic and disables IOT DLAG (GO)
1	Enables a shift to lower buffer (DB4) by setting the DB4 control flip-flop
2	Check CRC register
3	Check command register
4	Check surface and sector register
5	Check data buffer

Table 5-2 Maintenance Functions (Cont)

AC Bit	Function
6	Check data break request
7	Transfer contents of data buffer 4 to the AC
8	Not used
9	Not used
1Ø	Maintenance data bit
11	Not used

REGISTER DESCRIPTIONS

Command Register

The command register (Figure 5-1) is loaded from the AC by an IOT of 6746 (load command register - DLDC instruction). The DLDC also clears the AC and the status register.

Table 5-3 shows the bit definition for the command register.

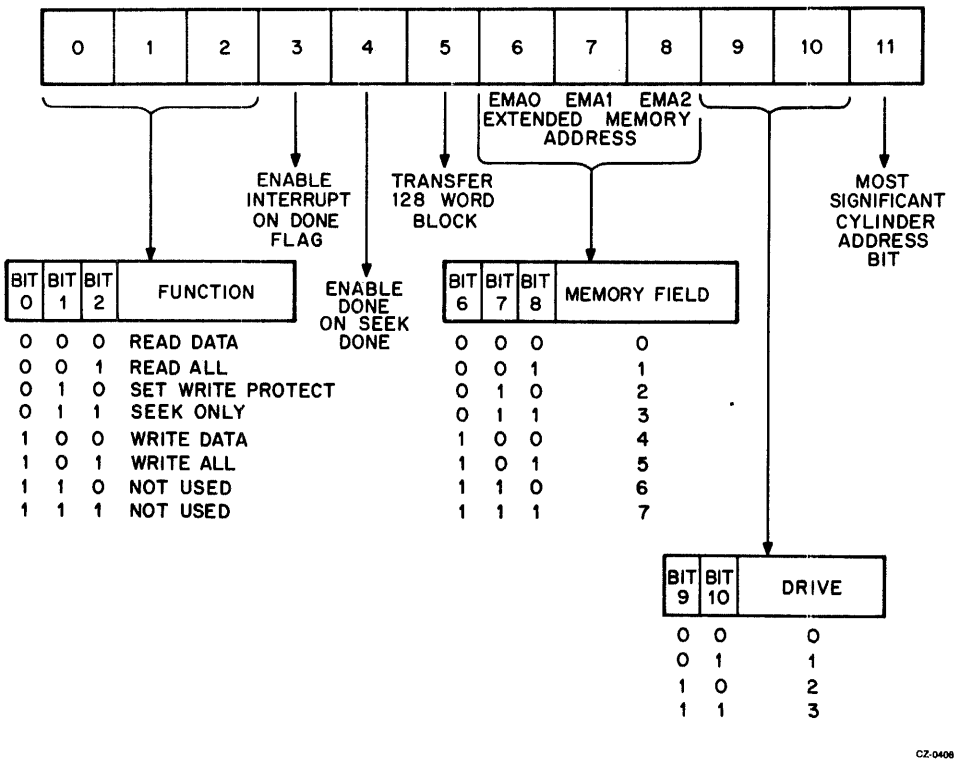


Figure 5-1 Contents of Command Register

Table 5-3 Command Register Bit Definition

Bit(s)	Function
ØØ, Ø1, Ø2	Indicate the function (command) to be performed by the device. The binary coding for each function is listed below. **Bit Ø Bit 1 Bit 2** Ø Ø Ø Read data Ø Ø 1 Read all Ø 1 Ø Write protect Ø 1 1 Seek 1 Ø Ø Write data 1 Ø 1 Write all 1 1 Ø Not used 1 1 1 Not used
Ø3	Enables interrupt on transfer done or error flag.
Ø4	Indicates that a seek is complete.
Ø5	Commands the controller to write or read 128 words instead of 256 (half sector instead of whole sector).
Ø6, Ø7, Ø8	Specify the address extended memory field to be used. The binary coding for each function is listed below. **Bit 6 (EMA2) Bit 7 (EMA1) Bit 8 (EMAØ)** Ø Ø Ø Field Ø Ø Ø 1 Field 1 Ø 1 Ø Field 2 Ø 1 1 Field 3 1 Ø Ø Field 4 1 Ø 1 Field 5 1 1 Ø Field 6 1 1 1 Field 7 When the current address register overflows (reads all zeros) these bits do not increment. The program must reload the command register to select a new memory field.
Ø9, 1Ø	Selects one of four disk drives as shown below. **Bit 9 Bit 1Ø** Ø Ø Drive Ø Ø 1 Drive 1 1 Ø Drive 2 1 1 Drive 3

Table 5-3 Command Register Bit Definition (Cont)

Bit(s)	Function
11	This bit combines with the 7-bit cylinder address register to allow program access to cylinder addresses up to 312 octal (202 decimal). Note that an address greater than 312 causes an address error.

Each function that the command register can select (by utilizing bits 01 and 02) is described below.

Read Data - Initiated when a code of 000 is transferred from AC0-AC2 to the command register by a DLDC instruction. The following text lists the sequence of events in performing a read data command.

- Seek (move the positioner to the desired cylinder).
- Check the header (verify positioner location).
- Read 256 words of data from the disk drive.
  - Read serial data into data buffer 1.
  - Data buffer 1 deserializes data (12-bit word).
  - 12-bit word transfers to last empty buffer.
  - 12-bit word transfers to data buffer 4.
  - Single cycle data break transfers word to memory.

The RK8-E initiates single cycle data breaks so that data buffer 1 will be empty when each new word is received from the drive. If data is read from the drive while data buffer 1 is full, the data request late flag is set and the sector must be read again.

A read operation continues until 256 words have been read from the drive and the transfer done flag sets. If the half-block bit is set, 256 words are read, but only the first 128 words are sent to memory. The second 128 words are all zeros and are not transferred to memory.

Read All - Initiated when a code of 001 is transferred from AC0-AC2 to the command register by the DLDC instruction. Read all is identical to a normal read data operation except that no verification of the headers takes place.

Write Protect - Initiated when a code of Ø1Ø is transferred from ACØ-AC2 to the command register by a DLDC instruction. This command write protects the selected drive. If the program attempts to write on a drive that has write protect set, a write lock error occurs and stops the write operation. The way to enable writing on a drive that has been write protected is to physically reset the WRT PROT switch on the drive that was write protected.

Seek Only - Initiated when a code of Ø11 is transferred from ACØ-AC2 to the command register by a DLDC instruction. The selected drive seeks to the cylinder contained in the cylinder address register. It does not check the header or start a read or write operation.

At the initiation of the seek only command, the transfer done flag sets after IOT DLAG is executed. Transfer done is set again when the seek is complete if bit 4 in the command register is set.

Write Data - Initiated when a code of 1ØØ is transferred from ACØ-AC2 to the command register by a DLDC instruction. The following text lists the sequence of events in performing a write data command.

- Seek (move the positioner to the desired cylinder).
- Check the header (verify positioner location).
- Write 256 data words from memory.
    - Single cycle data breaks load data buffer 1 with a 12-bit parallel word.
    - 12-bit word transfers to last empty buffer.
    - 12-bit word transfers to data buffer 4 where it is serialized.
    - 12-bit word is shifted to drive for writing.

The RK8-E performs single cycle data breaks at a rate that allows a word to be available (in the data buffer register) when the drive is ready to write. If the disk drive calls for data when the data buffer register is empty, the data request late flag is set and the sector must be rewritten.

The write operation continues until 256 words have been written on the cartridge and the transfer done flag sets. If the half block bit is set, 128 words of data from memory are written on the disk cartridge and 128 words of all zeros are written on the remainder of the sector.

Write All - Initiated when a code of 101 is transferred from AC0-AC2 to the command register by the DLDC instruction. This function is identical to the write function except the headers are not checked by the RK8-E.

Write all is used to format a new disk cartridge. In formatting a disk cartridge, a header word is written at the beginning of each sector.

Current Address Register

The current address register is a 12-bit register loaded from the AC with an IOT of 6744 (load current address - DCLA instruction), which also clears the AC. This register and the three EMA bits of the command register (bits 6, 7, and 8) are combined to make up a 15-bit memory address register.

The contents of the current address register and the three bits in the command register are applied to the OMNIBUS MA and EMA lines to select a memory location during a data transfer. The current address register is incremented before each data transfer to select the next sequential memory location. The extended memory address bits in the command register are not incremented, and these bits must be changed by the program to select new memory fields.

If the current address register is incremented past the last memory location in a field, the current address will wrap around in the same memory field. The data is then stored in location 000 and continues incrementing through the field again.

Disk Address Register

The disk address register is loaded from the AC by an IOT of 6743 (load address and GO - DLAG instruction). The DLAG also clears the AC and enables the command in the command register to be executed. See Figure 5-2.

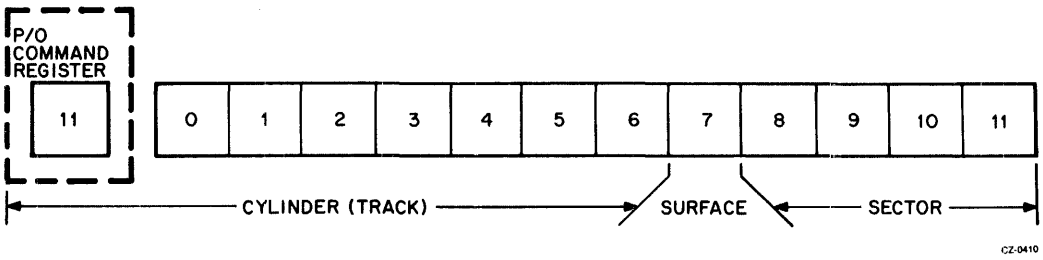


Figure 5-2 Disk Address Register

The disk address register selects a sector to be used in the execution of a data transfer command.

The disk address register and bit 11 in the command register combine to select 1 of 203 (decimal) cylinders, 1 of 2 surfaces, and 1 of 16 (decimal) sectors.

The sequence listed below describes a normal write operation.

- The selected drive seeks to the cylinder specified by bits 0 through 6 in the disk address register and bit 11 in the command register.
- When the selected drive signals it has completed a seek, the header word is checked on the first sector to pass under the read/write heads.
- If the cylinder specified checks with the header word (i.e., the read/write heads are on the right cylinder), the control waits for the next sector pulse.
- The control reads the sector address of each sector passing under the read/write heads.
- The write operation is performed when the correct sector is found.

The sequence listed below describes a normal read operation.

- The selected drive seeks to the cylinder specified by bits 0 through 6 in the AC and bit 11 in the command register.
- When the selected drive signals that it has completed a seek, the controller reads the sector address of each sector passing under the read/write heads.
- When the correct sector is found, the header word is checked against bits 0 through 6 in the disk address register and bit 11 of the command register.
- If the cylinder specified checks with the header word (i.e., the read/write heads are on the right cylinder), the read operation continues.

Status Register

The status register is loaded by the controller and Figure 5-3 shows the information that is available for software to evaluate the operation of the RK8-E and RK05.

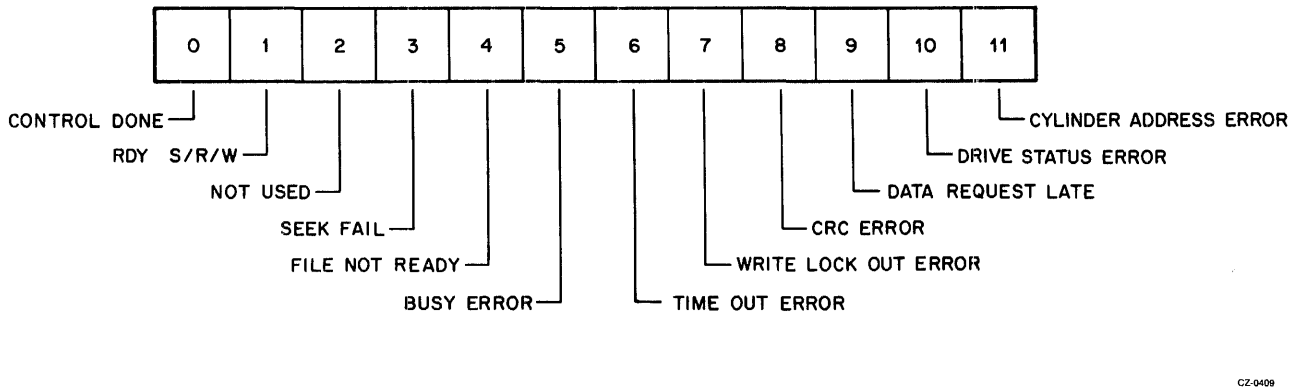


Figure 5-3 Contents of Status Register

The read status register instruction (DRST) is used to access the status register. This instruction will clear the AC and transfer the contents of the status register to the AC. The octal code for the DRST instruction is 6745.

Table 5-4 gives the bit definitions for the status register.

Table 5-4 Contents of Status Register

Bit(s)	Indication
ØØ	Transfer done indicates that one of the following has occurred. • A data transfer command has completed. • An error occurred while the controller was executing an operation. • The selected drive completed a seek only command. • The selected drive completed a recalibrate operation if bit 4 in the command register is set. **NOTE** **The transfer done flag causes a program to interrupt if bit 3 in the command register is set.**
Ø1	RDY S/R/W indicates the selected disk drive heads are not in motion and the selected drive is ready (RDY) to seek, read or write.
Ø2	Not used

Table 5-4 Contents of Status Register (Cont)

Bit(s)	Indication
Ø3	Seek fail indicates that the selected drive did not seek to the cylinder address specified by the program. A recalibrate operation would normally be performed following this error and clearing bit Ø3.
Ø4	File not ready indicates the selected drive is not ready or is inoperative.
Ø5	Control busy error indicates that the program tried to execute a DLAG, DLCA, or DLDC instruction while the control was busy (idle is cleared). **NOTE** **IOT DCLR with AC bit 11 should not be used to clear a control busy error. If the DCLR instruction is issued by the program, the operation is aborted even if the program is writing a header word.**
Ø6	Time out error indicates that the controller has been busy for more than 32Ø milliseconds. Time out error indicates a hardware problem and can be cleared by the DCLR instruction.
Ø7	Write lock error indicates that the program attempted a write data command on a write-protected disk drive.
Ø8	CRC error indicates that the CRC character read from the disk does not agree with the CRC character calculated by the RK8-E.
Ø9	Data request late indicates that the processor did not respond to a break request within 22.5 microseconds. Data request late indicates one of the two conditions listed below. • Read Data Commands - The data buffer register is full, and the processor did not grant a BRK RQST within 6.5 microseconds after the register was filled. • Write Data Commands - The data buffer register emptied, and the processor did not grant a BRK RQST within 6.5 microseconds after the register was emptied.

Table 5-4 Contents of Status Register (Cont)

Bit(s)	Indication

10	Drive status error indicates that the DLAG instruction was executed by the program for one of the two reasons listed below.
	• The drive is not ready (file not ready - bit 04) because of one or more of the conditions listed below.
	  • No power.
	  • Non-existent drive (incorrect address).
	  • No cartridge in selected drive.
	  • The door on the selected drive is not closed (interlock open).
	  • Disk is not up to speed (disk rotation less than 1500 r/min).
	  • Load switch on the selected drive is not in the RUN position. The transfer done flag is set as a result of drive not ready.
	• The write check error sets, indicating the drive has one of the error conditions listed below.
	  • Erase or write current without a write gate (FAULT lamp is illuminated on drive front panel).
	  • The head position transducer lamp is inoperative. If write check error is set, the WT PROT switch on the selected drive must be depressed to remove the error. Write check error does not set the transfer done flag (FAULT lamp is illuminated on drive front panel).
	  • If disk capacity is exceeded (cylinder adddress greater than 312 octal was sent to the selected drive), the program must select a new disk address that is less than 312 octal. The transfer done flag is set if the disk capacity is exceeded.
	  If a seek failure occurs in the drive, this indicates a seek was not completed because of some drive malfunction. If the controller is busy at the time a seek failure occurs, the transfer done flag is set and the disk drive must be recalibrated using the recalibrate IOT DCLR with AC = 10.

Table 5-4 Contents of Status Register (Cont)

Bit(s)	Indication
11	Cylinder address error indicates that the header word of a sector does not agree with the cylinder address sent to the drive.

You have studied the four registers which are loaded or read by software. The remaining registers in the RK8-E are transparent to the user. These registers also perform a vital function in the controller and are listed below.

- Four-word data buffer
- CRC register
- Major state register
- Divide by 12 and divide by 16 bit counters
- Divide by 128 or 256 word count register

The function of these registers are described below.

Four-Word Data Buffer

All data transferred between memory and a selected drive pass through the four-word data buffer register (DB1 through DB4). The buffer serves two purposes in the controller logic. The buffer serializes/deserializes the data being transferred to/from the disk drive. The buffer also compensates for the timing differences in the data rates of the OMNIBUS and the disk bus.

This four-word register increases the latency of the RK8-E control from 6.2 microseconds with a single serial register and one data buffer to 22.5 microseconds with four data buffer registers. (Latency is defined as the maximum time the RK8-E control waits for access to the computer memory before data is lost.)

During a read operation, data buffer 1 accepts the serial data from the drive and transfers a 12-bit parallel word to the last unused buffer. Data is eventually transferred from data buffer 4 to memory. During a write operation, data from memory enters data buffer 1 in parallel mode, transfers to the last unused buffer, and is shifted out to the drive as a 12-bit serial word from data buffer 4.

CRC Register

The CRC register is a 16-bit register that performs the four functions listed below.

- The CRC register receives a cylinder address from the AC when the DLAG instruction is executed by the software. The register then transfers the cylinder address to the selected disk drive to initiate a seek.

- This register also makes bit-by-bit comparisons of the cylinder address specified by the software and the cylinder address from the drive to determine if the disk has positioned the heads over the correct cylinder.

- During write operations, a 16-bit CRC character is generated, transferred to the disk, and written at the end of the sector.

- During read operations, a 16-bit CRC character is generated and compared with the CRC character written at the end of the sector. If the two characters are different, the signal NOT EQUAL asserts the CRC error flag. A CRC error is produced if bits are lost or added during the read or write operations.

NOTE

The CRC register and the disk address register are physically one multipurpose register.

Major State Register

The major state register is part of the control sequencer of the RK8-E. With its associated logic, this register performs the major portion of the control functions of the RK8-E such as determining the format of the disk, i.e., preamble, header, data, CRC, and postamble.

The major state register is basically a shift register that shifts a binary one through the stages of the register (states). This register will shift through all the states unless one of the conditions listed below occurs.

- An error is detected.

- The desired function does not require all major states (i.e., seek and recalibrate).

Each state that the major state register goes through is described below.

Idle State - Allows initiation of a disk function and returns to the idle state after an operation is completed. The idle state indicates that the control is not busy and is therefore capable of accepting IOT instructions from the processor.

The idle state flip-flop is set by any of the conditions listed below.

- At the end of erase delay during a write function

- During last break of a read operation (after data buffer register is empty)

- When the selected drive asserts ACKNOWLEDGE during a seek only operation
- When the error flag is set

Restore State - This is a special state used to clear select errors and cylinder address errors. Restore is set by file ready and the CLR DRIVE command which is generated by the DCLD instruction (causes drive to initiate a recalibrate operation).

When the selected disk asserts ACKNOWLEDGE, the restore flip-flop is cleared, returning the major state register to the idle state. In this state, the controller is waiting for new instructions while the disk drive returns to the home position (cylinder ØØØ).

Strobe State - Transfers the cylinder address from the CRC register to the drive and waits for the selected drive to acknowledge the cylinder address. The strobe flip-flop is set by GO when the DLAG instruction is executed by the program if the selected disk drive is ready (FILE READY asserted).

Strobe is cleared when ACKNOWLEDGE is received from the selected drive and the major state register moves to the header A state or sector seek state (when the selected drive is ready to seek, read, or write).

Header A State - Starts a read delay and waits for a sector mark during a read data and write data command. When a sector mark is obtained from the drive, the header B state is entered and the header A state is cleared by header B.

Header B State - Enables the disk to read at the end of read delay. The disk reads zeros until a sync pulse is encountered. The sync pulse indicates the beginning of the header area of the disk format.

During a write data command, the write sync delay is triggered when a sector mark is received from the disk. After 14Ø microseconds (write sync delay), a one bit (the sync pulse) is written on the disk to indicate where the header area starts. When the sync pulse is read or written, the RK8-E advances to the header C state and header B is cleared.

Header C State - Reads the 16-bit header word from the disk and compares it bit by bit with the disk address in the CRC register. Header C is cleared when the divide-by-16 counter overflows to indicate the 16th bit of the header word has been read from the drive. When header C clears, it sets sector seek and starts the sector seek major state.

Sector Seek State - Compares the sector address lines from the RKØ5 to the contents of the surface/sector register.

Header D State - Waits for the completion of READ DLY (85 microseconds) during a read function or the completion of SYNC DLY during a write function.

If the function is to read data, the controller reads all zeros until a sync bit is read. When the sync bit is read, the controller advances to the header E state.

If the function is to write data, the controller writes zeros, and at the assertion of SYNC DLY, writes the sync bit. When the sync bit is written, the RK8-E moves to the header E state and clears the header D state.

Header E State - Reads and ignores the header word during read data operations. (The header word is ignored because header C state determined that the heads are at the desired cylinder.) During write data operations, the 16-bit header word in the CRC register is written. When the 16-bit header word has been read or written, the major state register advances to the data state.

Data State - Transfers 256 data words from PDP-8/E memory to the drive during a write data command, or transfers 256 words of data from the drive to memory during a read data command.

The data break control logic issues single-cycle data breaks at a rate to keep the data buffer full during write data commands. During a read data command, it issues the data breaks to keep the data buffer empty. The data state ends when 256 words have been transferred (one sector) and the word counter overflows.

If the RK8-E has been instructed to transfer a half-block transfer (bit 5 of the command register set), the word counter overflows after 128 words have been transferred. The 128th word ends data transfer operations and the disk reads or writes zeros until the full block of data (256 words) has been read or written. When last word is read or written, the RK8-E advances to the CRC state and clears the data state.

CRC State - Writes the CRC character (generated by the CRC register logic) on the disk at the end of a sector during a write data command.

During a read data command, the CRC character generated during the data transfer is compared with the CRC character read from the disk. Exclusive-OR logic on the CRC register makes a bit by bit comparison of the CRC character read from the disk. If the two characters are different, the CRC error flag is set. Then, the program must check the status register to determine if a CRC error set the error flag.

The major state register advances to the end state and clears the CRC state when the CRC character has been read.

End State - The time when the items listed below can occur.

- Data buffer register is emptied by the single cycle data breaks.
- The CRC error flag is set if the CRC characters were different.
- Read is cleared.
- The done flag is set.
- The RK8-E returns to the idle state (not busy).

During write data commands, the following sequence listed below occurs.

- The controller starts ERASE DLY, and after 25 micro-seconds, write is cleared.
- Done flag is set.
- RK8-E is returned to the idle state.

Note that there is no CRC character comparison during a write operation and thus no CRC error will be detected.

Divide by 12 Bit/Divide by 16 Bit Counters

The divide by 12 bit counter defines PDP-8 data word boundaries. The divide by 16 bit counter determines the boundaries of the header and CRC characters (these are 16-bit words).

The divide by 12 bit counter increments the word counter. As each 12-bit word is read or written, the word counter increments. At a count of 128 or 256 (depending on the HALF BLOCK signal), the counter overflows, stopping all data transfers.

The divide by 16 bit counter counts the bits of the two 16-bit words used in the sector formatting. After reading or writing these 16-bit words, the counter overflows, allowing advancement of the major state register.

Divide by 128 or 256 Word Counter

This register counts the overflow of the 12-bit counter to determine when the correct number of data words (normally 256 words) have been transferred to or from the disk. When the half-block bit is set in the command register, the data transfers stop after the 128th word instead of the usual 256th word.

If the half-block bit is set, data transfers between memory and the drive stop, but the drive continues to read or write zeros until LAST WORD L is asserted (256 words have been read or written). When LAST WORD L is asserted, the data transfer is complete.

SECTOR FORMAT

You have now studied the registers and functions used in the RK8-E. Now, the data (sector) format will be described. Use Figure 5-4 as a reference.

The surface of every RK05 and RK05J Disk Cartridge is divided into 203 cylinders with 16 sectors per track. Each surface of the disk platter has one read/write head. Each sector has the same format for all 16 sectors.

RK05F Disk Drives are double-density units. Each drive formats a cartridge into 406 cylinders utilizing 16 sectors and two surfaces. This drive is unique in that the software considers one RK05F as two logical 203 track disk drives. The sector format, however, is identical to that of the RK05J drive.

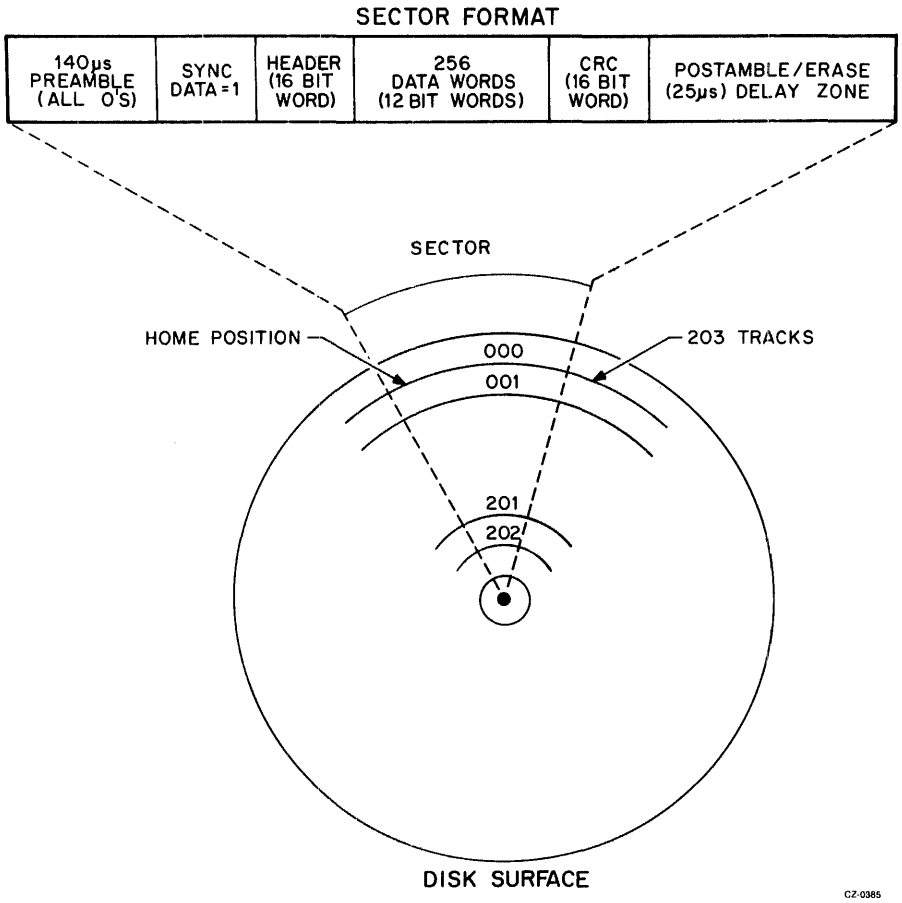


Figure 5-4 Sector Format

A sector consists of the items listed below.

- A preamble consisting of 140 microseconds of all zero data bits to allow time before detecting sync.
- A sync bit which is a single data bit equal to a 1, that is used to indicate that the next area is the header word.
- A 16-bit header word containing the cylinder address arranged as 5 zero bits, an 8-bit cylinder address, and 3 more zero bits..
- A data area consisting of 256 12-bit data words..
- A 16-bit CRC character.
- A 25 microsecond postamble delay zone used to allow a delay prior to the next sector pulse.

SUMMARY

RK8-E Registers

The RK8-E contains two types of registers.

- Loaded or read by user software
- Transparent to user software

The registers which are loaded and read by user software can only be accessed by using IOT instructions.

- Command register enables all functions (read, write, seek), selects a drive, selects a memory field, enables interrupts, determines number of words to be transferred and provides the most significant cylinder address bit.
- Current address register (and 3 bits of the command register) combine to make up a 15-bit memory address register that selects a memory address via the OMNIBUS during a data transfer.
- Disk address register (and one bit of the command register) combine to select a sector, cylinder and surface to be used during a data transfer.
- Status register contains information needed by the program to evaluate the operational status of the RK8-E and RK05.

The remaining registers are transparent to the user software.

- Data buffer register is a four word buffer used to compensate for the data rate timing differences of the OMNIBUS and the disk bus. All data passes through this buffer which also serves as a serializer/deserializer.

- CRC register is a 16-bit register used to calculate the CRC character.

- Major state register is the control sequencer of the RK8-E; with its associated circuitry, it performs the major portion of control functions of the RK8-E and determines the format of the disk (preamble, header, data, CRC and postamble).

- Divide by 12 bit and 16 bit counters are responsible to the major state logic for the determination of the various word lengths found in a sector. To advance from one major state to the next, the bits in a word must be counted. When a whole word has been counted as being read or written, an incrementing pulse is applied to the module 128 or 256 word counter.

- The divide by 128 or 256 word counter receives the output of the divide by 12 bit counter so that the length of a sector may be calculated when writing or reading data. This counter overflows at a count of 128 or 256 as determined by the half-block bit (bit Ø5 of control register).

Disk and Sector Format

The disk surface of an RKØ5J is divided into 2Ø3 tracks and 16 sectors. Each surface has one read/write head. Each sector has the format described below.

- A preamble consisting of 14Ø microseconds of all zero bits

- A sync bit consisting of a single data bit equal to a 1

- A 16-bit header word containing the cylinder address

- A data area consisting of 256 12-bit data words

- A CRC character consisting of one 16-bit check word

- A 25 microsecond postamble area used for a delay prior to the next sector pulse

MODULE EXERCISE

Using the program listed below, write in the REMARKS column what each instruction is doing. You may only use your PDP-8 programming card as a reference. You have 20 minutes to complete this exercise.

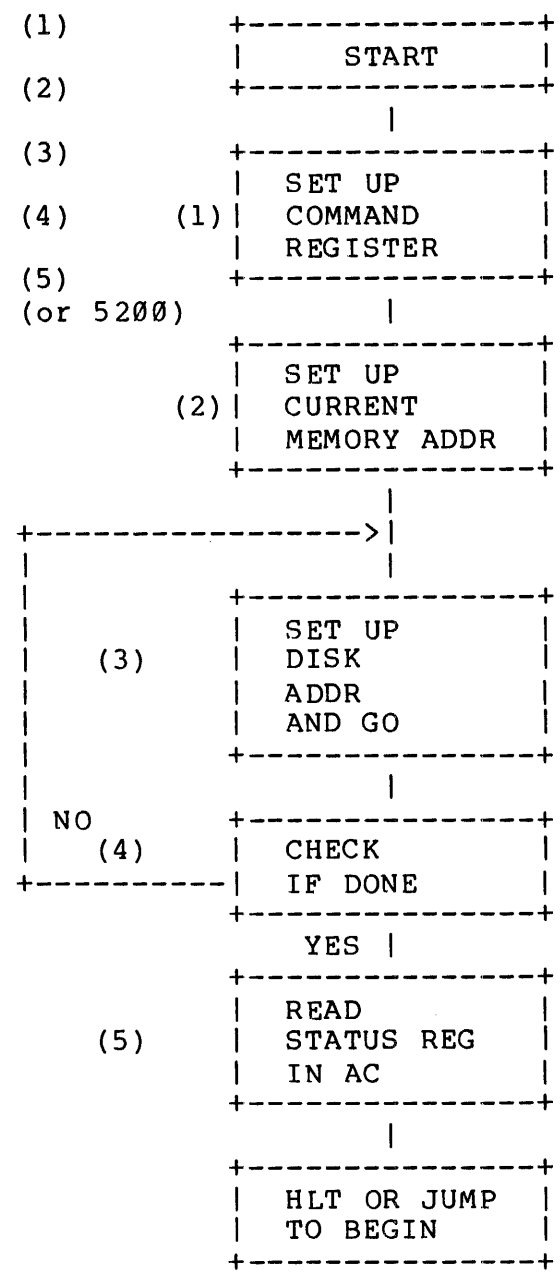
Memory Location	Remarks	Instruction
0200		1213
0201		6746
0202		1214
0203		6744
0204		1215
0205		6743
0206		6741
0207		5206
0210		6745
0211		7402 (or 5200)
0212	CMD REG = 4101	
0213	CURRENT ADDR = 5000	
0214	DISK ADD > 2434	

RK8-E SUBSYSTEM REGISTERS/COMMANDS

MODULE EXERCISE SOLUTIONS

The program below will write 128_{10} words from memory location 5000 to disk 0, cylinder 258_{10}, sector 14 of surface 1 and halt with status register in the AC (write all 1s).

Memory Location	Remarks	Instruction
0200	TAD CMD REG	1213
0201	DLDC	6746
0202	TAD CURRENT ADDR	1214
0203	DLCA	6744
0204	TAD DISK ADDR	1215
0205	DLAG	6743
0206	DSKP	6741
0207	JMP-1	5206
0210	DRST	6745
0211	HLT (or JMP 200)	7402
0212	CMD REG = 4101	
0213	CURRENT ADDR = 5000	
0214	DISK ADDR = 2434	



Now that you have completed this exercise, you can take the module test. The course administrator has the answers to the test.

RKØ5 DISK SUBSYSTEM MAINTENANCE

RK8-E Theory of Operation

RK8-E THEORY OF OPERATION

INTRODUCTION

In previous lessons, you studied the basic function of the modules that make up the RK8-E Controller. You have also studied the types of registers in the RK8-E, and the different functions or commands this device can execute. This information you have studied is important and will help you in studying this lesson.

The purpose of this lesson is to present the theory of operation of the RK8-E. This lesson uses a functional block diagram with mnemonics referencing field maintenance print set pages. This will enable you to easily correlate the block diagram to the logic diagrams in the print set if you so desire.

OBJECTIVES

Upon completion of this lesson, you will be able to describe the function of the major blocks within the functional block diagram. To demonstrate your ability to complete the objective you will be required to match 8 out of 10 definitions with their circuit name correctly. Time allowed to complete the test is 10 minutes.

ADDITIONAL RESOURCES

PDP8/E, F, M Maintenance Manual Volume 3, Chapter 11, Page 11-54 to 11-99	DEC 8E HMM3A-C-D
RK8JE Disk Drive Controller Print Set	MP-ORK8J-EO

BLOCK DIAGRAM

The RK8-E functional block diagram (Figure 6-1) gives you an overall view of the theory of operation of the RK8-E. The block diagram shows the major circuitry on each of the three modules which make up the RK8-E. The block diagram is described on a module by module basis with each block within a module being described.

The RK8-E Controller consists of the following modules and major logic circuits.

- Data buffer and status module (M7104)
  - I/O bus (MD bus)
  - Instruction decoder
  - Data buffer
  - Bus control logic
  - Status register
  - Data/status multiplexer
- Major registers module (M7105)
  - Data break control logic
  - Current address register
  - Command register
  - CRC and cylinder address register
  - Drive selection and cylinder address logic
- Control module (M7106)
  - Sector/surface register
  - Sector address comparitor
  - Major state register
  - Read/write control logic
  - Bit and word counters

Each of these major logic circuits are described below.

M7104 DATA BUFFER AND STATUS MODULE

The M7104 module is used to control data transfers and perform instruction decoding.

I/O Bus Control Logic

The I/O bus control logic buffers the MD 00-11 lines of the OMNIBUS (MD BUS), and contains the interrupt and skip logic. The bus control logic is used for program control and generates timing signals to allow register access and program control.

Instruction Decoder

The instruction decoder receives input from the MD BUS and decodes the instructions desired by the program. Signals will be generated which will load the RK8-E registers.

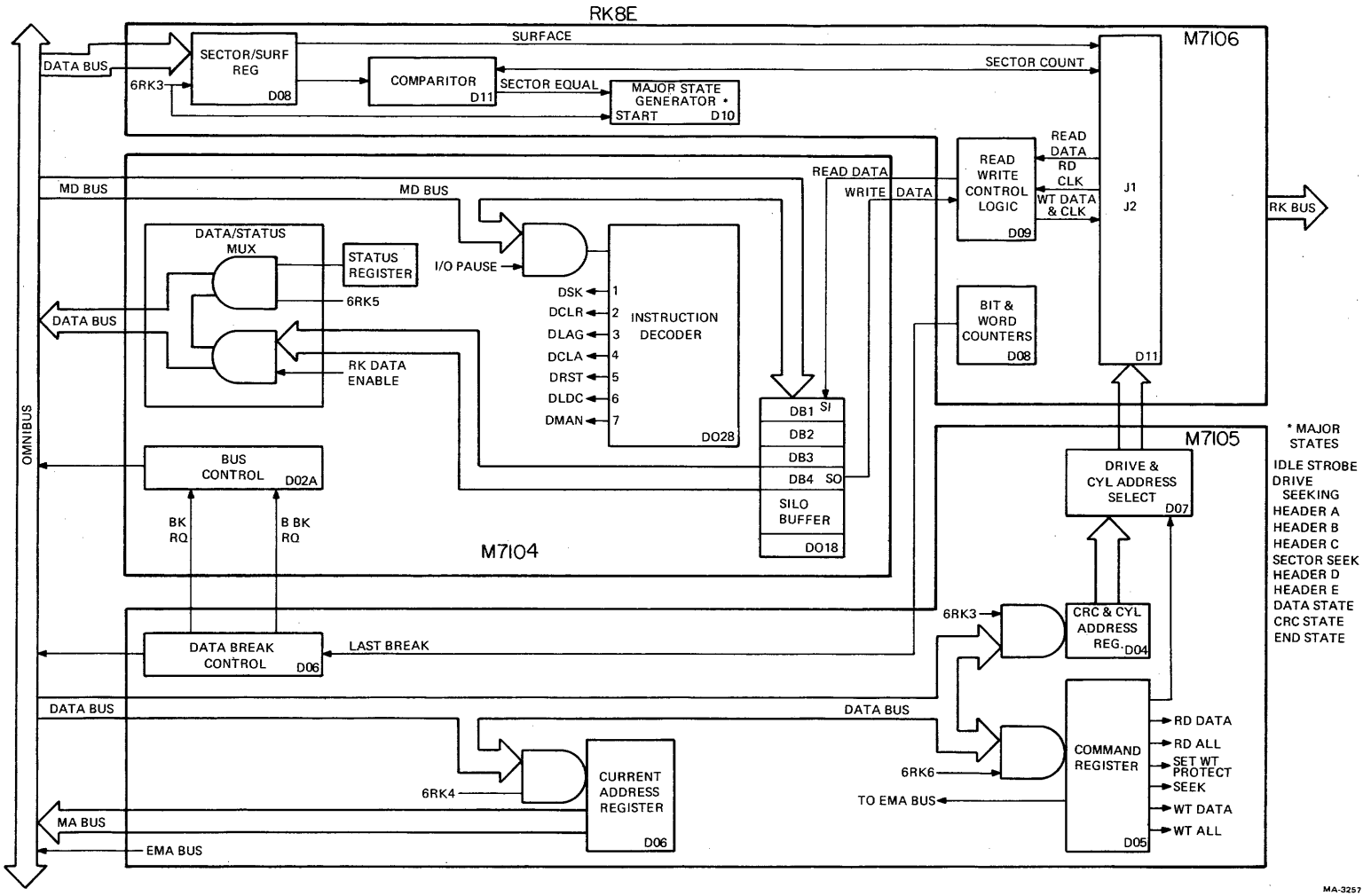


Figure 6-1 RK8-E Block Diagram

Data Buffer

The data buffer provides four buffering registers (DB1 - DB4) for temporary storage of data that is being transferred between memory and the drive. This buffer compensates for timing differences in the data transfer rates of the OMNIBUS and the I/O bus.

During a write operation, parallel data (MDØØ - MD11) are received from the OMNIBUS and applied to DB1. The parallel data words are moved through the other locations (DB2, 3, and 4) as the disk logic writes on the platter surface. Location DB4 of the buffer serializes the data for use by the selected drive.

During a read operation, serial data from the disk is shifted into DB1 and parallel-transferred to the other locations as single cycle data breaks to memory occur. The parallel data from DB4 is transferred to the data status multiplexer before being sent to memory via the data bus.

Status Register

The status register provides current status of the RK8-E and the selected drive to the program. The contents of the status register are transferred to the AC for evaluation by the program if the 6745 (DRST) instruction is executed by the program. The status register supplies input to the data/status multiplexer and its output is transferred to the AC via the data bus.

Data/Status Multiplexer

The data/status multiplexer allows either the information from the status register or the data from DB4 to be placed on the data bus for transferral to memory via the OMNIBUS.

M7105 MAJOR REGISTERS MODULE

This module performs the tasks listed below.

- Memory addressing for single cycle data breaks
- Drive selection
- Function decoding
- Cylinder selection
- CRC character calculation and generation

The data break control logic determines the break priority of the RK8-E. It also controls the direction of the data transfer (to or from memory) and selects a location in memory for the data transfer.

The data break control also sends a DATA LATE error signal to the status register if the processor does not respond to a BRK RQST within 22.5 microseconds.

The current address register contains the initial memory address to be used in a data transfer. The register is loaded from the AC using a DLCA instruction. The current address register is incremented after each data break and applied to the memory address (MA) lines to sequentially select memory locations for data transfers. The memory field (EMA) to be used is selected by the command register and is not incremented when the current address register is incremented.

The command register performs the tasks listed below.

- Selects a disk function for execution.
- Selects a disk drive unit (1 of 4).
- Selects a memory field for data transfers (1 of 7).
- Enables interrupts.
- Provides the most significant cylinder address bit.
- Determines the number of words to be transferred (128 or 256).

The command register is loaded from the AC by a 6746 (DLDC) instruction.

The CRC and cylinder address register is a 16-bit register which performs the tasks listed below.

- Receives the cylinder address from the AC when the DIAG (GO) instruction is executed by the program.
- Transfers the cylinder address to the drive and cylinder address select circuitry.
- Computes a 16-bit CRC character which is written at the end of a block during a write operation.
- Computes a 16-bit CRC character which is compared with the CRC character read from the disk during a read operation.

The drive selection and cylinder address logic is used to transfer the drive select code and cylinder address to the drive via drive signal cable J2. The drive select code determines which drive is on-line. The cylinder address is sent to a selected (on-line) drive as a destination address for seeks.

M7106 CONTROL MODULE

The circuitry on this module is responsible for the tasks listed below.

- Comparing sector addresses
- Reading/writing of data
- Selecting the major states of the RK8-E

Comparing Sector Addresses

The sector/surface register receives the surface bit and sector address to determine where the data is to be written or read. The surface bit is sent to the drive via cable J1. The sector address is sent to a comparator to be compared with the sector count coming from the drive. When they compare, the signal sector equal (actual sector equals desired sector) advances the major state register.

Reading/Writing of Data

The read/write control logic controls the reading or writing of data onto or from the disk surface. Data read from the disk is clocked in by read clock pulses supplied by the drive. The read data is shifted by the read/write control logic to the data buffer.

Data to be written is combined with the output of the crystal oscillator and encoded by the read/write control logic into frequency modulated data. This data is shifted to the disk for writing.

The clock logic consists of a crystal oscillator which outputs a frequency of 2.88 MHz for the RK05/RK8-E subsystem.

The bit and word counter logic consists of the four counters listed below.

- Divide by 16 bit counter
- Divide by 12 bit counter
- Divide by 128 or 256 counter
- Break counter

The divide by 16 counter counts the bits in the header word or CRC character as they are read or written. The major state register uses the output of this counter to advance into the data or end state.

The divide by 12 counter counts the bits of data as they are being read or written. Each time 12 bits (one PDP-8 word) are read or written, the 128 or 256 counter is incremented.

The divide by 128 or 256 counter is incremented by the output of the divide by 12 counter. The signal LAST WORD H is asserted after 256 words (one sector) has been read or written. If bit 5 in the command register is set, data transfers stop after the 128th word. However, the drive continues to read data or write zeros until the sector has been completely read or written. This data is not transferred to memory.

The read or write operation completes a sector in order to check or write the CRC character. The output of the divide by 128 or 256 counter (last word or 128th word) is applied to the major state register to advance into the checksum major state.

The break counter counts the number of single cycle data breaks that occur during a data transfer operation. If 128 words are to be read or written (indicated by bit 5 of the command register being set), then the signal LAST BRK is asserted at the count of 128. If bit 5 of the command register is not set, the signal LAST BRK does not stop the read or write operation until all 256 words in the sector are transferred.

Major State Selection

The major state register controls each phase that the RK8-E progresses through during a seek, read or write operation. Each major state causes specific logic operations to be performed. The output of this register corresponds to each area of a sector.

The major state register uses the output of the bit counters and the 128 or 256 word counter as conditions to advance to another state. Since not all functions require all possible major states, another condition to advance the state register is the function being performed.

J1 AND J2 CONNECTORS

One 70-09026 cable is used to connect the RK8-E controller to the first RK05 Drive. The 70-09026 cable is connected from the two Berg connectors on the M7106 module, to slots A07-A08 or B07-B08 on the drive closest to the controller. Table 6-1 gives the signal names and descriptions of each signal from J1 and Table 6-2 lists and describes the signals from J2.

NOTE

The signal name in parentheses following each description in these tables is the signal name as it appears in the RK05 print set.

Table 6-1 RK8-E - RKØ5 Interface Cable (J1)

Connector J1 on RK8-E Pin No.	Signal	Description
A	Not used	
B	Not used	
C	GND	
D	DSK DATA IN L	Serial data from the drive (BUS READ DATA L).
E	GND	
F	DSK RD CLK L	Clock pulses from the selected drive generated during read operations (BUS READ CLOCK L).
H	GND	
J	DSK WRT PROTECT L	Indicates that the selected drive is write protected (BUS WRITE PROTECT STATUS).
K	GND	
L	DSK READ L	Enables the selected drive to transfer read data to the controller (BUS READ GATE L).
M	GND	
N	Not used	
P	GND	
R	DSK WRT STATUS L	Indicates the drive has sensed one or more fault conditions (BUS WRITE CHECK).
S	GND	
T	DSK SECTOR MK L	Indicates a disk sector mark has been detected from the selected drive (BUS SECTOR PULSE L).
U	GND	

Table 6-1 RK8-E - RKØ5 Interface Cable (J1) (Cont)

Connector J1 on RK8-E Pin No.	Signal	Description
V	DISK FILE RDY L	Indicates that the selected drive is ready to read or write data (BUS FILE READY L).
W	GND	
X	DSK HEAD SEL 1	Indicates that the lower surface of the disk cartridge is selected. If unasserted, the upper surface is selected (BUS HD SELECT).
Y	GND	
Z	DSK INDEX MK L	Indicates that a disk index mark from the selected drive has been detected (BUS INDEX PULSE).
AA	GND	
BB	DSK WRT ERASE GATE L	Commands the drive to enable the write and erase logic. When unasserted, the disk will read (BUS WRITE GATE L).
CC	GND	
DD	DSK SEC 1 L	Disk sector address bit Ø from the selected drive (BUS SECTOR ADDRESS Ø L).
EE	GND	
FF	DSK SEC 4 L	Disk sector address bit 2 from the selected drive (BUS SECTOR ADDRESS 2 L).
HH	GND	
JJ	Not used	
KK	GND	
LL	DSK SEC 8 L	Disk sector address bit 3 from the selected disk drive (BUS SECTOR ADDRESS 3 L).

Table 6-1 RK8-E - RKØ5 Interface Cable (J1) (Cont)

Connector J1 on RK8-E Pin No.	Signal	Description
MM	GND	
NN	Not used	
PP	GND	
RR	DSK STROBE L	Enables the disk logic to receive a new cylinder address (BUS STROBE L).
SS	GND	
TT	Not used	
UU	GND	

Table 6-2 RK8-E - RKØ5 Interface Cable (J2)

Connector J2 on RK8-E Pin No.	Signal	Description
A	GND	
B		
C	DSK CAP EX L	Indicates that the address sent to the selected disk drive was greater than 312 octal (BUS ADDRESS INVALID L).
E	DSK SEEK FAIL	Indicates that the disk failed to seek to the address specified (BUS SEEK INCOMPLETE).
F	GND	
H	DSK ACKNOWLEDGE L	Indicates that the disk has received and acknowledged the new cylinder address (BUS ADDRESS ACCEPTED).
J	GND	
K	DSK SEC 2 L	Disk sector address bit 1 from the selected disk drive (BUS SECTOR ADDRESS 1).

Table 6-2 RK8-E - RKØ5 Interface Cable (J2) (Cont)

Connector J2 on RK8-E Pin No.	Signal	Description
L	GND	
M	DSK DRIVE 3 L	Controller drive select code bit 3 (BUS SELECT 3 L).
N	GND	
P	DSK RESTORE L	Recalibrate the selected disk drive by moving the positioner to cylinder ØØ (BUS RESTORE L).
R	GND	
S	DSK DRIVE 2 L	Controller drive select code bit 2 (BUS SELECT 2 L).
T	GND	
U	DKS CYL ADD 4 L	Drive cylinder address bit 2 (BUS CYL ADD 2 L).
V	GND	
W	DSK DRIVE 1 L	Controller drive select code bit 1 (BUS SELECT 1 L).
X	GND	
Y	DSK CYL ADD 1 L	Disk drive cylinder address bit Ø (BUS CYL ADD Ø L).
Z	GND	
AA	DKS DRIVE Ø L	Controller drive select code bit Ø (BUS SELECT Ø L).
BB	GND	
CC	DSK CYL ADD 32 L	Disk drive cylinder address bit 5 (BUS CYL ADD 5 L).
DD	GND	
EE	DSK RDY S/R/W L	Selected disk drive is ready to read, write or seek to a new address (BUS R/W/S READY L).
FF	GND	

Table 6-2 RK8-E - RK05 Interface Cable (J2) (Cont)

Connector J2 on RK8-E Pin No.	Signal	Description
HH	DSK CYL ADD 128 L	Disk drive cylinder address bit 7 (BUS CYL ADD 7 L).
JJ	GND	
KK	DSK WRT CLK DATA L	Write clock and data to be written on the disk (BUS WRITE DATA and CLOCK L).
LL	GND	
MM	DSK CYL ADD 16 L	Disk drive cylinder address bit 4 (BUS CYL ADD 4 L).
NN	GND	
PP	DSK CYL ADD 64 L	Disk drive cylinder address bit 6 (BUS CYL ADD 6 L).
RR	GND	
SS	DSK CYL ADD 2 L	Disk drive cylinder address bit 1 (BUS CYL ADD 1 L).
TT	GND	
UU	DSK CYL ADD 8 L	Disk drive cylinder address bit 3 (BUS CYL ADD 3 L).
VV	GND	

SUMMARY

The RK8-E Controller consists of three modules which plug into the OMNIBUS.

- M7104 - Data buffer and status module
- M7105 - Major registers module
- M7106 - Control module

The circuitry on the M7104 consists of the items listed below.

- I/O bus (MD bus) buffers the OMNIBUS MD 00-11 lines and supplies information to the instruction decoder or data buffer.

- Instruction decoder receives data from MD bus in order to decode instructions and generate signals for register accessing.

- Data buffer provides temporary storage of data being transferred between memory and the disk drive.

    - Write operation - Parallel data from the MD BUS is applied to DB1 and sequenced through DB2, DB3 and DB4. The data from DB4 is shifted to the drive as serial data.

    - Read operation - Data from the disk drive is shifted serially into DB1 and sequenced through DB2, DB3 and DB4. Parallel data from DB4 is transferred to the data/status multiplexer and sent out via the data bus.

    - Status register - Provides current status of RK8-E and the selected drive to the program.

    - Data/status multiplexer - Allows either status from the status register or data from DB4 to be transferred over the data bus to memory.

    - Bus control - Used for program control and register access.

The circuitry on the M7105 is used for memory addressing, command execution, cylinder addressing, drive selecting and CRC generation.

- Data break control - Used to determine the priority of the RK8-E and to control the direction of data transfers.

- Current address register - Used to contain the initial memory address for data transfers. It is incremented after each data break and the new address is sent over the memory address lines to sequentially select a memory location for the next data transfer.

- Command register has five functions.

    - Contains the command to be executed.
    - Selects a disk drive (1 of 4).
    - Selects a memory field (1 of 7).
    - Enables interrupts.
    - Contains the MSB for cylinder address.

- CRC and cylinder address register has four functions.

    - Receives the new cylinder address from the AC via DIAG instruction.

- Transfers the cylinder address to the drive.
- Computes a 16-bit CRC character which is written at the end of the sector.
- Computes a 16-bit CRC character which is compared with the CRC character read from the disk.

- Drive selection and cylinder address logic - Used to transfer the drive number and cylinder address to the drive.

The circuitry on the M7106 module consists of the items listed below.

- Sector/surface register - Receives the sector address and surface bit for the selected drive. The surface bit is sent to the drive to select one of the two heads. The sector address is sent to an address comparator.

  The comparator is used to compare the sector address with the current sector count generated by the disk. When the sector address and the current sector count are equal, the comparator outputs SECTOR EQUAL and sends it to the major state register.

- Bit and word counters - These counters keep track of word lengths and sector boundaries for use by the major state register.
  - A divide by 12 counter counts the bits in a data word.
  - A divide by 16 counter counts the bits in the header word and CRC character.
  - A divide by 128 or 256 counter counts the words in a sector to determine the sector boundary for the major state register. Bit 5 of the control register commands the 128 or 256 counter logic to output a half-block signal for the break counter.
  - A break counter counts the single cycle data breaks. This counter, in combination with bit 5 of the control register, commands the logic to terminate the data transfers at 128 words.

- Major state register - Controls each phase the RK8-E progresses through during a seek, read or write.

- Read/write control logic - Controls the reading and writing of data.

J1 and J2 connectors - Two Berg connectors on the M7106 module connect the 70-09026 interface cable (RK BUS) to the closest RK05.

Now that you have completed this module, you can take the module test. The course administrator has the test answers.

RK05 DISK SUBSYSTEM MAINTENANCE

RKØ5 Theory of Operation

RKØ5 THEORY OF OPERATION

INTRODUCTION

In previous modules you studied the controllers used with the RKØ5 family of disk drives. You have also studied the physical layout of, and the differences between, the three types of RKØ5 drives. Now, this module describes the RKØ5 theory of operation. This module includes the topics listed below.

- Drive controller interfacing
- Logic module functionality
- Index/sector detection
- Cylinder addressing
- Servo system functionality
- Servo positioner functionality
- Read/write control

To aid in the description of the above listed topics, a block diagram is included which shows the overall flow of signals in the RKØ5 drive. In addition, there are simplified block diagrams which show the servo and positioner systems.

The text does not use the field maintenance print set to describe individual circuits, but you can use the block diagrams to reference modules or circuits contained within the print set.

OBJECTIVES

At the completion of this module, you will be able to describe the function of the items listed below.

- Interface cable
- Interfacing signals
- Each drive logic module
- Servo system

To demonstrate your ability to do this, you will be given a series of true-false questions. You will be required to correctly answer 8 out of 1Ø questions within 1Ø minutes. You may use any reference material available.

ADDITIONAL RESOURCES

RKØ5/RKØ5J/RKØ5F Disk Drive Maintenance Manual	EK-RK5JF-MM-ØØ1
Field Maintenance Print Set DECpack Assembly	MP-ORKØ5J-Ø
RKØ5 Disk Drive User's Manual	EK-RKØ5-OP-ØØ1

RKØ5 INTERFACE

The RK11/RK8-E Controllers communicate with the drive via an interfacing cable. This cable plugs into card position 7 or 8 of the logic assembly in the RKØ5. Figure 7-1 shows each signal line including the direction of signal flow. Figure 7-1 is followed by a brief description of each signal.

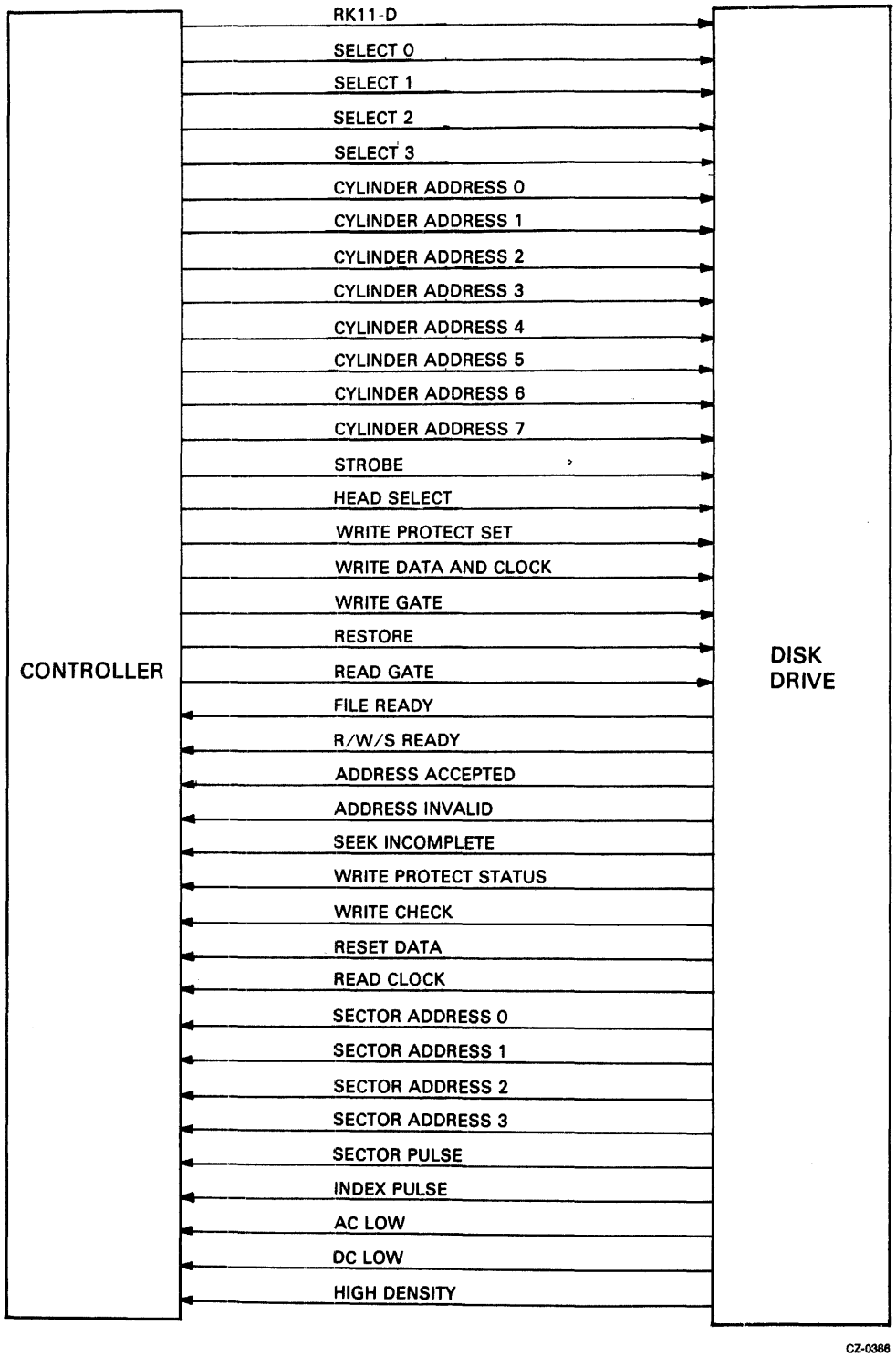


Figure 7-1 Controller/Drive Interface Lines

Input Interface Lines

BUS RK11D L configures the drive select logic to operate with a particular type of controller. This line negated indicates that the controller is not an RK11D (i.e., the controller may be an RK8-E, which can control only four drives on a single bus). BUS RK11D L asserted indicates that the controller is an RK11D.

BUS SEL Ø-3 L operates in conjunction with the RK11D interface line and an eight-position address select switch on the M77ØØ/M768Ø card. Together, these signals determine the drive selection by one of the two methods listed below.

- With the RK11D line asserted, the M77ØØ/M768Ø selection circuitry is configured to decode the lower three select lines as a binary number. To select a drive, the controller places a 3-bit binary code corresponding to the desired drive number, on the select lines. This binary code is then translated by a decoder to activate only one of the eight address select switch positions.

- With the RK11D line negated, the M77ØØ/M768Ø selection circuit is configured to use the four select lines differently. In a specific drive, only one of the four lines is internally connected (via positions Ø through 3 of the address select switch) to the drive control logic. To select a drive, the controller asserts only one of the four select lines. This line remains asserted throughout the entire data transfer or control operation.

BUS STROBE L enables the cylinder address or restore line to be received by the drive. The controller asserts the strobe line after the cylinder address or the restore command is settled on the interface.

The strobe line remains asserted until either the ADDRESS ACKNOWLEDGED or the ADDRESS INVALID signal is returned from the drive.

BUS CYL ADD Ø-7 L specifies the new seek address. In order to move the heads to a desired cylinder, the controller places an 8-bit binary code on the lines (valid codes are Ø through 2Ø2 decimal). These lines are gated by the bus strobe, directing the drive logic to position the heads at the addressed cylinder. The binary code remains on the lines until either the address acknowledged or the address invalid signal is returned from the drive.

BUS RESTORE L (RTZ) commands the disk logic to position the heads to cylinder zero. The controller asserts this line prior to issuing BUS STROBE L. Within two microseconds after this signal is issued, the drive should return ADDRESS ACKNOWLEDGED and clear the address register. The heads will them move to cylinder zero. The restore line remains asserted until the controller receives ADDRESS ACKNOWLEDGED.

BUS HD SELECT L determines which of the two read/write heads the drive is to select. The controller asserts this line to select the upper head, and negates this line to select the lower head. Either signal remains on the line throughout the entire read or write operation.

BUS WRITE PROTECT SET L disables the drive write amplifiers to prevent a write operation. The controller asserts this line to set the write protect flip-flop and inhibit the write capability of the drive. The write protect flip-flop can also be set by the WT PROT switch on the front panel.

BUS WRITE DATA and CLOCK L are multiplexed data and clock pulses encoded in a frequency modulated format sent to the drive.

BUS WRITE GATE L simultaneously turns on both write and erase current sources to the selected head. The controller asserts this line one microsecond prior to transmitting the write data. This line remains asserted throughout the data transmission time.

BUS READ GATE L allows read data to be gated out of the drive and sent to the controller. The controller asserts this line to enable the read clock and read data output lines. This line remains asserted throughout the entire read operation.

Output Interface Lines

BUS FILE RDY L indicates that all the conditions listed below are true.

- Drive operating powèr is correct.
- Disk cartridge is properly inserted.
- Drive front door is closed.
- RUN/LOAD switch is in the RUN position.
- Spindle is rotating at the correct speed.
- Read/write heads are loaded.
- Write check interface line is false.

BUS WT CHK L is asserted to indicate any of the conditions listed below.

- Erase or write current active without WRITE GATE being asserted.
- Inoperative linear positioner transducer lamp.
- Any or all of +15, -15 or +5 Vdc low.

When the WRITE CHECK signal is asserted, all external commands to the drive are suppressed and the FAULT indicator on the drive control panel lights. If the fault condition is temporary, the operator may turn off the FAULT indicator by pushing the WT PROT switch. This action, however, causes the WT PROT indicator to light; the WT PROT switch must be pushed again to turn off the WT PROT indicator.

BUS R/W/S RDY L is asserted to indicate that the drive is in the file ready condition and is not performing a seek operation (on cylinder). When this line is negated, the drive is either cycled down (heads unloaded) or in the process of performing a seek operation (moving the heads).

BUS ADDRESS ACCEPTED L is a five microsecond pulse that indicates the drive has accepted a seek command with a valid address and command execution has begun.

BUS ADDRESS INVALID L is a five microsecond pulse that indicates the drive has received a nonexecutable seek command containing a cylinder address greater than 2Ø2 (decimal). In this case, the seek command is suppressed and the heads do not move.

BUS SEEK INCOMPLETE L indicates that some drive malfunction did not allow the seek operation to be completed. BUS SEEK INCOMPLETE remains asserted until a restore command is received or the operator sets the RUN/LOAD switch to LOAD and then back to RUN.

BUS WRITE PROTECT STATUS L indicates that the write capability of the drive is inhibited (i.e., the drive is write-protected). When this line is asserted, the WT PROT indicator on the drive control panel is on. This line may be asserted because the front panel switch has been pushed, or the BUS WRITE PROTECT SET line was asserted from the controller.

BUS READ DATA L is data read from the disk, consisting of 16Ø nanosecond pulses.

BUS READ CLOCK L consists of 16Ø nanosecond clock pulses that strobe the BUS RD DATA to the controller.

BUS SECTOR ADDRESS Ø-3 L indicates the sector address that is passing under the heads. The sector address is a 4-bit binary code derived from the sector address counter.

BUS SECTOR PULSE L is a one microsecond pulse that occurs each time a sector slot passes the sector transducer. The index slot is suppressed in this line and is transmitted on the index pulse line.

BUS INDEX PULSE L is a one microsecond pulse that occurs once for each revolution of the disk. The index pulse occurs 6ØØ microseconds after the last sector pulse and is generated each time the index slot is detected by the sector transducer.

BUS AC LOW L indicates a loss of drive ac power. The line is asserted when there is a loss (for more than 45 milliseconds) of the 3Ø Vac within the drive. When ac low occurs, the drive finishes reading/writing the current sector, then initiates a normal head-retract and unload cycle. If a total power loss occurs before the heads are completely retracted, the safety relay is de-energized to retract the heads under battery power (emergency retract).

BUS DC LOW L indicates a low dc voltage condition. The line is asserted when the ±15 Vdc within the drive drops below 12 Vdc. When dc low is generated, the safety relay is de-energized to retract the heads under battery power (emergency retract). Since the RUN gate of each drive is connected to the dc low bus, a dc low signal from any one drive in a multidrive system disables all the drives in the system.

BUS HIGH DENSITY L indicates that a high density drive (2ØØ tracks/inch) is on-line to the controller. This line is normally asserted, indicating an RKØ5 is present. On older systems, the low-density RKØ3 will negate this line.

RKØ5 BLOCK DIAGRAM

Figure 7-2 shows the signal paths to and from each logic card. It also shows several relays and interlocks in the RKØ5. The text below describes the function of each logic card, relay and interlock.

The G18Ø module contains the logic required for head selection and reading and writing of data. The read/write heads are connected, via cables, to this module. The G18Ø module occupies slot 1 of the logic assembly.

The M77ØØ/M768Ø module contains logic to control the items listed below.

- Index/sector detection
- Drive selection
- Seeking
- Output interface line drivers

The M77ØØ module has been replaced by the M768Ø module. These modules perform the same functions except that the M768Ø module has an additional set of switches that differentiate an RKØ5J from an RKØ5F. The M77ØØ/M768Ø module occupies slot 2 of the logic assembly.

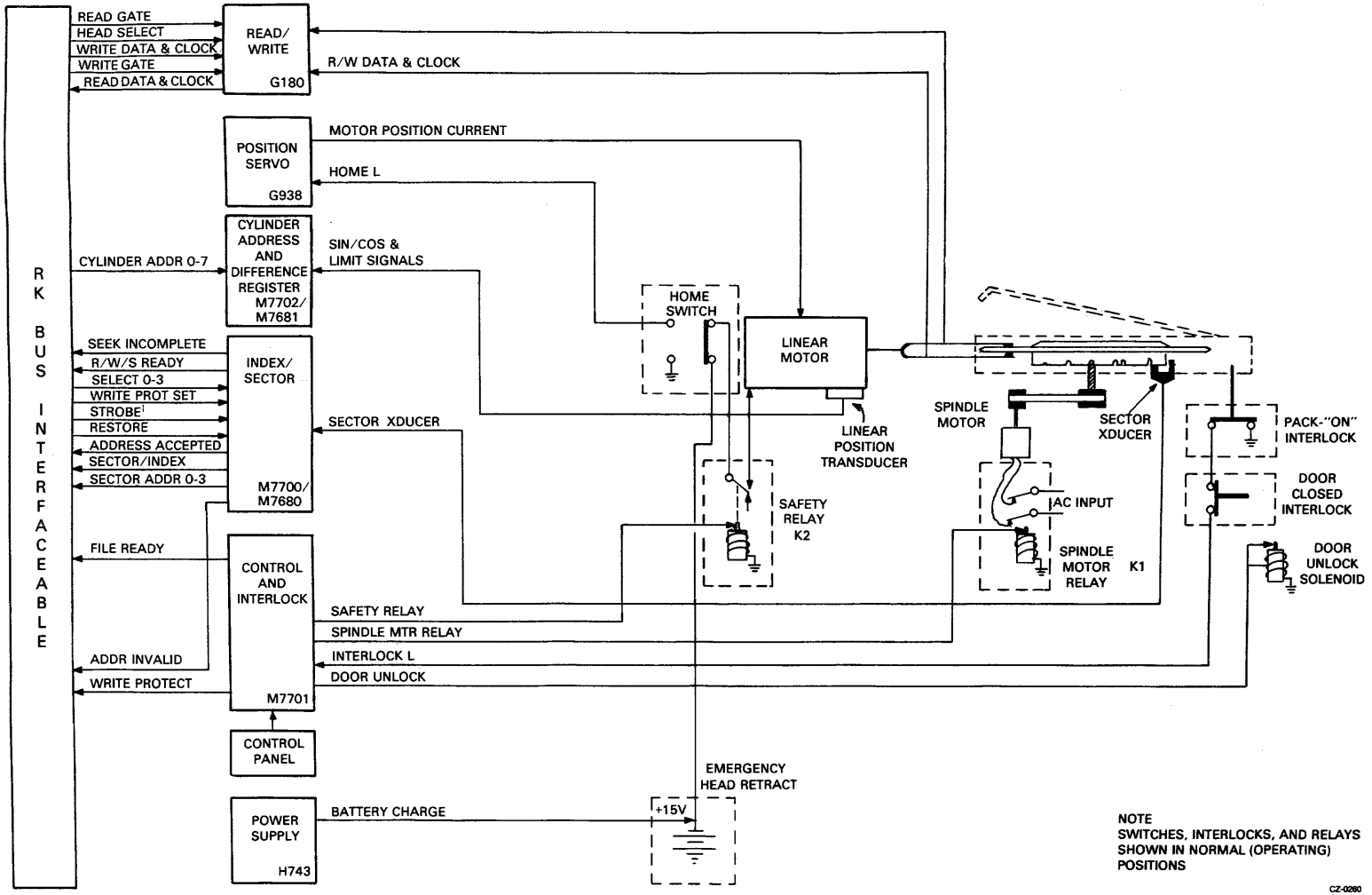


Figure 7-2 RKØ5 Block Diagram

RKØ5 THEORY OF OPERATION

The M77Ø2/M7681 module is primarily used to calculate the difference between the present cylinder address and the desired cylinder address. (The M77Ø2 module has been replaced by the M7681 module.) These modules perform the same function, except that the M7681 contains a switch that differentiates an RKØ5J from an RKØ5F.

The cylinder difference decode IC occupies either position E1 or E2 on the module. The IC is an 8223 and is placed into socket E1 if the device is an RKØ5J, and socket E2 if the device is an RKØ5F.

This module occupies slot 3 of the logic assembly.

The M77Ø1 module monitors the drive interlocks during drive start-up and controls the indicators on the front panel. This module occupies slot 4 of the logic assembly.

The G938 positioner servo module controls the carriage movement, utilizing two control loops in the servo system.

- Velocity loop - controls the carriage velocity during seek operations
- Detent loop - electronically detents the heads at the desired cylinder when the seek operation is completed

The G938 module occupies slot 5 of the logic assembly.

The control panel has two switches and eight indicators that are used to start and stop the drive and give visual indications of drive operation.

The power supply supplies the required voltages for the drive. It consists of three voltage regulators: +5 Vdc, +15 Vdc and -15 Vdc. The power supply is located in the left-rear area of the drive.

The spindle motor relay (K1) applies power to the spindle motor to rotate the disk platter if all of the conditions listed below are met.

- RUN/LOAD switch is in RUN position.
- Power supply voltages are OK.
- Cartridge is installed properly.
- Carriage is home.
- Drive front door is closed.
- Drive door lock is energized.

The safety relay (K2) causes the logic to retract the heads if dc power is lost. The relay allows the battery pack to power the positioning logic to unload the heads.

The pack on interlock is energized when a cartridge is properly inserted into the cartridge-handling system.

The door-closed interlock is enabled when the conditions listed below are met.

- Front door is closed.
- Door locking solenoid is de-energized.
- Door lock has locked the front door.

The door unlock solenoid de-energizes when the RUN/STOP switch is placed in the RUN position. The solenoid is energized when the RUN/LOAD switch is placed in the LOAD position and the disk has stopped rotating.

The sector transducer is an optical device which generates pulses detected from the slotted hub on the underside of the disk cartridge to the index/sector module.

The linear positioner transducer is an optical device which generates signals (SIN/COS and LIMIT) to the cylinder address/ difference register and the servo position servo modules. These signals help control the movement of the carriage.

The home switch shuts off drive to the positioning system when the heads are fully retracted in the home position. This switch is also an interlock for the drive logic, preventing the spindle motor relay from de-energizing when the carriage is not at the home position. In this case, the position of the heads is unknown, and allowing the disk to spin down under this condition could damage the heads and/or cartridge.

Now that you have studied the overall block diagram and understand the RKØ5 general theory of operation, the text gives you a detailed description, using several illustrations and block diagrams. The topics to be covered are listed below.

- Sector/index generation
- Cylinder addressing
- Servo system block diagram
- Positioner servo
- Read/write control

Sector/Index Generation

Figure 7-3 shows the sector/index timing for the RKØ5 Disk Drive. The text following the illustration describes how the sector/index pulses are generated.

The reading and recording of data with specific formats (e.g., data blocks) on the disk requires a timing scheme related to the rotational position of the disk. The sector transducer is used to relate the data format to the location of the disk.

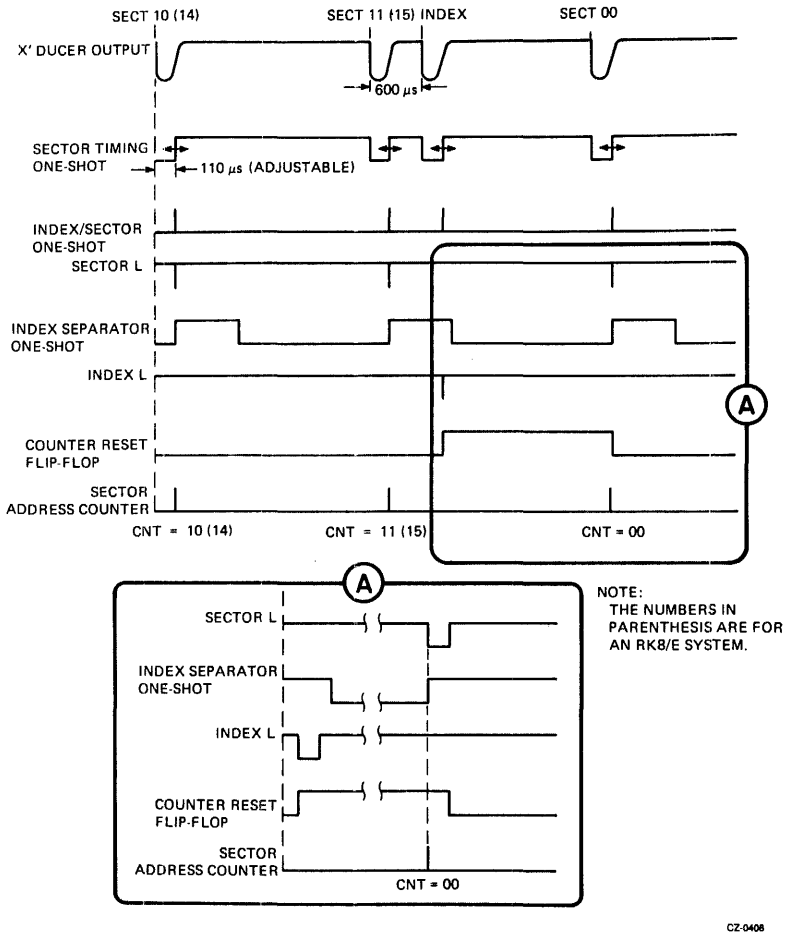


Figure 7-3 Sector/Index Timing

Slots in the recording disk hub pass through a groove in the transducer. Sector and index pulses are generated when the transducer detects light passing through these slots.

There are 12 equally-spaced sector slots (16 slots for an RK8-E), which designate the 12 (or 16) sectors on the disk. There is also one uniquely-spaced slot (index) on the disk. This index slot is located after the last sector to indicate each revolution of the disk.

The sector transducer is located in front of the spindle. It is an optical device that contains a light-emitting diode and a photosensor. As the disk rotates, the slots on the hub pass between the light-emitting diode and the sensor, producing negative SECTOR/INDEX pulses.

Because both the SECTOR and INDEX pulses are produced from a single transducer, logic elements on the M768Ø/M77ØØ are needed to separate these two pulses and to encode the sector address.

During disk rotation, SECTOR/INDEX pulses from the disk trigger a sector timing delay one-shot. The pulse width of this one-shot can be adjusted to compensate for different sector transducer locations among various disk drives. This ensures the proper sector-to-head relationship.

The trailing edge of the sector timing one-shot output triggers the index/sector one-shot, generating a one microsecond INDEX/SECTOR L pulse. The trailing edge of this pulse, in turn, triggers the one millisecond index separator one-shot. The output signal from this one-shot is applied to decoding gates to separate the SECTOR pulses from the INDEX pulse.

If another slot does not pass the transducer while the index separator one-shot is timing out, the SECTOR L signal is produced and the four-stage sector address counter is incremented. This sequence of events is repeated for every sector on the disk hub.

The occurrence of the last SECTOR pulse triggers the index/sector one-shot, as usual. However, 6ØØ microseconds later, the INDEX pulse from the disk hub retriggers the one-shot. The set output from this one-shot is then ANDed with the set output from the index separator one-shot (still high from the previous triggering). The output generates INDEX PULSE L and sets the counter reset flip-flop.

The leading edge of the next SECTOR pulse (sector ØØ) then clears the sector address counter, and the trailing edge of this pulse clears the counter reset flip-flop. Thus, for every revolution of the disk, the counter is cleared to maintain the correct sector address counter-to-disk relationship.

Cylinder Addressing Block Diagram

Figure 7-4 is a simplified block diagram showing how the cylinder difference is calculated. To move the read/write heads to a new location, the drive must perform a seek operation. Note that the drive sees no difference between a programmed seek command and an implied seek (during a data transfer command) from the controller.

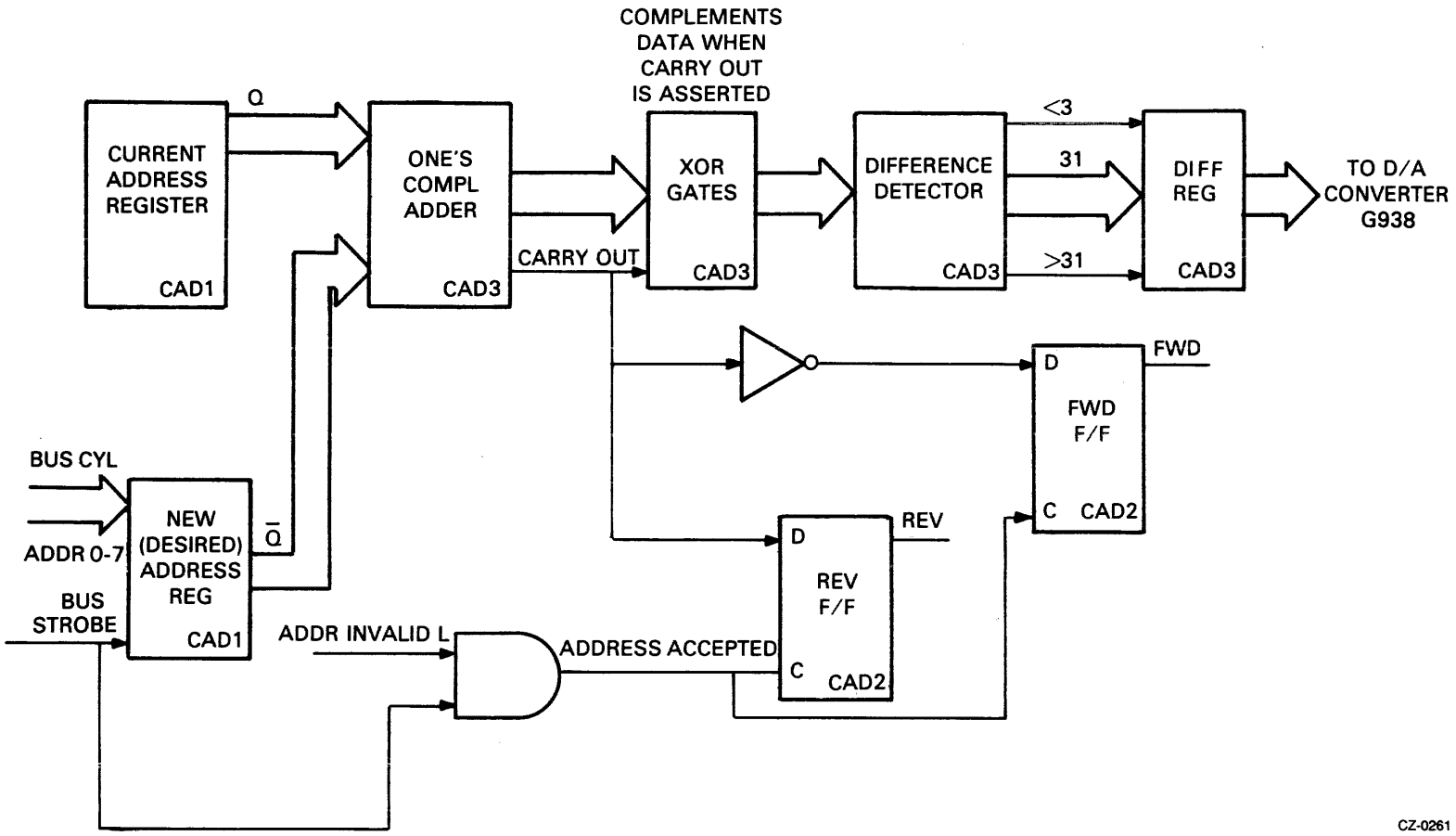


Figure 7-4 Cylinder Addressing Block Diagram

The sequence of events required to calculate the cylinder difference is listed below.

- Current address register contains the current cylinder address of the heads.
- Controller gates the desired cylinder address with bus strobe into the new address register.
- The output of both registers are applied to the 1's complement adder. The desired cylinder address register output is the complement of the desired cylinder.
- The adder result (cylinder difference) is applied to the XOR gates. If the addition process results in a carry, the XOR gates complement the address. The signal carry out then sets the reverse direction flip-flop. If the addition process does not generate a carry, then its absence sets the forward direction flip-flop.

See Table 7-1 for two examples of seeks. The first column shows a one cylinder forward seek, while the second column shows a one cylinder reverse seek.

Table 7-1 Seek Examples

	Forward Seek	Reverse Seek
Current Cylinder Address	ØØØØ	ØØØ1
New Seek Address	ØØØ1	ØØØØ
Current Cylinder Address Input to Adder	ØØØØ	ØØØ1
Complemented New Address Input to Adder	111Ø	1111
Sum	111Ø	ØØØØ
Add Carry Bit	Ø	1
Result of Second Add	111Ø	ØØØ1
Output of XOR (Cylinder Difference)	111Ø	111Ø *

* Carry bit was active in this (and all reverse seek) calculations, causing the reverse direction flip-flop to set and complement the adder result.

- The cylinder difference is then applied to the difference detector. The difference detector produces three types of commands as a result of the seek calculation.

- Low velocity - When cylinder difference is less than or equal to three cylinders.
- Proportional velocity - When cylinder difference is greater than three and less than or equal to 31 cylinders.
- High velocity - When cylinder difference is greater than 31 cylinders.

- The difference output is applied to the digital-to-analog (D/A) converter on the G938 position servo module. The D/A converter changes the selected one-of-three digital velocity commands into a representative analog voltage. This voltage is applied to the linear positioner so that the heads will accelerate.

If the forward flip-flop is set, the heads will move forward (toward the spindle). If the reverse flip-flop is set, the heads will move in a reverse direction (away from the spindle).

SERVO SYSTEM

The servo system uses the output of the difference detector to control carriage movement. Like most disk servo systems, the servo system in the RKØ5 operates in either velocity mode or detent mode. These two modes are described below.

Velocity Mode

During a seek operation, the cylinder address and difference logic computes the digital difference between the present cylinder address and the destination cylinder address. This digital difference is then converted to an analog velocity by the D/A velocity function generator.

The amplitude of the analog signal depends upon the distance to the destination cylinder. If the distance is greater than 31 (decimal) cylinders (or 63 [decimal] cylinders, in the case of an RKØ5F), a maximum velocity command is produced and applied to the velocity control loop. As the carriage accelerates, a feedback velocity signal is generated by the velocity synthesizer. When a speed of 35 inches per second (ips) is attained, this feedback signal inhibits further acceleration and maintains a constant 35 ips carriage speed until the heads are 31 (or 63, RKØ5F) cylinders from the destination cylinder.

From this point, the carriage decelerates at a controlled rate that depends on the decrementing digital difference applied to the function generator.

When the heads are three cylinders (or seven cylinders, RKØ5F) away from the destination cylinder, the velocity generator produces a fixed low-velocity command that continues to move the carriage at low velocity (about three ips) until the heads are approximately one-half cylinder from the destination cylinder.

At this point, the low velocity command is removed. The velocity signal, however, remains to dampen the carriage movement and prevent overshoot.

Once the destination cylinder is reached, the position loop (detent mode) electronically detents the carriage.

Detent Mode

The detent mode of operation electronically retains the read/write heads at the desired cylinder. During this mode, the velocity command from the function generator is zero. This allows a feedback which produces a stable position loop.

If the heads drift from the desired cylinder, an error correction signal is generated that is opposite in polarity from the direction of drift. This feedback is generated by the positioner transducer. The error correction signal is then directly applied through the loop amplifiers, returning the carriage to the desired cylinder.

Figure 7-5 shows the servo system used in the RKØ5. This servo system is composed of the three functional areas listed below.

- A linear positioner transducer that produces two sinusoidal signals. During the velocity mode, these signals control the rate of carriage movement. During the detent mode, only one of these signals is used to electronically detent the carriage. In addition, the transducer also generates two limit signals that indicate the two extremes of carriage travel (INNER LIMIT and OUTER LIMIT).

- A velocity function generator that converts the computed digital difference into corresponding analog velocity commands.

- A velocity synthesizer that generates a servo feedback signal from the positioner transducer.

Each of these three functional areas are described below.

Linear Positioner Transducer

The positioner transducer (located on the underside of the carriage), is an optical device that consists of two parts. Figure 7-6 illustrates the linear positioner transducer. The stationary portion of the transducer is U-shaped and is attached to the carriage slide. One side of the transducer contains a lamp. The other side contains a glass reticle with minute diagonal transparent slots. Six photosensors are located behind the slots.

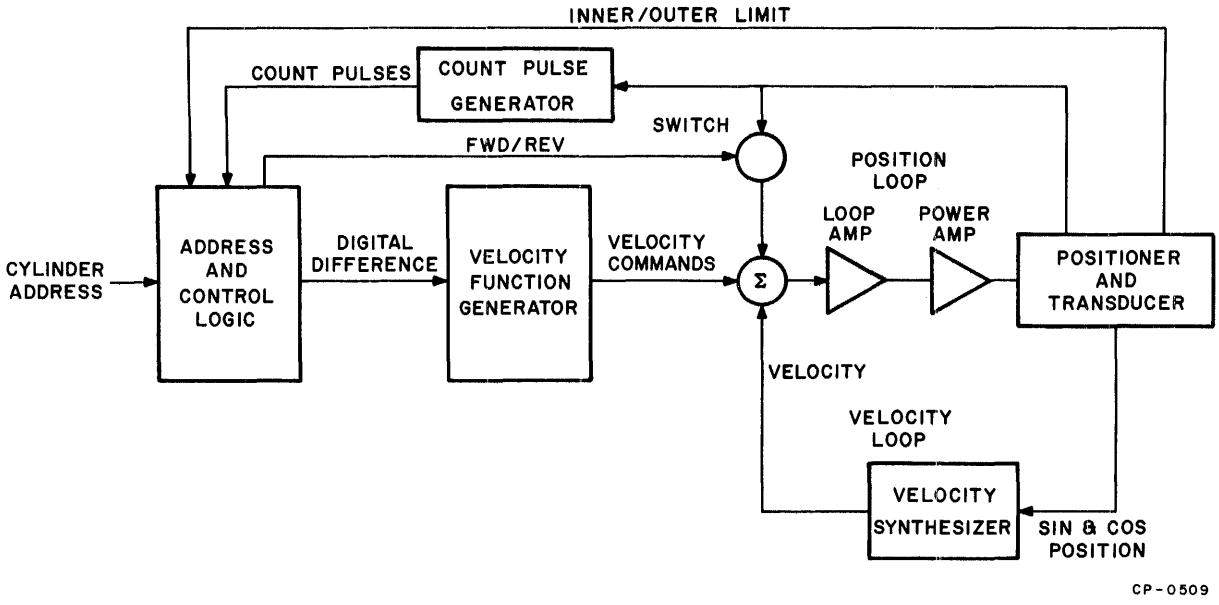


Figure 7-5 Servo System Block Diagram

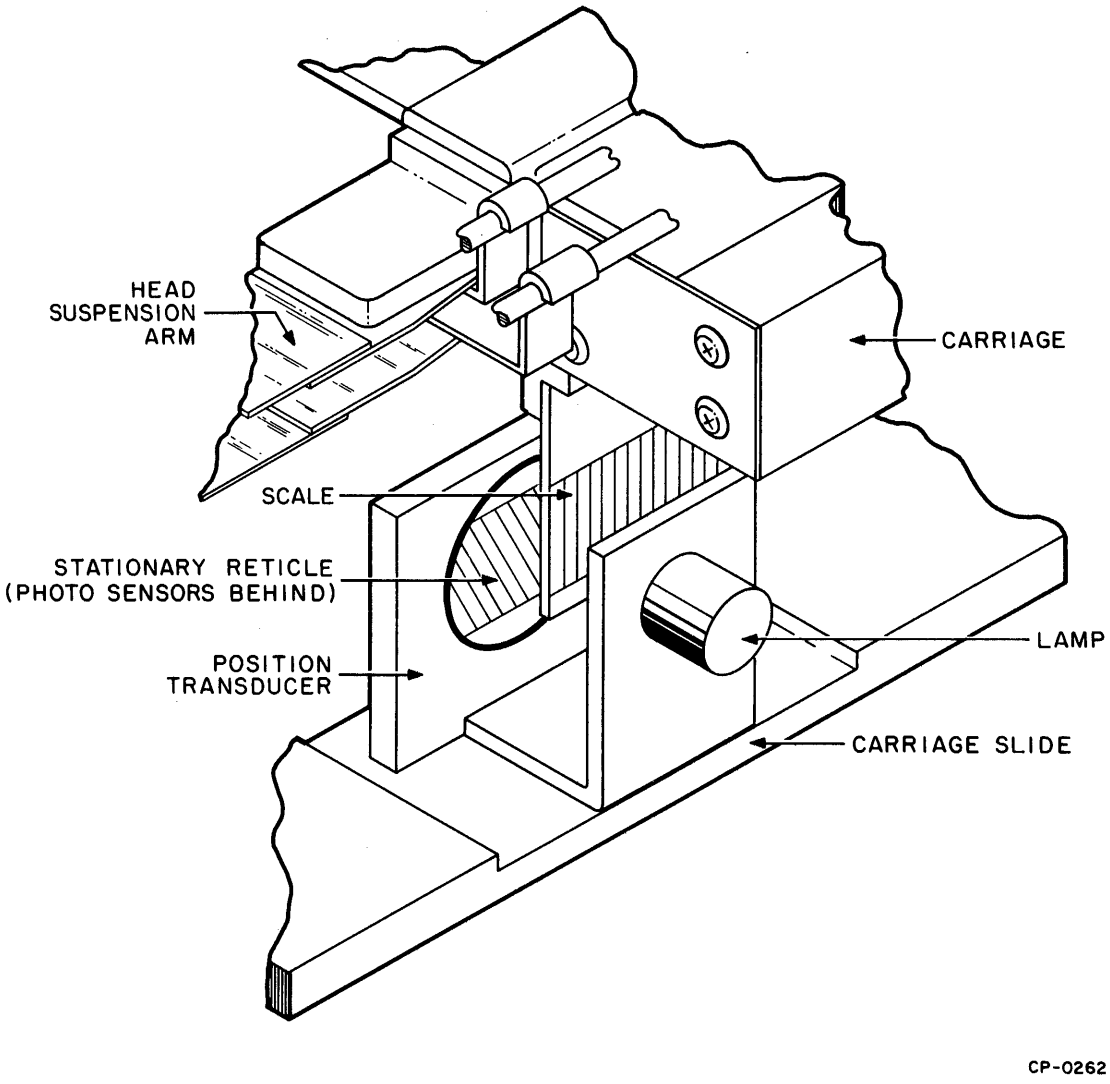


Figure 7-6 Linear Positioner Transducer

The movable portion (scale) of the transducer contains a similar section of minute vertical transparent slots and is attached to the movable carriage. As the scale moves, the vertical and diagonal slots allow varying light patterns to shine onto the photosensors. This action produces two sine wave output signals that occur 22Ø degrees out of phase. These signals (SIN POSITION and -COS POSITION) are used to control the movement of the carriage.

The transducer also generates two dc signals (INNER LIMIT and OUTER LIMIT). As long as the scale travel remains within the slotted section (cylinder Ø through 2Ø2, decimal), neither signal is produced. However, when the scale reaches the inner limit of travel (greater than cylinder 2Ø2 for RKØ5, RKØ5J, and the "odd" drive of an RKØ5F), the inner limit photosensor is uncovered, producing the INNER LIMIT signal. The positive OUTER LIMIT signal is produced in a similar manner at the outer limit of travel (less than cylinder Ø for RKØ5, RKØ5J, and the "even" drive of an RKØ5F).

Velocity Function Generator

The velocity function generator (see Figure 7-7) is a 5-bit D/A converter. The generator logic elements are on the G938 card.

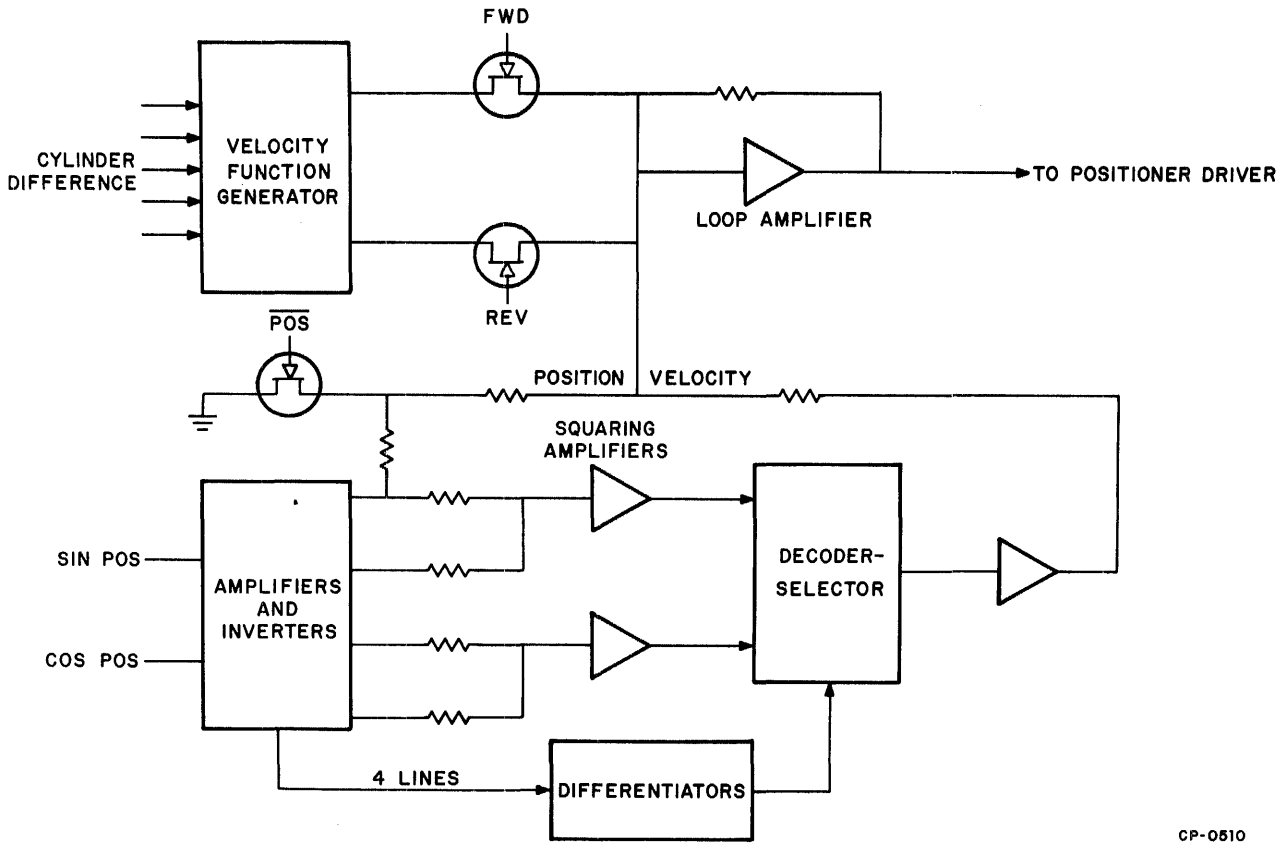


Figure 7-7 Simplified Positioner Servo Logic Block Diagram

The 5-bit digital input to this logic component is derived from the five difference bits from the cylinder address and difference logic. During a seek operation, these five bits represent the distance from the present cylinder address to the destination cylinder. If this distance is greater than 31 (decimal) cylinders in the RKØ5/RKØ5J (or 63 [decimal] cylinders, RKØ5F), all 5 input bits are low, producing a maximum amplitude velocity command.

If the travel distance is less than or equal to three cylinders for the RKØ5/RKØ5J (or seven cylinders, RKØ5F), all 5 inputs are high, producing a minimum velocity command. For differences between 4 and 3Ø for the RKØ5/RKØ5J (or between 8 and 62, RKØ5F), the velocity command is proportional to the 5-bit binary representation.

The velocity command is applied to the summing node of the loop amplifier by field-effect transistors (FET). To initiate carriage motion, the FWD or REV signal turns on the appropriate FET, applying the velocity and direction command to the loop amplifier.

Velocity Synthesizer

In a closed-loop servo system, a speed-sensing feedback control signal is required to prevent uncontrolled velocity within the system. In the RKØ5 this control (tachometer signal) is electronically derived in the velocity synthesizer. These elements are located on the G938.

During a seek operation, the SIN POSITION and -COS POSITION signals from the positioner transducer are applied to amplifiers and unity gain inverters to provide four phases of position signal at the input of the synthesizer. The inverter/amplifer outputs are also applied to four differentiator networks.

Appropriate pairs of amplifier/inverter outputs are applied to the summing junctions of two squaring amplifiers. The resultant square wave signals are displaced 9Ø degrees from each other. When these signals are gated together in the decoder/selector, they produce four separate selection signals that occur during one cycle of SIN position.

Each selection signal is centered around the peak of the corresponding differentiated signal. The derivative signals are then selectively summed in an operational amplifier to produce the velocity feedback signal. This signal is then applied, through a gain-setting resistor, to the summing node of the loop amplifier. Here, the velocity command from the velocity function generator is summed with the velocity feedback signal to produce a velocity profile signal.

Two of the four selection signals are also routed to the current cylinder address register (Figure 7-4), so that a new seek difference may be calculated. The new seek difference will produce a new five-bit desired velocity for the velocity function generator. The current cylinder address register uses one input to increment the address (forward direction) and the other to decrement the address (reverse direction).

During the detent mode of operation, the POS signal turns on an FET that applies the SIN POSITION signal directly to the summing node of the loop amplifiers. This circuit configuration retains the heads at the desired cylinder location.

READ/WRITE OPERATION

All read or write operations are executed by the G18Ø module. The sequence of events for both a write operation and a read operation is described below.

Write Operation

To initiate a write operation, the controller will perform the actions listed below.

- Select a drive.
- Position the heads over the desired cylinder (seek).
- Select a head.
- Apply write data and clock pulses to the write encoder flip-flop.
- Assert write gate.

On the G18Ø module the actions listed below occur.

- Write current driver applies current to one half of the center-tapped write coil of the selected head (enabled by write gate).
- The write encode flip-flop is set and reset to cause current to be applied to the other half of the center-tapped write coil. Thus, with each current transfer in the head coil, a flux reversal is recorded on the disk surface.

Read Operation

To initiate a read operation, the controller will perform the actions listed below.

- Address a particular drive.
- Position the heads over the desired cylinder.
- Select a head.

On the G18Ø module the actions listed below occur.

- Selected head detects flux reversals from the disk surface.
- Flux reversals generate voltage levels (millivolts). This voltage is amplified and filtered, and applied to wave-shaping circuit.
- The output of the wave-shaping circuit is a 347 nanosecond logic level pulse train (clock and data).

- The pulse train is applied to a data separator circuit.

The data separator will separate the individual clock and data pulses and output them back to the controller via the G18Ø module as read data and read clock.

The RKØ5/RKØ5J/RKØ5F Disk Drive Maintenance Manual (EK-RK5JF-MM) contains a detailed explanation of the reading and writing of data and of the data separator.

SUMMARY

Drive General Description

- One drive interface cable is used to transmit and receive control data and status information between the drive and controller.
- A logic assembly houses five logic modules. Their functions are listed below.
  - G18Ø controls the reading and writing of data and head selection.
  - M77ØØ/M768Ø generates sector/index pulses, monitors disk speed, and resets the sector counter.
  - M77Ø2/M7681 calculates the difference between the current cylinder address and the desired cylinder address.
  - M77Ø1 monitors the drive interlocks during start-up, and controls the indicators on the front panel.
  - G938 controls carriage movements by means of a servo system.
- Servo system operates in either of the two modes of operation listed below.
  - Velocity mode controls carriage velocity during seek operation.
  - Detent mode retains the heads positioned over the desired cylinder.
- Servo system is composed of the three functional areas listed below.
  - Linear positioner transducer - An optical device which transmits SIN, COS and limit signals to the M7681 and G938 modules.

    - Velocity function generator converts digital difference signals into analog velocity voltages.
    - Velocity synthesizer generates a feedback signal from the linear transducer output.
- Control panel starts/stops the drive, and gives the operator visual indications of the read/write, write protect, and ready status of the drive.
- Power supply supplies the required voltages. It contains three voltage regulators (+5 V, +15 V and -15 V).
- Spindle motor relay (K1) applies power to spindle drive motor.
- Safety relay (K2) enables the battery pack to power the positioner to retract the heads in case of a power loss.
- Pack-on interlock is used to denote when a cartridge has been inserted into the drive.
- Door closed interlock prevents spindle motor from being energized until the door is closed.
- Door unlock solenoid locks the front door when the RUN switch is pushed to avoid damage to the disk or the heads while the disk is spinning.
- Sector transducer is an LED/photosensor device which generates pulses from the slotted hub on the underside of the cartridge.

Read/Write Operations

- Write data
    - Select a drive
    - Position the heads
    - Select a head
    - Assert write gate (energize write current source)
    - Send write data and clocks
    - Write flux reversals

- Read data
    - Select a drive
    - Position the heads
    - Select a head
    - Assert read gate
    - Selected head detects flux reversals
    - Amplify, filter and shape voltage levels
    - Separate data from clock pulses in data separator
    - Send separated data and clock pulse trains to controller

Now that you have completed this module you can take the module test. The course administrator has the test answers.

RKØ5 DISK SUBSYSTEM MAINTENANCE

Component Location

COMPONENT LOCATION

INTRODUCTION

The more you know about a device, the easier it will be to maintain the device. Knowledge gained about a device aids in building confidence in your ability to maintain the device.

You have studied modules covering the theory of operation of both the controller and drive. It is now time to get involved with the "hands-on", or laboratory portion of the course. Part of your confidence in maintaining this device will come from the familiarity you will gain from the removal/replacement of drive components in this class. This module, therefore, will give you the experience needed to maintain this device.

OBJECTIVES

Upon completion of this module, you will be able to locate the components on the list below and be able to remove and replace those components identified with an asterisk (*).

- Carriage assembly*
- Linear positioner*
- Control and indicators
- Read/write heads*
- Sector transducer
- Carriage bearings
- Front door interlock
- Linear positioner transducer
- Logic chassis
- Spindle*
- Blower motor
- Spindle drive motor and belt*
- Duckbill
- Absolute filter*
- Power supply regulators: +5 Vdc, +15 Vdc and -15 Vdc*

To demonstrate your ability to meet this objective, you will complete the laboratory project at the end of this module within the allotted time stated on the worksheets.

COMPONENT LOCATION

REQUIRED RESOURCES

RKØ5/Ø5J/Ø5F Disk Drive Maintenance Manual	EK-RK5JF-MM-ØØ1

REQUIRED TOOLS AND EQUIPMENT

- RKØ5 Disk Drive
- Standard Field Service tool kit that includes the items listed below.

• Medium-sized flat-blade screwdriver	
• Small Phillips screwdriver	
• Torque wrench assembly (old screws)	DEC P/N 29-2Ø994
• Torque wrench tip, 55 oz-inch	DEC P/N 29-2Ø995
• Torque wrench assembly (new screws)	DEC P/N 29-22521
• Torque wrench tip, 3/32 inch Allen	DEC P/N 29-22522
• Extension bar 6 inch	DEC P/N 29-2Ø9Ø7
• Hex-head wrench 3/16 inch	DEC P/N 29-2Ø9Ø8
• 3/8 inch nutdriver	
• .ØØ5 inch (blue) shimstock	DEC P/N 29-19664
• .ØØ2 inch feeler gauge	

The laboratory worksheet tells you to remove several components before you replace any of them. For example, it doesn't make sense to remove, then replace, the linear positioner only to next remove the carriage, because to remove the carriage you must first remove the linear positioner. Follow the instructions carefully on the laboratory worksheet to avoid repeating steps. When you are ready, ask the course administrator to assign you an RKØ5 Disk Drive to begin your laboratory projects.

COMPONENT LOCATION

Laboratory Worksheet

Given an RKØ5 Disk Drive and the tools and reference material required, go to the lab and complete this laboratory worksheet within four hours or less. You may work in teams to complete the worksheet. After removing the top and bottom covers on the RKØ5, perform the following:

1. Locate the components on the supplied list, and place a check on the line when located.

   a. Controls and indicators ___
   b. Sector transducer ___
   c. Spindle ___
   d. Logic chassis ___
   e. Blower motor ___
   f. Absolute filter ___
   g. Spindle drive motor ___
   h. Power supply regulators: +5 V ___ +15 V ___ -15 V ___
   i. Linear positioner ___
   j. Read/write heads ___
   k. Front door interlock ___
   l. Duckbill ___
   m. Linear positioner transducer ___
   n. Carriage and bearings ___

2. Now that you have located these components, remove and then replace the following components in the order listed. Chapter 5 of the RKØ5/Ø5J/Ø5F Disk Drive Maintenance Manual lists the procedures you must follow.

   - Remove the linear positioner (Procedure 5.3.1.1)
   - Remove the carriage (Procedure 5.3.2.1)
   - Replace the carriage (Procedure 5.3.2.2)
   - Replace the linear positioner (Procedure 5.3.1.2)
   - Remove and replace the spindle (Procedures 5.3.4.1 and 5.3.4.2)
   - Remove and replace the spindle drive motor and belt (Procedures 5.3.5.1, 5.3.5.2, and 5.3.5.3)
   - Replace the read/write heads (Procedure 5.3.3.3)

RKØ5 DISK SUBSYSTEM MAINTENANCE

Alignments/Adjustments

ALIGNMENTS/ADJUSTMENTS

INTRODUCTION

Several of the RKØ5 drive components that you have learned to remove and replace require adjustment after replacement. These components that require adjustment are listed below.

- Positioner transducer
- Heads
- Sector transducer
- G938 module
- H6Ø4 module
- G18Ø module

This course module describes the major alignments/adjustments that must be made following the replacement of these components. In the previous laboratory project, when you removed and replaced the positioner, you also aligned the positioner. You also aligned the positioner transducer after replacing the carriage. These two alignments were done then to avoid possible damage to the drive.

The remainder of the alignments/adjustments are to be performed as part of two laboratory exercises following the text of this module. The text describes to you the purpose of each adjustment to help you understand what you are doing.

Learning how to do these adjustments well is extremely important because a large percentage of RKØ5 service calls are corrected by making one or more of the adjustments found in this laboratory exercise.

OBJECTIVES

Upon completion of this module, you will be able to adjust and/or align the following items.

- Servo electronics
- Read/write heads
- Read/write data separator
- Index/sector timing

To demonstrate your ability to meet this objective, you will complete the two laboratory worksheets found at the end of this module within the allotted time stated on the worksheets. You will also complete a written test consisting of multiple-choice and true-false questions concerning the alignments.

ALIGNMENTS/ADJUSTMENTS

REQUIRED RESOURCES

None

OPTIONAL RESOURCES

RKØ5/Ø5J/Ø5F Maintenance Manual	EK-RK5JF-MM-ØØ1

EQUIPMENT REQUIRED

- PDP-11 or PDP-8 system
- RK11D or RK8-E, RKØ5 Disk Drive
- Multimeter
- Oscilloscope with three probes
- Torque wrench, 55 oz-inch
- Torque wrench, 125 oz-inch
- 3/32 inch Allen tip for torque wrench
- 3/16 inch hex-head wrench
- 6 inch extension bar
- Alignment cartridge
- Scratch cartridge

GENERAL DESCRIPTION

As you have seen, certain components require some sort of adjustment or alignment after replacement in order to restore the drive to service. For example, the positioner must be correctly reinserted into the drive. Thus, you checked the placement of the positioner with a feeler gauge.

The carriage replacement requires that the read/write heads be realigned and the positioner transducer be aligned so that the glass scale is not damaged.

The sector transducer requires an index/sector timing adjustment when the transducer is replaced.

If either the G938 or the H6Ø4 modules are replaced, then the complete series of servo adjustments must be performed.

When a G18Ø module is replaced, then the data separator must be adjusted to the drive.

The following text describes the adjustments you will do in the laboratory exercises.

SERVO ADJUSTMENTS

The output of the position transducer consists of three signals. SIN POSITION and -COS POSITION are applied to a velocity synthesizer for carriage speed calculation. The velocity synthesizer also uses an input from the cylinder difference calculation and converts the difference into an analog function.

The third signal is LIMIT and is used to generate the inner and outer limit signals for the positioning logic.

The velocity, sine, cosine and limit signals are applied to operational amplifiers. These amplifiers must be adjusted due to the relative instability of the light source input. As the transducer light ages, the intensity and focus varies. This, in combination with the aging of discrete components of the module, creates servo feedback instability.

Field service adjustments compensate for these problems. The operational amplifiers are adjusted for both output signal amplitude and output signal offset relative to ground.

One other input to the module contributes to servo feedback instability. The power supply voltages in this circuit application are critical. Before making the servo adjustments, the power supply regulator outputs must be within specifications. If they are not correct, then one or more of the servo adjustments cannot be set to specifications. In this case, you have to correct the power supply output voltages and then perform the servo adjustments.

ALIGNMENTS/ADJUSTMENTS

The servo adjustments are set at the factory and should not be routinely adjusted or fine-tuned as part of any preventive maintenance (PM) procedure. The PM procedures only require checking of the adjustments. If a positioner malfunction is suspected, all waveforms related to each phase of servo operation should be checked. Based on these checks, the possible positioner problem should be diagnosed prior to any servo adjustments being made.

If adjustments are necessary to correct the problem, or when replacing the G938 module, then all of the adjustments for the servo must be performed, and they must be done in the following order.

1. SA (sine amplitude) - Sets the amplitude of SIN POSITION signal

2. SO (sine offset) - Adjusts the SIN POSITION signal to be symmetrical about a ground reference

3. VO (velocity offset) - Adjusts the velocity generator output to be symmetrical about a ground reference

4. CA (cosine amplitude) - Sets the amplitude of -COS POSITION signal

5. CO (cosine offset) - Adjusts the -COS POSITION signal to be symmetrical about a ground reference

6. VA (velocity amplitude) - Adjusts the velocity generator frequency

7. Positioner acceleration - Sets maximum positioner current

8. LSA (limit signal amplitude) - Adjusts the smaller of two amplitude positioner limit signals to a minimum acceptable level

9. LSO (limit signal offset) - Sets the reference level of the limit signals to zero

The adjustments must be done in the above sequence in order to avoid the following problems.

- Making one adjustment and forcing another out of tolerance

- Making excessive oscilloscope control changes

- Making excessive oscilloscope probe test point changes

HEAD ALIGNMENT

Head alignment is performed when the following conditions exist.

- The subsystem cannot read/write data properly
- One or both read/write heads have been changed
- Carriage has been removed
- Spindle has been removed
- Positioner transducer has been removed

A head alignment should not be attempted if either of the following conditions exist.

- The drive has other malfunctions.
- The heads have been contaminated by a defective cartridge, head crash, etc.

The two read/write heads must not only be aligned with each other, but must be aligned with the linear positioner transducer. The transducer determines the final position of the read/write heads.

The transducer produces three types of output signals. One type represents actual carriage velocity while another calculates the read/write track crossing by the heads. The third indicates that the heads are out of the data area of the cartridge.

The engineering technology present at the time of RKØ5 design did not allow for the detection of these items by reading the disk surface. In this situation, the positioner transducer directs the heads to the desired data track. The read/write heads may or may not be over the desired data track because they were left out of the control of positioner movement. To correct for the possible misalignment between the heads and the servo positioning system, an alignment cartridge was created.

The alignment cartridge provides a prerecorded reference for the read/write heads. There are three tracks of information recorded, one principle track (cylinder 105_{10}) and two spares (cylinders 85_{10} and 125_{10}).

The RKØ5F cannot use the spares because the cartridge was designed for use by the RKØ5J drive. The cylinder numbers do not translate for the two spare tracks. The controller sees cylinder 1Ø5 as track 5 of an odd drive in an RKØ5F subsystem, provided a jumper is installed in the backplane between ground and AØ8K2 or AØ8M2. This will select the odd drive.

Before a head alignment is started on an RKØ5, the mating surfaces of the spindle and disk must be checked and cleaned, if necessary. Dirty or improper mating can give the appearance of spindle runout.

Spindle runout (wobble) can be checked with the alignment cartridge by displaying an entire revolution of the alignment track on the oscilloscope. The selected head may appear to be aligned at some sector locations and misaligned at others. See Figures PM-7 and PM-8 in the Laboratory Projects Workbook for runout example waveforms.

NOTE

Before performing any head alignment, sector transducer or data separator adjustments, ensure that the customer has all critical data packs backed up. Changing any of these adjustments may make the original data irretrievable.

INDEX/SECTOR TIMING ADJUSTMENT

When the head alignment is completed, the index/sector timing adjustment must be made. This adjustment ensures that the placement of the sector transducer coincides with the placement of the read/write heads. In other words, when the sector transducer senses the start of a sector, the read/write heads should also be at the start of a sector. Due to packaging design problems in this type of drive, the transducer cannot be placed in the same physical location as the heads.

The sector transducer senses the start of each sector as determined by notches cut in the hub of the disk. The drive logic is enabled at the start of each sector by a signal from the transducer. If the read/write heads are out of alignment with respect to the transducer, it is possible that the logic could gate the start of the read operation too late; i.e., the heads will already be in the header area of the sector.

This adjustment ensures that the transducer is physically placed so that whenever the sector transducer detects a sector notch, the heads are reading the beginning (preamble area) of the sector.

The adjustment uses the index pulse as an external trigger to the oscilloscope. The signal on channel A probe is data coming from the selected read/write head. The alignment cartridge supplies a prerecorded burst of information to aid in the adjustment.

The sector transducer alignment consists of adjusting a potentiometer which varies the pulse width of a one-shot. This simulates the movement of the transducer in side-to-side motion. Figure 9-1 shows the oscilloscope waveform seen when performing this adjustment. This figure shows the prerecorded information using the cartridge index pulse to trigger the sweep. Within 70 (±12) microseconds following the index pulse, the heads should detect the prerecorded index pulse with data following.

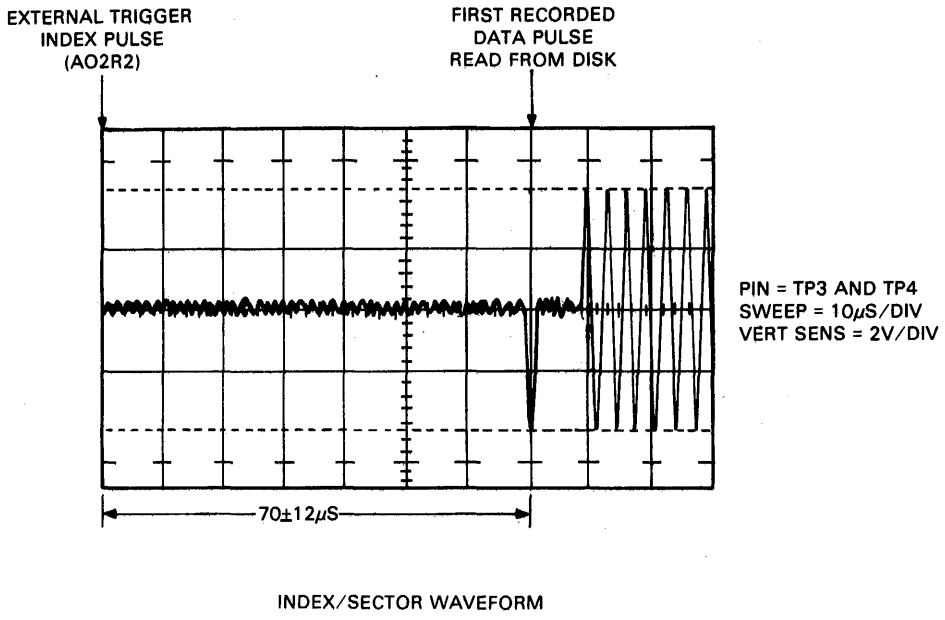


Figure 9-1 Index/Sector Waveform

Because of the manufacturing tolerances of the machined parts, the read/write heads may not read the data at the same time. The potentiometer enables averaging the results of reading the data.

READ/WRITE DATA SEPARATOR ADJUSTMENT

The data separator isolates the imbedded clock pulses from the data in the frequency modulated read data bit stream.

The technology present at the time of design did not allow for the phase-locked circuits that exist today. This data separator functions via a flip-flop and a one-shot.

There are two potentiometers in the separator which must be adjusted to allow the circuit to function effectively. The circuit is adjustable to compensate for changing component tolerances during manufacture and aging. If problems show up in compatibility or in read data errors, this adjustment should be checked, and if out of tolerance, readjusted.

The two potentiometers adjust the one-shot pulse width. OL (R54) establishes the coarse width of the one-shot output. CL (R55) is a fine-tune of the adjustment, and should be set to narrow the coarsely set pulse from 500 nanoseconds to 440 nanoseconds.

If the one-shot timing is set too low, data pulses will be missed (not gated out). If the one-shot timing is set too high, then clock pulses will be missed. In either case, the data being transferred to the controller will be in error.

SUMMARY

- Servo adjustments should be made when the G938 or H6Ø4 modules are replaced or when the drive seeks incorrectly
- Prior to making any adjustment, the power supply regulators must be checked and the voltages must be adjusted to the proper levels if needed.
- If servo adjustments are needed because of a malfunctioning positioner, all the adjustments must be done in the sequence listed.
    - Sine amplitude (SA)
    - Sine offset (SO)
    - Velocity (VO)
    - Cosine amplitude (CA)
    - Cosine offset (CO)
    - Velocity amplitude (VA)
    - Positioner current
    - Limit signal amplitude (LSA)
    - Limit signal offset (LSO)
- Head alignment should be performed when any of the following conditions exist.
    - Read/write heads have been replaced.
    - The drive cannot read data properly.
    - Spindle has been removed.
    - Carriage has been removed.
- Head alignment should not be attempted if either of the three conditions listed below exist.
    - The drive has other malfunctions.
    - The read/write heads have been contaminated by a defective cartridge, head crash, etc.
    - Customer data has not been backed up.
- The drive should be run for at least 3Ø minutes with the alignment cartridge in place before aligning the heads.
- The index/sector timing adjustment should be checked and performed after head alignment.
- The read/write data separator adjustment should be performed when the G18Ø module is replaced. The adjustment should be checked any time the drive exhibits read data errors in the course of troubleshooting.

ALIGNMENTS/ADJUSTMENTS

Laboratory Exercise 1

Given an operating subsystem, the supplied documentation, tools and test equipment, perform the following adjustments within one hour. You may work in teams on this exercise.

- Check and adjust the power supply regulator output voltages (see Appendix A in the Laboratory Projects Workbook).
- Check and adjust the servo system (see Appendix D in the Laboratory Projects Workbook).
- Check and adjust the data separator (see Appendix G in the Laboratory Projects Workbook).

Successful completion of this exercise is to accomplish all adjustments and checks within the allotted time.

Laboratory Exercise 2

Given an operating subsystem, the supplied documentation, tools and test equipment, perform the following alignments within one hour. You may work in teams on this exercise.

1. Check and perform a head alignment (see Appendix E in the Laboratory Projects Workbook).
2. Check and perform the index/sector adjustment (see Appendix F in the Laboratory Projects Workbook).

Successful completion of this exercise is to accomplish the head alignment and index/sector adjustment within the allotted time.

Now that you have completed the required laboratory exercise, you can take the module test. The course administrator has the test answers.

RKØ5 DISK SUBSYSTEM MAINTENANCE

Preventive Maintenance

PREVENTIVE MAINTENANCE

INTRODUCTION

The key to the performance of the RKØ5 Disk Drive is adequate preventive maintenance (PM) by Field Service personnel. Preventive maintenance is a combination of the following tasks.

- Visual inspection
- Cleaning
- Removal/replacement of key drive components
- Checking of adjustments/alignments

This module describes the PM schedule for an RKØ5 and contains a module exercise for you to complete. This exercise includes all the tasks for the PM schedule. In completing these tasks you will become familiar with the procedures you will be required to perform at a customer's site.

OBJECTIVES

Upon completion of this module, you will be able to perform preventive maintenance on an RKØ5 Disk Drive. Using the RKØ5 Laboratory Projects Workbook, you will complete the laboratory exercise found at the end of this module within the allotted time stated.

You will also complete a written test consisting of multiple-choice and true-false questions concerning the PM procedures.

REQUIRED ADDITIONAL RESOURCES

None

OPTIONAL ADDITIONAL RESOURCES

RKØ5/Ø5J/Ø5F Maintenance Manual	EK-RK5JF-MM-ØØ1

REQUIRED TOOLS

Multimeter	Simpson, Micronta, or equivalent
Oscilloscope	Tektronix 453 or equivalent
Probe, oscilloscope (voltage X1Ø)(3)	Tektronix P6Ø1Ø
Flag, probe (3)	DEC 29-15188
Adapter, flag (3)	DEC 29-19363
Field Service tool kit	DEC 29-23268
Wrench set, 1Ø pieces (Hex-Key Pak No. 1Ø7)	DEC 29-13519
Head cleaning kit	DEC 22-ØØØ7-ØØ
Inspection mirror	DEC 29-19663
Isopropyl alcohol (91%)	DEC 29-19665
Cotton tipped wooden swabs	DEC 9Ø-Ø8436
Blue shim stock, Ø.ØØ5 in.	DEC 29-19664
Cartridge, alignment	DEC RKØ5K-AC
Cartridge, disk (12-sector, 11-family)	DEC 3Ø-1Ø35Ø-ØØ
Cartridge, disk (16 sector, 8-family)	DEC 3Ø-1Ø35Ø-Ø2
Torque wrench, 55 in-oz for old head screws	DEC 29-2Ø994
Allen tip for 55 in-oz screws	DEC 29-2Ø995
Torque wrench, 128 in-oz for new head screws	DEC 29-22521
3/32" Allen tip, 128 in-oz screws	DEC 29-22522
Jumper strings	

GENERAL DESCRIPTION

Digital Equipment Corporation's PM schedule for the RKØ5 is shown in Table 1Ø-1.

Table 1Ø-1 RKØ5 Preventive Maintenance Schedule

Q	A	5	Task	Time (est.)
X	X	X	Inspect and clean heads	5 min
X	X	X	Inspect cartridges and spindle area	5 min
X			Clean prefilter	5 min
	X	X	Replace prefilter	2 min
	X	X	Replace absolute filter	1Ø min
	X	X	Check for worn shock mounts	1 min
		X	Replace spindle brush assembly	5 min
		X	Remove and clean blower	15 min
	X	X	Clean pulleys	1 min
	X	X	Inspect drive belt	1 min
	X	X	Check linear positioner	1 min
	X	X	Check power supply	5 min
	X	X	Check servo adjustments	2Ø min
	X	X	Check spindle runout	3Ø min
	X	X	Check head alignment	
	X	X	Check data separator	
	X	X	Check sector delay	
X	X	X	Check for head/disk interference	2 min
X	X	X	Run diagnostics (performance exerciser DZRKH-G)	1Ø min

NOTE

Q = perform quarterly (or 75Ø hours)
A = perform annually (or 3ØØØ hours)
5 = perform every five years (or 15ØØØ hours)
Completion times are minimum estimates, providing no trouble is found.

The laboratory project following this lesson is organized so that you will sequence through all three PM schedules, performing all the tasks required of you in the field.

Go to the administrator and find out the location of the equipment you will be working on. The administrator will also assign a tool set for you to use on the drive while performing the PM.

Open the Laboratory Projects Workbook to the PM section and follow all the steps outlined. If you have any problems, do not hesitate to ask the administrator for help.

When you have completed the Laboratory Projects Workbook you can take the module test. The course administrator has the test answers.

RKØ5 DISK SUBSYSTEM MAINTENANCE

Subsystem Diagnostics

SUBSYSTEM DIAGNOSTICS

INTRODUCTION

This module gives you a basic description of the diagnostics used to check out and isolate hardware malfunctions in the RK11/RKØ5 Disk Subsystem and the RK8-E/RKØ5 Disk Subsystem.

All diagnostics used with either subsystem operate in a standalone mode. Each diagnostic contains subroutines which provide error messages should a failure occur. These error messages provide useful information to help you isolate the malfunction.

It is the purpose of this module to give you the experience of interacting with the dialogue for each diagnostic. Knowing what each diagnostic can do for you and how to use it will give you additional help in troubleshooting RKØ5-related problems.

OBJECTIVES

Upon completion of this module, you will be able to load and run the diagnostics, interacting with them intelligently. Given an operating system and a set of diagnostic listings, you will be able to perform the tasks listed below.

- Load and run the diagnostics.
- Select and run an internal test (subroutine) using the console switches.
- Select and run an internal test (subroutine), and loop on that test.

To demonstrate your ability to perform these tasks, you will be required to load, run and interact with a diagnostic in a laboratory assignment.

REQUIRED RESOURCES

RK11/RKØ5 Diagnostic Listings	DZRKJ-E	Logic Test 1
	DZRKK-F	Logic Test 2
	DZRKL-E	Dynamic Test
	DZRKH-G	Performance
	DZRKI-E	Utility
RK8-E/RKØ5 Diagnostic Listings	DHRKA-E-D	Diskless
	DHRKB-G-D	Drive Control
	DHRKD-D-D	Formatter
	DHRKC-H-C	Reliability

SUBSYSTEM DIAGNOSTICS

RK11/RKØ5 DIAGNOSTICS

There are four diagnostics which check out a complete RK11/RKØ5 Disk Subsystem. They are listed below.

- DZRKJE RK11 basic logic test 1
- CZRKKF RK11 basic logic test 2
- DZRKLE RK11/RKØ5 dynamic test
- DZRKHG RK11/RKØ5 performance exerciser

In addition to these four diagnostics, there is a utility program (DZRKIE) which is used to perform the tasks listed below.

- Servo adjustments
- Head alignments
- Formatting a disk cartridge
- Checking the control panel indicators/switches

The complete series of diagnostics assure the Field Service engineer that the disk subsystem is operating properly.

The diagnostics are designed in a bottom-up manner. This means that each diagnostic uses a more complex subset of hardware than the previous diagnostic. Therefore, the diagnostics should be run in a sequence starting with the basic logic test and finishing with the performance exerciser. The following text describes each of the diagnostics.

The RK11 basic logic tests 1 and 2 check the most basic of logic in the RK11 Controller. Logic test 1 checks only the drive independent controller logic while logic test 2 checks the logic that is operated in conjunction with a drive. Since logic test 2 is used with a drive, the diagnostic is capable of detecting faults occurring in the drive as well as of detecting faults in the controller.

Basic logic test 1 takes approximately one minute to complete a pass. Basic logic test 2 takes approximately two minutes to complete a pass.

At the completion of these two tests, the RK11 Controller is assumed to be operating properly.

The RK11/RKØ5 dynamic test is run next and consists of a series of sub-tests aimed at providing the following four functions.

- Checking the electromechanical intregrity of the drive
- Checking the linear positioner and speed control logic of the drive

- Verifying the integrity of the read/write logic
- Provide a timing test for maximum and minimum seek times

Run time for one pass is approximately eight minutes.

RK11 Utility Package

The RK11 utility package contains seven programs which allow test selection and parameter inputs via the console device.

The program is loaded and started from memory address 200. The following table is printed out, informing the user of the name and type of each test.

RK11 UTILITY PACKAGE

NAME	**TYPE**
INDEX	**0**
COMPATIBILITY PACKAGE	**1**
OSCILLATING SEEK PACKAGE	**2**
FORMATTER-SURFACE VERIFIER	**3**
RK05 CONTROL PANEL TEST	**4**
RK05 CONTROL PANEL TEST #2	**5**
HEAD ALIGNMENT ROUTINE	**6**
POWER FAILURE (WRITE) TEST	**7**

TYPE = x

where "x" is the response (0-7) by the user.

As an example, if the user wants to format a disk cartridge, the response to the prompt

TYPE =

would be 3. The program would then print out all instructions for the user to follow, and format the cartridge. Upon completion, the program prints

FORMAT COMPLETED

Example:

TYPE = 3

FORMATTER-SURFACE VERIFIER, SET SW REG FOR DRV #'S. PRESS CONT.

This utility package can also be used to perform the tasks listed below.

- Perform servo adjustments
- Perform head alignments
- Check compatibility of disk drive (write on one drive/ read from another)
- Check proper operation of switches and indicators on front control panel

The formatter package should be used to format a disk cartridge prior to running the performance exerciser program. Also, the servo adjustments and head alignment should be checked and performed if necessary before running the performance exerciser.

RK11/RKØ5 Performance Exerciser

The RK11/RKØ5 performance exerciser is a high-level exerciser program. It is aimed at simulating an RK11/RKØ5 system environment, and checks for errors which arise in such an environment. This program provides a means of evaluating the RK11/RKØ5 system through data transfers and error logging.

Since this is a high-level exercise program, the controller and drive should be free of any basic faults. Therefore, the following programs should be run successfully before attempting to use the exerciser program.

- RK11 basic logic test (1 and 2)
- RK11/RKØ5 dynamic test
- RKØ5 utility package

Example printout:

```
RK11/RKØ5 PERFORMANCE EXERCISER
MAINDEC-11-DZRKH-G
TO TEST DRIVE Ø HALT PROGRAM, REMOVE RKDP PACK AND REPLACE IT
WITH A WORK PACK, CLEAR LOCATION 4Ø, AND RESTART PROGRAM
TYPE OCTAL BUS ADDRESSES FOR DATA XFER, BETWEEN Ø32514 & 131776
LO LIMIT?
```

The execution time of the exerciser program can vary from 3Ø to 9Ø minutes for one complete pass. The first pass is a short (5-2Ø minute) pass to serve as a quick verify of the subsystem.

Error Printouts

Each of the diagnostics used to check out the RK11/RKØ5 subsystem will, in the event of a failure, give the user error printouts.

The error printouts will contain the items listed below.

- The value of the program count at the time of error
- Contents of selected registers at the time of error
- What test was being run, and a brief description of the error

With this information the Field Service engineer can usually make a logical deduction as to what area of logic is causing the error, correct the error and return the system to an operating condition as soon as possible.

Switch Settings

The computer console switches are used to control diagnostic parameters. The switches can be used to provide the following controls over the running of the program.

- Halt on error
- Inhibit error printouts
- Dump all RK registers
- Ring bell on error
- Loop on error
- Loop on test

Each diagnostic listing contains a list of the console switches that control the various parameters used in the diagnostic. For a detailed explanation of each switch and the function it performs refer to the appropriate diagnostic listing in your microfiche library for the diagnostic being run.

The complete set of diagnostics used to check out the RK11/RKØ5 subsystem is a dynamic debugging tool, which aids the Field Service engineer in intelligently maintaining this device.

RK8-E/RKØ5 DIAGNOSTICS

The RK8-E/RKØ5 subsystem has its own set of four diagnostics to check the subsystem.

These diagnostics are designed to check out the simplest logic and then progress to the more complex circuits. Therefore, the diagnostics should be run starting with the basic diagnostic and leading up to the more complex diagnostics. The RK8-E/RKØ5 diagnostics should be run in the following order.

- DHRKA-E-D RK8-E diskless control test
- DHRKB-G-D RK8-E drive control test
- DHRKD-D-D RK8-E disk formatter program
- DHRKC-H-C RK8-E data reliability program

RK8-E Diskless Control Test

The RK8-E diskless control test is designed to check the RK8-E Controller logic. This test does not use the drive. This test can be run with a drive cabled to the controller, or with the cables disconnected from the RK8-E Controller. If a drive is cabled to the controller, power must be applied to the drive and the drive RUN/LOAD switch must be in the LOAD position.

RK8-E Drive Control Test

The RK8-E drive control test is designed to check the RK8-E control logic. This requires that the controller be connected to one or more drives.

In general, this test verifies basic operation of the following commands: seek, restore, write/read data, write-all and read-all. A manual intervention subroutine is included, allowing the Field Service engineer to select data patterns and command functions via the switch register.

The drive control test will format all drives being tested, provided that the conditions listed below are met.

- The test is run error-free
- Switch register bit 9 = 1

If the program is halted at the end of a completed pass, then the cartridge has been formatted.

RK8-E Disk Formatter Program

This program is designed to write and check the format of an entire disk cartridge. Both the RKØ5J and RKØ5F disk cartridges can be formatted using this program. When formatting an RKØ5F cartridge you must remember that the RKØ5F is considered as two separate drives. When answering questions asked by the program for an RKØ5F, each separate unit must be specified (for example, DSKØ?, DSK1?, etc.).

If the formatter program fails, run the programs listed below.

- Basic memory tests
- Extended memory tests
- RK8-E diskless
- RK8-E drive control test

RK8-E Data Reliability Program

The RK8-E data reliability program is a high-level diagnostic which is designed as an acceptance test to verify data transfers within the disk subsystem.

The data reliability program operates in two modes.

- Accept mode of operation verifies the capability of the controller to transfer data to and from each disk drive connected to it.

- Manual intervention mode is used as a hardware debugging aid allowing the Field Service engineer to select data patterns, transfer length, and addressing.

This program can be used to check out both RKØ5J and RKØ5F Disk Drives. The RKØ5F drive must be considered as two separate drives, and all questions must be answered for a specific drive (for example, DSKØ?, DSK1?, etc.)

Error Printouts

The diagnostics used to check the RK8-E/RKØ5 subsystem will display error printouts in the event of a failure.

All error printouts will contain the information listed below.

- The value of the program count at the time of error
- Contents of selected registers at the time of error
- The test number that was being run
- A brief description of the error

With this information, the Field Service engineer can usually make a logical deduction as to what area of logic is causing the error, correct the error, and return the system to an operating condition as soon as possible.

Switch Settings

The computer console switches are used to control diagnostic parameters. Each diagnostic listing contains a list of the console switches that control the various parameters used in the diagnostic. For a detailed explanation of each switch and the function it performs, refer to the appropriate diagnostic listing for the diagnostic being run.

SUMMARY

- The diagnostics used to check and maintain both the RK11/RKØ5 and the RK8-E/RKØ5 Disk Subsystems operate in a standalone mode.

- The RK11/RKØ5 subsystem has four diagnostic programs and a utility package.

    - RK11 basic logic tests 1 and 2

        - Logic test 1 checks only the drive-independent RK11 Controller logic

- Logic test 2 checks the drive-independent RK11 Controller logic with a drive connected to the RK11

- RK11/RKØ5 dynamic test
  - Checks electromechanical intregrity of the drive
  - Checks linear positioner control and speed of the drive
  - Checks the read/write logic
  - Checks seek timing of the drive covering maximum and minimum seeks
- RK11/RKØ5 performance exerciser
  - Performs data transfers to and from the drive
  - Checks the reliability of the complete subsystem
- RK11 utility package
  - Used during servo adjustments
  - Used during head alignments
  - Formats a disk cartridge
  - Checks the operation of switches and indicators on the drive front control panel
  - Checks read/write compatibility of one disk drive with another

- RK8-E/RKØ5 subsystem has four diagnostics which check the subsystem.
  - RK8-E diskless control test
    - Checks the drive-independent RK8-E Controller logic without a drive in the subsystem
  - RK8-E drive control test
    - Checks all drive-independent logic
    - Includes an instruction test which checks out the various commands the subsystem can execute

- Requires an RKØ5 Disk Drive be connected to the subsystem
- Formats the drive if bit 9 of switch register is set and a successful completion of the tests are run

- RK8-E formatter program
  - Writes and checks the format of the entire disk cartridge
  - Formats both RKØ5J and RKØ5F disk cartridges
  - Questions answered for RKØ5F must be answered for two separate drives (for example, DSKØ? DSK1? etc.)

- RK8-E data reliability program
  - Acceptance test which verifies data transfers within the subsystem
  - Operates in two modes
    - Accept mode verifies the capability of transferring data to and from each drive connected to an RK8-E.
    - Manual intervention mode is a hardware debugging aid which allows the Field Service engineer to select any of the items listed below.
      - Data patterns
      - Transfer length
      - Addressing

Error Printouts

The diagnostics used to check both the RK11/RKØ5 and RK8-E/RKØ5 disk subsystems will give the Field Service engineer error printouts which will contain the information listed below.

- The value of the program counter at the time of error
- Contents of selected registers at the time of error
- The test number that was being run at the time of error
- A brief description of the error

Switch Register

The console switch register on both the PDP-11 and PDP-8 processors can be used to control the operation of the diagnostic by performing the tasks listed below.

- Halt on error
- Inhibit error printouts
- Ring bell on error
- Loop on error
- Loop on test

Each diagnostic listing contains a listing of the switch controls.

SUBSYSTEM DIAGNOSTICS

LABORATORY WORKSHEET

Given a complete RK11/RKØ5 or a complete RK8-E/RKØ5 operating disk subsystem, and a complete set of diagnostic listings for each subsystem, demonstrate your proficiency of using the diagnostics by going to the lab and performing the tasks listed below. You may work in teams to complete this laboratory project. Time allowed to complete this project is two hours.

NOTE

Field Service engineers trained on the PDP-11-family computers are only required to perform tasks 1, 2, 4 and 5. Field Service engineers trained on the PDP-8-family computers are only required to perform tasks 1 and 3.

1. Load and run all the diagnostics used to check-out the respective disk subsystem. ____

2. Load RK11 utility package.

   - Use this program to format an RKØ5 cartridge. ____
   - Check the switches and indicators on RKØ5 front panel. ____

3. Load RK8-E formatter program and format a disk cartridge. ____

4. Load the RK11 basic logic test 1 and use the console switches to run test number 11. ____

5. Restart the RK11 basic logic test 1 and loop on test number 11. ____

You have successfully completed this project when you have performed the required tasks and have checked off each item in the space next to the task.

RKØ5 DISK SUBSYSTEM MAINTENANCE

Subsystem Troubleshooting

SUBSYSTEM TROUBLESHOOTING

INTRODUCTION

As a Field Service engineer, you will be required to perform corrective maintenance on a complete RK11/RKØ5 or RK8-E/RKØ5 disk subsystem. This module gives you the opportunity to gain proficiency in troubleshooting these subsystems to the field replaceable unit (FRU) level of repair.

The course administrator will give you at least two problems to troubleshoot as a practice exercise. When you feel you have had enough practice troubleshooting, ask the administrator for the module test.

OBJECTIVES

Given an RK11/RKØ5 or an RK8-E/RKØ5 subsystem, all required documentation, test equipment and diagnostic listings, be able to diagnose, and then locate an inserted problem to the failing FRU. Time allowed for troubleshooting is one hour per problem.

REQUIRED RESOURCES

RK11/RKØ5 Diagnostic Listings
RK8-E/RKØ5 Diagnostic Listings

OPTIONAL RESOURCES

RK11D Print Set	MP-ORK11-DØ
RK8-E Print Set	MP-ORK8J-EØ
RKØ5 Print Set	MP-ORKØ5-JØ

REQUIRED EQUIPMENT

PDP-11 or PDP-8 computer
RK11/RKØ5 or RKR8-E/RKØ5 Subsystem
Console output device
XXDP media loading device
Oscilloscope
Two oscilloscope probes

TROUBLESHOOTING SUGGESTIONS

When troubleshooting any device, approach the problem in a logical manner. Use the diagnostic error printouts, print sets and manuals to assist you. The items listed below are common causes of intermittent problems in any device.

- Cables - improperly seated, disconnected, broken or cut, placed in wrong slot (especially drive bus cable in RK11D subsystems)
- Connectors - improperly connected or not connected, bent pins
- Modules - improperly seated, placed in wrong slot, configuration of switches and jumpers wrong
- Backplane - bent pins, broken wires, jumper configurations wrong
- Voltages - incorrect or missing
- Fuses - blown or missing

The problems which are inserted by the administrator will not cover every conceivable problem you may encounter in the field. Rather, they are intended to be representative of a typical problem.

When you are ready to begin troubleshooting, ask the administrator to insert a problem in the equipment. During the "practice" troubleshooting you may work in groups, but during the module test, you must work alone.

Remember to think about what you are doing, and to observe common-sense safety rules.

Use the exercise worksheet (on the next page) to record the symptoms and solutions for each problem.

NOTE

PDP-11-family trained Field Service engineers should work on the RK11/RK05 problems.

PDP-8-family trained Field Service engineers should work on the RK8-E/RK05 problems.

Exercise Worksheet

Symptom	Description of Failure	Failing Item

After completing this module exercise, take the module test. The course administrator will insert a fault for you to troubleshoot.

When you have completed the module test you can take the final test. The administrator has the answers to the final test.

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