DEC STANDARD 160 REV. A

LSI-11 BUS SPEC.

TITLE: LSI-11 BUS SPECIFICATION-DESIGN SPECIFICATION

ABSTRACT: This standard includes the information necessary to interface to the LSI-11 Bus. Section 0 is the specification. It is a general, or universal, specification with no references to Digital products past or present. It covers the 1980 version of the LSI-11 Bus, including 22 bits of address space and block mode transfers.

Section 1 is a history or folklore section with references to past Digital products and is more instructional in nature. It refers to past Digital backplanes that implemented systems having 16 bits and 18 bits of address space.

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SECTION 0 - DESIGN SPECIFICATION

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1 INTRODUCTION

The original backplane to implement the LSI-11 Bus was designed to accommodate Digital's quad and dual height modules. It became known as the "Q-Bus" to reflect the quad board form factor. Both LSI-11 bus and Q-Bus are Digital trademarks, but are not registered trademarks. Several bus architecture features of the LSI-11 Bus are protected by claims in Digital Unibus patent numbers 3,710,324 and 3,815,099. Some publications may also use the term SUB-UNIBUS, although this is not recommended.

When the LSI-11 Bus was expanded to provide 22 address lines, the terms Q22-Bus and extended LSI-11 Bus were adopted to specify backplanes that bus the four additional lines.

1.1 PURPOSE

The LSI-11 Bus is defined by this standard as the interconnection medium for LSI-11 system components. By adhering to specifications included in this standard, the designer can correctly design and configure system hardware that will be compatible with other LSI-11 system components designed to the same standard. Each Digital option or system component that is designed to connect to the LSI-11 Bus, or a subset of LSI-11 Bus functions, must comply with this standard.

1.2 SCOPE

This section contains complete specifications for the LSI-11 Bus, including quantitative descriptions of signals, functional descriptions of signals, protocol, electrical and transmission line characteristics, transceiver specifications, timing constraints and configuration restrictions.

1.3 RESPONSIBILITIES

This standard is the result of efforts by the Q-Bus Task Force, which is representative of the design community of engineers from product line and central engineering organizations. Accountability and responsibility for maintainence of this standard resides with one person. That person is designated responsible engineer and his or her name will appear as the latest originator on the title page of this standard. It is that person's responsibility to convene the task force to review and approve any ECO's to this standard, to sign ECO's, and to transfer accountability via ECO to update author history.

A list of past and current Q-Bus Task Force members is maintained on file by Digital Standards Administration, ML3-2/E56, DTN: 223-9475.

1.4 HOW TO USE THIS DOCUMENT

First, use the Table of Contents to find specific items of interest, such as DATI Protocol or Bus Mastership Protocol, or Electrical Characteristics.

Second, know how this document is organized. Section 0 is the true and current specification of the bus, and all designs released after the release date of this specification shall conform to it. It is organized to provide a series of overviews for first time users, followed by specifications. Section 1 is a history of previous versions of the bus.

Conventions used in the protocol section follow the electrical section and precede the protocol section.

The protocol descriptions are presented with overviews, followed by specification format where possible, otherwise by just specifications, as follows:

Power Up/Down Protocol (specification)
Initialization (specification)
Boot Protocol (specification)
Data/Address Structure (specification)
Definition of I/O Page (specification)
Interrupt Structure (overview)
Bus Mastership (DMA) Protocol (specification)
Data Transfer Protocol (specification)
Refresh Protocol (specification)
Interrupt Protocol (specification)
BEVENT and BBOK Protocol (specification)
HALT Protocol (specification)

Third, classify your needs from this document.

a. If you are new to the Q-Bus, you will benefit most by reading the document completely. It will take less than an hour, if you just read it without stumbling over points of technical interest.

b. If you are designing a Q-Bus option, you may want to go directly to the electrical characteristics and protocol descriptions of interest to you.

c. If you are involved in older Digital systems, the history of the LSI Bus in Section 1 may be of more interest.

d. If you are designing new systems, the configuration of options section will give you some ideas.

1.5 REFERENCED STANDARDS

DEC STD 007	Design Review Process
DEC STD 030	Module Manufacturing Standard
DEC STD 102	Environmental Standard For Computers and Peripherals
DEC STD 103, (proposed)	Electromagnetic Compatibility (EMC) Hardware Design Requirements
DEC STD 122	Ac Power Line Standard
DEC STD 158 (proposed)	Unibus Specification
DEC STD 186	Signal Integrity

1.6 CONFORMANCE

All new designs must be reviewed in accordance with DEC STD 007, Design Review Process. It is the responsibility of those persons participating in the design review of a new product that connects to the LSI-11 Bus to assure that the design conforms to the requirements stated in this specification.

1.7 GLOSSARY

Asynchronous - Indicates that an event occurs without any fixed or constant time relationship with respect to bus signals.

Backplane - The physical mounting blocks into which modules are inserted; bus signals are connected on the reverse side by wire or etch.

Bus Node - Point of contact between a stub and the bus.

Bus Segment - Portion of the Q-Bus system between and including two terminators. A bus segment consists of a termination, a 120-ohm transmission path (cable) with options containing drivers and receivers attached to it, and another terminaton in that order.

Characteristic Impedance (ZO) - The impedance presented to a traveling wave by a transmission line; equal to $\sqrt{L/C}$.

Cross-talk - Injection of a voltage or current spike into a signal line due to capacitive or inductive coupling from adjacent signal lines.

Daisy Chain - A bus signal that is broken at each module slot, which may be terminated or passed along by the insertion of a module with circuitry.

F11 LSI-11/23 - A family of programmable data processors. The F11 microprocessor chip set consists of the following parts:

57-00000-01 DAT/CTL
21-15542-01 MMU
57-00001-01 FP

Far End - The far end of the bus is the last bus interface slot (the near end is the first).

Finger - The point of contact between a signal on a module or a cable and the same signal on a backplane; also called a pin contact, connector, or connection point.

Interrupt Fielding Processor - Usually considered as part of the processor or processor module, this control logic arbitrates asynchronous interrupts from devices on the bus to determine which device has a higher priority. Once the priority is established, the processor acknowledges the interrupt.

Logic Reference - Return path or common power supply output for a logical reference voltage (i.e. with TTL a logic "1" might be 3.4 V with respect to logic reference). Sometimes referred to as ground.

LSI-11 - A family of programmable data processors based on the LSI-11 microprocessor chip set, which includes the following parts:

21-15579-00 DAT
23-002C4-00 CTL
23-001B5-00 MICROM
23-002B5-00 MICROM
23-003B5-00 MICROM

Master - The device, module or option that is currently controlling bus transactions. There can only be one bus master at a time.

Near End - The near end of the bus is the first bus interface slot (the far end is the last).

ODT, Online Debugging Technique (Halt Mode) - Some processors feature a console communication mode for debugging and starting programs from the Halt state, which is called ODT.

PC, Program Counter - A processor register that generally contains the address (memory location) of the next instruction to be executed.

PS, PSW, Processor Status Word - A processor register that contains data relevant to the status of the processor and the operation most recently completed; the data indicates what interrupt levels will be acknowledged and what some of the results of the most recently completed operation were.

Q-Bus - Any of a group of backplane and cable systems that carry the Q-Bus signals, including 18 lines for address delimitation.

Q22 Bus - Any of a group of backplane and cable systems that implement the Q-Bus signals and are capable of handling 22 lines for address delimitation.

Signal Skew - The difference in propagation delay between any two devices, one being at maximum propagation delay and the other being at minimum propagation delay.

Slave - A bus device that can be addressed by, and participate in bus transactions with a bus master. It has the subordinate role in a data transfer.

Slot - One of several locations into which a modular interface with the bus may be physically inserted.

Stack - An area of memory reserved for storing working program data. Under control of a processor register called the stack pointer, data is referred to as being pushed onto and popped off of the stack, in a last in, first out sequence.

State 0 - In devices whose logic proceeds through a series of states after power up, the initial, ready to begin work, state is often referred to as state 0.

Stub - A connection to a bus line that does not form part of the continuous conductor from near end to far end.

Victim - If signal transitions on one or more cable or etch conductors cause a voltage spike to develop on a nearby non-involved conductor, the non-involved conductor is designated as the victim.

2 BUS SIGNALS

2.1 PHYSICAL OVERVIEW

An LSI-11 computer system is basically a controlling processor, memory and I/O (input/output) devices. These devices are generally constructed on printed circuit boards, sometimes called modules, which connect to the bus via fingers.

Mechanical form factor/dimensions of dual and quad Digital modules can be found in DEC STD Ø3Ø, Module Manufacturing Standard. The fingers of the module plug into connectors whose pins become the LSI-11 Bus signal lines. These lines may be connected via etch or wires and these wires or etch on the back of the block become the backplane. Up to three backplanes may be connected by cables totaling a maximum of 16 feet. A total of 42 signal lines are used in the LSI-11 Bus. The signal lines are functionally divided as listed in Table 1.

Table 1. Summary of Signal Line Functions

Quantity	Function	Bus Signal Mnemonic
16	Data/Address Lines	BDAL<15:ØØ>
2	Memory Parity/Address Lines	BDAL<17:16>
4	Address Lines	BDAL<21:18>
6	Address and Data Transfer Control Lines	BSYNC, BDIN, BDOUT, BWTBT, BBS7, BRPLY
3	Direct Memory Access DMA Control Lines	BDMR, BDMG, BSACK
5	Interrupt Control Lines	BIRQ4, BIRQ5, BIRQ6, BIRQ7, BIAK
6	System Control Lines	BPOK, BDCOK, BINIT, BHALT, BREF, BEVNT

All LSI-11 Bus signals are asserted low and negated high, except BPOK and BDCOK, which are asserted high and negated low to indicate an event such as impending loss of power.

The asserted polarity of a bus signal is indicated by the letter L or H following the signal name. For example:

BDAL16 L or BDCOK H

LSI-11 Bus signals, with the exception of DMA grant and interrupt acknowledge signals, are bi-directional. This means they can be driven or received at any point along the signal line. When driven, bi-directional signals travel in two directions; from the driver to the near end terminator, and from the driver to the far end terminator. The exceptions are BIAKO L, BIAKI L, BDMGO L, and BDMGI L.

BIAKI L (Interrupt Acknowledge) is received by an LSI-11 Bus device on one pin and conditionally (depending on whether or not the device has the highest priority interrupt pending) re-transmitted out within 500 ns on a different pin as BIAKO L to the next device on the bus.

Bus wiring connects BIAKO L as output from one device to BIAKI L as input to the next device on the bus. BDMGI L and BDMGO L form a similar priority daisy chain for Bus Mastership Grant.

Devices connect to all Q-Bus lines via high impedance receivers and gated, high current, open-collector drivers.

2.2 BUS TRANSACTIONS OVERVIEW

There are four basic kinds of transactions that can take place over the bus:

a. Power up/down signal sequencing.
b. Transfer of bus mastership from bus master.
c. Transfer of data between a bus master and a slave.
d. Interrupts to the interrupt fielding processor.

These basic transactions and their variations occur within the constraints of protocols defined in the protocol section of this standard.

2.2.1 Power Up/Down Overview

When power is first applied, the BPOK H, BDCOK H and BINIT L signals initialize devices on the bus and cause the controlling processor to assume control (mastership) of the bus. The controlling processor may then execute some boot program or other power up option.

2.2.2 Transfer of Bus Mastership

The bus master initiates a transfer by placing the address of the slave device on the bus along with control signals. It then waits for the slave's reply and continues with the transfer according to the protocol. A bus cycle is not complete until the required master/slave signal sequence is completed. Thus, fast and slow devices, each determining its own bus cycle time, can connect to the bus.

2.2.3 Data Transfer Overview

Data transfers occur asynchronously within a master/slave relationship under a strict protocol defined in this standard (subhead 4.4). The controlling processor is generally the default bus master. It will relinquish bus mastership to any requesting device (sometimes referred to as a direct memory access or DMA device) when it is not currently using the bus. Any device that contains the appropriate circuitry may become the bus master and control data transfers over the bus to or from any slave device.

Because bus cycle completion by the bus master requires response from the slave device, each bus master must include a time out error circuit that will abort the bus cycle if the slave device does not respond within the required 1ø microseconds. Masters generally allow 12 microseconds.

2.2.4 Interrupts

Interrupts to the interrupt fielding processor from any device on the bus follow a unique protocol. When a device wishes to interrupt the processor, it asserts a request line. When the processor acknowledges the interrupt, the device places an address (called a vector) on the bus and the processor reads the contents of that address location and the following one to obtain a new PC and PSW.

The processor then executes the interrupt routine starting at the new PC. When the task is completed, the last instruction, RTI or RTT, restores the old PC and PSW from the stack. The processor then starts executing the instructions located at the address of the old PC (where it was interrupted). See processor handbooks for more detail on interrupt and PSW. Interrupts are prioritized and are described in detail in subhead 4.5.4.

2.3 SIGNALS AND PINS (Quantitative and Descriptive Overview)

A summary of LSI-11 bus signals and their pin assignments are listed in Table 2. Detailed functional descriptions are provided under subhead 6. The pin nomenclature is for reference and is only applicable when examining Digital modules constructed according to DEC STD ø3ø and Digital circuit schematics.

Table 2. LSI-11 Bus Signals and Pin Summary

Number of Pins	Functional Category	Digital's Nomenclature (name) (Pin)
16	Data/Address	BDAL0, BDAL1, BDAL2, BDAL3...BDAL15 AU2 AV2 BE2 BF2.....BV2
2	Memory Parity Control/ Error Address	BDAL16, BDAL17 AC1 AD1
4	Address	BDAL18, BDAL19, BDAL20, BDAL21 BC1 BD1 BE1 BF1
6	Address and Data Control	BDOUT, BRPLY, BDIN, BSYNC, BWTBT, BBS7 AE2 AF2 AH2 AJ2 AK2 AP2
6	Device Interrupt Control	BIRQ7, BIRQ6, BIRQ5, BIRQ4, BIAKO, BIAKI BP1 AB1 AA1 AL2 AN2 AM2
4	DMA Control	BDMR, BSACK, BDMGO, BDMGI AN1 BN1 AS2 AR2
6	System Control	BHALT, BREF, BEVNT, BINIT, BDCOK, BPOK AP1 AR1 BR1 AT2 BA1 BB1
4	S SPARES	AE1, AH1, BH1, AF1 (Slot 1 only: SRUN @ AF1)
4	M SPARES	AK1 & AL1, BK1 & BL1 (pairs connected)
2	P SPARES	AU1, BU1
2	+12B (battery)	AS1, BS1
1	+5B (battery)	AV1
3	+5 Vdc	AA2, BA2, BV1
2	+12 Vdc	AD2, BD2
2	-12 Vdc	AB2, BB2
8	GND	AC2, AJ1, AM1, AT1, BC2, BJ1, BM1, BT1
72	Total Pins	

3 ELECTRICAL CHARACTERISTICS

3.1 OVERVIEW AND DESIGN GOALS

The Q-Bus is designed to be the interconnect medium for devices that consist of small, LSI-based PDP-11 computing systems. Some of the design goals are:

a. That the customer's systems be expandable and upgradeable (i.e. not a bounded system)

b. That the bus will have well-controlled characteristics and clearly defined limits consistent with the term "small computer system".

c. That the number of bus signals be as small as possible, while consistent with PDP-11 functionality.

With these goals in mind, and a knowledge of available interconnection and transmission technology, the designers developed the Q-bus.

3.2 THEORETICAL DESIGN CENTER/Q-BUS SPECIFICATIONS

3.2.1 Backplanes

3.2.1.1 Maximum Number of Backplanes - A system can have either one, two, or three backplanes. Bus signals run from the near end of the first backplane to the far end of the last backplane.

3.2.1.2 Impedance of Wire or Etch - The characteristic impedance of a backplane signal line, with all other signal lines and logic references tied together, must be 120 ohms, $\pm$ 10%.

3.2.1.3 Maximum Resistance of a Signal Line - A signal line (wire or etch) must have a dc resistance of less than 0.1 ohm per signal line.

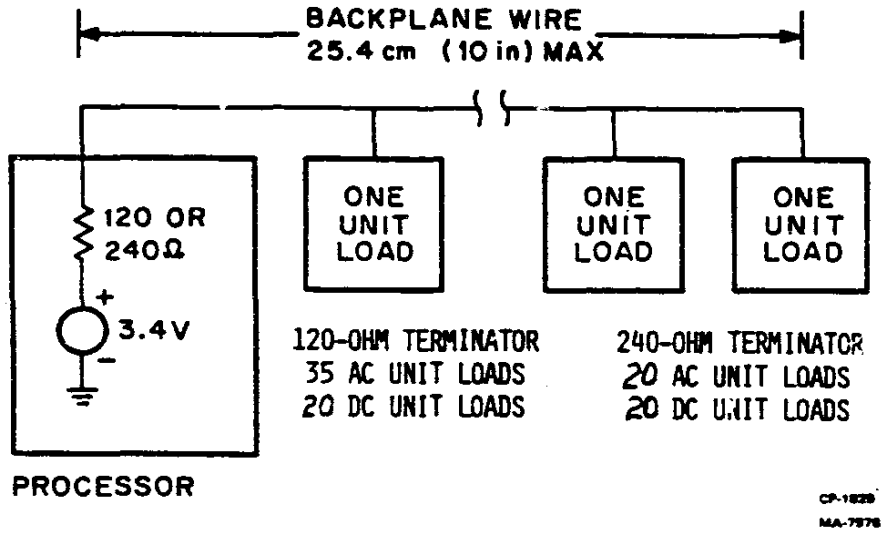


Figure 1. Minimum Configurations

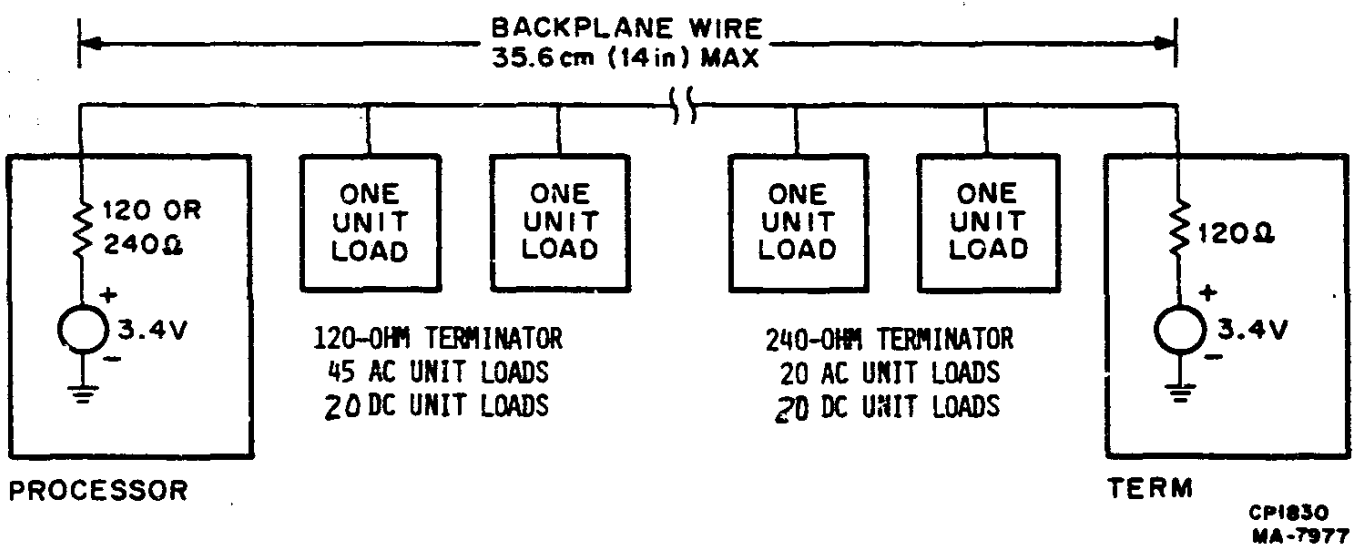
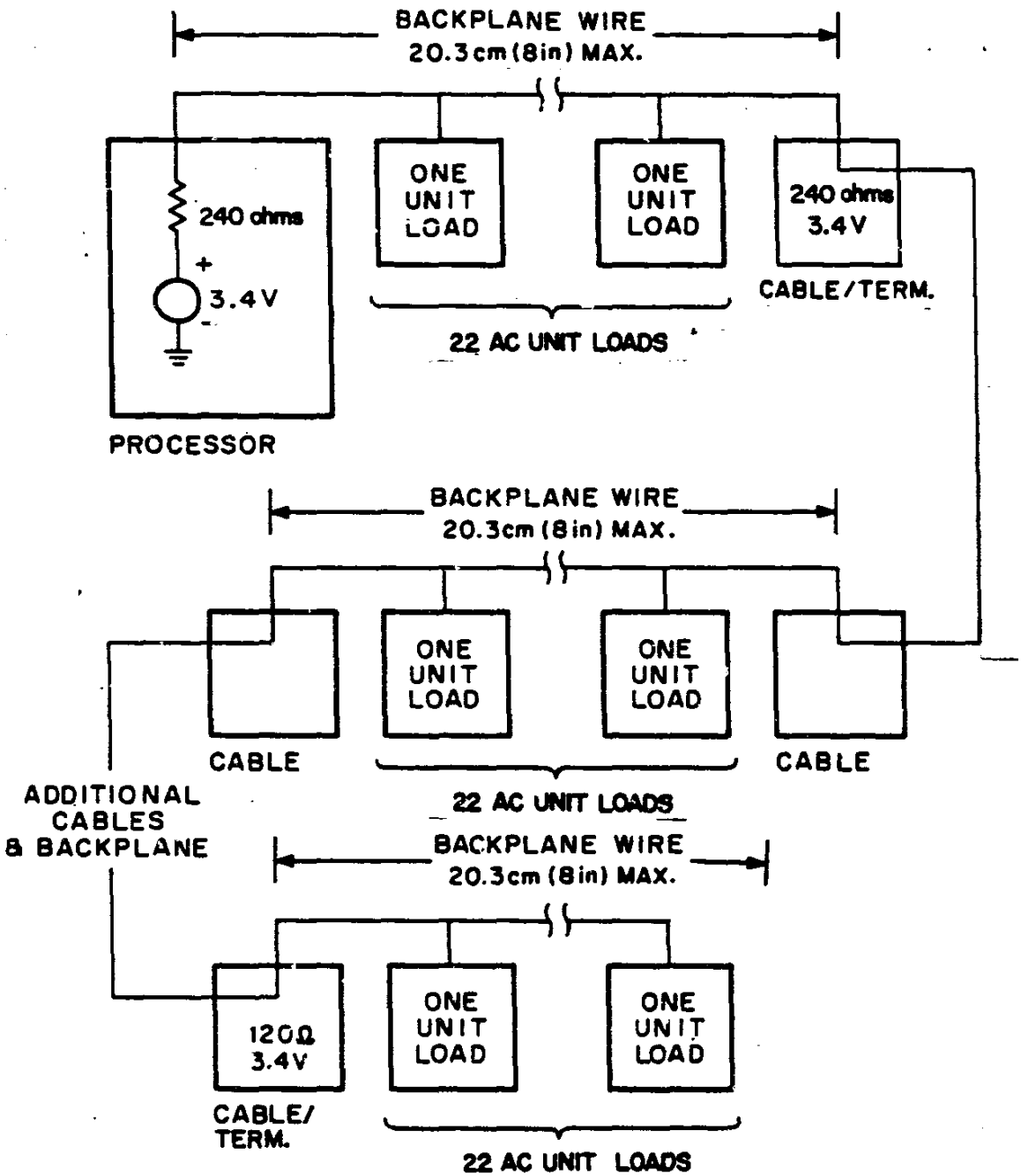


Figure 2. Intermediate Configurations



NOTES :

1. TWO CABLES (MAX.) 4.88m (16ft) (MAX.) TOTAL LENGTH.
2. 20 DC UNIT LOADS TOTAL (MAX.)

Figure 3. Maximum Configurations

CP-1831
MA-7978

3.2.2 Interconnect Cables

3.2.2.1 Impedance of Cable

With a two or more backplane system, an interconnect cable can be used to bus the backplanes together. This cable must have a characteristic impedance of 120 ohms, ± 20%.

3.2.2.2 **Maximum Length of Cable** - In a two backplane system, the interconnect cable (or cable set) must be between 2 and 16 feet long.

In a three backplane system, one of the two interconnect cables must be between 2 and 6 feet long; the other interconnect cable must be at least 4 feet long, but not more than 10 feet long.

3.2.2.3 **Maximum Crosstalk** - With a constant voltage of 5 volts on a given signal line (victim line), and a 8 ns rise/fall time pulse applied to all other signal lines simultaneously, the crosstalk on the victim line must be less than 5% of the 5 volts (or .25 volt). This must be true for both near and far ends of the cable.

3.2.3 Connection Points

3.2.3.1 **Maximum Contact Resistance** - A contact point (such as cable to cable header or module-to-backplane) must have a dc resistance of less than 0.02 ohm.

3.2.4 Return Path (or Logic Reference Line)

3.2.4.1 **Maximum Resistance** - Resistance of the common return path, (signal ground), as measured between near end and far end (including all intervening connectors, cables, backplane wiring, connection module etch, etc.) must not exceed an equivalent of 2 ohms per signal line path. This provides a return path resistance of not more than 2 ohms divided by 40 bus signal lines, or 50 milliohms.

3.2.4.2 Signal Path Routing - Logic reference, or the return path for bus receivers must be part of the bus signal distribution.

Common system, or power reference, (ground) must be routed a minimum of three inches outside of and away from the bus distribution path.

3.2.5 Bus Drivers and Receivers

3.2.5.1 Length of Etch from Driver/Receiver to Finger - From the module finger (module contact point) to the output pin of a driver or the input pin of a receiver, the length of etch must be less than two inches. Drivers and receivers are considered part of the bus even though they are located on the module

3.2.5.2 Driver and Receiver Power and Reference Separation - Drivers and Receivers should have adequate (50 mil nominal, 30 mil minimum) and separate power and reference etch. Power and logic reference paths must be direct from finger to IC (no tap offs are allowed, except at a finger).

3.2.5.3 Operating Temperature Range for Drivers and Receivers - Electrical specifications for drivers and receivers must be guaranteed between temperatures of 0° C and 70° C.

3.2.5.4 Operating Supply Voltage Range for Drivers and Receivers - Power supply voltage for a driver or receiver can vary between 4.75 volts and 5.25 volts dc without violating the specifications in this section.

3.2.5.5 Driver and Receiver Decoupling - Drivers and receivers must be properly decoupled per DEC STD 030, preferably with one 0.01 uF capacitor per IC.

3.2.5.6 Receiver Input Thresholds -

High Level Input Voltage (V_{IH}) Vcc = 5.0 V, $\pm$ 5%
1.90 V minimum

Low Level Input Voltage (V_{IL}) Vcc = 5.0 V, $\pm$ 5%
1.30 V maximum

Note

Future designs should try to conform to the 8641-2 specification for improved noise immunity.

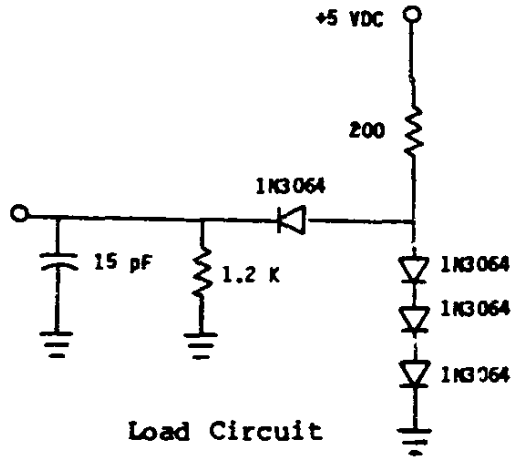
3.2.5.7 Receiver Propagation Delay - Propagation delay from the input of the receiver to the output of the receiver must not be greater than 35 ns. This value should be measured from the receiver input threshold voltage of 1.7 V, to an output voltage of 1.5 V. An input with a 10 ns rise/fall time with V between 0.8 V and 2.6 V must be used for the measurement. Loading of the output will be 390 ohms to +5 V and 1.6 kilohms to logic reference, with a capacitance of 50 pF to logic reference.

3.2.5.8 Receiver Skew - Any two receivers will have a maximum skew between them of 25 ns.

3.2.5.9 Receiver Noise Immunity - The current Q Bus receivers do not have a noise rejection specification. The following specification is recommended for new receiver designs:

Volts	Pulse Width (ns)	Transition Time
0.0 to 3.8	8	3.2 ns rise/fall
0.0 to 2.5	14	2.4 ns rise/fall
3.4 to -0.4	8	3.2 ns fall/rise
3.4 to 0.9	14	2.4 ns fall/rise

With a load circuit of 1.2 kilohms and 15 pF to ground, isolated by a 1N3064 diode from 200 ohms to +5 Vdc in series with three 1N3064 diodes to ground. See the following figure and the 8641-2 specification.



Load Circuit

3.2.5.10 Receiver Input Capacitance - A bus receiver can have a maximum input capacitance of 10 pF.

3.2.5.11 Receiver Leakage Current - With Vcc between 0.0 and 5.25 V dc, the maximum receiver leakage current is as follows:

High Level 80 ua @ 3.8 V dc
Low Level -10 ua @ 0.4 V dc

3.2.5.12 Driver Power Down Conditions - During power down of a bus driver, while it's asserting a bus signal, the driver must negate that signal and not glitch or assert the signal while power is off or during power down. Also, when a bus driver is not asserting a signal while powering down, it must not glitch or assert the signal.

3.2.5.13 Driver Output Voltages

Low Level output Voltage (V_{OL}) - 0.8 V maximum @ 70 mA

High Level Output Voltage - No high level output voltage is specified because bus drivers have open collector outputs and the specific voltage will depend on bus loading and bus terminators.

3.2.5.14 Driver Propagation Delay - Propagation delay from driver input to driver output, or from enable to driver output, with an input between 0.0 V and 3.0 V, a 10 ns rise/fall time, and with 91 ohms to +5.0 V and 200 ohms to logic reference, must not exceed 25 ns maximum @ 15 pF to logic reference.

3.2.5.15 Driver Skew - As is the case for a receiver, the skew between two bus drivers, one at maximum propagation delay and the other at minimum, must not exceed 25 ns maximum.

3.2.5.16 Driver Rise and Fall Times - Rise and fall times of drivers shall not be less than:

10 ns: with 15 pF to logic reference
25 ns: with 330 pF to logic reference

3.2.5.17 Driver Output Capacitance - A driver can contribute a maximum input capacitance of 10 pF.

3.2.5.18 Driver Leakage Current - With Vcc between 0.0 V and 5.25 V dc the maximum driver leakage current is as follows:

High Level 25 ua @ 3.8 V dc

Low Level -10 ua @ 0.4 V dc

3.2.6 Bus Loading

3.2.6.1 Dc Unit Load - A dc unit load is defined as 2100 mA, which is related to the amount of dc leakage current that a bus element presents to a bus signal line that is high (undriven).

3.2.6.2 Ac Unit Load - An ac unit load is defined as 9.35 pF, which is related to the impedance that a bus element presents to a bus signal line (due to backplane wiring, PC etch runs, receiver input loading and driver output loading).

3.2.6.3 Maximum Bus Dc Unit Loads - Total amount of dc unit loads allowed for the entire bus is 20 dc unit loads.

3.2.6.4 Maximum Bus Ac Unit Loads - Total ac loading allowed in a single backplane system is 45 ac unit loads with 120-ohm terminators.

Total ac loading allowed in a multiple backplane system is 22 ac unit loads per backplane.

Refer to document retrieval documents for data published about ac and dc loads. Values were determined using these documents.

3.2.6.5 Ac Loads Distribution

a. Capacitance must be distributed as evenly as possible along the bus. Lumped capacitance along a transmission line will cause reflections and cause timing relationships to be violated. To insure that a bus will be glitch-free, some analysis should be done to insure the proper placement of devices on the bus. One such analysis program is PAULI which can be run by Field Service.

b. Ac loads must also be distributed among the signal lines. That is no single signal line should have more then a 3 to 1 difference in ac loads present on the bus to another signal line.

3.2.7 Bus Terminators - Terminating Resistor Values

Resistor values that meet the following Thevinin equivalent should be used:

120 $\pm$ 5% to 3.4V

240 $\pm$ 5% to 3.4V

3.2.8 Maximum Q-Bus Skew

With 25 ns skew allowed for the bus transmission system and bus loading variations, the maximum Q-Bus skew is 75 ns. This is measured as the maximum difference in propagation delay from the input of driver to the output of a receiver.

3.2.9 Power Failure Control Signals

3.2.9.1 Shorting Element - Signal line BPOK H and BDCOK H are generated by the power supply control logic. When these signals (or a bus signal) are negated, they should be shorted to logic reference, according to DEC STD 186. A power supply reference other than logic reference, or chassis (earth reference) should never be used.

3.2.9.2 Glitch Rejection - Devices that monitor BPOK H to perform some operation should provide some type of glitch rejection upon receipt of BDCOK H. These devices should use a minimum of glitch rejection, as described in paragraph 3.2.5.9.

3.3 Q-BUS IMPLEMENTATION GUIDELINES

Guidelines presented in this section provide information for designing Q-Bus system from the electrical viewpoint. The information is derived from the specifications mentioned in subhead 3.2.

3.3.1 Backplanes

3.3.1.1 Length of Etch or Wire - Wire or etch for a signal line on each backplane can be a maximum of 8 inches in a multiple backplane system.

In a system with only a single backplane, the wire or etch length can be a maximum of 14 inches.

3.3.1.2 Connection Points - In a single backplane system, there can be 18 connection points (receiver/driver pair, cable conductor or terminator) to any bus signal line.

A two backplane system can have up to 12 connection points in each backplane.

Each backplane in a three backplane system can have up to 9 connection points.

3.3.1.3 Backplane Capacitance - The maximum capacitance allowed per signal line per backplane should be 68 pF. Capacitance of any signal line should be reduced as low as possible to increase signal integrity. (All signal lines should be kept as short as possible.)

3.3.2 Interconnect Cables

3.3.2.1 Allowable Cables - Cables that can be used for backplane interconnection are the BCV11A and BCV11B.

3.3.2.2 Signal Routing In Cables - To better control the impedance and crosstalk of a cable, the logic reference should be interweaved with signal lines.

3.3.3 Allowable Bus Interfaces

Below is a list of the ICs that can be used to drive and receive bus signals.

Type No.	Digital Part No.
DC003	19-12730-00
DC004	19-12729-00
DC005	19-13040-00
DC010	19-14038-00
DC021	Not available
8640	19-11469-00
8641	19-11579-00
8641-2	19-14987-00
8881	19-09705-00
2908	19-15305-00

Because the 8881 presents a variation to the allowable driver specification, the following guidelines must be observed when the driver is used.

3.3.3.1 - The driver must not be used to drive data/address, BBS7, or WTBT lines onto the bus.

3.3.3.2 - During a DMA request/grant (Figure 5), if the driver is used for RPLY then the 0 ns minimum specified from the negation of RPLY to the negation of SACK must be changed to 10 ns min.

3.3.3.3 - During a DATI or DATO (Figures 6 and 7), when the driver is used to drive SYNC, the relationship for the negation of SYNC to the assertion of the next SYNC should be changed from 200 ns min. to 210 ns min. Also, if the driver is used to drive RPLY, the specification for the negation of RPLY to the assertion of the next SYNC should be changed from 300 ns min. to 310 ns min.

In addition, during a DATO, if the driver is used to drive DOUT, the relationship for the negation of DOUT to the negation of SYNC must be changed from 175 ns min. to 185 ns min. and the relationship for the negation of DOUT to the release of the data lines or WTBT must be changed from 100 ns min. to 110 ns min.

3.3.3.4 - For the DATIO case (Figure 8), the DATO portion of the transfer must follow the same restrictions described in the above paragraphs that describe DATO timing relationships.

During the DATI portion of the transfer when the driver is used for RPLY, the relationship for the negation of RPLY to the assertion of DOUT must be changed from 200 ns min. to 210 ns min.

3.3.3.5 - A DATBI transaction has the same changes as the DATI transaction and in addition, when the driver is used for RPLY, the relationship for the negation of RPLY to the assertion of DIN must be changed from 150 ns min. to 160 ns min. and the relationship of the assertion of RPLY to the negation of DIN, when the driver is used to drive DIN, must be changed from 200 ns min. to 210 ns min.

3.3.3.6 - A DATBO transaction has the same changes as the DATO transaction and in addition, when the driver is used for RPLY, the relationship for the negation of RPLY to the assertion of DOUT must be changed from 150 ns min. to 160 ns min. and the relationship of the assertion of RPLY to the negation of DOUT, when the driver is used to drive DOUT, must be changed from 150 ns min. to 160 ns min.

3.3.3.7 - During an interrupt transaction (Figure 11) if RPLY is driven with that driver, the relationship for the negation of RPLY to the negation of the vector must be changed from 0 ns min. to 10 ns min.

3.3.3.8 - In addition, caution must be used when implementing the parity in Appendix A of this standard.

3.3.4 Allowable Terminating Resistors

In a single backplane system for a maximum of 20 ac or dc loads, including backplane, the near end term nation need only be a 330-ohm pull-up (to +5 V) and 680-ohm resistor to logic reference. No far end termination is needed for or small systems.

3.3.5 Variations

Deviations from this standard will produce systems that are difficult, if not impossible, to support. Only drivers and receivers listed or conforming to the specifications in this standard may be used on the bus. Designers of new systems and options should strive towards the specifications in this standard.

4 PROTOCOL

Throughout the following protocol specifications, bus signals are referred to in several different ways:

a. In general discussions where timing, polarity, and physical location are unimportant, the base signal name without any prefixes or suffixes is used. For example:

   SYNC, WTBT, BS7, DAL<17:00> or the DAL lines

b. Most signals on the backplane etch are asserted low and referred to with a prefix character B, and a suffix (space) L. For example:

   BSYNC L, BWTBT L, BBS7 L, BDAL<17:00> L

   BPOK H and BDCOK H are asserted high.

c. Receivers and drivers are considered part of the bus. Signal inputs to drivers are referred to with a prefix character T for transmit. For example:

   TSYNC, TWTBT, TBS7, TDAL<17:00>

d. Signal outputs of receivers are referred to with a prefix character R for received. For example:

   RSYNC, RWTBT, RBS7, RDAL<17:00>

Whenever timing is important, c and d above are used to reference timing to a receiver output or driver input. For example, after receipt of the negation of RDIN, the slave negates its TRPLY (0 ns minimum, 8000 ns maximum). It must maintain data valid on its TDAL lines until 0 ns minimum after negation of RDIN and must negate its TDAL lines 100 ns maximum after negation of its TRPLY.

4.1 POWER UP/DOWN PROTOCOL

Refer to the Timing Diagram in Figure 4.

4.1.1 Power Up

1. Power supply logic negates BDCOK H during power up and asserts BDCOK H 3 ms minimum after dc power is restored to voltages within specification.

2. The processor asserts BINIT L after receiving nominal power and negates BINIT L 0 nsec minimum after the assertion of BDCOK H.

3. Power supply logic negates BPOK H during power up and asserts BPOK H 70 ms minimum after the assertion of BDCOK H>. If power does not remain stable for 70 ms, BDCOK H will be negated, therefore, devices should suspend critical actions until BPOK H is asserted. The assertion of BPOK H will cause a processor interrupt.

4. BPOK H must remain asserted for a minimum of 3 ms. BDCOK H must remain asserted 4 ms minimum after the negation of BPOK H.

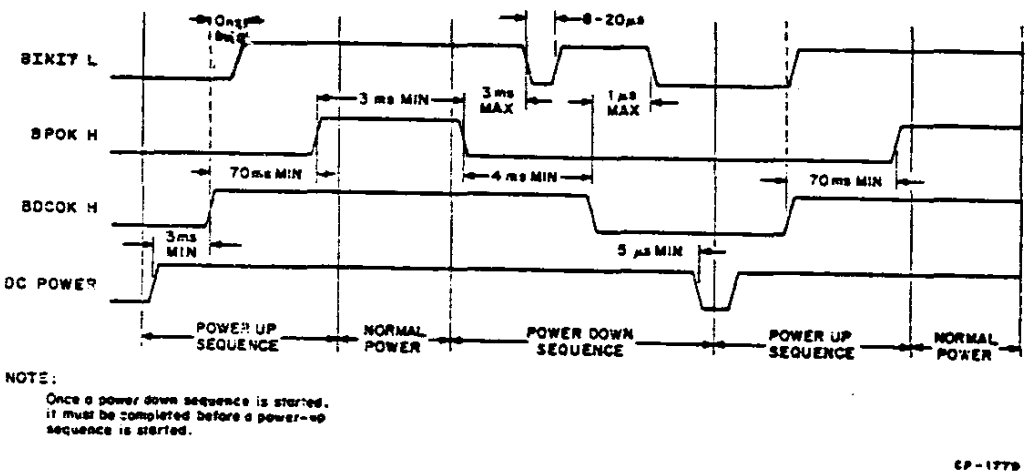


Figure 4. Power-Up/Power-Down Timing

4.1.2 Power Down

1. If the ac voltage to a power supply drops below 75% of the nominal voltage for one full line cycle (15 - 24 ms), BPOK H is negated by the power supply. Once BPOK H is negated the entire power down sequence must be completed.

   A device that requested bus mastership before the power failure, and has not become bus master, may maintain the request until BINIT L is asserted or the request is acknowledged (in which case regular bus protocol is followed).

2. Processor software should execute a RESET Instruction 3 ms minimum after the negation of BPOK H. This asserts BINIT L for from 8 to 20 us. Processor software executes a HALT instruction immediately following the RESET instruction.

3. BDCOK H must be negated a minimum of 4 ms after the negation of BPOK H. This 4 ms allows mass storage and similar devices to protect themselves against erasures and erroneous writes during a power failure.

4. The processor asserts BINIT L 1 us minimum after the negation of BDCOK H.

5. Dc power must remain stable for a minimum of 5 us after the negation of BDCOK H.

6. BDCOK H must remain negated for a minimum of 3 ms.

4.1.3 Implementation Guidelines

4.1.3.1 **Memories** - Memories must remain active during a power down sequence until the negation of BDCOK H. At that time, they must disable all read/write logic and reset all control logic.

4.1.3.2 **Bus Masters** - In general, no bus device should attempt to gain mastership of the bus during a power fail sequence. There are exceptions to this rule when system control functions, such as DMA refresh over the bus, or power failure code is executed in an attempt to save some valuable data.

4.1.3.3 **Bus Devices** - All non-memory bus devices must insure that all buffers, control and status registers, storage, sequential and state logic are initialized by the negation of BDCOK H.

When appropriate, bus devices should reset mechanical devices to starting or safe positions and prepare status information within the first 1 millisecond after the negation of BPOK H for interrogation during power fail code execution. As stated in 4.1.2, mass storage and similar devices must protect themselves from erasure and erroneous writes during this time.

During the negation of BDCOK H, all bus devices must insure that no bus signals are asserted. Devices may use BINIT L for initialization instead of BDCOK H. BINIT L is asserted by the processor whenever BDCOK H is negated. Refer to subheads 4.1.1 and 4.1.2.

4.1.4 Maximum Timing Specification

Where maximum times are not specified, a designer should try to remain as close to minimums as reasonable to reduce the amount of time required for the power up/down sequences.

4.2 INITIALIZATION

The processor asserts the BINIT L signal under the following conditions:

a. During a Power Down sequence as described in subhead 4.1.2.

b. During a Power Up sequence as described in subhead 4.1.1.

c. During the execution of a RESET instruction for 8 to 20 microseconds.

d. After detection of a "G" character in ODT for 8 to 20 microseconds.

4.2.1 Implementation Guidelines

All bus devices must initialize as described in subheads 4.1 and 4.2 on receipt of the BINIT L signal. There are certain exceptions that may be required for system control. For example, in some systems it is required that a UART be able to gain control of the system, by assertion of the BHALT L line to force the system into ODT Mode, or by assertion of the BDCOK H line to force a simulated power up, (refer to subhead 4.3, Boot Protocol). After detection of a certain character, without the interference of RESET instructions.

However, the UART must be clear of extraneous characters after the power up sequence. This can be accomplished by an AND of BDCOK H negated and BINIT L. This kind of special initialization condition must be carefully defined in the engineering and programming specifications for the device.

The intent of the BINIT L signal is to reset all devices on the bus to a state in which any bus device can be accessed by a controlling device. BINIT L is also intended to clear the bus. Good design dictates that certain operations in progress, such as the UART character transmission described above, should be completed. Similarly, it may be that certain status bits such as Parity Error or Parity Error Enable should not be reset at all except by software. These special conditions must be specified in the engineering and programming specifications for the device.

4.3 BOOT PROTOCOL

4.3.1 Hardware Boot

A hardware boot sequence can be accomplished by negating BPOK H for 4 ms minimum. At that point the power up/down protocol will be followed as described in section 4.1.

When BPOK H is negated the processor will be interrupted. The entire bus power up/down protocol must be followed. When BPOK H becomes asserted again, during power up, the processor proceeds to boot the system.

4.3.2 Software Boot

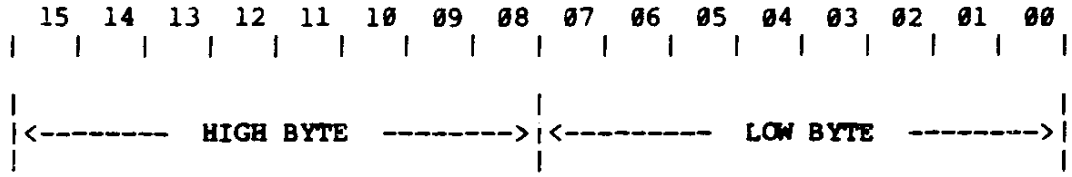
Under software control, the system can begin executing instructions at the starting address of the boot ROM (i.e. Jump instruction). BDCOK H is never negated and RESET INIT L is only asserted if the boot program performs the instruction.

4.4 DATA AND ADDRESS STRUCTURE OVERVIEW

The DAL lines and control signals are the physical means of implementation of the bus architecture. There are 18 bussed DAL lines, DAL<17:00>, in the Q-Bus, and 22 bussed DAL lines, DAL<21:00>, in the Q22-Bus. The control signals are the same on both.

4.4.1 Data Structure

The data structure in both busses is a 16-bit word comprised of high and low 8-bit bytes as illustrated below.



During the portion of the data transfer bus cycles in which data is being placed on the bus by the slave for the bus master, bit 17 may be asserted to inform the bus master that parity error detection logic on the bus master should be enabled. Bit 16 may be asserted to indicated that a parity error has occurred whenever one does occur.

Bits <21:17> are not currently used during the data out portion of the cycle and should not be asserted.

Bits <21:18> are not currently used during the data in portion of the cycle and should not be asserted.

4.4.2 Address Structure

On the Q22-Bus, devices are addressed by the BDAL lines and by the signal BBS7. The signal BSYNC is used as a reference to indicate that BDAL<21:00> and BBS7 have valid address information and that BWTBT contains valid control information.

The Q22-Bus supports systems with 16-, 18-, and 22-bit physical address space. In each instance, the top 4KW (8KB) of physical address space is designated as the I/O page address area. The processor and all other master devices assert BBS7 When referencing the I/O page. Note that the old Q-Bus supports 16- and 18-bit physical address spaces only.

I/O page devices respond to their device addresses, on BDAL<12:00>, if, and only if, BBS7 is asserted. Memory locations not in the I/O page respond to their addresses on BDAL<21:00> if, and only if, BBS7 is negated.

The 16-bit physical address space covers addresses from 000000 to 177777. The 16-bit I/O page is located from 160000 to 177777 for systems which support up to 28KW of memory.

The 18-bit physical address space covers addresses from 000000 to 777777. The 18-bit I/O page is located from 760000 to 777777.

The 22-bit physical address space covers adddresses from 00000000 to 17777777. The 22-bit I/O page is located from 17760000 to 17777777.

For all systems, virtual addresses 000 thru 376 are reserved for trap and interrupt vector addresses. In some larger systems virtual addresses 400 thru 776 are also reserved for interrupt vector addresses. Depending on how memory management is set up, the actual physical addresses may or may not coincide with their corresponding virtual addresses.

The one exception to the above rules involves special 16-bit systems which contain 30KW of memory. These systems support a reduced 2KW I/O page. Refer to subhead 4.4.5.

4.4.3 Definition Of The I/O Page

The Q-Bus has an 8 Kbyte address space designated as the I/O page which is accessed by assertion of BBS7 and by an address on BDAL<12:00>. The first 8 bytes of this space are reserved as non-existent for purposes of diagnostic testing. Bus masters can access the I/O page only by asserting BBS7.

A 16-bit processor, or a processor with memory management disabled, asserted BBS7 for addresses 160000 through 177777. A processor with 18-bit memory management enabled asserts BBS7 for addresses 760000 thru 777777. A processor with 22-bit memory management enabled asserts BBS7 for addresses 17760000 through 17777777.

A DMA bus master should automatically assert BBS7 whenever it generates an address in the top 8 Kbytes of its address space. Depending on whether the device supports 16-, 18-, or 22-bit addressing, it asserts BBS7 for address ranges 160000 through 177777, 760000 through 777777, or 17760000 through 17777777. Note that although it is not mandatory that a DMA device have the ability to access the I/O page, access to the initial I/O page location(s) is used by diagnostics for testing the device logic that detects non-existent memory.

Systems that support 30 Kwords of memory in 16-bit mode place an additional constraint on bus masters. Refer to subhead 4.4.5.

4.4.4 Definition of Memory Address Space

The Q-Bus memory address space is accessed by the negation of RBS7 and a numeric address (valid on the leading edge of RSYNC) on RDAL lines.

The 16-bit memory address space includes addresses 000000 through 157777 for systems that support up to 28KW of memory. The 18-bit memory address space covers addresses 000000 through 757777. The 22-bit memory address space covers addresses 00000000 through 17757777.

For special 16-bit systems which support 30KW of memory, the additional memory in address space 160000 through 167777 responds even when BBS7 is asserted. Refer to subhead 4.4.5.

4.4.5. Special 16-bit Systems with 30 KW Memory

Early Q-Bus CPU's, memories, and DMA devices were designed to support special 16-bit systems with 30 KW memory. 16-bit/30 KW systems allow a CPU without memory management to reduce the I/O page to 2 KW and thus increase the memory size. In these systems, each memory location between addresses 160000 and 167777 must respond to its address even if BBS7 is asserted. Also, all I/O page devices must be assigned device addresses at 170000 or above.

Future design intended for use on existing 16-bit/30 KW systems must observe the following guidelines:

1. A CPU module or DMA device supports 16-bit/30 KW systems only if, when running in 16-bit mode, it generates the correct 16-bit address on BDAL<21:16>. This means that BDAL<21:16> must remain unasserted even when BBS7 is asserted. For exmple, 160000 must not be converted to 760000 or 17760000.

2. Q-Bus memory modules are designed to access memory only if BBS7 is negated. A memory module supports 16-bit/30 KW systems only if it contains an option jumper that allows memory addresses 160000 through 167777 to respond even when BBS7 is asserted.

4.4.6 Interrupt Structure

Any bus device may assert one of the four interrupt request lines IRQ4, IRQ5, IRQ6, IRQ7 at any time during normal power. The interrupt fielding processor must be bus master and designed to service interrupts on a given line in order for service to be initiated. The processor asserts the Data In signal, DIN, and then an Interrupt Acknowedge signal, IACKO. There is an interrupt priority scheme that is described in subhead 4.5.4.2.

The interrupt requesting device with the highest priority asserts its TRPLY and then places a number called its vector on TDAL<08:02> with BDAL<21:9> and BDAL<01:00> equal to zero. It is important to note that the DAL lines are being used to transfer information during this asynchronous interrupt event. Conflicting use of the DAL lines by bus masters can only be avoided by adherence to the requirements for gaining bus mastership and initiating and terminating bus cycles outlined in the following sections. The vector is the address of a location in low memory that contains the starting address of a routine to accomplish what the interrupting device wants accomplished. The word location following the vector location contains a new value for the processor status word (PSW).

4.5 BUS MASTERSHIP PROTOCOL

The controlling processor is the default bus master. Any bus device containing the appropriate circuitry may become bus master and control data transfers over the bus. A DMA transaction can be divided into three phases:

a. Bus mastership acquisition protocol.

b. Data transfer protocol.

c. Bus mastership relinquish protocol.

4.5.1 Bus Mastership Acquisition and Relinquish

Refer to Figure 5.

1. A DMA Bus Master Device requests control of the bus by asserting TDMR.

2. The Bus Arbitration logic the processor asserts TDMGO 0 nsec minimum after RDMR asserts and 0 ns minimum after RSACK negates (if a DMA device was previous Bus Master).

3. The DMA Bus Master device asserts TSACK 0 ns minimum after the assertion of RDMGI; 0 ns minimum after the negation of RSYNC; and 0ns minimum after the negation of RRPLY.

4. The DMA Bus Master device negates TDMR 0 ns minimum after the assertion of TSACK.

5. The Bus Arbitration logic clears TDMGO 0 ns minimum after the assertion of TSACK. The bus arbitration logic must also negate TDMGO if RDMR negates or if RSACK fails to assert within 10 us ("No SACK" timeout).

6. The DMA Bus Master device has control of the Bus, and may gate TADDR onto the bus, when the conditions for asserting TSACK are met.

7. The DMA Bus Master negates TSACK 0 ns minimum after negation of the last RRPLY.

8. The DMA Bus Master negates TSYNC 300 ns maximum after it negates TSACK.

9. The DMA Bus Master must remove TDATA, TBS7, TWTBT, and TREF from the bus 100 ns maximum after clearing TSYNC.

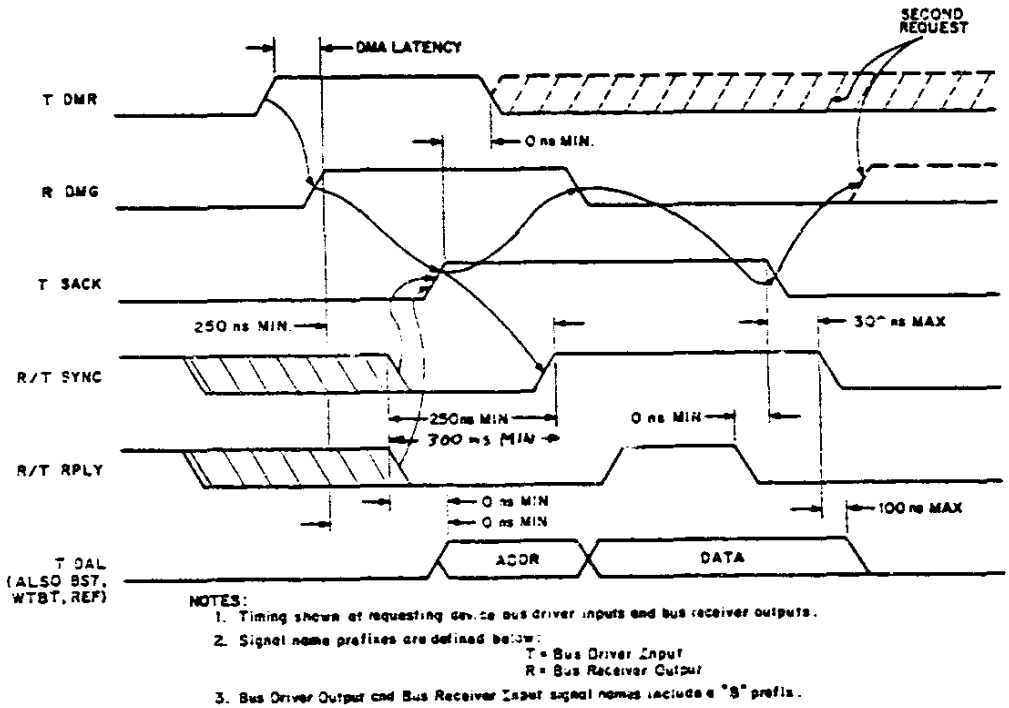


Figure 5. DMA Request/Grant Timing

4.5.2 Data Transfer Protocol

The seven types of data transfer bus cycles are listed in Table 3.

Table 3. Summary of Data Transfer Bus Cycles

Bus Cycle Mnemonic	Description	Function With Respect to Bus Master
DATI	Data word input	Read word
DATO	Data word output	Write word
DATOB	Data byte output	Write byte
DATIO	Data word input/output	Read word, modify, write word
DATIOB	Data word input/byte output	Read word, modify, write byte
DATBI	Data block input	Read block
DATBO	Data block output	Write block

These bus cycles, transfer 16-bit words or 8-bit bytes to or from slave devices. In block mode, multiple words may be transferred to sequential word addresses starting from a single bus address. In byte output operations, the data to be written in the destination byte is valid on the appropriate DAL lines.

4.5.2.1 Address Portion Of The Cycle -

1. As soon as a Bus Master gains control of the bus, it gates TADDR, TBS7, and TWTBT onto the Bus.

2. The Bus Master asserts TSYNC 150 ns minimum after it gates TADDR, TBS7, and TWTBT onto the Bus; 300 ns minimum after the negation of RRPLY; 250 ns minimum after the negation of RSYNC (if another device had asserted BSYNC); and 200 ns after the negation of TSYNC (if the current Bus Master had asserted BSYNC).

3. The Bus Master continues to gate TADDR, TBS7, and TWTBT onto the Bus for 100 ns minimum after the assertion of TSYNC.

Allowing for 75 ns bus skew, this timing provides all slave devices with 75 ns set up and 25 ns hold times minimum with respect to the rising edge of RSYNC. This allows slaves to compare the address on the bus with their address, and assert an internal device selected signal if a match exists.

If more than one data transfer is performed (without the use of block mode) while the device is bus master, the address portion of the cycle must be repeated for each transfer. TSACK must remain asserted, while TSYNC is negated a minimum of 0 ns after the negation of RRPLY, and then asserted again (for the next data transfer) a minimum of 200 ns after the negation of the last TSYNC and/or a minimum of 300 ns after the negation of RRPLY. TSACK is negated with the same restrictions as with one data transfer, after the last data transfer has been performed.

Note

In order for systems engineers to properly design and evaluate system performance, specifications for DMA devices must specify the following:

a. The maximum delay between bus mastership acquisition and initiation of the first bus cycle.

b. The maximum number of transfers per acquisition. The guidelines are:

Systems with memory refresh over the bus must not include devices that perform more than transfer per acquisition.

Bus masters that do not use Block Mode are limited to four DATI, four DATO, or two DATIO transfers per acquisition.

Block Mode bus masters that do not monitor RDMR are limited to eight transfers per acquisition.

Block Mode bus masters that do monitor RDMR may, if RDMR is not asserted after the seventh transfer, continue until the bus slave fails to assert BREF (16 transfers maximum). Otherwise, they stop after eight transfers.

Block Mode bus slaves must not cross 16-ward boundaries. This limitation facilitates cache design.

c. The maximum delay from bus acquisition to bus relinquish.

d. The minimum delay from bus relinquish until next request.

e. The maximum tolerable DMA latency.

4.5.2.2 Data Transfer Portion Of The Bus Cycle - The data transfer portion varies slightly for each type of data transfer. Details for each type of data transfer are provided in the following subheads 4.5.2.2.1 through 4.5.2.2.5.

4.5.2.2.1 DATI Bus Cycle -

1. Timing for the address portion of cycle is given in subhead 4.5.3. The Bus Master gates the negation of TWTBT along with the assertion of TADDR onto the bus.

2. The Bus Master asserts TDIN 100 ns minimum after asserting TSYNC.

3. The Bus Slave asserts TRPLY 0 ns minimum (8000 ns maximum to avoid Bus Timeout) after the assertion of RDIN.

4. The Bus Slave gates TDATA onto the Bus 0 ns minimum after the assertion of RDIN and 125 ns maximum after the assertion of TRPLY.

5. The BUS master receives stable RDATA from 200 ns maximum after the assertion of RRPLY until 20 ns minimum after the negation of TDIN. (The 20 ns minimum represents total minimum receiver delays for RDIN at the slave and RDATA at the Master.)

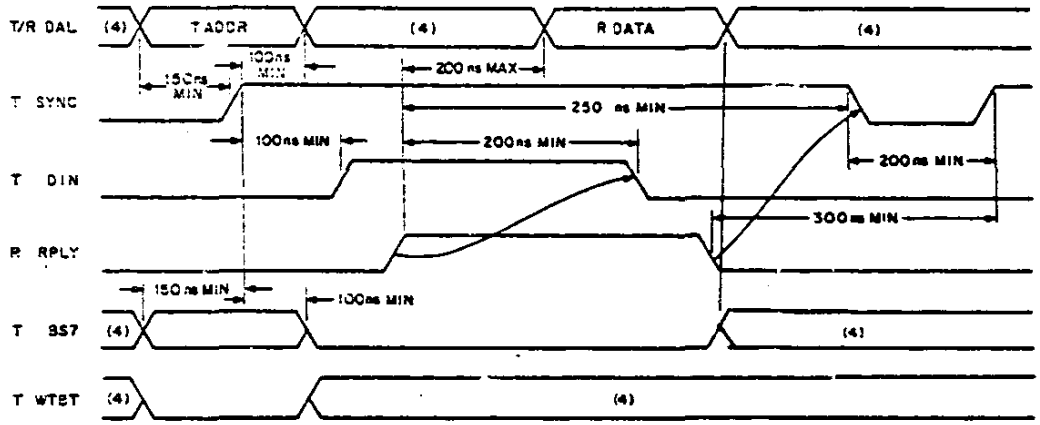
6. The Bus Master negates TDIN 200 ns minimum after the assertion of RRPLY.

7. The Bus Slave negates TRPLY 0 ns minimum after the negation of RDIN.

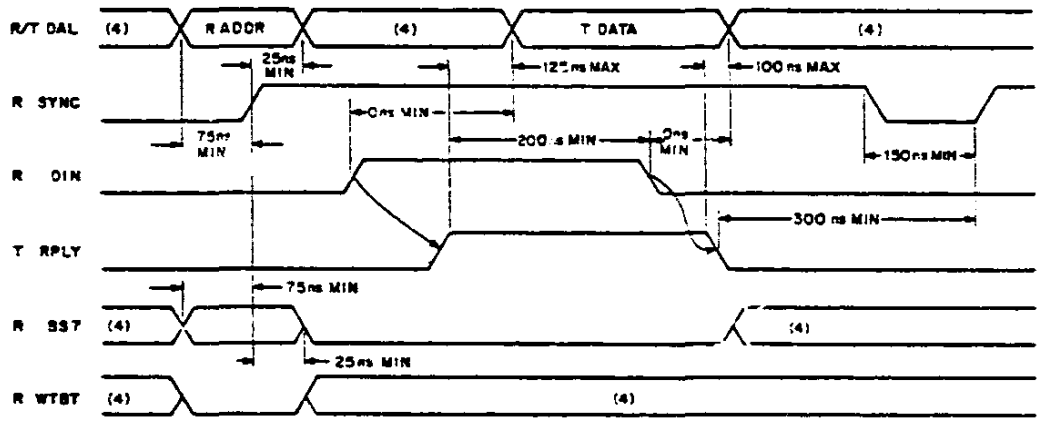
8. The Bus Slave continues to gate TDATA onto the Bus for 0 ns minimum and 100 ns maximum after negating TRPLY.

9. The Bus Master negates TSYNC 250 nsec minimum after the assertion of RRPLY and 0 ns minimum after the negation of RRPLY.

DAL<17> and DAL<16> may be used to force error indications for testing of error detection logic.



TIMING AT MASTER DEVICE



TIMING AT SLAVE DEVICE

NOTES:

1. Timing shown at Master and Slave Device Bus Driver Inputs and Bus Receiver Outputs.
2. Signal name prefixes are defined below:
   T = Bus Driver Input
   R = Bus Receiver Output
3. Bus Driver Output and Bus Receiver Input signal names include a "B" prefix.
4. Don't care condition.

Figure 6. DATI Bus Cycle Timing

4.5.2.2.1 DATO and DATOB Bus Cycles -

1. Timing for the address portion of the cycle is given in subhead 4.5.3. The Bus Master gates the assertion of TWTBT along with the assertion of TADDR onto the bus.

   The slave device may latch in the state of RWTBT at the same time as the device is selected (address match).

2. The Bus Master gates TDATA and TWTBT onto the Bus 100 ns minimum after TSYNC. TWTBT is negated for DATO Cycles and asserted for DATOB Cycles.

3. The Bus Master asserts TDOUT 100 ns minimum after gating TDATA onto the Bus.

4. The Bus Slave receives stable RDATA and RWTBT from 25 ns minimum before the assertion of RDOUT until 25 ns minimum after the negation of RDOUT.

5. The Bus Slave asserts TRPLY 0 ns minimum (8000 ns maximum to avoid Bus Timeout) after the assertion of RDOUT.

6. The Bus Master negates TDOUT 150 ns minimum after the assertion of RRPLY.

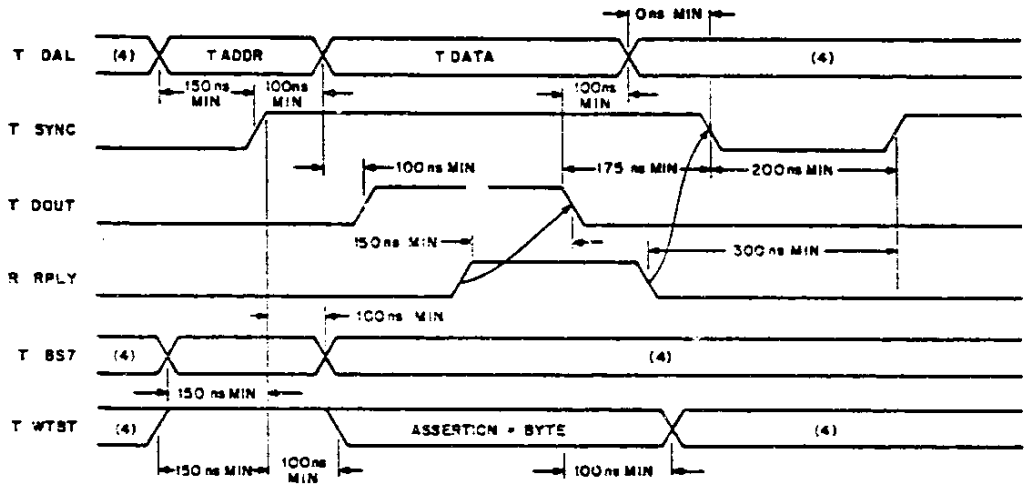
7. The Bus Master continues to gate TDATA and TWTBT onto the bus for 100 ns minimum after negating TDOUT.

8. The Bus Slave negates TRPLY 0 ns minimum after the negation of RDOUT.

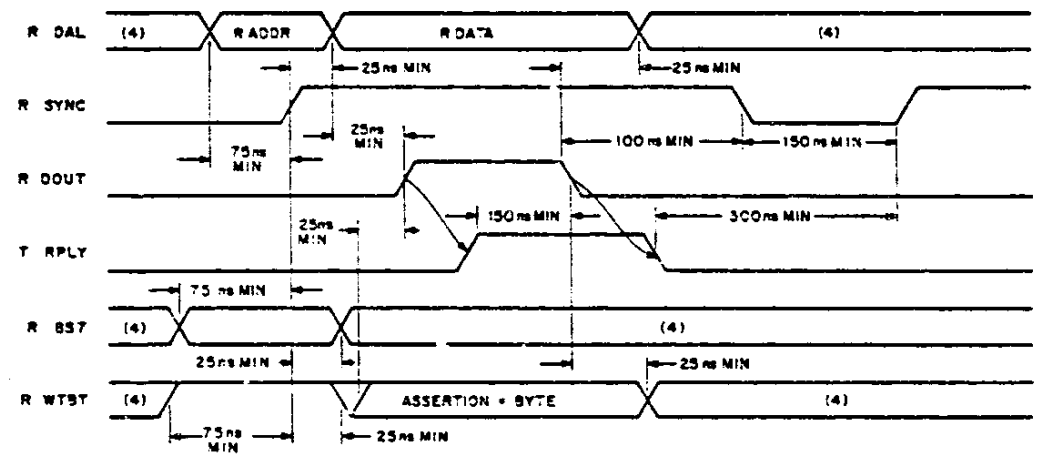
9. The Bus Master negates TSYNC 175 ns minimum after negating TDOUT, 0 ns minimum after removing TDATA and TWTBT from the Bus, and 0 ns minimum after the negation of RRPLY.

This completes the DATO cycle.

DAL<16> asserted during this data transfer will force a parity error simulation in some slave devices that have parity detection and error reporting logic.



TIMING AT MASTER DEVICE



TIMING AT SLAVE DEVICE

NOTES:

1. Timing shown at Master and Slave Device Bus D[ ] Inputs and Bus Receiver Outputs.
2. Signal name prefixes are defined below:
   T = Bus Driver Input
   R = Bus Receiver Output
3. Bus Driver Output and Bus Receiver Input signal names include a "B" prefix.
4. Don't care condition.

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Figure 7. DATO or DATOB Bus Cycle Timing

4.5.2.2.3 DATIO and DATIOB Bus Cycles -

1. Timing for the first portion of the DATIO and DATIOB Bus Cycles is the same as that given for the DATI Cycle in section 4.5.4.1 (timing relationships 1-8).

2. The Bus Master gates TDATA and TWTBT onto the Bus 0 ns minimum after latching the incoming data. TWTBT is negated for DATIO Cycles and asserted for DATIOB Cycles.

3. The Bus Master asserts TDOUT 200 ns minimum after the negation of RRPLY and 100 ns minimum after gating TDATA and TWTBT onto the Bus.

4. Timing for the last portion of the DATIO and DATIOB Bus Cycles is the same as that given for the DATO and DATOB Cycles (in section 4.5.4.2 (timing relationships 4-9).

TADDR<00> asserted indicates that the valid data during the DATOB data out portion of the transfer will be in the high byte DAL<15:08>. TADDR<00> negated during address time implies valid data on DAL<07:00>. DAL<16> may be used in both cases to force an error condition.

4.5.2.2.4 DATBI Bus Cycles -

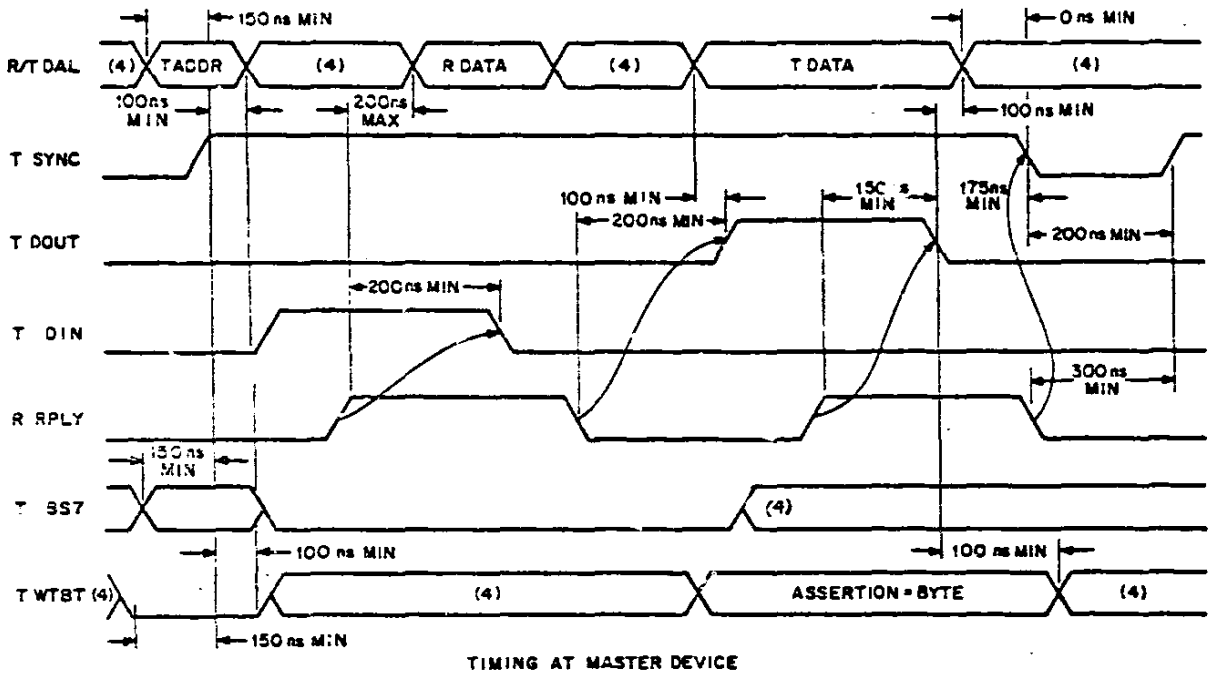
1. Timing for the address portion of the cycle is given in 4.5.3. The Bus Master gates the negation of TWTBT along with the assertion of TADDR onto the bus.

2. The Bus Master asserts the first TDIN 100 ns minimum after asserting TSYNC.

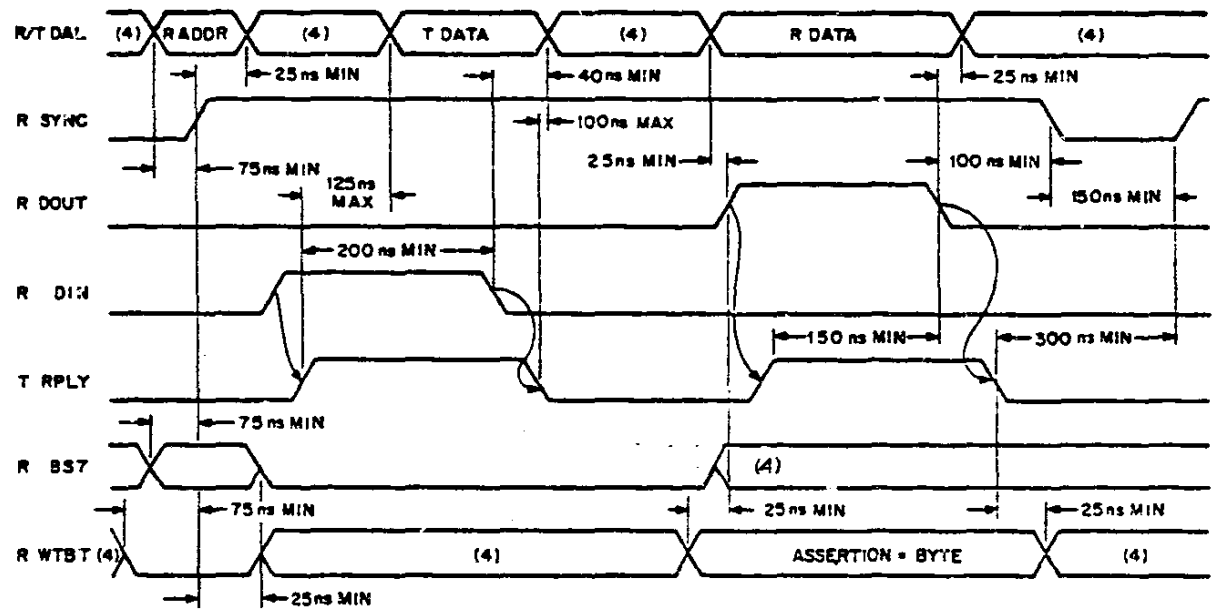
3. The Bus Master asserts TBS7 50 ns maximum after asserting TDIN for the first time. TBS7 remains asserted until 50 ns maximum after the assertion of TDIN for the last time. In each case, TBS7 can be asserted or negated as soon as the conditions for asserting TDIN are met.

Note

> The Bus Master must limit itself to not more than eight transfers unless it monitors RDMR. If it monitors RDMR, it may continue with blocks of eight so long as RDMR is not asserted at the end of each seventh transfer.



TIMING AT MASTER DEVICE



TIMING AT SLAVE DEVICE

NOTES:

1. Timing shown at Requesting Device Bus Driver inputs and Bus Receiver Outputs.
2. Signal name prefixes are defined below:
   T = Bus Driver Input
   R = Bus Receiver Output
3. Bus Driver Output and Bus Receiver Input signal names include a "B" prefix.
4. Don't care condition.

Figure 8. DATIO Bus Cycle Timing CP-1776

4. The Bus Slave asserts TRPLY 0 ns minimum (8000 ns maximum to avoid Bus Timeout) after the assertion of RDIN. The Bus Slave asserts TREF concurrent with TRPLY if, and only if, it is a block mode device which can support another RDIN after the current RDIN.

5. The Bus Slave gates TDATA onto the bus 0 ns minimum after the assertion of RDIN and 125 ns maximum after the assertion of TRPLY.

6. The Bus Master receives stable RDATA from 200 ns maximum after the assertion of RRPLY until 20 ns minimum after the negation of RDIN. (The 20 ns minimum represents total minimum receiver delays for RDIN at the slave and RDATA at the Master.)

7. The Bus Master negates TDIN 200 ns minimum after the assertion of RRPLY.

8. The Bus Slave negates TRPLY 0 ns minimum after the negation of RDIN.

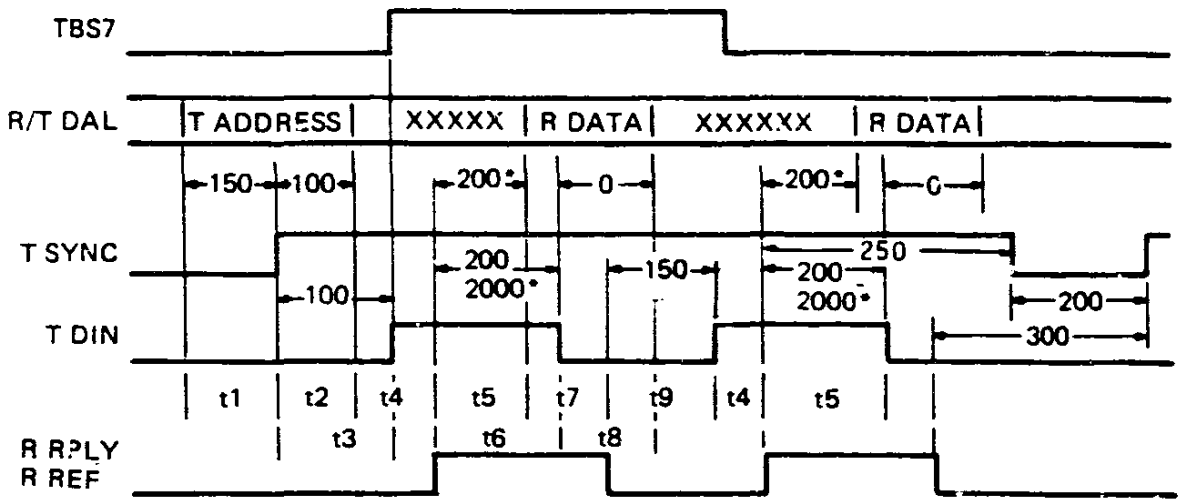
9. If RBS7 and TREF are both asserted when TRPLY negates, the Bus Slave prepares for another RDIN cycle. RBS7 is stable from 125 nsec after RDIN asserts until 150 ns after TRPLY negates.

10. If RBS7 and TREF are not both asserted when TRPLY negates, the Bus Slave removes TDATA from the Bus 0 ns minimum and 100 ns maximum after negating TRPLY.

11. If RREF and TBS7 were both asserted when TDIN negated (above, timing relationship 7), the Bus Master asserts TDIN 150 ns minimum after RRPLY negates and continues with timing relationship 3 above. RREF is stable from 75 nsec after RRPLY asserts until 20 ns minimum after TDIN negates. (The 20 ns minimum represents total minimum receiver delays for RDIN at the slave and RREF at the Master.)

12. If RREF and TBS7 were not both asserted when TDIN negated (above, timing relationship 7), the Bus Master negates TSYNC 250 ns minimum after the assertion of the last RRPLY 8 and 0 ns minimum after the negation of that last RRPLY.

SIGNALS AT BUS MASTER Times are min. except where "*" denotes max.



t1	=	address to T SYNC 150ns MIN.	
t2	=	address hold	100ns min
t3	=	T SYNC to T DIN	100ns min
t4	=	T DIN to R RPLY T (drive) + T (prop) + T (receive) + T (delay) + T (drive) + T (prop) + T (receive)	
t5	=	R RPLY to data	200ns max
t6	=	R RPLY to T DIN	200ns min
t7	= =	T DIN to R RPLY T (drive) + (prop) + T (receive) + T (delay) + T (drive + T (prop) + T (receive)	
t8	=	R RPLY to data	0ns min
t9	=	R RPLY to T DIN	150ns min
T cell	=	t4 + t6 + t7 + t9	–since t6 must be > t5 for master to have valid data - and t9 >t8

Figure 9. DATBI Bus Cycle Timing

4.5.2.2.5 DATBO Bus Cycles -

1. Timing for the address portion of the cycle is given in 4.5.3. The Bus Master gates the assertion of the TWTBT along with the assertion of TADDR onto the bus.

2. The Bus Master gates TDATA and TWTBT onto the bus 100 ns minimum after TSYNC. TWTBT is negated.

3. The Bus Master asserts TDOUT 100 ns minimum after gating TDATA onto the bus.

4. The Bus Slave receives stable RDATA and RWTBT from 25 ns minimum before the assertion of RDOUT until 25 ns minimum after the negation of RDOUT.

5. The Bus Slave asserts TRPLY 0 ns minimum after the assertion of RDOUT. The Bus Slave asserts TREF concurrent with TRPLY if, and only if, it is a block mode device which can support another RDOUT after the current RDOUT.

6. The Bus Master negates TDOUT 150 ns minimum after the assertion of RRPLY.

7. If RREF was asserted when RDOUT negated and the Bus Master wants to transmit more data in this Block Mode Cycle, then the Bus Master gates the new TDATA onto the Bus 100 ns minimum after negating TDOUT. RREF is stable from 75 ns maximum after RRPLY asserts until 20 ns minimum after RDIN negates. (The 20 ns minimum represents minimum receiver delays for RDIN at the slave and RREF at the Master.)

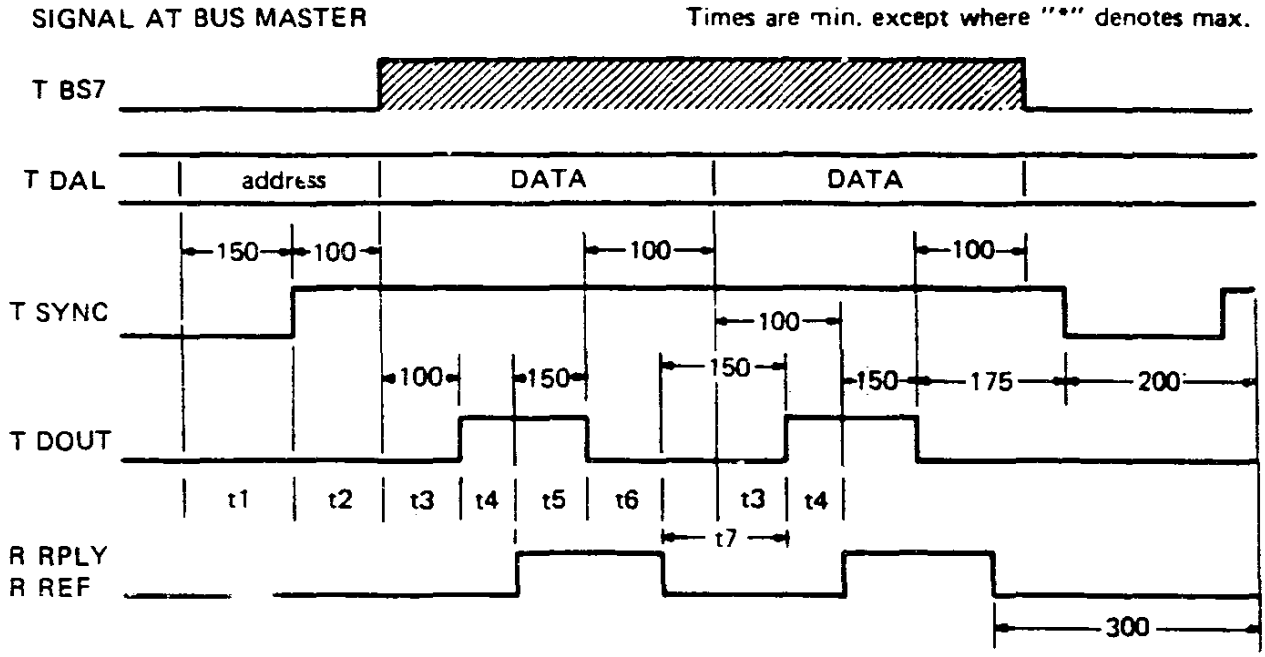
Note

> The Bus Master must limit itself to not more than eight transfers unless it monitors RDMR. If it monitors RDMR, it may perform up to 16 transfers as long as RDMR is not asserted at the end of the seventh transfer.

8. If RREF was not asserted when TDOUT was negated or if the Bus Master does not want to transmit more data in this Block Mode Cycle, then the Bus Master removes TDATA from the bus 100 ns minimum after negating TDOUT.

9. The Bus Slave negates TRPLY 0 ns minimum after the negation of TDOUT.

10. The Bus Master asserts TDOUT 100 ns minimum after gating new TDATA onto the Bus and 150 ns minimum after RRPLY negates. The cycle continues with the timing relationship in 4 above.



t1	=	address to T SYNC	150ns min
t2	=	address hold	100ns min
t3	=	data to T DOUT	100ns min
t4	=	T DOUT to R RPLY	
	=	T (drive) + T (prop) + T (receive) + T (delay) + T (drive) + T (prop) + T (receive)	
t5	=	R RPLY to T DOUT	150ns min
t6	=	T DOUT to R RPLY	
	=	T (drive) + T (prop) + T (receive) + T (delay) + T (drive) + T (prop) + T (receive)	
t7	=	R RPLY to T DOUT	150ns min
T cell	=	t3 + t4 + t5 + t6 + t7	—since t3 < t7

MA-7980

Figure 10. DATBO Bus Cycle Timing

4.5.3 Refresh Protocol

Dynamic random access memories require refresh at some interval. Data is stored in the form of a charged capacitance within each memory cell. The charge leaks off and must be restored periodically in what is called a refresh cycle. The Q-Bus provides a protocol for refreshing dynamic memory modules which do not contain on-board refresh circuitry.

When a refresh cycle is called for, the bus master performing the refresh asserts its TREF line a minimum of 200 ns before asserting TSYNC for the first refresh cycle.

Most dynamic memories are organized in some array of cells with, for example, 64 rows and 64 columns. A bank selected input enables/disables the entire array.

One field of the bus address (for example, DAL< 6:1>) corresponds to the row address. Another field (for example, DAL<12:7>) corresponds to the column, and another (for example, DAL<21:13>) to the bank.

When a memory module receives its RREF signal, it enables all its banks regardless of which bank is selected in the following address. It also disables its outputs. As each row is addressed, all cells on that row in all chips are refreshed by a process of reading the charge on the capacitor, amplifying it to a solid 1 or 0, then recharging the capacitor to that value.

The bus cycle involved is the standard DATI cycle, except that the bus master need only put the row address to be refreshed on the corresponding DAL lines at address time. The memory does not put data on the BDAL L lines during data time and the bus master does not input data from its RDAL lines.

The bus master may keep its TREF signal asserted throughout 64 (or whatever number of rows there are) continuous DATI/REF refresh cycles, or may do some smaller number of contiguous refresh cycles, negate TREF with the same timing as negation of TDIN, end the DATI/REF cycle normally, and later do some more.

Most dynamic memory cells require refresh once every 2 milliseconds. Approximately 130 microseconds are required to perform 64 contiguous refresh cycles, assuming the memory does not hold up RPLY or one refresh cycle every 30 microseconds will refresh 64 rows in 2 milliseconds. Only one memory module in the system should assert B RPLY L, during refresh, as selected by jumper during system configuration.

4.5.4 Interrupt Protocol

The LSI-11 Bus provides a protocol by which devices on the bus can temporarily suspend (interrupt) the execution of programs by the interrupt fielding processor. A device may require service for a variety of reasons, such as device ready, operation done or detection of some error condition.

Interrupt operations can also originate from within the processor. These interrupts are called traps and have priority levels determined by the processor design. Traps are caused by programming errors, special instructions and maintenance features.

Most external interrupting devices contain an addressable control and status register (CSR) which may contain a bit to enable/disable interrupts from the device. When conditions are right for a device to interrupt the processor, it does so by asserting one or more of the interrupt request lines IRQ4, IRQ5, IRQ6, IRQ7 according to protocol explained in the following paragraphs. The interrupt fielding processor frequently checks these lines for interrupts, generally after each fetch/execute cycle.

The processor generally also has a status register called the Processor Status Word (PSW). Three bits (generally bits 7:5) in this word can be be programmed to a number from 0 to 7. Only interrupts on a level higher than the number in this field of the PSW will be serviced by the processor. Thus, the processor can lock out external interrupts by writing a 7 in this field (340 in the PSW).

Interrupt request lines remain asserted until the processor initiates service or, the device's CSR Interrupt Enable bit is reset or the bus is initialized.

Software must lock out interrupts before resetting Interrupt Enable bits in devices CSR.

4.5.4.1 Interrupt Service Cycle -

1. The processor, as Bus Master, begins the interrupt service cycle by asserting TDIN. Note that TSYNC is not asserted during this cycle.

2. On the leading edge of RDIN, each bus option capable of requesting interrupts decides whether to accept or to pass on the RIAKI signal if it's received later in the cycle. That decision must be clocked into logic which settles within 150 ns maximum.

3. The Processor asserts TIAKO 225 ns minimum after the assertion of TDIN. This assures that the reception of RIAKI will not happen untill 150 us minimum after the assertion of RDIN at the device.

   The measure of interrupt latency is the time from assertion of IRQ until IACK is accepted by the interrupting device. A more comprehensive measure is the time from assertion of IRQ until completion of execution of the service routine, since interrupts can be nested.

4. Each Bus Option which receives the assertion of RIAKI either accepts it and becomes Bus Slave or passes it on to the next Bus option as TIAKO. Traditionally, the propagation time from BIAKI to BIAKO has been spec'd at 500 ns maximum, but 55 nsec typical.

5. The Bus Slave negates IRQ and asserts TRPLY 0 ns minimum after the assertion of RIAKI. Note that the Bus Slave must assert TRPLY 8000 ns maximum after RDIN to avoid a Bus Timeout.

6. The Bus Slave gates the Interrupt Vector (TVECT) address onto the Bus 125 ns maximum after asserting TRPLY.

   Because the vector is the first of a pair of addresses and because vectors are constrained to addresses between 0 and 777, only bits TDAL<08:02> are involved and no others should be asserted.

7. The Processor receives stable RVECT from 200 ns maximum after the assertion of RRPLY until 20 ns minimum after the negation of TIAKI. The 20 ns minimum represents the minimum receiver delays for RIAKI at the slave and RVECT at the master.

8. The Processor negates TDIN and TIAKO 200 ns minimum after the assertion of RRPLY.

9. The Bus Slave negates TRPLY 0 ns minimum after the negation of RIAKI.

10. The Bus Slave continues to gate TVECT onto the Bus for 0 ns minimum and 100 ns maximum after negating TRPLY.

4.5.4.2 Interrupt Priority Scheme - Devices decide whether or not to accept service on the rising edge of RDIN. Devices that monitor higher priority request lines must delay those lines by 60 ns (50 ns worst case bus skew plus 10 ns margin) to avoid the case where no device accepts service because a high-priority device posted a request just as or after it receives its RDIN and because of bus skews, the lower priority device receives the high-priority request line before it receives its RDIN.

Some systems are designed using devices that only assert IRQ4. In such systems priority is determined solely on the basis of position along the daisy chain which is the IACK signal. The closer to the processor, the higher the priority. If the RIACKI signal arrives and the device has an interrupt pending, it accepts the service and proceeds with the protocol. If the device does not have an interrupt pending, it passes the IACK to the next device on the chain by asserting its TIACKO within 500 ns maximum.

Other systems are designed using devices that are assigned one of four priority levels. Such systems must assert and monitor IRQ lines as follows:

Interrupt Level	Lines Asserted	Lines Monitored
4	TIRQ4	RIRQ5, RIRQ6
5	TIRQ4, TIRQ5	RIRQ6
6	TIRQ4, TIRQ6	RIRQ7
7	TIRQ4, TIRQ6, TIRQ7	------

This second scheme provides the maximum flexibility. Systems can be constructed using processors that only monitor level 4 interrupts or interrupts on all four levels. In addition, devices that only assert IRQ4 and do not monitor request lines can be used with devices that monitor higher priority request lines, as long as they are placed after them in the daisy chain.

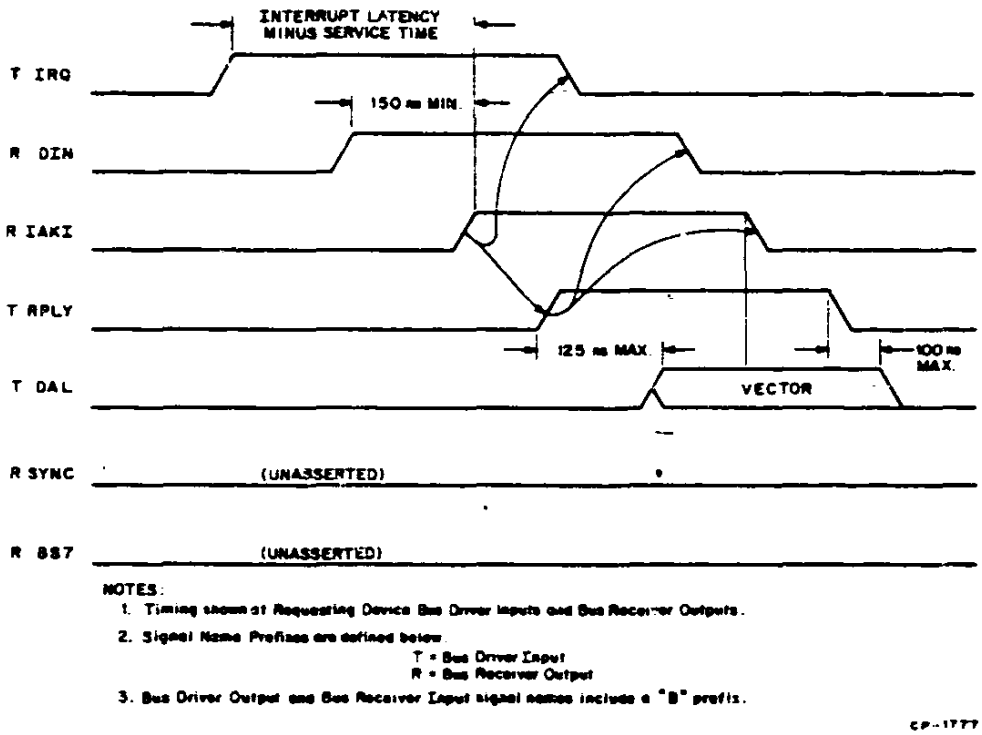


Figure 11. Interrupt Transaction Timing

4.5.5 EVENT and BPOK Protocol

One special class of interrupt on the LSI-11 Bus is incurred when the BEVENT L signal is asserted or the BPOK H signal is negated. These are asynchronous interrupts to the processor to which the processor assigns priority levels. The processor assumes that only one device in the system will assert these bus signal lines. It therefore does not go through the protocol for reading in the interrupt vector. It assigns location 100 as the vector address for EVENT and 24 for power fail and proceeds as usual to handle the interrupt.

4.5.6 HALT PROTOCOL

Assertion of the BHALT L line can be considered an interrupt to the processor. However, no interrupt vector is involved. The processor simply proceeds to its halt state as described in the processor handbook. The processor does not assert the BHALT L bus line when it comes to a programmed HALT.

5 ENVIRONMENTAL REQUIREMENTS

The Q-Bus, including all drivers, receivers, terminators, cables and power supplies must operate as specified over the worst case ranges (i.e., Class C) for devices enclosed in a box that is enclosed in a cabinet as specified in the following Digital Standards:

DEC STD 102	Environmental Standard For Computers and Peripherals
DEC STD 103 (proposed)	Electromagnetic Compatibility (EMC) Hardware Design Requirements
DEC STD 122	AC Power Line Standard

6 FUNCTIONAL DESCRIPTIONS OF BUS SIGNALS

Bus Pin	Signal Mnemonic	Signal Function
AA1	BIRQ5 L	Interrupt Request priority level 5
AB1	BIRQ6 L	Interrupt Request priority level 6
AC1	BDAL16 L	Address line 16 during addressing protocol; parity control line during data transfer protocol.
AD1	BDAL17 L	Address line 17 during addressing protocol; parity control line during data transfer protocol.
AE1	SSPARE1 alternate +5B	Special spare--not assigned or bussed in Digital cable or backplane assemblies; available for user connection. Optionally, this pin may be used for +5 V battery (+5B) backup power to keep critical circuits alive during power failures. A jumper is required on LSI-11 Bus options to open (disconnect) the +5B circuit in systems that use this line as SSPARE1.
AF1	SSPARE2 SRUN	Special spare--not assigned or bussed in Digital cable or backplane assemblies; available for user interconnection. In the highest priority device slot, the processor may use this pin for a signal to indicate its RUN state.

6 FUNCTIONAL DESCRIPTIONS OF BUS SIGNALS (Cont'd)

Bus Pin	Signal Mnemonic	Signal Function
AH1	SSPARE3	Special spare--not assigned nor bussed in Digital cable or backplane assemblies; available for user interconnection.
AJ1	GND	Ground--System signal and dc return.
AK1 AL1	MSPAREA MSPAREB	Maintenance Spare--Normally connected together on the backplane at each option location (not a slot-to-slot bussed connection).
AM1	GND	Ground--System signal and dc return.
AN1	BDMRL	Direct Memory Access (DMA) Request--device asserts this signal to request bus mastership.
AP1	BHALT L	Processor Halt--When BHALT L is asserted, the processor responds by going into its halt state (generally console ODT mode.)
AR1	BREF L	Memory refresh--used during refresh protocol to override memory bank selection decoding and cause all banks to be selected. Asserted or negated with BRPLY L by Block Mode Slave Devices to indicate to the Bus Master if the slave can accept another Block Mode DIN or DOUT transfer.
AS1	+5B or +12B battery	+12 or +5 V dc battery backup power to keep critical circuits alive during power failures. This signal is not bussed to BS1 in all Digital backplanes. A jumper is required on all LSI-11 Bus options to open (disconnect) the backup circuit from the bus in systems that use this line at the alternate voltage.
AT1	GND	Ground--Systems signal and dc return.
AU1	PSPARE1	Power spare 1 (not assigned a function; not recommended for use). If a backplane is bussing -12 V (on pin BB2) and a module is accidentally inserted upsidedown in the backplane, -12 V dc appears on pin AU1. If AU1 is unused on the module, no damage will occur.
AV1	+5B	+5 V Battery Backup Power--to keep critical circuits alive during power failures.

6 FUNCTIONAL DESCRIPTIONS OF BUS SIGNALS (Cont'd)

Bus Pin	Signal Mnemonic	Signal Function
BA1	BDCOK H	DC Power OK--Power supply generated signal that is asserted when there is sufficient dc voltage available to sustain reliable system operation. Part of Power up and Power down protocol and Boot protocol.
BB1	BPOK H	AC Power OK--Asserted by the power supply when primary power is normal. When negated during processor operation, a power fail trap sequence is initiated. Part of Power up and Power down protocol
BC1	SSPARE 4 BDAL 18L	Special spares <7:4> in older (per 122-Bus) LSI-11 Bus Systems. Not assigned nor bussed in Non Q22-Bus cable and backplane assemblies.
BD1	SSPARE 5 BDAL 19L	Address Lines <21:18> Bussed in Q22-Bus Backplane and Cable assemblies.
BE1	SSPARE 6 BDAL 20L	**CAUTION:** These pins may have been used as test points in some Digital or customer options. These options must be modified or designated incompatible with Q22-Bus backplanes.
BF1	SSPARE 7 BDAL 21L	
BH1	SSPARE 8	Special Spare - Not assigned nor bussed in Digital cable or backplane assemblies available for user interconnection.
BJ1	GND	Ground--System signal and dc return.
BK1 BL1	MSPAREB MSPAREB	Maintenance Spares--Normally connected together on the backplane at each option location (not a slot to slot bussed connection).
BM1	GND	Ground--System signal and dc return.
BN1	BSACK L	This signal is asserted by a DMA device in reponse to the processor's BDMGO L signal, indicating that the DMA device is accepting bus mastership. Device remains bus master until it negates BSACK L.
BP1	BIRQ 7 L	Interrupt request priority level 7.

6 FUNCTIONAL DESCRIPTIONS OF BUS SIGNALS (Cont'd)

Bus Pin	Signal Mnemonic	Signal Function
BR1	BEVNT L	External Event Interrupt Request--The processor latches the leading edge and arbitrates as an interrupt. A typical use of this signal is a line time clock interrupt.
BS1	+12B	+12 V dc battery backup power (not bussed to AS1 in all Digital backplanes)
BT1	GND	Ground--system signal and dc return.
BU1	PSPARE2	Power spare 2 (not assigned a function, not recommended for use). If a backplane is bussing -12V (on pin AB2) and a module is accidently inserted upsidedown in the backplane, -12 Vdc appears on pin BU1. If BU1 is unused on the module, no damage will occur.
BV1	+5	+5 V power--Normal +5 V dc system power
AA2	+5	+5 V power--Normal +5 V dc system power
AB2	-12	-12 V Power-- -12 V dc (optional) power for devices requiring this voltage.
AC2	GND	Ground--System signal and dc return.
AD2	+12	+12 V Power-- Normal +12 V dc system power
AE2	BDOUT L	Data Output--BDOUT, when asserted, implies that valid data is available on BDAL <15:0> L and that an output transfer, with respect to the bus master device, is taking place. BDOUT L is de-skewed with respect to data on the bus.
AF2	BRPLY L	Reply--BRPLY L is asserted in reponse to BDIN L or BDOUT L and during IAK transaction. It is generated by a slave device to indicate that it will place its' data on the BDAL bus or that it will accept data from the bus, according to the appropriate protocol.

6 FUNCTIONAL DESCRIPTIONS OF BUS SIGNALS (Cont'd)

Bus Pin	Signal Mnemonic	Signal Function
AH2	BDIN L	Data Input--BDIN L is used for two types of bus operation: 1. When asserted during BSYNC L time, BDIN L implies an input transfer with respect to the current bus master and requires a response (BRPLY L) from the addressed slave. 2. The interrupt fielding processor initiates interrupt service by asserting TDIN L followed by TIACK L.
AJ2	BSYNC L	Synchronize--BSYNC L is asserted by the bus master device to indicate that it has placed an address on the bus. The transfer is in process until BSYNC L is negated. In block mode BSYNC L remains asserted until the last transfer cycle is completed.
AK2	BWTBT L	Write/Byte--BWTBT L is used in two ways to control a bus cycle: 1. It is asserted during the address portion of a cycle to indicate that an output cycle is to follow (DATO, DATOB, DATBO) rather than an input cycle. 2. It is asserted during the Data portion of a DATOB or DATIOB bus cycle, to indicate a byte rather than a word transfer is to take place.
AL2	BIRQ4 L	Interrupt request priority level 4.
AM2 AN2	BIAKI L BIAKO L	Interrupt acknowledge--In accordance with interrupt protocol, the processor asserts BIAKO L to acknowledge an interrupt. The bus transmits this to BIAKI L of the next priority device (electrically closest to the processor). This device accepts the Interrupt Acknowledge under two conditions: 1. The device requested the bus by asserting an interrupt, BIRQX L. and 2. The device had the highest priority interrupt request on the bus at the time of the preceeding BDIN L assertion.

6 FUNCTIONAL DESCRIPTIONS OF BUS SIGNALS (Cont'd)

Bus Pin	Signal Mnemonic	Signal Function
		If both of these conditions are not met, the device asserts BIAKO L to the next device on the bus. This process continues in a daisy-chain fashion until the device with the highest interrupt priority receives the Interrupt Acknowledge (IAK) signal and proceeds with Interrupt Protocol.
AP2	BBS7 L	Bank 7 select--When the Bus Master asserts TADDR, it assert this signal to reference the I/O page (including that portion of the I/O page reserved for nonexistent memory). The address on BDAL <12:0> L when BBS7 L is asserted is the address within the I/O page. During DATBI Transfers, the Bus Master asserts this signal with the first data transfer until the last transfer to indicate to the Block Mode slave that there will be subsequent transfers.
AR2 AS2	BDMGI L BDMGO L	Direct memory access grant--The bus arbitrator asserts this signal to grant bus mastership to a requesting device, according to bus mastership protocol. The signal is passed in a daisy-chain from the arbitrator (as BDMGO L) through the bus to BDMGI L of the next priority device (electrically closest device on the bus). This device accepts the grant only if it requested to be bus master (by assertion BDMR L). If not, the device passes the grant (asserts BDMGO L) to the next device on the bus. This process continues until the requesting device acknowledges the grant by asserting BSACK L after BRPLY L and BSYNC L are both negated.
AT2	BINIT L	Initialize--This signal is used for system reset. All devices on the bus are to return to a known, initial state; i.e., registers are reset to zero, all Bus drivers are diabled and logic is reset to state 0, ready to be addressed for operations. Exceptions should be completely documented in programming and engineering specifications for the device.
AU2	BDAL0 L	Data/address line 00. Specifies high or low byte during address for DATOB and DATIOB cycles.
AV2	BDAL1 L	Data/address line 01.
BA2	+5	+5 V dc power.

6 FUNCTIONAL DESCRIPTIONS OF BUS SIGNALS (Cont'd)

Bus Pin	Signal Mnemonic	Signal Function
BB2	-12	-12 V dc power (optional, not required for DIGITAL LSI-11 or F11 hardware options).
BC2	GND	Power supply return.
BD2	+12	+12 V dc power.
BE2	BDAL2 L	Data/address line 02.
BF2	BDAL3 L	Data/address line 03.
BH2	BDAL4 L	Data/address line 04.
BJ2	BDAL5 L	Data/address line 05.
BK2	BDAL6 L	Data/address line 06.
BL2	BDAL7 L	Data/address line 07.
BM2	BDAL8 L	Data/address line 08.
BN2	BDAL9 L	Data/address line 09.
BP2	BDAL10 L	Data/address line 10.
BR2	BDAL11 L	Data/address line 11.
BS2	BDAL12 L	Data/address line 12.
BT2	BDAL13 L	Data/address line 13.
BU2	BDAL14 L	Data/address line 14.
BV2	BDAL15 L	Data/address line 15.

APPENDIX A

Q22-BUS PARITY

Note

> The bus parity protocol described in this Appendix is an optional extension to the Q-Bus specification. Devices that use this protocol are compatible with devices that do not use it. Bus parity checks occur only if both the master and slave have implemented bus parity.

Bus parity provides single bit parity on address transfers and byte parity on data transfers. Parity information for both address and data is transferred during data cycles on the four most significant data/address lines. The bus master checks parity during data in transfers; the bus slave checks parity during data out transfers.

A.1 BUS PARITY PROTOCOL

Bus parity is checked for both address and data cycles during DATI, DATO, and DATIO transactions. Bus parity is also checked during interrupt vector fetches and block mode DATBI and DATBO transactions. For all transactions except interrupt vector fetches, bus parity information for both address and data is gated onto bus lines BDAL21-18 when data is gated onto BDAL15-00. Bus parity on the address is calculated by both bus master and bus slave during the address cycle and the two results are compared during the data cycle(s). For interrupt vector fetches, bus parity information is gated onto BDAL21-19 while the interrupt vector is gated onto BDAL15-00. Because there is no address cycle, there is no address parity.

A.2 BUS PARITY DURING DATI TRANSACTIONS

A DATI transaction consists of an address cycle followed by a single data in cycle. During the address cycle, the bus master gates a 22-bit address onto BDAL21-00, asserting BBS7 for I/O Page references. Both master and slave devices calculate odd parity on BDAL21-00 and BBS7. However, during I/O Page references, both slave and master ignore BDAL21-13 and calculate parity as if those bits were all zeros. During the data in Cycle, the bus slave gates data onto BDAL15-00, asserts BDAL17 and BDAL16 if a memory parity error has been detected and gates the following bus parity information onto BDAL21-18:

BDAL2 Bus Parity On. The bus slave asserts this bit if it supports bus parity.

BDAL20 Data HB Parity. The bus slave calculates odd parity for BDAL15-00 and gates it onto this line.

BDAL19 Data LB Parity. The bus slave calculates odd parity for BDAL07-00 and gates it onto this line.

BDAL18 Address Parity. The bus slave gates onto this line the odd parity it calculated during the address cycle.

The bus master checks bus parity for the high and low data bytes and compares the slaves address parity bit with its own address parity bit. When a bus parity error is detected, the bus master would typically halt operation and interrupt the CPU. Figure A-1 shows a typical DATI transaction with bus parity. Bus signal timing is the same as for the DATI transaction described in subhead 4.5.4.1.

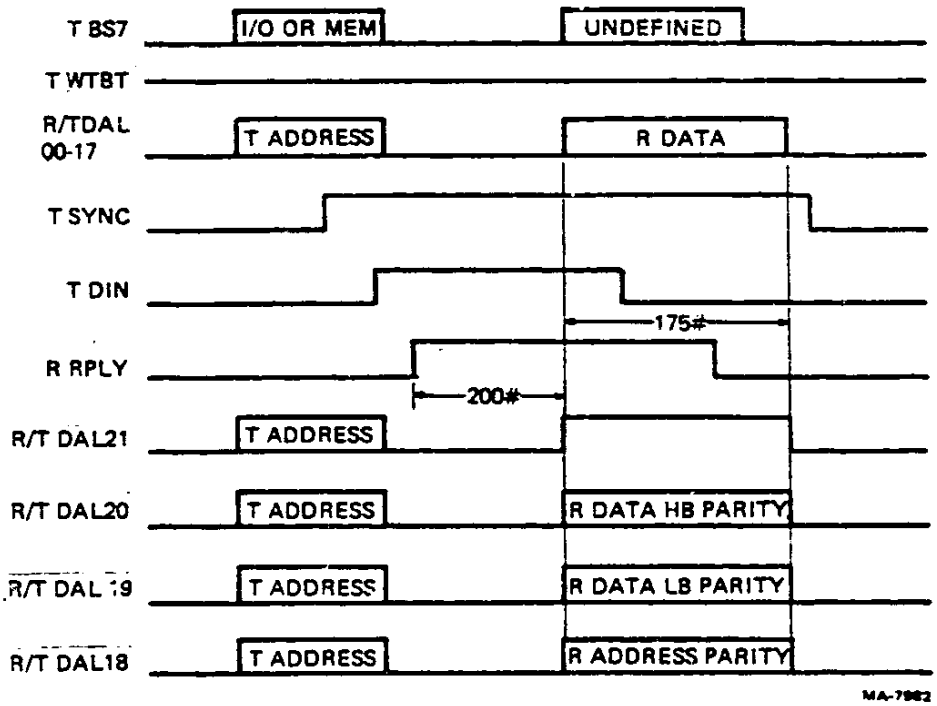


Figure A-1. DATI Timing Diagram at Master (with Parity)

A.3 BUS PARITY DURING DATO TRANSACTIONS

A DATO transaction consists of an address cycle followed by a single data out cycle. During the address cycle, the bus master gates a 22-bit address onto BDAL21-00, asserting BBS7 for I/O Page references. Both the master and slave devices calculate odd parity on BDAL21-00 and BBS7. However, during I/O Page references, both slave and master ignore BDAL21-13 and calculate parity as if those bits were all zeros. During the data out cycle, the bus master gates data onto BDAL15-00, and gates the following bus parity information onto BDAL21-18:

BDAL21 **Bus parity on.** The bus master asserts this bit if it supports bus parity.

BDAL20 **Data HB Parity.** The bus master calculates odd parity for BDAL15-08 and gates it onto this line.

BDAL19 **Data LB Parity.** The bus master calculates odd parity for BDAL07-00 and gates it onto this line.

BDAL18 **Address Parity.** The bus master gates onto this line the odd parity it calculated during the address cycle.

The slave device checks parity for the high and low data bytes and for the address. Figure A-2 shows a typical DATO transaction with bus parity. Bus signal timing relationships are the same as for a DATO described in subhead 4.5.4.2.

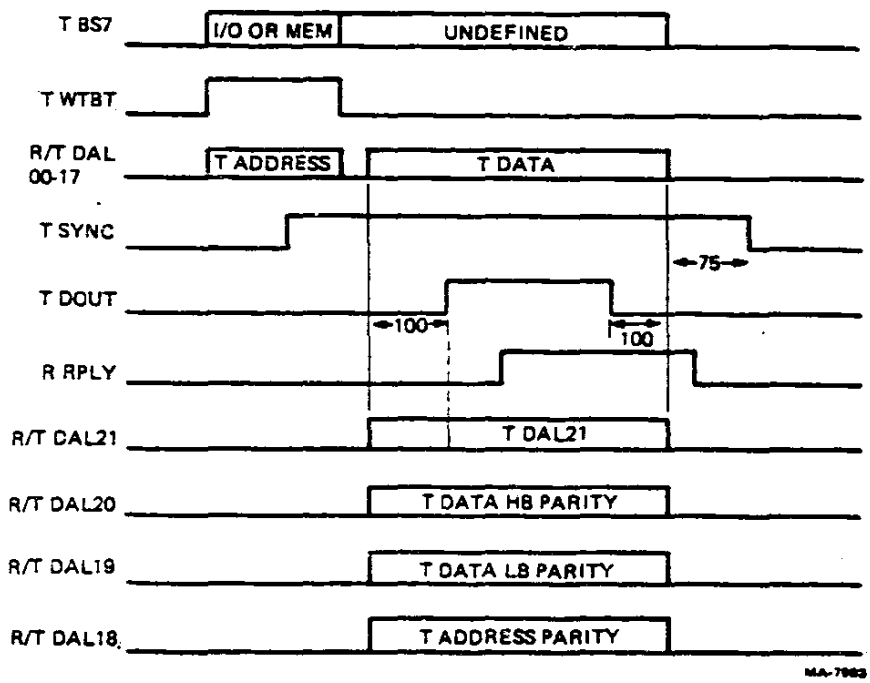


Figure A-2. DATO Timing Diagram at Master (with Parity)

A.4 BUS PARITY DURING DATIO TRANSACTIONS

A DATIO transaction consists of an address cycle followed first by a data in cycle and then by a data out cycle. During the address cycle, the bus master gated a 22-bit address onto BDAL21-00, asserting BBS7 for I/O Page references. Both master and slave devices calculate odd parity on BDAL21-00 and BBS7. However, during I/O Page references, both slave and master ignore BDAL21-13 and calculate parity as if those bits were all zeros. During the data in cycle, the bus slave gates parity information onto BDAL21-18 and data onto BDAL15-00. This bus parity information is identical to that listed in subhead A.2 for DATI cycles.

The bus master checks bus parity for the high and low data bytes and compares the slaves address parity bit with its own address parity bit. When a bus parity error is detected, the bus master would typically halt operation and interrupt the CPU.

During the data out cycle, the bus master gates data onto BDAL15-00, and gates bus parity information onto BDAL21-18. This bus parity information is identical to that listed in subhead A.3 for DATO cycles.

The bus slave checks parity for high and low data bytes and address.

A.5 BUS PARITY DURING DATBI TRANSACTIONS

A DATBI transaction consists of an address cycle followed by two or more Data In cycles. The bus protocol procedure is identical to that described in subhead A.2 for DATI transactions. During each data in cycle, the bus slave gates bus parity information onto BDAL21-18. The bus master checks both address and data parity for the first cycle. The bus slave provides the address parity bit for succeeding cycles as well, but the bus master may, at its option, ignore it and check only data parity.

A.6 BUS PARITY DURING DATBO TRANSACTIONS

A DATBO transaction consists of an address cycle followed by two or more Data Out cycles. The bus protocol procedure is identical to that described in subhead A.3 for DATO transactions. During each data out cycle, the bus master gates bus parity information onto BDAL21-18. The bus master provides the address parity bits for succeeding cycles as well, but the bus slave may, at its option, ignore it and check only data parity.

A.7 BUS PARITY DURING INTERRUPT VECTOR FETCHES

An interrupt vector fetch consists of a modified data in cycle. The DIN signal causes each multi-level interrupt device to examine the bus request lines and to determine whether a higher priority device has requested an interrupt. The first device which did not detect a higher priority level responds to the BIAK signal, gates its vector address onto BDAL15-00 and gates the following information onto BDAL21-19:

BDAL21 Bus Parity On. The bus slave asserts this bit if it supports bus parity.

BDAL20 Data HB Parity. The bus slave calculates odd parity for BDAL15-08 and gates it onto this line.

BDAL19 Data LB Parity. The bus slave calculates odd parity for BDAL07-00 and gates it onto this line.

The processor checks bus parity for the high and low data bytes. When a bus parity error is detected, the bus master would typically halt operation and interrupt the CPU. Figure A-3 shows a typical interrupt request with parity. All the timing relationships are the same as for an interrupt request described in subhead 4.5.6.

A.8 POTENTIAL RESPONSES TO PARITY ERRORS

The master and slave response to bus parity errors has implications for system software as well as for system hardware. During "data in" transfers the bus master detects any bus parity errors. A DMA device, that supports bus parity, should set an error bit, halt operation, and interrupt the CPU. If the CPU that supports bus parity is bus master, it should halt execution of the current program and trap to an error handling routine. During "data out" cycles, however, the bus slave detects any bus parity errors.

When the slave detects a parity error, BRPLY is suppressed if a bus parity error is detected. If a DMA device is bus master, it would halt operation, set a non-existent memory indication, and interrupt the CPU. If the CPU is bus master, it would trap to non-existent trap location 4. For consistency, the CPU could block BRPLY and trap to location 4 when a bus parity error is detected during "data in" cycles.

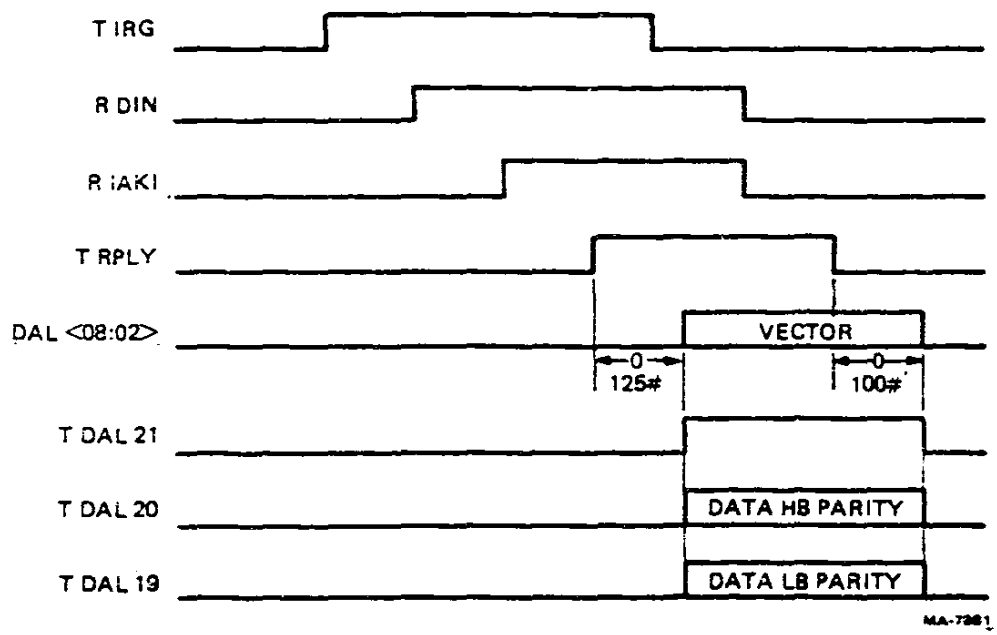


Figure A-3. Interrupt Request Timing Diagram at Slave (with Parity)

DEC STANDARD 160 SEC. 1 REV. A

HISTORY OF LSI-11 BUS

TITLE: LSI-11 BUS SPECIFICATION - HISTORY OF THE LSI-11 BUS

ABSTRACT: This section of DEC STD 160 describes earlier versions of the LSI-11 Bus for historical reference. It is not a design specification.

FOR INTERNAL USE ONLY

DATE	ECO #	ORIGINATOR	APPROVED	REV
17-Sep-81		Bill Newton	Eng. Comm. Carl Noelke, Sec'y	A

Document Identifier

Size	Code	Number	Rev
A	DS	EL00160-01-0	A

digital

SECTION 1 - HISTORY OF THE LSI-11 BUS

TABLE OF CONTENTS/REVISION STATUS

1 INTRODUCTION

The LSI-11 Bus has envolved from 16 and 18 bit bus address versions to the current version that is specified in Section 0 of this standard.

1.1 PURPOSE

The purpose of this section of the standard is to document the earlier versions of the LSI-11 Bus for reference purposes. It is not intended to be a specification for new product design. However, it could be useful if a new product design requirement includes backward compatibility with older LSI-11 Bus devices.

1.2 SCOPE

This section applies only to out-of-date versions of the LSI-11 Bus. The scope is limited to describing the major differences between older versions and the current LSI-11 Bus that is described in Section 0.

1.3 RESPONSIBILITIES

Refer to Section 0, subhead 1.3.

1.4 REFERENCED STANDARD

Refer to Section 0, subhead 1.4.

2 BUS SIGNALS

2.1 PHYSICAL OVERVIEW

The earlier versions of the LSI-11 Bus included only 38 signal lines (instead of the 42 signal lines currently inclued). The signal line functions are summarized in Table 1.

2.2 BUS TRANSACTIONS OVERVIEW

Refer to Section 0, subhead 2.2.

Table 1. Summary of Signal Line Functions

Qty	Functions	Bus Signal Mnemonic
16	Data and address lines	BDAL <15:00> L
2	Memory parity or address lines	BDAL <17:16> L
6	Address and data/Transfer control lines	BSYNC L, BDIN L, BDOUT L, BWTBT L, BBS7 L, BRPLY L
3	Direct memory access control lines	BDMGI L, BDMGO L, BSACK L
5	Interrupt control lines	BIRQ4 L, BIRQ7 L, BIAKI L, BIAKO L
6	System control lines	BPOK H, BDCOK H, BINIT L, BREF L, BHALT L, BEVNT L

2.2.1 Power Down Protocol Exception

During a power down sequency BPOK H is used to indicate that power is about to fail and BDCOK H is going to be negated. Some older CPU's perform fast DIN's to monitor bus signals during the time between BPOK H negation and BDCOK H negation. Upon the negation of BDCOK H, BINIT L is generated which will cause a initilization of the bus during a data transfer (DIN). Some non-volatile memories will not tolerate this, resulting in memory data alterations. One such CPU is the PDP 11/03. User's should beware of the consequences of performing a power down sequence with this processor.

2.2.2 DATO Protocol Exception

Some Digital microprocessors perform don't care DATIs before a DATO (or a DATIO) during every DATO. Designers should be aware of this when designing new bus options.

2.3 SIGNALS AND PINS

The signals and their pin assignments for earlier versions of the LSI-11 Bus are listed in Table 2.

3 BOOT PROTOCOL

Some systems may require fast initialization or restart of the system software without going through a power down and up again. This is provided by the boot protocol and selection of processor. A power up mode that causes the processor to execute a small program out of ROM, (sometimes called a bootstrap program) is used to initialize the software system.

The boot protocol is followed to negate the BDCOK H signal long enough for the processor to reset itself and assert BINIT L. See Figure 1.

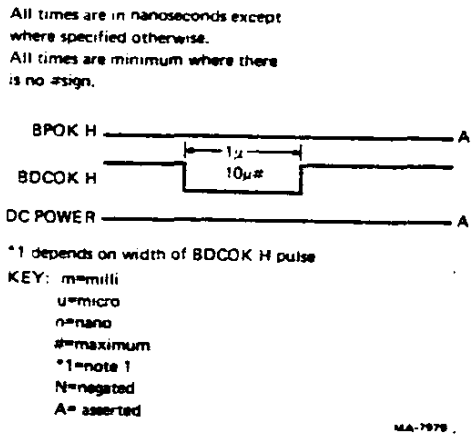


Figure 1. Boot Timing Diagram

BDCOK H should be negated for a minimum of 100 nanoseconds, maximum of 10 microseconds.

The BINIT L signal will be generated by the controlling processor in the same way as described in the power up and power down protocols.

It should be clear from the care taken in the power down protocol that activation of the boot protocol (usually done by human intervention) is risky business. Mechanical devices in operation when the switch is pressed may malfunction. To date, no Digital devices have been designed to self destruct on Boot, but the potential is there. System designers and mechanical device designers must be aware, and design their devices to respond properly to power up, power down, initialize and boot protocols. Boot protocol is similar to a false start, except that BPOK H and DC POWER remain high, and BDCOK H is negated for a maximum of 10 microseconds instead of a minimum of 3 milliseconds. Boot protocol might better be named START or better yet, RESTART protocol.

4 WAKE UP CIRCUIT

Some of Digital's processors have an option called a wake up circuit. This circuit monitors +5 V dc and holds the BDCOK H line negated until approximately 1 second after nominal 5 V power is applied to the good power and a fully initialized system. Therefore, it should only be used in very small systems where the system owner is aware of the consequences and is certain that no device in that system requires the power up protocol. Q-Bus systems with non-Digital power supplies that do not generate BPOK H at all will also be missing the power down protocol and may be subject to disk erasures, loss of status information, loss of core memory data, etc.

5 ELECTRICAL CHARACTERISTICS

5.1 BACKPLANE EXCEPTION

Early LSI-11 Bus backplanes that do not meet the ideal 120-ohm guideline are listed below:

Backplane	Characteristic Impedance
H9273	43 ohms, (.055 mh, 30 pF)
H9281	76 ohms, (.055 uh, 9.5 pF)
DDV11B	45 ohms, (.200 uh, 70 pF)
H9270	50 ohms, (0.12 uh, 52 pF)
*Ideal	120 ohms, (0.12 uh, 8 pF)

5.2 TTL BUS

It is possible to construct a very small system using TTL. This would be a one-backplane system, with the etch conductors as short as possible (10 inches, maximum). Not more than three open-collector TTL drivers and three TTL receivers are allowed, per signal line. The 330-ohm, pull-up resistor to + 5 V dc and the 680-ohm resistor to ground, available on most Digital Q-Bus CPUs, may be used as the open-collector driver pull-up.

This type of system is essentially a user-designed system. It is not recommended nor is the reliability guaranteed.

5.3 DEVIATIONS FROM 120-OHM CABLE

120-ohm cables are expensive and physically difficult to terminate. For example, the BCV11A and BCV11B cables use a cable that is nominally 120 ohm ± 2%, but is actually 170-ohms for center conductors and 210 ohms for outside conductors.

5.4 DRIVERS AND RECEIVERS SPECIFICATIONS EXCEPTION

5.4.1 Receiver Input Voltage

High Level Input Voltage

1.53 V minimum @ Vcc = 4.75 V
1.61 V minimum @ Vcc = 5.00 V
1.70 V minimum @ Vcc = 5.25 V

Low Level Input Voltage

1.30 V maximum @ Vcc = 4.75 V
1.38 V maximum @ Vcc = 5.00 V
1.47 V maximum @ Vcc = 5.25 V

5.4.2 Driver Output Voltage

.08 V maximum @ 70 ma
.05 V maximum @ 16 ma

Drivers and receivers to meet the nearly ideal specification have never been available. However, they are currently being evaluated in Component Engineering and will soon be available as 8641-2 tranceivers (Digital part number 19-14987-00) for future designs. These, or devices with equivalent specifications as described above, are the preferred bus interface. Subject to availability, cost, and the need to use LSI devices, the new transceiver should be used for all new Q-Bus designs.

6 CONFIGURATION OF BUS OPTIONS

The position of each option within the interrupt acknowledge and bus mastership grant daisy chains, with respect to the controlling and interrupt fielding processor, has influence on total system performance. Selection of interrupt request level also influences total system performance because of the priority schemes previously described.

In this context, system performance can be viewed as a waiting line problem. (i.e., How long will you have to wait in line at a McDonald's hamburger stand before getting service?)

System performance will depend more on some devices being able to get service than on others. These devices must be placed at a higher priority than those that can afford to wait longer to receive service.

How does the system designer decide where to place each device in his system? Most systems are lightly loaded, having only one or at most two DMA devices and two or three interrupting devices. In these systems, it is probably no concern at all, but in busy systems, it becomes an interesting and complex problem.

One approach the system designer may take is to tabulate the pertinent parameters as shown in Table 3.

Note, there are some mutually exclusive options in Table 3 that would not exist in a real system.

Note

The numbers in Table 3 are not necessarily correct and are provided only for illustration.

Finally he may assume that all feasible DMR's and IRQ's are up together and go through the exercise again, re-arranging and re-trying until no slack times are violated.

If CPU refresh is being used, the problem is somewhat more complicated. The designer may consider the CPU as a DMR that must be serviced between all others until 64 refreshes have occurred.

This technique is not foolproof. Many more sophisticated techniques of "Scheduling/Waiting Line/Queuing Theory" can be used as well as probably some much simpler techniques. This section is offered as a starting point in case it might help some system designers.

A good reference is Chapter 7 and the supplement in Production and Operations Management by Chase and Aquillano 1977 edition.

There are some other considerations to be taken into account when configuring options.

The LSI-11 processors use a 4-phase clock to run the microprocessor. External signals are generally clocked into the microprocessor on phase 3. If a device is just asserting or negating a signal (for example, RPLY) as phase 3 is about to occur, it may get caught if the device is close to the CPU and missed if the device is far away (further down the bus). If it is missed, it will get caught on the next phase 3, which means a delay of 383 ns (LSI-11 microcycle time) or perhaps many cycles depending on what is happening. For this reason LSI-11 systems tend to be configured as follows:

CPU Memory
fastest DMA
.
.
Slowest DMA
Fastest Level 7
.
.
Slowest Level 7
Fastest Level 6
.
.
Slowest Level 6
Fastest Level 5
.
.
Slowest Level 5
Fastest Level 4
.
.
Slowest Level 4
Fastest Program Transfer
.
Slowest Program Transfer

In F11 systems, the processor stops its clock while waiting for many events, and some signals are strobed in by a 65 microsecond clock so that the effect is much less evident but the principle (configure fastest to slowest) still has some merit.

Obviously, the importance of real time data from certain devices, how frequently certain devices need the bus, and what else can possibly be going on in an operating system when a device needs service will have some impact on system design. After all these considerations, one must then check totals of ac and dc loading, distribution of loads, and power drain.

From the above considerations, it can be seen that system design for maximum performance is no easy task in large systems. Benchmarks can be used as a measure of success.

7 POWER DISTRIBUTION, REGULATION AND BACK-UP

Power is supplied to the Q-Bus backplanes from one or more power supplies, generally via cables and terminal strips. Power and power return must not be passed from backplane to backplane in or near the same cables as the LSI-11 Bus signals and their returns.

It is preferrable to have a separate power supply for each backplane, with power cables no longer than three feet. Signal return paths between backplanes will provide common low signal reference. Maximum composite signal return path resistance, near end to far end is 50 milliohms.

Each bus interface slot has connector pins assigned for the following dc voltages:

+5 V dc: Three pins, AA2, BA2, BU1; 1.5 A maximum per pin

+12 V dc: Two pins, AD2, BD2; 1.5 A maximum per pin

-12 V dc: Two pins, AB2, BB2; 1.5 A maximum per pin

GND: Eight pins, AC2, AJ1, AM1, AT1, BC2, BJ1, BM1, BT1; 1.5 A maximum per pin

+12 VB: Two pins, AS1, BS1; 1.5 A Maximum per pin
Battery Backup

+5 VB: One pin, two alternates, AV1, [AE1, AS1 alternates when not in Battery Backup use in the system as a special spare (AE1) or 12 B (AS1)]; 1.5 A maximum per pin.

Power is transmitted to each interface slot by etch or wire from the backplane terminal strip. Backplanes must be constructed with the minimum current carrying capabilities listed in Table 5.

Table 5. Backplane Current-Carrying Capacity Minimum Specifications

Voltage	Backplane Interface Slots		
	8	12	18
+5 V	18 A	27 A	30.5 A
+12 V	9 A	13.5 A	20.25 A
-12 V	4 A	6 A	9 A
GND	20 A	30 A	45 A
+5 B	12 A	18 A	27 A
+12 B	6 A	9 A	13.5 A

The power supply, cabling from the power supplies to the backplane terminals strips and wiring from the terminal strips to the interfaces slots must be of adequate quality to provide the following at no load, full load, high line and low line in DEC STD 103 (proposed) class C environment.

+5 V dc ± 5%: Maximum ripple 100 MV pp; maximum high frequency noise assuming adequate bypass on load modules 100 MV.

+12 V dc ± 3%: Maximum ripple 200 MV pp; maximum high frequency noise assuming adequate bypass on load modules 100 MV.

-12 V dc ± 3%: Maximum ripple 200 MV pp; maximum high frequency noise assuming adequate bypass on load modules 100 MV.

When power is failing and a battery back-up unit is switched in to keep critical circuits alive through the special battery backup (BB) pins provided, the back-up units must meet the same regulation specifications as the appropriate normal voltage. These specifications must apply throughout the transition normal-to-BB and BB-to-normal. In addition, when the transition occurs, no Q-bus signals or other interfaces should be affected (i.e. glitches or crosstalk created by transition).

8 INTERRUPT AND TRAP VECTORS (Cont'd)

Vector	Unibus	LSI-11 Bus
200	LP11/LS11, line printer: LA180	LAV11, LPV11
	LA180	
204	RS04/RF11, fixed head disk	
210	RC11, disk	
214	TC11, DECtape	
220	RK11, disk	RKV11
224	TU16/TM11/TS03, magnetic tape	
230	CD11-CM11-CR11, card reader	
234	UDC11, digital control sub-	
	system	
240	PIRQ, program interrupt	
	request (11/45)	
244	Floating-point error	FIS (optional)
250	Memory management	
254	RP04/RP11 disk pack	
260	TA11, cassette	
264	RX11, floppy disk	RXV11
- - -	- - - - - - - - - - - - - - - - - -	- - - - - - - - - - - - - - - - -
270	User reserved	
274	User reserved	User reserved
300	(Start of floating vectors)	
- - -	- - - - - - - - - - - - - - - - - -	- - - - - - - - - - - - - - - - -
374		
400		
404		ADV11-A
410		
414		
- - -	- - - - - - - - - - - - - - - - - -	- - - - - - - - - - - - - - - - -
420		
424		IBV11-A
430		
434		
- - -	- - - - - - - - - - - - - - - - - -	- - - - - - - - - - - - - - - - -
440		KWV11-A
444		
- - -	- - - - - - - - - - - - - - - - - -	- - - - - - - - - - - - - - - - -
450		
		User reserved
777	(End of floating vectors)	

9 DEVICE ADDRESS ASSIGNMENTS

Address	Unibus	LSI-11 Bus
777 776	Processor status word (PS)	
777 774	Stack limit	
777 772	Program interrupt request (PIRQ)	
777 770		
.	DEC reserved	
777 720		
777 716		
.	CPU registers	
777 710		
777 707	R7 (PC)	
777 706	R6 (SP)	
777 705	R5	
777 704	R4 General	
777 703	R3 Registers	
777 702	R2	
777 701	R1	
777 700	R0	
777 676		
.	Memory Management	
777 600		
777 576	(SR2)	
777 574	Memory management status reg (SR1)	
777 572	(SR0)	
777 570	Console switch and display register	
777 566	(XBUF)	
777 564	(XCSR) Console	Console
777 562	(RBUF) Terminal	Terminal
777 560	(RCSR)	
777 556		
777 554	PC11/PR11	
777 552		
777 550		

9 DEVICE ADDRESS ASSIGNMENTS (Cont'd)

Address	Unibus		LSI-11 Bus
777 546	KW11-L, DL11-W		(LTC) KPV11, BDV11
777 544			
.			
.	XY11		
.			
777 530			
777 526	Unassigned		
777 524			
777 522	Unassigned		BDV11
777 520			
777 516	LA180, LP11		
777 514	LS11, LV11		LAV11, LPV11
777 512			
777 510			
777 506			
.			
.	TA11		
.			
777 500			
777 476			
.			
.	RF11		
.			
777 460			
777 456			
.			
.	RC11		
.			
777 440			
777 436		#8	
777 434		#7	
777 432		#6	
777 430	DT11, bus switch	#5	
777 426		#4	
777 424		#3	
777 422		#2	

9 DEVICE ADDRESS ASSIGNMENTS (Cont'd)

Address	Unibus		LSI-11 Bus
775 626 775 624 775 622 775 620	#2		units with modem control capability.
775 616 775 614 775 612 775 610	#1		
775 608 775 604 775 602 775 600	DEC reserved		
775 576 . . 775 400	DS11	#4 #1	
775 376 . . . 775 200	DN11	#16 #1	
775 176 . . . 775 000	DM11	#16 #1	
774 776 . . . 774 410	DP11	#1	
774 406 774 404 774 402 774 400	DP11 RL01	#32	RLV11

9 DEVICE ADDRESS ASSIGNMENTS (Cont'd)

Address	Unibus	LSI-11 Bus
774 376	#32	
.		
.	DC11	
.		
774 000	#1	
773 376		
.		
.	Maintenance loader	
.		
773 700		
773 676	↓ M792 diode ROM ↓	
.		
.		
.		
773 400		
773 376		
.		
.	BM792-YH cassette	
.		
773 300	↑ M792 diode ROM ↑	
773 276	↓ MR11-DB ↓	
.		
.	BM792-YC card	
.		REV11, BDV11
773 200		MRV11-AA
773 176		256-word ROM
.		space
.	BM792-YB disk/DECtape	
.		
773 100	↑ MR11-DB ↑	
773 076		
.		
.	BM792-YA paper tape	
.		
773 000		

9 DEVICE ADDRESS ASSIGNMENTS (Cont'd)

Address	Unibus	LSI-11 Bus
772 776 . . . 772 700	PA611 typeset punch	
772 676 . . . 772 600	PA611 typeset reader	
772 576 772 574 772 572 772 570	AFC11	
772 566 . . . 772 560	DEC reserved	
772 556 . . . 772 550	DEC reserved	
772 546 772 544 772 542 772 540	KW11-P	
772 536 772 534 772 532 772 530 772 526 772 524 772 522 772 520	TM11	
772 516	Memory mgt status reg (SR3)	

9 DEVICE ADDRESS ASSIGNMENTS (Cont'd)

Address	Unibus	LSI-11 Bus
770 416 . . .	AR11, LPS11	
770 404 770 402 770 400		ADV11-A
770 376 . . . 770 000	DEC reserved	
	↓ User Reserved Area ↓	
767 776 767 774 767 772 767 770	DR11-C'#1	DRV11'#1
767 766 767 764 767 762 767 760	DR11-C'#2	DRV11'#2
767 756 767 754 767 752 767 750	DR11-C'#3	DRV11'#3
767 746 . . . 766 000		
765 776 . . . 765 000		REV11 256 word ROM space

9 DEVICE ADDRESS ASSIGNMENTS (Cont'd)

Address	Unibus	LSI-11 Bus
764 776		
.		
.		
.		
764 000		
	↑ User Reserved Area ↑ Start here and assign upwards to 767 776	
- - - -	- -	- - - - - - - -
- - - -	- -	- - - - - - - -
763 776	(top of floating addresses)	
.		
.		
.		
760 154		
760 152	Floating	IBV11-A
760 150	Addresses	Floating
760 146		Addresses
.		
.		
.		
760 010	Start here and assign upwards to 763 776	
- - - -	- -	- - - - - - - -
- - - -	- -	- - - - - - - -
760 006		
.		
.	DEC Reserved	DEC Reserved
.		
760 000		