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The Memory Daughter-Card Version 1.5 User's Manual

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Abstract

The *memory daughter-card* is memory extension board for the *Itsy pocket computer* developed at Compaq Computer Corporation's *Western Research Laboratory (WRL)*. It provides an additional bank of flash memory and up to three additional banks of DRAM. It is possible to boot from this daughter-card. This document describes the architecture and the low-level programming model of the memory daughter-card.

Revision 1.0

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Disclaimer

1 Introduction

This document describes the architecture and the programmer's model of the *memory daughter-card* for the *Itsy pocket computer* [Vir98]. It should be considered as a guide for low-level software developers.

A good understanding of the Itsy computer [Vir98] is assumed throughout this report.

1.1 Purpose

The design of the memory daughter-card was aimed at achieving several goals:

- Provide additional flash memory and DRAM (memory extension).
- Be usable as a "safety daughter-card," i.e., it should be possible to boot from the daughter-card, in order to recover from a corrupted mother-board flash memory.
- Be usable as a system test and debug platform, i.e., it should be possible to boot from the daughter-card and use sockets for the flash memory, so that it can be programmed with an external programmer.
- Provide a prototyping platform to interface additional hardware to the Itsy computer.

1.2 History

The first *printed-circuit board (PCB)*, referred to as *memory daughter-card version 1.0*, was completed in November 1997. This first prototype had a few minor flaws, all of which could be corrected. The logic design corresponding to a modified (i.e., patched) version 1.0 board is known as *memory daughter-card version 1.1*. This design corresponds only to a set of schematics, no physical PCB having been manufactured.

A second prototype, named *memory daughter-card version 1.5* was complete in July 1998. It corresponds to a version 1.1 system with a few additional features. From the programmer's point-of-view, there are almost no differences between the versions 1.1 and 1.5.

This document describes the memory daughter-card version 1.5. All relevant differences between the versions 1.1 and 1.5 are outlined in foot-notes.

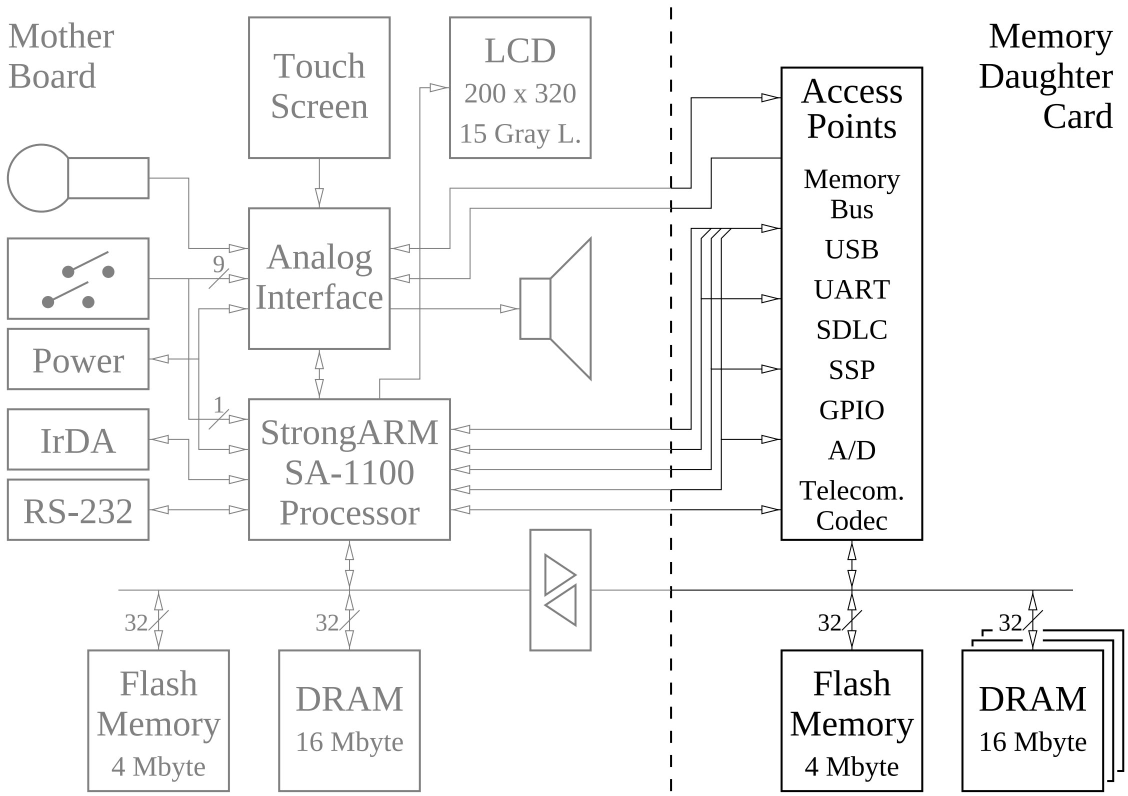

Figure 1: Architecture of the memory daughter-card.

1.3 Notations

In this report, electrical signals are represented as upper-case names in a sans-serif font (e.g., PWR_EN). Active-low signals are denoted by over-lines (e.g., $\overline{\mathsf{RESET\_OUT}}$), while buses and element of buses are specified by subscripts (e.g., $\mathsf{DCD}_{31..0}$, DCA_0). In the schematics, the same signals are represented using the syntax and conventions of the WindowSIL [Tha97] CAD tools. For example, the signal $\overline{\mathsf{DCCS}}_2$ appears as `~dccs[2]`.

2 Architecture

Figure 1 presents the architecture of the memory daughter-card (right part), shown in respect to the Itsy computer (left part). The memory daughter-card versions 1.1 and 1.5 are both compatible with both versions of the Itsy mother-board (i.e., versions 1.1 and 1.5).

2.1 Memory system

The memory daughter-card features a *flash memory* decoded as static-memory bank 2 and the three *dynamic random-access memory (DRAM)* banks 1, 2, and 3. Depending on the application's needs, only some of these banks (or even none) might be present. Since this daughter-card is bootable, the flash memory is also decoded as static-memory bank 0, from which the StrongARM SA-1100 processor [DEC98] boots.

2.1.1 Flash memory

A pair of 16-bit flash-memory circuits implement the 32-bit flash memory. These circuits can be either soldered on the board or put in *zero insertion force (ZIF) sockets*. Many different devices can be accommodated:

AMD Am29LV160B$OssPT$ [AMD97e]
AMD Am29LV800O-$ssPT$/Am29LV800B$OssPT$ [AMD97c, AMD97d]
AMD Am29LV400O-$ssPT$ [AMD97a]
AMD Am29LV200O-$ssPT$ [AMD97b]
Hitachi HN29VO800P-ss/HN29WO800P-ss [Hit97c, Hit97d]
Motorola M29F800A2$OPss$/M29F800A3$OPss$ [Mot97]
Sharp LH28F800SGP-Lss [Sha97]

where "O" specifies the internal sector organization, "ss" specifies the speed, "P" specifies the package, and "T" specifies the temperature range. Any other compatible parts can also be used.

Following the Itsy static-memory identification scheme [Vir98], a non-volatile memory identification structure describes the characteristics of the specific parts used on a given daughter-card and hence allows the software to configure the memory interface correctly.

The *reset/power-down pin* of the flash-memory circuits is asserted (0) during a reset (i.e., hardware, software, or watch-dog reset) and during sleep mode. When the flash memory does not need to be accessed, this signal can also be asserted (0) by setting the signal GPIO_{16} ($\overline{\mathsf{DCFLFOFF}}$) to 0 (see Section 3.1).[1] When the Itsy computer must boot from the daughter-card, this signal should never be set to 0 during sleep mode, since the processor would be unable to read the boot memory upon wake up. This can easily be achieved by setting bit 16 of the *power manager GPIO sleep state register* PGSR of the StrongARM SA-1100 processor [DEC98] to 1.

The *ready/not-busy pins* of the flash-memory circuits can be monitored using the signals GPIO_{17} ($\mathsf{DCFL0RY}/\overline{\mathsf{BY}}$), for the least significant 16 data bits $\mathsf{D}_{15..0}$, and GPIO_{18} ($\mathsf{DCFL1RY}/\overline{\mathsf{BY}}$), for the most significant 16 data bits $\mathsf{D}_{31..16}$ (see Section 3.1).

The hardware write-protection mechanism, featured by some of the supported parts, is never used, and the corresponding pin is always de-asserted (1). However, it is still possible to protect the flash memory against write accesses, by using the jumper provided for this purpose. The flash memory is protected when this jumper is open and is writable when this jumper is short-circuited.

2.1.2 Dynamic RAM

Three pairs of 64 Mbit (i.e., 2^{12} rows $\times$ 2^{10} columns $\times$ 16 bits) self-refresh DRAM circuits implement the three 32-bit DRAM banks. Many different *fast-page mode* or *enhanced data out (EDO)* devices can be accommodated:

[1] On the memory daughter-card version 1.1, the reset/power-down pins are only asserted (0) during sleep mode or when the signal GPIO_{16} ($\overline{\mathsf{DCFLFOFF}}$) is set to 0.

Signal	Name	Function	Dir.	Def.
GPIO_{16}	$\overline{\mathsf{DCFLFOFF}}$	**D**aughter-**c**ard **fl**ash memory **f**orce **off**	O	1
GPIO_{17}	$\mathsf{DCFL0RY}/\overline{\mathsf{BY}}$	**D**aughter-**c**ard **fl**ash memory **0** **r**ead**y**/**b**us**y**	I	
GPIO_{18}	$\mathsf{DCFL1RY}/\overline{\mathsf{BY}}$	**D**aughter-**c**ard **fl**ash memory **1** **r**ead**y**/**b**us**y**	I	

Table 1: Memory daughter-card general-purpose input/output signals.

Hitachi HM5165160ALTT-*ss* [Hit97a]
Hitachi HM5165165ALTT-*ss* [Hit97b]
Samsung KM416V4100AS-L*ss*/KM416V4100BS-L*ss* [Sam97a, Sam98a]
Samsung KM416V4104AS-L*ss*/KM416V4104BS-L*ss* [Sam97b, Sam98b]
Toshiba TC5165165AFTS-*ss* [Tos96]

where "*ss*" specifies the speed. Any other compatible parts can also be used.

Since all DRAM banks must be accessed at the speed of the slowest one, it is best to use the same devices as on the Itsy mother-board, that is, 50 ns EDO DRAM circuits (KM416V4104AS-L5, KM416V4104BS-L5, or TC5165165AFTS-50).

3 Programmer's model

This section presents additional information on the model that the low-level software has of the memory daughter-card hardware.

3.1 Memory daughter-card general-purpose input/output signals

Table 1 shows the general-purpose input/output signals used on the memory daughter-card. Both input signals can be used as interrupts. After a hardware reset (i.e., power-up or push-button reset), all input/output signals are configured as input. Therefore, a pull-up resistor is used to provide a default value to the signal GPIO_{16} ($\overline{\mathsf{DCFLFOFF}}$), as shown in the last column of Table 1. The function of all signals are:

GPIO_{16}**:** $\overline{\mathsf{DCFLFOFF}}$**: D**aughter-**c**ard **fl**ash memory **f**orce **off**

This output signal is used to control the reset/power-down pin of the flash-memory circuits (see Section 2.1.1). When this signal is set to 0, the reset/power-down pins are asserted (0). When it is set to 1, the reset/power-down pins are only asserted (0) during a reset (i.e., hardware, software, or watch-dog reset) and during sleep mode.[2] A pull-up resistor sets the default value of this signal to 1 when the GPIO_{16} pin is configured as input (e.g., after a hardware reset). When the Itsy computer must boot from the daughter-card, this signal should never be set to 0 during sleep mode, since the processor would be unable to read the boot memory upon wake up. This can be easily achieved by setting bit 16 of the *power manager GPIO sleep state register* PGSR of the StrongARM SA-1100 processor [DEC98] to 1.

[2] On the memory daughter-card version 1.1, the reset/power-down pins are only asserted (0) when this signal is set to 0 and during sleep mode.

GPIO_{17}: $\mathsf{DCFL0RY}/\overline{\mathsf{BY}}$: **D**aughter-**c**ard **fl**ash memory **0** **r**ead**y**/**b**us**y**

This input signal is connected to the ready/not-busy pin of the flash-memory circuit used for the least significant 16 data bits $\mathsf{D}_{15..0}$ (see Section 2.1.1). It is set to 0 when the flash-memory circuit is executing an erase or program operation and to 1 when it is ready for use.

GPIO_{18}: $\mathsf{DCFL1RY}/\overline{\mathsf{BY}}$: **D**aughter-**c**ard **fl**ash memory **1** **r**ead**y**/**b**us**y**

This input signal is connected to the ready/not-busy pin of the flash-memory circuit used for the most significant 16 data bits $\mathsf{D}_{31..16}$ (see Section 2.1.1). It is set to 0 when the flash-memory circuit is executing an erase or program operation and to 1 when it is ready for use.

3.2 Non-volatile memory identification structure

Following the Itsy *static-memory identification scheme*, the flash memory must implement a *non-volatile memory identification structure* [Vir98]. The *class identification* value is $\mathsf{CID} = 0$, the read-only bit is $\mathsf{R} = 0$, the daughter-card bit is $\mathsf{D} = 1$, and the width bit is $\mathsf{W} = 0$. The values of the SIZE field and of the different MSC fields depend on the specific parts used on a given daughter-card (see Section 2.1.1). The fields EN0, $\mathsf{RY}/\overline{\mathsf{BY}}\mathsf{0}$, EN1, and $\mathsf{RY}/\overline{\mathsf{BY}}\mathsf{1}$, defining the general-purpose input/output signals, have the values $\mathsf{EN0} = 16 = 10_{16}$, $\mathsf{RY}/\overline{\mathsf{BY}}\mathsf{0} = 17 = 11_{16}$, $\mathsf{EN1} = 16 = 10_{16}$, and $\mathsf{RY}/\overline{\mathsf{BY}}\mathsf{1} = 18 = 12_{16}$.

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