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DQS11-A/B
PDP-11 COMMUNICATIONS CONTROLLER

OPTION DESCRIPTION
CSS-MO-F-3.2-03

digital

Computer Special Systems

NOTEBOOK SECTION

3.2-03

OPTION NUMBER

-

DRAWING SET NUMBER

DQS11-A
DQS11-B

PROGRAM NUMBER

DECSPEC-11-ARIAD
DECSPEC-11-ARIBD
DECSPEC-11-ATKAD
DECSPEC-11-ATKBD

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DQS11-A/B
PDP-11 COMMUNICATIONS CONTROLLER

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CSS-MO-F-3.2-03

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Computer Special Systems

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CONTENTS

CONTENTS (Cont)

CONTENTS (Cont)

ILLUSTRATIONS

CONTENTS (Cont)

Computer
Special
Systems

digital

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Section 3.2-3B

DQS11-A/B

BI-SYNC CONTROLLERS FOR PDP-11

1.1 GENERAL DESCRIPTION

DQS11-A/B are half-duplex synchronous communications controllers for the PDP-11 Family, capable of operating as speeds to 230.4K baud depending on the characteristics of the modem employed. Data transfers occur directly to memory by means of the PDP-11 NPR facility.

The DQS11-A/B follows the IBM Binary Synchronous Communication (BSC) line-control procedures for the transmission of data. The two available options provide automatic recognition of standard ASCII (DQS11-A) or EBCDIC (DQS11-B) control characters. Additional features include automatic sync acquisition, automatic control of DLE sequences for "transparent" operation, and automatic generation and checking of a two character (16-bit) cyclic redundancy check message. The DQS11-A also performs odd parity generation and checking for "non-transparent" text.
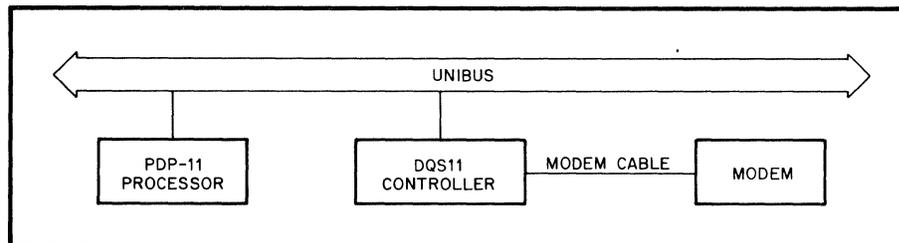
CS-0643

Figure 1-1 System Block Diagram

1.2 OPERATION

The DQS11-A/B is initialized (Power ON or System RESET) to the Transmit Idle state. No transmission occurs until the software has prepared a message, loaded the Bus Address and Byte Count registers and issued a GO command to the device. The DQS11-A/B precedes the message with four SYN (ASCII or EBCDIC Synchronous Idle) characters and appends two CRC characters if the message ends with ETX or ETB. One pad character (377_8) is sent at the end of transmission. During transparent mode transmission, the DQS11-A/B generates an additional DLE character for each DLE character encountered in the data string. The Control DLE in the terminating sequence (DLE ETX or DLE ETB) is not padded. Upon completion of transmission, the device sets its RDY bit and, if Interrupt Enable is set, generates an interrupt request to the program interrupt facility.

When "primed" by the operating program to receive a message , i.e., set to the Receive mode, the DQS11-A/B monitors the receive data for two consecutive SYN characters. Once synchronization has been achieved, the first non-SYN character is handled as data. If a GO Command has been received, specifying that a buffer area has been reserved for data storage, memory transfers commence. Normal mode SYN characters, Transparent mode DLE SYN sequences, and the first DLE of DLE DLE sequences are not transferred to memory. At the end of the message, the two character CRC word is checked (when present), and the device's RDY bit is set. The DQS11-A/B remains in Receive mode, searching for Synchronous Idle, until software places it in Transmit mode.

1.3 CONFIGURATIONS

The DQS11-A/B is available in four configurations. Model numbers and configurations are:

DQS11-AA	ASCII characters, EIA interface levels
DQS11-AB	ASCII characters, Current Mode
DQS11-BA	EBCDIC characters, EIA interface levels
DQS11-BB	EBCDIC characters, Current Mode.

1.4 SPECIFICATIONS*

a. Mechanical:

Logic Panels	One, Type H933-C (System Unit)
Dimensions	19 in. w, 10-1/2 in. h, 2-1/2 in. d
Weight	10 lb (approx.)
Interconnections	Supplied
Unibus	BC11A or M920 (as required)
Modem Cable	BC01R25 (25 feet) for EIA drive.
	BC01W25 (25 feet) for current drive
Mounting Prerequisite	Space in BA11 mounting box

b. Electrical:

Prerequisite Power Source	H720 mounted in BA11 box
Input Voltages	+5 Vdc, +8 Vdc, –15 Vdc
Logic	TTL
Module Type	M-Series

c. Operational:

Transfer Mode	DMA via Non-Processor Request (NPR)
Data Transfer	Block, Half-duplex, Bi-directional
Control Characters	ASCII (DQS11-A)
	EBCDIC (DQS11-B)
Modem Signal Drive	EIA (standard)
	Current (optional)
Operating Speed	Standard: 2000 baud
	Optional: any speed up to 230.4K baud

1.5 AVAILABILITY

The DQS11-A/B are products of Digital's Computer Special Systems group and are available, with new installations or for add-on to existing compatible systems, from facilities in:

Digital Equipment Corporation
Main Street
Maynard, Massachusetts 01754 U.S.A.
Telephone: (617) -897-5111

Digital Equipment Corporation
310 Soquel Way,
Sunnyvale, California 94086 U.S.A
Telephone: (408) -735-9200

Digital Equipment Corporation
2110 South Anne Street
Santa Ana, California 92704 U.S.A.
Telephone: (714) -979-2460

Digital Equipment Corporation International
Kowa Building No. 25 (3rd Floor)
8-7, Sanban-cho,
Chiyoda-ku, Tokyo 102, JAPAN
Telephone: 264-7101

Digital Equipment Corporation Ltd.
4 Arkwright Road
Reading, Berkshire, England
Telephone: 0734-583555

Digital Equipment GmbH
8 Muenchen 13
Wallensteinplatz 2 West Germany
Telephone: 0811-35031

Digital Equipment France
18 rue Saarinen
Zone Silic
94533 Rungis, France
Telephone: 687-2333

Digital Equipment AB
Stockholm
Englundavagen 7, 171 41 Solna, Sweden
Telephone: 98 13 90

Digital Equipment Australia Pty., Ltd.
75 Alexander Street
Crows Nest
N.S.W., Australia 2065
Telephone: 439-2566

Digital Equipment of Canada, Ltd.
100 Herzberg Drive
Kanata, Ontario, Canada
Telephone: (613) -592-5111

Main offices are at 146 Main Street, Maynard, Massachusetts, 01754.

d i g i t a l

SECTION 2
INSTALLATION

Each DQS11 occupies one PDP-11 system unit which is usually housed in a BA11 Mounting Box as shown in Figure 2-1 but can be mounted in a vertical rack when required.

BB11 SYSTEM UNIT

BA11 MOUNTING BOX
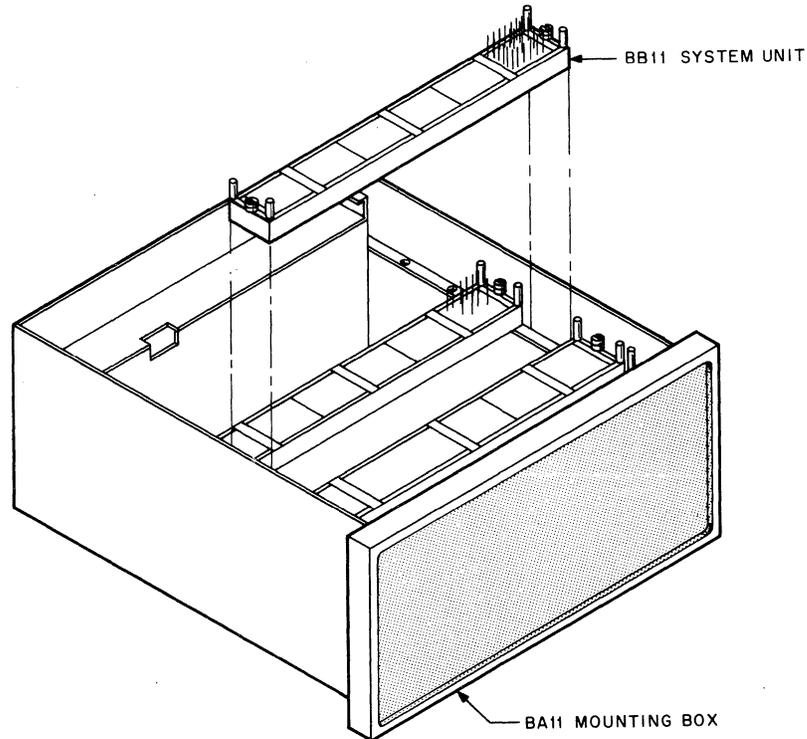
CS-0664

Figure 2-1   System Unit Mounting

2.1   SITE CONSIDERATIONS

Environmental requirements for this device are identical to those specified for the PDP-11 computer system in the PDP-11 maintenance literature.

2.2   CABLES

The DQS11 requires Unibus and Modem Control Cables. Figure 2-2 shows the cable slot assignments. These cables assemblies are described in the following paragraphs.

UNIBUS OUT   MODEM CABLE
                         MODEM CONTROL

AO4	BO4	CO4	DO4		
AO3					
AO1	BO1				

POWER IN
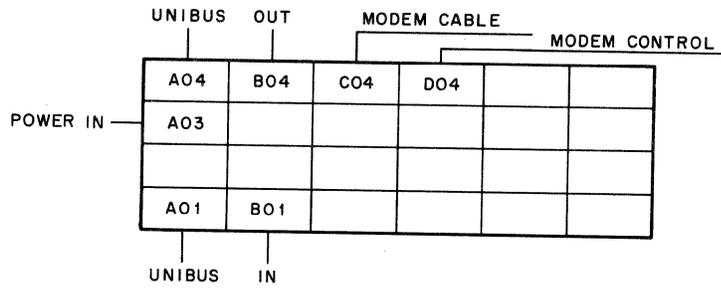
UNIBUS IN

CS-0654

Figure 2-2   Cable Slot Assignments

2.2.1   PDP-11 Unibus

All communications with the PDP-11 system take place over the Unibus. BC11A Unibus cables or M920 Unibus Jumper Modules are supplied as required. The input slots for the Unibus are A01 and B01. The output slots, A04 and B04, connect to another system device or, if the DQS11 is the last unit on the bus, they accept the M930 Bus Terminator Module.

2.2.2   Modem Control

Data and modem control signals are carried on either a BC01R or a BC01W cable, depending on the modem employed. The BC01R cable is used with the M594 EIA Voltage Converter. The BC01W cable is used with the M595 Current Mode Converter. The BC01R has a DEC "paddle board" connected at the DQS11 end and an RS232 compatible connector at the modem end. The BC01W has a DEC "paddle board" connector at one end and a Burndy MD 12MXP-17TC connector at the other. Both cables connect to DQS11 slot C04. The following are names with respective pin locations.

Signal Names	Modem Connector Pin
BA TRANSMIT DATA	E2
BB RECEIVE DATA	F2
CA REQUEST TO SEND	L2
CB CLEAR TO SEND	K2
CC DATA SET RDY	N2
CD TERM RDY	R2
CF CARRIER	P2
DB TRANSMIT CLOCK	H2
DD RECEIVE CLOCK	J2

2-2

2.3 INITIAL OPERATION

The following Checkout and Acceptance procedures are performed in-house prior to shipment of the DQS11. These, if performed again at the time of installation, serve an initial turn-on procedure which validates proper operation.

2.3.1 Checkout And Acceptance Procedure

Perform the Checkout And Acceptance Procedure in the following sequence:

a.   Remove the converter module from slot D04 of the device system unit. Run either DECSPEC-11-ARIAD or DECSPEC-11-ATKAD (the DQs11-A and DQs11-B diagnostic programs discussed in Appendix A). The diagnostic exercises and checks the entire device except for the nine logic paths leading to and from the modem. If no failure is detected, the DQS11 satisfies this portion of the Checkout and Acceptance Procedure.

b.   Run either DECSPEC-11-ARIBD or DECSPEC-11-ATKBD (the DQS11-A and DQS11-B Modem Exerciser Programs discussed in Appendix B). These programs require that two similar DQS11 devices be located on a common Unibus and that the two devices be attached to two modems through which communications can take place. If no failure is detected, the DQS11 satisfies this portion of the Checkout and Acceptance Procedure.

NOTE

Omit Section b. if the required equipment is not available.

2.4 RELATED DOCUMENTS

The following DEC publications contain material which supplements the information in this option description:

PDP-11 Processor Handbook
PDP-11 Peripheral Handbook
Logic Handbook

SECTION 3
OPERATION AND PROGRAMMING

This device provides the means by which bidirectional block data transfers occur between the PDP-11 core memory and certain half-duplex synchronous communication equipments (modems).

All data transfers occur directly with the PDP-11 core memory utilizing the PDP-11 Non-Processor Request (NPR) facility. Non-data transfers for establishing and examining control conditions occur over the PDP-11 Unibus under program control.

3.1 DQS11 REGISTERS

Four registers employed by the DQS11 reside on the PDP-11 Unibus. The absolute bus addresses of these registers are determined by jumpers on the M105 Device Selector Module. Within any DQS11 the relative register addresses are fixed and only the address of the Controller Status Register need be specified.

3.1.1 Controller Status Register 16XXX0

The Controller Status Register (CSR) provides the means by which the PDP-11 commands and monitors the DQS11. The CSR is organized as shown in Figure 3-1.
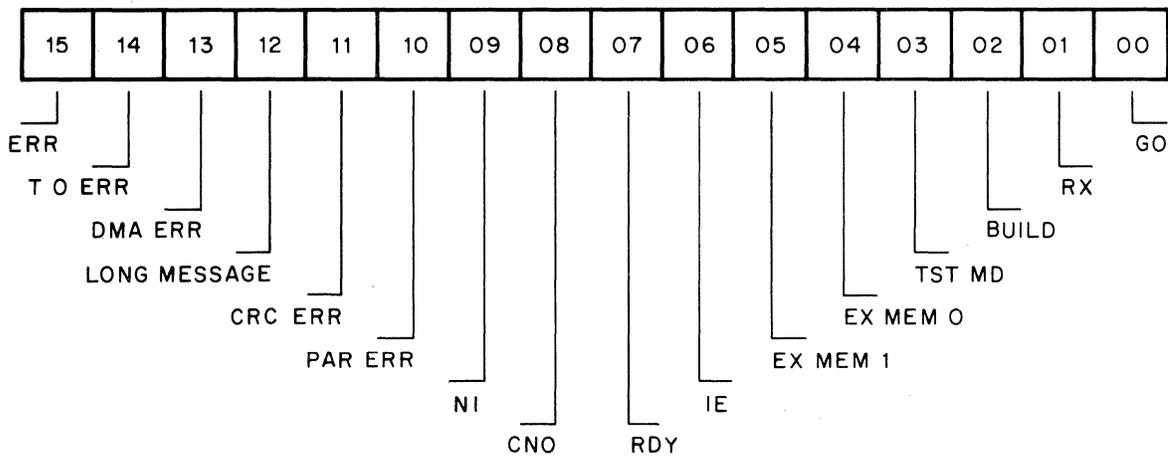
CS-0409

Figure 3-1 Controller Status Register Word Format

3-1

The following lists each CSR bit and the significance of each when set.

Bit	Mnemonic	Function
00	GO	This write-only bit (always read as zero) in Transmit Mode causes the DQS11 to transmit the message specified by the Bus Address and Word Count Registers. In the Receive Mode, the DQS11 is notified that an input buffer has been established for the received message.
01	RX	RECEIVE. This read-write bit places the DQS11 in the Receive mode. This bit is cleared by system RESET.
02	BUILD	This read-write bit alters the significance of Byte Count Overflow. When this bit is clear, Byte Count Overflow signals end of message when transmitting and data buffer overflow when receiving. When this bit is set, Byte Count Overflow asserts the RDY bit, notifying the software that a new data buffer must be assigned. This feature conserves core memory by allowing the software to process a message in segments. While the software handles one data buffer, the DQS11 transfers data to or from another data buffer. This bit is cleared by system RESET.
03	TST MD	TEST MODE: This read-write bit is set for maintenance purposes only. Bits 08 and 09 become the read-write bits; TEST CLOCK, and TEST DATA respectively. This bit is cleared by system RESET.
04 05	EX MEM 0 EX MEM 1	These read-write bits specify the 32K memory field which is to be the target of NPR data transfers should the PDP-11 system contain more than 28K of core memory. These bits are cleared by system RESET.
06	IE	INTERRUPT ENABLE: This read-write bit causes the DQS11 to interrupt the PDP-11 whenever the Ready bit is set. Interrupts are inhibited when the IE bit is cleared. This bit is cleared by system RESET.

Bit	Mnemonic	Function

07   RDY

READY. This read-only bit is set whenever the DQS11 is available to receive a transfer to the CSR with the GO bit set. This GO Command clears the RDY bit. RDY is set at the completion of the transmit or receive operation or by Time Out Error. RDY is set by a transfer to the CSR with the GO bit clear. System RESET also sets RDY.

08   CNO

CARRIER NOT ON: During normal operation, this read-only bit reflects the Data Carrier Detector (Connection CF) signal from the Modem. A true condition indicates that the data carrier is lost, either because the transmitting signal converter is turned OFF or because of a fault condition.

When bit-3 (TEST MODE) is SET, bit-8 becomes the read/write bit TEST CLOCK used by maintenance software to simulate transmit or receive clock pulses.

09   NI

NO INTERLOCK: During normal operation, this read-only bit reflects the Data Set Ready (Connection CC) signal from the Modem. When this bit is true, the modem is not in the data mode.

When bit-3 (TEST MODE) is SET, bit-9 becomes the TEST DATA bit. If bit-1 (RX) is also set, TEST DATA is a read/write bit which simulates the serial receive data. If bit-1 is clear, TEST DATA is a read-only bit which reflects the serial transmitted data.

10   PAR ERR

PARITY ERROR: This read-only bit is set whenever the DQS11-A is not in transparent mode and an ASCII character is received consisting of an even number of ones (even parity). This bit is cleared by system RESET and by any GO Command which initiates a new operation. This bit is not cleared by a GO Command that continues a build mode operation. The DQS11-B does not check vertical parity and never causes this bit to be set.

Bit	Mnemonic	Function
11	CRC ERR	Cyclic Redundancy Check Error. This read only bit is set when the DQS11 receives a character CRC message which does not equal the CRC message generated by the receiver. This bit is cleared by system RESET and by any GO Command which initiates a new operation. This bit is not cleared by a GO Command that continues a build mode operation.
12	LM	LONG MESSAGE: This read-only bit specifies that the message is longer than the available memory buffer area. When transmitting, the final character (as indicated by CSR Bit-2 clear and Byte Count Overflow set) must be a terminator character. If it is not, the Interface transmits the ENQ Character to specify faulty transmission. When receiving, Byte Count Overflow inhibits the transfer of data to memory. Bit-12 sets when a data word is lost. The RDY bit is not set until the end of the message and the entire message is checked for parity errors. When receiving in Build Mode (CSR bit-2 set), Byte Count Overflow must be cleared by a GO Command before data is lost. Otherwise Bit-12 is set. This bit is cleared by system RESET, and any GO Command which initiates a new operation. This bit is not cleared by a GO Command which continues a build mode operation.
13	DMA ERR	DMA ERROR: This read only bit specifies that the transfer of data between the interface and the computer is failing to keep up with the communications channel. When receiving, a GO Command must be received from the computer before the detection of the first non-SYN character following synchronization. Also, the DMA transfer of each two character word must occur within the

Bit	Mnemonic	Function
13	DMA ERR (Cont)	transmission time of one character. When transmitting, the interface responds to a DMA Error by terminating transmission with an ENQ character. This bit is cleared by system RESET, and by any GO Command which initiates a new operation. This bit is not cleared by a GO Command that continues a build mode operation.
14	TO ERR	TIME OUT ERROR: This bit sets between 5.0 and 6.0 seconds after the beginning of transmission or, when in Receive mode, after synchronization. In Transmit mode, the Time Out Clock begins with the initial GO Command. In Receive mode, the Time Out Clock begins when the first two consecutive SYN characters are received. In both cases, the Time Out Clock is stopped if the message ends before the time out period. This error, which should only occur in the event of a hardware failure, sets the RDY bit. Bit-14 is cleared by system RESET and any GO Command.
15	ERR	ERROR: This read-only bit is the "OR" condition of PAR ERR, CRC ERR, LONG MESSAGE, DMA ERR, and TO ERR.

3.1.2 Byte Count Register 16XXX2

The Byte Count Register is a 16-bit read-write register which specifies the maximum (or total) number of bytes to be transferred to or from memory. When transmitting, the program loads this register with the 2's complement of the exact number of bytes to be transferred to the DQS11. Although each transfer contains two bytes, the interface handles byte count incrementation in a manner which allows an odd number to be specified. When receiving, this register specifies the number of memory bytes available for character storage. Because each transfer contains two bytes, this number must be even.

3.1.3 Bus Address Register 16XXX4

The Bus Address Register is a 16-bit read-write register which specifies the Bus Address which is the target of the next NPR transfer. Since data is transferred on a word basis, this register must contain a word address. The contents of the Bus Address Register are increased by two with each NPR transfer.

3.1.4 Data Buffer Register 16XXX6

The 16-bit Data Buffer Register may be written into and read from for maintenance purposes.

<div align="center">

NOTE

</div>

> During message handling, this register forms part of the
> data path to memory. Any attempt to write into the
> Buffer Register during message handling will cause loss
> of data.

3.2 MESSAGE FORMATS

The DQS11 is capable of sending or receiving 8-bit bytes of data in either character or transparent mode. In character mode, each byte represents a seven bit ASCII (DQS11-A) or an eight bit EBCDIC (DQS11-B) character. The DQS11-A generates and detects odd parity. In transparent mode, 8-bit bytes are sent as retrieved from memory. Lateral parity is neither generated nor detected. Text Control characters for both modes conform to Binary Synchronous Communications (BSC) conventions.* As described in this section, most control characters must be supplied as part of the message block stored in computer memory for transmission. The leading SYN characters and the DLE characters used to pad the appearance of DLE in transparent text are the two main exceptions. These are generated by the transmitting interface and stripped (not transferred to memory) by the receiving interface. The interface also generates and detects a two byte Cyclic Redundancy Check (CRC) word following each properly delimitted block of data.

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*Conventions of Digital Data Communications Link Designed by J.L. Eisenbies, IBM Systems Journal Vol. 6 No. 4 1967.

3.2.1 Character Mode

The DQS11 detects and responds to ten Control characters which compose five groups. SYN establishes character synchronization. SOH and STX indicate the beginning of data blocks and initiate CRC generation and detection. ETX and ETB terminate data blocks and are followed by the two byte CRC word. EOT, ENQ, ACK, and NAK abruptly terminate transmission and are not followed by a CRC word. DLE is used primarily for transparent mode control.

The DQS11 also detects a group of "Stick" characters which, when preceeded by DLE, abruptly terminate transmission. This feature allows the DQS11 to handle the two character affirmative acknowledge sequences.

Table 3-1 lists the ASCII and EBCDIC characters which are decoded by the DQS11-A and DQS11-B respectively. Bits represented by "X" may be either a "0" or a "1".

Table 3-1
Characters Decoded by DQS11-A and DQS11-B

Character	DQS11-A ASCII P, 7-1		DQS11-B EBCDIC 0-8	
	Octal	Binary	Octal	Binary
SYN	026	X0010110	062	00110010
SOH	001	X0000001	001	00000001
STX	002	X0000010	002	00000010
ETX	003	X0000011	003	00000011
ETB	027	X0010111	046	00100110
EOT	004	X0000100	067	00110111
ENQ	005	X0000101	055	00101101
ACK	006	X0000110	056	00101110
NAK	025	X0010101	075	00111101
DLE	020	00010000	020	00010000
Stick	–	XX1XXXXX	–	01XXXXXX
Stick	–	–	–	10XXXXXX
Stick	–	–	–	11XXXXXX

3.2.1.1 SYN - Synchronous Idle - The interface preceeds each transmission with four SYN characters. When receiving, the interface synchronizes on the first pair of consecutive SYN characters and treats the next non-SYN character as data. SYN control characters are not sent to computer memory.

3.2.1.2 SOH - Start of Heading - SOH preceeds a block of characters (the heading) which contains address or routing information. Whether transmitting or receiving, the interface begins CRC accumulation with the character following SOH. The appearance of STX indicates the end of the "heading", but the CRC accumulation is not terminated until the detection of either ETX or ETB.

3.2.1.3 STX - Start of Text - STX preceeds a block of characters (text) which is transmitted as an entity. If an SOH character has been detected, the interface includes STX in the CRC accumulations. Otherwise, CRC accumulation begins with the character following STX. The text and CRC accumulation are both terminated by either ETX or ETB.

3.2.1.4 ETX - End of Text - ETX terminates a block of characters started with SOH or STX and transmitted as an entity. When transmitting, the interface sends the two CRC bytes immediately following ETX. When receiving, the interface shifts ETX and the two following bytes into the CRC accumulator and sets an ERROR Flag if the result is not zero.

3.2.1.5 ETB - End of Transmission Block - ETB terminates a block of characters started with SOH or STX, where block structure is not necessarily related to processing format. The interface treats ETX and ETB identically.

3.2.1.6 EOT - End of Transmission - EOT indicates conclusion of a transmission (including text and associated headings) of one or more messages. When transmitting, the interface recognizes EOT as a legitimate message terminator. When an interface in Receive Mode detects EOT, it transfers the character to memory and then sets the RDY bit (CSR bit-07). EOT will usually be sent as a single character.

3.2.1.7 ENQ - Enquiry - As a single character, ENQ requests a response indicating identification, station status, repeat, or reply. When ENQ terminates a message string, it specifies that the message was in error and should be ignored. When transmitting, if the last character does not correctly terminate the message, the interface sets Long Message Error and terminates transmission by generating an ENQ character. In Receive Mode, the interface treats ENQ as EOT.

3.2.1.8 <u>ACK – Acknowledge</u> – ACK specifies that the previous block in the transmission was received without error and that the receiver is ready for the next block. The interface responds to ACK and EOT identically.

3.2.1.9 <u>NAK – Negative Acknowledge</u> – NAK indicates that the previous block in the transmission was not accepted and that the receiver is ready for retransmission. The interface responds to NAK and EOT identically.

3.2.1.10 <u>DLE – Data Link Escape</u> – DLE provides additional BSC control signals by changing the meaning of the character that follows it. Section 3.2.2 discusses the use of DLE for controlling transparent mode. Section 3.2.1.11 discusses the use of DLE in two character affirmative acknowledge sequences.

3.2.1.11 <u>Stick Characters</u> – Any stick character preceeded by DLE forms part of a two character control sequence. When transmitting, the interface recognizes DLE "Stick" as a legitimate message terminator. When an interface in Receive Mode detects DLE "Stick", it transfers both characters to memory and then sets the RDY bit (CSR bit-07). This feature is intended primarily for the detection of the BSC affirmative acknowledge sequences which are DLE0 and DLE1 for ASCII and DLE "160_8" and DLE / for EBCDIC.

3.2.2 <u>Transparent Mode</u>

Transparent mode control is provided automatically by the DQS11. The DQS11 remains in the character mode until the data link escape (DLE, 020_8), start of text (STX, 002_8) sequence is recognized in the message. All subsequent data is in the transparent mode. Because line control is provided in the transparent mode by DLE, whenever the DLE bit pattern (020_8) is encountered during transparent text, it must be paired with a second DLE if it is not intended as a control character. When transmitting in transparent mode, the interface generates an additional DLE following every DLE in the message except when Byte Count Overflow is set indicating the end of the message. This exception specifies that the control DLE in the terminating DLE ETX (or DLE ETB) sequence is not padded. When receiving in transparent mode, the interface strips (does not transfer to memory) the first DLE in every DLE DLE sequence received. All control characters not preceeded by an unpaired DLE are treated as data.

3.2.2.1 <u>DLE STX - Start of Transparent Text</u> - All characters following DLE STX are treated as transparent text. If an SOH character has been detected, the interface includes both DLE and STX in the CRC accumulation. Otherwise, CRC accumulation begins with the character following STX. The text and CRC accumulation are both terminated by either DLE ETX or DLE ETB.

3.2.2.2 <u>DLE ETX - End of Transparent Test</u> - DLE ETX terminates a block of transparent text started with DLE STX and transmitted as an entiry. When transmitting, the interface sends the two CRC bytes immediately following ETX. When receiving, the interface shifts ETX and two following bytes into the CRC accumulator and sets an ERROR Flag if the result is not zero. In neither case is the DLE control character included in the CRC accumulation.

3.2.2.3 <u>DLE ETB - End of Transparent Block</u> - The interface treats DLE ETB and DLE ETX identically.

3.2.2.4 <u>DLE ENQ - End of Faulty Transparent Text</u> - When transmitting in transparent mode, and if the message is not properly terminated, the interface sets Long Message error and terminates the message by generating the DLE ENQ sequence. When receiving in transparent mode, the interface recognizes the DLE ENQ sequence as a message terminator.

3.2.2.5 <u>DLE SYN - Transparent Synchronous Idle</u> - DLE SYN is used as a time fill to retain character synchronization in a transparent text message. Because the DMA facilities provide data must faster than the transmission rate, the interface is never required to generate the DLE SYN sequence. If the data is not provided, the DMA ERROR Flag is set and the message is terminated. However, when receiving in transparent mode, the interface detects and strips all DLE SYN sequences. Both characters are omitted from CRC accumulation.

3.2.3 <u>Cyclic Redundancy Check</u>

The DQS11 hardware provides a cyclic redundancy checking (CRC) feature to facilitate error detection in messages in both the character and transparent modes. Two 8-bit CRC bytes are derived from the circuit-implemented cyclic redundancy checking polynominal $X^{16} + X^{15} + X^2 +1$ (IBM CRC - 16 compatible). Whether transmitting or receiving, CRC accumulation starts with the character following the first SOH or STX control character in the data block. In character mode, all characters except SYN are included in the CRC accumulation. In transparent mode all characters except DLE SYN sequences, one DLE of DLE DLE sequences, and the DLE of

the terminating sequence (DLE ETX, or DLE ETB) are included in the CRC accumulation. When transmitting, the interface sends the two CRC bytes immediately following the terminating ETX (or ETB). When receiving, the interface shifts the ETX (or ETB) and the two following bytes into the CRC accumulator and sets an ERROR Flag if the result is not zero.

The Hardware which implements the CRC function can be modified as required to provide compatibility with remote terminal equipment. Consult DEC Special Systems personnel for information.

3.3 TRANSMIT

The DQS11 is initialized to the transmit idle state (RX bit clear, RDY bit set). The software initiates transmission by clearing the RDY bit with a GO Command to the CSR (bit-0 set). Immediately upon entering the transmit active state (RX bit clear, RDY bit clear), the DQS11 raises Request to Send (Connection CA) to the modem. When the modem responds with Clear To Send (Connection CB) and Transmitter Signal Element Timing (Transmit Clock, Connection DB), the DQS11 transmits four SYN characters followed by the message data retrieved from memory.

Before issuing the GO Command, the software loads the Bus Address Register with a pointer to the even byte which contains the first character and loads the Byte Count Register with the negative of the number of characters to be transmitted. When transmitting normal text, the last character must be either a terminating control character (ETX, ETB, ENQ, ACK, or NAK) or part of a two character terminating sequence (DLE "Stick"). When terminating transparent text, the last two characters must be one of the terminating control characters preceeded by DLE (e.g. DLE ETX, DLE ETB, or DLE ENQ). Otherwise, a Long Message error will occur. After sending the entire message, including the two CRC bytes (if applicable) and one pad character (a 377_8), the DQS11 sets the RDY bit and, if Interrupt Enable is asserted, causes the processor to trap to the interface's vector address. The Build mode feature of the DQS11 reduces the core memory required for message storage by allowing the software to build messages during transmission and store the message segments in two or more memory buffers. For example, the software stores the first segment in buffer one, initializes the Bus Address and Byte Count Registers, and asserts Build mode (CSR bit-02) when issuing the GO Command. The software stores the second segment in buffer two and then waits for the DQS11 to assert the RDY bit, indicating that the first segment has been sent. Because Build mode is asserted, the interface does not look for a terminating character, but asserts RDY when byte count overflow sets. The software reinitializes the Bus

Address and Byte Count Registers for the new buffer, issues a new GO Command and then stores the next segment in the buffer area which is now available. This process continues through the last segment except that, when the final GO Command is issued, Build Mode must be cleared, causing the interface to search for and recognize the terminating character.

3.4 RECEIVE

The DQS11 is placed in the Receive mode by setting Bit-1 in the CSR. Immediately upon entering the Receive Mode, the DQS11 monitors the Receiver Signal Element Timing (Receive Clock, Connection DD) from the modem. When the Receive Clock becomes active, the Received Data (Connection BB) is monitored for SYN. When two consecutive SYN characters are detected, the DQS11 becomes synchronized. If the software has initialized the Bus Address and Byte Count Registers and issued a GO Command to the CSR, data transfer begins with the first Non-SYN character and continues until either Byte Count Overflow occurs or a terminating control character is received. If Byte Count Overflow occurs before a terminating character is detected, Long Message Error and DMA Error are set. Although data transfer ceases, RDY is not set until the terminating character (and CRC bytes, if applicable) has been received. If a GO Command has not been issued, the detection of the first Non-SYN character causes DMA Error to be set. No data is transferred to memory.

The Build Mode feature of the DQS11 reduces the core memory required for message storage by allowing the interface to store segments of the message in two or more independent memory buffers as directed by software. Once received, each segment must be processed or transferred to secondary storage before the software reassigns that buffer to the interface. For example, the software initializes the Bus Address and Byte Count Registers and issues a GO Command while asserting BUILD and RX. At each instance that the interface asserts RDY, the software tests the BUILD bit to determine if it has been cleared by the interface. If Build Mode is still set, the software reinitializes the Bus Address Byte Count Register and issues another GO Command, leaving BUILD and RX asserted. The clear condition of Build Mode specifies that the entire message has been received. The software checks the error bits and sends the relevant positive or negative acknowledge character.

3.5 INTERRUPTS

Conditions required for trapping to the DQS11 Vector Address and service routine timing restrictions are discussed in this section.

3.5.1 Interrupt Level And Vector Address

The interrupt level and the vector address for each DQS11 is determined at system configuration time. The DQS11 will cause the processor to trap to its vector address if the following conditions are true.

    a.   The unit's interrupt enable is asserted and

    b.   The units RDY bit is asserted and

    c.   The units interrupt level is greater than the current processor priority and

    d.   No higher priority devices are requesting attention.

3.5.2 Service Routine Timing Restrictions

The DQS11 imposes no timing restrictions on service routines which respond to the end of a Transmit or Receive Mode operation; however, when using Build Mode, the service routine must set up a new buffer and issue a GO Command during the interval between two NPR transfers. When transmitting in Build Mode, all memory blocks except the last must contain an even number of characters. A time interval, defined as 15/BAUD RATE (368 microseconds for 40.8K Baud), is allowed between setting the interrupt request and completion of the NPR data transfer, initiated by the GO Command. In Receive Mode, a similar interval is allowed between the beginning of the NPR transfer which sets Byte Count Overflow and the time when the service routine issues the GO Command.

SECTION 4
THEORY OF OPERATION

4.1 THE DQS11 AND THE UNIBUS

All logic described in this section appears on Drawing DQS11-0-0-2. All transfers of information between the central processor and the DQS11 or between the DQS11 and memory occur via the Unibus on a master/slave basis. During a program controlled transfer, the processor, as Bus Master, loads or reads one of the four device registers. The register addresses are decoded from the Bus Address Lines by the M105 Address Selector card which also provides the necessary slave response. The M105 output signals are combined on the M8506 Control card to produce the signals which load the registers or gate their contents onto the Data Bus.

The DQS11, as Bus Master, can transfer data directly to or from memory. The logic for requesting and acknowledging control of the bus is contained on the M7821 Interrupt Control card and the M796 Unibus Master Control card. When the DQS11 becomes Bus Master, the M796 card generates the Master control signals to the Unibus and the internal signals which gate the slave address onto the Bus Address lines. These internal signals enable the Data Buffer or gate its contents onto the Bus Data lines, depending on the direction of data transfer. The slave address, contained on the M795 Word Count and Bus Address card, is incremented by two at the completion of each transfer.

The M7821 card also contains logic for generating a program interrupt request. An interrupt request occurs if both the RDY and the Interrupt Enable bits (Controller Status Register Bits 7 and 6) are set. The level of the interrupt is determined by a jumper plug located on the M8504 (M8505 for DQS11-B) register card, IC slot E1. Figure 4-1 is a general block diagram of the device.

The two M785 Transceiver cards contain Bus Data line receivers for the Controller Status Register and the Data Buffer and Bus Data Line drives for the Controller Status Register. The Bus Data line drivers for the Data Buffer are located on the M8504 (M8505) Register Card.

Part 2 of the PDP-11 Peripherals and Interfacing Handbook contains a detailed description of Unibus Operation and of the standard Unibus interfacing modules used in this device (M105, M7821, M785, M795 and M796 modules).
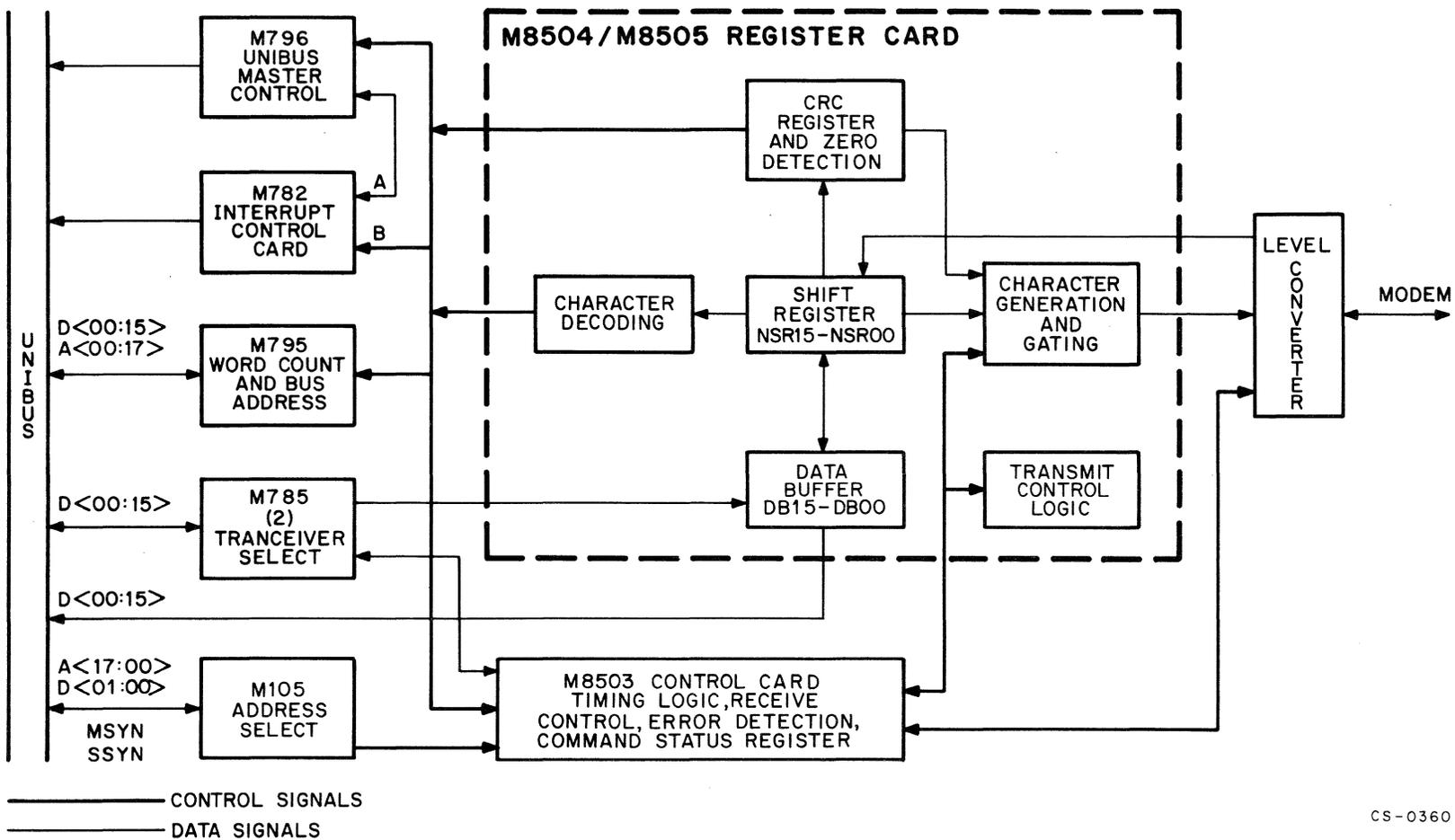
Figure 4-1 General Block Diagram

4.2   THE DQS11 AND THE MODEM

All logic described in this section appears on Drawing DQS11-0-02 (Sheet 2 of 3). The DQS11 asserts Circuit CD-Data Terminal Ready whenever power is supplied to the system unit. When The DQS11 has a message to be transmitted, it asserts Circuit CA-Request to Send. When the modem responds by asserting Circuit CB-Clear to Send, the DQS11 Monitors Circuit DB-Transmitter Signal Element Timing for internal clocking and output serial data on Circuit BA-Transmitted Data. When in Receive Mode, the DQS11 monitors Circuit DD-Receiver Signal Element Timing for internal clocking and monitors Circuit BB-Received Data for Serial Data In.

Controller Status Register bits 8 and 9 reflect the status of Circuit CF-Data Carrier Detector and Circuit CC-Data Set Ready respectively. The status bits are asserted whenever respective signals are off.

EIA Standard RS-232-B, Interface Between Data Processing Terminal Equipment and Data Communication Equipment, contains a more complete description of these signals.

4.3   DATA FLOW DURING TRANSMISSION

The logic described in this section appears on drawing M8504-0-01 (DQS11-A) and on drawing M8505-0-01 (DQS11-B). The CRC and NSR Registers appear on sheet 4 of 6. The Data Buffer Register and character generation logic appear on sheets 3 and 6 respectively.

The serial data sent to the modem has three possible sources: the 16-bit shift register (data originating in core memory), the 16-bit CRC register (the two Cyclic Redundancy Check Characters which follow a terminating ETX or ETB) and a multiplexer controlled by the transmit logic (for interface generated characters SYN, DLE and ENQ). Serial Data Out is asserted during the transmission of the required final pad character. Serial Data Out also serves as the input to the CRC register, which is initialized by the first STX or SOH character in a message. The CRC register is inhibited (not strobed) during the transmission of characters which should not be included in the accumulation.

The portion of the message originating in core memory is transferred from memory to the 16-bit Data Buffer (DB15-DB00) in two character blocks. The even byte (DB07-DB00) contains the first character (of the two) to be transmitted. DB00 contains the least significant bit, which is the

first bit to be transmitted. The complements of data buffer bits DB15-DB00 are transferred in parallel to shift register bits NSR15-NSR00 respectively.

4.4 TRANSMIT MODE CONTROL LOGIC

This section contains a description of events which occur within the Transmit Mode Control logic during a data transfer operation. Control logic pertaining to Transmit mode only appears on drawing M8504-0-01 (M8505-0-01 for the DQS11-B), Sheet 2 of 6. Control logic used by both Transmit and Receive mode appears on Drawing M8506-0-01, Sheet 2 of 5. Timing logic appears on Drawing M8506-0-01, Sheet 4 of 5.

4.4.1 The Register And the Counter

During transmission, the DQS11 bases its internal clocking on Circuit DB-Transmitter Signal Element Timing from the Modem. Changes in the serial data sent to the modem occur at the time of Circuit DB transitions from the OFF to the ON condition. The following operations occur on this clock edge:

a. The shift register is loaded if the state flip-flops SHFT SR and SRINH are both in the clear condition.

b. The contents of the shift register are shifted one bit to the right if state flip-flop SHFTSR is set and state flip-flop SRINH is clear.

c. The previous data out bit is shifted into the CRC register if state flip-flop CRC ON is set and state flip-flop CRCINH is clear.

d. The divide by eight counter is incremented. When the output data is the first or least significant bit of a character, this counter equals one, and the signal CNTR1 is asserted. When the output data is the eighth or most significant bit of a character, this counter equals zero (0) and the signal CNTR0 is asserted. Signals C1, C2 and C4 represent the binary coded value of the counter and serve as input to the multiplexer which generates the SYN, DLE and ENQ characters.

4.4.2 State Flip-Flops Strobed By TOGCND

The serial data sent to the modem remains constant during Circuit DB transitions from the ON to OFF condition. This transition, gated by CNTR1, is the leading edge of the signal TOGCND, which strobes those state flip-flops whose state depend on the identity of the character being

transmitted. The control characters are decoded from the shift register byte NSR 07–NSR 00, which contains the entire character when CNTR1 is asserted. The following state flip-flops are strobed by the leading edge of TOG CND:

a. If DLESTR is in the clear condition and if the present character is a DLE, then DLESTR is set by TOG CND; otherwise, it is cleared.

b. If the present character is either SOH or STX, then STX SOH is set and remains set until the end of transmission.

c. If STX SOH is already set, then CRCON is set, causing CRC accumulation to begin with the first character following the initial SOH or STX.

d. If DLESTR is set and the present character is STX (indicating the DLESTX sequence), then TRNSP is set and remains set until the DLE ETX or DLE ETB sequence terminates transparent mode.

e. If TRNSP is set, DLESTR is clear, and the present character is DLE, then CRC INH is set. Thus, in transparent mode, the first DLE of all two character control sequences is omitted from CRC accumulation.

f. If SNDDLE is set (indicating that the interface is generating a DLE character), SRINH is set to inhibit the shift register, preventing the loss of one character.

g. If LSTCHR is set (indicating that the present character is the last character coming from core memory), if RFC (Ready For Command) is asserted (indicating that either transmission is in non-transparent mode or that the present character was preceeded by a single DLE), and if ENDCHR is asserted (indicating that a correct non-CRC termination is present), then STREC is set.

h. If LSTCHR is set, if RFC is asserted, and if the present character is either ETX or ETB, then STP1 is set, beginning the CRC termination sequence. The state of STP1 is strobed into STP2 and the state of STP2 is strobed into STP3.

i. If LSTCHR is set and if a correct termination character is not present, then NOEND is set.

4.4.3 State Flip-Flops Strobed By CNTR1

The leading edge of CNTR1 signals that the first bit of the next character is set up for transmission. This leading edge strobes the state flip-flops, including those which determine the origin and composition of the serial data, in the following manner:

a. SNDSYN is held clear when RX is set and is held set during the transmission of the four leading SYN characters. Once TRENB4 is asserted, SNDSYN is strobed clear by the next CNTR1 pulse and remains clear until the end of transmission.

b. SND DLE is set by CNTR1 causing the interface to generate a DLE character if either one of two condition is met: If TRNSP and DLESTR are both set and the conditions for setting LSTCHR are not met, then a data DLE character has been detected and must be padded with an additional DLE; if TERMT (Terminate Transmission) is asserted (indicating a fault condition) and RFC (Ready for Command) is not asserted, then a DLE must be generated to preceed the terminating ENQ.

c. If TERMT and RFC are both asserted, then SND ENQ is set by CNTR1 to generate a terminating ENQ character which indicates faulty transmission.

d. If STP1 or STP2 was set during the transmission of the previous character, then SNDCRC is strobed set and the CRC register is the origin of the serial data out.

e. If SNDENQ was previously set or if TRNEND is asserted (indicating that the entire message, including CRC characters if necessary, has been sent), then PAD CHR is set, causing the interface to generate a final pad character (377_8).

f. If PAD CHR was previously set, CNTR1 sets DONET which sets the RDY flip-flop.

g. If OVF has been set by the Byte Count Register, if BUILD is not set, and if the contents of the Data Buffer have been transferred to the shift register, then LST CHR is set, indicating that the character being transmitted is the last character coming for core memory.

h. If, because of system failure, no data is ready for transmission, DMA FLT (DMA Failure during Transmission) is set by CNTR1.

4.4.4 Control Of Parallel Data Flow

During transmission, the control of parallel data flow depends on the following four state flip-flops on the M8504 (M8505) Register Card:

a. DBFULL is set at the end of an NPR transfer of data from memory to the data buffer. DBFULL is cleared when SHFTSR is cleared.

b. SHFT SR is always set except when the contents of the data buffer are loaded into the shift register. SHFTSR is cleared by the trailing edge of STRBSR only if four

conditions are met: CNTR0 must be asserted, indicating that the next STRBSR will set up the first bit of a new character; SREMP must be set, indicating that both characters previously loaded into the shift register have been transmitted; DBFULL must be set; and SRINH (Shift Register Inhibit) must be clear.

c.   SREMP (Shift Register Empty) is held clear when SHFTST is in a clear condition. Otherwise, SREMP is strobed set by CNTR1 if either SREMP was previously set or if SRINH is clear.

d.   DMAENBT (Transmit Mode DMA Enable) is set by the trailing edge of STRBSR if SHFTSR was previously cleared. Assuming OVF and DBFULL are not set, DMAENBT allows the trailing edge of the next STRBSR to initiate a DMA request.

4.5   RECEIVE MODE DATA FLOW

All logic described in this section appears on Drawing M8504-0-01 (M8505-0-01 for DQS11-B), Sheets 3 and 4 of 6.

The serial data from the modem is loaded first into shift register byte NSR07-00 where most of the character decoding takes place. The data shifted from NSR00 provides input both to shift register byte NSR15-08 and to the 16-bit CRC register. When the shift register contains two complete characters, one or both of them may be transferred in parallel to the data buffer. Because the character in NSR15-08 preceeded the character in NSR07-00, this character is transferred into the low data buffer byte, DB07-00. The character in NSR07-00 is loaded into DB15-08. Normal mode SYN characters, transparent mode DLE SYN sequences and the first DLE of transparent mode DLE DLE sequences are not part of the message and, therefore, are not sent to the computer memory.

Whenever the shift register contains two complete characters, one of the following conditions results:

a.   If the data buffer is empty and the character contained in NSR15-08 is not part of the message, no data transfer occurs.

b.   If the data buffer is empty and the character contained in NSR15-08 is part of the message, both shift register bytes are loaded into the Data Buffer. The Data Buffer is now considered half full.

c.   If the Data Buffer is half full and the character contained in NSR15-08 is not part

of the message, the character in NSR07-00 is loaded into DB15-08 where it replaces the character in NSR15-08. The Data Buffer is still considered half full.

    d.   If the Data Buffer is half full and the character contained in NSR15-08 is part of the message, the contents of the Data Buffer are transferred to core memory. After completion of the transfer, the data Buffer is again considered empty.

4.6 RECEIVE MODE CONTROL LOGIC

This section contains a description of events which occur within the Receive Mode control logic during a data transfer operation. Most of the logic described in this section appears on Drawing M8506-0-01 (Sheet 2 of 5).

4.6.1 The Registers And The Counter

When in Receive Mode, the DQS11 bases its internal timing on Circuit DD-Receiver Signal Element Timing from the modem. The transition of Circuit DD from ON to OFF indicates the center of each signal element on Circuit BB-Received Data. The following operations occur on this clock edge:

    a.   The contents of the shift register are shifted one bit to the right. Received data provides the input to NSR07. NSR00 provides the input to NSR15.

    b.   The content of NSR00 is shifted into the CRC register if state flip-flop CRC ON is set and state flip-flop CRC INH is clear.

    c.   The divide by eight counter is held equal to zero until two consecutive SYN characters are received. When the first, or least significant bit of the next character is received, the counter is incremented to one and CNTR1 is asserted. After the eighth or most significant bit has been received the counter equals zero and CNTR 0 is asserted.

4.6.2 State Flip-Flops Strobed After Every Bit

The transition of Circuit DD from OFF to ON is used by the DQS11 to strobe the following state flip-flops:

    a.   INSYNC is strobed set when both shift register bytes contain SYN characters. It is forced clear either by SET RDY or by RX bit clear.

b. When LDDB is set, both shift register bytes are transferred into the Data Buffer. LDDB is strobed set when the following conditions are met: CNTR0 is asserted, indicating that the shift register contains two complete characters; DBEMP (Data Buffer Empty) is set; DBTAK is set; DATDIS is not asserted indicating that the character destined for the data buffers low byte (DB07-00) is part of the message.

c. When LDHB is set, shift register byte NSR07-00 is transferred to the high data buffer byte (DB15-08). LDHB is strobed set when the following conditions are met: CNTR0 is asserted; DBEMP (Data Buffer Empty) is clear; DBTAK is clear, indicating that the Data Buffer is only half full; DATDIS is asserted, indicating that the character which was sent to DB15-08 during the last transfer is not part of the message and should be replaced by the next character which is now in NSR07-00.

d. DMAFLR (Receive Mode DMA Failure) is strobed set when the following conditions are met: CNTR0 is asserted; DBEMP (Data Buffer Empty) is clear; DBTAK is set, indicating (with DBEMP Clear) that the Data Buffer is completely full and should have been transferred to memory, setting DBEMP; DATDIS is not asserted, indicating that data is available for transfer to the data buffer.

4.6.3   State Flip-Flops Strobed By TOGCND

When the transition of Circuit DD from OFF to ON is gated by CNTR 0, it becomes the leading edge of TOGCND which strobes the state flip-flops whose states depend on the identity of the last character received. The control characters are decoded from shift register byte NSR07-00, which contains the entire character when CNTR 0 is asserted. The following state flip-flops are strobed by TOG CND:

a. DLESTR, STXSOH, CRCON, TRNSP, and CRCINH state flip-flops function as described in Section 4.4.2.

b. If RFC (Ready For Control Character) is asserted and if END CHR is asserted (indicating that a correct non-CRC termination is present), then STREC is strobed set.

c. If RFC is asserted and if the present character is either ETX or ETB, then STP1 is strobed set, beginning the CRC termination sequence. With each successive TOG

CND, the state of STP1 is strobed into STP2 and the state of STP2 is strobed into STP3.

d. DATENB is strobed set if INSYNC has been set, if a message terminator has not yet been recognized, and if the character is NSR07-00 is not a control SYN character. The character is then shifted into NSR 15-08 and is accepted as part of the message if DATENB is set and if it is not a transparent mode control DLE character followed by either a data DLE or a control SYN character.

e. FINRCV (Finish Receive) is strobed set if STP1 is set, if STREC is set, or if FINRCV has already been set.

f. DONER is strobed set by the trailing edge of TOGCND if FINRCV was set by the leading edge. If DONER and DBEMP are both set and if CRCIP (CRC in process) is not asserted, RDY is set.

4.6.4 Control Of Parallel Data Flow

The Control of parallel data flow depends on the following four state flip-flops on the M8506 Control Card.

a. LDDB and LDHB are described in Section 4.6.2.

b. DBEMP is set either by a software initiated GO Command or by the completion of an NPR data transfer from the Data Buffer to core memory. It is cleared when DBTAK is cleared, indicating that the data buffer is half full.

c. DBTAK is set at the start of Receive Mode operation and remains set until data is transferred to the Data Buffer. DBTAK is strobed clear by TOG CND whenever LDDB or LDHB are being set. DBTAK clear indicates that the Data Buffer is half full. When the Data Buffer contains two valid message characters, DBTAK is strobed set, initiating an NPR data transfer from the Data Buffer to core memory.

SECTION 5
MAINTENANCE

5.1 SPECIAL TEST EQUIPMENT

No special test equipment is required for maintaining the DQS11.

5.2 MAINTENANCE TECHNIQUES

Maintenance procedures are based primarily on the DQS11-A and DQS11-B diagnostics described in Appendix A. These diagnostics not only isolate and describe individual failures, but can be caused to loop on any particular test for use with an oscilloscope. An additional feature allows the technician to step through the simulated transmission or reception of data on a bit-by-bit basis.

The DQS11-A and DQS11-B Modem Exercisers are described in Appendix B. Assuming the diagnostic runs correctly, problems uncovered by the Modem Exerciser will probably be traced to the level converter card (M594 or M595), the logic and signal paths leading directly to or from that card, or the modem and modem connections.

SECTION 6
MODULE LIST

6.1 MODULES

Table 6-1 lists the DQS11 modules by type number, function, and system unit slot location.

Table 6-1
DQS11 Module Complement

DEC Type No.	Function	Slot Location
G8000	+8V Filter	A02
M105	Address Selector	B02
M594*	EIA Voltage Converter	D04
M595*	Current Level Converter	D04
M7821	Interrupt Control	B03
M785	Unibus Transceiver	C03
M785	Unibus Transceiver	D03
M795	Word Count And Bus Address	EF03
M796	Unibus Master Control	E04
M8504†	DQS11-A Register Card	CDEF01
M8505†	DQS11-B Register Card	DCEF01
M8506	DQS11 Control Card	CDEF02

*DQS11 system unit slot D04 contains an M594 for interfacing modems which feature EIA voltage signals or an M595 for interfacing modems which feature current signals.

†DQS11-A system unit slots CDEF01 receive the M8504 Register Card. DQS11-B system unit slots CDEF01 receive the M8505 Register Card.

APPENDIX A
DQS11 DIAGNOSTIC PROGRAM DESCRIPTION

A.1 ABSTRACT

The DQS11-A Diagnostic Program (DECSPEC-11-ARIAD) and the DQS11-B Diagnostic Program (DECSPEC-11-ATKAD) are identical except that the first features ASCII characters as test data and the second uses EBCDIC code. Each diagnostic consists of 161 independent tests designated octally from "TEST1 to TST241". The first 33 tests (TEST1-TEST41) ch ck the initialization loading and reading of the device registers. The next 43 tests (TEST42-TST114) simulate the transmission of a wide range of character strings which check the Transmit Mode control logic. The next 77 tests (TST115-TST231) check the Receive Mode control logic. Five tests (TST232-TST236) check the device's interrupt logic. The remaining tests check the ECO's that have been implemented. See the assembly listing for a description of each test.

Two program start locations are available to provide for instances where the operator must specify a new device code and vector address. These are as follows:

a. 1000_8 (program requests new device code).

b. 1010_8 (program does not request new device code).

If computer console switches (15-11) remain clear, the program runs continuously, returning to TEST1 after completing TST235. Following each complete pass, the program types the character "1". Should a test fail, the program types out a description of the error and continues with the next test. By setting certain computer console switches, the operator can control program operation to assist troubleshooting. Table A-1 lists the switch options available to the operator.

A.2 REQUIREMENTS

The DQS11 is intended for use within a PDP-11 System where certain half-duplex synchronous communications equipments (modems) are implemented. The diagnostic program runs with the modem detached from the system. The minimum required configuration consists of a PDP-11 with 8K core storage, one interface with or without modem, and an ASR-33 teleprinter.

Table A-1
Program Switch Options

Switch	Position	Function
SW15	SET	Enter wait loop after completing current test.
SW14	SET	When SW15 is toggled clear, begin the test designated octally in switches 07-00.
SW13	SET	Loop on test.
SW12	SET	Suppress teleprinter output.
SW11	SET	Step through those tests which simulate the transmission or reception of data. Enable Switches 10 and 9.
SW10	SET	If SW11 is set and SW9 is clear, pause on high clock pulse.
SW10	CLEAR	If SW11 is set and SW9 is clear, pause on low clock.
SW09	SET	If SW11 is set, pause between characters.
SW07-00		Contains an octal test number used with SW14.

A.3 LOADING PROCEDURE

The diagnostic is contained on one binary tape, DECSPEC-11-ARIAD-PB for the DQS11-A and DECSPEC-11-ATKAD-PB for the DQS11-B. This punched paper tape is loaded through either the teleprinter or the high speed reader (if available) using the binary loader.

A.4 OPERATING PROCEDURE

Before running the diagnostic, turn off system power and remove the converter module from slot D04 of the device system unit. When using a computer other than the PDP-11/15 or PDP-11/20, the operator must correct the 100 msec delay by altering location "LUPTIM". For instructions, refer to the assembly listing subroutine "DL100M".

A.4.1 Starting Addresses

Each DQS11 in a PDP-11 system must have a unique device code and vector address. To initialize the diagnostic for a particular device, start at location 1000_8. The program immediately types out "DEVICE CODE=". Type in the device code as six octal number e.g., 165050 followed by a carriage return. If an illegal code (less than 164000) is received, or if the

operator types the character "RUBOUT", the program repeats the request. The program stores a valid device code and then types out "VECTOR ADDRESS=". Type in the vector address as three Octal numbers e.g., 150 followed by a carriage return. If an illegal address is received, or if the operator types the character "RUBOUT", the program repeats the request. The program stores a valid vector address and then begins with TEST1.

To restart the diagnostic without changing the device code and vector address, begin at location 1010_8. The diagnostic is loaded with the device code 165040 and the vector address 140.

A.4.2   Option Switches

Table A-1 lists the switch options available to the operator. For normal operation of the diagnostic, computer console switches 15-11 must be in the clear position. The diagnostic then executes all tests sequentially, returning to TEST1 after completing TST236. The character "1" is typed at the end of each pass. A carriage return/line feed precedes each group of 50 1's. By setting and clearing combinations of the console switches, the operator can transfer control to specific tests, loop on any one test, suppress teleprinter output, and cause the diagnostic to enter a wait loop at certain points within tests which simulate transmission or reception of serial data.

A.4.2.1   The Test Monitor – After completing each test, the diagnostic enters a subroutine (MONITOR) which scans certain console switches. If Switch 15 is clear, control is transferred either to the next sequential test (Switch 13 clear) or the last test completed (Switch 13 set). Thus, setting Switch 13 causes the diagnostic to loop on one test. If Switch 15 is set, the diagnostic enters a wait loop where it remains until the operator clears that switch. If Switch 14 is set when the diagnostic leaves the wait loop, program control is transferred to the test specified in Switches 07-00. If Switch 14 is clear, control is transferred to the next sequential test (Switch 13 clear) or the last test completed (Switch 13 set).

If Switch 13 is set during an error printout, the diagnostic loops on that test until the switch is cleared. To loop on a test for which no error printout is provided, set Switches 15, 14 and 13 and set the octal number assigned to the test in Switches 07-00. Waiting several seconds (for completion of the previous test), then clear Switch 15.

A.4.2.2   Printout Suppression – When Switch 12 is set, all teleprinter output is suppressed. By setting Switch 12 while looping on a test (Switch 13 set), the resulting tight loop facilitates tracing signals with an oscilloscope.

A.4.2.3 <u>Transmit And Receive Clock Simulation</u> - Tests which check out the transmit and receive control logic use the TEST CLOCK bit (Bit-8 of the Controller Status Register) to simulate transmit and receive clock pulses. Using computer console Switches 11, 10 and 9, the operator can cause the diagnostic to enter a wait loop:

a. Before the next group of eight clock pulses (if Switch 11 and Switch 9 are set) or

b. After the next leading (setting) edge of the clock (if Switch 11 and Switch 10 are set and if Switch 9 is clear) or

c. After the next trailing (clearing edge of the clock (if Switch 11 is set and if Switch 10 and Switch 9 are clear).

To sequence through a test, set up a loop on the test and then set Switch 15. Wait several seconds for the completion of the test and then set Switches 11 and 9. When Switch 15 is cleared, the test performs the initial instructions and enters a wait loop before the first clock pulse. Interface status may be electrically checked at this point. Clearing Switch 9 causes the program to enter another wait loop either after one half clock pulse (Switch 10 set) or one complete clock pulse (Switch 10 clear). The operator can then either sequence through a half pulse at a time (by alternately setting and clearing Switch 10) or eight pulses at a time (by clearing Switch 09).

A.5 ERRORS

Eight categories of error subtests exist which are used by each test either individually or in combination. The subtests are designed and located to provide maximum information about any fault that occurs. A RESET instruction is executed at the beginning of each test. Error recovery is, therefore, automatic.

A.5.1 <u>BITCHK (Bit Check)</u>

BITCHK compares the actual bit pattern resulting from a particular test with the known pattern. If the patterns are not identical, a typical error message is: "DURING TEST 3 THE BIT PATTERN WAS 140000 INSTEAD OF 100000". In this case, TEST 3 loaded the Word Count Register with 100000 but read back 140000.

A.5.2 <u>CHBAWC (Check Bus Address And Word Count)</u>

CHBAWC compares the contents of the Bus Address Register and Word Count Register with the

correct values. If the content of either register does not agree with its respective known correct value, an error is signaled. A typical error message is: "DURING TEST 32 THE BUS ADDRESS WAS 2 INSTEAD OF 4. DURING TEST 32 THE WORD COUNT WAS 2 INSTEAD OF 3". The Bus Address and Word Count Registers should have been incremented by the occurance of a second DMA transfer. The interface probably failed to initiate that transfer.

A.5.3   CHKCHR (Check Characters)

CHKCHR compares two tables of characters. An error is signaled if the two tables are not identical. One table contains those characters transmitted or received in the given test. The other table contains the correct values. A typical error message is: "TEST 42 RESULTED IN THE FOLLOWING INCORRECT CHARACTERS: #6 WAS 115 (M) INSTEAD of 315 (M). #7 WAS 71 (9) INSTEAD OF 271 (9)". The DQS11-A failed to generate odd parity.

The subroutine VRFYTR (verify transmit) and CHKRCV (receive check) both use CHKCHR. VRFYTR also uses the subroutine SNDCHR (send characters) to simulate transmission. CHKRCV is described in Section A.5.4.

A.5.4   CHKRCV (Check Receive)

CHKRCV checks the contents of the Bus Address Register and signals an error if too few data transfers to memory occurred. A typical error message is: "DURING TEST 131 THERE WERE ONLY 2 CHARACTERS TRANSFERRED TO MEMORY". Four characters should have been transferred. CHKRCV then uses CHKCHR (Section A.5.3) to check those characters which were transferred to memory and to indicate any errors.

A.5.5   STATUS And STAMSK (Status Masked)

STATUS checks all 16-bits of the Controller Status Register and signals an error if an incorrect bit is detected. STAMSK performs the same function but checks only 14-bits, omitting Bit-8 and Bit-9. A typical error message is: "TEST 43 RESULTED IN THE FOLLOWING INCORRECT STATUS BITS: BIT-12 WAS CLEAR. BIT-15 WAS CLEAR". The test should have resulted in a Long Message error. The purpose of each CSR bit is explained in Section 3.1.1.

A.5.6   TRPNO (NO TRAP)

Certain tests which do not expect a device interrupt use the subroutine TRPNO which signals

an error if the system traps to the device's vector address. A typical error message is: "DURING TEST 232 THE SYSTEM TRAPPED TO 140". The device should not have interrupted because the Interrupt Enable bit was not set.

A.5.7 TRPYES (TRAP EXPECTED)

TRPYES signals an error if an expected device interrupt did not occur or if the system trapped to the device's vector address more than once. Typical error messages are: "DURING TEST 234 THE SYSTEM FAILED TO TRAP TO 140" and "DURING TEST 236 THE SYSTEM TRAPPED TO 140 MORE THAN ONCE".

A.5.8 TRPSUB (TRAP SUBROUTINE)

TRPSUB signals an error whenever the system traps to a vector address other than the device's vector address. A typical error message is: "DURING TEST 234 THE SYSTEM TRAPPED TO 310. RETURN ADDRESS IS 15264". The return address indicates which portion of the diagnostic was being executed when the interrupt occurred.

APPENDIX B
DQS11 MODEM EXERCISER PROGRAM DESCRIPTION

B.1 ABSTRACT

The DQS11-A Modem Exerciser Program (DECSPEC-11-ARIBD) and the DQS11-B Modem Exerciser Program (DECSPEC-11-ATKBD) are identical except that the first uses ASCII characters as test data while the second uses EBCDIC code.

Each program consists of 70 tests which initiate and check the transfer of data between two DQS11 devices. Each program requires that the two devices be located on a common Unibus and that they be attached to two modems through which communications can take place.

Six different data blocks, and several single character control blocks, are sent in both directions. The data blocks include two counting patterns (both normal and transparent text), a random number pattern, and patterns with all bits set, all bits clear, and alternating bits set. Several transmissions are set up incorrectly to test the device's error control facilities.

B.2 REQUIREMENTS

The DQS11 is intended for use within a PDP-11 System where certain half duplex synchronous communications equipments (modems) are implemented. The Modem Exerciser requires that two DQS11 devices be located on a common Unibus and that they be attached to two modems through which communications can take place. The minimum required configuration consists of a PDP-11 with 4K core storage, two interfaces with modems, and an ASR-33 teleprinter.

B.3 LOADING PROCEDURE

The Modem Exerciser is contained on one binary tape (DECSPEC-11-ARIBD-PB) or DECSPEC-11-ATKBD-PB) which is loaded through either the teleprinter or high speed reader (if available) using the binary loader.

B.4 OPERATING PROCEDURE

Before running the Modem Exerciser, turn off system power and attach the modem cables to slots F04 of each DQS11 device system unit. Each DQS11 should have a level converter card in slot F03 of its device system unit. Establish communications between the two modems.

B.4.1   Starting Addresses

Each DQS11 in a PDP-11 system must have a unique device code and vector address. To initialize the Modem Exerciser for two particular devices, start at location 1000_8. The program immediately types out "DEVICE CODE ONE=". Type in the device code as six octal numbers e.g., 165050 followed by a carriage return. If an illegal code (less than 164000) is received, or if the operator types the character "RUBOUT", the program repeats the request. The program stores a valid device code and the types out "VECTOR ADDRESS ONE=". Type in the vector address as three octal numbers e.g., 160 followed by a carriage return. If an illegal address is received, or if the operator types the character "RUBOUT", the program repeats the request. The program stores a valid vector address and then repeats the process with "DEVICE CODE TWO=" and "VECTOR ADDRESS TWO=". After storing the second vector address, the program initiates the first test.

B.4.2   Option Switches

When computer console Switch 12 is set, all teleprinter output is suppressed. The other switches have no effect on program operation.

B.5   ERRORS

At the completion of each test, the devices trap to their respective vector addresses. The service routines check device status and either initiate the next test or set software flags which enable the subroutine MSTCHK (master check). This subroutine not only checks the device status words stored when their respective interrupts occurred, but also verifies the received data. Because MSTCHK is never entered until both devices are in a quiescent state, the flow of data is temporarily interrupted. Some tests regularly enter MSTCHK to verify received data. Other tests enter MSTCHK only when they detect an error in one or both status words.

Five categories of error printouts exist. These are generated either by MSTCHK, by the sub-routine TOERR (Time Out Error), or by TRPSUB (Trap Subroutine). The test during which an error occurred is identified by its decimal number.

B.5.1   CHKCHR (Check Characters)

CHKCHR compares two tables of characters. An error is signalled if the two tables are not

identical. One table contains those characters which were received during a given test. The other table contains the correct values. A typical error message is: "TEST 35 RESULTED IN THE FOLLOWING INCORRECT CHARACTERS: #221 WAS 347 (G) INSTEAD OF 377 (DEL)". Only characters actually received are checked. If an insufficient number of transfers occur, an error printout results. For example, "DURING TEST 3 THERE WERE ONLY 8 CHARACTERS TRANS- FERRED TO MEMORY".

B.5.2   CHKST1 (Check Status Of Device One)

CHKST1 checks 15-bits of the device one Controller Status Register and signals an error if any are incorrect. Bit-8, Carrier Not On, is omitted from the test because its condition is in- determinant at the time of device interrupt. Bit-8 status is reported if an error printout is caused by one of the other bits. A typical error message is: "DURING TEST 5 DEVICE ONE CSR WAS 110300 INSTEAD OF 000300". Bits 15 and 12 were incorrectly asserted, indicating a Long Message error. Because device one was transmitting (bit-1 is clear), this error indicates that the last character was not recognized as a message terminator.

B.5.3   CHKST2 (Check Status Of Device Two)

CHKST2 serves the same purpose for device two as CHKST1 (Section B.5.2) serves for device one. A typical error message is: "DURING TEST 35 DEVICE TWO CSR WAS 104302 INSTEAD OF 000302". Bits 15 and 11 were incorrectly asserted, indicating a cyclic redundancy check error. If one or more data characters were incorrectly received (Section B.5.1), the message was probably altered either by the transmission line or the modems. If the data were received in- correctly and no error bits were set, a problem would exist within the interface.

B.5.4   TOERR (Time Out Error)

A Time Out Error occurs if one or both devices hang up and fail to interrupt. A typical error message is: "A TIME OUT OCCURRED AFTER DEVICE ONE HAD COMPLETED TEST 1 AND BEFORE DEVICE TWO HAD COMPLETED TEST 1". The Time Out Subroutine then uses CHKST1 and CHKST2 (Section B.5.2 and B.5.3) to generate error printouts which describe device status.

B.5.5   TRPSUB (Trap Subroutine)

TRPSUB signals an error whenever the system traps to a vector address other than the two device vector addresses. A typical error message is: "DURING TEST 1 THE SYSTEM TRAPPED

TO 310. RETURN ADDRESS IS 1134". The return address indicates the part of the program being executed when the trap occurred.

APPENDIX C
SHIPPING LIST

C.1 EQUIPMENT FURNISHED (DQS11-A)

A complete DQS11-A device consists of the following:

a. DQS11-A logic, one H933-C (System Unit) including all modules.

b. Unibus Cable Set, BC11A or M920, as required (1 ea).

c. Option Description, CSS-MO-F-3.2-3B (1 ea).

d. Engineering Drawing Set, A-M-L-DQS11-A (1 set).

e. DECSPEC-11-ARIAD, DQS11-A Diagnostic Program binary punched on paper tape (1 ea).

f. DECSPEC-11-ARIAD, DQS11-A Diagnostic Program Listing (1 ea)

g. DECSPEC-11-ARIBD, DQS11-A Modem Exerciser Program binary punched on paper tape (1 ea).

h. DECSPEC-11-ARIBD, DQS11-A Modem Exerciser Program Listing (1 ea)

C.2 EQUIPMENT FURNISHED (DQS11-B)

A complete DQS11-B device consists of the following:

a. DQS11-B logic, one H933-C (System Unit) including all modules.

b. Unibus Cable Set, BC11A or M920, as required (1 ea).

c. Option Description, CSS-MO-F-3.2-3B (1 ea).

d. Engineering Drawing Set, A-M-L-DQS11-B (1 set).

e. DECSPEC-11-ATKAD, DQS11-B Diagnostic Program binary punched on paper tape (1 ea).

f. DECSPEC-11-ATKAD, DQS11-B Diagnostic Program Listing (1 ea).

g. DECSPEC-11-ATKBD, DQS11-B Modem Exerciser Program Binary punched on paper tape (1 ea).

h. DECSPEC-11-ATKBD, DQS11-B Modem Exerciser Program Listing (1 ea).