APPENDIX J

Supervisor 214 SB (Small Box Version)

Contents

J1.0 Introduction

The 214SB is a small box version of the larger 214 system. It has all the features of the larger system in terms of performance and software compatibility with the exception of hardware capacity. The small box version is limited to three backplane assemblies instead of nine which reduces the total printed circuit board capacity to 12 quad size cards.

The 214 SB features DC on-off, halt/enable and line time clock control via switches on the front panel. The switches are supported by indicator Leds for the processor RUN and Active states and also for DC power rail status. A neon indicates the state of the AC mains supply.

J1.1 214 System Manual

The 214 system manual should be used in conjunction with this appendix. Users may recognise text in the 214 manual which will not apply to the small box version and in these cases this appendix should be consulted.

J1.2 Basic Configuration

Gresham Lion PPL Ltd. should be consulted in the event of special requirements. A basic configuration is a graphics system supporting four monochrome channels or a single colour channel with an overlay. An LSI11 processor is included to handle the graphics software routines and has a maximum capacity of eight dual modules.

J1.3 Power Supplies and Power Control

There are three voltage levels in the SB system (+12v, +5v and -5v,) which can be controlled from the front panel. It should be noted that turning the DC off does not render the system safe as AC power is still connected. It does, however, enable the operator to remove the electronic cards without fear of damage. The user should ensure that the voltage indicator Leds extinguish when the DC is turned off.

J2.0 Indicator Panel

The indicator panel gives the user control over both the DC operating voltages and the LSI11 computer.

DC Switch

In the 'ON' position the -5v, +5v and +12v Leds should illuminate. In the 'OFF' position the LEDs should extinguish.

CPU Switch

In the HALT position the BHALT input on the LSI11 processor board is pulled low causing the computer to halt the execution of the user program.

In the ENABLE position the user is able to restart the program by a suitable command to the processor.

LTC Switch

This switch controls the linetime clock interrupt to the LSI11 processor. In the 'ON' position the processor is interrupted every 20 milliseconds in order that a 'clock' routine may be serviced. In the 'OFF' position this interrupt is disabled.

RUN LED

This LED when illuminated indicates that the processor is executing a user program. The LED will be extinguished if the processor is in the HALT mode or if the user program fails to run.

Active LED

This is not a processor status. When illuminated it indicates that the 214SB hardware has been accessed by the processor under program control.

Power Supply LEDs

These will extinguish when the DC switch is in the 'OFF' position or if a power supply has failed.

J3.0 Rear Panel

The user information on this panel should be used in conjunction with this appendix.

Mains In

Connect the 240v/110v AC supply to this unfiltered input. (See Section J6.0).

Mains ON-OFF

This is the main AC supply switch and overload contact breaker. In a fault condition the switch will not maintain the ON position and PPL service personnel should be consulted.

Fuse

A 5 amp anti-surge fuse protects the overall S214SB system.

J4.0 Safety Aspects

The equipment has been manufactured to high safety standards and is safe under all normal conditions of use. Gresham Lion (PPL) Ltd. recommends that only trained personnel service the equipment and in every case the mains supply be disconnected before access to the unit is attempted. The USER must ensure that the equipment is connected to an adequate EARTH and a further earth strap from the chassis is recommended.

J5.0 Mounting Arrangements

The 214SB is designed to fit in a standard 19" (483 mm) rack. The overall mounting dimensions are:

width	430 mm	17 1/8"
depth	345 mm	13 5/8" (behind mounting brackets)
height	220 mm	$8\frac{3}{4}$" (5U)
weight	17.0 kg	

For ease of removal and replacement it is recommended that side mounting brackets be used to locate the unit in the rack before the front screws are inserted.

The 214SB may also be used as a free standing unit. In any situation the airflow cooling requirements are from the right hand side to the left hand side and, therefore, the user must ensure that both sides are unrestricted.

J6.0 Voltage Selection and Initial Power-Up Procedures

After removal from the packaging inspect the general condition of the equipment and contact Gresham Lion (PPL) Ltd. in the event of any damage. Remove the front panel by turning the front fasten screws $\frac{1}{4}$ turn. Ensure that all the electronic cards are firmly inserted and all cable connections are made. Switch the front panel DC switch to OFF.

At the rear of the unit ensure that the mains ON-OFF switch is off and with no mains plug connected remove the rear panel. The rear panel is removed by releasing the top rear fasteners $\frac{1}{4}$ turn and allowing the panel to hinge down.

Check that the right hand side of the main power supply (located on the hinged panel) is wired for the required supply voltage. Check that the switch to the inner top left hand corner is switched to the required supply voltage.
Refit the hinged cover and and connect a suitable cable to the mains supply socket.

Switch the MAINS switch to ON and the fan will be heard to start. Wait 30 seconds for the fan to attain full power and at the front panel turn the DC switch to 'ON'.
The voltage supply Leds will illuminate.

Turn the DC switch to the OFF position.

J7.0 Electronic Connections

Monitor Video and Computer Input Connectors

Remove the front panel and turn the DC switch to the OFF position.

From the rear of the unit feed the cables through the LHS cable channel (viewed from the front of the 214SB) and connect to the computer interface modules or S214 memory boards as required. Ensure the BNC connectors are hinged back towards the circuit board then locate the cables in the cable clips at the rear of the cable channel. Check that there is no undue slack between the circuit boards and the cable clips.

Refer to the S214 manual for details of the computer/control board interface connections.

J8.0 Maintenance

J8.1 Routine procedures

It is recommended that at suitable intervals (depending on the environment) the fan filters are cleaned and inspected as follows :

Disconnect the mains supply.

Unclip the two retaining fasteners and hinge the back panel down. Pull out the framed filter assembly from the rear LHS of the unit.

Wash the filter in luke warm soapy water, clean the plastic mesh and remove any loose particles from the fan chamber. Spin the fan and verify that the bearings are free and quiet.

Replace the dry filter assembly carefully.

J8.2 Removal of Serviceable Parts

No covers must be removed from the 214 SB unless the unit is disconnected from the mains supply.

Main Power Unit

Release the rear panel to gain access to the supply which is located on the rear panel.

Remove the cables from the left of the supply by releasing the terminal screws and remove the cable P-clip.

To the right of the supply remove the protective mains cover and release the two supply wires, the earth wire and the cable P-clip.

Undo the four corner screws and nuts being careful not to lose any washers, and remove the power unit.

Replacement is the reverse of removal. Note that on the cable loom to the left hand side of the supply the thicker white cable connects to 5V RTN and that the -12v output is not used.

Indicator and Switch Assembly

Remove the four FRONT screws of the indicator panel and lift the panel away.

Disconnect the two circuit connectors and the in-line AC neon connector.

Removal of Fan Unit

Remove the fan filter unit as described under section J8.1

Remove the six screws which hold the 214SB fan unit side panel. Remove the four SLOT HEAD screws which hold the fan mounting panel to the main chassis. Pull the base of the panel outwards and down to remove the fan assembly.

Release the fan by removing the four cross head screws and disconnecting the in line connectors and earth wire.

Refitting is the reverse of the removal.

Removal of Auxiliary Power Supply Unit

Release the rear panel and hinge the panel down. Remove the mains cover panel at the base of the unit by removing the two locating screws. Carefully remove the panel by lifting and gently pushing the panel to the right. Be sure not to bend any back plane wire wrap pins.

Remove the four external screws which hold the auxiliary power supply to the main chassis. Note the position of the cables and disconnect the wiring.

Refitting is the reverse of removal, again being sure not to damage any wire wrap pins.

J9.0 Circuit Descriptions

J9.1 Switch Panel and Display PCB 02-558

Supply Leds

The three voltage levels each drive an led via a series current limiting resistor. (D3-D5). The zener diode D1 prevents excess power being dissipated in R3.

Run Led

The processor generates a pulse at the 'RUN' output during execution of a user program. The resulting signal is a pulse stream which continually retriggers a monostable IC1. The RUN led is continually illuminated while RUN is active.

Active Led

Active is connected to the REPLY line of the 214SB signal bus, the monostable IC1 being continually retriggered while Reply is active. A single REPLY pulse will cause the ACTIVE led to illuminate for approx. 1 second.

LTC ON/OFF

A low voltageAC sinewave drives T2 via an R/C noise filter and a Schmitt 'squaring' inverter. A 4.7v zener diode limits the input voltage. When the LTC switch is in the 'ON' position T2 emitter is at 0v and BEVNTL is active every 20 mS. If the LTC switch is 'OFF' then IC2 pin 8 drives T2 emitter high (approx. 35v) which disables T2 and BEVNTL remains high. IC2 pins 8 and 10 form a debounce circuit for SW1.

CPU Enable/Halt

SW2 directly controls T1 via a debounce circuit (IC2 pin 4 and 2) which sets BHALTL high (enable) or low (halt).

J9.2 Auxiliary Power Supply (02-559)

This unit provides a low voltage AC waveform for the line time clock (pins 1 and 4) and a controlling voltage for the solid state relay RL1.

The transformer primary windings are seperate on pins T1/T2 T3/T4 to facilitate 240v/110v operation.

The low voltage is derived from a simple $\frac{1}{2}$ wave rectified supply limited to 4.7v by zener diode D2. When CNTRL (pin 5) is taken low then relay RL1 turns 'ON'.

J9.3 General Wiring Diagram 016-01-11

Fan fail and DC 'ON'/OFF

The DC on/off switch operates in conjunction with the fan fail switch in the fan assembly. When the fan is working correctly a vane in the main airflow holds a microswitch (FAN SWITCH) closed. The DC on/off switch is in series with this and when closed drives the solid state relay 'ON'. If the fan should fail the micro-switch opens and the relay turns OFF. The relay directly controls the supply to the main power unit and so controls the dc voltage levels.

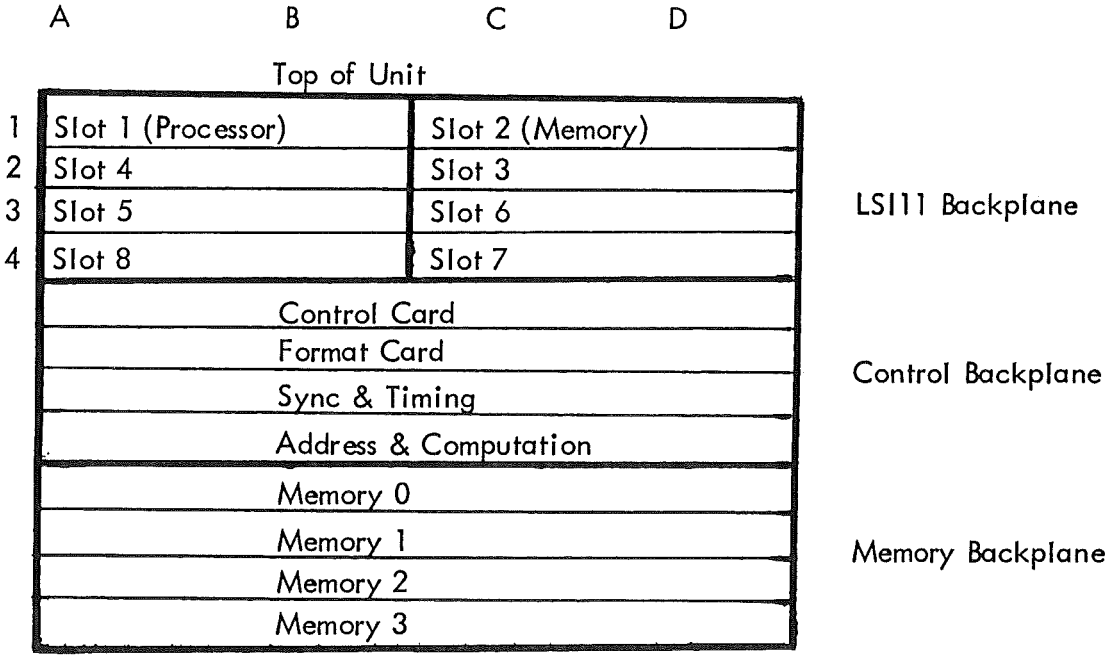
Voltage Changeover

The voltage changeover switch operates by putting the T1/T2 and T3/T4 windings of the auxiliary PSU and the fan unit in series (240v) or parallel (110v). The neon is 115v and in a 240v supply application this voltage is derived from the volt drop across a T3/T4 winding.

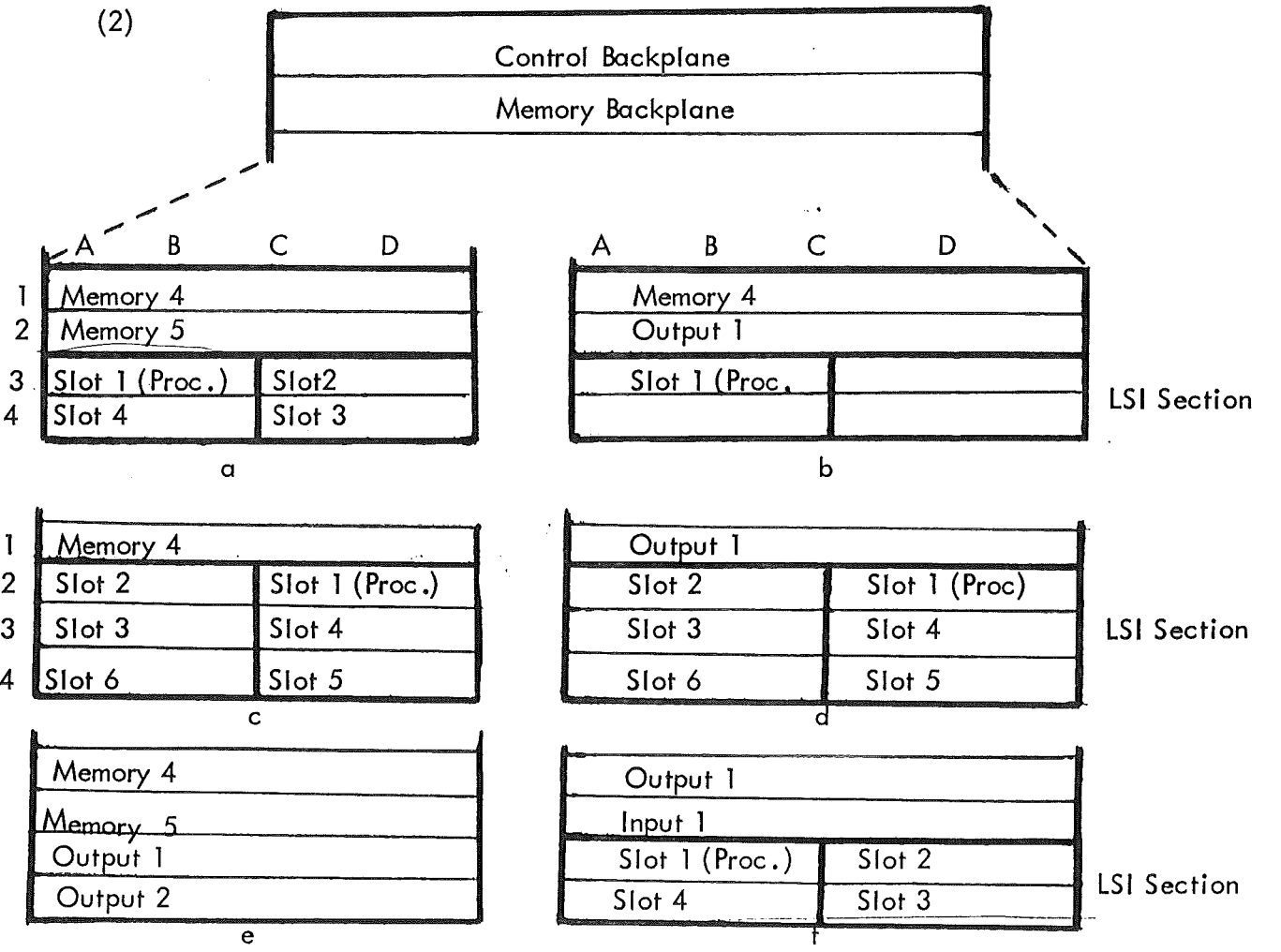
J10 Backplane Options

There are various combinations of backplanes available for 214SB as shown below.

(1)



(2)



Option 1 requires no special backplane so it uses the standard S214 system backplanes.

Options 2a - 2f use special segmented backplane assemblies in order to optimise the system card count to a customers specific requirements.

J11 Segmented Backplane Options

1. 2LSI - 2 Memory
2. 2LSI - 1 Memory - 1 Output
3. 2 Output - 2 Memory
4. 3LSI - 1 Memory
5. 3LSI - 1 Output
6. 1 Input - 1 Output - 2 Memory

where numbers refer to the backplane slots available.

Drawings called up in text

Circuit Diagrams

02-483	Internal Power Module
02-485	Address Computation
02-500	Control
02-502	Termination Resistor Networks
02-503	Indicator Panel
02-504	LSI11 Interface
02-505	PDP11 Interface
02-514	Sync and Timing
02-522	Programmable Format
02-555	Hardware Cursor
02-558	Switch Display (small box 214)
02-559	Auxiliary PSU (small box 214)
02-562	Memory

013-344	System Configuration
013-345	Image Output Board Patching
013-346	Backplane Customisation

214-07	Typical Supervisor 214, Block Diagram
07-03-14	Installation Drawing - S214
07-03-16	Installation Drawing - S214 SB12
07-03-15	Installation Drawing - Ext PSU
07-03-17	Installation Drawing - 214SB16

APPENDIX L

RTC IMAGE INPUT (ADC) CARD

L.1 General Description

The Image Input Card (IIC) is an A/D converter card for real time frame capture. It accepts a video input and digitises to either 6 bit or 8 bit resolution (dependant on type of A/D converter used).

It features black level clamping which is controlled by software. The analogue signal range to be digitised is also controlled by software.

Mixed blanking is output from this card.

L.2 Detailed Description

Figure L2.1 shows a block diagram of how an Image Input Card (IIC) is connected into a 214 system.

A video source (e.g. camera, tape recorder etc.) is fed into the IIC. This is digitised into either 8 bits or 6 bits dependant upon the type of ADC fitted. The X, Y resolution follows the 214 resolution thus programmable to all the standard resolutions.

The digitised O/Ps are fed to an Image Output Card (IOC) and the required number of RTC memory planes. Thus the line image is converted back to analogue form for viewing.

L.2.1 Board Address

Up to 4 IIC's can be incorporated. Either 4 separate monochrome video signals, can, therefore, be processed, or 3 cards used for a colour video signal.

Each card requires two address:

a. To control digitising range of ADC (lower address)
b. To control black level change (upper address).

They are read/write registers. The board address is achieved with a link field on the board. Table L.2.1 shows the addresses and the required linking.

PDP11 - LSI11 Address (Octal)	Link			Function
	D	C	B	
170120-170122	1	0	0	IIC 1
170124-170126	1	0	1	IIC 2
170130-170132	1	1	0	IIC 3
170134 -170136	1	1	1	IIC 4

0 - Link to 0V
1 - Link to 5V

Table L.2.1. Board Address Linking

L2.2 Black Level Clamp Control

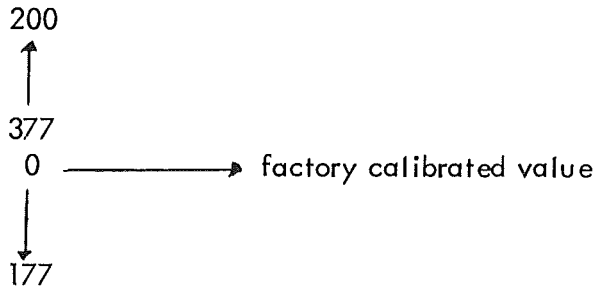
There are 2 methods for controlling the black level clamp.

a. By a potentiometer on the board.
b. By software control.

The board is calibrated at the factory for a digital value of 0 when the software value is equal to the start up value (The board is initialised on power up or by computer reset which sets the register to digital value of 0).

The scale of adjustment is as follows :-

Programmable value (octal)



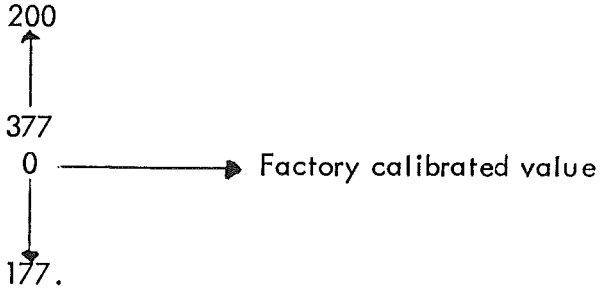
Programming is achieved by writing to the lower byte of the data of the upper address of the board (If only 1 card is fitted = 170122). Figure L.2.2 shows the configuration of the data words.

L.2.3 ADC Digitising Range Control

The board is calibrated at the factory to give maximum digital O/P for a video input voltage of 0.7V. Software control can vary the range above or below 0.7V (Camera Aperture will also affect the output level).

The scale of adjustment is as follows:

Programmable value (octal)



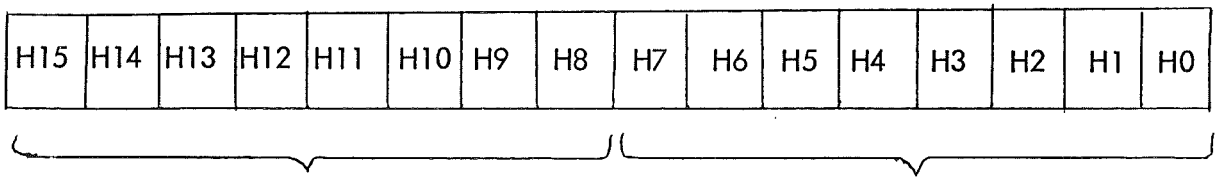
Programming is achieved by writing to the lower byte of the data of the lower address of the board (If only 1 card is fitted = 170120). Figure L.2.2 shows the configuration of the data words.

L.2.4 Reading Digital O/P of Black Level

The board is configured such that the digital value of the black level is output on the upper byte of data on either address.

Figure L.2.2 shows the configuration of the data words.

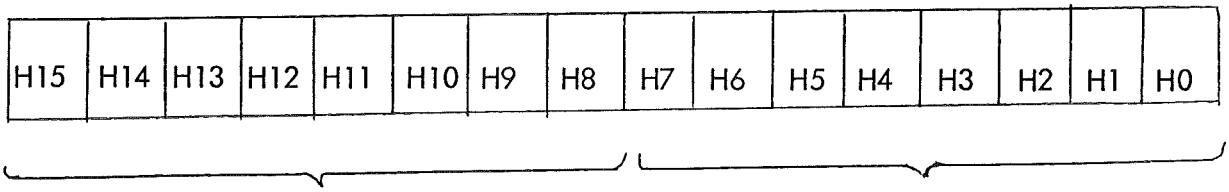
170120 (IIC 1)



Black Level Value
Read Only (ADC O/P)

Digitising Range
Read/Write

170122 (IIC 1)



Black Level Value
Read Only (ADC O/P)

Black Level Value
Read/Write

Figure L.2.2

Data Word Configuration

L.3 Circuit Description

L.3.1 Analogue Amplifier

Video in is terminated at 75 ohm. VR3 provides a gain control for the video. The signal is a.c. coupled and fed through an emitter follower amplifier. The amplifier is biased for 3V quiescant voltage.

The signal is again a.c. coupled through C16. The signal is black level clamped (at TP4, See L3.2.1 for description of black level clamp circuit).

The signal is then amplified by 3 by X5 and fed to the ADC. TR4 is a buffer amplifier to produce the required drive for the ADC.

L.3.2 Black Level Clamp Circuit

The black level can be adjusted by 2 controls :

a. VR2.
b. Computer via C4 (DAC).

VR2 is a calibration control and is adjusted in the factory to give the black level at TP5 = 0V with the O/P of C4 at the boards initialisation setting.

The digital value of the black level is clocked into flipflops (B2 and B4). These feed to the Digital-to-Analogue Converter (DAC - C4). The MSB of the flip-flop is inverted such that when 0 is programmed (this is also the initialisation value), the O/P of the DAC is halfway in its range (1.25V) and, therefore, facilitates a plus and minus control for the black level.

The O/P of C4 is fed through a buffer (X1a)as C4 has a high impedance O/P. The voltage is divided by 5 through (X1b) such that the eventual O/P has a voltage swing of $\pm$ 0.25V. X2 buffers the voltage and feeds to an analogue switch.

MXSYNC provides the control for the analogue switch via a monostable (D5a). Fig. L.3.1 shows the waveforms for black level clamping.

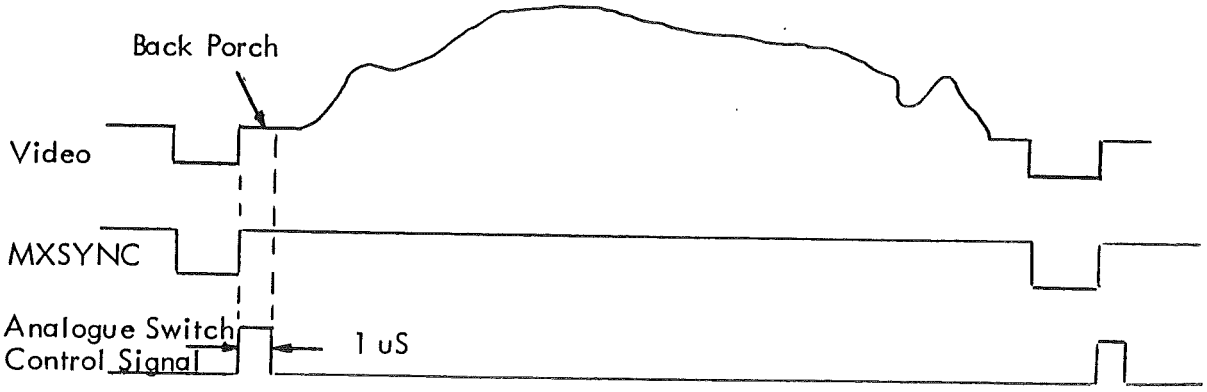


Fig. L.3.1

The back edge of MXSYNC triggers (D6a) which produces a 1 uS pulse to turn on the analogue switch

Then the switch is on C16 is charged up to the value of the black level.

L.3.3 Digitising Range Control

This controls the analogue value relating to the maximum digital output (i.e. 255 for 8 bit or 63 for 6 bit ADC's). On initialisation it is set to -1.5V. VR3 (Video I/P pot) with a calibrated signal fed in, is adjusted to give this result.

At TP3 a $\pm$ 0.5V adjustment can be made on -1.5V from the computer. As with the black level control, the computer writes to the board and the data value is stored in flip-flops (C1 and C3). This value feeds through a DAC (C2), is buffered by X4(a) and amplified by X4(b). This value feeds to the ADC.

L.3.4 Addressing and Control Circuit

Fig. L.3.3 shows a timing diagram of clocking the data into the flip-flops. The magnitude comparitor (C6) compares the address from the bus with the link field. Only bits A1-A5 are compared. AØ determines whether it is lower or upper address. The comparitor enables a monostable D2(a). WRITE clocks the mono which produces the clock pulse for the flip-flops. If AØ is not set (i.e. lower address) the Nand Gate (D3d) is enabled and C1 and C3 are clocked. If AØ is set (i.e. upper address) the Nand Gate (D3d) is enabled and B2 and B4 are clocked. Mono D2a also clocks D2b). This produces the Reply signal and ensures that the data is clocked in before it sends back reply to the computer.

L.3.5 Mixed Blank (MXBNK)

Some cameras require mixed blank and this board provides such a signal.

Frame capture requires LINE UNBLANK to be shifted by 32 pixels on the captured frame. This is unsuitable for MXBNK thus LNBNK cannot be used. A separate LUNBNK is produced on the IIC using a monostable (C7). Fig. L.3.2 shows the waveform. The width of the blanking envelopes the video sync tip and back porch.

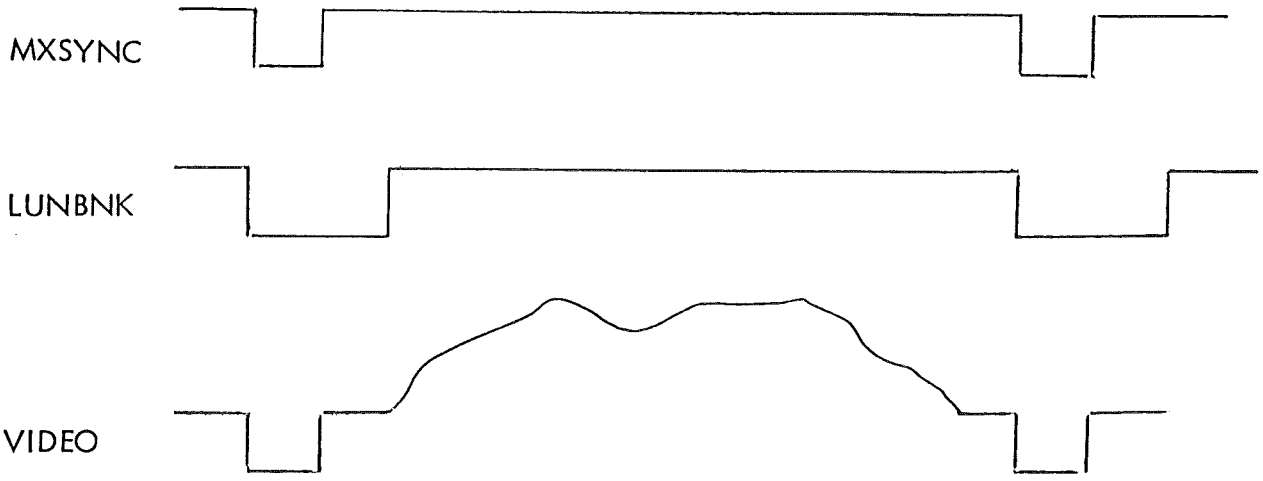


Fig. L.3.2

LUNBNK is 'ANDED' with FUNBNK. This is O/P as a 75 ohm 2V signal.

L.3.6 Calibration Signal

MXBNK is also used as a calibration signal. SW1 switches out R2 and R3 and switches in R53 and R54 to give a 75 ohm 0.7V pk-pk signal. This is fed to the video input for calibration. A video source must not be connected when the calibration signal is connected. On the board SW1 (both switches) in the the upper position turns the calibration signal on.

L.3.7 Computer Read of ADC O/P

The digital O/P of the ADC can be read by the computer. It is output on the upper byte of the data of either address. The O/Ps of the ADC are fed to a latch (B6). The data is clocked by monostable D6 (b) (TP6). The position of clocking along the line is controlled by a potentiometer (VR1). When leaving the factory it is set to read the back porch of the video signal. It cannot be adjusted with the board in situ.

L.3.8 ADC & O/P

Either an 8 bit or 6 bit ADC can be fitted. The O/P of the ADC is clocked into a latch (X10) and then fed to line drivers. The latch is needed to minimise the propogation delay of the data path.

APPENDIX M

ADDRESS COMPUTATION BOARD MKII

Contents

M1 General Description

The MKII Address Computation Board provides extra facilities that make it non-compatible with the MKI. These extra facilities are :

a. Hardware Vector Generation - this enables the generation of high speed vectors.

b. 64K RAM option - enables the use of Memory Card incorporating 64K Random Access Memories.

Two facilities have been removed, these are :

a. 4KRAM option - the MKII will no longer drive 4K RAM memory boards.

b. Double buffering of the Addressing Control Register.

All other functions of the Address Computation Board are still provided, which are :

a. To control the X and Y co-ordinates for computer access cycles.

b. To control the Y offset for the start address of Scan Cycles.

c. To provide a means of providing the required mode of operation of the Address Computation board.

M2 Detailed Description

A second generation Address Computation Board has been developed to give extra facilities to the 214. It is non-compatible with systems incorporating 4K RAM memory boards but compatible with all other systems. The extra facilities are :

1. Hardware Vector Generation. This enables vectors to be drawn much quicker than the software method. Ignoring any software overhead in the vector subroutines, the existing program VEC produces vectors at approximately 50μS per pixel. The Hardware vector speeds depend on resolution, and are as follows.

Resolution	Time per pixel uS
1024 x 512	1.33
768 x 585	1.77
512 x 512 square	1.45
512 x 512 rect.	1.0
384 x 293	1.33
256 x 256 rect.	0.89

Fig. M1

2. 64K RAM option - this enables Refresh Memory planes utilising 64K Random Access Memories (RAM). The 4K RAM option has been removed thus allowing use only with 16K and 64K Ram memory boards.

Double buffering on the Addressing Control register has also been removed.

The major function of the Address Computation board is to control the scan and access addressing of the memory boards. The board contains the X and Y access registers for the X and Y co-ordinates for access cycles, the Y offset register for the starting address for scan cycles, and the addressing control register which sets up these registers for the required mode of generation.

M2.1 Computer Addressing

There are 5 registers on the board each requiring a unique address.

i. X - Access Register
ii. Y - Access Register
iii. Y - Offset Register
iv. Addressing Control Register
v. Fractional Register.

Fig. 4.1 (See Section 4) shows the address allocation of these registers. The addressing control register and fractional register share the same address. There is decoding on board of bit 15 (MSB) of the data bus such that when : Clear, i.e. = 0 Addressing Control Register addressed.
: Set, i.e. = 1 Fractional Register addressed.

Note :- When the addressing control register is written to, the fractional register it is cleared in hardware, therefore, if fractional register is to be used it must be written to after the addressing control register.

M2.2 Addressing Control Register

This is a 6-bit register the data being transferred on the bottom 6 bits of the data highway D0-D5.

Fig. M3 shows the allocation of the bits.

D0	Y- Access register, automatic count/Fractional Count
D1	Y - Access register count direction. Set = count up; cleared = count down
D2	X - Access register, automatic count/Fractional Count
D3	X - Access Register count direction. Set = count up; cleared = count down
D4	Scan Cycle - exchange mode
D5	Maintenance Mode
D6 ↓ D14	Not Used
D15	Address Bit = 0

Fig. M3

Addressing Control Register Bit Allocation

M2.3 Access Cycle Addressing

An Access Cycle allows the computer to randomly address the Memory PCBs.

The computer sets the X and Y Cartesian co-ordinates into the X and Y access registers respectively. These are converted by the address computation logic into the bit, row and column addresses. The physical memory address is calculated from the X and Y cartesian co-ordinates according to the formula :

Mem Address = Y(HRES) + X.

Once the X and Y access registers have been loaded they are controlled by the access flags in the Addressing Control Register. The X and Y access registers are fed to counters which can be set to auto count after every access cycle. The count direction can also be selected, i.e. count up or count down from initial value.

M2.4 Scan Cycle Addressing

A Y - Offset Register is provided to set the memory address at which scanning of the visible picture begins. Unlike the access registers which accepts cartesian co-ordinates, the Y-offset register requires the actual memory address. For the formulae for calculating the required offset see section 4.2.4. Vertical scrolling can, therefore, be achieved using the Y - offset register. On interlaced systems if vertical scrolling is required by an odd number of lines the exchange bit (D4) in the Addressing Control Register must be set.

M2.5 Maintenance Mode

The purpose of the maintenance mode is to allow the computer to verify the physical memory addresses generated from the X and Y Access registers, the Y offset register and the scan counter.

For maintenance mode bit D5 in the addressing control register is set. This inhibits the normal docking of the scan counter and selection of the memory address.

A diagnostic program loads the X and Y access registers and the Y offset register with a range of values, and the resultant access or scan addresses are read by the computer to check the accuracy of the address computation circuits.

Fig. M4 shows the maintenance information that can be read by the computer. The addresses at which they are accessed are also shown. Note they are the same addresses as for normal address computation working.

Address	Normal Address Computation Mode	Maintenance Mode
170010	X Access Register	Access Row Address
170012	Y Access Register	Access Column Address
170014	Y Offset Register	Scan Row Address
170016	Addressing Control Register /Fractional Register	Scan Column Address

Fig. M4

Address Computation Board Addressing Allocation

M2.6 Hardware Vector Generation

This allows fast vectors to be drawn using hardware techniques and a small amount of initialisation from the software. Fig. M5 shows a brief flowchart of the setting up procedure of the hardware by software.

As seen in Fig. M5 the system is based around the algorithm.

1. Set I/O cycle counter = major axis, i.e. length of vector.
2. Set major axis to automatic count.
3. ACC = ACC + Fractional Register (FR).

$$\text{where FR} = \frac{\text{major axis}}{\text{major axis}} \times 16384.$$

4. When ACC + FR overflows, increment minor axis.

The FR value is calculated in software and loaded into the FR. The hardware then carries out parts 3 and 4 of the algorithm. When the vector has been completed the Supervisor 214 sets the Data Ready Flag in the Command and Status Register. This indicates that the 214 is ready for further accesses.

Using the hardware vector generator and changing the software slightly, dotted vectors can be generated. This is achieved by writing a bit pattern to the Data Register instead of 177777 as in the flowchart. This, therefore, does not give any speed penalty when writing a dotted vector, and the type of dotted pattern can be software selectable.