EMULEX MICRO DEVICES
SCSI CHIP
ESP200/100A *

FEATURES

❑ Supports ANSI X3.131 SCSI Standard
❑ Supports synchronous data transfers of 5 MB/sec
   – Programmable synchronous transfer period
   – Programmable synchronous offsets up to
      15 bytes
❑ Buffer controller interface for I/O and fast DMA
❑ Contains control logic for differential transceivers
❑ Up to 12MB/sec DMA burst transfer rate
❑ Interfaces to 8-bit microprocessor data bus with no
   support logic
❑ On-chip single-ended SCSI transceivers (48-mA
   drivers)

* ESP200 refers to ESP100A as well, except as noted.

❑ Functions as initiator or target
❑ Utilizes pipelined command structure
❑ 16-byte data FIFO between the DMA and SCSI
   channels
❑ Clock rates up to 25 MHz
❑ Low power requirements
❑ SCSI sequences implemented without microproces-
   sor intervention
   – Selection sequence from arbitration through
      command
   – Reselection sequence from arbitration
      through message
   – Bus-initiated selection through received
      command
   – Command complete sequences
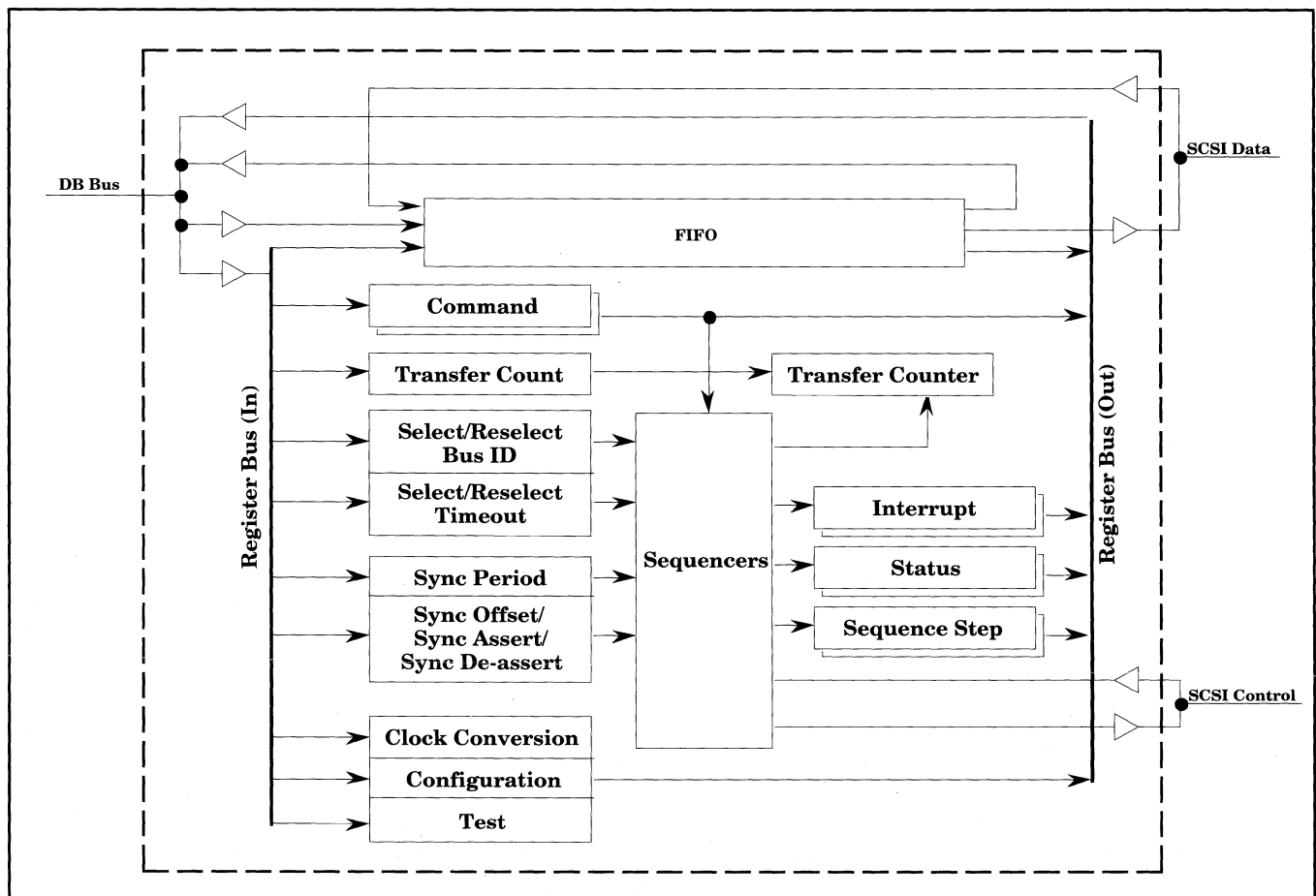   – Terminate and disconnect sequences

Figure 1. ESP200 Block Diagram
Mode 2/3

❏ Microprocessor interrupted only when service is required
- Disconnect or bus reset
- Selection/reselection sequence complete
- Target Mode command complete or ATN detected
- Initiator Mode complete or phase change detected

PRODUCT DESCRIPTION

The Emulex SCSI Processor (ESP200) chip is a VLSI device which implements the detailed protocol of the SCSI Bus Standard. The ESP200 chip operates in both the Initiator and Target modes and can therefore be used in both host adapter and peripheral application. The chip performs such functions as bus arbitration, selection of a target, or reselection of an initiator. The ESP200 handles message, command, status and data transfers between the SCSI Bus and its internal FIFO or a buffer memory. Figure 1 shows the internal architecture of the ESP200. The chip maximizes protocol efficiency by utilizing a first-in, first-out command pipeline and combination commands to minimize host intervention.

The ESP200 has been optimized for interaction with the controller processor. Common SCSI bus sequences that would typically require significant amounts of processing and interaction have been reduced to single commands. The commands are listed in Table 1.

SYSTEM ORGANIZATION

The ESP200 chip provides a controller with a complete SCSI interface. The other major chips in the circuit include the Emulex Merged Architecture Controller (MAC) and a microprocessor.

The MAC chip controls data movement in and out of the buffer memory. It supports up to four DMA channels with a total throughput rate up to 4MB/sec and provides format control for a wide spectrum of 14-, -8, 5.25-, and 3.5-inch disk drives.

The 8031 microprocessor coordinates the interaction of the VLSI devices on the board. It also implements high level SCSI protocol, such as the message system, SCSI pointers, and command set.

Sequence	Description
Selection	Arbitration, target selection, transmission of an optional one-byte message followed by a multiple-byte command.
Reselection	Arbitration, initiator reselection, and transmission of a one-byte message.
Bus-Initiated Selection	Transmission of selection bus ID, a 1-byte Identify or null message, a 2-byte Queue Tag Message (if SCSI-2 mode), followed by Command Phase bytes.
Bus-Initiated Reselection	Reselection detection and receipt of a one-byte message.
Target Command Complete	Transmission of a status byte and a one-byte message.
Target Disconnect Sequence	Transmission of two one-byte messages followed by discon- nection from SCSI bus.
Initiator Command Complete	Receipt of a status byte and one-byte message.

Table 1. ESP200 Single SCSI Commands

REGISTERS

The ESP200 registers are used to configure, command, monitor and pass data to the chip. These registers are shown in Figure 2. The Command Register is an 8-bit read/write register used to give commands to the ESP200. The register is double ranked, enabling the microprocessor to stack one level of command to the ESP200.

INTERFACES

The ESP200 has two separate interfaces: the buffer data bus and the SCSI Bus. The buffer data interface is used for strobe, DMA request, DMA acknowledge and microprocessor interrupt signals. For DMA operations, the buffer controller manages access timing and generates all buffer memory addresses.

The SCSI Bus signals have separate input and output pins. All are 8-bit busses. The SCSI interface can be configured for operation in either single-ended or
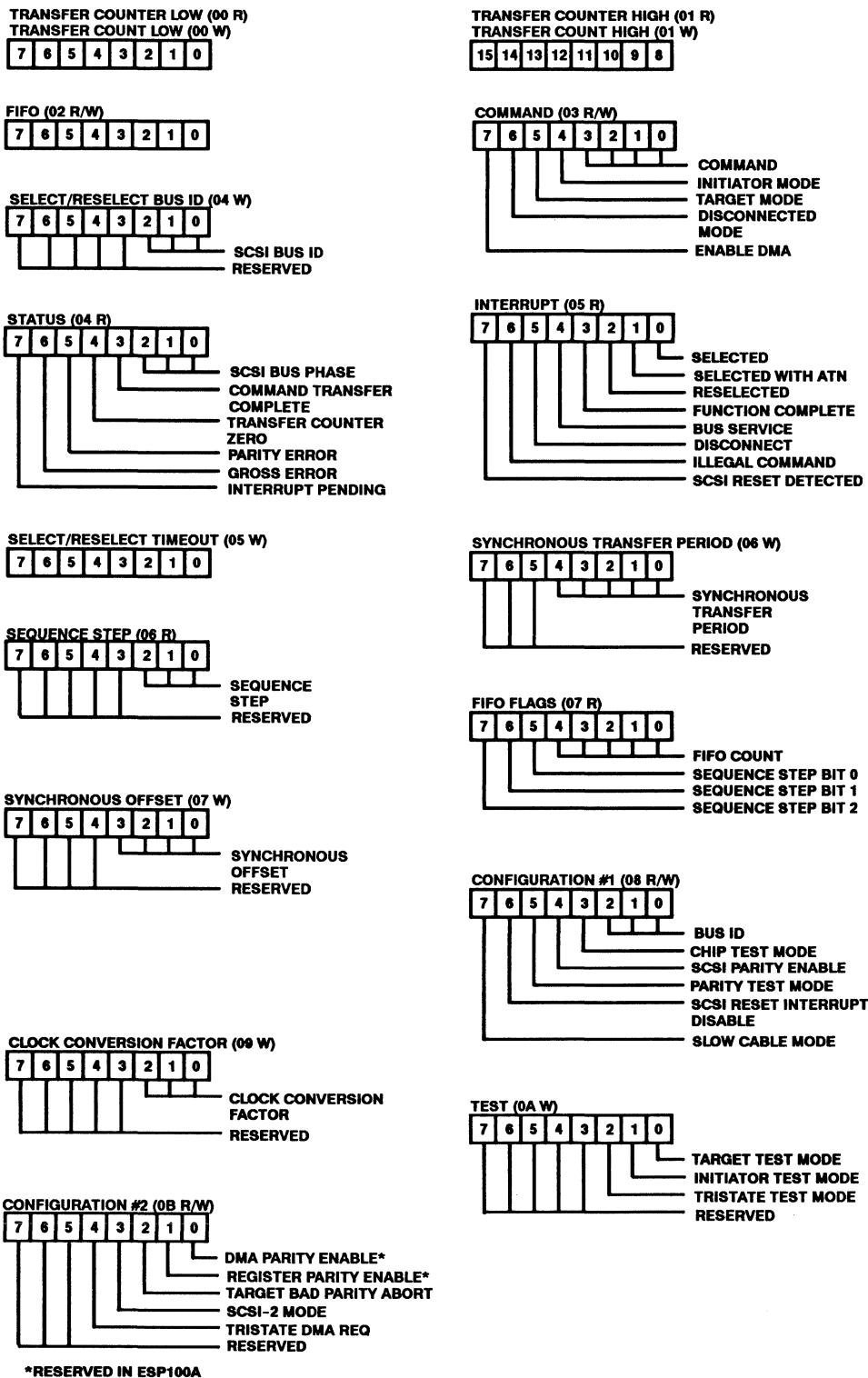
TRANSFER COUNTER LOW (00 R)
TRANSFER COUNT LOW (00 W)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

FIFO (02 R/W)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

SELECT/RESELECT BUS ID (04 W)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
- SCSI BUS ID
- RESERVED

STATUS (04 R)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
- SCSI BUS PHASE
- COMMAND TRANSFER COMPLETE
- TRANSFER COUNTER ZERO
- PARITY ERROR
- GROSS ERROR
- INTERRUPT PENDING

SELECT/RESELECT TIMEOUT (05 W)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

SEQUENCE STEP (06 R)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
- SEQUENCE STEP
- RESERVED

SYNCHRONOUS OFFSET (07 W)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
- SYNCHRONOUS OFFSET
- RESERVED

CLOCK CONVERSION FACTOR (09 W)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
- CLOCK CONVERSION FACTOR
- RESERVED

CONFIGURATION #2 (0B R/W)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
- DMA PARITY ENABLE*
- REGISTER PARITY ENABLE*
- TARGET BAD PARITY ABORT
- SCSI-2 MODE
- TRISTATE DMA REQ
- RESERVED

*RESERVED IN ESP100A

TRANSFER COUNTER HIGH (01 R)
TRANSFER COUNT HIGH (01 W)

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |

COMMAND (03 R/W)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
- COMMAND
- INITIATOR MODE
- TARGET MODE
- DISCONNECTED MODE
- ENABLE DMA

INTERRUPT (05 R)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
- SELECTED
- SELECTED WITH ATN
- RESELECTED
- FUNCTION COMPLETE
- BUS SERVICE
- DISCONNECT
- ILLEGAL COMMAND
- SCSI RESET DETECTED

SYNCHRONOUS TRANSFER PERIOD (06 W)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
- SYNCHRONOUS TRANSFER PERIOD
- RESERVED

FIFO FLAGS (07 R)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
- FIFO COUNT
- SEQUENCE STEP BIT 0
- SEQUENCE STEP BIT 1
- SEQUENCE STEP BIT 2

CONFIGURATION #1 (08 R/W)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
- BUS ID
- CHIP TEST MODE
- SCSI PARITY ENABLE
- PARITY TEST MODE
- SCSI RESET INTERRUPT DISABLE
- SLOW CABLE MODE

TEST (0A W)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
- TARGET TEST MODE
- INITIATOR TEST MODE
- TRISTATE TEST MODE
- RESERVED

Figure 2. ESP200 Register Summary

differential mode. In the single-ended mode, the SDI/SDO lines interface directly with the SCSI Bus. In differential mode, the SDI bus becomes bidirectional and the SDO bus controls the direction of the external differential transceivers. Figure 3 shows the functional signal grouping of the ESP200.
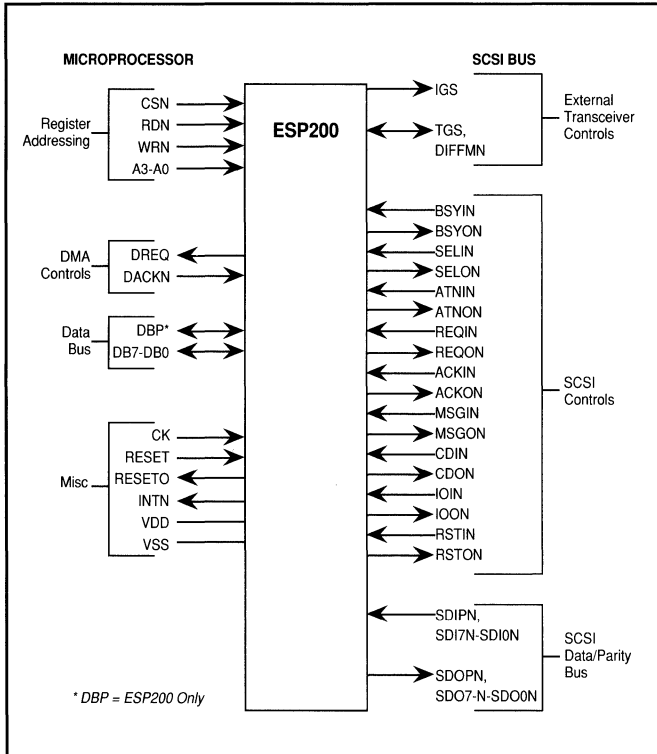

Figure 3. Functional Signal Grouping

PIN DESCRIPTIONS

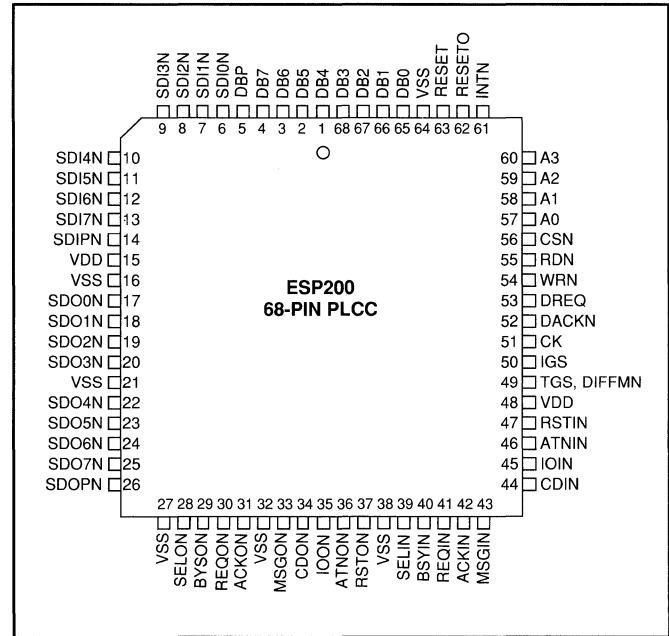Figures 4 and 5 illustrate the ESP200 pins for both the PLCC 68-pin and the PQFP 80-pin models, together with the signal names associated with each pin.

Figure 4. ESP200 68-pin PLCC Pin Diagram
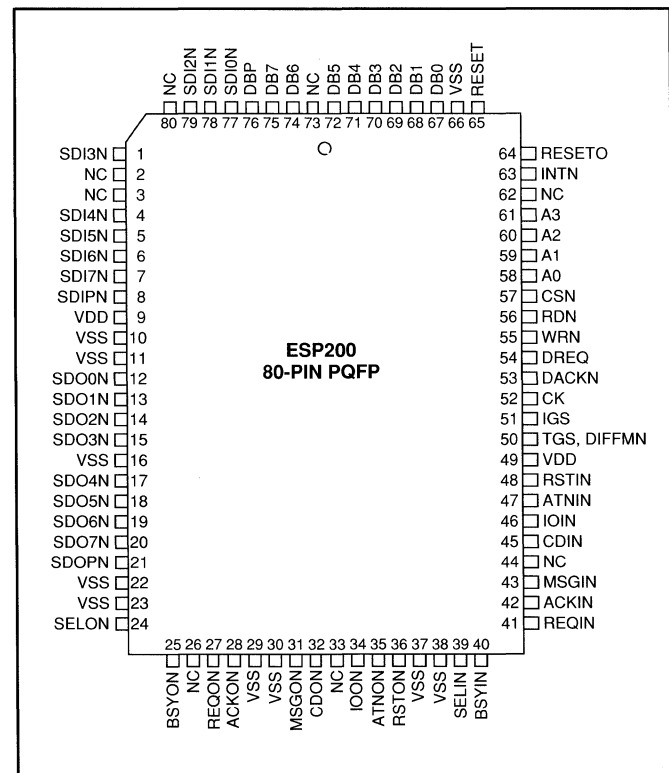
Figure 5. ESP200 80-pin PQFP Pin Diagram

AC TIMING

The following figures and table values are illustrative of the ESP200 chip timing characteristics. For more information, see the ESP200/100A Application Manual, VLSI51002-00.
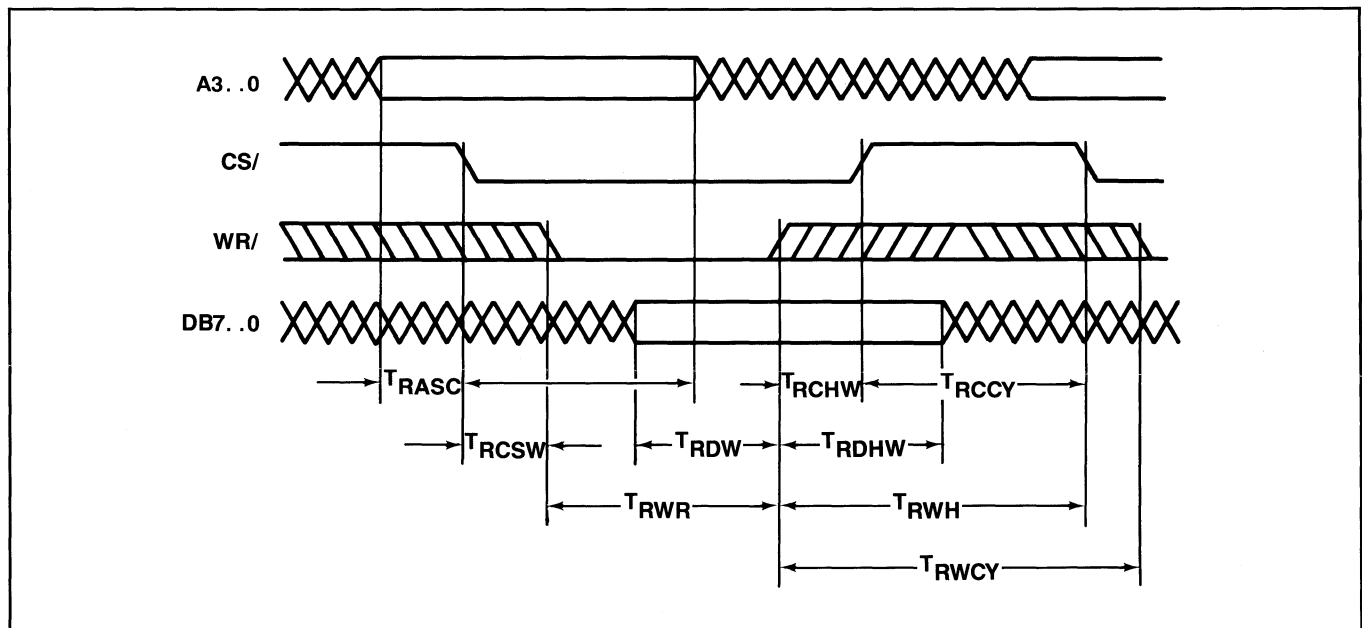
REGISTER INTERFACE

Register Write (in ns)

For the following register write operations, note that ACK/ must be inactive during all register I/O, and CS/ must make a high to low transition to capture a new register address. Reserved registers should not be accessed.

Symbol	Description	Minimum	Maximum
TRASC	Address Setup to CS/	0	
TRCSW [1]	CS/ Setup to WR/	0	
TRWR	WR/ Pulse Width	40	
TRDW	Data Setup to WR/	11	
TRAHC	Address Hold from CS/	50	
TRDHW	Data Hold from WR/	0	
TRCHW [1,2]	WR/ High to CS/ High	0/50	
TRWCY	WR/ High to WR/ Low	60	
TRWH	WR/ High to CS/ Low	60	
TRCCY [1]	CS/ High to CS/ Low	40	

Notes:

1. WR/ edges may precede or follow CS/ edges. Recommended values are TRCSW ≥ 0 and TRCHW ≥ 0, unless Note 2. below applies. If WR/ is held low, the data setup to CS/ high is 25ns minimum, the data hold from CS/ high is 60ns minimum, and TRCCY is 60ns minimum.
2. ESP200 only: TRCHW must be ≥ 50ns if writing to the FIFO register and the DMA Parity Enable bit does not equal the Register Parity Enable bit (Configuration #2 Register bits 0,1). Under this condition, WR/ cannot be held low.

Figure 6. Register Write

Register Read (in ns)

For the following register read operations, note that ACK/ must be inactive during all register I/O, and CS/ must make a high to low transition to capture a new register address. Reserved registers should not be accessed.

Symbol	Description	Minimum	Maximum
TRASC	Address Setup to CS/	0	
TRCSR [1]	CS/ Setup to RD/	20	
TRRD	RD/ Pulse Width	50	
TRDR [2]	RD/ to Data		50
TRDC [2]	CS/ to Data		70
TRAHC	Address Hold from CS/	50	
TRDHR	Data Release Time	2	40
TRCHR [1]	RD/ High to CS/ High	2	
TRRCY	CS/ High to CS/ Low	40	

Notes:

1. RD/ edges may precede or follow CS/ edges. Recommended values are TRCSR > TRDC - TRDR, and TRCHR > TRDHR. If RD/ is held low, the time from CS/ low to stable data is TRDC, and the data release time from CS/ high is TRDHR.
2. TRDC and TRDR must both be satisfied.
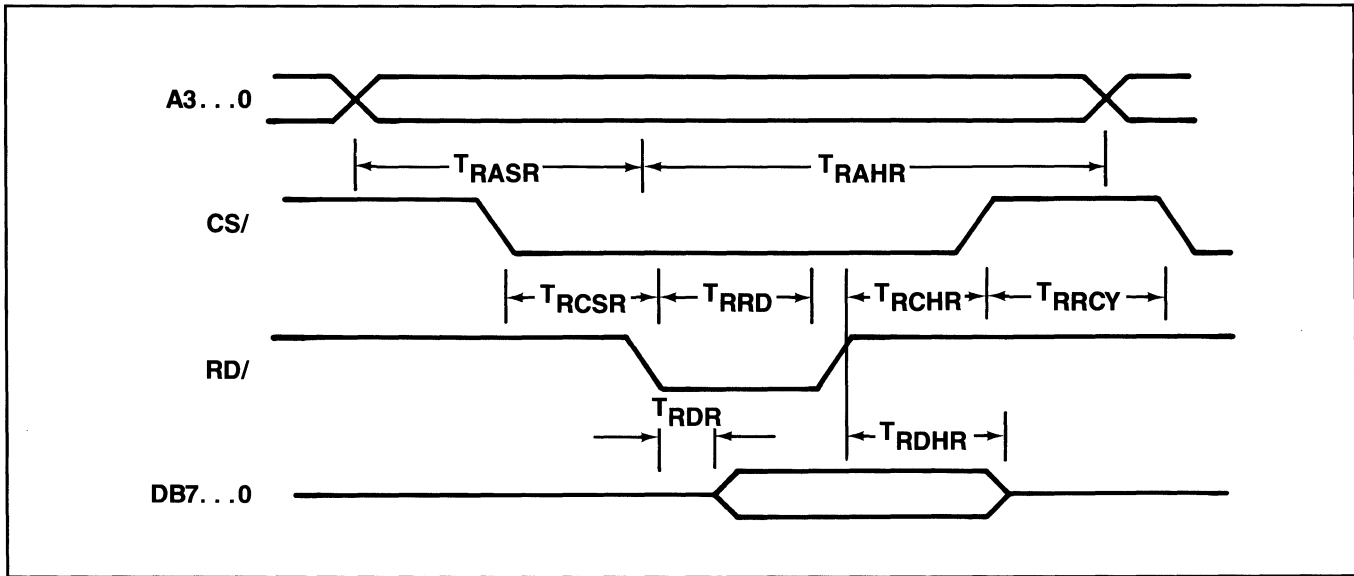
Figure 7. Register Read

DMA INTERFACE
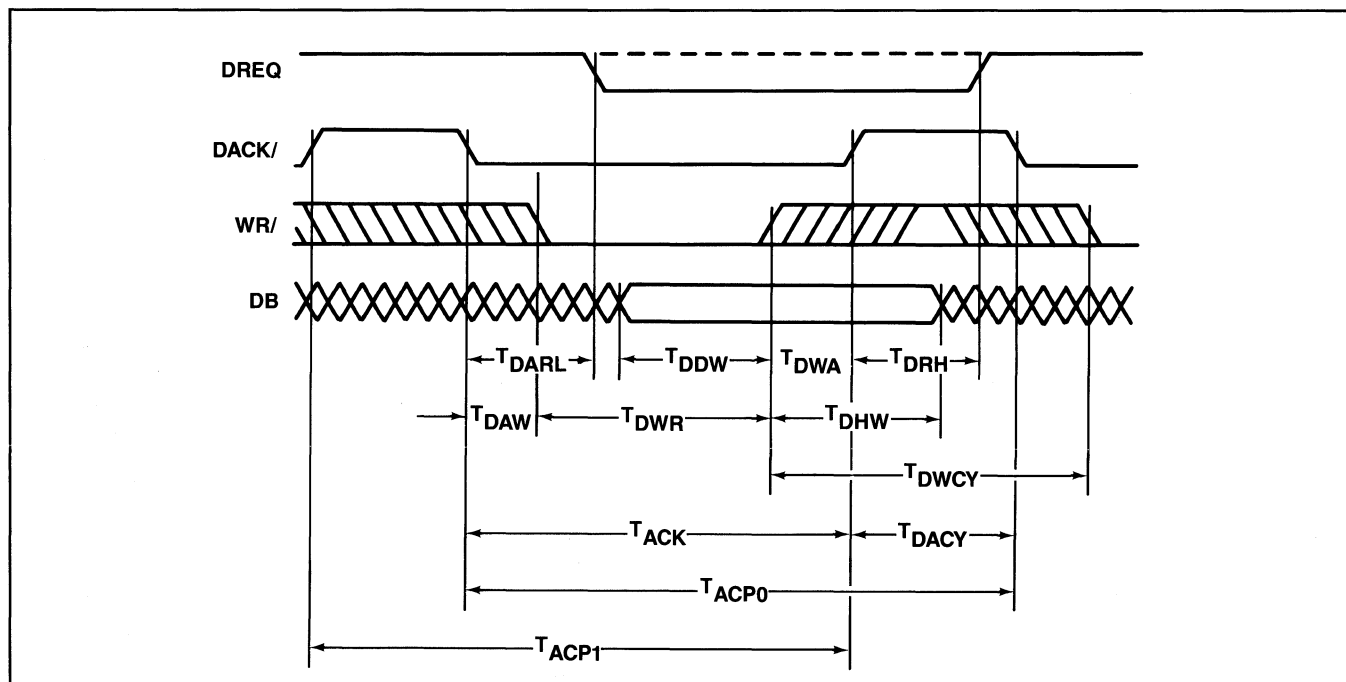
DMA Write (in ns)

For the following DMA write operations, note that CS/ must be inactive during all DMA accesses, and DACK/ must toggle once for each write access. DREQ remains active as long as the FIFO is not full and the Transfer Counter is not zero.

Symbol	Description	Minimum	Maximum
TDARL	DACK/ Low to DREQ Low (negation pending)	0	38
TDAW [1]	DACK/ Low to WR/ Low	0	
TDWR	WR/ Pulse Width	40	
TDDW	Data Setup to WR/	11	
TDWA [1]	WR/ High to DACK/ High	0	
TDHW	Data Hold from WR/	0	
TDACY [1]	DACK/ High to DACK/ Low	12	
TDRH	DACK/ High to DREQ High (assertion pending)		50
TDWCY	WR/ High to WR/ Low	40	
TACK	DACK/ Pulse Width	50	
TACP0	DACK/ Period (Low to High)(sync SCSI transfer)	83.33	
TACP1	DACK/ Period (High to High)	TCS + 35ns -TDACY and 2TCP	

Notes:

1. WR/ edges may precede or follow DACK/ edges. Recommended values are TDAW $\geq$ 0 and TDWA $\geq$ 0. If WR/ is held low, the data setup to DACK/ high is 15ns minimum, the data hold from DACK/ high is 15ns minimum, and TDACY is 40ns minimum.

Figure 8. DMA Write

DMA Read (in ns)

For the following DMA read operations, note that CS/ must be inactive during all DMA accesses, and DACK/ must toggle once for each read access. DREQ remains active as long as the FIFO has data to be read and the Transfer Counter is not zero.

Symbol	Description	Minimum	Maximum
TDARL	DACK/ Low to DREQ Low (negation pending)		38
TDAR [1]	DACK/ Low to RD/ Low	0	
TDRD	RD/ Pulse Width	TDDR	
TDDR [2]	RD/ to Data		41
TDRA [1]	RD/ High to DACK/ High	0	
TDHR	Data Release Time	2	40
TDACY	DACK/ High to DACK/ Low	12	
TDRH	DACK/ High to DREQ High (assertion pending)		50
TDDAL [1]	DACK/ Low to Data		41
TDDAH	Previous DACK/ High to Data		60
TACK	DACK/ Pulse Width	50	
TACP0	DACK/ Period (Low to Low)	83.33	
TACP1	DACK/ Period (High to High)(sync SCSI transfer)	TCS + 35ns -TDACY and 2TCP	

Notes:

1. RD/ edges may precede or follow DACK/ edges. Recommended values are TDAR $\geq$ 0, and TDRA $\geq$ 0. If RD/ is held low, the time from DACK/ low to stable data is TDDAL, and the data release time is TDHR.
2. TDDR, TDDAL, and TDDAH must all be satisfied.
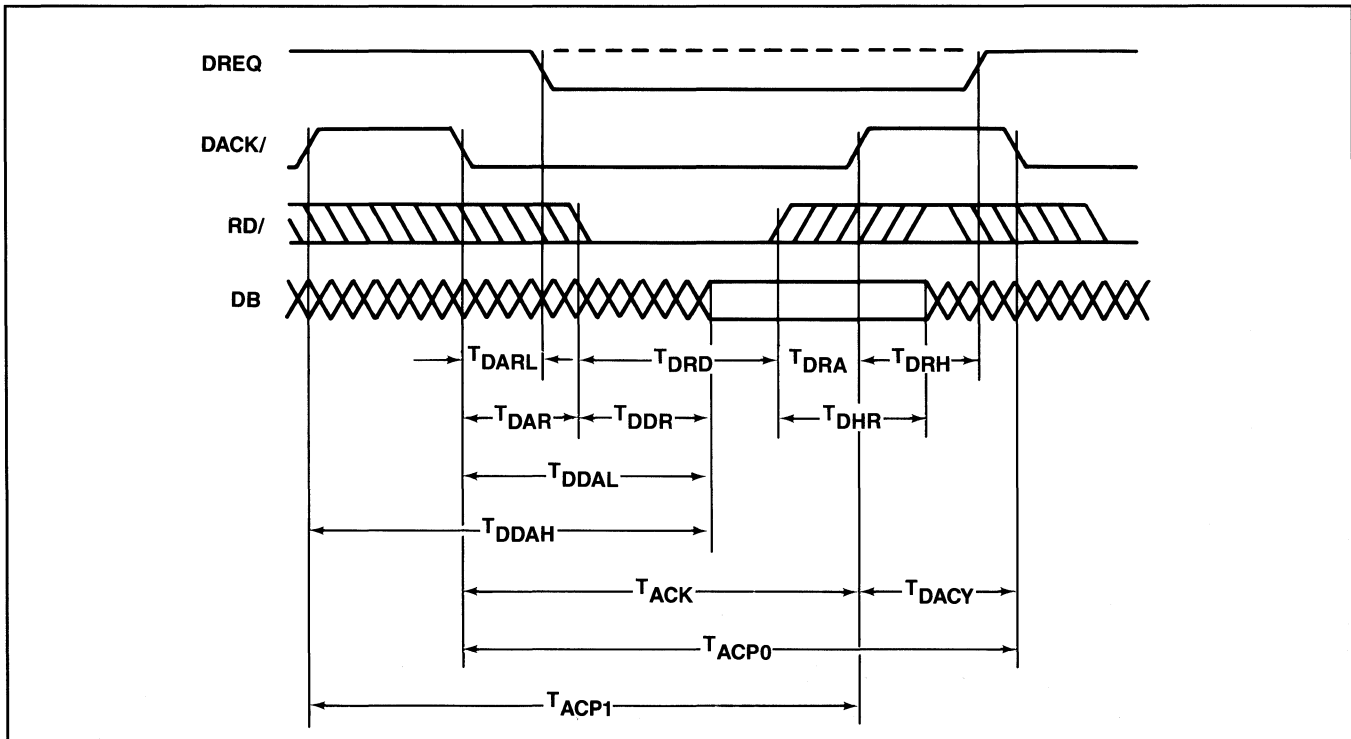
Figure 9. DMA Read

SCSI INTERFACE

Target Asynchronous Data In Phase (in ns)

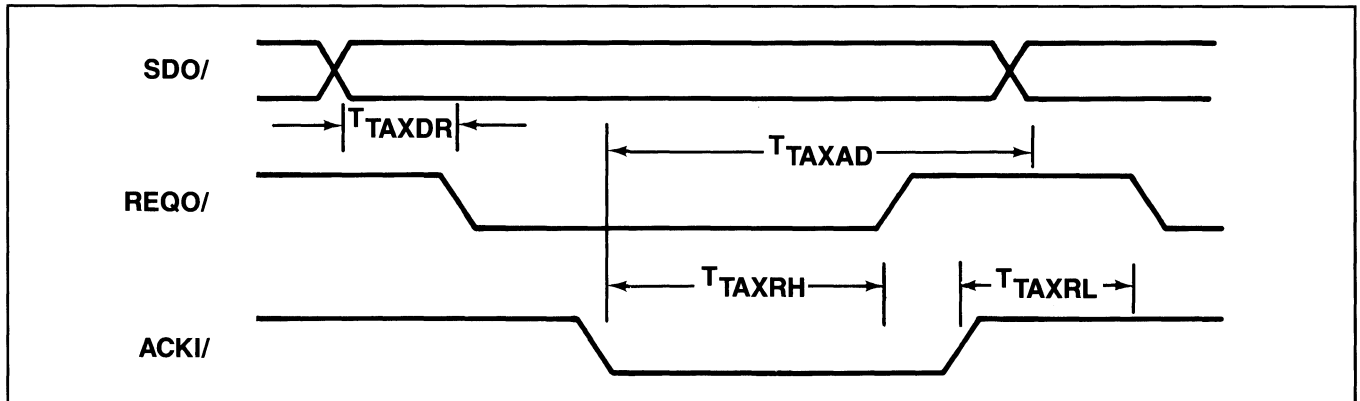| Symbol	Description	Minimum	Maximum
TTAXDR	Data to REQO/	55	
TTAXRH	ACKI/ Low to REQO/ High		25
TTAXAD	ACKI/ Low to Data (FIFO bottom full)		40
TTAXRL	ACKI/ High to REQO/ Low (data already set up)		25

Figure 10. Target Asynchronous Data In Phase

Target Asynchronous Data Out Phase (in ns)

Symbol	Description	Minimum	Maximum
TTARRH	ACKI/ Low to REQO/ High		25
TTARRL	ACKI/ High to REQO/ Low (FIFO not full)		25
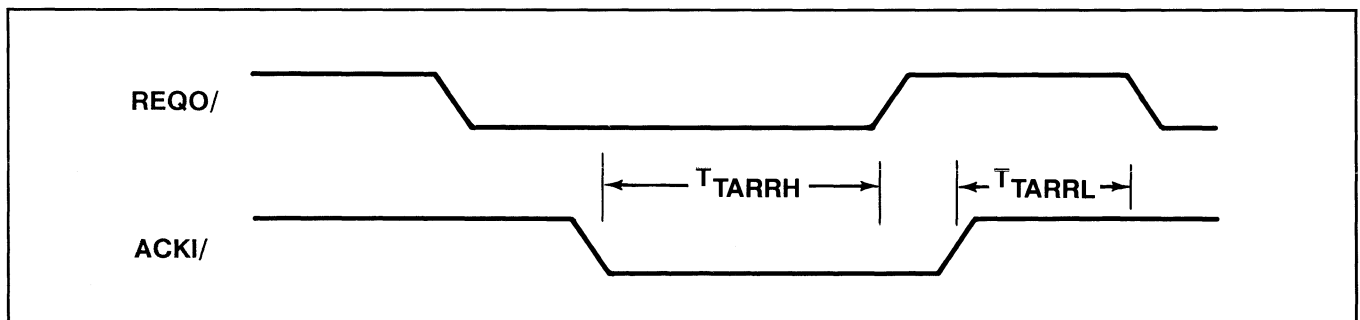
Figure 11. Target Asynchronous Data Out Phase

Initiator Asynchronous Data In Phase (in ns)

Symbol	Description	Minimum	Maximum
TIARAH	REQI/ High to ACKO/ High		25
TIARAL	REQI/ Low to ACKO/ Low (FIFO not full)		25
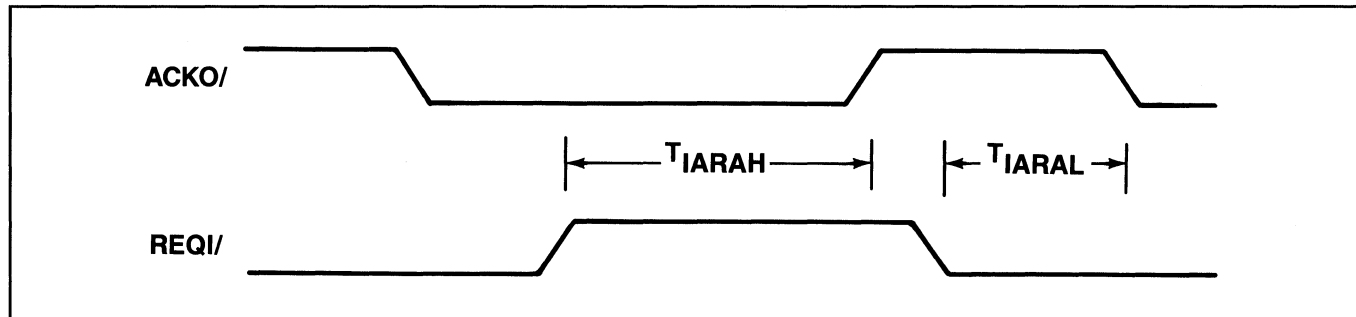
Figure 12. Initiator Asynchronous Data In Phase

Initiator Asynchronous Data Out Phase (in ns)

Symbol	Description	Minimum	Maximum
TIAXDA	Data to ACKO/	55	
TIAXAH	REQI/ High to ACKO/ High		25
TIAXRD	REQI/ High to Data (FIFO bottom full)		40
TIAXAL	REQI/ Low to ACKO/ Low (data already set up)		25
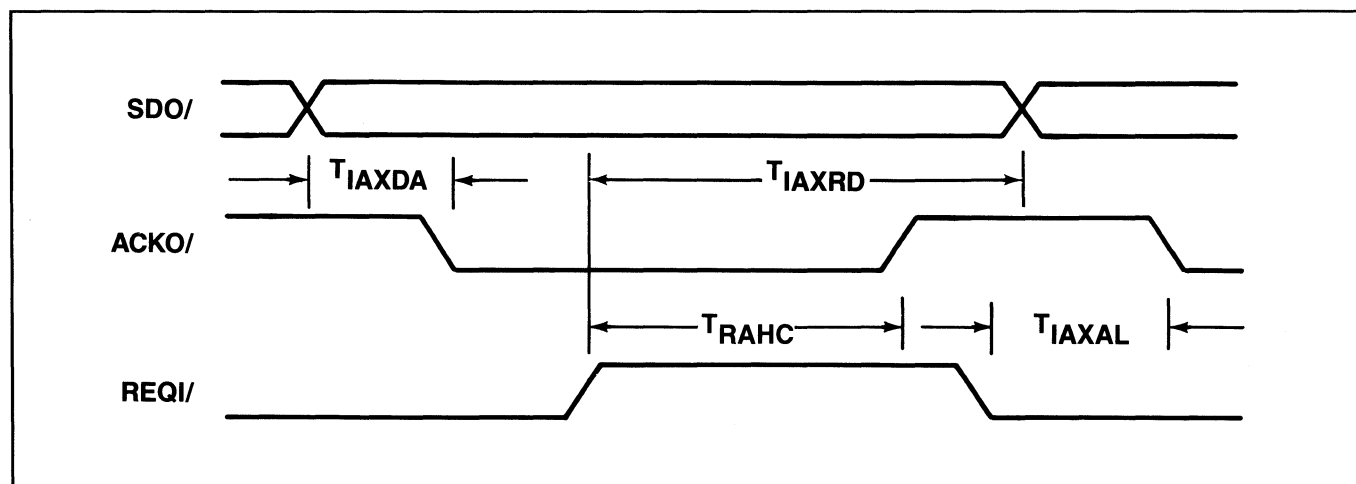
Figure 13. Initiator Asynchronous Data Out Phase

Synchronous Transfer (in ns)

Symbol	Description	Minimum	Maximum
TSXD	Data from CK High		40
TSXDR	Data to REQO/ Low	55	
TSXDA	Data to ACKO/ Low	55	
TSXRL	REQO/ Low from CK High		35
TSXRH	REQO/ High from CK Low		35
TSXAL	ACKO/ Low from CK High		35
TSXAH	ACKO/ High from CK Low		35
TSAST	Assertion Period	90	
TSNEG	Negation Period	90	
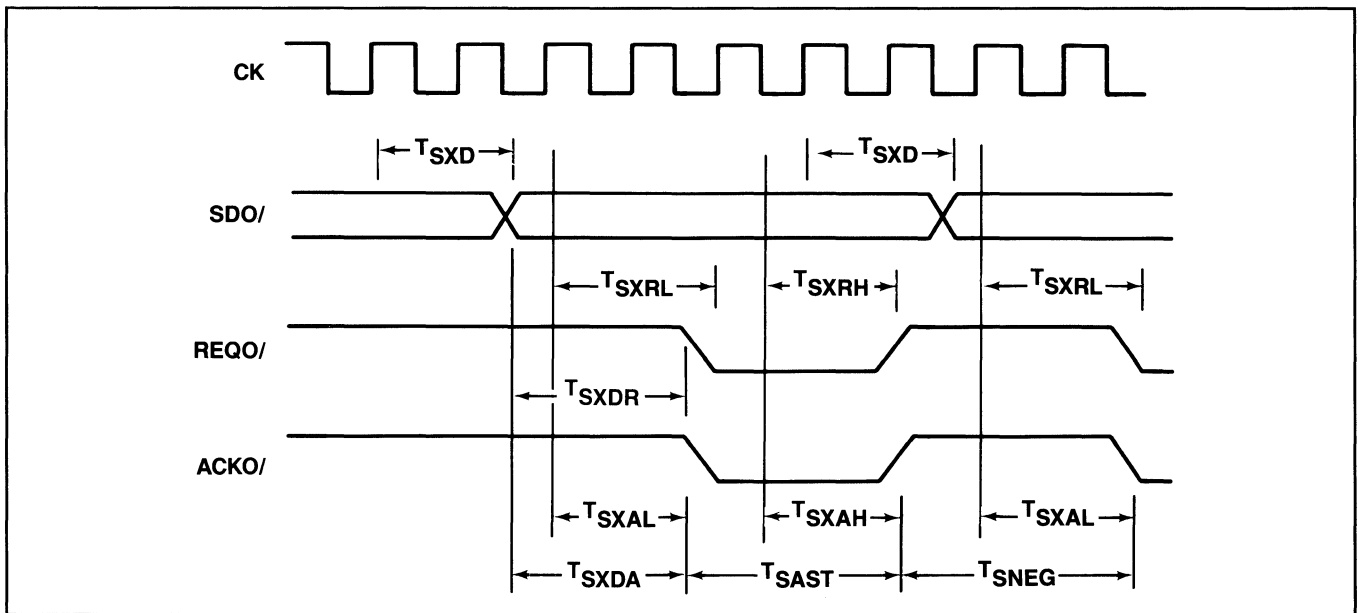
Figure 14. Synchronous Transfer