CHAPTER 3
OPTION
(PRINCIPLES OF OPERATIONS)

3.1 Microcassette

The microcassette tape is controlled by the 6303 slave CPU. The unit requires a comparatively large power supply because of the mechanical functions it performs. It is powered only when used. Fig. 3-1 is a block diagram illustrating signal flow to and from the microcassette.

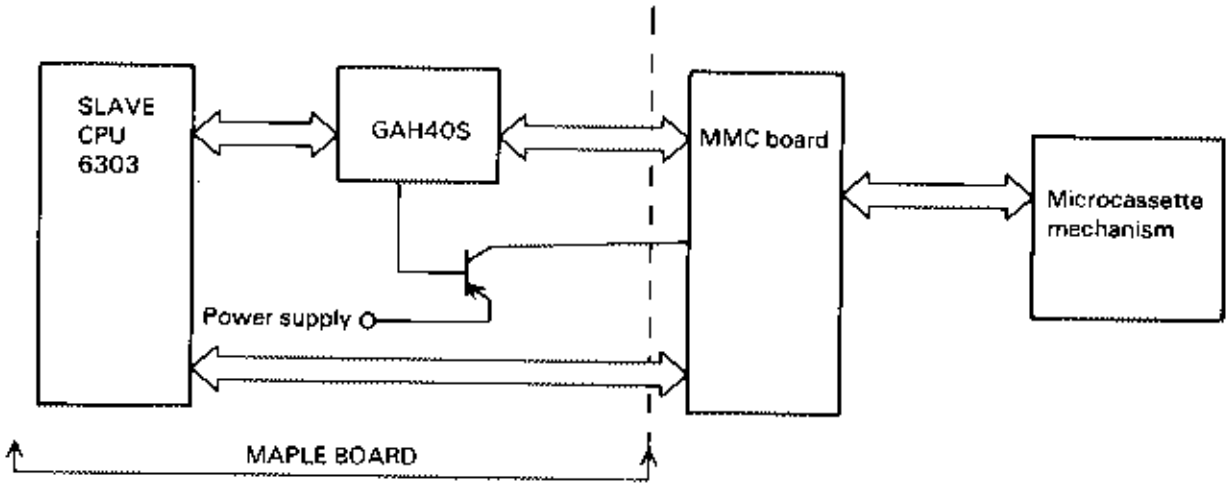


Fig. 3-1 Microcassette Tape Operation Control Block Diagram

3.1.1 Slave CPU Functions

The 6303 slave CPU directly controls all microcassette tape operations using the following signals:

HSW: Indicates the current position of the read/write head (LOAD/ UNLOAD).
WE: Indicates whether the microcassette is write-enabled.
(detects the presence of the microcassette write inhibit tab).
ERAH: Erase signal.
HMT: Head pinch motor drive signal.
D: Write data.

3.1.2 Gate Array Functions

The gate array issues or accepts the following signals under the control of the slave CPU:

MTA – MTC: Capstan motor drive control signal
CNTR: Tape count detection signal (photo-reflector detection signal)
RDMC: Read data
SWMC: MMC board and mechanism operation power control signal

3.1.3 Microcassette Tape Data Format

Data are recorded on a microcassette tape in blocks of 256 bytes and all cassette tapes are accessed in blocks. Fig. 3-2 illustrates the structure of a data block.

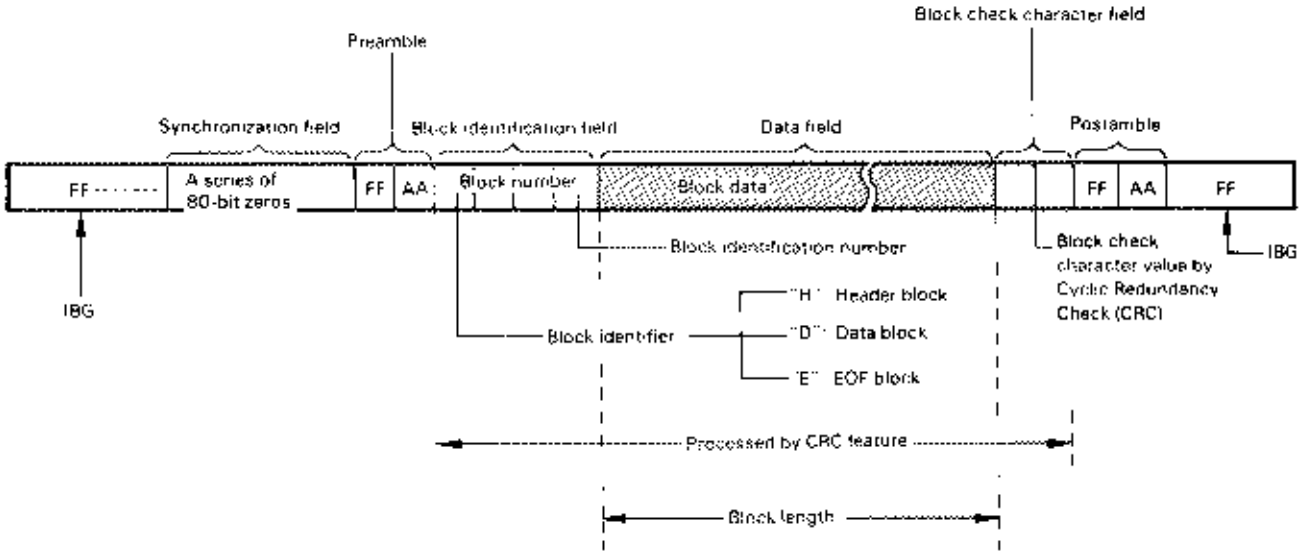


Fig. 3-2 Microcassette Tape Data Format

One tape reel (or one tape volume) consists of a directory and one or more files. The directory consists of three blocks; the first block contains identification data for the tape and directory and the second and third blocks contain control data for the files.

One file consists of a header block, one or more data blocks, and an end-of-file (EOF) block. Fig. 3-3 illustrates the general data structure of one reel.

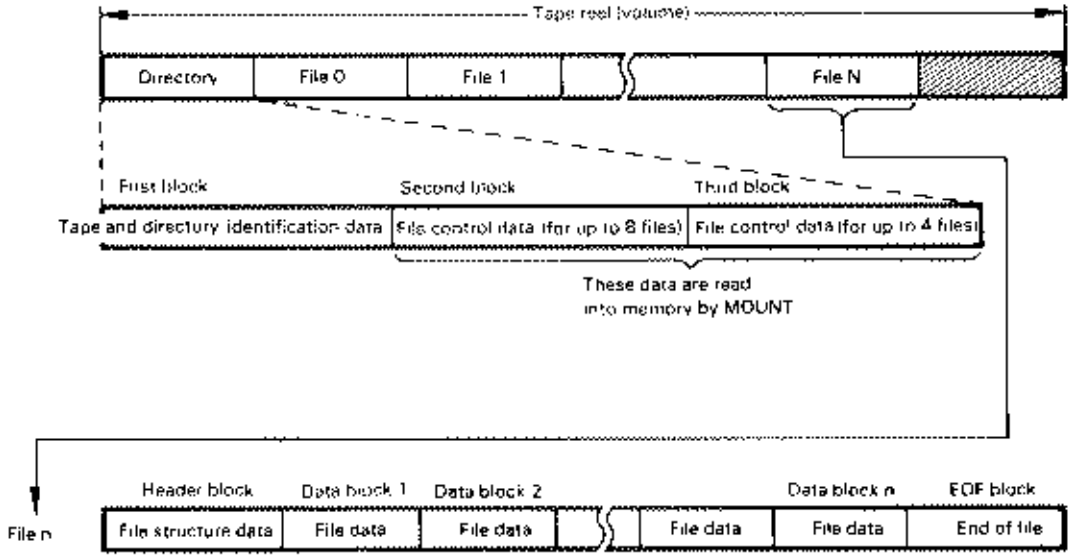


Fig. 3-3 Cassette Tape Reel Structure

3.1.4 Outline of Microcassette Mechanism

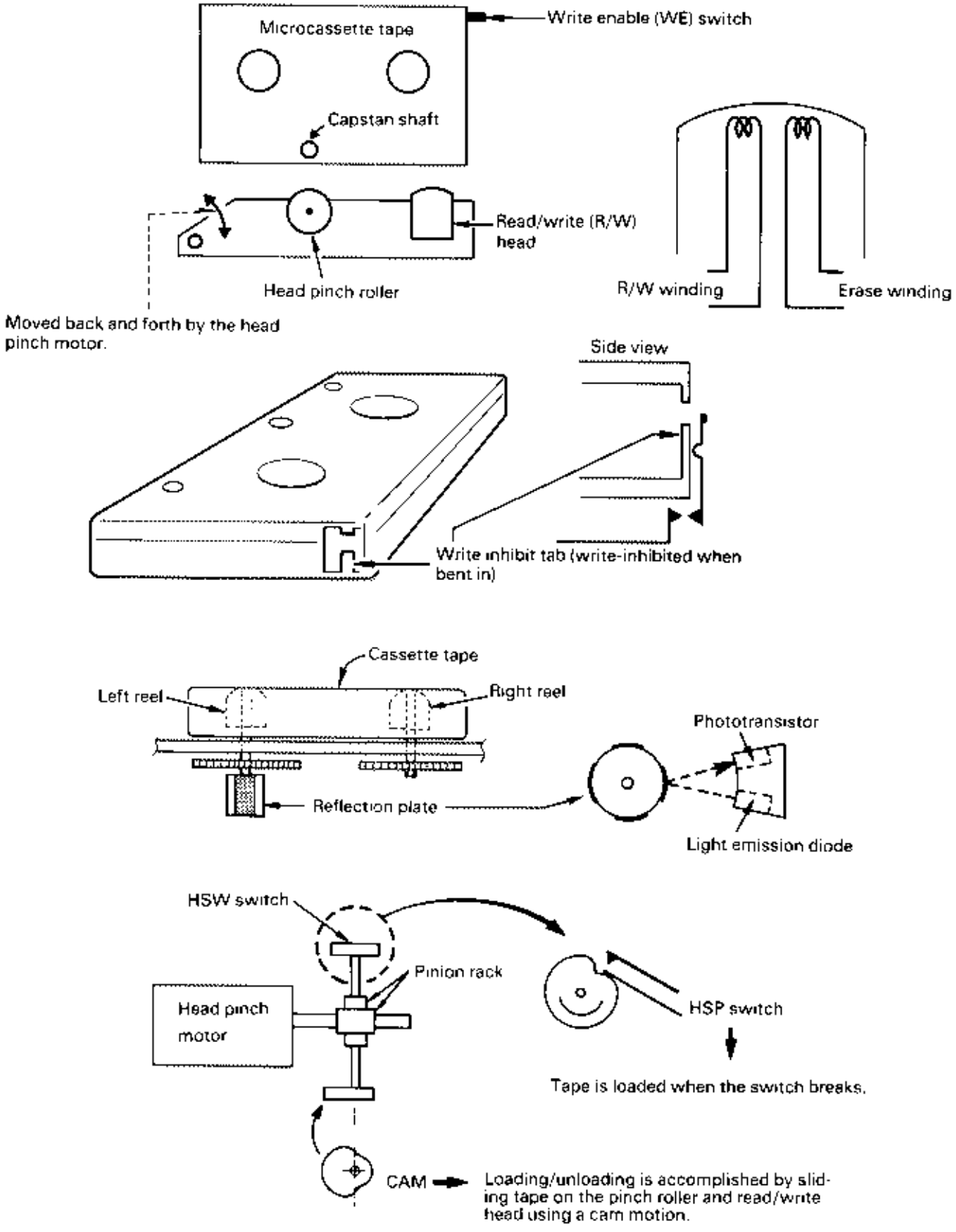


Fig. 3-4

3.1.5 MMC Board

The MMC board consists of two major sections, the motor drive control and read/write, which provide the following functions:

3.1.5.1 Motor Control Section

The motor control section occupies the upper half of the MMC board and controls the capstan motor and head pinch motor drive, and tape count detection. The individual circuits are discussed in the following:

(1) Capstan motor drive circuit

This circuit uses two ICs: IC1 and IC2. IC1 controls motor drive circuit switching and IC2 controls motor revolution speed.

● Motor drive circuit

Fig. 3-5 shows the internal circuit of IC1.

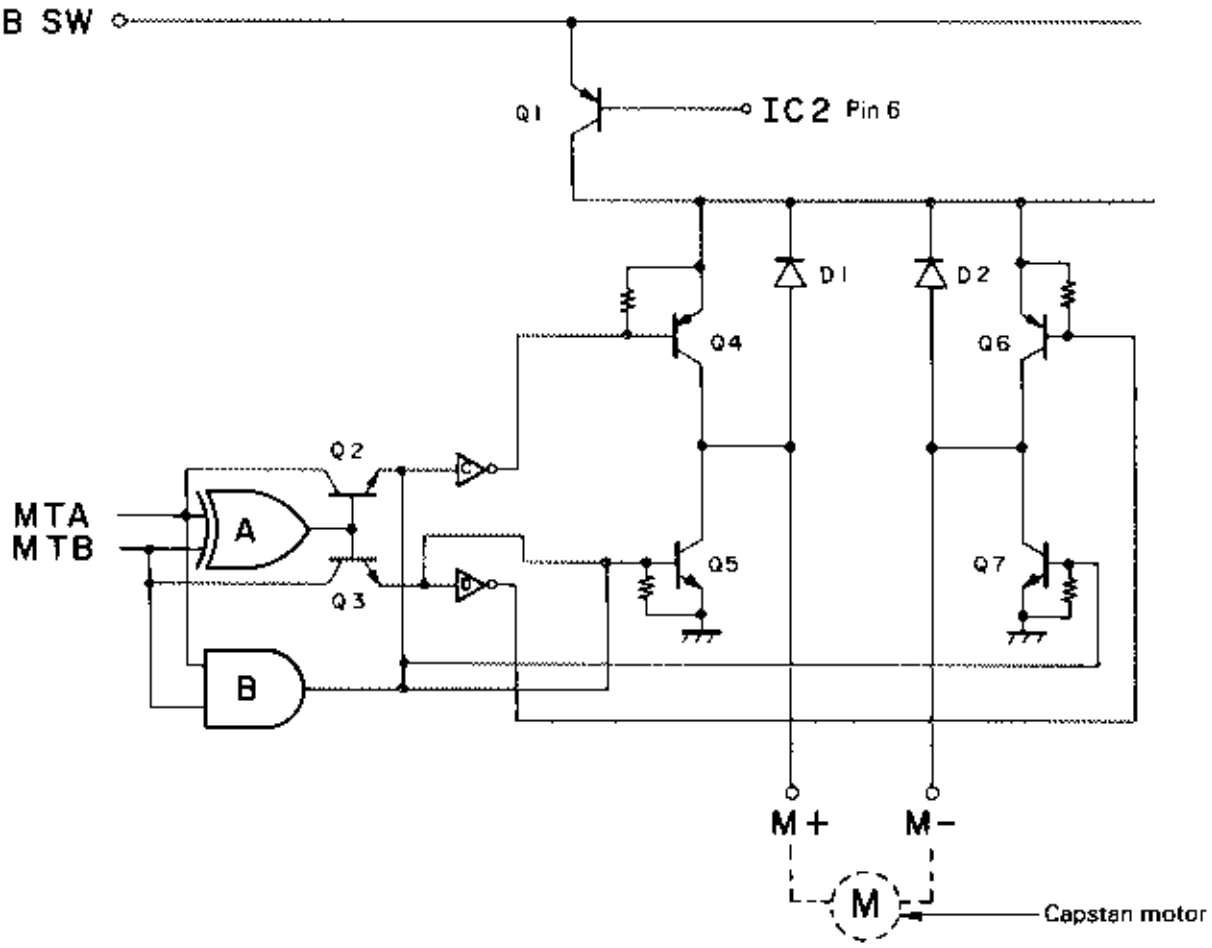


Fig. 3-5 Motor Drive IC Circuit

The circuit switches the polarity of the voltage applied to the capstan motor. Simplified circuit descriptions follow. While the actual circuit operation is more complicated, the basic operation is the same.

Table 3-1 Cassette Tape Operation Truth Table

Operation	MTC	MTB	MTA	Erase Head	Head Position
READ (Replay)	0	0	1	0	Load
WRITE (REC)	0	0	1	1	Load
REWIND (FAST)	1	1	0	0	Unload
REWIND (SLOW)	0	1	0	0	Unload
F.F. (FAST)	1	0	1	0	Unload
F.F. (SLOW)	0	0	1	0	Unload

MTA = High, MTB = Low

Since both the signals are supplied to the exclusive OR gate A, the base of the transistors Q2 and Q3 are held high, maintaining them in conduction. This causes the emitter of Q2 to be held high which in turn maintains transistor Q7 in conduction, holding the M- terminal of the capstan motor at ground level. The low signal inverted by inverter C turns transistor Q4 on which drives the external transistor Q1, supplying the VBSW voltage to the M+ terminal of the capstan motor. This results in a forward capstan motor drive which winds the tape. (The motor control transistors Q4 and A7 are in conduction.)

MTA = Low, MTB = High

Both Q2 and Q3 are in conduction similare to the above phase. However, the high level at the collector of Q3 maintains the transistor in conduction this time, causing the the M+ terminal of the capstan motor to be held at ground level. The low signal inverted by inverter D turns transistor Q6 and supplies the VBSW voltage to the M– terminal. This results in a backward capstan motor drive, which rewinds the tape. (The motor control transistors, Q5 and Q6, are in conduction.)

MTA = High, MTB = High

When both the signals are high, the low output of the exclusive OR gate A cuts off transistors Q2 and Q3, and no effective control signal can be output at the emitter of either transistor, but the high level output of AND gate B maintains transistors Q5 and Q7 in conduction, holding both the M+ and M– terminals of the capstan motor at ground level. (The motor control transistors Q5 and Q7 are in conduction.)

MTA = Low, MTB = Low

Both the outputs of the exclusive OR gate A and the AND gate B are low; no control signal is available. All the motor control transistors, Q4 through Q7, are cut off, leaving the capstan motor in a floating state.

The external transistor Q1 is controlled by the output at pin 6 of IC2 (a speed control signal). Thus, the VBSW voltage may not be supplied to the capstan motor if either Q4 or Q6 is in conduction.

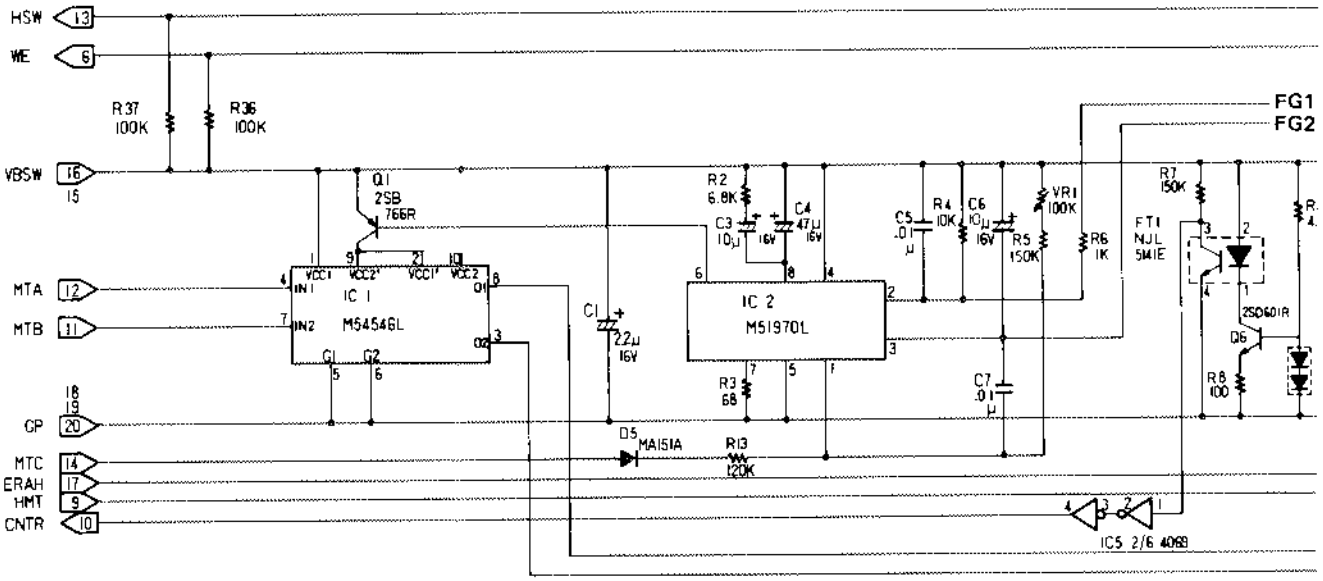


Fig. 3-6

3.1.5.2 Motor Revolution Speed Control Circuit

This circuit controls revolution of the capstan motor to ensure a cassette tape feed at a constant speed. Tape must be read/written at a speed of 2.4 cm/s. To secure this tape speed, the capstan motor must revolve at 2,400 rpm.

Because no tape speed control is desired during fast forward feed or rewind, a function which can enable or disable the tape speed control is also required. Fig. 3-7 is a block diagram of the internal circuit of IC2.

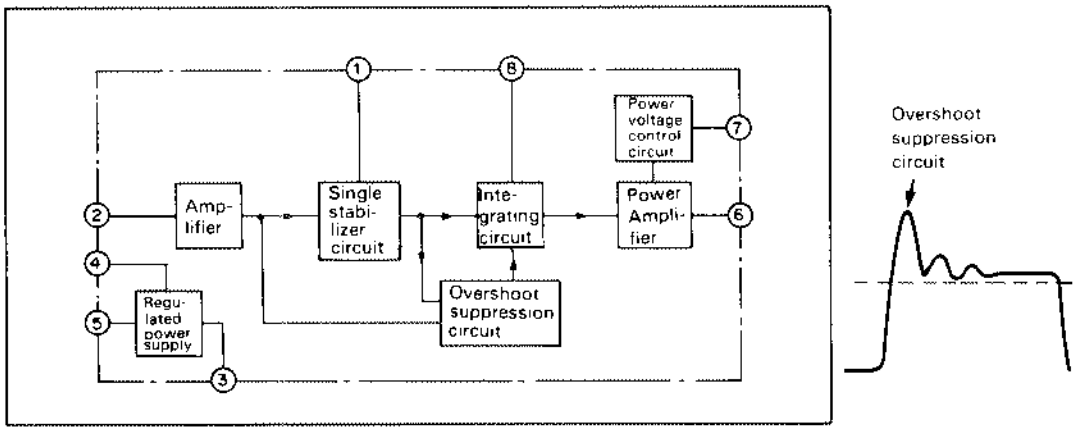


Fig. 3-7 IC2 Internal Circuit Block Diagram

The principle of the motor speed control can be illustrated by Fig. 3-8.

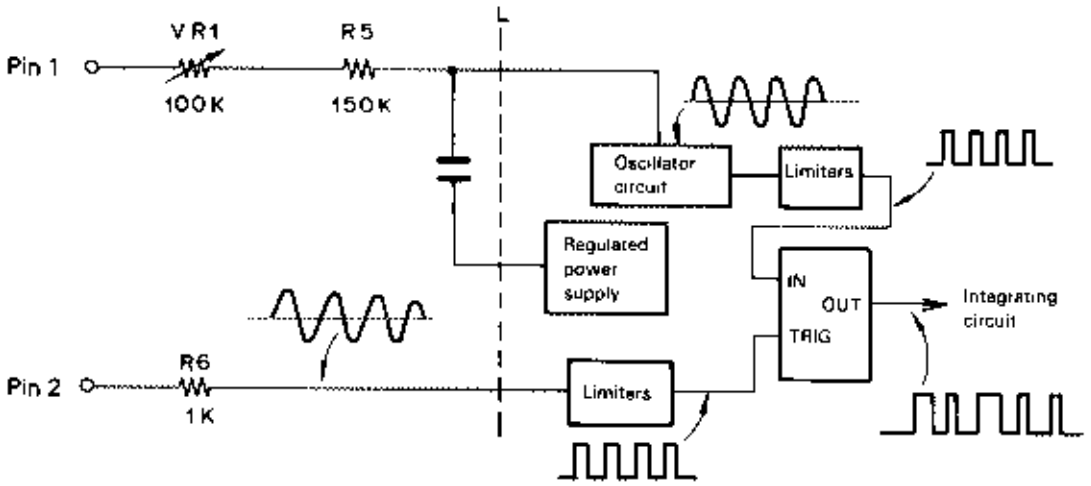


Fig. 3-8 Motor Speed Control Circuitry

Integrating Circuit

The IC output is a pulse signal as shown in Fig. 3-9. However, the capstan motor cannot be controlled by a pulse signal as the motor would oscillate. The IC output is integrated by the next stage integrating circuit, which uses the external capacitors C3 and C4. The pulse delay time (t) is determined by the capacitance of C4.

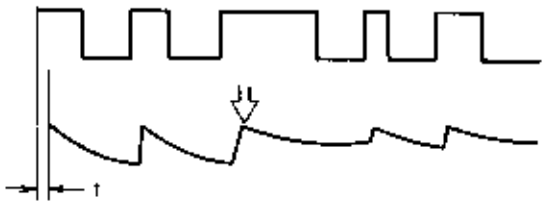


Fig. 3-9 Integrating Circuit

Current Control

The output current from the integrating circuit is amplified and the amplified current is limited to a proper value by the external resistor R3. Fig. 3-10 conceptually illustrates the principle.

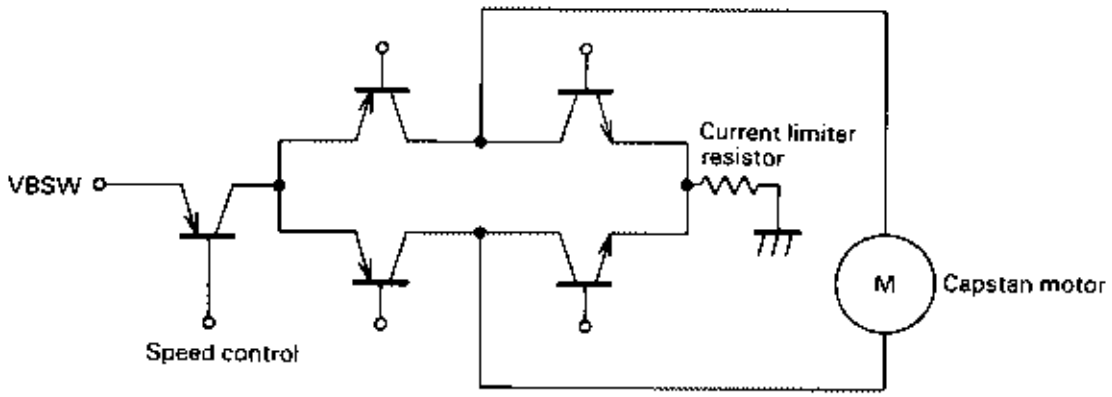


Fig. 3-10

3.1.5.3 Power Supply

Because IC 2 requires a negative voltage supply, pin 5 is grounded and pin 4 is connected to the VBSW voltage.

Input – Monostable Circuit

Motor speed control is accomplished by comparing the time constant determined by VR1, R5, and C7 with the frequency fed back from the capstan motor tachogenerator. The relationship between the time constant and the rpm of the capstan motor is as follows:

$$NP = \frac{1}{1.17Rx\,C7}$$

$$2400 \cdot 10 = \frac{1}{1.17Rx \cdot 0.01}$$

$$Rx = \frac{24 \times 10^3}{1.17 \times 0.01} \quad \text{..... Approximately 205 k}\Omega$$

where N: rpm of capstan motor – 2,400 rpm
P: Number of tachogenerator poles – 10
Rx: Total resistance of VR1 and R5 (kohms)
C7: 0.01 uF (pF)

The specified speed should be attained by adjusting VR1 nearly at the center. The optimum frequency output from the tachogenerator, 400 Hz, is deviced as follows:

$$\frac{2{,}400 \text{ rpm}}{60} \times 10 \text{ (poles)} = 400 \text{ Hz}$$

3.1.6 Mechanism Control

3.1.6.1 Tape Count Detection

Tape count detection is accomplished by mirrors directly coupled to the left reel (the reel taking up tape during read/write) and a photo-reflector assembly (a single element which is a combination of a light emission diode and a phototransistor). Fig. 3-11 shows the circuit and the positional relationship between the elements.

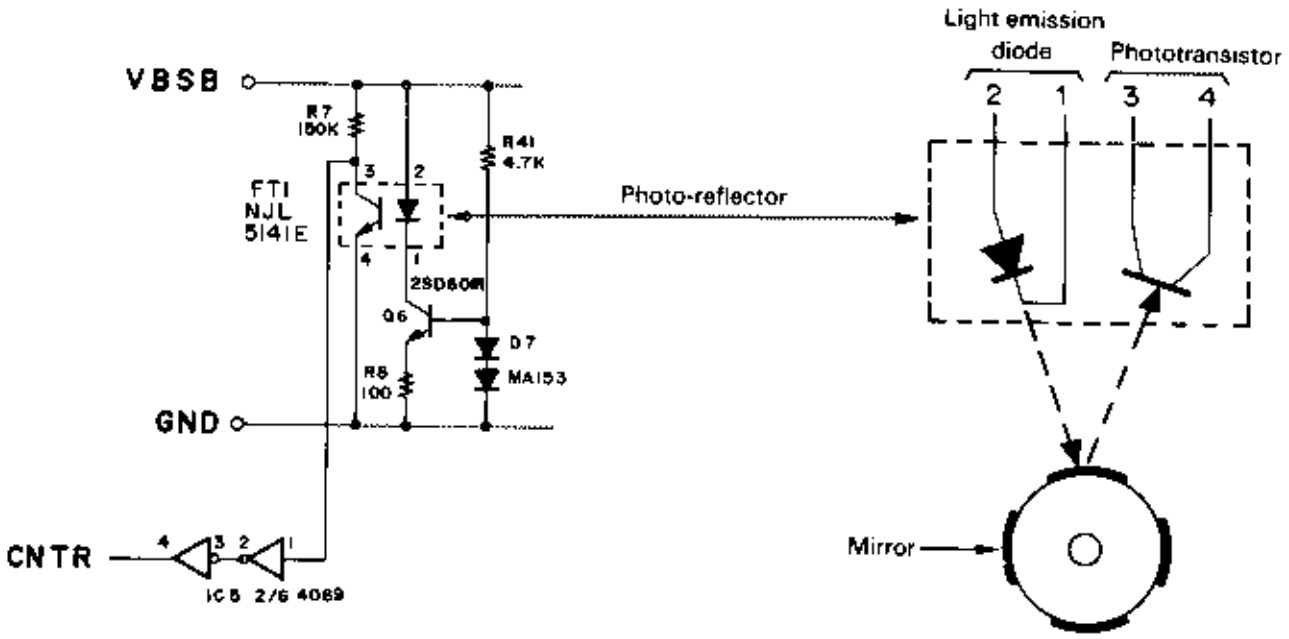


Fig. 3-11 Tape Count Detector Circuit and Positional Relationship between Elements

The reflector drum has four mirrors on it as shown in Fig. 3-11. One reel revolution is counted as four.

3.1.6.2 Head Pinch Motor Control

The head pinch motor moves the P-lever assembly consisting of the pinch roller and the read/write head. The assembly slides back and forth to accomplish tape loading and unloading. This motor always revolves in a direction and drives two cams; one is used to move the P-lever assembly back and forth and the other makes and breaks the HSW switch, which detects the read/write head position. Fig. 3-12 shows the control circuit.

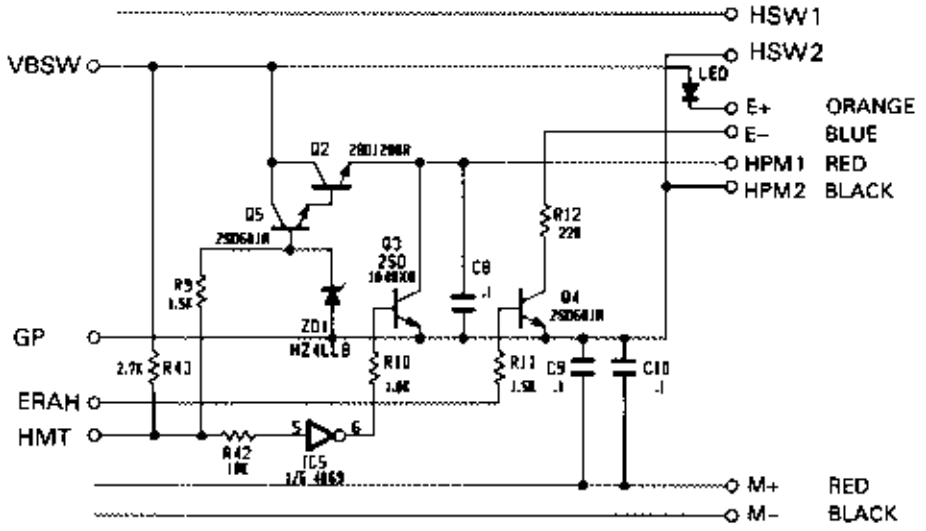


Fig. 3-12 Head Pinch Motor Control Circuit

When the HMT signal goes high, the transistors Q5 and Q2 are turned on and the VBSW voltage is supplied to HPM1 (the positive side terminal of the motor), revolving the motor which in turn causes the P-lever assembly to move back and forth.

When the HMT signal is turned low to stop the motor, the output of IC5 turns off and the output of pin 6 goes high, turns off transistors Q5, Q2, and turns on Q3. This causes the HPM1 line to be shorted to ground, and applies a brake to the motor, preventing revolution by inertia. If the motor continued revolving by inertia, the read/write head position and the pinch roller's contacting pressure against the capstan shaft would deviate from the specifications, and such failures as read/write error would occur.

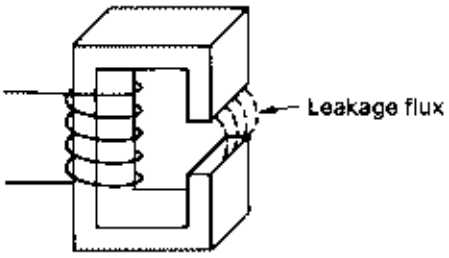
The zener diode ZD1, connected at the base of Q5 maintains the voltage supplied to the motor below the VBSW voltage (approximately 5V). – (A higher motor drive voltage would increase the motor inertia as described above.)

3.1.6.3. Erase Circuit

When the ERAH signal is activated low, transistor Q3 is turned on. This causes a current from the VBSW line to ground passing through the erase winding of the read/write head, and erasing previously written tape data. This circuit operates only during write.

Read/Write Head Structure

Both the read/write and erase heads make use of leakage flux.



Data are actually written on the tape at the copre slit where leakage flux is generate.

Fig.3-13 Read/Write Head Structure

3.1.7 Read/Write Control Section

The read/write control is located in the lower half of the MMC board and consists of a read and write circuit. However, most of the section is actually occupied by the read circuit operational amplifier.

3.1.7.1 Write Circuit (Erase and Write)

Magnetic tape write is accomplished using leakage flux as illustrated above. A logical value of 0 or 1 can be written on reversing tape by reversing the direction of the flux; i.e., the direction of the current through the write head winding.

This circuit reverses the write current direction by means of charging and discharging an electrolytic capacitor. Thus, the current waveform theoretically looks as shown in Fig. 3-14.

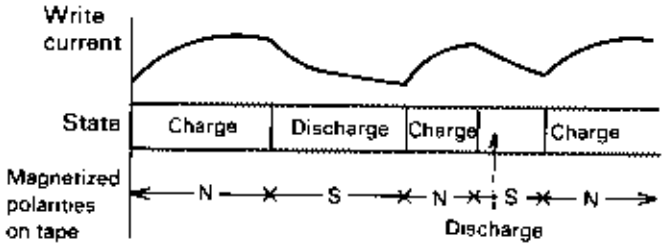


Fig. 3-14 Tape Write Current Waveform

Writing a value is ultimately generating a magnetic polarity determined by the write current direction. In order to eliminate interference which may be caused by data patterns previously written (magnetized) on the tape, the erase head is always activated during write operation initiated by the ERAH signal. New data, then will not be affected by previously magnetized polarities and the tape can be uniformly magnetized as new data is written Fig. 3-15 conceptually illustrates this operation, including the positional relationship between the read/write and erase heads.

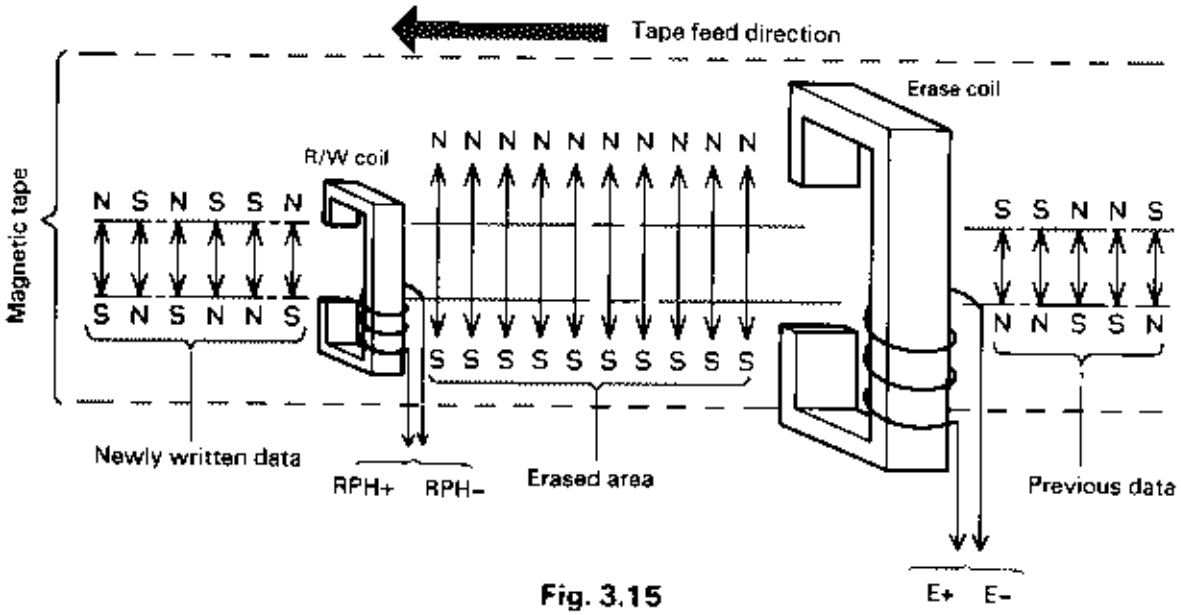


Fig. 3.15

3.1.7.2 Circuit Operations

Fig. 3-16 illustrates the write circuit. To write data, the direction of the write current through the read/write head is alternated by repeating charging and discharging the electolytic capacitor C12.

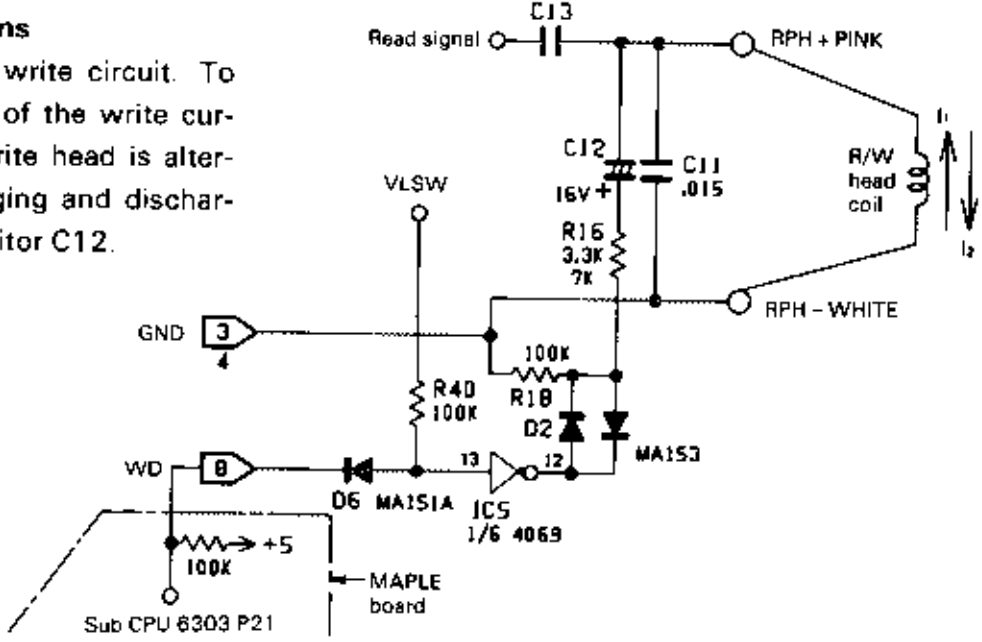


Fig. 3-16

A series of actual data bits is written on tape by alternating current to enable or disable, depending on the value of each bit, the pull-up of the input to pin 5 of IC5 to the VLSW voltage line through R4. The WD signal, which represents the logical value 0 or 1 of each data bit, usually varies its level and appears as shown in Fig. 3-17; it looks like a train of pulses.

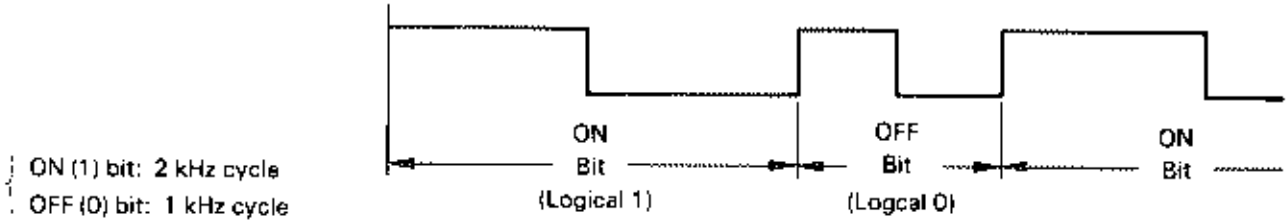


Fig. 3-17 Write Signal (WD) Pulse Train

* The flag bit is also written for each data byte and the write signal appears as shown in Fig. 3-18.

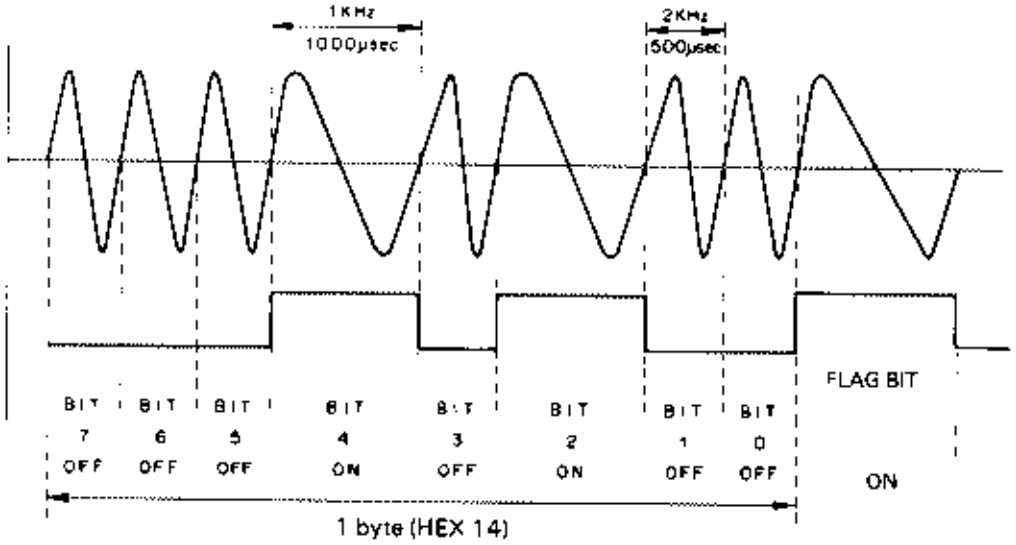


Fig. 3-18 Sample Write Signal Waveform

The above sample illustrates a data write (i.e. transfer) rate of approximately 1286 bps. As shown below, the rate varies depending on the bit configuration of the byte. Because the above sample data byte has four bits on and four bits off, the time required to write the entire byte (8 data bits and 1 stop bit) is:

$$4 \times 0.5 + 5 \times 1.0 = 7 \text{ ms}$$

Thus, a write time of 0.777 ms (7/9) is required per bit, resulting in the data transfer rate of approximately 1286 bps.

Circuit Operations During Non-Write

Part 21 of the 6303 slave CPU on the MAPLE board is a floating part, IC neither activate nor non-active signals are output. The WD signal line is always pulled up through a 100 kohm resistor. This causes output pin 13 of IC5 to be held low. The positive pole terminal of capacitor C12 is always grounded through the diode D2 and IC5, and no current flows through the read/write head.

Circuit Operations During Write

When the WD signal is low, a current flows from the VLSW line to port 21 through R40 and D6, lowering pin 13 of IC5 to almost 0V. This causes pin 12 to go high which allows the capacitor C12 to be charged, resulting in the write current through the read/write head in the direction indicated as I2 in Fig. 3-16.

When the WD signal goes high, C12 starts charging and results in the write current indicated as I1. This charge and discharge cycle is repeated for each data bit until the complete series of data bits is written. The diode D2 connected at pin 12 of IC5 limits the top and bottom of the signal by approximately 0.6V each as shown in Fig. 3-19. This serves to supply the optimum current waveform to the write winding.

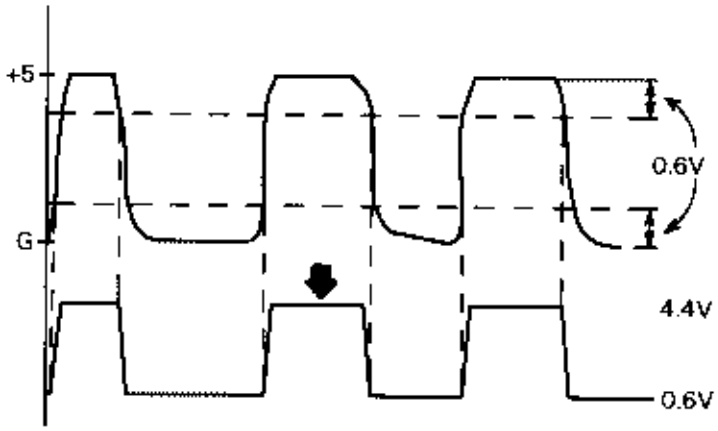


Fig. 3-19 Write Current Waveshaping

For data integrity, however, the data section of each file is written twice. Furthermore, each cassette tape reel requires a directory and a gap between blocks. Thus, the actual write time requires more than twice as long as that obtained from the above transfer rate.

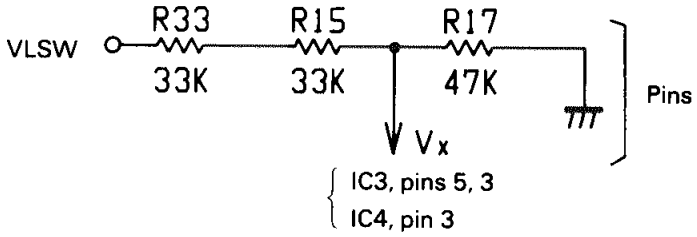
3.1.7.3 Read Circuit

Data written on tape as a series of alternating magnetized polarities is read using voltage induction across the read winding. The induced voltage is amplified by a negative feedback integrating circuit and played back. To also allow sound playback, this circuit has a signal output terminal to the speaker (RDSP) in the middle of a series of amplifiers. Fig. 3-20 shows the circuit.

Circuit Operations

The read signal from the read winding is fed to pin 6 of IC3, after its dc component is removed by capacitor C13. Divided voltage from VLR0 is supplied to pin 5 by the voltage divider circuit.

$$Vx = \frac{5 \cdot 47K}{33K + 33K + 47K} \rightarrow = 2.0\ V$$



Pins 5 through 7 of IC3 form a negative feedback amplifier ($G = -\frac{R20}{R14}$).
The output signal is fed, after its dc component is rejected by capacitor C18, to the next stage, which is also a negative feedback amplifier ($G = -\frac{R22}{R21}$).
The output of this amplifier is fed to the next filter circuit. It is also supplied to the speaker circuit on the MAPLE board. Since no phase compensation is provided in the previous stages, the signal here has some delay.

In the filter circuit, a high frequency component is removed by the T-type filter consisting of R26, R27, and C23, and the amplifier circuit. The amplifier frequency response is varied to lower the gain in a high frequency range.

The amplifier, consisting of pins 1 through 3 of IC3, detects signal peaks.

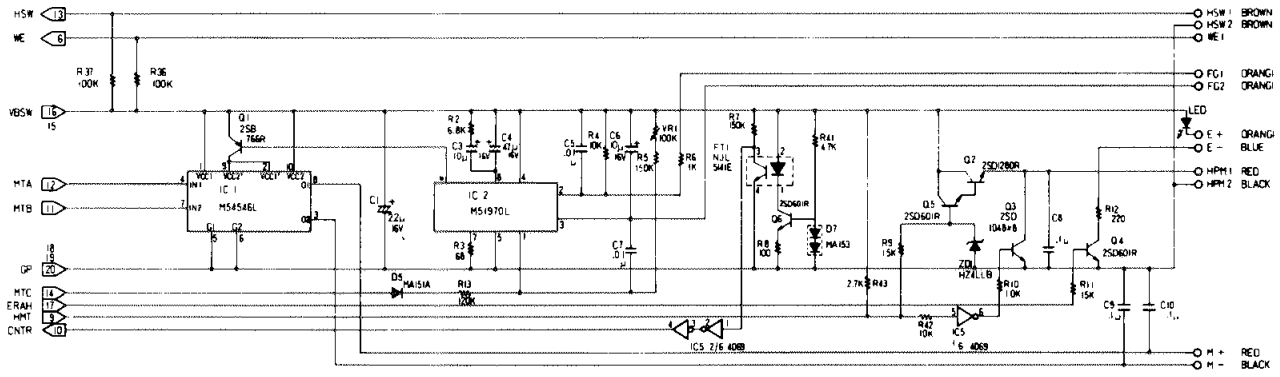


Fig. 3.20 Read Circuit

Observed read signal waveforms – (AZIMUTH tape playback signals)

(Top) Measured at IC3, pin 7 – 5 mV/DIV

(Bottom) Measured at IC3, pin 1 – 5 mV/DIV
Sweep: 0.1

200 μS/DIV

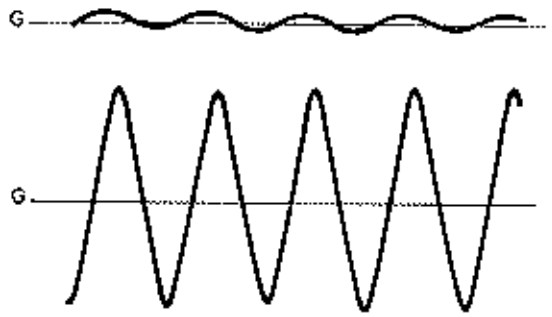


Fig. 3-21

(Top) Measured at IC4, pin 7 – 200 mV/DIV

(Bottom) Measured at IC4, pin 1 – 500mV/DIV

200 μS/DIV

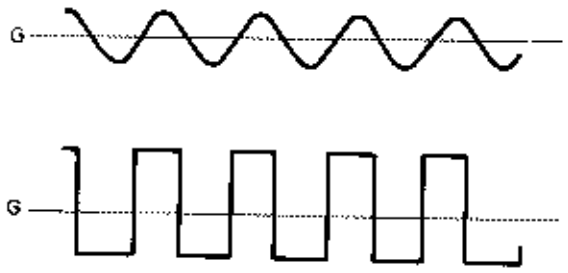


Fig. 3-22

(Top) Measured at IC4, pin 2 – 50 mV/DIV

(Bottom) Measured IC4, pin 1 – 500 mV/DIV

200 μS/DIV

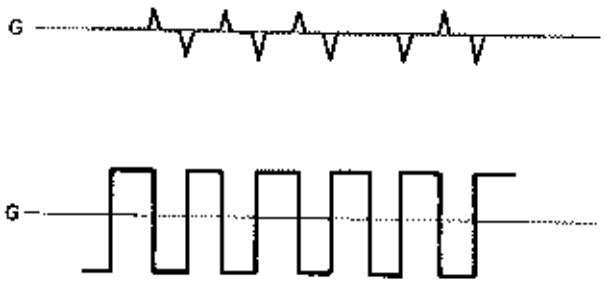


Fig. 3-23

Observed microcassette tape playback waveforms – AZIMUTH tape

(Top) Measured at IC3, pin ..... 5 mV/DIV
(Second from top) Measured at the center of R26 and R27 ..... 20 mV/DIV
(Second from bottom) Measured at IC4, pin 6 ..... 50 mV/DIV
(Bottom) Measured at IC4, pin 5. AC mode ..... 2 V/DIV

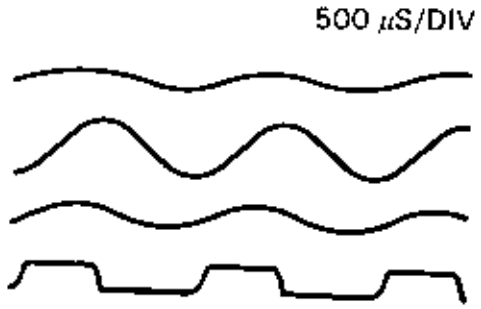


Fig. 3-24

The top three are since waves. The bottom signal is almost a square wave, due to a peak detection by a diode inserted across pins 1 and 2 of IC4.

Observed noise filter (phase compensation) circuit signal waveforms AZIMUTH – tape

(Top) Measured at IC3, pin
(Second from top) Measured at the center of R26 and R27.
(Second from bottom) Measured at IC4, pin 6.
(Bottom) Measured at IC4, pin 5. AC mode

200 mV/DIV
50 μS/DIV

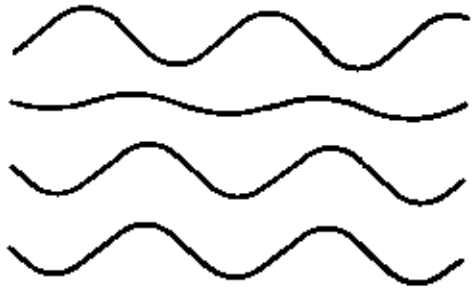


Fig. 3-25

Observed capstan motor control signal waveforms

(Top) Feedback signal from tacho generator – measured at IC2, pin 3.

(Bottom) 400 kHz basic clock signal measured at IC2, pin. 2.

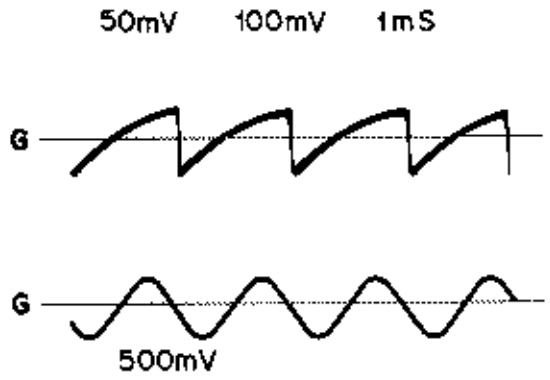


Fig. 3-26

(Top) Capstan motor drive voltage input – measured at IC, pin 2.

(Bottom) Voltage control signal – measured at IC2, pin 6.

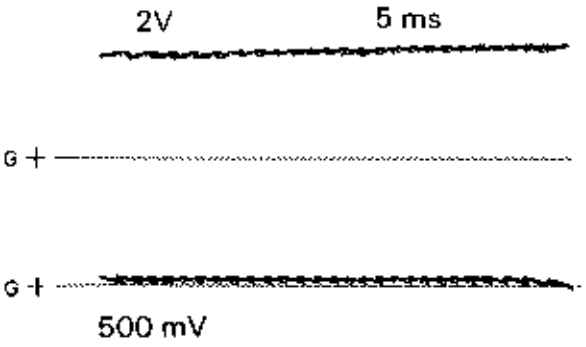


Fig. 3-27

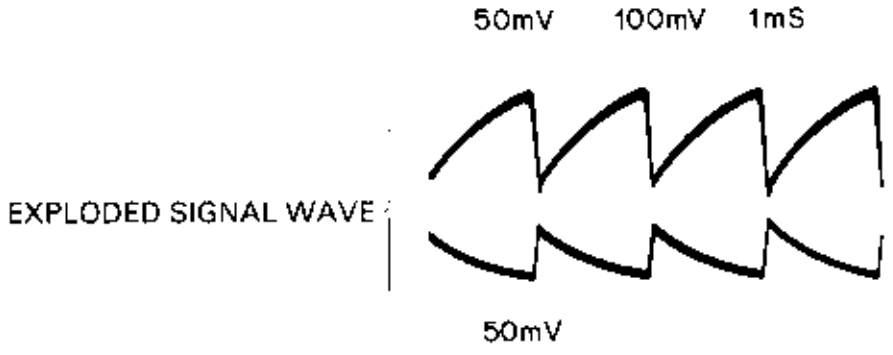


Fig. 3-28

3.2 RAM Disk Unit

Two models of 60K and 120K bytes are available. The models have the same circuit and operates exactly the same way. Only the difference is whether 64K or 128K bytes of DRAM are installed. The RAM disk unit has a Z-80 CPU built in and is operated asynchronously with the Main Frame.

3.2.1 Major Circuit Elements

The RAM disk unit is built on a circuit board which contains casing components and the following major circuit elements shown and listed below including a battery.

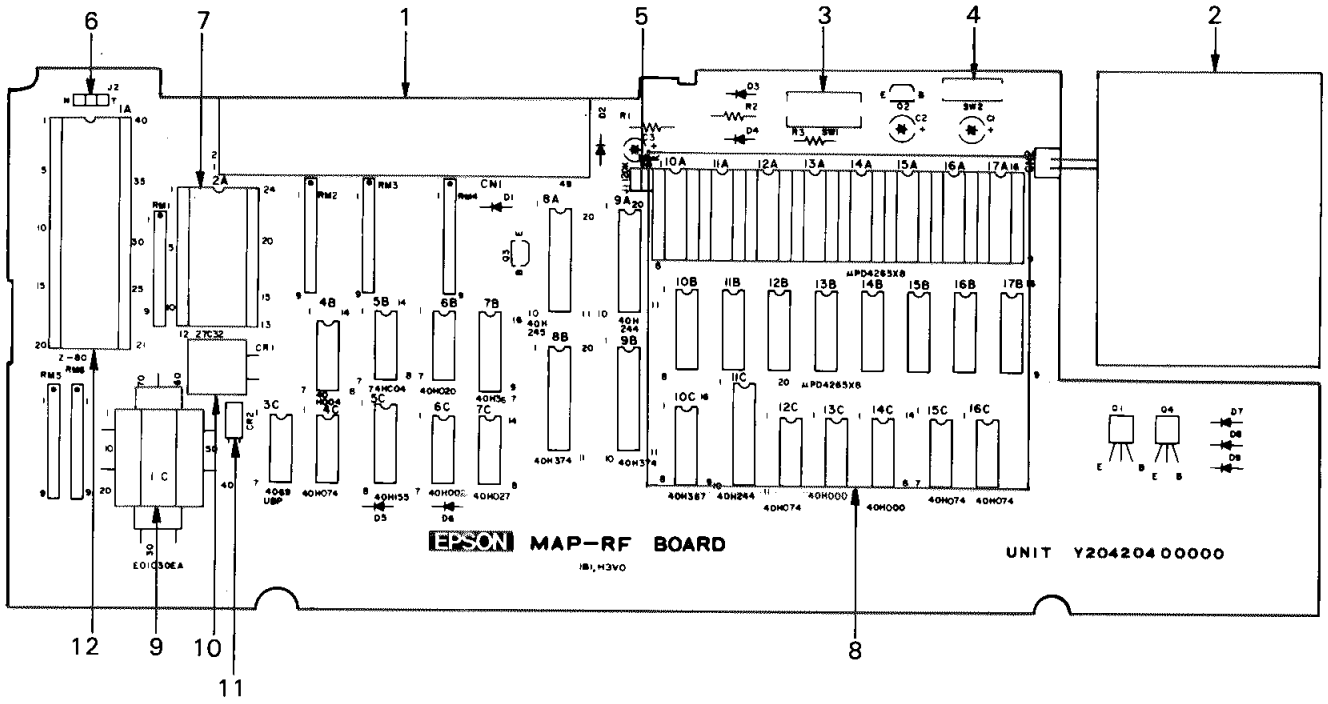


Fig. 3-29 RAM Disk Board Element Lay-Out

Table 3-2 Major Circuit Element

No.	Element	Function	No.	Element	Function
1	Connector CN1	Interface the data and address busses with Main Frame.	2	Battery	4.8V, 480mAH
3	SW 1	Write protect control ON: Protect OFF: Unprotect	4	SW 2	Connect/disconnect the built-in battery – the line normally connected.
5	Jumper J1	Define RAM capacity (60 K or 120 K).	6	Jumper J2	Z-80 CPU selection.
7	ROM (27C32)	Control for RAM disk Operation.	8	D-RAM	64/128 K D-RAM
9	Gate array (GAH40D)	Control for DRAM read/write.	10	Crystal resonator CR1	Provide a clock signal of 9.8 MHz
11	Crystal resonator (R2)	Provide a clock signal of 32.768kHz.	12	CPU Z-80	Control the RAM disk unit – operates at a clock rate of 2.45 MHz.

3.2.2 Function Circuit Blocks

Fig. 3-30 is a functional block diagram of the RAM disk unit.

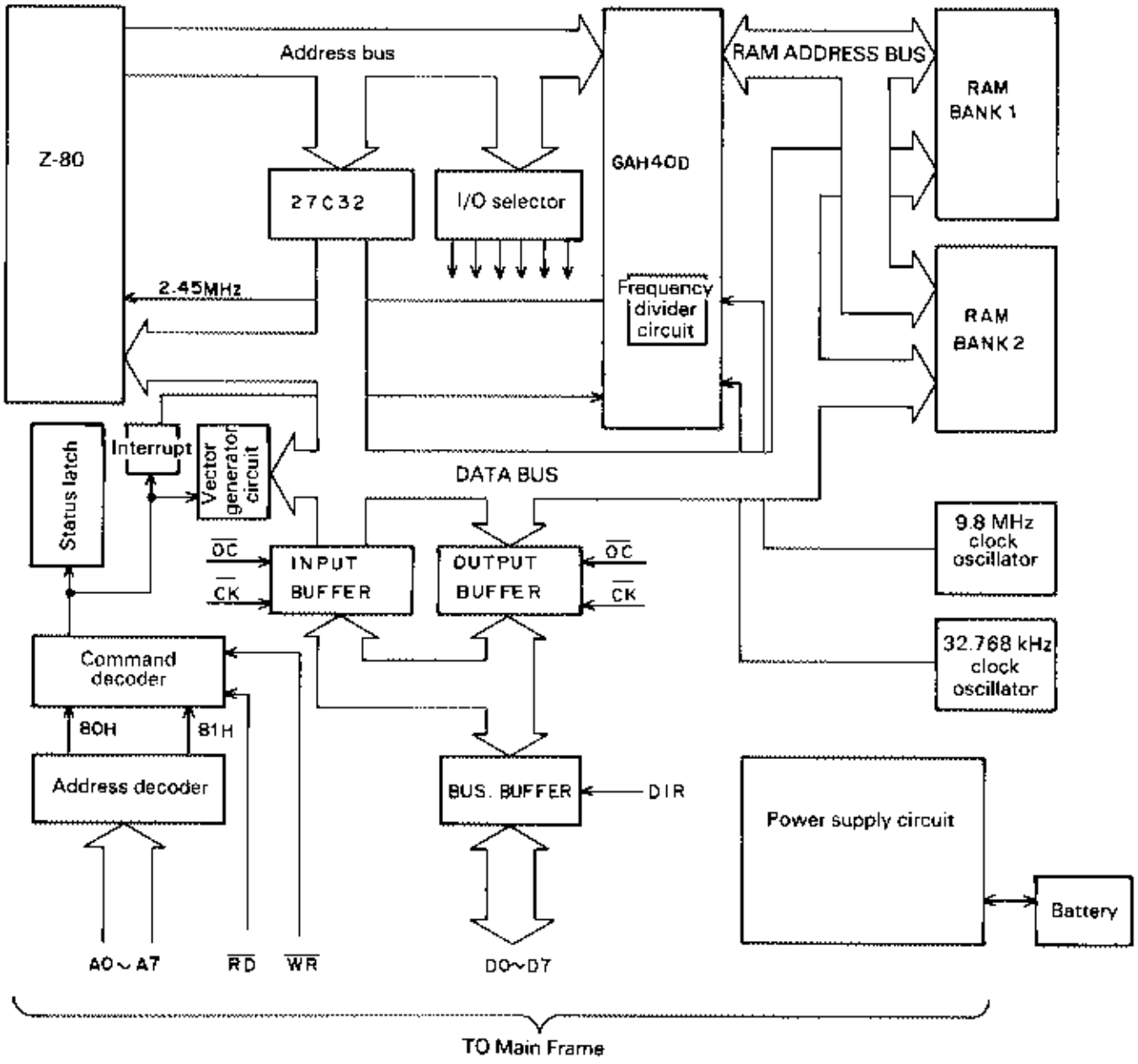


Fig. 3-30 RAM Disk Unit Block Diagram

The RAM disk unit includes a power supply circuit, hand-shaking circuits such as an address and command decoders and a status latch, etc.; a DRAM control circuit; a interrupt control circuit; a data bus input/output control circuit; two clock-oscillator circuits; and an I/O selector circuit. etc. Data are transferred between the Main Frame and RAM disk main CPUs (i.e., read/write operation for RAM disk unit by referring to the status latch. The CPUs have their own memory spaces independent from each other and data transfers between them are accomplished in forms of I/O read/write operations.

3.2.3 Interface Signals

The RAM disk unit is connected to the Main Frame board via a cable assembly # 727. Table 3-3 lists the interface signals.

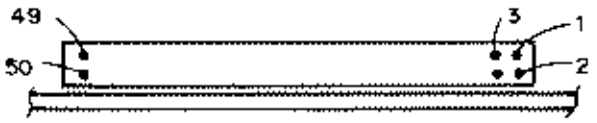


Table 3-3. RAM Disk Unit Interface Signals

Pin No.	Signal Name	Direction	Definition
1	–	–	Not used.
3	–	–	Not used.
5	AB1	Input	Address but line 1
7	–	–	Not used
9	AB4	Input	Address bus line 4
11	AB6	Input	Address bus line 6
13	–	–	Not used.
15	–	–	Not used.
17	DB0	Input/ Output	Data bus line 0
19	DB2	Input/ output	Data bus line 2
21	DB4	Input/ Output	Data bus line 4
23	DB6	Input/ Output	Data bus line 6
25	–	–	Not used.
27	–	–	Not used.
29	VL	Input	Logic circuit +5V supply
31	GND	–	Signal ground
33	$\overline{RS}$	Input	Reset
35	$\overline{RD}$	Input	Read
37	$\overline{WR}$	Input	Write
39	VCH	Input	Battery charge voltage
41	DCAS	Input	Cata CAS
43	–	–	Not used.
45	–	–	Not used.
47	VB1	Input	Battery voltage
49	–	–	Not used.

Pin No.	Signal Name	Direction	Definition
2	–	–	Not used.
4	–	–	Not used.
6	AB2	Input	Address bus line 2
8	AB0	Input	Address bus line 0
10	AB3	Input	Address bus line 3
12	AB5	Input	Address bus line 5
14	AB7	Input	Address bus line 7
16	–	–	Not used.
18	DB1	Input/ Output	Data bus line 1
20	DB3	Input/ Output	Data bus line 3
22	DB5	Input/ Output	Data bus line 5
24	DB7	Input/ Output	Data bus line 7
26	–	–	Not used.
28	–	–	Not used.
30	–	–	Not used.
32	GND	–	Signal ground
34	–	–	Not used.
36	–	–	Not used.
38	–	–	Not used.
40	$\overline{IORQ}$	Input	I/O Request
42	DW	Input	Data Write
44	OFF	Input	GAH40D Initialization
46	–	–	Not used.
48	–	–	Not used.
50	–	–	Not used.

Note:

Some of the signals used in the Main Frame including the address bus lines AB7 through AB15, etc. are not used in this interface.

3.2.4 Jumpers and Switches

The following jumpers and switches are mounted on the RAM disk unit board. The switches SW 1 and SW 2 will be accessed by user.

Table 3-4 Jumper and Switch

Jumper/switch	Standard	Drawing coordination	Function
J1	—	D.E -4	Select a RAM capacity: 60K or 120K bytes, according to the installed RAM elements.
J2	—	E -2	Specifies the main CPU.
SW1	ON	ONE -4	Enable/disable DRAM write protection ON: Enables write protection – allows read only. OFF: Disables write protection – allows both read and write.
SW2	ON	A -6	Enable/disable battery backup ON: Enables battery backup – allows battery charge/discharge. OFF: Disables battery backup – battery charge/discharge is inhibited.

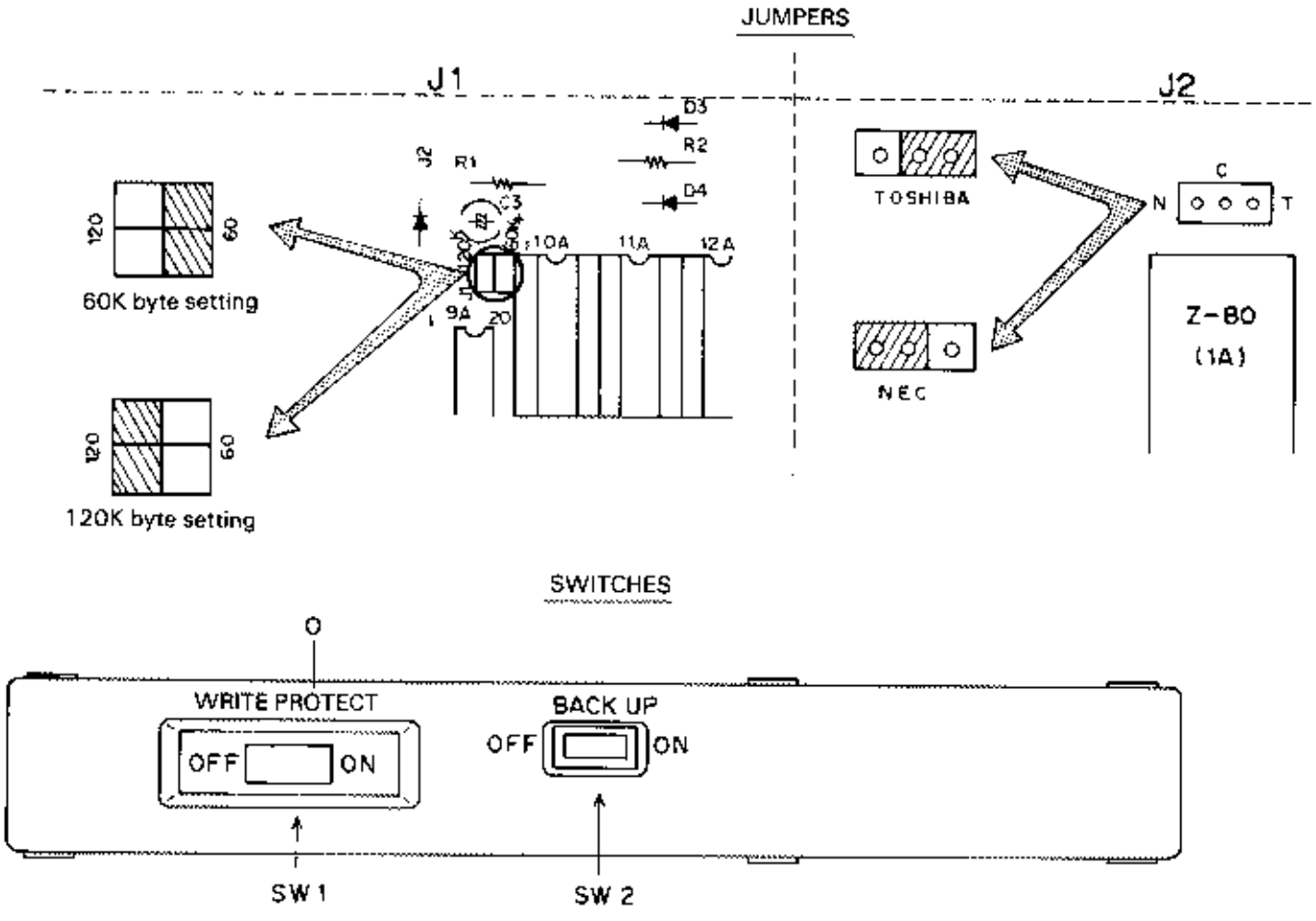


Fig. 3-31 Jumper and Switch Location

3.2.5 Power Supply Circuit

The RAM disk unit power supply circuit consists of a +4.8V, 450 mAH rechargeable battery, a charge circuit, a logic voltage source circuit, and a backup circuit.

1. Rechargeable battery and charge circuit

   The battery is connected to the MAP-RF board via a connector CN 2. The switch (SW2) on the board allows the user to connect or disconnect the battery to the MAP-RF board.

   The circuit surrounding the battery is shown below.

1) Battery backup switch SW2

   This switch should be reset OFF when storing this unit alone or when not using it for a long period of time as attached to the Main Frame. With this switch reset OFF, the battery is prevented from any discharge other than the natural one so that the longest life can be ensured.

* The backup line circuit operates irrespective of the setting of this switch; when the switch is reset OFF, the line is backed up from the Main Frame battery and its working time may be shortened.

2) Battery charging

   The battery is always charged toward the full via either of the following two charging paths:

   When the Main Frame AC adaptor is connected to the AC power source.

   $V_{CH} \rightarrow D2 \rightarrow R1 \rightarrow SW2 \rightarrow CN2 \rightarrow Battery$

   When the AC adaptor is not used but the battery voltage is lower than the VB1 supply voltage from the Main Frame.

   $V_{B1} \rightarrow D3 \rightarrow R2 \rightarrow SW2 \rightarrow CN2 \rightarrow Battery$

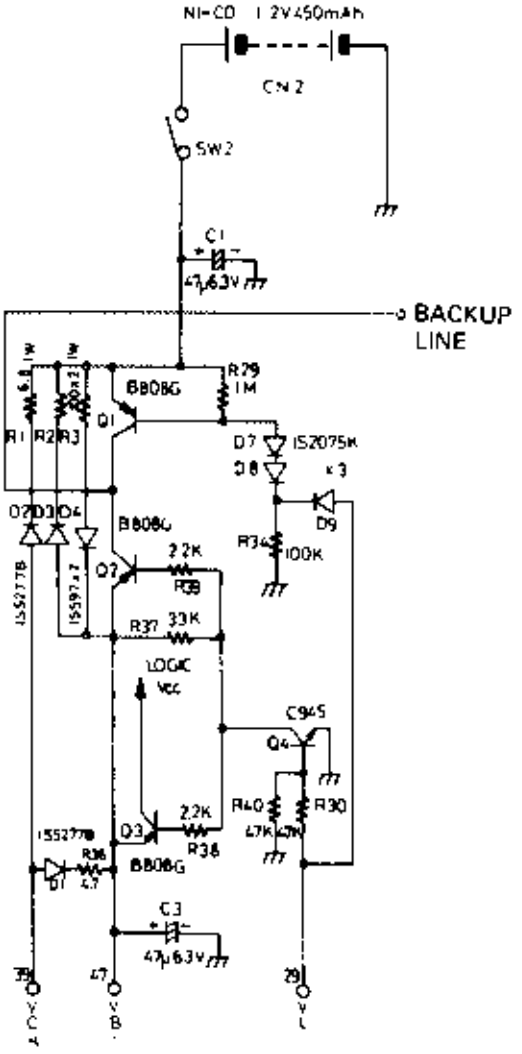


Fig. 3-32 Power Supply Circuit

2. Backup circuit

The backup circuit supplies power required to protect data in the DRAM.

Table 3-5 lists the elements backed up by this circuit.

Table 3.5 Backed Up Elements

Element	Drawing coordination	Function
1C	F-1, 2	Read/write control gate array
9A	H-1	Gate
3C	A, B-7	Gate

Element	Drawing coordination	Function
17B ~ 10B	G-2 ~ 6	D-RAM
17A ~ 10A	H-2 ~ 6	D-RAM
3C	F-3	Gate

These elements are powered from a special line called "Backup" and always active; they are powered by the operating voltage supply while Main Frame is on and from the backup voltage while off.

1) Power supply paths to the backup line

There are the six paths listed in table 3-6 which are selected to supply power to the backup line depending on the various conditions. The abbreviations used in the table mean the following:

V_{B1} : Main Frame battery voltage
V_x : RAM disk unit battery voltage
Battery: RAM disk unit battery

Tabel 3-6 Backup Line Supply Paths

Main Frame power	AC adapter	Battery voltage relation	Path
OFF	Connected	—	V_{CH} → D2 → R1 → Q1 →
	Not connected	$V_{B1} > V_x$	V_{B1} → D3 → R2 → Q1 →
	Not connected	$V_{B1} < V_x$	Battery → CN2 → SW2 → Q1 →
ON	Connected	—	V_{CH} → D1 → R36 → Q2 →
	Not connected	$V_{B1} > V_x$	V_{B1} → Q2 →
	Not connected	$V_{B1} < V_x$	Battery → CN2 → SW2 → R3 → D4 → Q2 →

The backup line is powered either transistor Q1 or Q2 depending on whether Main Frame power is on or off.

* While Main Frame is off, VL is low because the logic circuit operating voltage is not supplied. This maintains transistor Q4 cut off and the collector is pulled up high through resistor R37. Thus, transistors Q2 and Q3 remain cut off.

  VL is also connected to the base of Q1 through diodes D7, D8, and D9. The emitter of Q1 is connected to VB1 or the RAM disk battery voltage and normally maintained at +5V. The source is also connected to the base through R29. Because the base is connected to the signal ground through D7, D8, and R34, the current, which flows from the base to the ground unless the junction of D8 and R34 is pulled up to the VL line, generates a potential across the emitter and base. That is, transistor Q1 conducts due to this potential while Main Frame is off.

While Main Frame Power is on, no effective potential is generated across the emitter and base of Q1 because the base is pulled up to VL, and Q1 is maintained cut off. Q4 conducts because the base input (VL) is low and the collector is held low. This maintains Q2 and Q3 in conduction. Thus, the backup line is powered via Q2 and the logic circuit voltage is supplied through Q3.

3. Logic circuit voltage

The logic circuit voltage is supplied from the collector of transistor Q3. The voltage applied to the emitter (VB1 or V_{CH} through D1 and R34) is supplied to the circuit power line. The supply circuit operates as descried above.

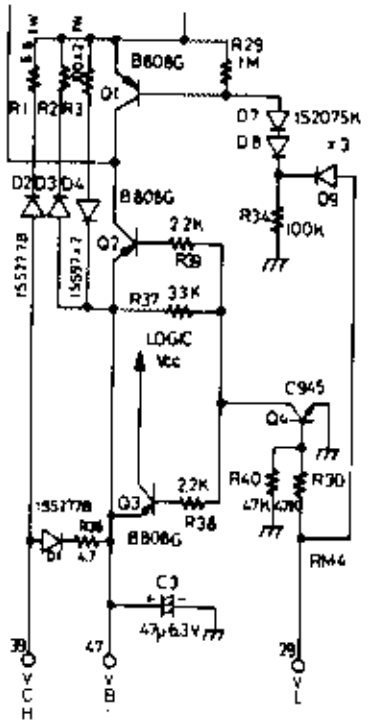


Fig. 3-33 Power Supply Circuit

3.2.6 Interface Circuit

Since this RAM disk unit and Main Frame asynchronously operate, either one must examine the status of the other to accomplish a RAM disk read/write. A function, which temporarily stores the data until it is written in RAM disk or read by Main Frame, is also required.

1. Address decoder

The RAM disk is looked upon as an I/O device by the Main Frame CPU and two I/O addresses are assigned. Fig. 3-34 shows the address decoder circuit.

Pin 10 and 13 of IC "6C" are the outputs of the decoder. As obvious from the figure, the output (pin 8) of IC "6B" must be low to enable the two decoder outputs. Either of them is selected depending on the state of A0. The output IC "6B" is low when the following relation is satisfied among the input signals to this IC and the preceding IC "7C"; $\overline{A1} - \overline{A6}$ .A7.$\overline{IORQ}$. This relation can be logically represented as in Fig. 3-34; an address 80 (H) or 81(H) is decoded to access the RAM disk unit.

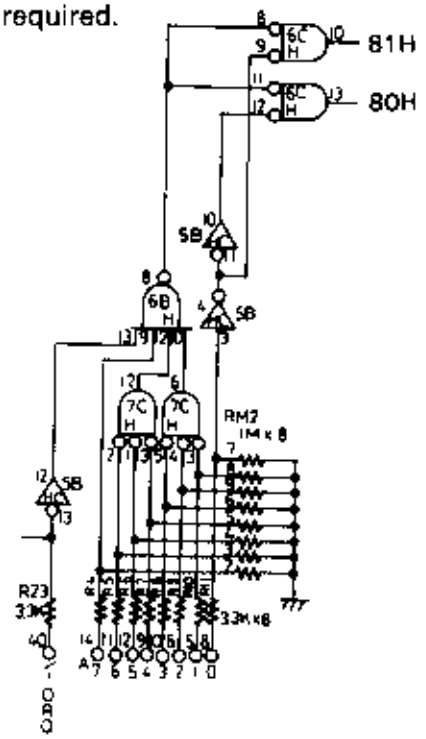


Fig. 3-34 RAM disk address decoder circuit

A7	A6	A5	A4	A3	A2	A1	A0
1	0	0	0	0	0	0	1/0

80 (H)
or
81 (H)

2. Command decoder

Four signals are generated by IC "14C" from either address supplied from the address decoder and the $\overline{RD}$ and $\overline{WR}$ signals as shown in fig. 3-35.

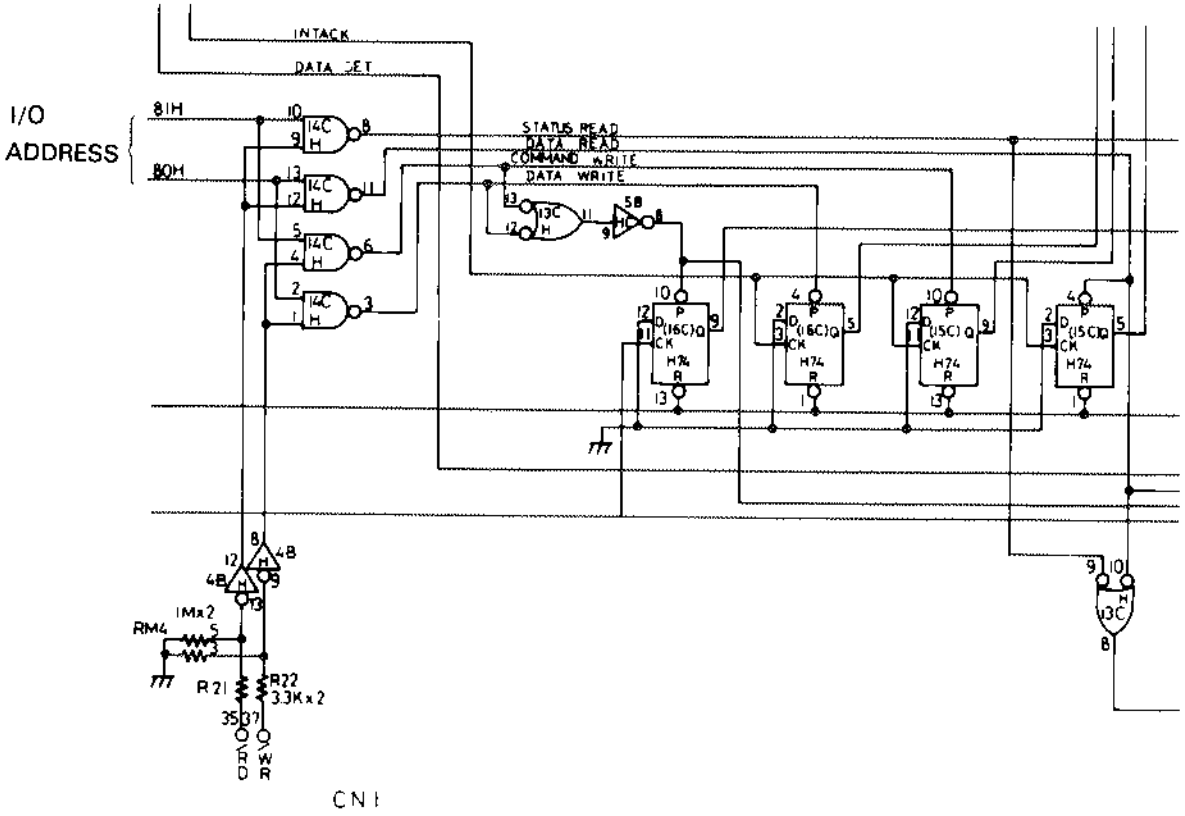


Fig. 3-35

The four I/O read/write signals provide the functions listed in table 3-7.

Table. 3-7 Command Decoder Signals

I/O Addrss	$\overline{RD}$/$\overline{WR}$ signal	Generated signal	Function
81 (H)	$\overline{RD}$	Status Read	Read RAM disk status to Main Frame
	$\overline{WR}$	Command Write	Write a command from Main Frame to RAM disk.
80 (H)	$\overline{RD}$	Data Read	Read data from RAM disk to Main Frame
	$\overline{WR}$	Data Write	Write data from Main Frame to RAM disk.

Unlike the other three, the Status Read signal reads the RAM disk status register irrespective of the RAM disk CPU operation, directly controlling the register read access and data bus drive. The other signals cannot accomplish their functions without intervention by the RAM disk CPU. In addition, any of these signals cannot be directly transferred between the Main Frame and RAM disk CPUs because they are operating asynchronously. Thus, a means is required to temporarily store the signals. This is accomplished by the circuit consisting of the two ICs "15C" and "16C" both of which contain two D-type FF having Preset (P) and Clear (C) terminals. Each of four signals is connected to the Preset terminal of one of the four D-type FFs. Once a signal activated low, the corresponding FF is set and the Q output remains high until either of the following occurs:

* CK input: I/O port 03 (H) read by RAM disk unit - FF output read.
* R input : PX-8 reset or I/O port 01 (H) write by RAM disk unit - program reset.

3. Data and command registers

Two 8-bit registers are provided for input and output which serve as buffers (temporary data storage) used during data transfers between the RAM disk unit and Main Frame. Their input/output or read/write is controlled via an address assigned to them. The data is directed on the data bus from/to the registers under a directional control by the data bus control feature provided by a tri-state buffer IC "8A". Fig. 3-30 shows the data transfer directions and the direction control circuit.

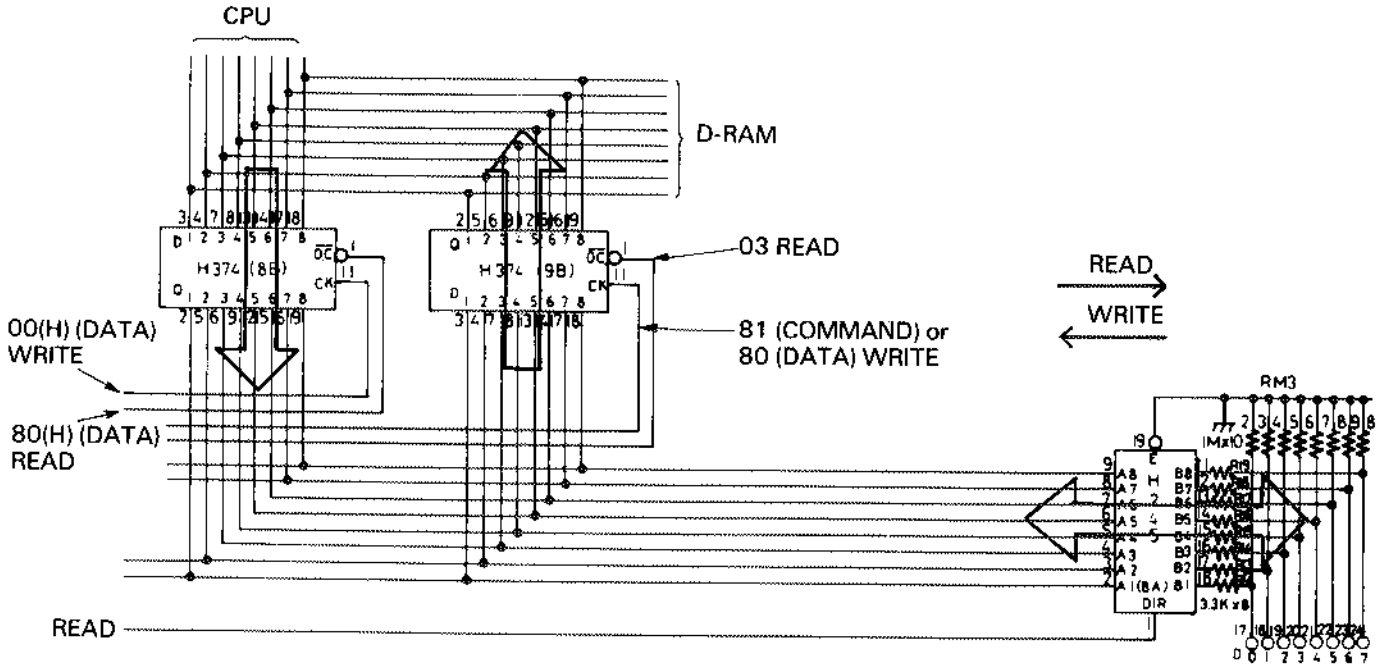


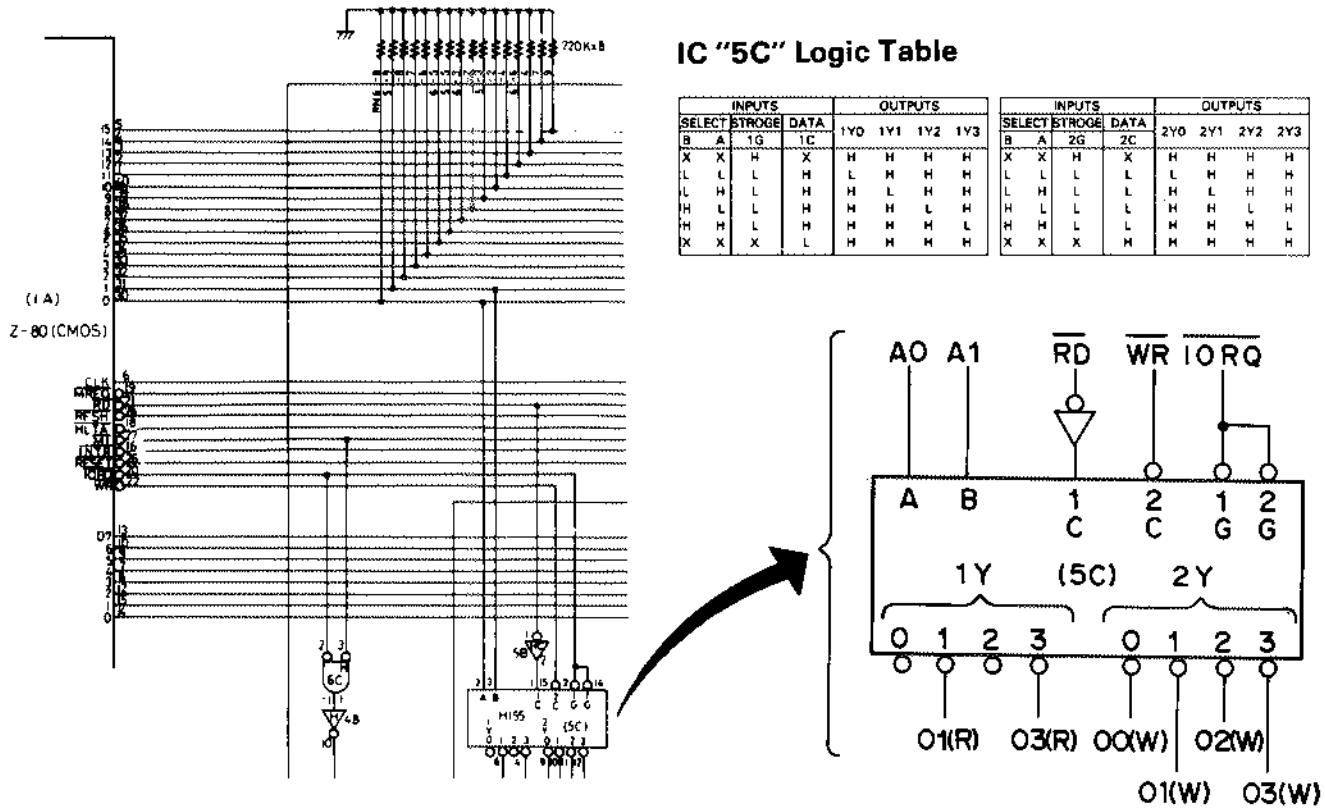
Fig. 3-36 Data Transfer Directions and Control

ICs "8B" and "9B" contain eight tri-state D-type FFs each. The FFs read and latch data from either data bus as arrowed when the "CK" signal rises. When the "$\overline{OC}$" signal goes low, the latched data becomes available onto the data bus from the output (Q) terminals.

- IC "9B" is the Input register. It latches a data directed from Main Frame via address 81 (H). This data is then transferred to the RAM disk CPU when it reads its I/O port 03 (H).
- IC "8B" is the Output register. It latches a data when the RAM disk CPU writes to its I/O port 00 (H). Then, the latched data is sent over the data bus to Main Frame when it reads its I/O port 80 (H)..
- The tri-state buffer register "8A" is controlled by the DIR input signal. When this signal is high, the "bufferred" data is directed from the RAM disk unit to Main Frame. When the signal is low, the data transfer direction is reversed.

3.2.7 I/O Selector

The I/O selector (IC "5C") is the RAM disk CPU I/O address decoder which is used for handshaking in the interface. Fig. 3-37 shows the circuit and table 4-7 lists its decoding logics.



IC "5C" Logic Table

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	1G	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	2G	2C	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

Fig. 3-37 I/O Selector Circuit

IC "5C" has six outputs whose functions are listed in table 3-8.

Table 3-8 I/O Selector Logics

Read/Write	I/O Port Address	Supplied To	Function
READ	01	7B	Read J1 and SW1 status.
	03	9B	Read data or command from input register.
WRITE	00	12C, 8B	Write data to output register.
	01	13C	Program Reset output signal.
	02	4C	RAM bank 0/1 control
	03	4C	RAM bank 2 control

3.2.8 Bank Control

The RAM disk unit can contain a 4 K byte IPL ROM and 64 K or 128 K byte DRAM. However, the Z-80 CPU cannot directly access DRAM above 64 K bytes. Thus, DRAM needs to be divided into banks so that entire DRAM can be accessed indirectly by selecting bank. This control is accomplised by the Bank Latch circuit and the gate array GAH40D shown in fig. 3-38.

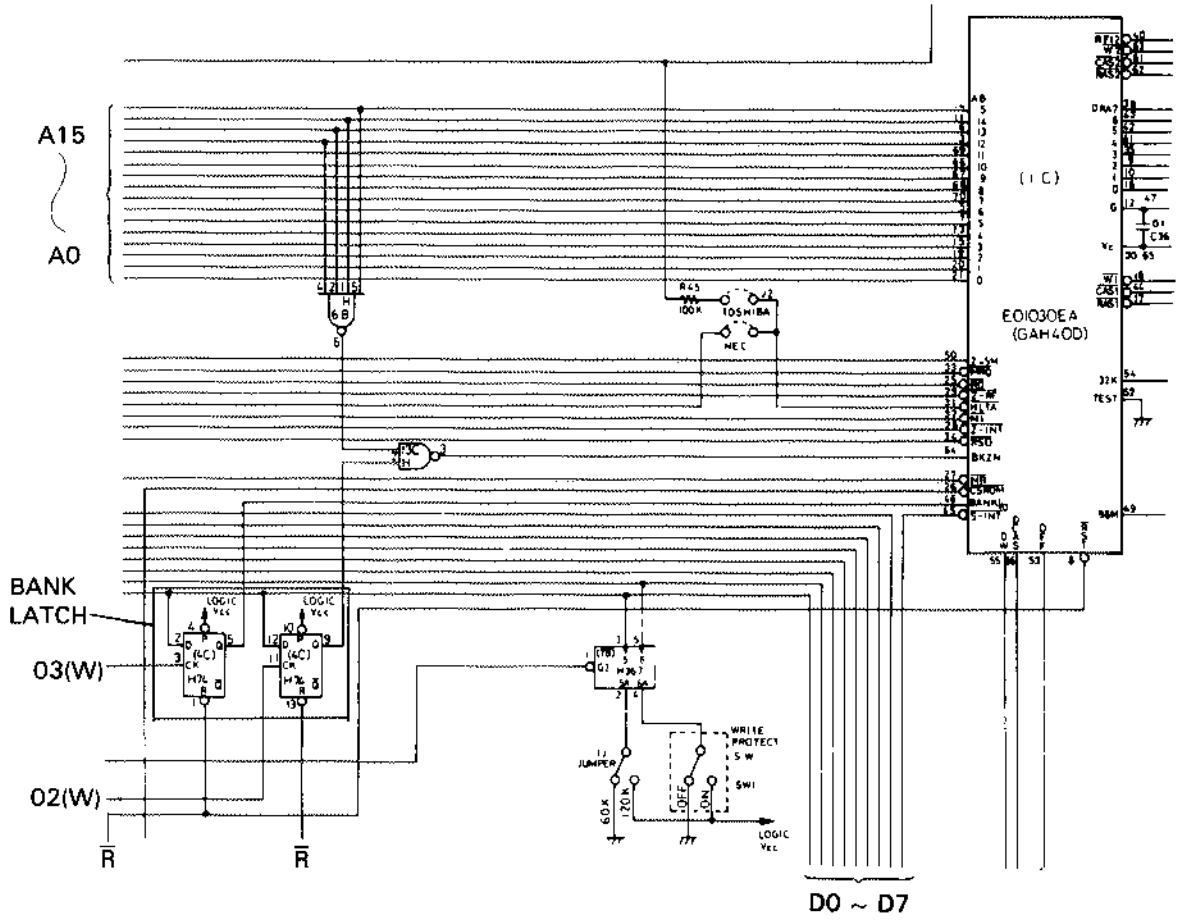


Fig. 3-38 Bank Control Circuit

1. Momory map

The bank control signals and the memory map are associated as shown in table 3-9.

Table 3-9 Bank Control Signal and Memory Map

BK 2 / BK 0/1 / Address	1 / 0	1 / 1	0 / 0	0 / 1
FFFF (FC00)	DRAM 2	DRAM 2	DRAM 1	DRAM 1
(0FFF) 0000	IPL ROM		IPL ROM	

Note:

The DRAM address space from FC00 to FFFF is a comon area which contains the bank selection program.

Gate GAH40D is initialized as follows when Main Frame Power is turned on:

Bank 2 = 1, Bank 0/1 = 0

This initialization is of course accomplished by a hardware reset logic. The initialization circuit operation is described below.

- The Reset ($\overline{R}$) signal is connected to both the Bank Latch FFs located in drawing coordinations C,D-3. Thus, the two Q outputs are held-low - the output from pin 5 is the Bank 0/1 Selection signal and the output from pin 9 is the Bank 2 Selection signal. Address bus lines 12 through 15 from the Z-80 CPU are respectively connected to pins 4, 2, 1, and 5 of IC "6B" which are all low immediately after Main Frame power is turned on, raising the output (pin 6) high. This output signal is fed to IC "13C" where it is NANDED with the Bank 2 Selection signal from the Bank Latch circuit which is also low immediately after power on. Thus, the output from pin 3 is high.

The RAM disk memory address space is mapped as shwon in the second (from the left) or fourth column of table 3-9 by initialization so that the CPU accesses address 0000; i.e., the IPL ROM area.

2. Bank selection

   Bank selection is accomplished by the program in IPL ROM which accesses I/O ADDRESS 02 and 03, which are connected to the Bank Latch, to change the latch setting. Thus, if a bank, which allows no IPL ROM access, were selected by simply accessing the Bank Latch, no subsequent bank selection would be possible. In order to solve this problem, the bank control program is usually written in the DRAM area from a certain address during the IPL program execution. This unit initially loads the bank control program in a DRAM 2 address space from FC00 to FFFF, and a common DRAM 2 area of the highest 64 bytes is always selected independently by gate array GAH40D regardless of bank (0/1 or 2).

3.2.9 Interrupt

As previously stated, the command (i.e., Read or Write) and 8-bit data sent from the Main Frame is temporarily stored in an internal buffer because the RAM disk unit operates asynchronously. The unit is notified of this temporary storage by an interrupt. Fig. 3-39 shows the interrupt circuit.

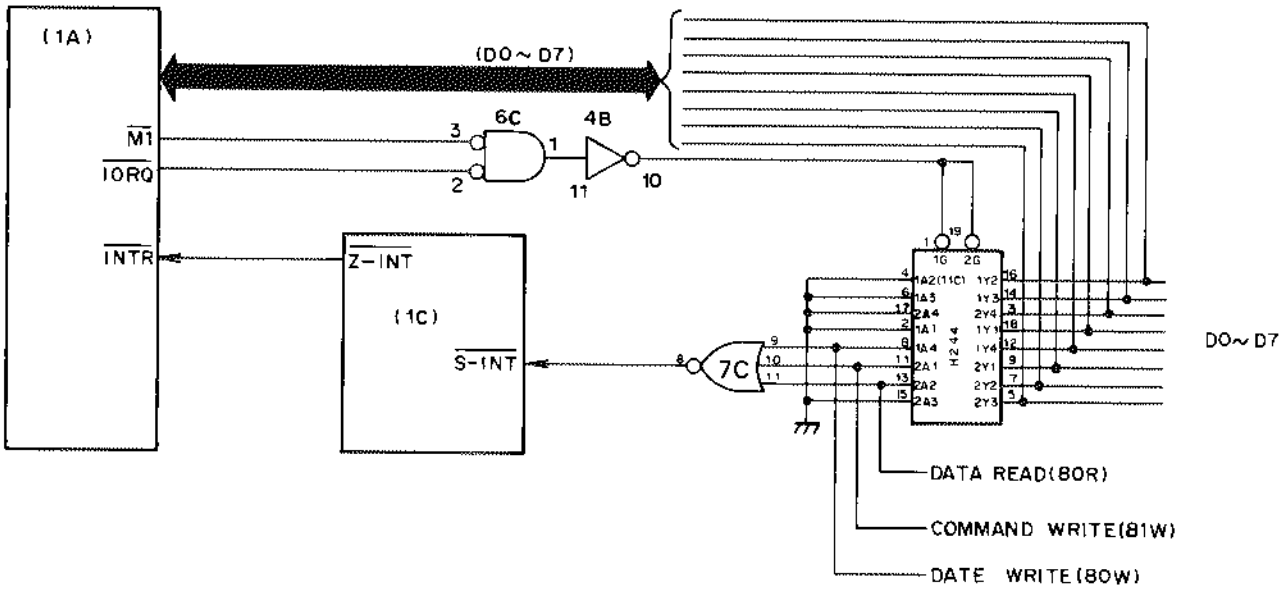


Fig. 3-39 RAM Disk Interrupt Circuit

As obvious from the drawing, the three signals other than Status Read, which instructs an immediate read, are fed to the OR circuit of IC "7C" via D-type FFs "15C" and "16C" whose output is connected to the $\overline{\text{S-INT}}$ terminal of gate array "1C". This input signal is output from the gate array as the $\overline{\text{Z-INT}}$ signal to the $\overline{\text{INTR}}$ terminal of the CPU as the interrupt input. When the AND condition between $\overline{\text{M1}}$ and $\overline{\text{IORQ}}$ is met (indicating that a vector address is output on the data bus in the CPU mode 3) after an interruption occurs, a byte data corresponding to the RAM disk command signal is output on the data bus from the right terminals of IC "11C". This data is the interrupt vector which is fed to the CPU. There are the following interrupt vectors corresponding to the RAM disk command signals:

Command signal	**Interrupt vector**	
Data Read	02	Each of these vector address calls a specific routine that processes the corresponding command and data.
Command Write	04	
Data Write	08	

After an interrupt is accepted, the D-type FF which caused the interrupt ("15C" or "16C") is initialized. Fig. 3-40 shows the related circuit. The vector address is output and the D-type command buffer FF is reset by the same signal INTACK. However, the FF is reset at the rising edge to ensure the interrupt vector to be completely fed to the CPU as shown in fig. 3-41.

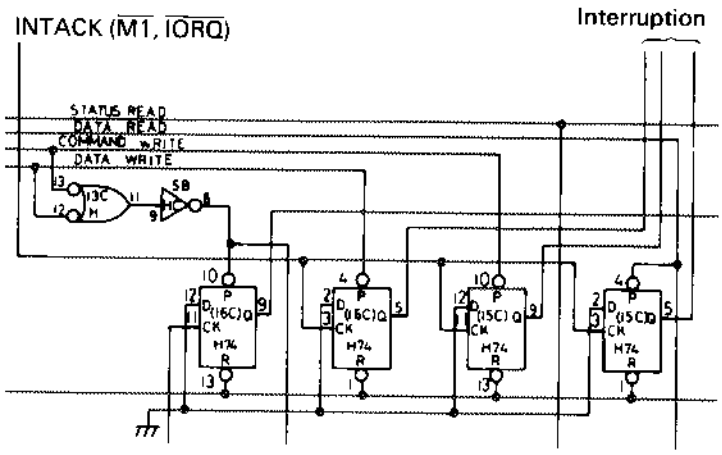


Fig. 3-40

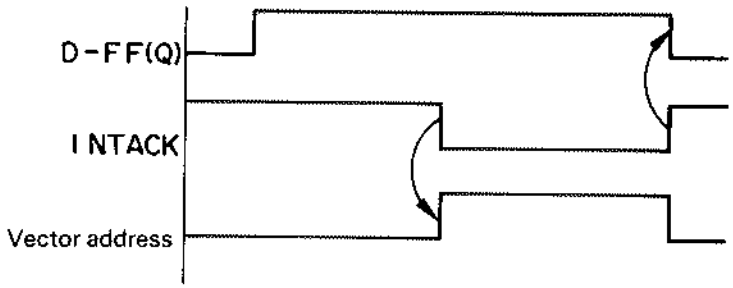


Fig. 3-41 RAM disk command buffer circuit

3.2.10 Clock Signals

Two clock signals of 9.8 MHz and 32.768 kHz are generated in the RAM disk unit. 9.8 MHz clock signal is divided in gate array GAH40D to 2.45 MHz and fed to the CPU. The 32.768 kHz clock signal is also divided in the gate array and used as the DRAM refreshing signal. Fig. 3-42 shows the clock signal oscillator circuits.

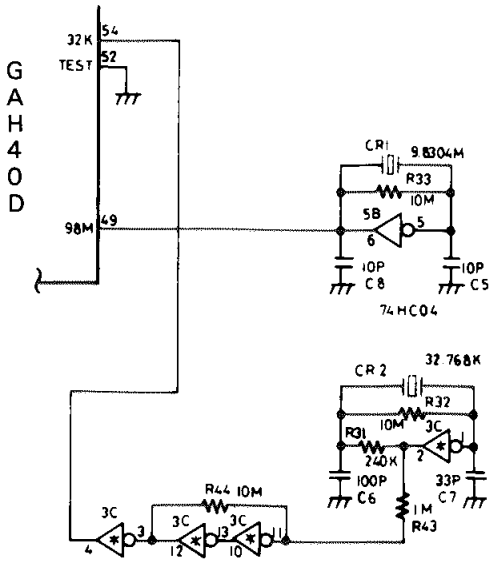


Fig. 3-42

3.2.11 DRAM Banks

The DRAM circuit is organized as shown in fig. 3-43 and controlled by gate array GAH40D.

It is read/written and refreshed (also while Main Frame power is off) in the same way as Main Frame RAM. This unit has two DRAM banks of 64 K bytes each and can provide a capacity of 64 K or 128 K bytes. Two signals DCAS and DW, which determine a refresh mode while power is off, are applied from Main Frame.

- IC "9C" is provided to ensure the address output that can drive 128 K bytes of RAM.

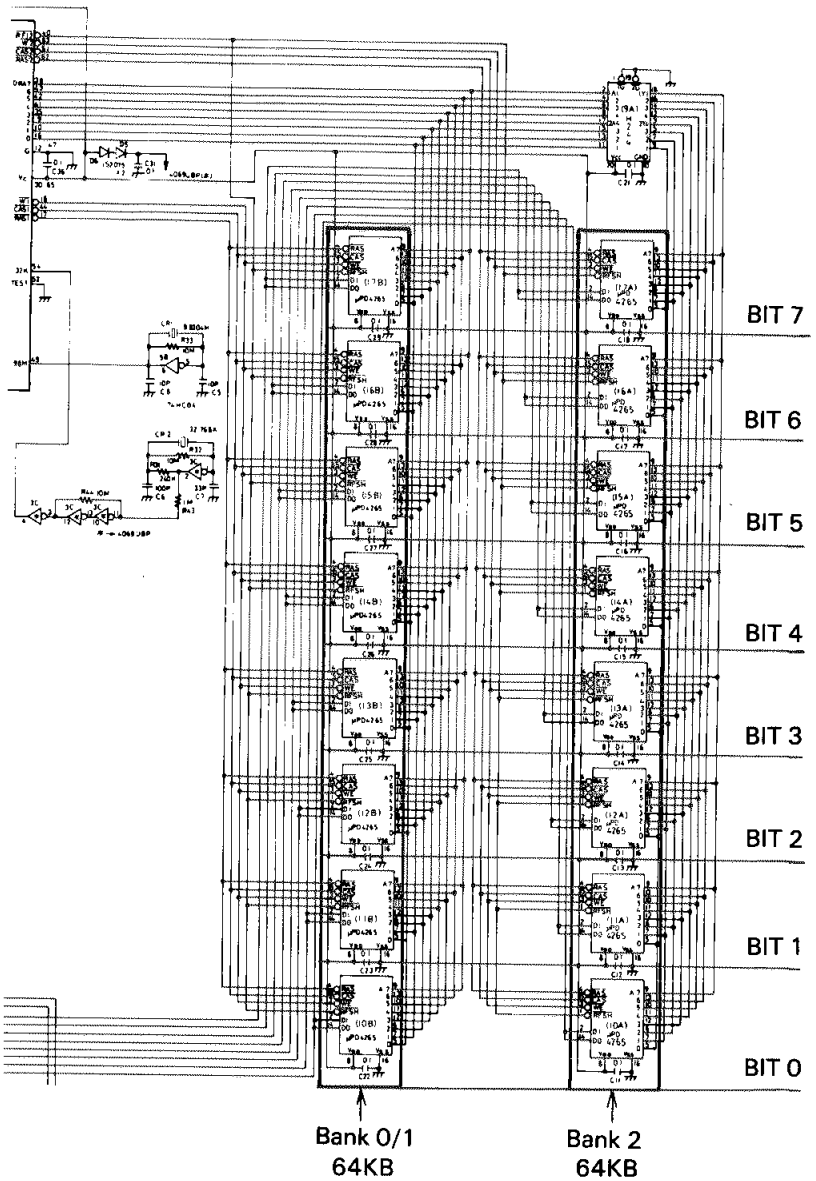


Fig. 3-43 DRAM Circuit Organization

3.2.12 Jumpers and Switch

The combination of jumper J1 and switch SW1 allows the IPL program to be read via I/O port address 01. Jumper J2 selects a CPU model.

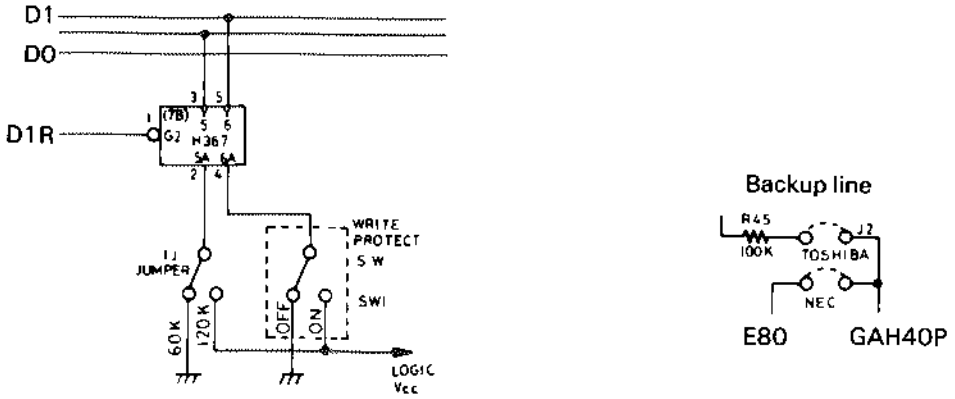


Fig. 3-44

3.2.13 Status Register

The Main Frame CPU reads the RAM disk status from IC "10C" shown in fig. 3-45. Input terminals 6 and 10 are grounded to produce the ID code of the RAM disk unit. The Date/COM Write signal input to terminal 4 indicates whether a data or command received from Main Frame is being processed or not. The signal input to terminal 2 from D-type FF "12C" indicates whether a data is latched (buffered) to be sent to Main Frame or not.

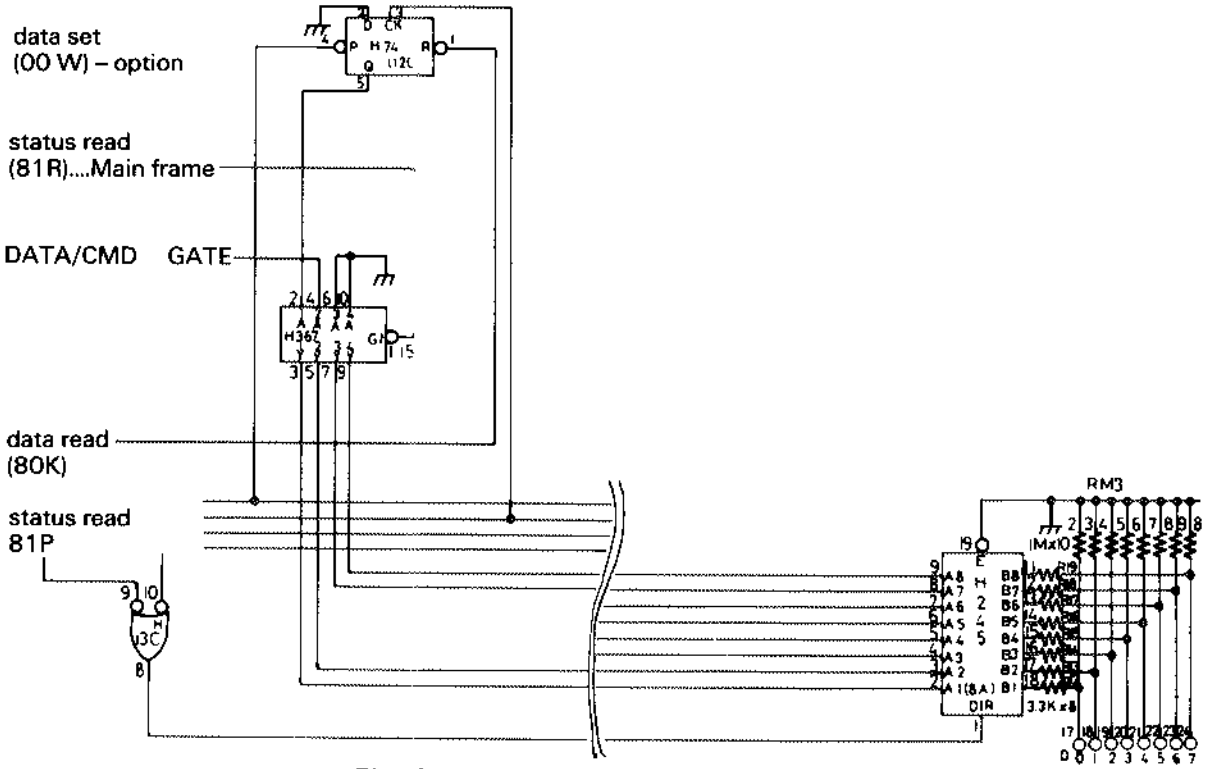
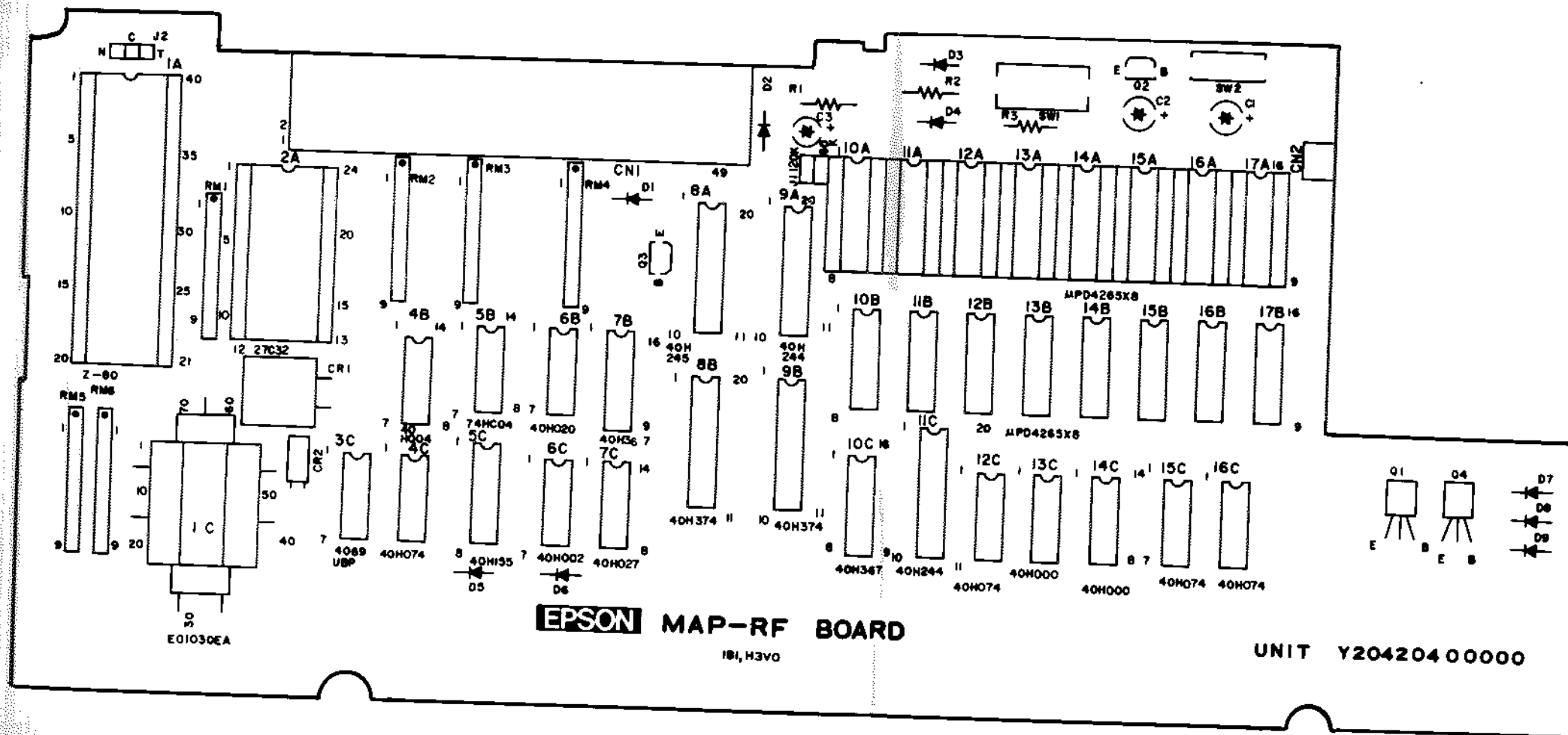


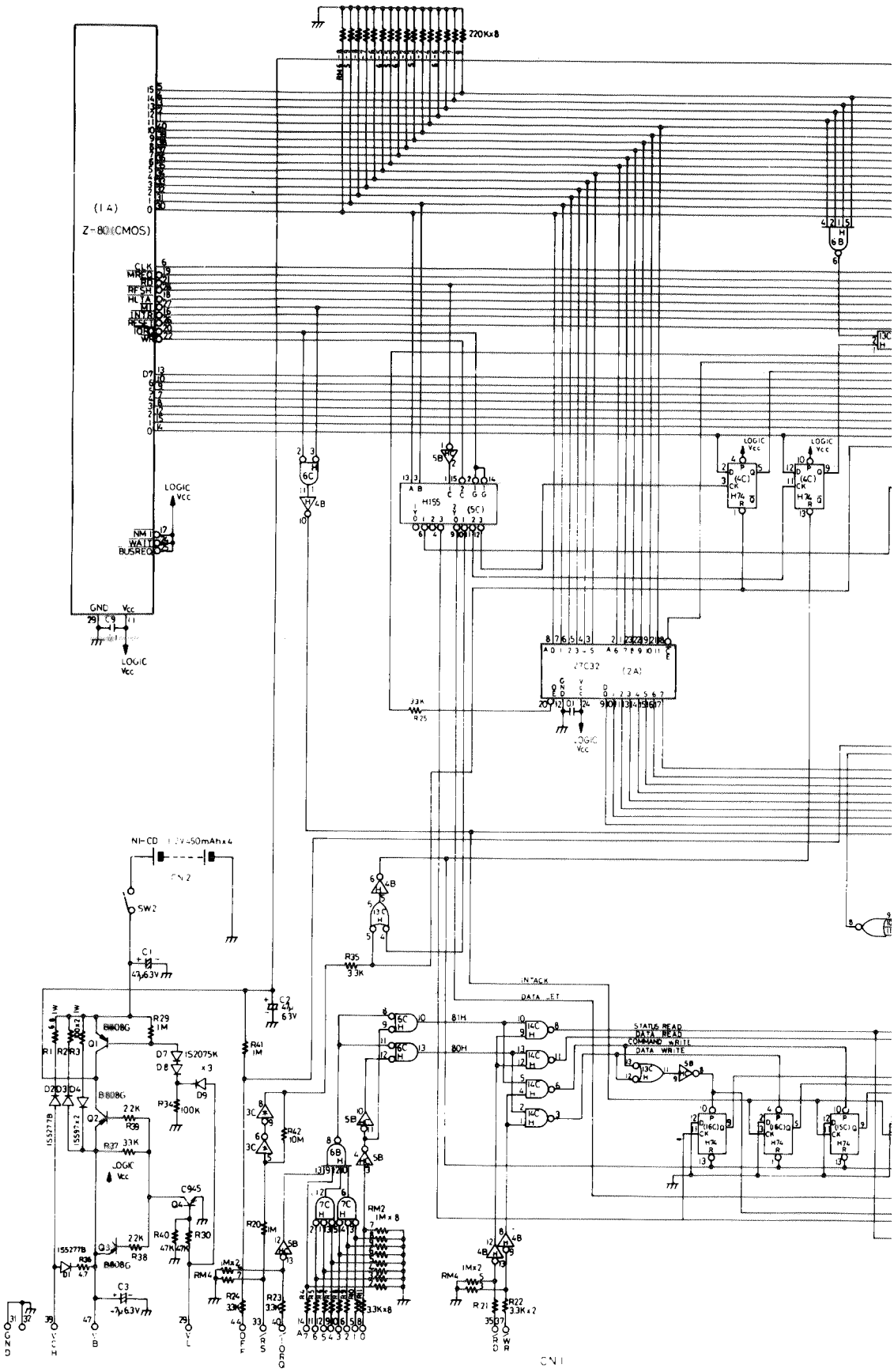
Fig. 3-45 DRAM Circuit Organization

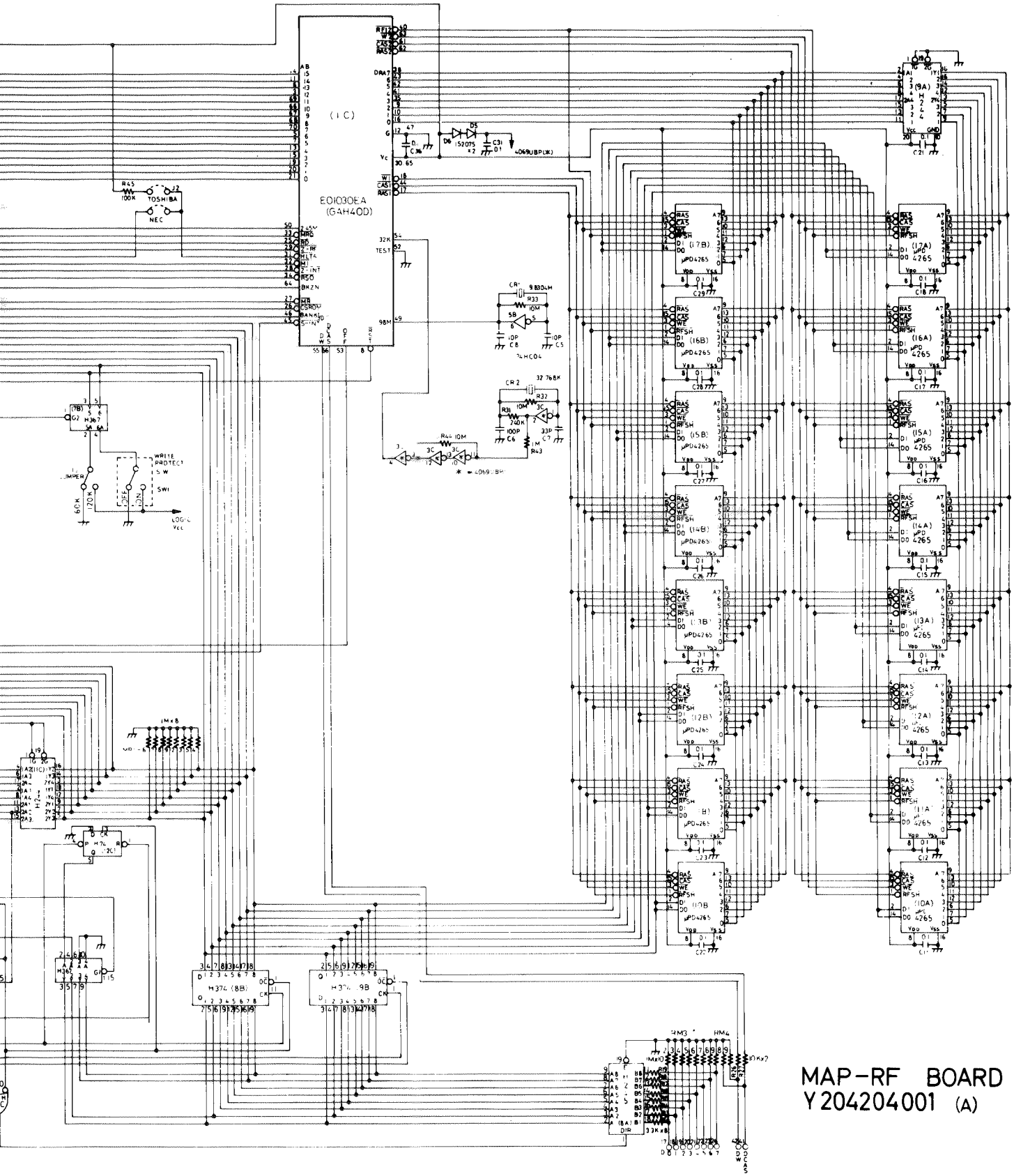


EPSON **MAP-RF BOARD**

IBI, H3V0

UNIT Y204204 00000


A
B
C
1
2
3
4
5
6
7
8
220K×8
RM5
(1A)
Z-80(CMOS)
CLK
MREQ
RD
RFSH
SYNC
HLTA
MT
INTR
RESET
IORQ
WR
D7
D6
D5
D4
D3
D2
D1
D0
LOGIC Vcc
NMI
WAIT
BUSREQ
GND
Vcc
C9
LOGIC Vcc
HI55
(5C)
27C32
(2A)
23K
R25
NI-CD 1.2V-50mAh×4
CN2
SW2
C1
47μ/63V
C2
44
63V
R35
3.3K
INTACK
DATA SET
81H
80H
STATUS READ
DATA READ
COMMAND WRITE
DATA WRITE
R29
1M
R41
1M
R42
10M
R20
1M
R40
47K
R30
47K
R38
22K
R39
22K
R37
33K
R34
100K
D7
D8
D9
1S2075K
×3
B808G
Q1
Q2
Q3
Q4
C945
155277B
155972×2
D1
4.7
C3
7μ/6.3V
RM4
1M×2
RM2
1M×8
R24
33K
R23
33K
33K×8
R21
R22
33K×2
CN1


E
F
G
H
(I C)
E0I03OEA
(G4H40D)
TOSHIBA
NEC
R45
100K
WRITE
PROTECT
SW
SW1
JUMPER
60K
120K
OFF
ON
LOGIC
Vcc
9.830M
74HC04
32.768K
4069UBP
MAP-RF BOARD
Y204204001 (A)

3.3 Modem Unit

This option unit is designed to meet a wide variation of applications and provides the following features:

(1) Communicating capability

This unit BELL103 (ORIG/ANS) compatible and is capable of a full-duplex FSK communication of up to 300 bps.

(2) Connection with telephone line

An FCC-registered line interface, which allows a direct connection to telephone line, is included as a standard feature.

A connection via acoustic coupler is also possible.

(3) Voice communication capability

The unit allows voice communications with the use of a handset.

(4) Monitoring capability

The line state can be monitored via the Main Frame speaker.

(5) Automatic dialing and answering capabilities

The unit is capable of automatic dialing by pulse or tone, and automatic answering by BELL signal detecting circuit.

3.3.1 General

The subsequent descriptions require some knowledge of the operations of telephone lines because this option unit is directly connected to one of them. There are several types of telephone lines are available which require different communications specifications such as communication system, etc. However, only concepts which are required to understand the unit are discussed here.

(1) Telephone line network

A telephone line network is rationally structured including several levles of exchanges through which any communication is accomplished. Thus, the same party may be connected through various routes depending on the state of interexchange channels which affects the connection route. Fig. 3-46 shows an example structure.

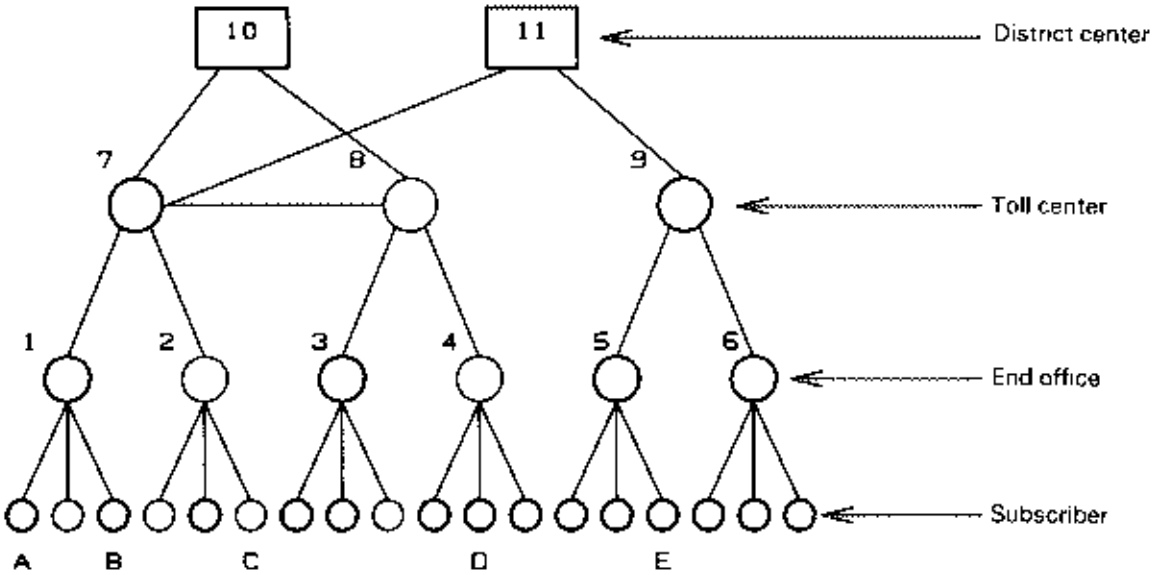


Fig. 3-46 Network Structure Example

The following table lists some possible connections:

Table 3-10 Network Connection Routing

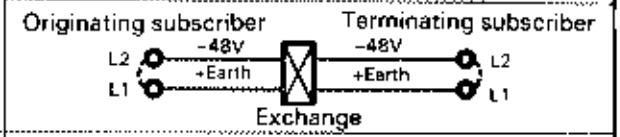
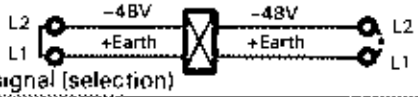
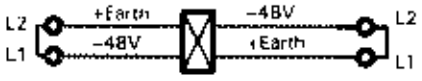
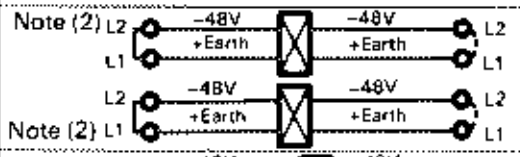
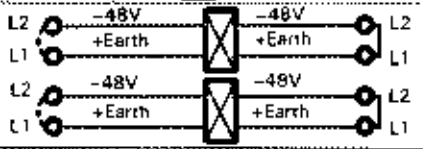
Subscribers	Possible connection route
A → B	A → 1 → b
A → C	A → 1 → 7 → 2 → C
A → D	A → 1 → 7 → 8 → 4 → D, A → 7 → 10 → 8 → 4 → D
A → E	A → 1 → 7 → 11 → 9 → 5 → E, A → 1 → 7 → 10 → 11 → 9 → 5 → E, A → 1 → 7 → 8 → 10 → 11 → 9 → 5 → E
D → C	D → 4 → 8 → 7 → 2 → C, D → 4 → 8 → 10 → 7 → 2 → C

As the above table clarifies, the same two subscribers may be connected through different routes. A route is normally established through the minimum links. When lines, which satisfies this principle, are occupied, however, other lines requiring more links but fewer than the others are selected to complete the channel. The more links there are between the two subscribers, however, the more the transmission loss grows which is reflected as an unnegligible attenuation of the signal. Thus, restrictions are generally imposed on the maximum links, etc.

(2) Telephone line operations

Table 3-11 shows a general sequence of line state changes that occur during a telephone line communication since the call until the end of communication through a data communications. The line voltages, polarity, etc. may ary depending on type of exchange.

Table 3-11 Line Selection (Connection)

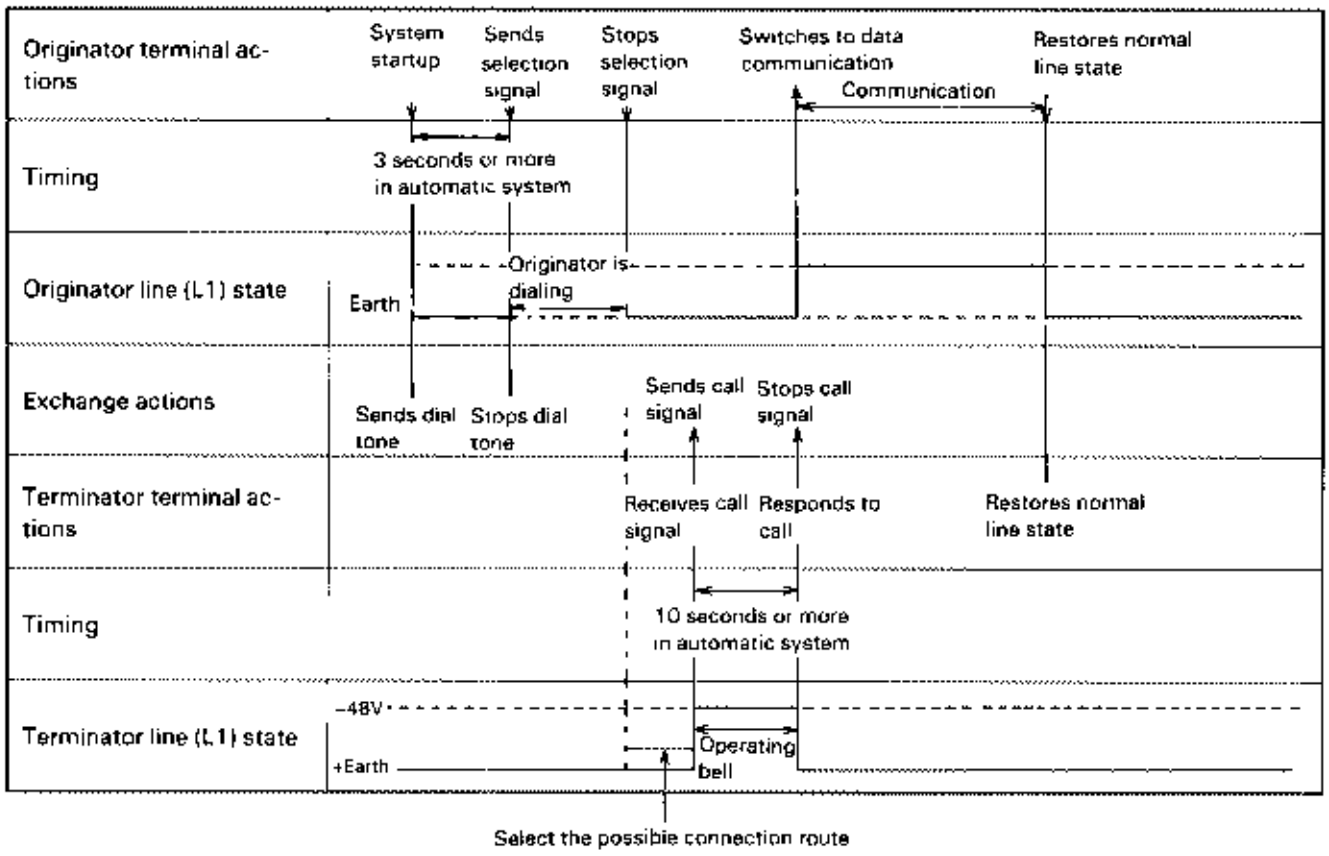
State of terminal	Exhange action	State of line
① Normal	Monitors state of terminals.	
② Originator handset is unhooked. (Loop closes)	Exchange is activated. Sends dial tone to originator	
③ Sends out dial signal (selection signal).	Exchange is activated. Selects outgoing line.	
④ Terminator is being called.	Completes outgoing line selection. Seizes terminator. Reverses polarity and sends out call signal. Sends ringing tone to originator.	
⑤ Terminator unhooks handset. ⑥ Both subscriber initate communication.	Response to terminator. Restores original polarity and stops call signal. Actions to originator. Reverses polarity and stops ringing tone.	
⑦ End of communication: Originator hooks handset. Terminator hooks handset.	Restores all trains.	
⑦ End of communication: Originator leaves handset unhooked. Terminator hooks handset.	Leaves all trains activated and restores only terminator trains after a certain time interval elapses.	
⑦ End of communication: Originator hooks handset. Terminator leaves handset unhooked.	Restores only originator trains and restores part of terminator trains after a certain time interval elapses.	

Note (1) ↑ indicates that the handset is hooked (ON)
↓ indicates that the handset is unhooked (OFF)
(2) The originator line polarity remains unchanged in toll call

The above table includes the actions of the option unit; the handset is unhooked by the user and the unit sends out the dial signal. The timing of all the line connection action and state changes included in the above table is shown in table 3-12.

(Telephone line connection timing)

Table 3-12 Line Selection (connection)



General precautions on using telephone lines

Problems such as line noises and signal attenuation must always be taken into consideration when using a telephone line. These problems may sometimes cause communication failures or errors which cannot be attributed to the equipment including this Modem-unit. When any of such problems occurs, the following should be practiced:

① Once disconnect the telephone line (hook the handset) and then dial the other station again. This changes the connection route.

② Examine whether the communication procedure contains error recovery capabilities such as transmission retry, etc. and how do the tow stations shake hands.

(3) Modem-unit connection to a telephone line

This option unit has three connectors which are used as illustrated in fig. 3-47. The following precautions should be used before connecting the unit to the telephone line:

1. The unit cannot be connected simultaneously to an acoustic coupler and a telephone line. Either one must be selected.
2. The unit and the Main Frame RS-232C must not be simutaneously used.
3. When the handset is connected, it must not operate together with the acoustic coupler or telephone line.

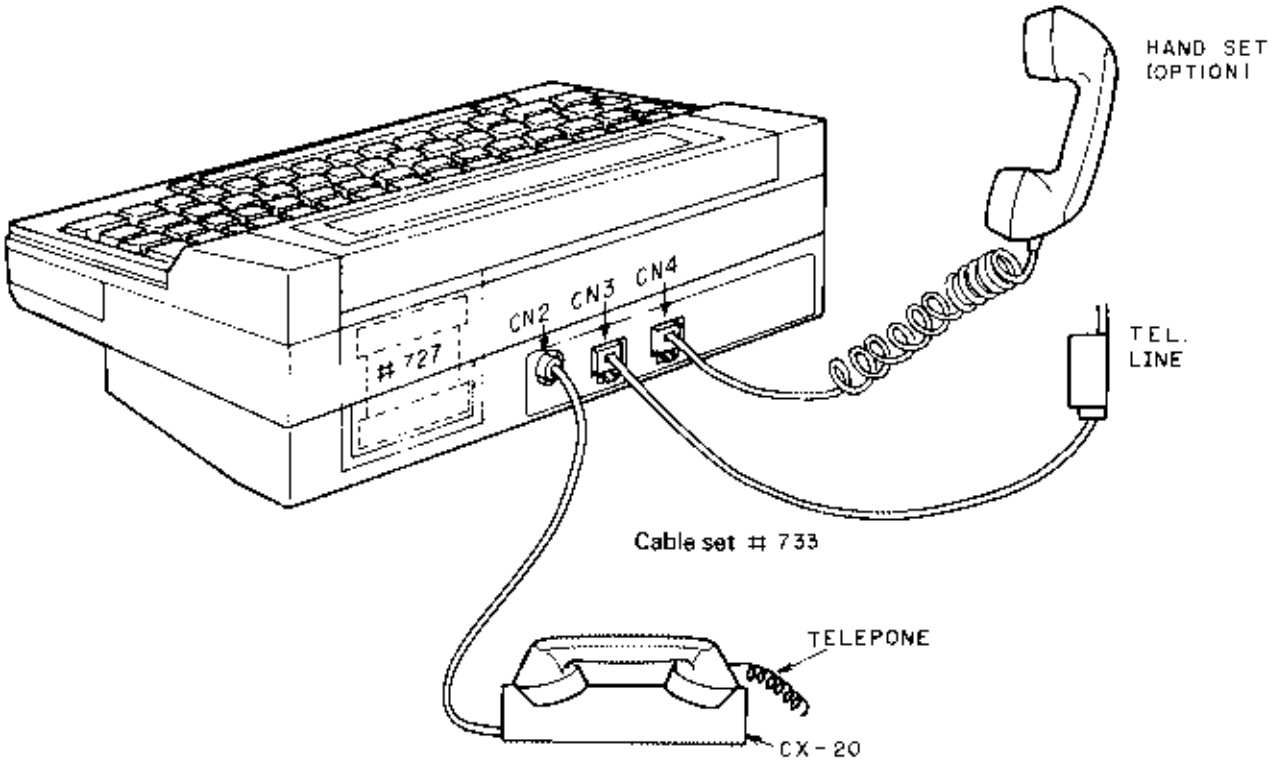


Fig. 3-47 Modem-Unit Connection to Telephone Line

(4) Transmission mode (line signals)

This Modem-unit allows two-line full duplex frequency shift keying (FSK) data communications at up to 300 bps. The two carriers of high and low groups, which are shown in table 3-13, are available.

Table 3-13 Available carriers

Mode	Group	Line frequency (Hz) (BELL/CCITT)	Mark/space
ANS	Low	1270/980	Mark
		1070/1180	Space
ORG	High	2225/1650	Mark
		2025/1850	Space

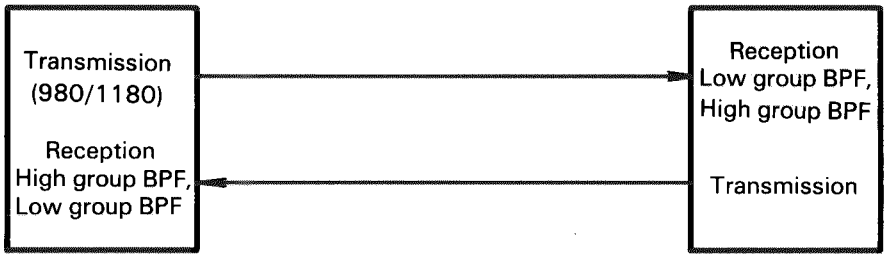
The ORG and ANS modes can be selected by software. The lines operate in the two modes as shown in table 3-14.

Table 3-14 Line Frequencies

Mode	Transmission (line frequency)	Reception (line frequency)
ANS	High group (1650/1850Hz)	Low group (980/1180Hz)
ORG	Low group (980/1180Hz)	High group (1650/1850Hz)

As the table 3-15 indicates, the mode opposite to the other station must be selected.

Table 3-15



*BPF;BAND PASS FILTER

Mode selection

Generally, the calling (dialing) station selects the "ORG" mode and the called station selects the "ANS" mode. In a system which used a center machine, generally the terminal selects the "ORG" mode and the center modem selects the "ANS" mode.

3.3.2 Major Modem-Unit Circuit Elements

The Modem-unit consists of a control board named MAP-MD and top and bottom casing parts. Fig. 3-48 shows the MAP-MD board and table 3-16 lists major circuit component elements mounted on the board.

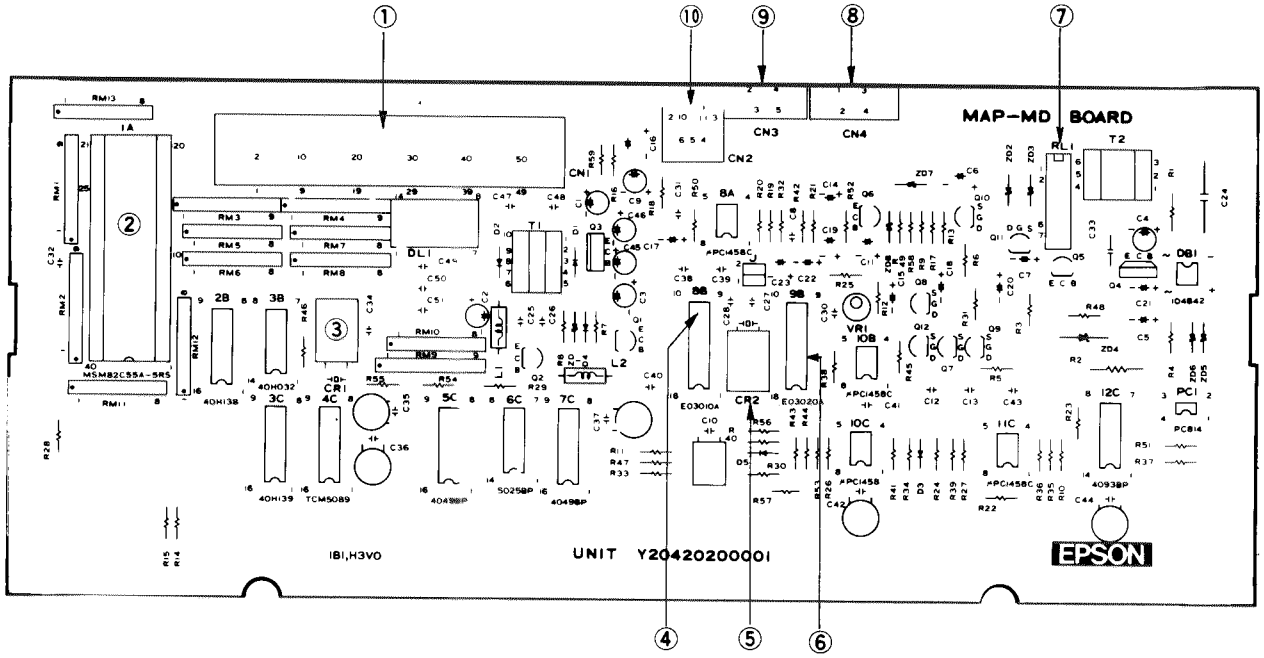


Fig. 3-48

Table 3-16 Major Circuit Component

No.	Name	Function	No.	Name	Function
1	CN1	Bus interface with Main Frame	2	82C55	Modem CPU
3	CR1	3.579594 MHz	4	E03010A	Modulator IC
5	CR2	4 MHz	6	E03020A	Filter IC
7	RL1	Switching	8	CN4	Interface for handset
9	CN3	Interface for telephone line	10	CN2	Interface for acoustic coupler

3.3.3 Function Circuit Blocks

As shown in fig. 3-49, the MAP-MD board consists of a power supply (DC-DC converter) section (1), a telephone line interface (2), a handset interface (3), a coupler interface (4), a tone generator (5), a filter section (6), a modulator/demodulator section (7), a speaker amplifier (8), an addess decoder section (9), and a parallel controller (10). The unit operations are accomplished through a read/write from the Main Frame CPU using the I/O address that is assigned to this unit.

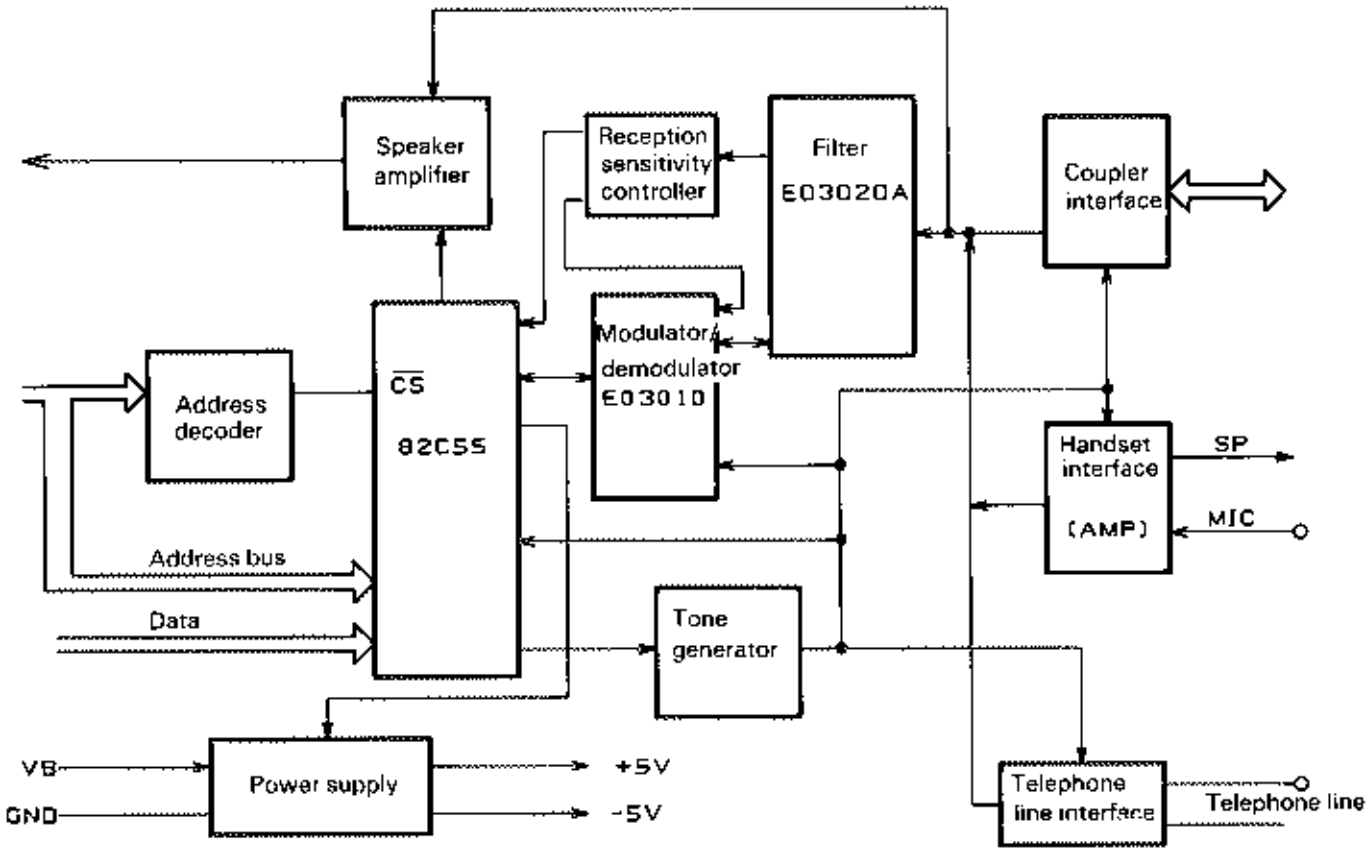


Fig. 3-49 Modem Unit Funtional Circuit Block Diagram

The filter and modulator/demodulator elements are the same as those used in the coupler CX-20/21. Many operational amplifiers and static couplings characterize this unit. Static couplings allows the use of FET elements which can minimize switchiong noises (switching noise reduction is essential to clear a restriction imposed by FCC).

3.3.4 Interface Signals Modem

The unit is connected to the Main Frame through connector CN1. The Main Frame interface provides many signals for universal application. However, this unit used only a part of them. Table 3-17 lists the Modem unit interface signals.

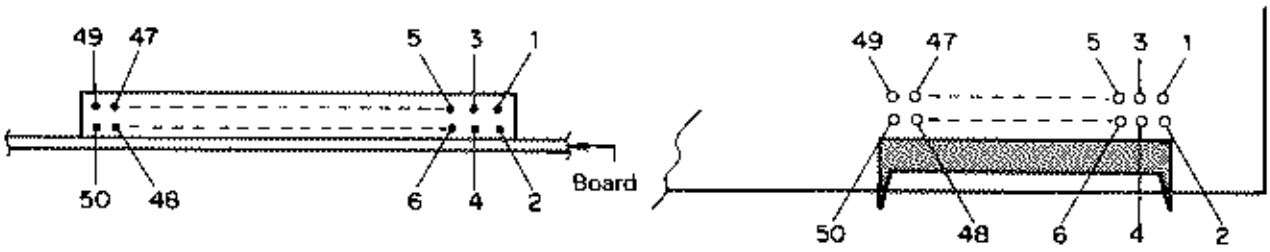


Table 3-17 Modem unit interface signals

Connection pin No.	Signal name	Input/Output	Function	Connection pin No.	Signal name	Input/Output	Function
1	—	—	Not used	26	—	—	Not used
2	—	—	Not used	27	—	—	Not used
3	—	—	Not used	28	—	—	Not used
4	—	—	Not used	29	VL	Input	Logic circuit voltage
5	AB1	Input	Address bus line 1	30	—	—	Not used
6	AB2	Input	Address bus line 2	31	GND	—	Signal ground
7	—	—	Not used	32	GND	—	Signal ground
8	AB0	Input	Address bus line 0	33	$\overline{RS}$	Input	Reset signal
9	AB4	Input	Address bus line 4	34	SPI	Output	Speaker output signal
10	AB3	Input	Address bus line 3	35	$\overline{RD}$	Input	Read-signal
11	AB6	Input	Address bus line 6	36	—	—	Not used
12	AB5	Input	Address bus line 5	37	$\overline{WR}$	Input	Write signal
13	—	—	Not used	38	-	—	Not used
14	AB7	Input	Address bus line 7	39	—	—	Not used
15	—	—	Not used	40	$\overline{IORQ}$	Input	I/O Request signal
16	—	—	Not used	41	—	—	Not used
17	DB0	Input/Output	Data bus line 0	42	—	—	Not used
18	DB1	Input/Output	Data bus line 1	43	—	—	Not used
19	DB2	Input/Output	Data bus line 2	44	—	—	Not used
20	DB3	Input/Output	Data bus line 3	45	RX-$\overline{D}$	Output	Receive data
21	DB4	Input/Output	Data bus line 4	46	$\overline{TX\text{-}D}$	Input	Transmit data
22	DB5	Input/Output	Data bus line 5	47	VB1	Input	Battery voltage
23	DB6	Input/Output	Data bus line 6	48	—	—	Not used
24	DB7	Input/Output	Data bus line 7	49	—	—	Not used
25	-	—	Not used	50	—	—	Not used

(Option Unit Side)

Acoutic coupler interface (CN2)

This is the interface used to an otional acoustic coupler.

Connector The coupler must be terminated with the connector plug HSJ0863-01-420 (HOSHI-DEN) which mates with the interface jack.

Interface signals

The following table 3-18 lists the coupler interface signals:

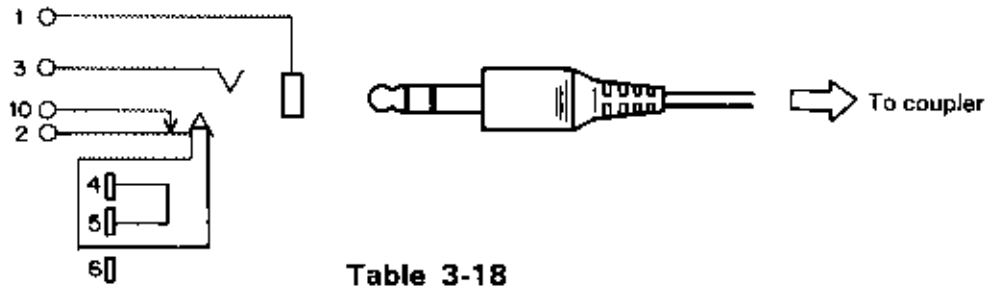
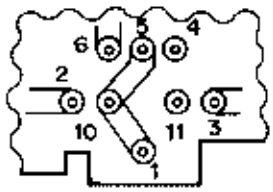


Table 3-18

Pin No.	Signal name	Input/output	Function
1	GND	—	Signal ground
2	ACMI	Input	Input analog signal
3	ACSP	Output	Output analog signal
4	GND	—	Signal ground
5	SWNC	—	Grounded when not connected
6	SWNO	—	Grounded when not connected
10	GND	—	Signal ground



(Soldering side)

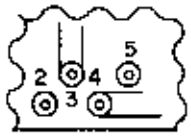
Telephone line interface (CN3)

Interface signals

The following table 3-19 lists the telephone line interface signals:

Table 3-19

Pin No.	Signal name	Input/output	Function
2	—	—	Not used
3	RING	Input	Ring detection (16 ~ 68 Hz)
4	TIP	Output	
5	—	—	Not used



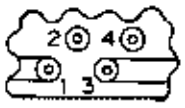
(Soldering side)

Handset interface (CN4)

The following table 3-20 lists the handset interface signals:

Table 3-20

Pin No.	Signal name	Input/output	Function
1	HSMI	Input	Signal input (MO)
2	GND	—	Signal ground
3	HSSP	Output	Signal out (SP)
4	GND	—	Signal ground



(Soldering side)

3.3.5 Power Supply Circuit

This option unit is powered by the Main Frame main battery; the battery voltage VB1 and the logic circuit voltage VL supply through the interface. The unit generates +5 V and –5 V sources, which are supplied to various IC elements. Fig. 3-50 shows the power supply circuit.

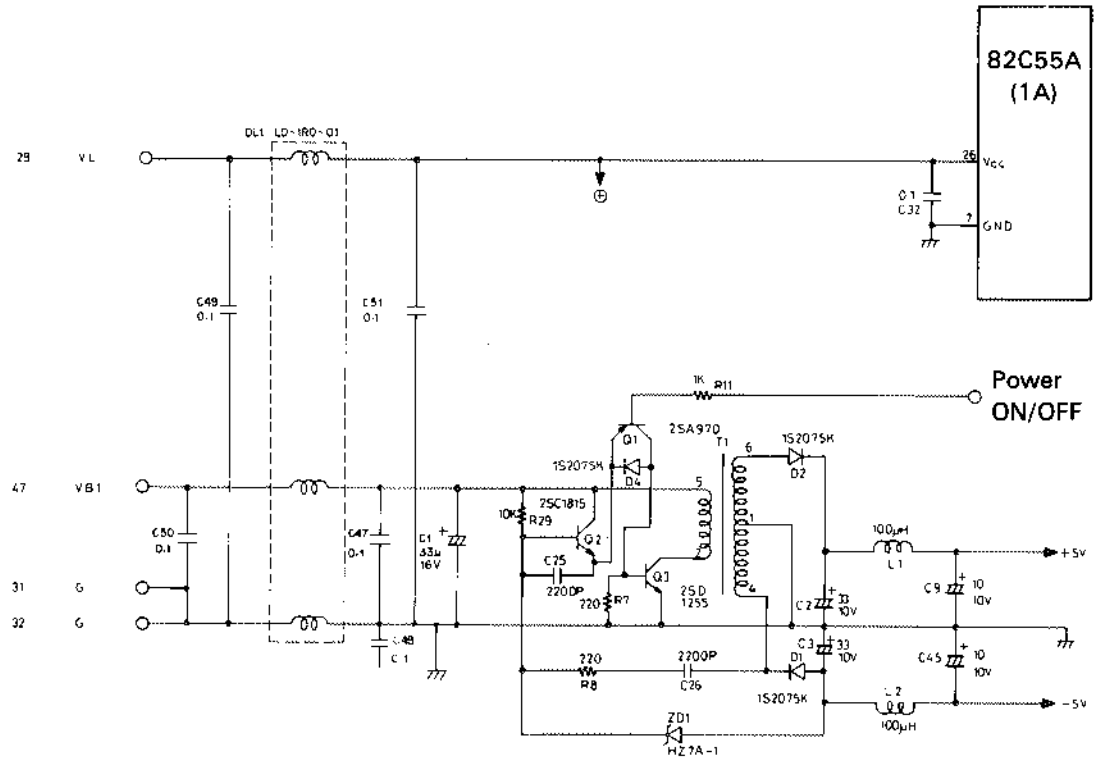


Fig. 3-50 Modem Unit Power Supply Circuit

Four power lines are used in the unit which are respectively distributed to specific elements as listed in table 3-21.

Table 3-21 Power Sources

Power Line	Functions	Use
VL	Circuit voltage output of Main Frame	Battery voltage output of Main Frame
VB1	Power supply for IC '1A' (82C55A) and '2B' (40H138)	Power supply for RL1, +5V and –5V regulators
+5V	Voltage generated by VB1	Power supply for ICs other than '1A' and '2B'
–5V	Voltage generated by VB1	IC (Filter IC)

The ±5 V supply regulator circuit can be enabled and disabled by Main Frame software so that powr consumption can be minimized.

- When Main Frame is off, only VB1 is supplied to this unit because VL (the Main Frame circuit voltage supply) is off. The ±5 V regulator to which VB1 is supplied contains switching circuits using IC '1A'. When Main Frame is off, the switching circuits are maintained in the cut off condtion so that no current other than the leak through the regulatorcircuit elements flows.
- When this unit is not being used (no data transmittion/reception is in progress) though Main Frame is on, the circuit is in a standby condition where the required minimum elements need to be maintained active so that the unit can immediately start operating at any time. To accomplish this,the Main Frame circuit voltage (VL) is supplied to the address decoder (IC 2B) and parallel controller (IC 1A) so that the parallel controller can be accessed for both read and write in the standby condition. This enables line monitoring and internal power control, etc.
- Before this unit can be used for data transmission/reception, the driving bias voltage must be supplied to the filter IC (9B), the modulator/demodulator IC (8B), and the Tone generator IC (4C), etc. to actiate them. This internal power supply control is implemented by the Main Frame program.

Table 3-22 lists the current requirements of the Modem unit in the various modes:

Table 3-22 Current Requirement

No.	Operation Mode	Current Requirement	
		TYPICAL	MAX.
1	Main Frame power off	3μA	10μA
2	Modem not in use with Main Frame on	0.4mA	1mA
3	Both Main Frame and modem power on but not connected to line	50mA	60mA
4	Both Main Frame and modem power on and modem is connected to line	65mA	80mA

(1) ±5 V supply regulator circuit operation

This circuit contains an oscillator circuit formed by a feecback through resistor R8 and capacitor C26 whose output is used as the swiching signal for a DC-DC conversion. Fig. 3-51 is a circuit diagram of the supply circuit.

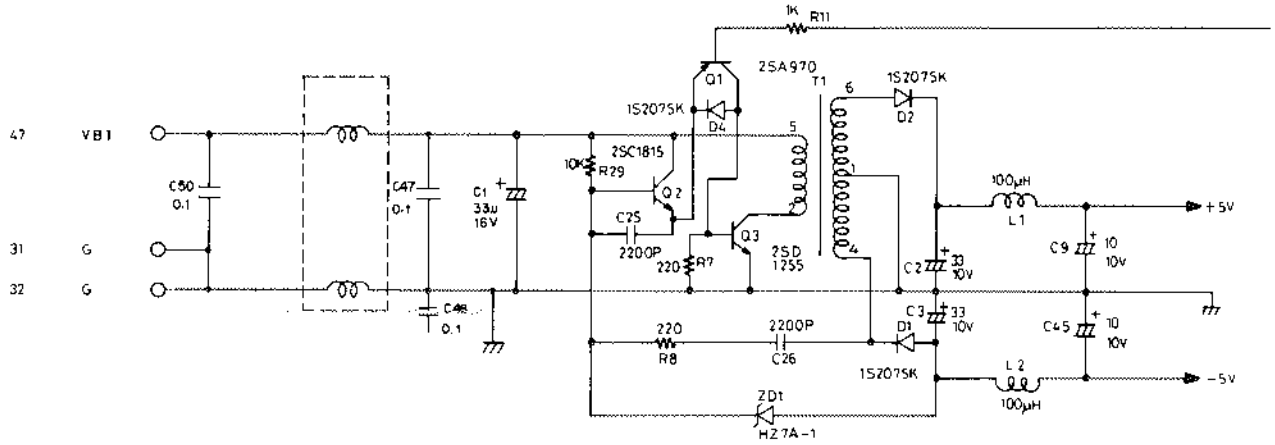


Fig. 3-51 Modem unit ±5 V supply circuit

This circuit is contrlled by the signal supplied to the base of transistor Q1 from the 82C55 PB2 terminal. This signal is controlled via bit 6 of I/O address 85H as follows as stated in the description on the Address Control circuit:

PB2 output signal { Low – enables the regulator. / High – disables the regulator.

DC-DC conversion

When PB2 of IC '1A' (82C55) rises high, transistor Q1 turns on. This causes the emitter of Q1 to go low because the collector is connected to ground via resistor R7 (220 ohms).

Thus, transistor Q2 also turns on due to the forward potential difference generated across its base and emitter. When Q2 start conducting, the emitter potential rises toward the VB1 voltage supplied to the collector. Thus, there is soon nearly no potential difference between the base and emitter and Q2 is cut off. When Q2 is in conduction, the low emitter voltage is supplied to the base of transistor Q3 through Q1. Thus, the forward pottential difference across the base and emitter also turns the transistor on. This closes the current path through the primary winding of transformer T1. The current flows only for an instant while Q2 is in conduction.

This current induces a voltage across the secondary winding.

This voltage is halfwave-rectified by diodes D1 and D2 and then respectively filetered through an LC circuit. The filtered outputs are supplied to the ±5 V lines. the negative voltage, which appears at the cathode of D1 is also fed back to Q2 through resistor R8 and capacitor C26 all of which form a phase shift oscillator loop together with Q3, C25, R7, and T1.

This feedback accelerates the switching of Q2 which is further intensified by Q3 so that the oscillation is maintained at the following frequency determined by the circuit time constant, as long as the 82C55 PB2 signal is low:

- The ±5 V output voltages are regulated constant by moitoring the potential difference between the –5 V line the base of Q2.
  If the line voltage falls too low (i.e., the absolute value rises too high), the switching is suppressed.
- The signal waveforms at various points are shown in the Fig. 3-52 to Fig. 3-56.

Base of Q2

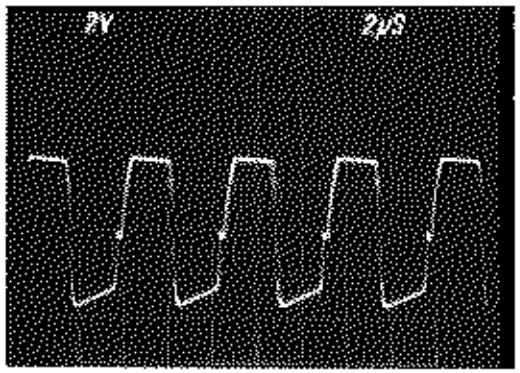


Fig. 3-52

Emitter of Q2

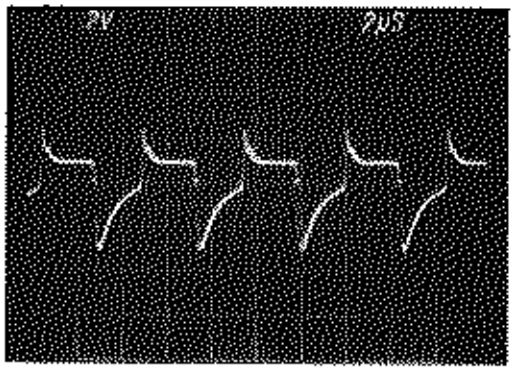


Fig. 3-53

Collector of Q1

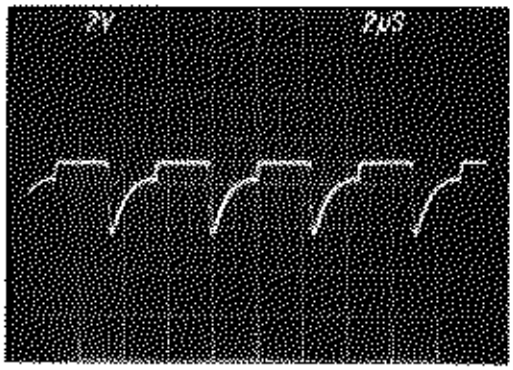


Fig. 3-54

Collector of Q3

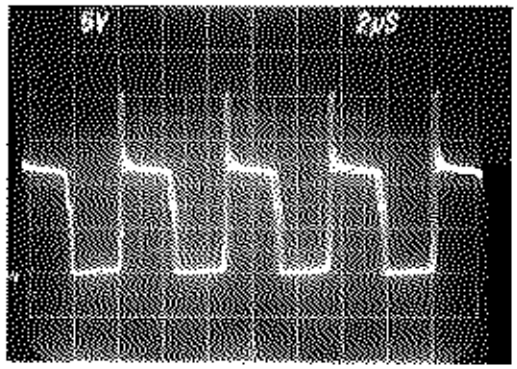


Fig. 3-55

Anode of D1

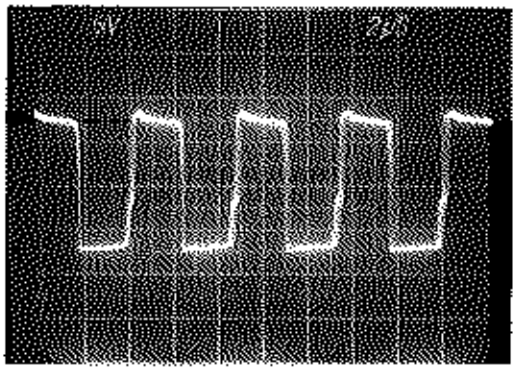


Fig. 3-56

3.3.6 Reset Signal ($\overline{RS}$)

The Reset signal is supplied from IC '6A' on the MAPLE board and activated low when Main Frame power is turned on or the Reset switch is pushed. Fig. 3-57 shows the Reset signal circuit.

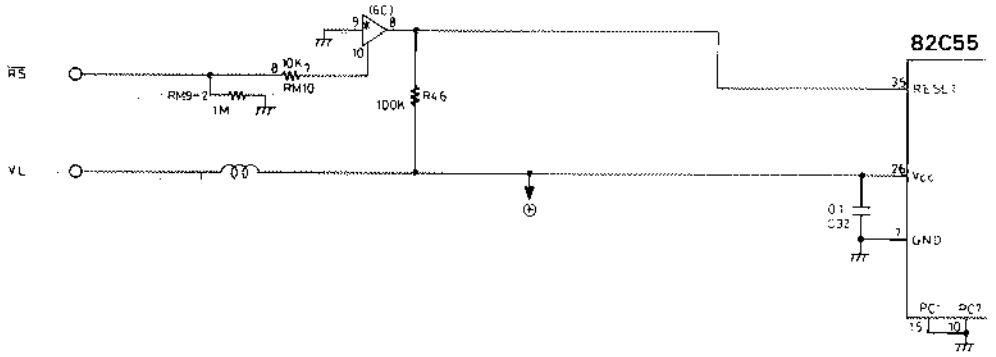


Fig. 3-57 Reset Signal Circuit

While the $\overline{RS}$ signal line is low, the gate input of IC '6C' (pin 10) is maintained deactivated and the RESET input of 82C55 is pulled up to the VL line through resistor R46, resetting the IC. This initializes all the 82C55 ports to the input mode (the high impedance state). When the $\overline{RS}$ signal returns high, the input of IC '6C' (pin 10) goes high, the output of IC'6C' (pin 8) goes Low, removing the resetting state from 82C55.

3.3.7 Address Control Circuit

This Modem unit is controlled as an I/O device by the Main Frame CPU (Z-80) on the MAPLE board. This control is accomplished through the IC 2B and address line A0/1. Four I/O addresses are provided for the 82C55 internal control for this purpose. Fig. 3-58 shows the Address Control circuit.

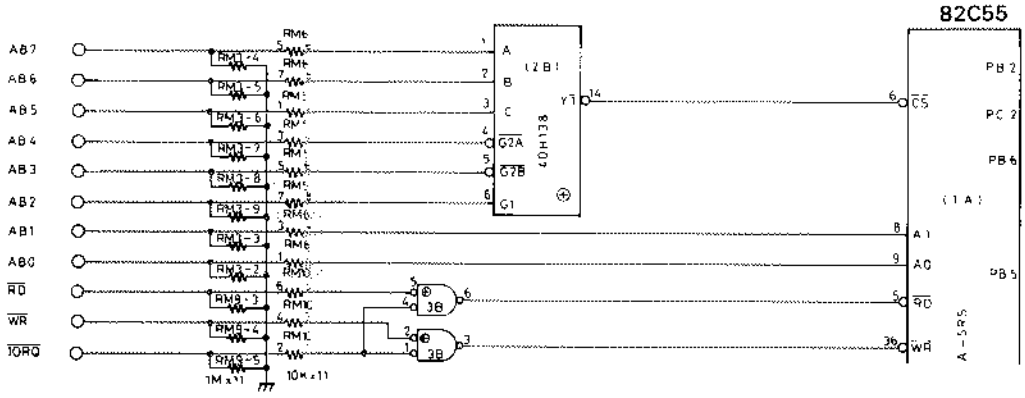


Fig. 3-58 Address Control Circuit

Circuit operation

Address bits 0 through 7 are used for this control. Bits-2 through 7 (which are decoded to the Chip Select signal) select 82C55 and bits 0 and 1 selects an internal port register A, B, or C, or the control register. Bits 2 through 7 are decoded to the 40HB8 and used to $\overline{CS}$ signal control for 82C55.

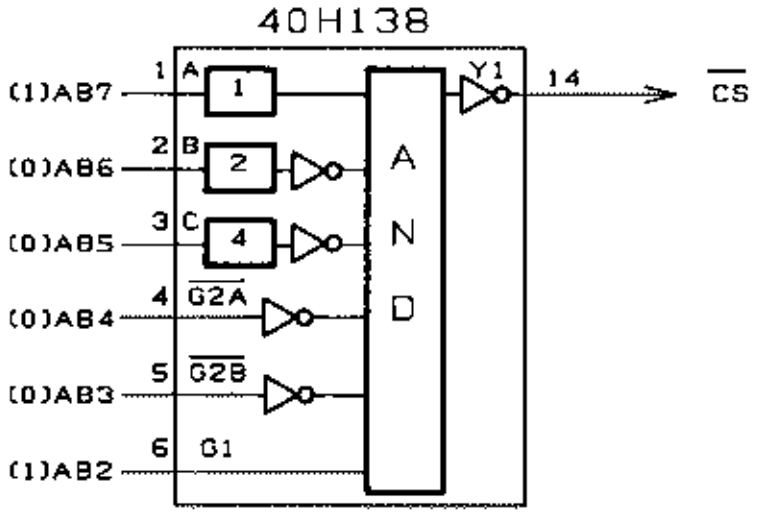


Fig. 3-59 Chip Select Signal Decoder Circuit

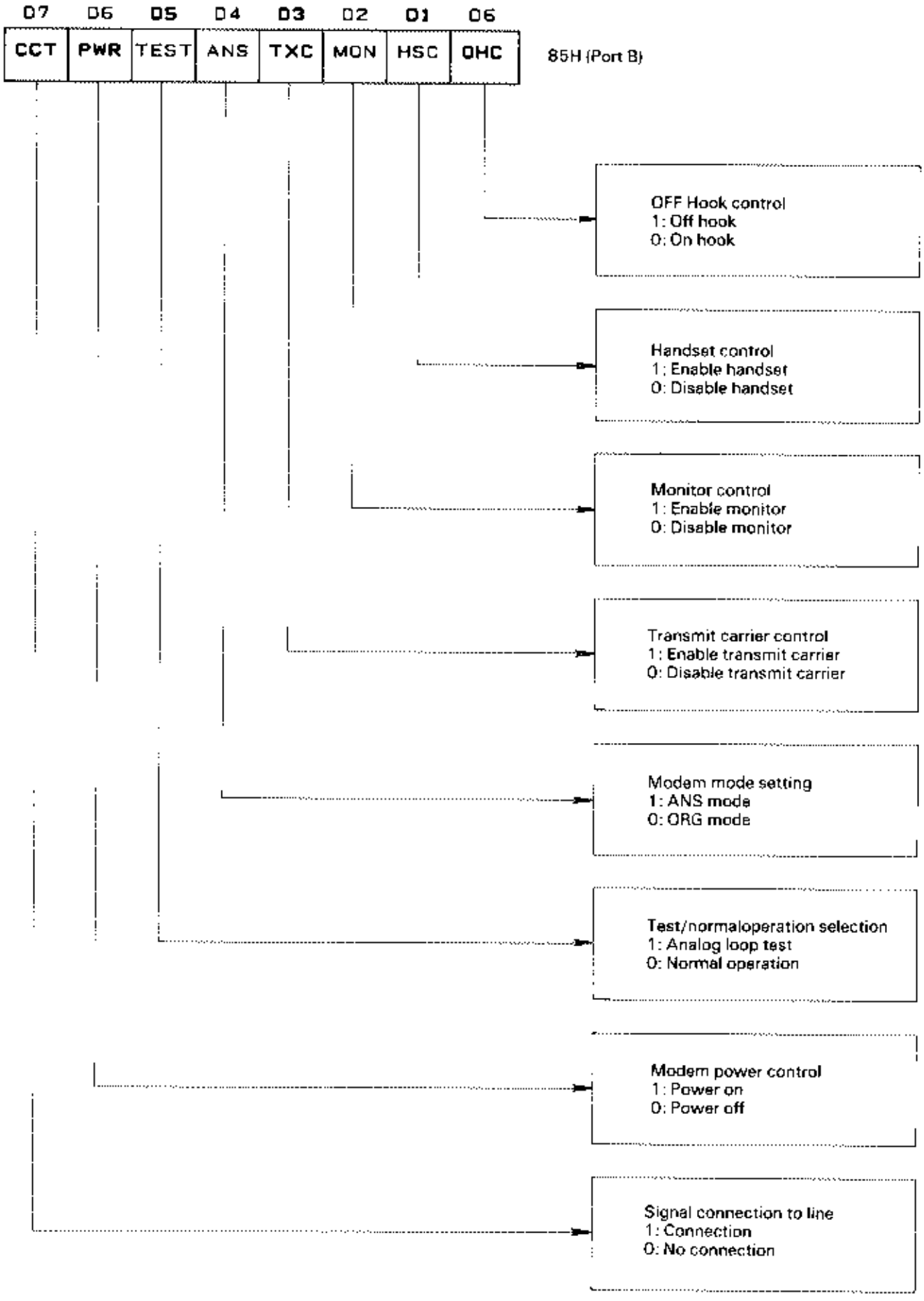
As obvious from the circuit, the CS signal is activated low for addresses 84H through 87H; address bits 2 and 7 should be "1" and the rest should be "0".

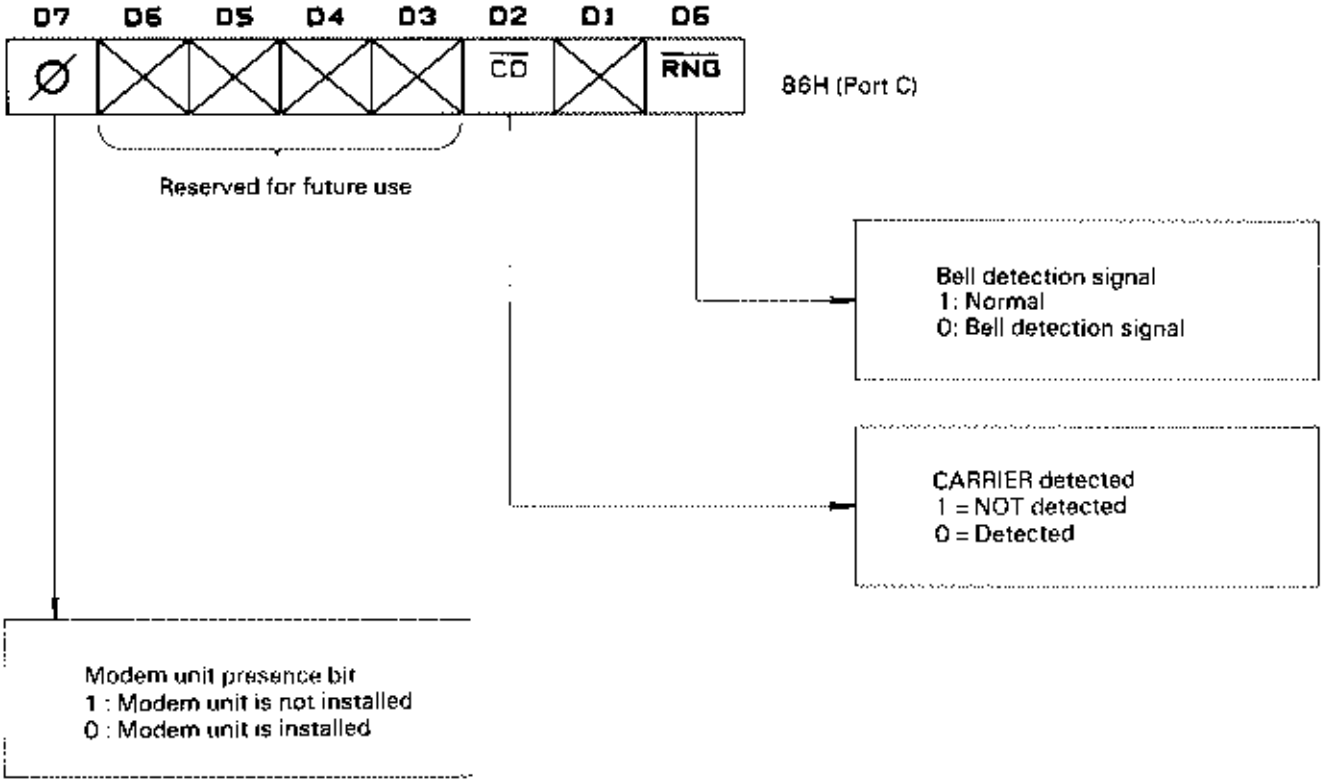
Address bits 0 and 1, which are combined to allow access to four different functions (84H – 87H), are directly fed to 82C55.

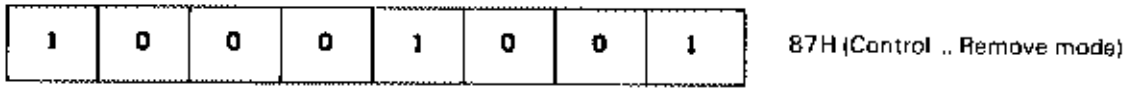
Table 3-23 lists the possible address bit configurations and accessed functions.

Table 3-23 I/O Addresses for Modem Unit Functions

Address (hex.)	A7	A6	A5	A4	A3	A2	A1	A0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	82C55 internal operation	Function
84	1	0	0	0	0	1	0	0	0	1	0	Not used	–
84	1	0	0	0	0	1	0	0	1	0	0	Data bus → Port A	Tone dialer control
85	1	0	0	0	0	1	0	1	0	1	0	Not used	–
85	1	0	0	0	0	1	0	1	1	0	0	Data bus → Control	Modem control
86	1	0	0	0	0	1	1	0	0	1	0	Port C → Data bus	Modem status read
86	1	0	0	0	0	1	1	0	1	0	0	Not used	–
87	1	0	0	0	0	1	1	1	0	1	0	Not used	–
87	1	0	0	0	0	1	1	1	1	0	0	Data bus → Control	82C55 mode selection


D7 D6 D5 D4 D3 D2 D1 D6
CCT PWR TEST ANS TXC MON HSC OHC
85H (Port B)
OFF Hook control
1: Off hook
0: On hook
Handset control
1: Enable handset
0: Disable handset
Monitor control
1: Enable monitor
0: Disable monitor
Transmit carrier control
1: Enable transmit carrier
0: Disable transmit carrier
Modem mode setting
1: ANS mode
0: ORG mode
Test/normaloperation selection
1: Analog loop test
0: Normal operation
Modem power control
1: Power on
0: Power off
Signal connection to line
1: Connection
0: No connection


D7 D6 D5 D4 D3 D2 D1 D0
Ø
CD
RNG
86H (Port C)
Reserved for future use
Bell detection signal
1: Normal
0: Bell detection signal
CARRIER detected
1 = NOT detected
0 = Detected
Modem unit presence bit
1 : Modem unit is not installed
0 : Modem unit is installed


1 0 0 0 1 0 0 1
87H (Control .. Remove mode)

3.3.8 Connection interface

(1) Acoustic coupler interface (CN2)

- The input signal is supplied to pin 2 (ACMI), then it is pulled up to +5V in the circuit composed of R59, 16, and C46. Consequently, the input signal takes the form based on +5V. The DC of this signals is removed by C15, and the signal is integrally amplified in IC "2A", then the DC is removed by C17 again. This signal is amplified in IC "8A" again and suplied to the filter IC.

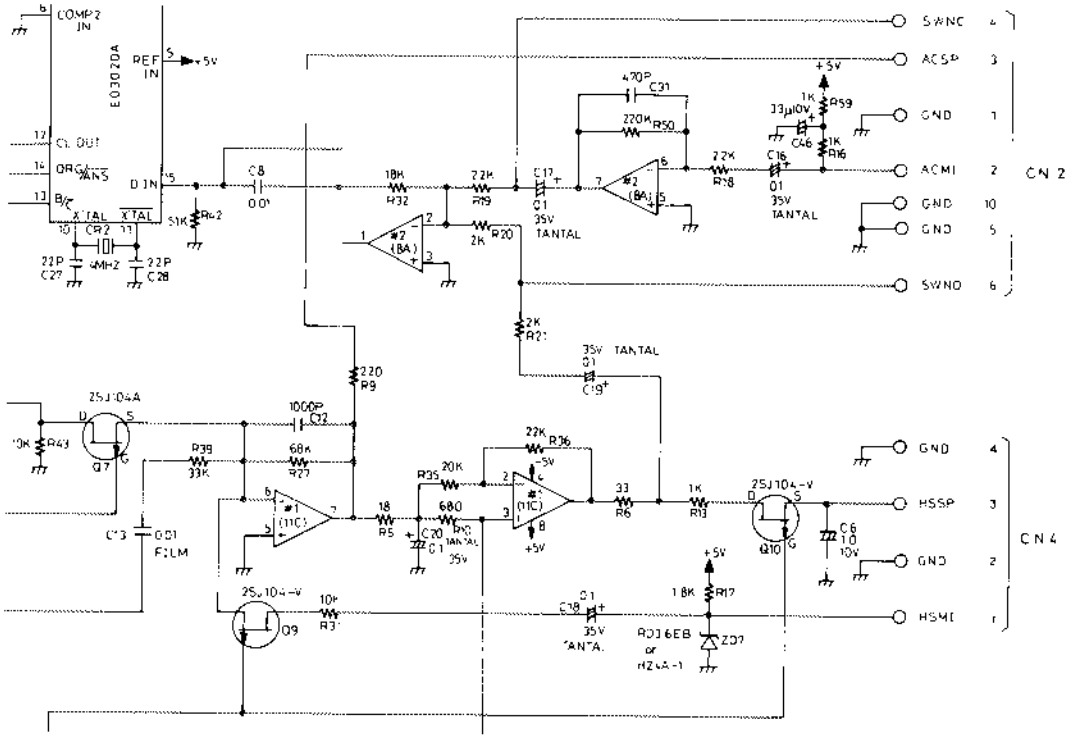


Fig. 3-61

- The output signal outputted from the modem IC is supplied through C10 and R33 to the drain of TrQ7 and integrally amplified in IC "11C" under the condition that the gate is turned on and then outputted to pin 3 (ACSF).
- SWNC sets the output (ACMI) of the acoustic coupler to inoperative state so that the noise from the coupler will not be picked up while using another interface.
- SWNO, contrast with SWNC, is used to prevent the effects of the noise from the other interfaces while using the acoustic coupler.

(2) Hand-set interface (CN4)

- The input signal (HSMI) is pulled up by R17 and its input of high level is cut off by Zener diode ZD7 so that the signals at levels higher than the specification will not supplied to the line. Then, this signal is supplied to pin 6 under the condition that the gate of TrQ9 is turned on (PB7 control of 82C55), where it is integrally amplified and supplied through R5 and 10 to the telephone line interface.
- The output signal from the telephone line interface is supplied to pin 3 of IC "11C" and amplified and then outputted to the speaker under the condition that the gate of TrQ4 is gate on.

(3) Telephone line interface

This interface is used to connect to the line directly. Therefore, the controller and protective circuit unique to the line are installed as shown in Fig. 3-62.

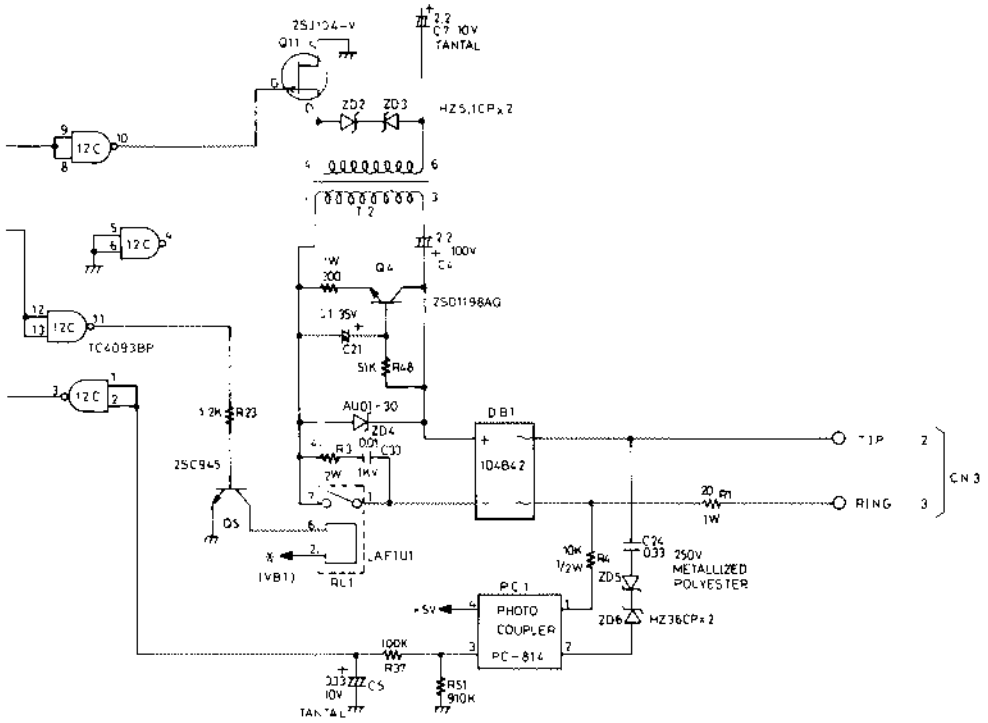
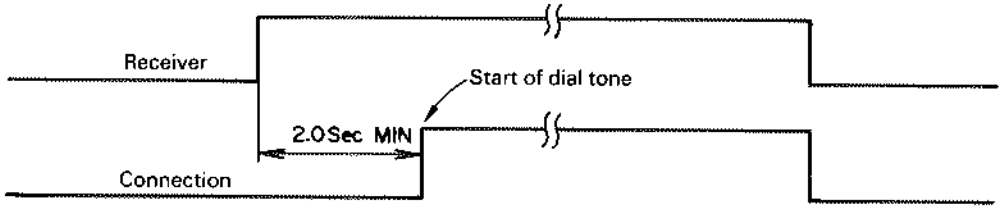


Fig. 3-62

The DC voltage is applied between TIP and RING according to the standard of the telephone line, and the condition of the line also changes according to the operation as explained in Paragraph 4.3.1 (2). The operation of the circuit is explained below.

(Hooking): Operation after the receiver is picked up.



The hooking is the operation performed after the receiver is picked up and the exchanger start the operation until the dial tone is returned. In the circuit, the high level is outputted by IC "1A" to PB0 and TrQ5 is turned on. When TrQ5 is turned on, RL1 operates to make up a closed circuit by connecting DB1, primary side of coil T2, C4, and DB1 on the line. As the result, the dial tone outputted from the exchanger side can be detected.

(Dialing): Sending the tone signal.

This operation is performed to connect to the other party through the exchanger as explained below.

The frequency of tone corresponding to each key is generated using port A of IC "1A". The eight tones shown in Table 3-23 are used. Those are supplied to pin 6 of IC "11C" and amplified and then supplied through capacitor C7 to the secondary side of coil T2. If PB7 of IC "11C" is at high level and TrQ11 is turned on, a closed circuit is made up on the secondary side of coil T2 and a wave is induced on the primary coil according to the input frequency (tone) and outputted to the line.

The frequencies of the tones generated are shown in Table 3-24 and the output frequencies corresponding to the keys are in Table 3-25.

Table 3-24

	Standard DTMF	Tone output	Deviation from standard
f_1	697	701.3	+0.62
f_2	70	771.4	+0.19
f_3	852	857.2	+0.61
f_4	941	935.1	–0.63
f_5	1209	1215.9	+0.57
f_6	1336	1331.7	–0.32
f_7	1477	1471.9	–0.35
f_8	1633	1645.0	+0.73

Table 3-25

Low group [Hz] \ High group [Hz]	1209	1336	1477
697	1	2	3
770	4	5	6
852	7	8	9
941	*	0	#

Then, the exchanger connect to the terminal of the other party. At this time, the polarity of the line of the other party is inversed to sound the bell. (In this device, the LED's in the photocoupler of PC1 is biased in the normal direction instead of sounding the bell and the signal is outputted to pin 3.)

(Receiving)

When the receiver is picked up, the polarity of the line is returned and the bell sound signal (Calling) from the exchanger is stopped, and the communication is possible. (In this device, instead of picking up the receiver, RL1 is turned on to set the photocoupler for detecting RING to inoperative state by making an open circuit connecting UTIP, DB1, TrQ4, DB1, and RING. In addition, since a current larger than the one in calling state flows through DB1 on the exchanger side the hooking operation on the receiving side is detected and the polarity of the line is returned.) The polarity of the line on the sending side is inverted. The outline of the input circuit and the polarity of the line are shown in Fig. 3-63 and Table 3-26.

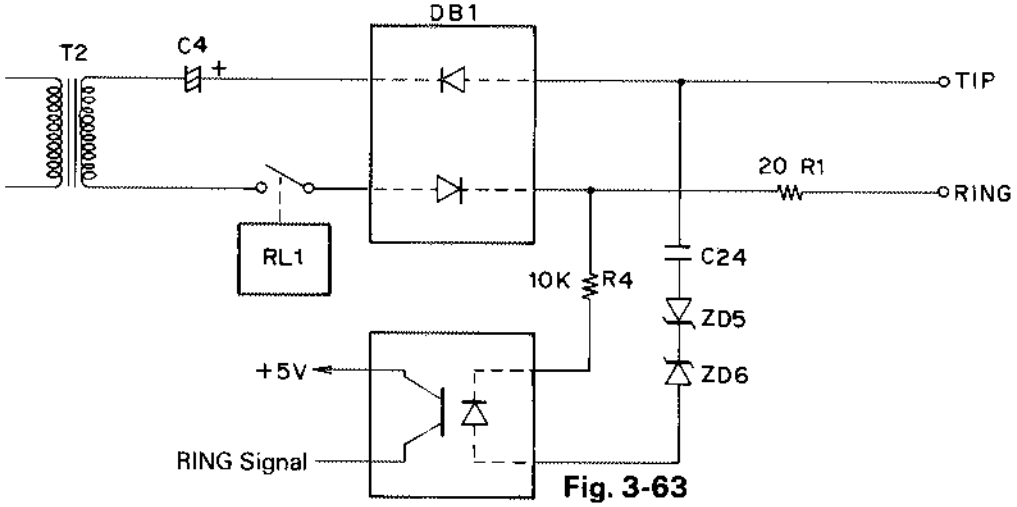


Fig. 3-63

Table 3-26

Sending side			Receiving side		
	Polarity			Polarity	
	TIP	RING		TIP	RING
While not communicating	Negative	GND	While receiving call (bell is sounding)	GND	Negative
While communicating	GND	Negative	While not receiving call	Negative	GND

- Function of each element

  R3 and C33 are installed to protect the contacts of relay RL1 (to prevent arcing) when it is turned off. Zener diode ZD4 removes the surge noise generated in the line. TrQ4 is used as the bypass circuit when receiving the signals, that is, when a call is received and RL1 is turned on, TrQ4 works as if it short-circuits the line with the resistor of 200Ω (R2) (This operation is the same as picking up the receiver), and notifies the exchanger of this condition.

3.3.9 Filter circuit

This unit can use two types of carrier waves (high group and low group) by means of frequency shift keying (FSK). Therefore, the special filter IC for FSK must be used to detect the data (band-passing).

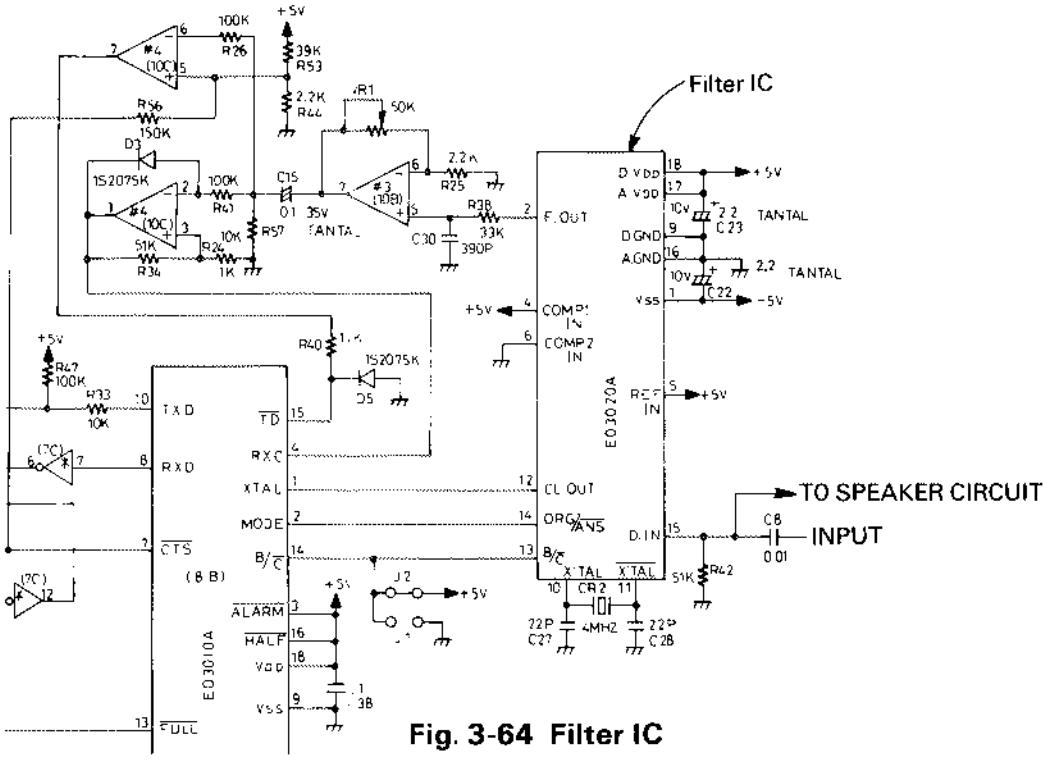


Fig. 3-64 Filter IC

The function block diagram of the filter IC is shown in Fig. 3-65 and the function of signal pin are shown in Table 3-27.

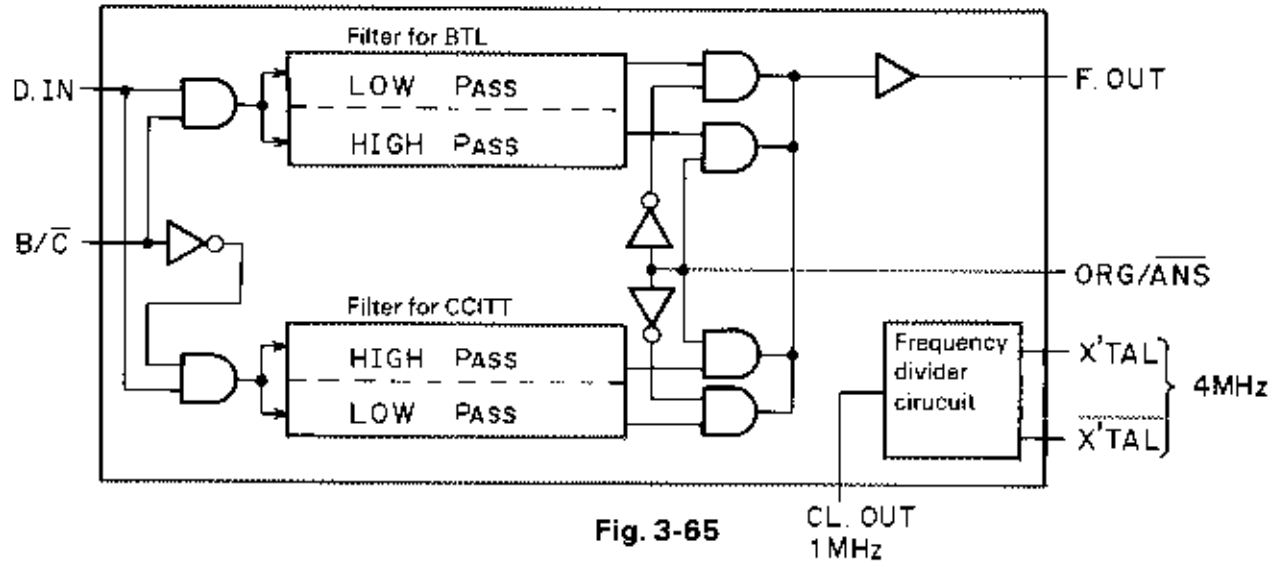


Fig. 3-65

Table 3-27 The Function Signal Pin

Pin No.	Signal Name	Input/ Output	Function
1	Vss	INPUT	Negative voltage
2	F. OUT	OUTPUT	Filter output
3	N.C	—	———
4	COMP1 IN	INPUT	Comparator input for CARRY DET
5	PEF IN	INPUT	Carrier detecting level input
6	COMP2 IN	INPUT	Comparator input for received data output
7	D.OUT	OUTPUT	Received data output (Comparator output)
8	CARRY DET	OUTPUT	Carrier detect
9	D. GND	—	Digital ground
10	X'tal	—	Crystal (4MHz) connecting Terminals
11	$\overline{\text{X'tal}}$		
12	CL.OUT	OUTPUT	1MHz clock output
13	BTL/$\overline{\text{CCITT}}$	INPUT	BTL or $\overline{\text{CCITT}}$ standard select terminal
14	ORG/$\overline{\text{ANS}}$	INPUT	Originate or answer mode select terminal
15	D. IN	INPUT	Receiving data input (Filter input)
16	A. GND	—	Analog ground
17	D. VDD (+V)	INPUT	Digital positive voltage
18	A. VDD (+V)	INPUT	Analog positive voltage

There are four band-pass filters (high group and low group of BTL and high group and low group of CCITT) installed functionally in the filter circuit, and each filter takes out a certain frequency element from the line. Since only the line frequency sent from the connected party is detected, it is necessary to select one from the four band-pass filters in advance. This operation is started by signals B/$\overline{C}$ and ORG/$\overline{ANS}$. The filter circuit selection logic based on Fig. 3-65 is shown below.

Table 3-28

B/$\overline{C}$ \ ORG/$\overline{ANS}$	HIGH (ORG)	LOW (ANS)
HIGH (BTL)	High group (2225 ~ 2025 Hz)	Low group (1270 ~ 980 Hz)
LOW (CCITT)	High group (1650 ~ 1850 Hz)	Low group (1070 ~ 1180 Hz)

On the other hand, the filter circuit has the clock generator function as well as the band-pass filtering function. That is, the clock of 4 MHz generated in a external oscillator is divided by the filter circuit to make the clock of 1 MHz which is supplied to the modem IC (8B).

- Amplifying circuit

  The element of the received signal which has passed the specified band-pass filter is outputted through "F. OUT". Then, the noise in this signal is removed by the low-pass filter which is composed of R38 and C30, and the signal is supplied to IC "10B" and amplified by means of negative feedback:

  $$(Af = \frac{Rx + R25}{R25}$$: Rx is the set resistance of VR1).

  This output is supplied through static coupling capacitor C15 to the two OP amplifiers. (Operation of pins 5 – 7 as OP amplifiers)

  Pins 5 – 7 work as a voltage comparator. The voltage divided by R53 and R44 from +5V

  $$(Vx = 5 \times \frac{2.2}{39 + 2.2}$$ ..... Approx. 0.27V)

  is applied to pin 5 (positive side). This voltage is applied to prevent wrong reaction to noises. While receiving the signals, the input element on the positive side is outputted to pin 7. The theory of this operation is shown in Fig. 3-66.

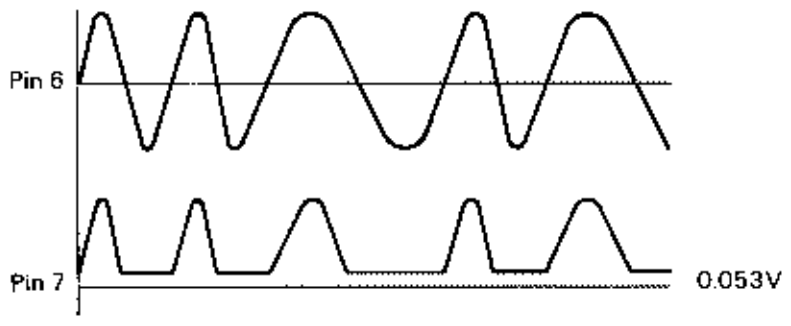


Fig. 3-66

This output is connected through current control resistance R40 and limiter diode D5 for the negative element to $\overline{TD}$ (Threshold Detect) of IC (8B) and used to see if the line is used for communication.

(Operation of pins 1 – 3 as OP amplifiers)

In this circuit, R34 and R24 are used for the positive feedback amplification

$$(Af = \frac{R34 + R24}{R24}),$$

and the positive peak is detected by diode D3. The theory of this operation is shown in Fig. 3-67.

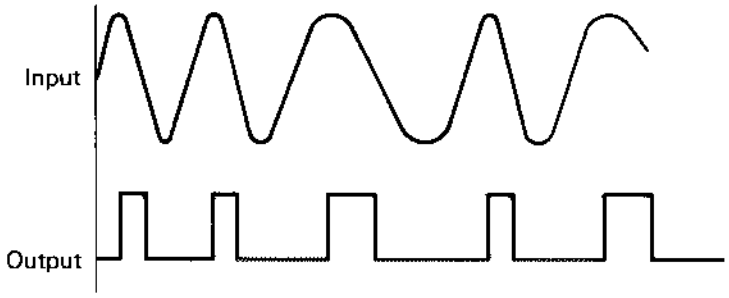


Fig. 3-67

This output is connected R x C (Receive Carrier) of IC "8B" (for modem) and used to detect the data bits.

3.3.10 Modem Circuit

(1) Demodulation circuit

Since the received signal through the filter circuit has undergone frequency modulation, it is converted from the signal frequency into the data bits in this circuit.

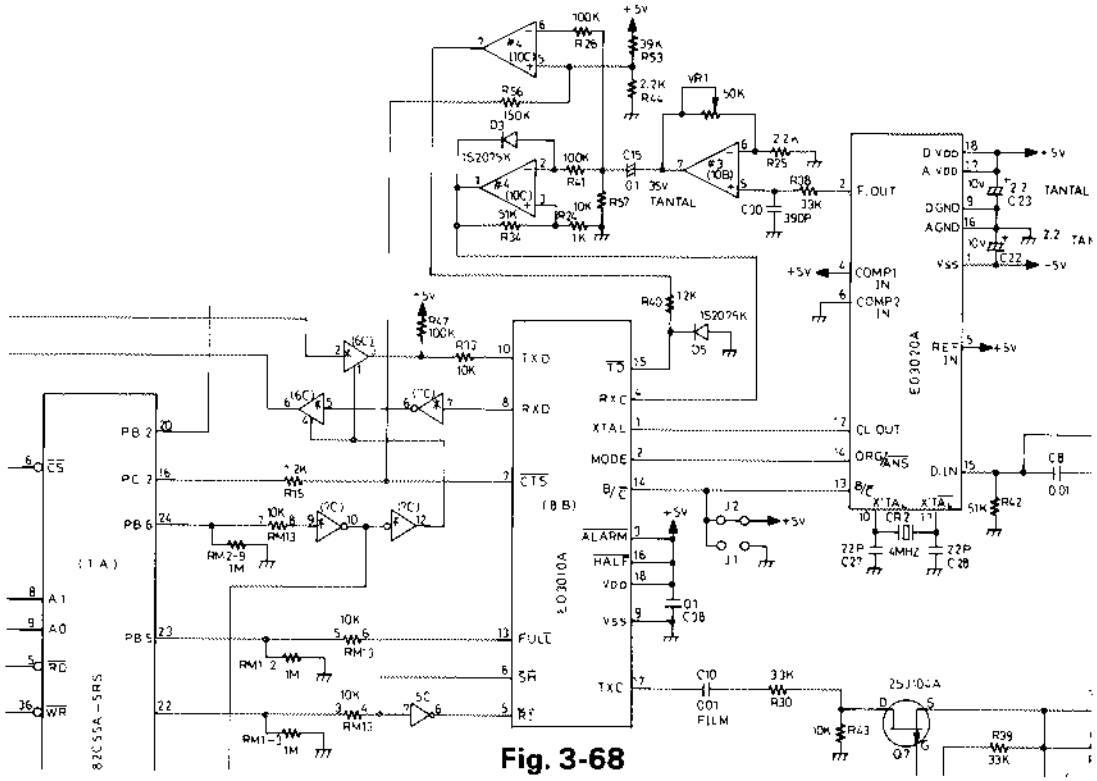


Fig. 3-68

B/$\overline{C}$ signal which is the same as that inputted to the filter circuit is inputted to IC "8B" in the demodulation circuit, and the demodulation is carried out according to this signal. In the circuit, the width of time of input signal "RXC" is measured every half period using the input clock (1 MHz) of pin 1 "XTAL", and the mark and space of the received signal is judged (demodulated) from the measured width of the signal. The result of this judge is outputted to pin 8 "RXD" as two-value signal (High and Low). The mark and space are recognized by seeing if the width of the signal is above the intermediate frequency of the mark and space in each mode (B/$\overline{C}$, high/low group).

(2) Modulation circuit

The two-value signal inputted to transmission data terminal "TXD" is supplied to theclock dividing circuit and used to change the dividing ratio (There is a frequency dividing circuit which generates the line frequency according to each mode using the clock of 1 MHz). As the result, the FSK signal is generated. However, since this signal is a square wave, it is converted to a approximate sine wave in the inside intergration circuit by means of A/D conversion. (The wave actually outputted has a form of stairs.) The DC of the outputted signals is removed by the external static coupling capacitor C10, then the signal is supplied through resistance R30 and TrQ7 to the output amplifying circuit.

(3) Control signal

- Since the $\overline{CTS}$ output line is set to that it will be outputted when the carrier is received by input "RXC" of pin 4, the control signal is used as a "carrier detection" signal. This signal is called so because of the operation of the circuit as CX-20 and has the functions of the following two signals ($\overline{CTS}$ and $\overline{CD}$).

  Fully double: $\overline{CD}$
  Half double : $\overline{CD}$, $\overline{CTS}$

  The $\overline{CTS}$line is also connected through R56 tothe reference input of the ampligying circuit for the $\overline{TD}$ signal for the secure detection of the signalafter the receipt ofthe carrier. That is, this line is connected so that the signal can be detected even if the signal level is lowered temporarily (for example, when the input of pin 6 of IC "10C" is lowered below 0.27V). When the carrier is received and $\overline{CTS}$ is set to the low level, the reference voltage of the amplifier is lowered below the voltage generated by voltage dividing resistore R53 and 44, and the threshold level is lowered by the difference between both voltages to heighten the signal detecting power.
- The $\overline{SH}$ and $\overline{R1}$ signals are used to select ORG or ANS mode and selected with PB4 of 82C55 ($\overline{R1}$: ANS, $\overline{SH}$: ORG).
- For other signals, see Table 3-29.

Table 3-29

Pin	Abbreviation	Official name	Direction of signal	Explanation
1	X'tal	Crystal	Input	Input terminal for 1-MHz clock signal from outside.
2	MODE	Mode	Output	Output terminal for indicating the mode of modem. ● ORG mode (High-Band receiving: H) ● ANS mode (Low-Band receiving: L)
3	$\overline{\text{ALARM}}$	$\overline{\text{Alarm}}$	–	Not used.
4	RXC	Receive Carrier	Input	Input terminal for received signals for demodulation. Spedivied standard signals are shown below. Mode / BTL / CCITT / Signal ORG / 2225Hz / 1650Hz / Mark ORG / 2025Hz / 1850Hz / Space ANS / 1270Hz / 980Hz / Mark ANS / 1070Hz / 1180Hz / Space
5	$\overline{\text{RI}}$	$\overline{\text{Ring Indicator}}$	Input	Input terminal for set signals for changing to ANS mode. If an input signal above 17 – 48 ms is received, Active signal is inputted. If applied directly, Ringing signal is inputted. TTL output is inputted depending on modem. When frequency of Ringing signal is above 20 Hz, set to Active.
6	$\overline{\text{Switch}}$	$\overline{\text{Switch Hook}}$	Input	Input terminal for set signal for changing to ORG mode. If L-level signal above 16 – 33 ms is received, set to Active. Transmission side may be kept to L-level during communication.
7	$\overline{\text{CTS}}$	$\overline{\text{Clear to Send}}$	Output	Transmission Ready signal.
8	RXD	Recieved Data	Input	Output terminal for demodulation signal. ● Mark signal: H-level ● Space signal: L-level Common to BTL CCITT
9	Vss	–	–	GND
10	TXD	Transmit Data	Input	Terminal for two-value input signals for FSK. (Mark: H-level, Space: L-level)
12	$\overline{\text{DSR}}$	$\overline{\text{Data Set Ready}}$	Input	Output terminal for outputting L-level when L-level signal of $\overline{\text{RI}}$ or $\overline{\text{SH}}$ is inputted.
13	$\overline{\text{FULL}}$	$\overline{\text{Full Duplex}}$	Input	Input terminal for setting to normal fully double communication mode.
14	B/$\overline{\text{C}}$	BTL/$\overline{\text{CCITT}}$	Input	Selected as follows: ● BTL standard: H-level ● CCITT standard: L-level
15	$\overline{\text{TD}}$	$\overline{\text{Threashold Detect}}$	Input	Input terminal for signals from external threshold detector. To Maintain the normal condition (Communication state), L-level signals of 20 sec must be inputted at least every 33 msec. If H-level is maintained longer than 33 – 48 msec, $\overline{\text{CTS}}$ is set to H-level, and TXC is turned off in ORG mode, and Mark signal is sent out in ANS mode.
16	$\overline{\text{HALF}}$	$\overline{\text{Half Duplex}}$	–	Not used
17	TXC	Transmit Carrier	Output	Output terminal for modulation signal of stepped sine wave (In ANS mode, Mark signal is sent out as soon as DSR is turned on.) Mode / Signal / BTL / (Hz) / CCITT (Hz) ORG / Mark / 1270 / –0.98 / 980+0.39 ORG / Space / 1070 / +0.66 / 1180–0.75 ANS / Mark / 2225 / –2.78 / 1850+0.17 ANS / Space / 2025 / –0.71 / 1850+1.85
18	Vpp	–	–	Power source terminal (4.5V Vpp 6.0V)

3.3.11 Tone/Dial Control Circuit

This circuit generates a required dial tone by dividing the original frequency of the crystal oscillator (CR1). Fig. 3-69 shows the control circuit.

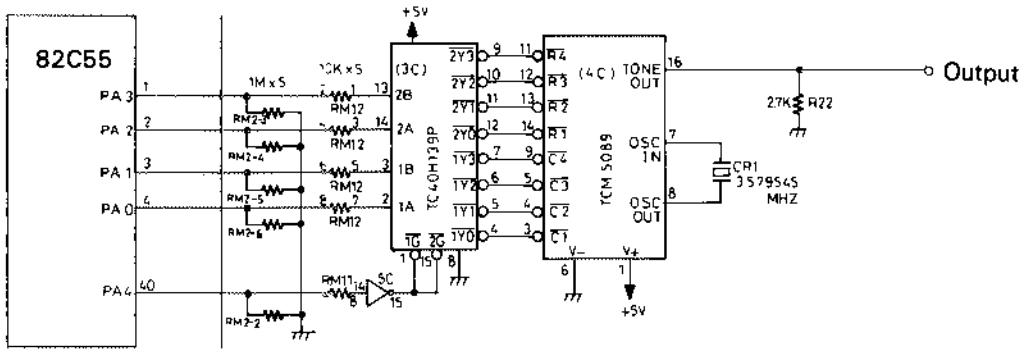


Fig. 3-69

Circuit operation

Port A bits PA0 through PA4 are decoded by the dual 2 to 2 line decoder 40H139. The eight outputs are supplied to the tone generator IC "4C" to control its tone frequency. Fig. 3-70 shows the relation of push-button and control.

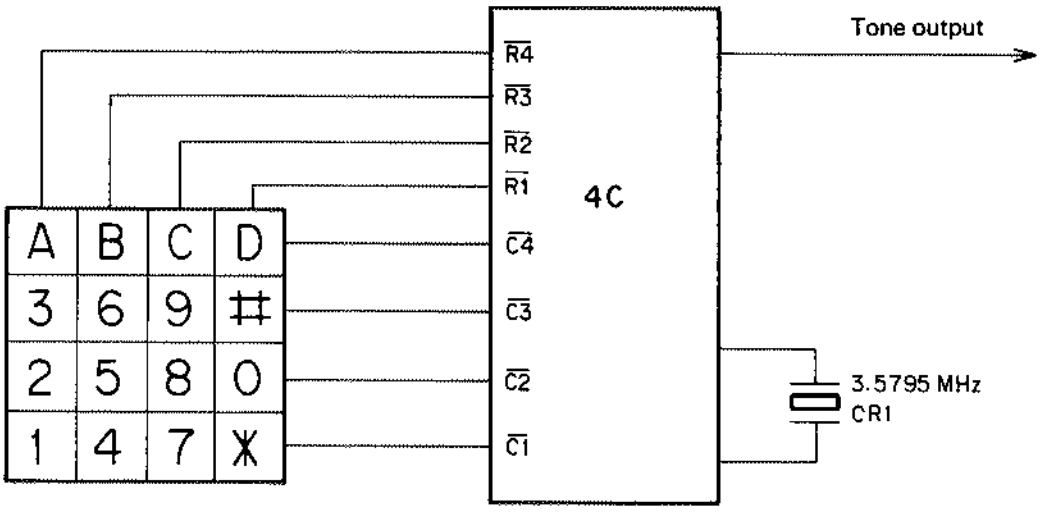


Fig. 3-70

3.3.12 Speaker Output Circuit

The amplifying circuit for the received signals is shown if Fig. 3-72. This circuit is composed of the ON/OFF circuit for the input signal line (amplifying circuit)and the feedback circuit.

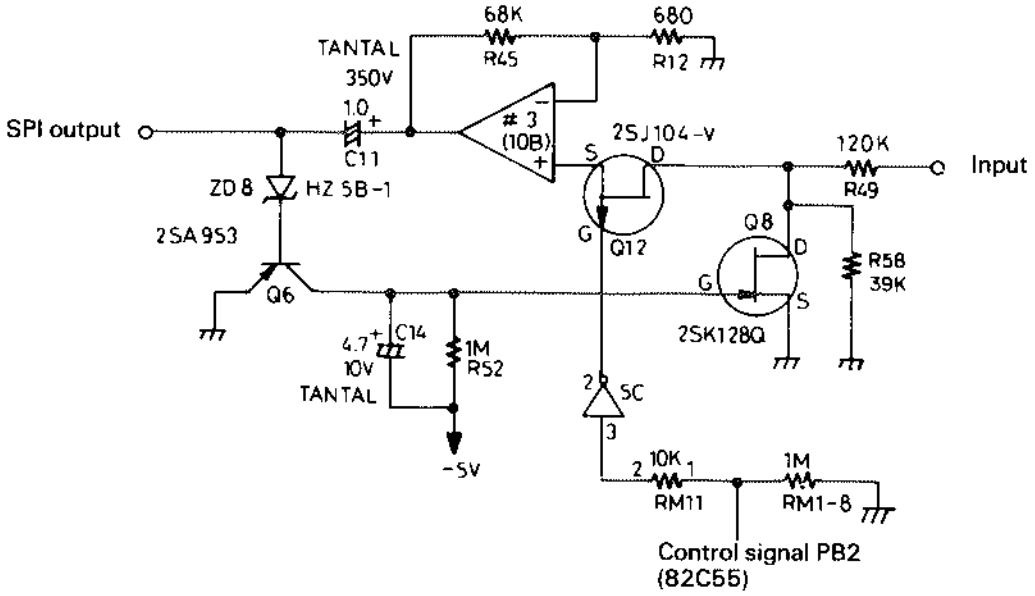


Fig. 3-72

(1) ON/OFF circuit

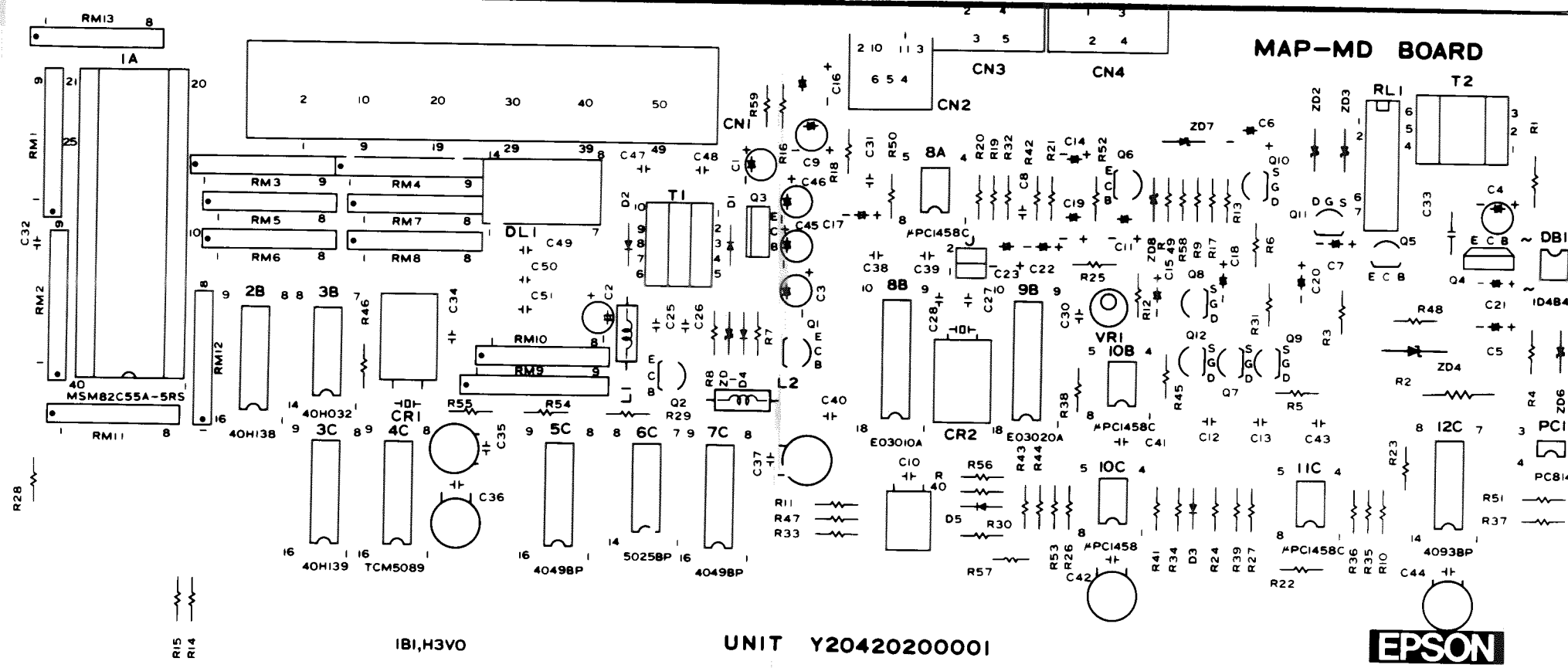
The input signal line has switching control with the output of PB2 (85 (H) bit 2) of 82C55. If the output of PB2 is at high level, the polarity is inverted by IC "5C" and the low level signal is supplied to the gate of Q12 to turn it on, and the input signal is supplied to the negative feedback amplifier of "10B". The amplification of the amplifier is calculated by the following equation.

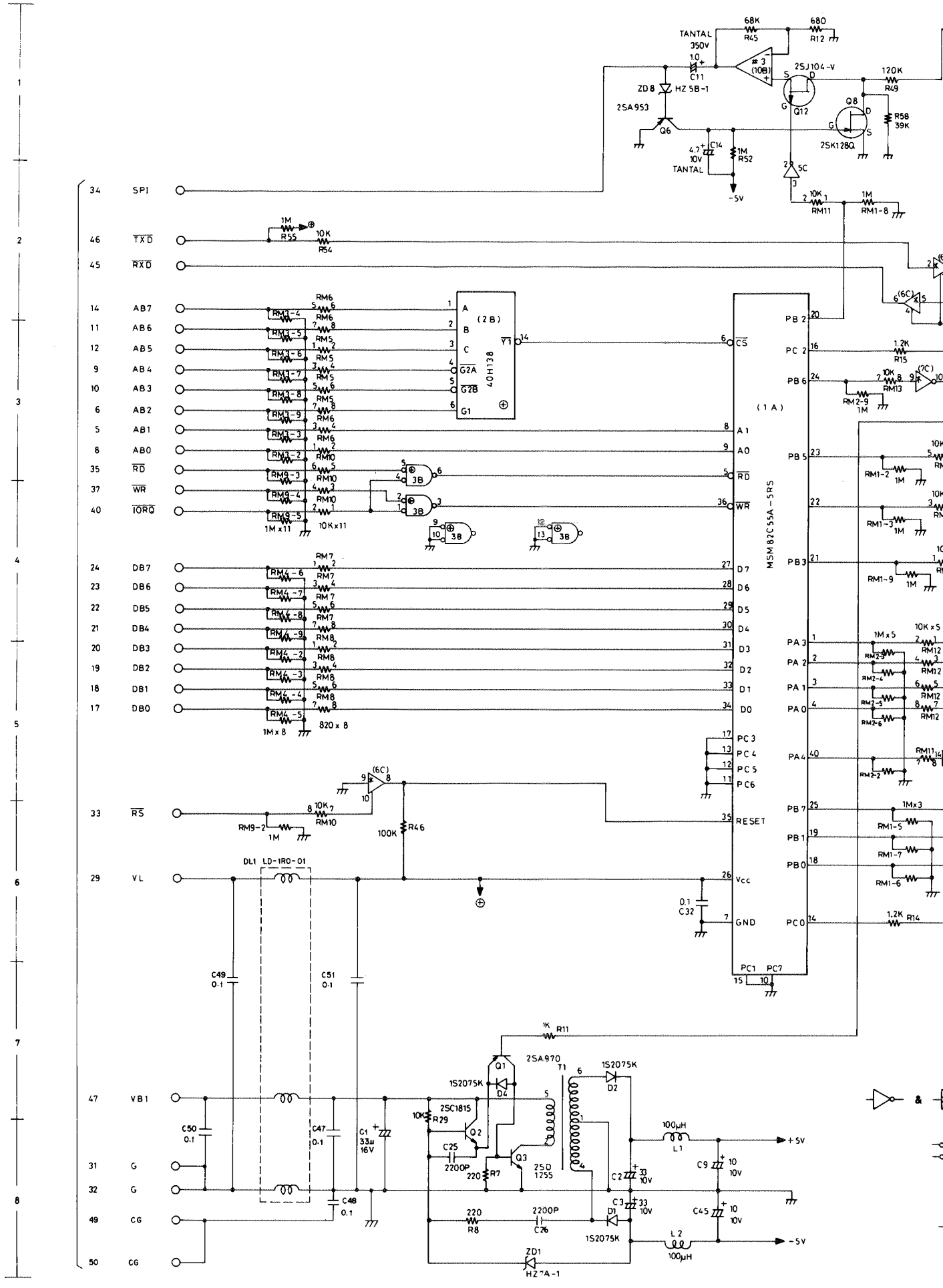
$$(AF = \frac{R45+R12}{R45} \longrightarrow 101\ dB$$

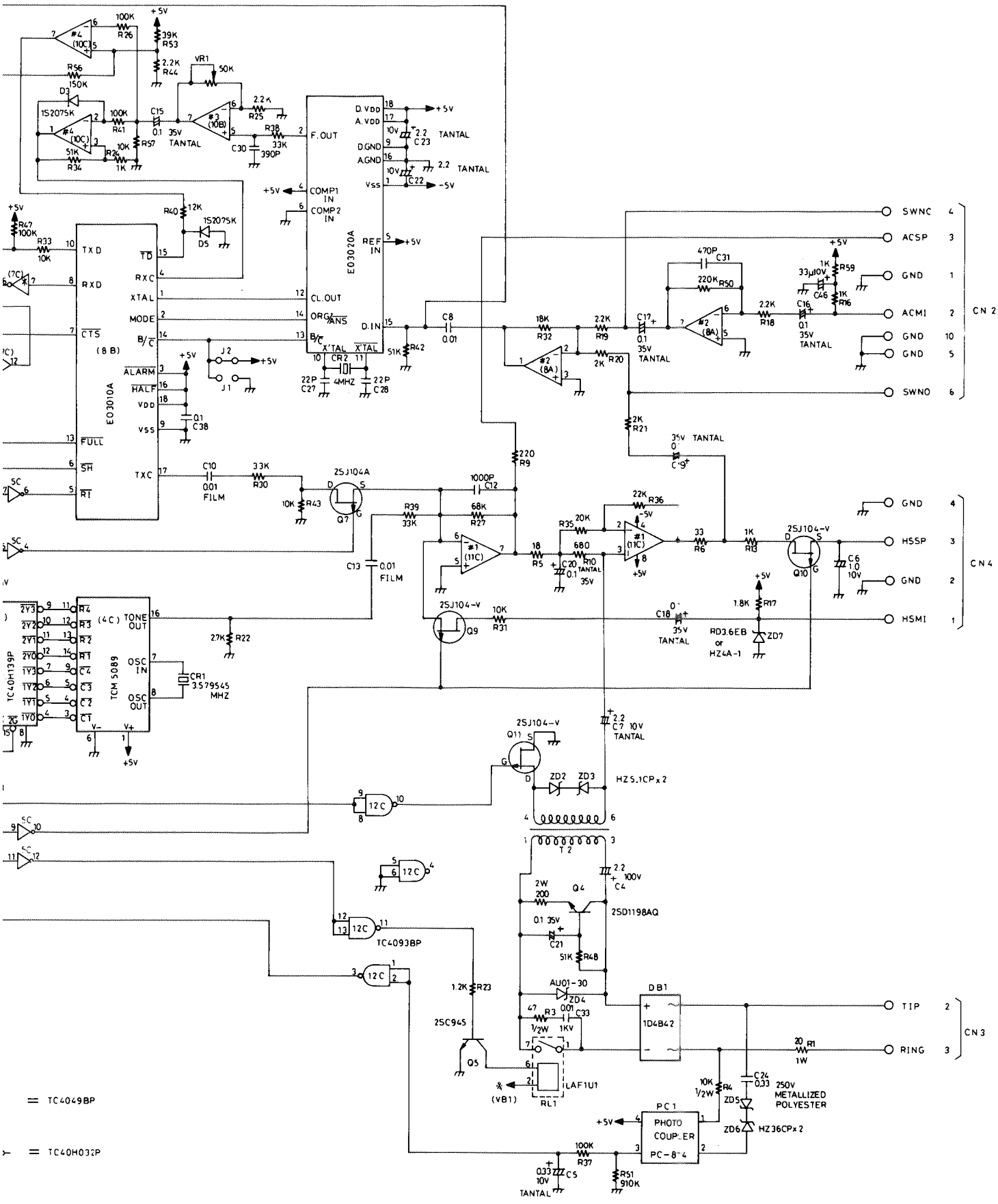
(2) Feedback circuit

The output of the amplifier is outputted to the negative pole side by means of the static coupling with capacitor C11. This output is supplied to the speaker circuit in the body and also supplied through Zener diode ZD8 to the base of TrQ6. This circuit operates as explained below to keep the signal output for the speaker in the body within a certain range.

Normally, the gate of TrQ8 is pulled up to –5V and turned on. In this state, the drain side is near the ground level and the low-level signals such as noises are not amplified by IC "10B", and they are not outputted to the speaker. However, if a signal is inputted, its waveform is presented on the drain side of TrQ8 and supplied through TrQ12 to IC "10B", where it is amplified. As the result, a voltage is generated on the anode side of the Zener diode through the static coupling capacitor C11 on the output terminal side. If this voltage becomes almost –5V, ZD8 is punctured and TrQ8 is turned on. In this state, the gate voltage of TrQ8 is lowered and TrQ8 is turned off, and the amplification is carried out according to the input signal. Since the operation described before is repeated according to the output IC "10B", the output signal for the body is near 4Vp-p.


MAP-MD BOARD
RM13
1A
RM1
RM2
RM12
RM11
MSM82C55A-5RS
RM3
RM4
RM5
RM6
RM7
RM8
DL1
RM10
RM9
CN1
CN2
CN3
CN4
T1
T2
RL1
L1
L2
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
8A
8B
2B
3B
3C
4C
5C
6C
7C
9B
10B
10C
11C
12C
CR1
CR2
VR1
DB1
ZD2
ZD3
ZD4
ZD6
ZD7
ZD8
40H032
40H138
40H139
TCM5089
40498P
50258P
E03010A
E03020A
μPC1458C
μPC1458
40938P
IBI,H3V0
UNIT Y20420200001
EPSON
IKI262


TANTAL 350V
68K R45
680 R12
C11
ZD8 HZ5B-1
2SA953 Q6
2SJ104-V Q12
2SK1280 Q8
120K R49
R58 39K
C14 4.7 10V TANTAL
1M R52
-5V
5C
10K RM11
1M RM1-8
34 SPI
46 TXD
45 RXD
1M R55
10K R54
14 AB7
11 AB6
12 AB5
9 AB4
10 AB3
6 AB2
5 AB1
8 AB0
35 RD
37 WR
40 IORQ
RM1-4
RM1-5
RM1-6
RM1-7
RM1-8
RM1-9
RM1-3
RM1-2
RM9-3
RM9-4
RM9-5
1M x11
10K x11
40H138
(2B)
G2A
G2B
G1
Y1
3B
MSM82C55A-5RS
(1A)
CS
A1
A0
RD
WR
D7
D6
D5
D4
D3
D2
D1
D0
RESET
Vcc
GND
PC3
PC4
PC5
PC6
PC1
PC7
PB2
PC2
PB6
PB5
PB3
PA3
PA2
PA1
PA0
PA4
PB7
PB1
PB0
PC0
1.2K R15
RM2-9 1M
RM13
RM1-2 1M
RM1-3 1M
RM1-9 1M
1M x5
10K x5
RM12
RM2-3
RM2-4
RM2-5
RM2-6
RM2-2
RM11
1M x3
RM1-5
RM1-7
RM1-6
1.2K R14
24 DB7
23 DB6
22 DB5
21 DB4
20 DB3
19 DB2
18 DB1
17 DB0
RM4-6
RM4-7
RM4-8
RM4-9
RM4-2
RM4-3
RM4-4
RM4-5
1M x8
820 x 8
33 RS
RM9-2 1M
RM10
100K R46
29 VL
DL1 LD-1R0-01
C49 0.1
C51 0.1
0.1 C32
47 VB1
31 G
32 G
49 CG
50 CG
C50 0.1
C47 0.1
C48 0.1
C1 33μ 16V
1K R11
Q1 2SA970
T1
1S2075K D4
1S2075K D2
1S2075K D1
2SC1815 Q2
Q3 2SD1255
10K R29
C25 2200P
220 R7
220 R8
2200P C26
100μH L1
L2 100μH
C2 33 10V
C3 33 10V
C9 10 10V
C45 10 10V
+5V
-5V
ZD1 HZ7A-1



MAP-MD BOARD
Y204202000 (A)

3.4 Multi-Unit

This unit consists of the 60K byte RAM, ROM capsule and a direct modem. The modem is controlled via an 82C55. The RAM elements are backed up by an internal battery. The RAM elements are hacked up by an internal battery. The ROM elements can be accessed for replacement by removing a bottom plate. For further details, see the descriptions on the RAM disk and modem units.

3.4.1 Circuit operation

The Multi-unit is made up of a control board, a battery, and casing parts. Fig. 3-73 shows the element layout on the control board and table 3-30 lists major board elements.

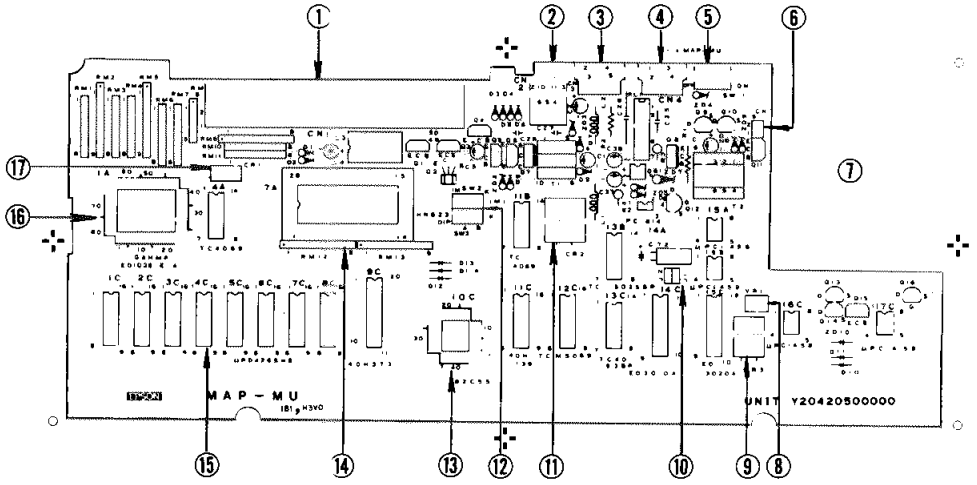


Fig. 3-73 Multi-unit board element layout

Table 3-30 Major multi-unit board elements

Indication of figure	Element name	Function	Indication figure	Element name	Function
1	CN1	Main Frame system bus interface	2	CN2	Coupler interface
3	CN3	Telephone line interface	4	CN4	Receiver interface
5	SW1	RAM backup switch – ON: Enabled, OFF: Disabled	6	CN5	Battery interface
7	Internal battery	4.8V, 480 mAh	8	VR1	Receive Sensitivity
9	CR3	4 MHz	10	J1, J2	Mode Selection
11	CR2	3.58 MHz	12	SW2, 3	ROM Selection
13	82C55	Modem control gate array	14	ROM capsule	Application ROM
15	DRAM	64K.B	16	GAHMP	DRAM, ROM, and 82C55 control gate array
17	CR1	32.77 KHz			

3.4.2 Functional Circuit Blocks

The Fig. 3-74 is a block diagram of the Multi-unit:

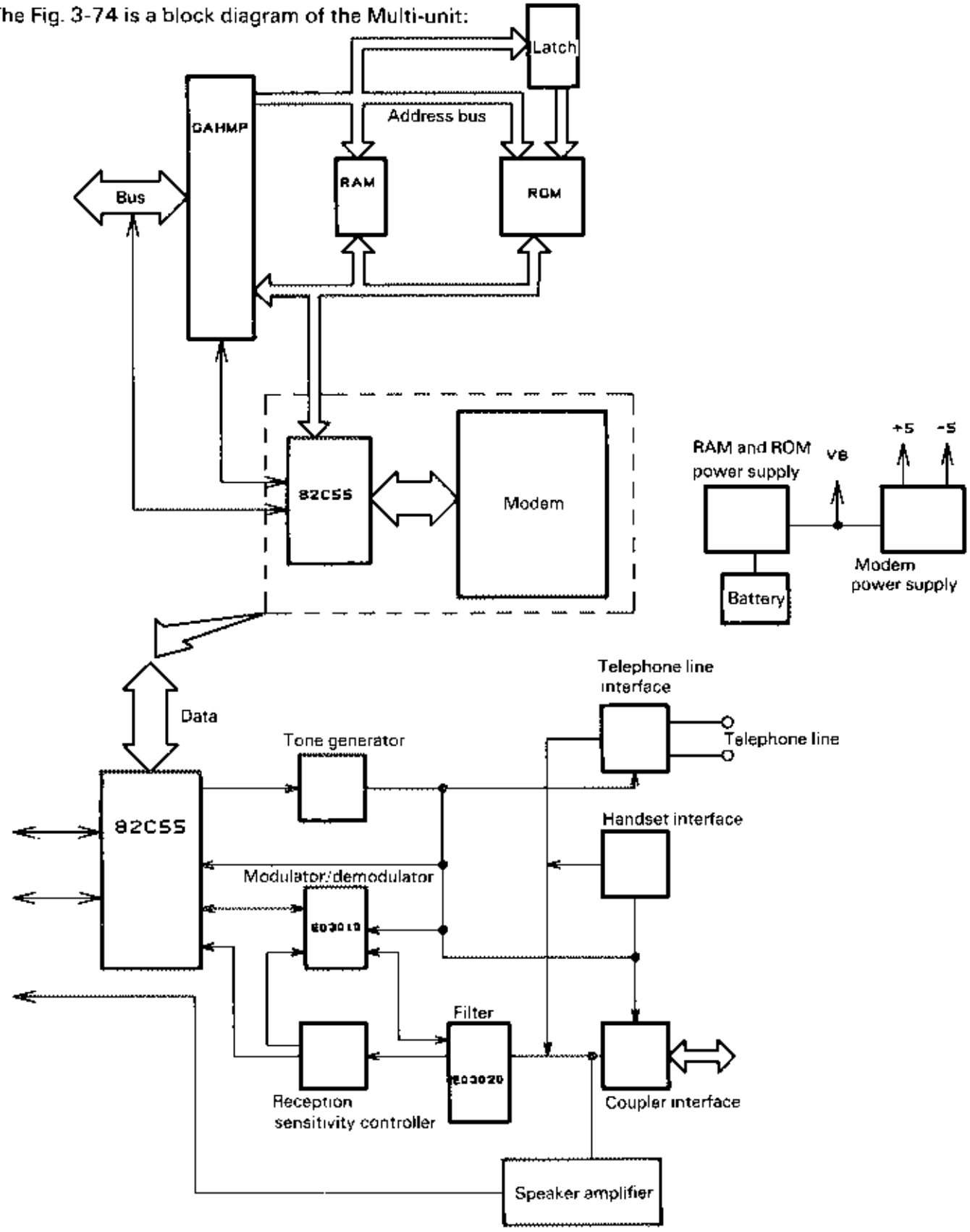


Fig. 3-74

The MAP-MU board can be divided into a ROM/RAM file section and a modem section. The ROM/RAM file section is structured in the same concept as the Main Frame or RAM disk unit, and the modem section used almost the same circuit as the modem unit.

3.4.3 Interface Signals

The Multi-unit is connected via connector CN1. The Main Frame side interface provides many signals for universal application. However, this option unit used only a part of them. Table 3-31 lists the signals and their functions.

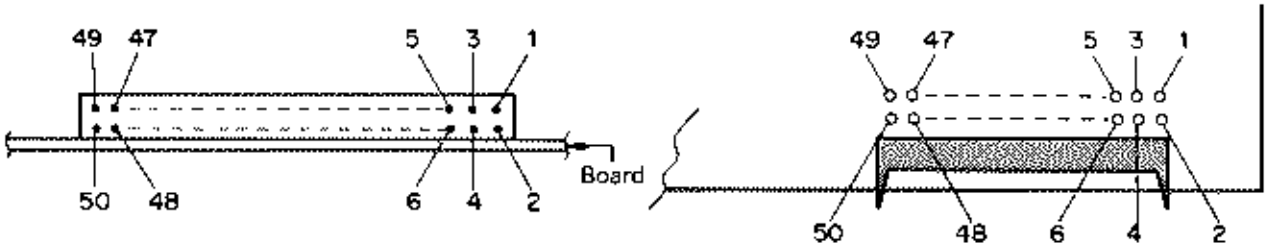


Table 3-31 Multi-Unit Interface Signals

Connection pin No.	Signal name	Input/ Output	Function	Connection pin No.	Signal name	Input/ Output	Function
1	——	——	Not used	26	——	· ·	Not used
2	——	——	Not used	27	$\overline{M1}$	Input	Machine cycle 1
3	——	——	Not used	28	$\overline{WAIT}$	Output	Wait signal
4	——	——	Not used	29	VL	Input	Logic circuit voltage +5V
5	AB1	Input	Address bus line 1	30	$\overline{HLTA}$	Input	HLTA acknowledge
6	AB2	Input	Address bus line 2	31	GND	——	Signal ground
7	· ·	-	Not used	32	GND	——	Signal ground
8	AB0	Input	Address bus line 0	33	$\overline{RS}$	Input	Reset signal
9	AB4	Input	Address bus line 4	34	SPI	Output	Speaker output signal
10	AB3	Input	Address bus line 3	35	$\overline{RD}$	Input	Read-signal
11	AB6	Input	Address bus line 6	36	$\overline{MRQ}$	Input	Memory Request signal
12	AB5	Input	Address bus line 5	37	$\overline{WR}$	Input	Write signal
13	——	——	Not used	38	$\overline{CLK}$	Input	2.45 MHz clock signal
14	AB7	Input	Address bus line 7	39	VCH	Input	Charge voltage
15	——	——	Not used	40	$\overline{IORQ}$	Input	I/O Request signal
16	——	——	Not used	41	DCAS	Input	Data CAS signal
17	DB0	Input/Output	Data bus line 0	42	DW	Input	Data Write signal
18	DB1	Input/Output	Data bus line 1	43	——	——	Not used
19	DB2	Input/Output	Data bus line 2	44	——	——	Not used
20	DB3	Input/Output	Data bus line 3	45	$\overline{RXD}$	Output	Serial Receive data
21	DB4	Input/Output	Data bus line 4	46	$\overline{TXD}$	Input	Serial transmit data
22	DB5	Input/Output	Data bus line 5	47	VB1	Input	Battery voltage
23	DB6	Input/Output	Data bus line 6	48	——	-	Not used
24	DB7	Input/Output	Data bus line 7	49	CG	——	Frame ground
25	—— -	·	Not used	50	CG	——	Frame ground

3.4.4 Selector Jumpers and Switches

Jumpers 1 and 2 are used to select either the CCITT or BTL standard as follow:

Table 3-32

Jumpter setting		Standard
J1	J2	
Short	Open	CCITT
Open	Short	BTL

The Battery Backup switch SW1 controls the charge/discharge of the DRAM backup battery:

ON : Enables charge/discharge

OFF: Disables charge/discharge

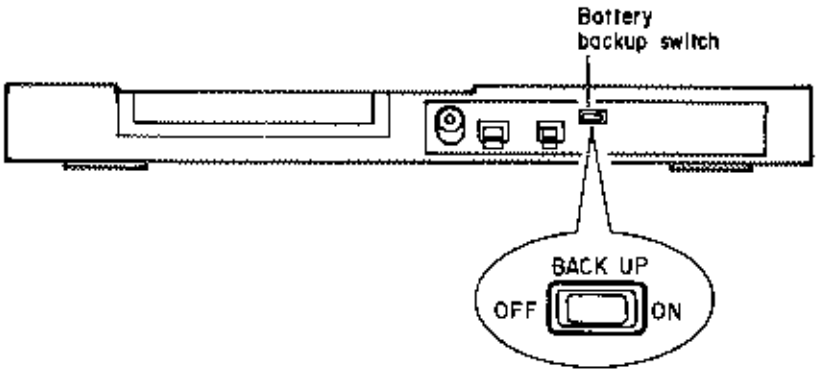
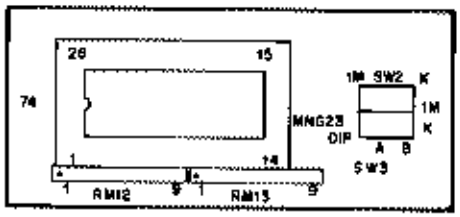


Fig. 3-75

Switches 2 and 3 are used for ROM capacity selection as follow:

Table 3-33

Switch setting		ROM capacity
SW2	SW3	
K	B	64K bytes
K	B	128K bytes
K	B	256K bytes
1M	B	512K bytes*
1M**	A**	1M bytes



* 512K byte ROM is not presently released.

** Shipment setting.

3.4.5 Exterior Views

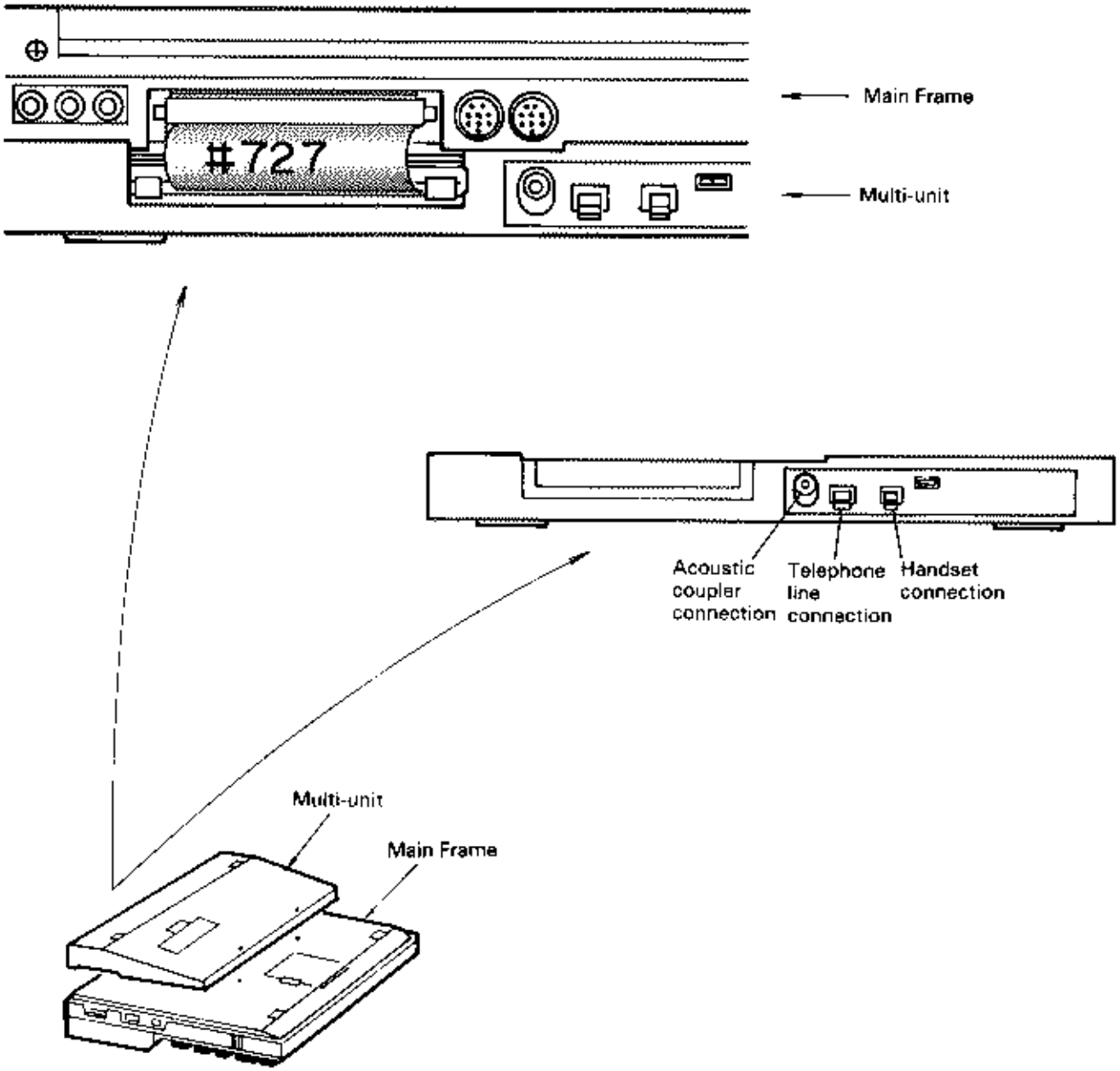


Fig. 3-76

3.4.6 Power Supply Circuit

The power supply circuit consists of a rechargeable battery (4.8V, 450 mAH), a battery charging circuit, a logic circuit drive voltage supply circuit, a backup circuit, and a modem power cupply circuit.

(1) Rechargeable battery and charging circuit

The battery is connected to the MAP-MU board via a connector CN2. The Battery Backup switch SW1, which enables or disables the DRAM backup circuit, is located at the rear of the unit.

The circuit surrounding the battery is shown below.

(2) Battery backup switch SW1

This switch should be reset OFF when storing this unit alone or when not using it for a long period of time as attached to the Main Frame. With this switch reset OFF, the battery is prevented from any discharge other than the natural one so that the longest life can be ensured.

- The logic circuit operates irrespective of the setting of this switch; when the switch is reset OFF, the line is backed up from the Main Frame supply and its working time may be shortened.

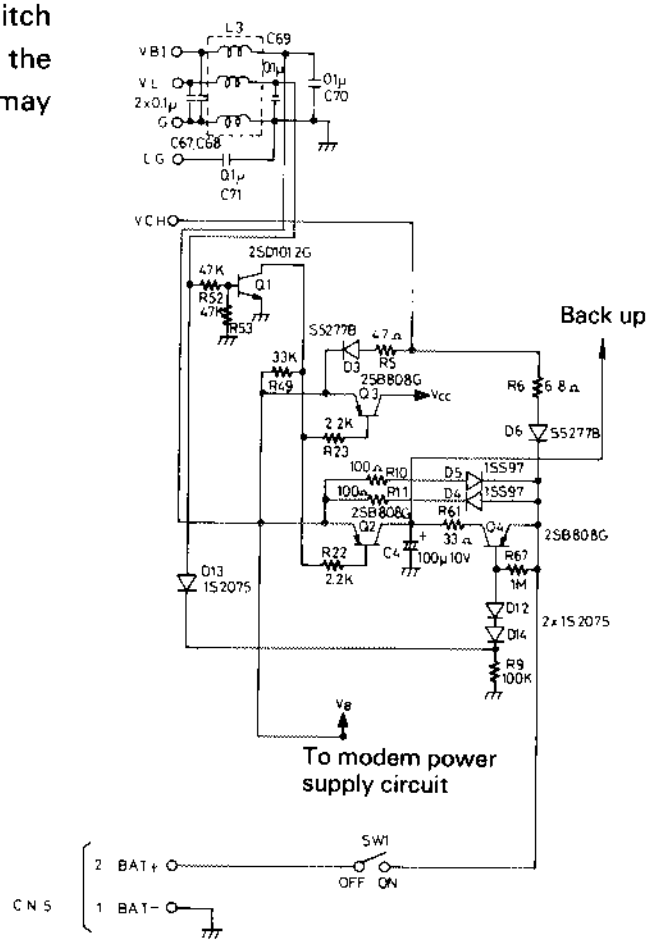


Fig. 3-77

(3) Battery charging

The battery is always charged toward the full via either of the following two charging paths:
When the Main Frame AC adaptor is connected to the AC power source, the battery is charged via the path:

V_{CH} → R6 → D6 → SW1 → CN2 → Battery

When the AC adaptor is not used but the battery voltage is lower than the VB1 supply voltage from the Main Frame, the path is:

V_{B1} → R10 → D5 → SW1 → CN2 → Battery

(4) Backup circuit

The backup circuit supplies power required to protect data in the DRAM elements while Main Frame is off. Table 3-34 lists the elements backed up by this circuit.

Table 3-34

Location	Name	Function	Location	Name	Function
4A	TC4069	Inverter	16C	μPC1458	Operational Amplifier
15A	μPC1458	Operational Amplifier	17C	μPC1458	
15B	μPC1458	Operational Amplifier	1 ~ 8C	4265 × 8	D-RAM

These elements are powered from a special line called "Backup" and always active; they are powered by the operating voltage supply while Main Frame is on and from the backup line while off.

1) Power supply paths to the backup line

There are the sixpaths listed in table 3-35 which are selected to supply power to the backup line depending on the various conditions. The abbreviations used in the table mean the following:

V_{B1} : Main Frame power supply
V_X : Option unit battery voltage
Battery: Option unit battery

Table 3-35 Backup Line Supply Paths

PX-8 power	AC adaptor	Battery voltage relation	Path
OFF	Connected	–	V_{CH} → R6 → D6 → Q4 →
	Not connected	$V_{B1} > V_X$	V_{B1} → R10 → D5 → Q4 →
	Not connected	$V_{B1} < V_X$	Battery → CN2 → SW1 → Q4 →
ON	Connected	–	V_{CH} → R5 → D3 → Q2 →
	Not connected	$V_{B1} > V_X$	V_{B1} → Q2 →
	Not connected	$V_{B1} < V_X$	Battery → CN2 → SW1 → D4 → R11 → Q2 →

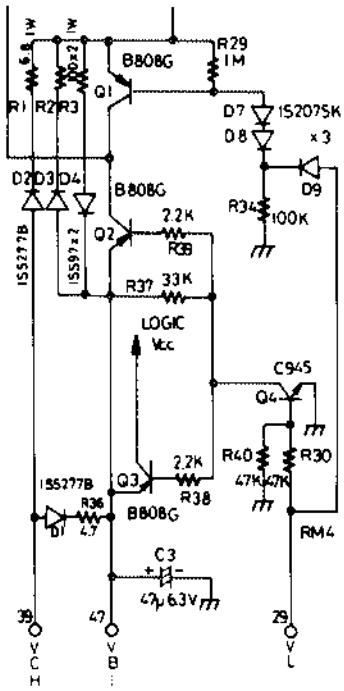
The backup source is supplied through either transistor Q2 or Q4 depending on whether Main Frame is on or off.

- While Main Frame is off, VL is low because the logic circuit operating voltage is not supplied. This maintains transistor Q3 cut off and the collector is pulled up high through resistor R49. Thus, transistors Q2 and Q3 remain cut off.

  VL is also connected to the base of Q4 through diodes D13. The emitter of Q4 is connected to VCH or battery voltage (normally maintained at +5V). The source is also connectd to the base through R67.

  Because the base is connected to the signal ground through D12, D14, and R9, the current, which flows from the base to the ground unless the junction of D14 and R9 is pulled up to the VL line, generates a potential across the emitter and base.

  That is, transistor Q4 conducts due to this postential while Main Frame is off. Thus, all the bckup sources are supplied via Q4.



  While Main Frame is on, no effective potential is generated across the emitter and base of Q4 because the base (the cathode of D14) is pulled up to VL, and Q4 is maintained cut off. Q1 conducts because the base input (VL) is high and the collector is held low. This maintains Q2 and Q3 in conduction. Thus, the backup line is powered via Q2 and the option logic circuit voltage is supplied through Q3.

(5) Logic circuit voltage

The logic circuit voltage is supplied from the collector of transistor Q3. The voltage applied to the emitter of Q3 (VB1 or VCH through D3 and R5) is supplied to the circuit power line. The supply circuit operatesas described above.

(6) Modem power supply circuit

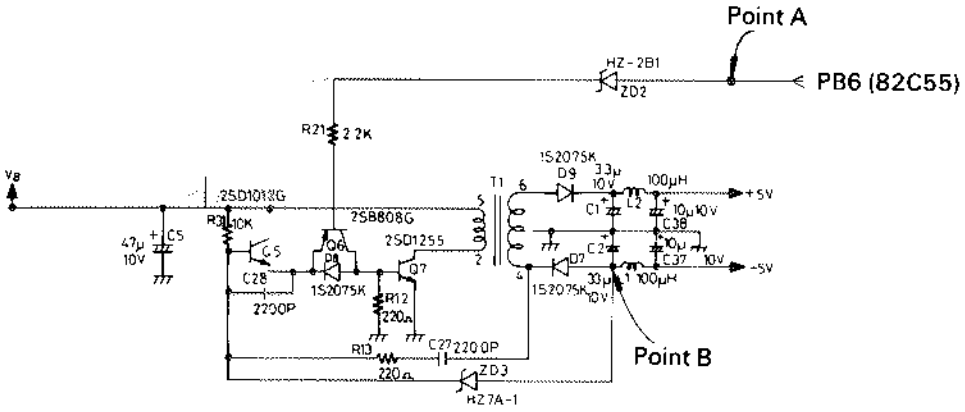


Fig. 3-79 Modem power supply circuit

When the PB6 signal from 82C55 is high (at point A), this modem power supply circuit is disabled because the base of transistor Q6 and the emitter of transistor Q5 is high.
When the PB6 signal is low, the power supply circuit is enabled. Q6 is turned on, also turning Q7 on. The current through the primary winding of transformer T1 induces a voltage across the secondary winding. A –5 V voltage generated at point B is fed back to the base of Q5 through capacitor C27 and resistor R13. This feedback completes an oscillator loop of an approximately 24 kHz. The oscillation maintains the source voltages of +5 V and –5 V which are supplied to the modem section.

The following pictures shows the proper signal waveforms at various points:

Base of Q5

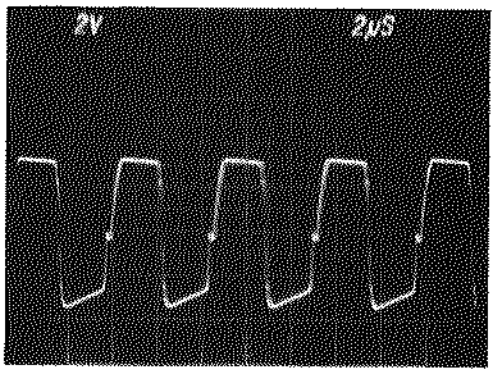


Fig. 3-84

Emitter of Q2

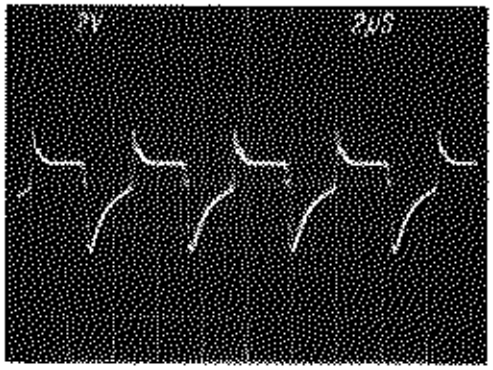


Fig. 3-81

Collector of Q1

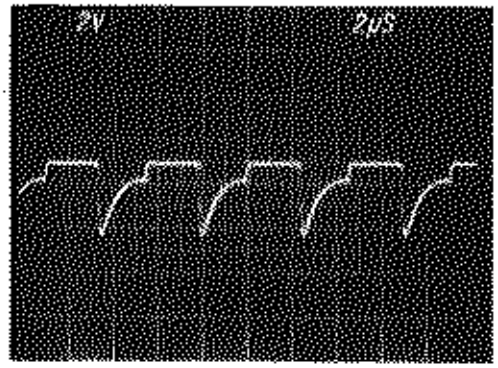


Fig. 3-82

Collector of Q3

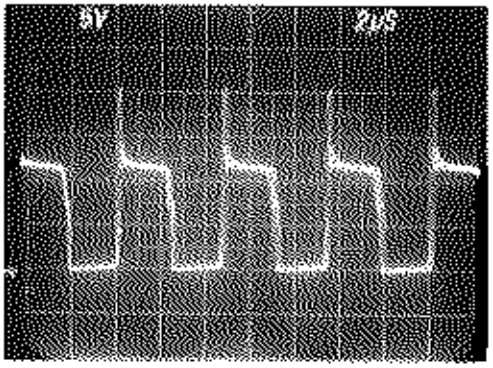


Fig. 3-83

Anode of D1

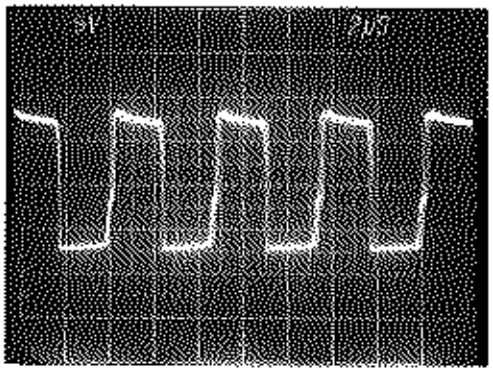


Fig. 3-84

3.4.7 ROM Section

The following is a block diagram of the ROM section:

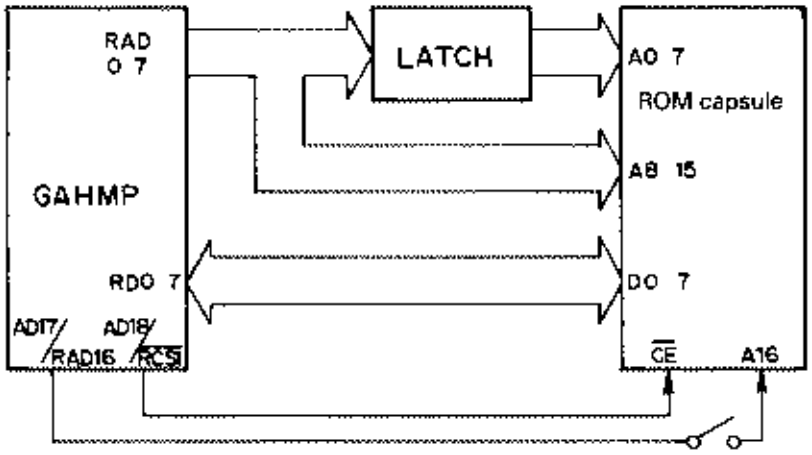


Fig. 3-85

The gate array GAHMP contains four bank registers. When Main Frame reads the Multi-unit ROM when bit 6 is high, a 1M byte ROM Chip Select signal is sent through interface connector pin P19. A signal to latch address lines A0 through A7 is output through P28 at the same time. The latches eight address bits are sent to the ROM capsule together with the address bits A8 through A15 which are output next. Then, accessed ROM data bits D0 through D7 are sent to Main Frame via the gate array.

ROM is accessed at a high speed of 350ns with J1 (P22) set high and J2 (P14) low. The FC signal from P24, which allows the gate array to enable the ROM capsule is normally activated low. Thus, the ROM capsule is always enabled.

The available ROM capacity is determined by two switches SW2 and SW3 as follows:

Table 3-36

Switch setting		ROM capacity
SW2	SW3	
K	B	64K bytes
K	B	128K bytes
K	B	256K bytes
1M	B	512K bytes
1M*	A*	1M bytes

* Shipment setting

When no proper operation is guaranteed when an N-MOS element is used because of the restriction by battery capacity.

3.4.8 RAM Section

The following is a block diagram of the RAM section:

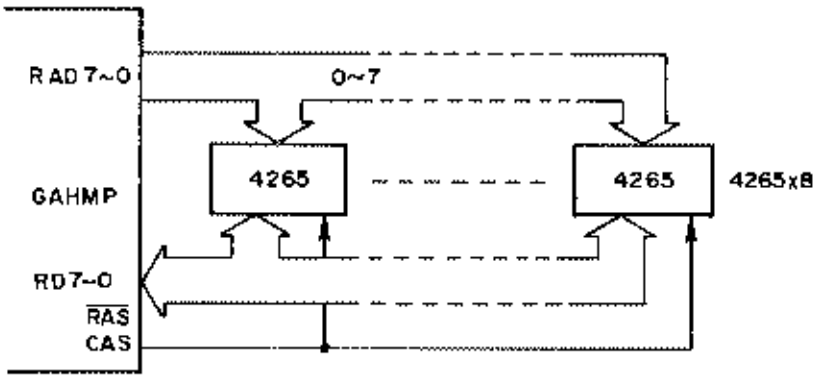


Fig. 3-86

The Multi-unit contains RAM elements which provide a total capacity of 64K bytes. While Main Frame is off, two DRAM refresh mode selection signals DCAS and DW are supplied from Main Frame to the gate array GAHMP. The signals change their states as shown in the table below depending on the ambient temperature:

Table 3-37

Ambient temprature	DW	DCAS	$\overline{CAS1, 2}$	$\overline{WE}$
0 ~ 70°C	L	L	H	H
0 ~ 45°C	H	L	H	L
0 ~ 25°C	H	H	L	

Cycle time: 20 – 30 μs
30.5μs: when 32.768 kHz is supplied to the C32K inpout terminal.

The $\overline{CLOSE}$ signal is activated low by ORing the $\overline{HALT}$ and $\overline{RESET}$ signals to close the RAM file. The signals such as RAS, CAS, and WE, etc. are generated from GAHMP by I/O commands addressing 93H.

3.4.9 Modem Section

The following is a block diagram of the modem section:

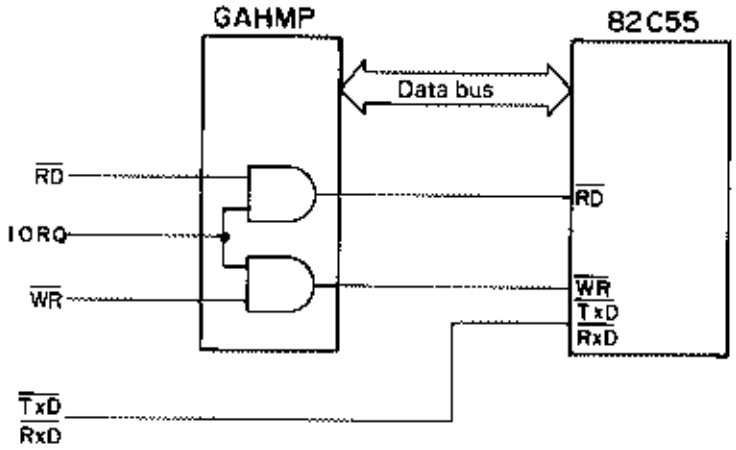
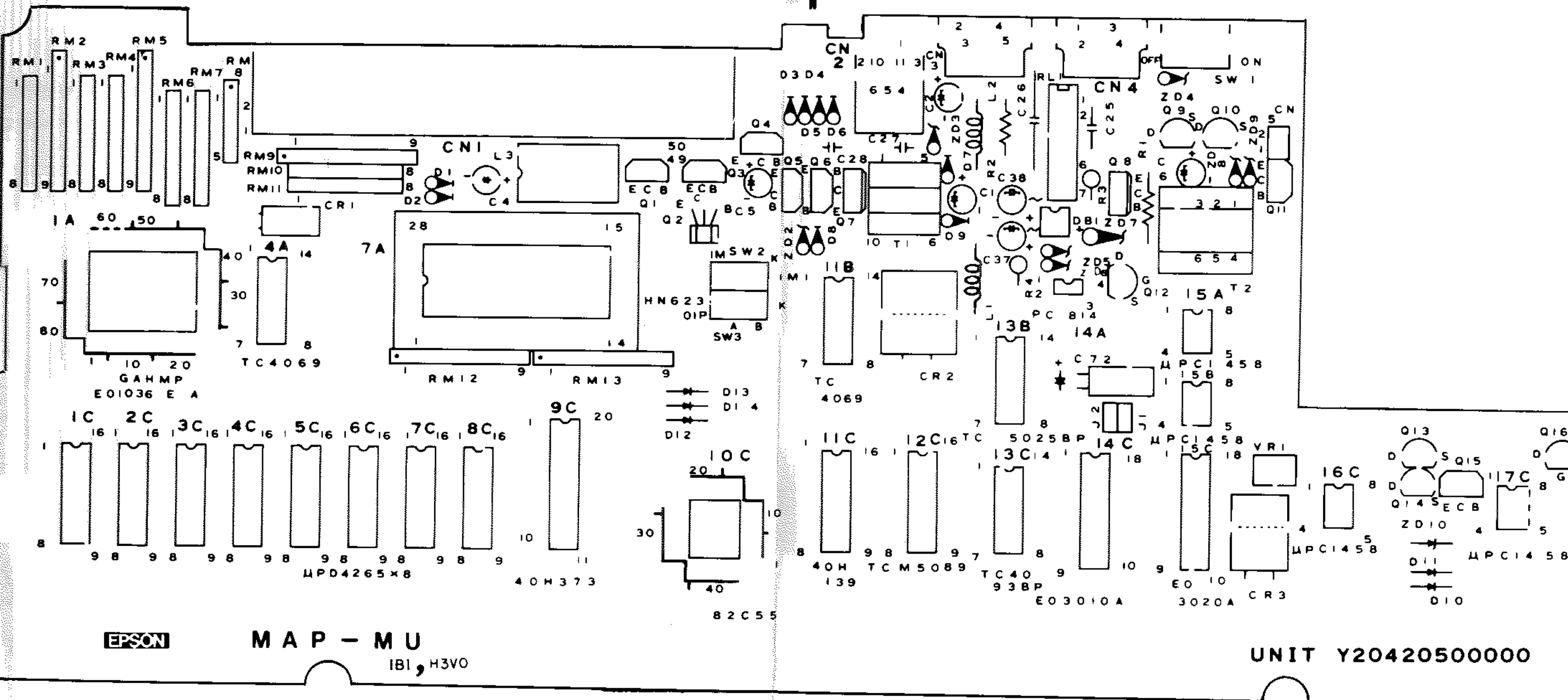
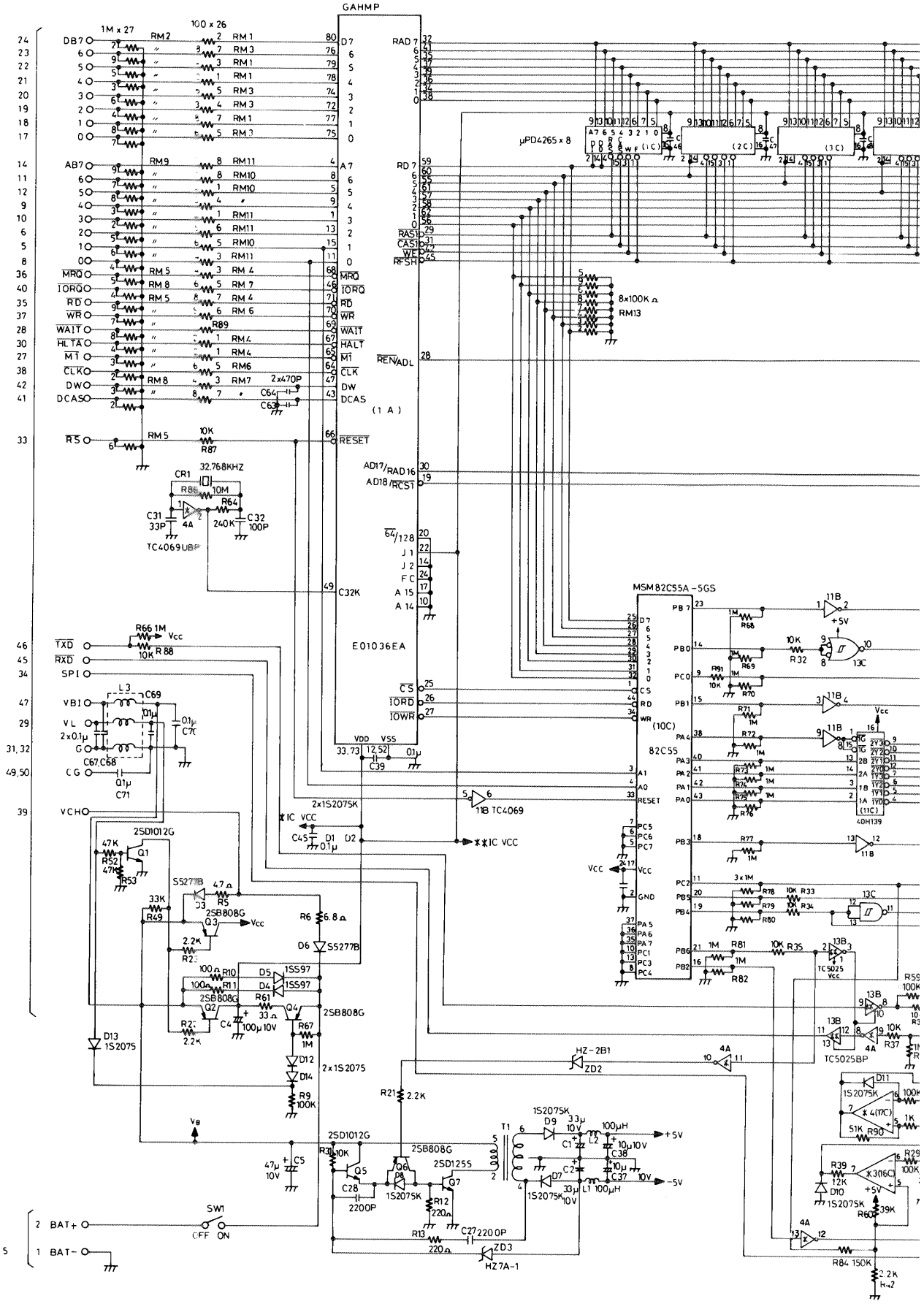
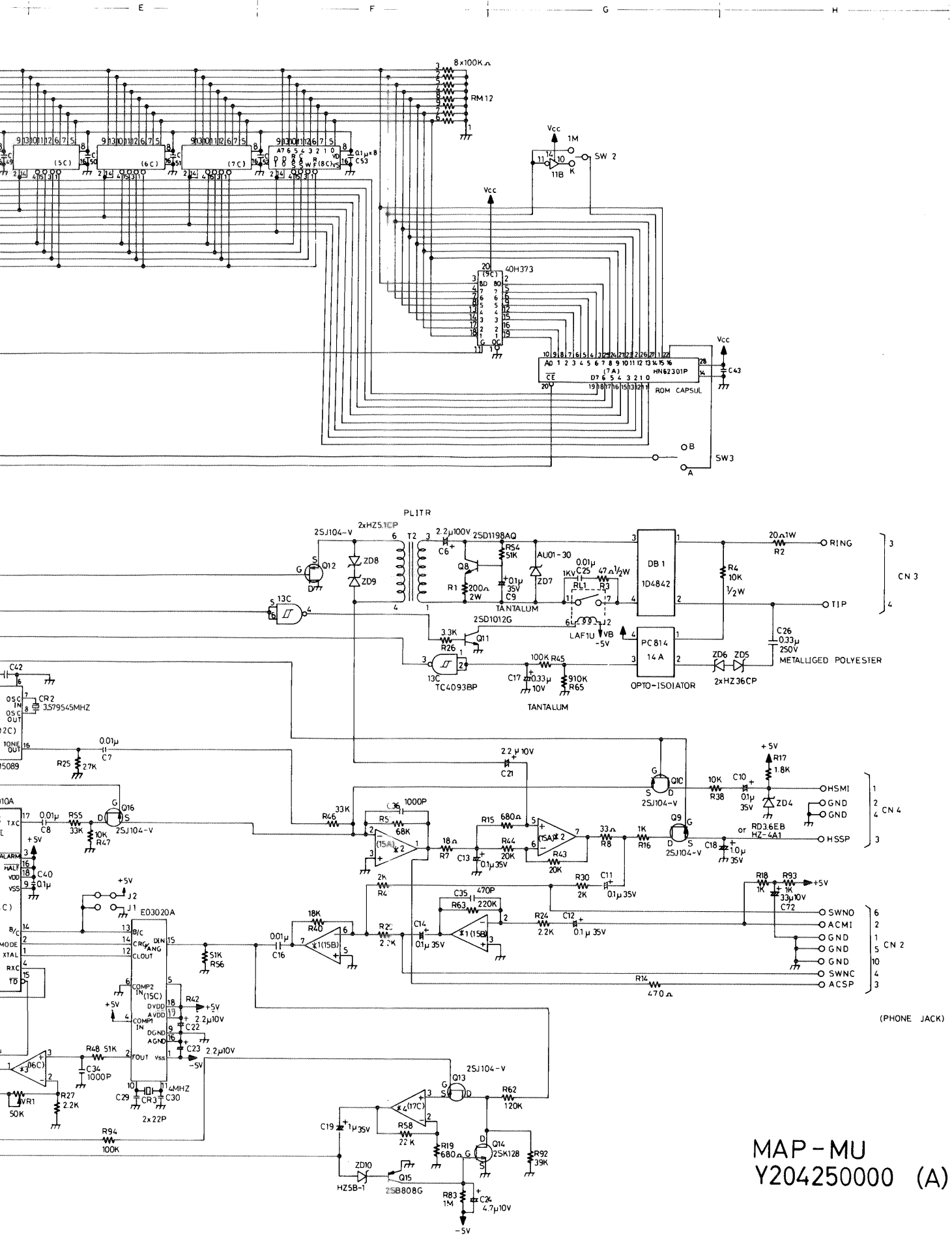


Fig. 3-87

Signals sent from gate array (GAHMP) to modem are composed as shown in Fig. 3-87. This is the same circuit as the optional modem. See Chapter 3.3 Modem Unit for the details of the modem.


MAP-MU
CN1
CN2
CN4
SW1
ON
OFF
1A
4A
7A
9C
10C
11B
11C
12C
13B
13C
14A
14C
15A
15C
16C
17C
1C
2C
3C
4C
5C
6C
7C
8C
GAHMP
E01036 E A
TC4069
HN623
OIP
SW2
SW3
CR1
CR2
CR3
VR1
T1
T2
RL1
TC 4069
μPD4265×8
40H373
82C55
40H 139
TCM5089
TC40 93BP
5025BP
E03010A
E0 3020A
μPC1458
PC 814
MAP-MU
IBI, H3VO
UNIT Y20420500000


GAHMP
1M x 27
100 x 26
RM2
RM1
RM3
RM9
RM10
RM11
RM5
RM8
RM4
RM7
RM6
R89
DB7
AB7
MRQ
IORQ
RD
WR
WAIT
HLTA
MT
CLK
DWO
DCAS
R5
RESET
2x470P
C64
C63
(1A)
CR1
32.768KHZ
R86 10M
R64
240K
C31 33P
C32 100P
TC4069UBP
CN1
RAD7
RD7
RAS
CAS
WE
RFSH
μPD4265 x 8
8x100K Ω
RM13
RENADL
AD17/RAD16
AD18/RCST
64/128
J1
J2
FC
A15
A14
C32K
E01036EA
CS
IORD
IOWR
VDD
VSS
33,73
12,52
0.1μ
C39
MSM82C55A-5GS
82C55
(10C)
PB7
PB0
PC0
PB1
PA4
PA3
PA2
PA1
PA0
PC5
PC6
PC7
PB3
PC2
PB5
PB4
PB6
PB2
PA5
PA6
PA7
PC1
PC3
PC4
RESET
GND
VCC
11B
13C
40H139
(11C)
TC5025
TC5025BP
4A
TXD
RXD
SPI
VBI
VL
G
CG
VCH
R66 1M
10K R88
L3
C69
C67,C68
C71
0.1μ C7(
2x0.1μ
2SD1012G
Q1
47K
R52
47K
R53
S5277B
D3
47Ω
R5
33K
R49
2SB808G
Q3
2.2K
R2
R6 6.8Ω
D6
S5277B
100Ω R10
100Ω R11
D5 1SS97
D4 1SS97
Q2
Q4
R61 33Ω
C4 100μ 10V
R67 1M
R2 2.2K
D13 1S2075
D12
D14
2x1S2075
R9 100K
2x1S2075K
IC VCC
C45
D1
D2
0.1μ
HZ-2B1
ZD2
R21 2.2K
Vs
2SD1012G
R3 10K
Q5
Q6
Q8
2SB808G
2SD1255
Q7
C28
2200P
R12 220Ω
R13 220Ω
C27 2200P
ZD3
HZ7A-1
T1
1S2075K
D9
33μ 10V
100μH
L2
C1
C38
10μ 10V
+5V
-5V
D7
C2
C37
L1
47μ 10V
C5
SW1
OFF ON
CN5
2 BAT+
1 BAT-
R84 150K
2.2K
R42
R90 51K
1K
R39 12K
D10
R60 39K
R59 100K
R29 100K
R37 10K
R32 10K
R33 10K
R34 10K
R35 10K
R68 1M
R69 1M
R70 1M
R71 1M
R72 1M
R73 1M
R74 1M
R75 1M
R76 1M
R77 1M
R78 3x1M
R79 1M
R80 1M
R81 1M
R82 1M
TC4069
11B
3x1M

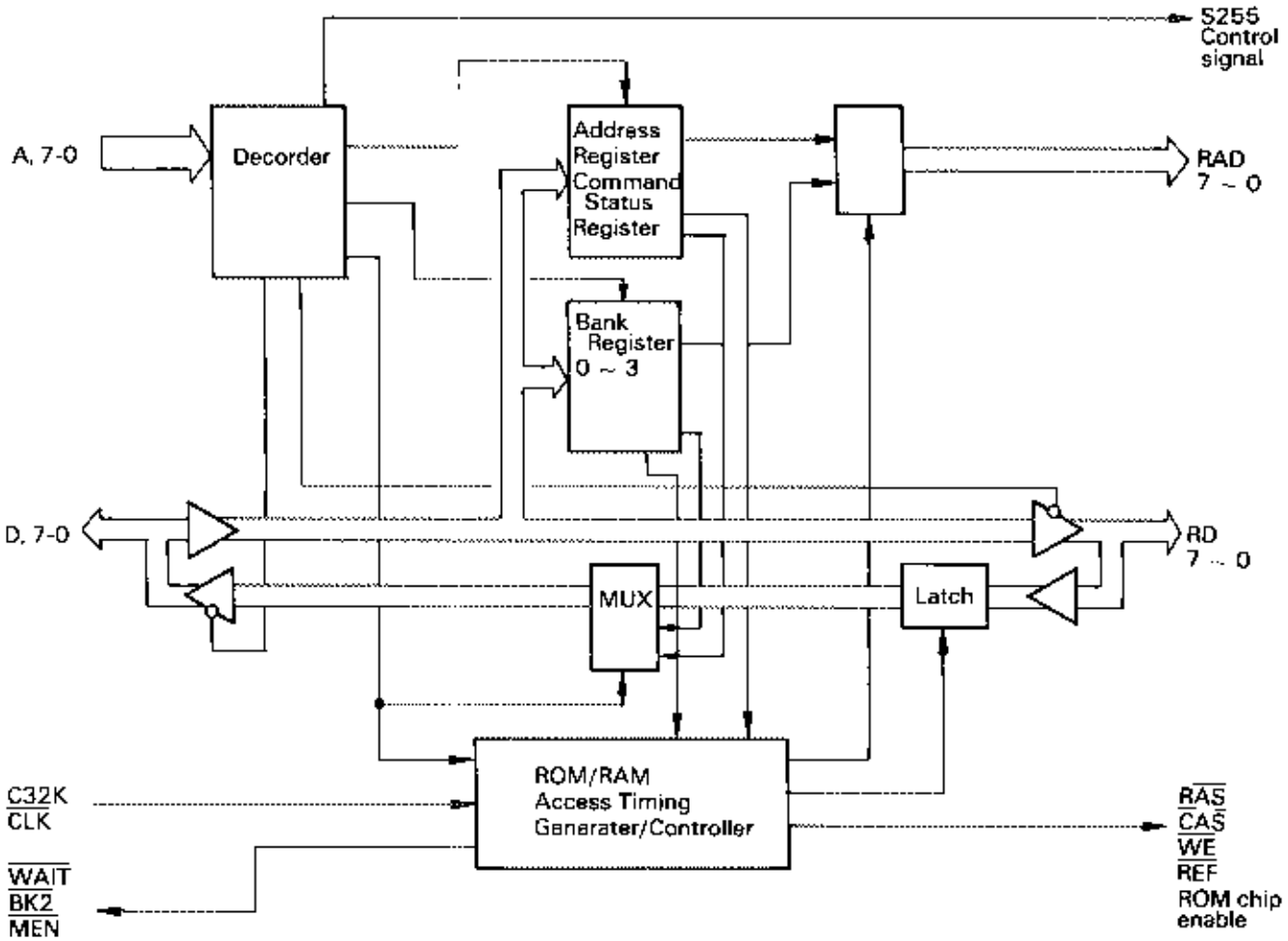


MAP-MU
Y204250000 (A)

APPENDIX

This gate array is connected to the Main Frame systm bus and provids the following three fatures:
(1) A RAM file of up to 128K bytes and a ROM file of 256K bytes
(2) Banked ROM of up to 1M bytes
(3) Modem control
The ROM file of (1) allows the RAM and ROM spaces to be accessed during the Main Frame I/O space (90 – 94H) and is used as a RAM and ROM disk. RAM can be backed up.
The banked ROM of (2) is a memory system which divides its memory space into four segments of 16K bytes each and allows up to 64 – 16K byte banks through an access to one of the segments. The modem control section of (3) is a decoder which generates the three signals of CS, RD and WR whick are used by the modem controller 8255.

This gate array can be used in either of the following ways:
As a RAM file of up to 128k bytes and a ROM of up to 256K bytes plus a modem controller, or as a RAM file of up to 128K bytes and ROM banks of up to 1M bytes in total.
Either can lbe selected by, changing the selector terminal wiring.
The highest operating clock rate of the gate array is 3.6 MHz.



Connection Pin No.	Signal Name	Input/output	Function
1	A3	Input	Address bus line 3
2	MEN	Output	External memory access signal
3	NC	—	—
4	A7	Input	Address bus line 7
5	A5	Input	Address bus line 5
6	NC	—	—
7	NC	—	—
8	A6	Input	Address bus line 6
9	A4	Input	Address bus line 4
10	A14	Input	Address bus line 14 – used to select a bank register.
11	A0	Input	Address bus line 0
12	VSS	—	
13	A2	Input	Address bus line 2
14	J2	Input	A ROM Chip Select signal used for ROM file accessing
15	A1	Input	Address bus line 1
16	NC	—	
17	A15	Input	Address bus line 15 – used to select a bank register.
18	AD19/$\overline{RCS2}$	Output	Lower 1M byte ROM Chip Select output
19	AD18/$\overline{RCS1}$	Output	Lower 1M byte ROM Chip Select output
20	128/$\overline{64}$	Input	RAM file capacity selection input
21	NC	—	—
22	J1	Input	A ROM Chip Select signal used for ROM file accessing
23	NC	—	—
24	FC	Input	A Function Select signal
25	CS	Output	Modem controller 82C55 Chip Select signal
26	IORQ	Output	I/O Request signal
27	IOWR	Output	Output of AND between IORQ and WR

Connection Pin No.	Signal Name	Input/output	Function
28	ADL/$\overline{REN}$	Output	Signal to set RA0 through RA7 to the external latch
29	$\overline{RAS1}$	Output	RAS signal for RAM file's lower 64K bytes
30	RAD0	Output	Address bus line 0
31	$\overline{CAS1}$	Outpout	CAS signal for RAM file's lower 64K bytes
32	RAD7	Outpout	Address bus line 7
33	VDD		
34	RAD1	Output	Address bus line1
35	RAD5	Output	Address bus line 5
36	RAD2	Output	Address bus line 2
37	RAD4	Output	Address bus line 4
38	RAD0	Output	Address bus line 0
39	RAD3	Output	Address bus line 3
40	$\overline{RAS2}$	Output	RAS signal for RAM file's upper 64K bytes
41	RAD6	Output	Address bus line 6
42	$\overline{WE}$	Output	RAM File Write signal
43	DCAS	Input	DRAM self-refresh control signal
44	$\overline{CAS2}$	Output	CAS signal for RAM file's lower 64K bytes
45	$\overline{REF}$	Output	RAM file Refresh signal
46	$\overline{IORQ}$	Input	I/O Request signal from Main Frame system bus
47	DW	Input	DRAM self-refresh control signal
48	$\overline{BK2}$	Output	External memory access signal from Main Frame MAPLE system bus-external memory is accessd when this signal is low.
49	C32K	Input	DRAM self-refresh clock signal
50	$\overline{RCS12}$	Output	A 256K byte ROM Chip Select signal either from the banked ROM or ROM file – the lowest address ROM Chip Select signal
51	$\overline{RCS10}$	Output	A 256K byte ROM Chip Select signal either from the banked ROM or ROM file – the third lowest ROM Chip Select signal
52	Vss	—	
53	$\overline{RCS13}$		Lowest 256K byte ROM Chip Select signal
54	$\overline{RCS11}$		The second lowest 256K byte ROM Chip Select signal

Connection Pin No.	Signal Name	Input/output	Function
55	RD5	Input/output	Memory or modem data bus line 5
56	RD0	Input/output	Memory or modem data bus line 0
57	RD3	Input/output	Memory or modem data bus line 3
58	RD2	Input/output	Memory or modem data bus line 2
59	RD7	Input/output	Memory or modem data bus line 7
60	RD6	Input/output	Memory or modem data bus line 6
61	RD4	Input/output	Memory or modem data bus line 4
62	RD1	Input/output	Memory or modem data bus line 1
63	NC	—	
64	$\overline{CLK}$	Input	Main Frame system bus clock signal – 180 degree shifted from the system clock signal
65	$\overline{M1}$	Input	Main Frame system bus M1 signal
66	$\overline{RESET}$	Input	Main Frame system bus Reset signal
67	$\overline{HALT}$	Input	Main Frame system bus Halt signal
68	$\overline{MRQ}$	Input	Main Frame systme bus Memory Request signal
69	$\overline{WAIT}$	Output	Main Frame system bus Wait signal
70	$\overline{WR}$	Input	Main Frame system bus Write signal
71	RD	Input	Main Frame system Read singla
72	D2	Input/output	Main Frame system data bus line 2
73	V_{DD}	—	
74	D3	Input/output	Main Frame system data bus line 3
75	D0	Input/output	Main Frame system data bus line 0
76	D6	Input/output	Main Frame system data bus line 6
77	D1	Input/output	Main Frame system data bus line 1
78	D4	Input/output	Main Frame system data bus line 4
79	D5	Input/output	Main Frame system data bus line 5
80	D7	Input/output	Main Frame system data bus line 7