INTRODUCTION
TO
INTEGRATED CIRCUIT TESTING

FAIRCHILD

INTRODUCTION TO INTEGRATED CIRCUIT TESTING

A Special Course for Secretaries
(and other interested persons)

PURPOSE OF COURSE

To help secretaries and other non-technical clerical support personnel to understand, from a layman's viewpoint, some of the "why's" and "how's" of integrated circuit testing. The student will also be exposed to the FST product line of testers to a depth that will allow her/him to better understand some of the day-to-day tester oriented language that she/he deals with in the course of her/his normal job activities.

COURSE OBJECTIVES

At the completion of this course, the student will be able to:

1. Recognize an Integrated Circuit at sight.
2. Understand, in general, what an Integrated Circuit is and some of it's many applications.
3. Understand, in general, why Integrated Circuit testing is required and what Fairchild's role in that industry is.
4. Recognize a Sentry or Xincom test system at sight.
5. Perform simplified operator functions, as defined by the instructor, which will result in an integrated circuit being tested.

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COURSE OUTLINE

MONDAY

I Course Orientation

- a. Introductions
- b. Purpose of course
- c. Course objectives

II An Introduction to Integrated Circuits

- a. What's an Integrated Circuit?
- b. Digital Integrated Circuit operation - greatly simplified!

TUESDAY

III An Introduction to Digital Integrated Circuit Testing

- a. Why test?
- b. Who uses IC testers?
- c. Applications
- d. Types of tests normally performed
- e. Sentry testing techniques - simplified

WEDNESDAY

IV The Computer - Heart of the Test System

- a. Fundamentals of EDP - an A/V media presentation
- b. An overview of computer programming

THURSDAY

V FST Product Line Description

- a. Sentry
- b. Xincom
- c. Others

FRIDAY

VI Laboratory

- a. Demonstration of system operation
- b. Students perform selected lab exercises

VII Commencement Exercises

WHAT CAN BE TESTED?

DIGITAL INTEGRATED CIRCUITS
(MOS OR BI-POLAR)

INCLUDING:

- MEMORIES (RAM, ROM) – PPM
- CALCULATOR CHIPS
- WATCH CHIPS
- MICROPROCESSORS – ≥PM
- SIMPLE GATES

TYPICAL APPLICATIONS

* ENGINEERING EVALUATION
* DEVICE CHARACTERIZATION
* MONITOR PROCESS CONTROL
* FINAL TEST
* QUALITY CONTROL

* INCOMING INSPECTION
* PRODUCTION TESTING

TYPES OF TESTS

* FUNCTIONAL TESTING
  - LOW SPEED — 25 HZ
  - HIGH SPEED (DYNAMIC) — 10MHZ
* D.C. (STATIC) PARAMETRIC TESTING
* A.C. (DYNAMIC) PARAMETRIC TESTING

FUNCTIONAL TESTING

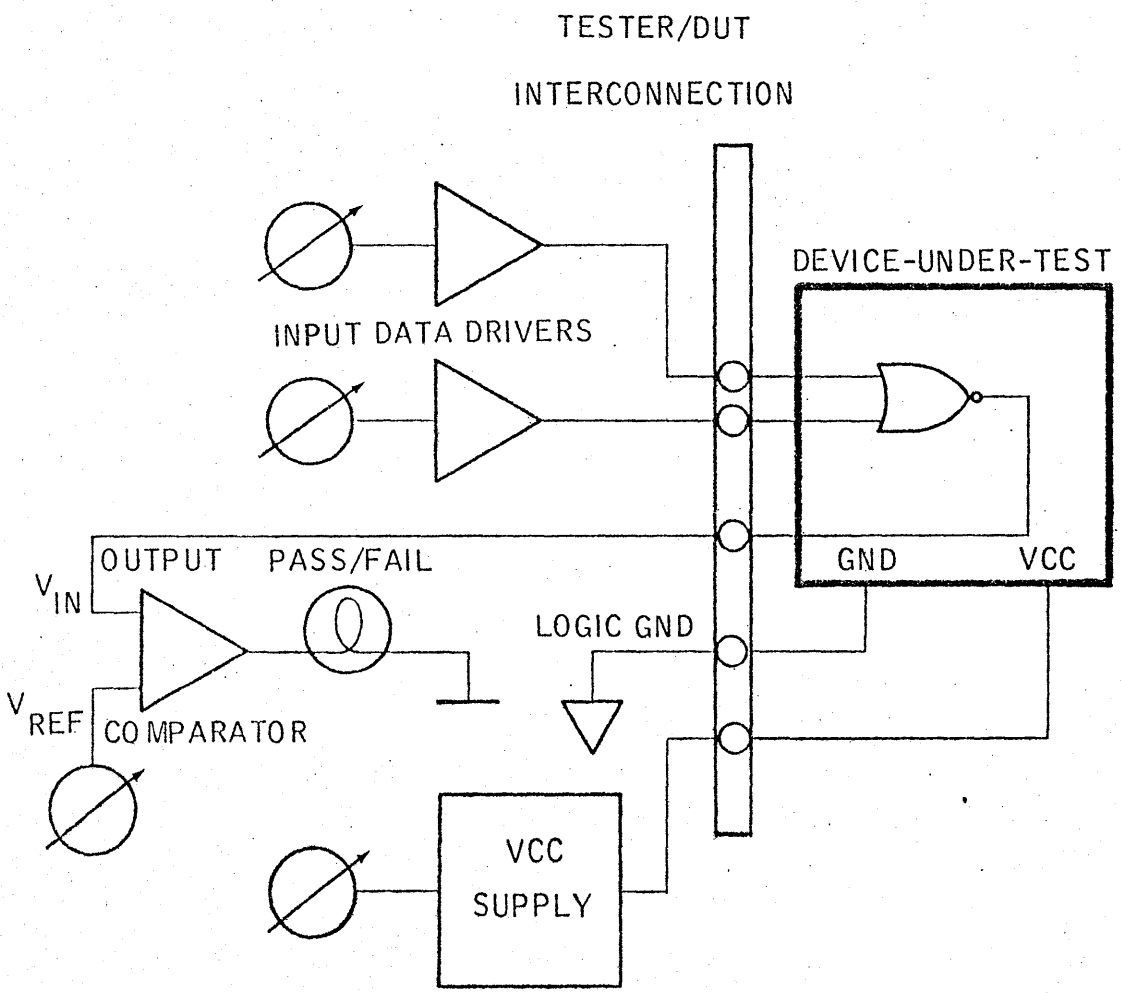
TESTING THE LOGICAL OPERATION OF A DIGITAL ELECTRONIC CIRCUIT BY EXECUTING THE CONDITIONS SHOWN IN A LOGICAL OR VOLTAGE TRUTH TABLE.

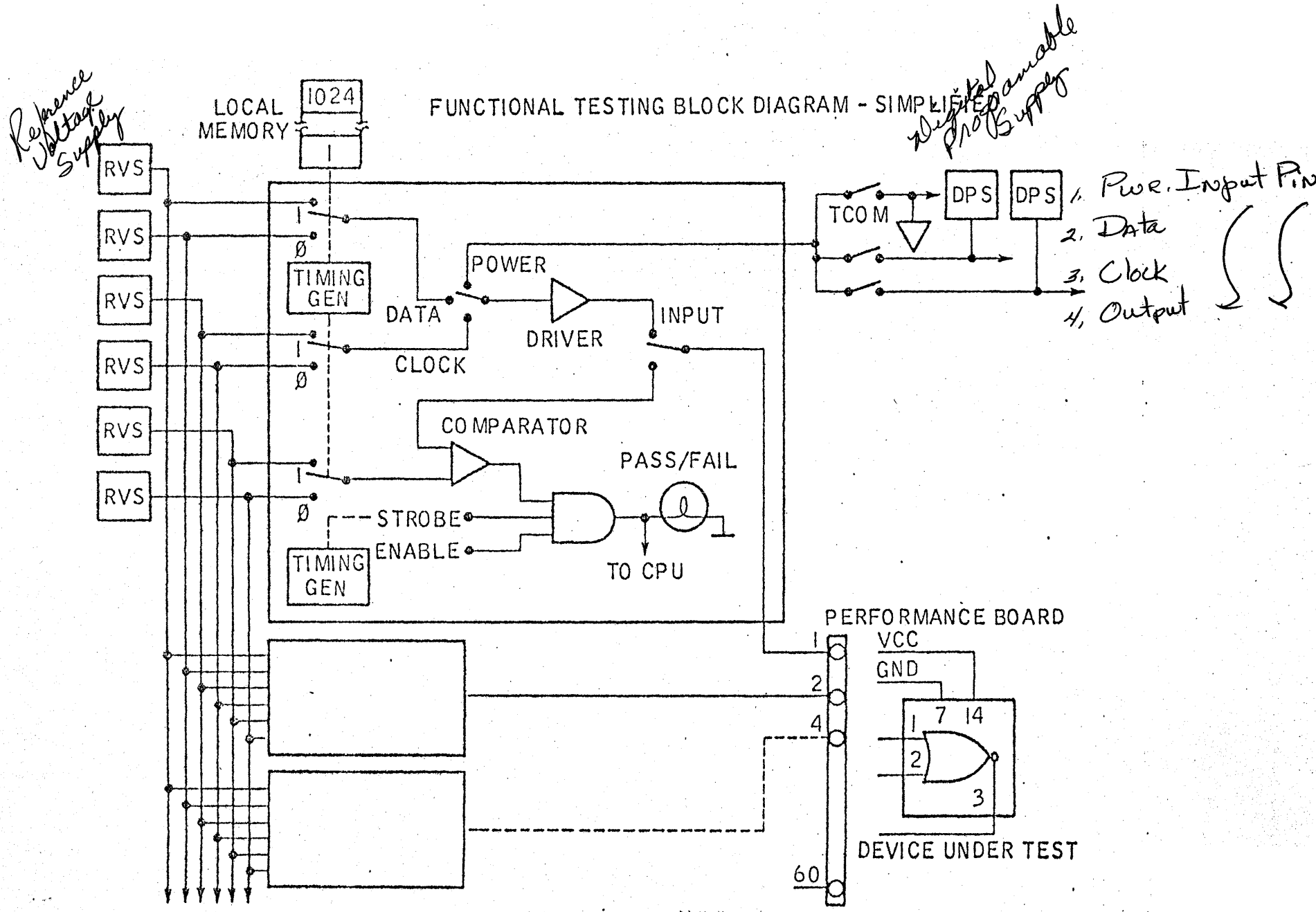
VOLTAGE TRUTH TABLE

1	2	3
L	L	H
H	L	L
L	H	L
H	H	L

LOGICAL TRUTH TABLE

1	2	3
0	0	1
1	0	0
0	1	0
1	1	0


TESTER/DUT
INTERCONNECTION
DEVICE-UNDER-TEST
INPUT DATA DRIVERS
GND
VCC
OUTPUT
PASS/FAIL
V_{IN}
LOGIC GND
V_{REF}
COMPARATOR
VCC
SUPPLY

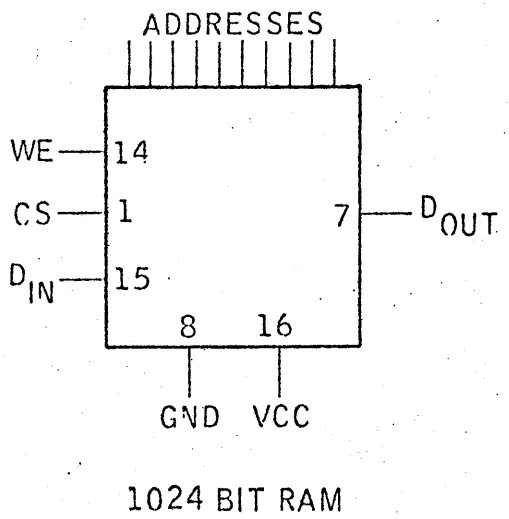

FUNCTIONAL TESTING BLOCK DIAGRAM - SIMPLIFIED
Reference Voltage Supply
LOCAL MEMORY
1024
RVS
RVS
RVS
RVS
RVS
RVS
TIMING GEN
DATA
CLOCK
POWER
DRIVER
INPUT
COMPARATOR
PASS/FAIL
STROBE
ENABLE
TIMING GEN
TO CPU
Digitally Programmable Pro Supply
TCOM
DPS
DPS
1. Pwr. Input Pin
2. Data
3. Clock
4. Output
PERFORMANCE BOARD
1
2
4
60
VCC
GND
1
7
14
2
3
DEVICE UNDER TEST

1 = Input
0 = Output

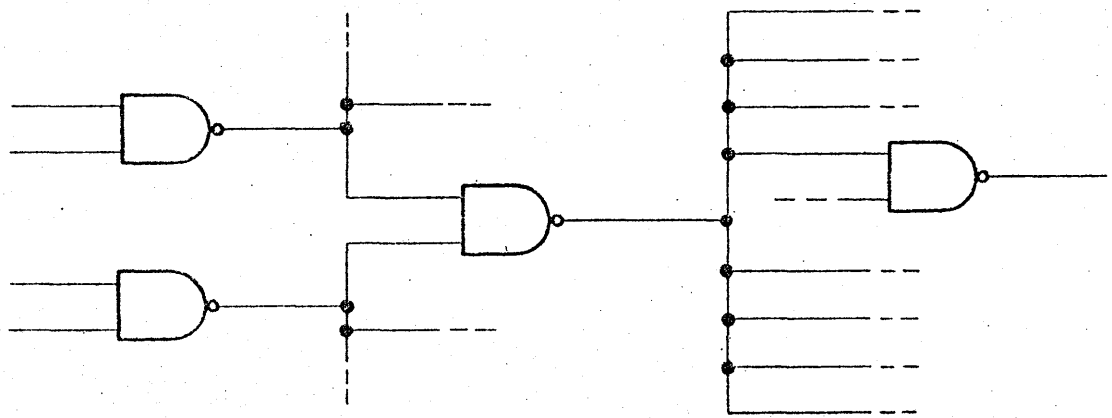
```
SET PAGE 1024;
SET DA 11000001 00000001;
SET MA 001;
CONN TCOM 7;
CONN DPSI 14;
FORCE VFI 5, RNG2;
FORCE E0 0.9, RNG2;
FORCE EI 1.7, RNG2;
SET S0 0.4, RNG2;
SET SI 2.4, RNG2;
SET TG7 DELAY 50E-9, RNG0;
SET TG7 WIDTH 20E-9, RNG0;
SET PERIOD 100E-9, RNG0;
SET F 001;
SET F 100;
SET F 001;
SET F 010;
SET F 001;
ENABLE TEST;

END;
```

```
SET PAGE 1Ø24;
SET DA IIIIIIOIIIIIIII;
SET MA ØØØØØØI;
        :
FORCE EAØ1.7, RNG2;
FORCE EAI Ø.9, RNG2;
        :
CONN CLK 14;
SET TGI DELAY 4ØE-9,RNGØ;
SET TGI WIDTH 60E-9, RNGØ;
CGEN TGI 14;
        :
SET F ØxxxxxIØxxxxxIIØ
        :
SET F ØxxxxxØxxxx
SET F ØxxxxxOxxxxxØxØ
        :
ENABLE TEST;
        :
```



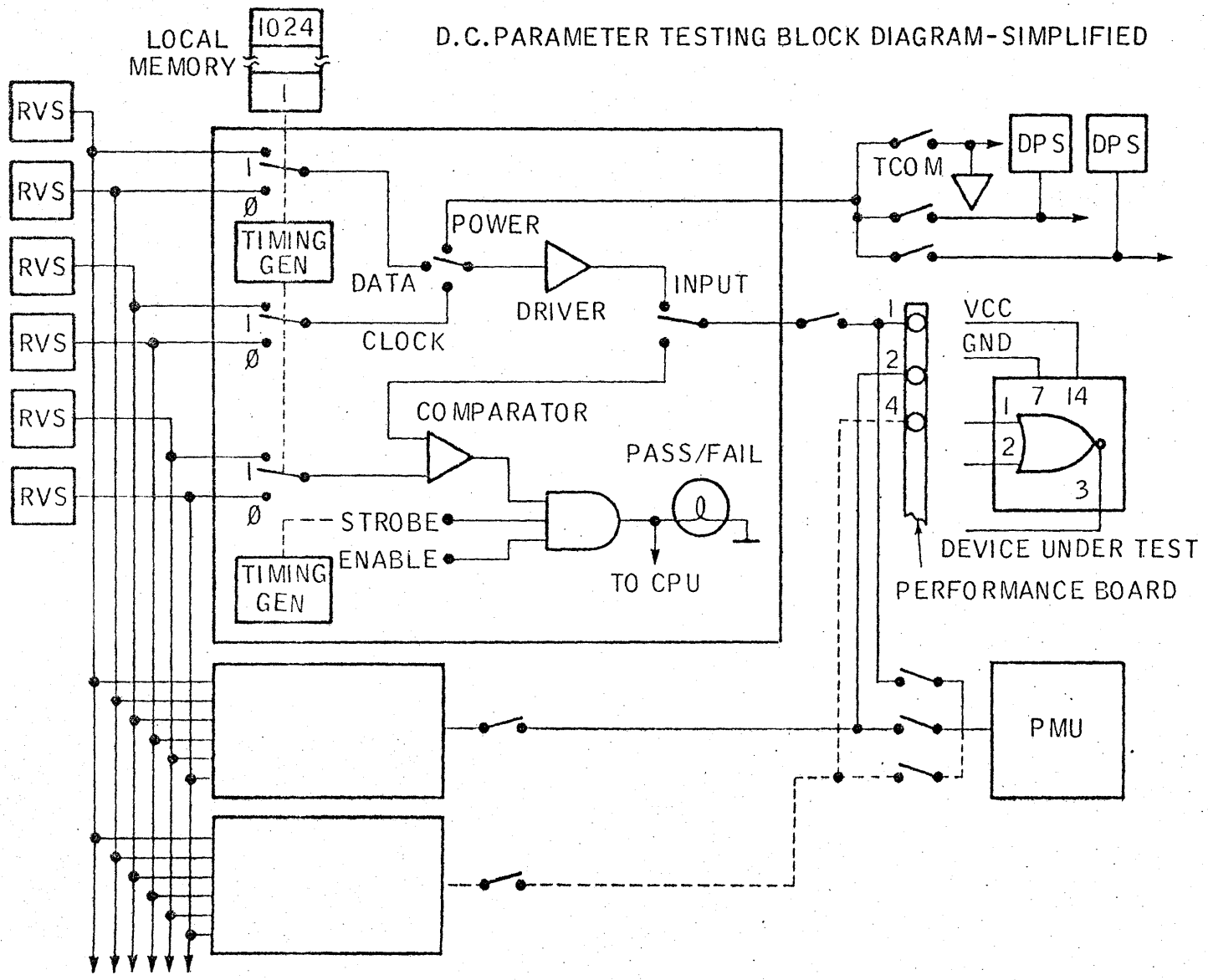
1024 BIT RAM



DEFINITION: D.C. PARAMETER TESTING

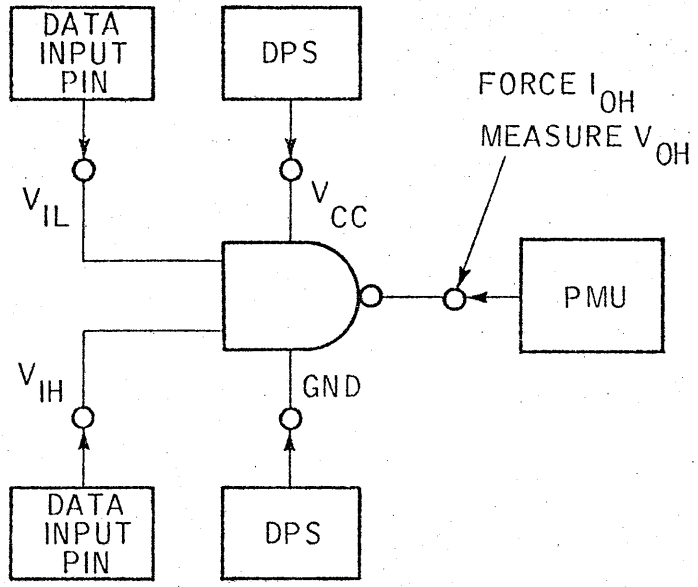
D.C. PARAMETER TESTING (OR "STATIC TESTING") IS CONCERNED WITH THE MEASUREMENT OF VOLTAGE AND CURRENT CHARACTERISTICS (OR "PARAMETERS") OF AN ELECTRONIC CIRCUIT.

THIS IS ACCOMPLISHED DURING TIME INTERVALS WHICH ARE VERY LONG, AS COMPARED WITH THE NORMAL SWITCHING SPEEDS OF THE DEVICE UNDER TEST - I.E., THE INPUTS ARE HELD CONSTANT UNTIL THE OUTPUTS STABILIZE.


D.C. PARAMETER TESTING BLOCK DIAGRAM-SIMPLIFIED
LOCAL MEMORY
1024
RVS
RVS
RVS
RVS
RVS
RVS
TIMING GEN
POWER
DATA
CLOCK
DRIVER
INPUT
COMPARATOR
PASS/FAIL
STROBE
ENABLE
TO CPU
TIMING GEN
TCOM
DPS
DPS
VCC
GND
DEVICE UNDER TEST
PERFORMANCE BOARD
PMU

TYPICAL DC PARAMETRIC TESTS

* INPUT VOLTAGE BREAKDOWN
* INPUT FORWARD CURRENT
* INPUT REVERSE CURRENT
* OUTPUT FAN-OUT CURRENTS
* POWER DISSIPATION



VOH TEST SET-UP

```
                    ¦
                    ¦
SET F ØØ1;
ENABLE TEST;
FORCE VFI 4.5, RNG2;
                    ¦
                    ¦
ENABLE DCTO LT 2.4;
SET PMU SENSE, RNG2;
FORCE CURRENT 0, RNG2;
SET DELAY 3E-3, DC;
CPMU PIN 3;
FORCE CURRENT -Ø.36E-3, RNG2;
MEASURE VALUE;
FORCE CURRENT Ø, RNG2;
XPMU PIN;
                    ¦
                    ¦
                    ¦
END;
```