GIMIX DMA DOUBLE DENSITY DISK CONTROLLER #68
for the SS-50 and SS-50C bus

The GIMIX DMA (Direct Memory Access) DISK CONTROLLER has the capabilities needed to realize the full potential of todays sophisticated multi-user/ multi-tasking operating systems such as OS-9™ and UniFLEX™.

FEATURES

HIGH SPEED using bi-polar logic DMA circuitry for guaranteed operation at 2MHz. DMA transfers take place at full bus speed using 6809 cycle steal DMA . Once the required parameters are passed to the controller and DMA transfer is initiated the processor is free for other tasks. Interrupts can be generated to indicate the completion of the transfer.

SINGLE AND DOUBLE DENSITY data storage on any combination of 5¼" and 8" floppy disk drives; single and double headed, single and double track density, up to 4 drives total.

LOW ERROR RATES are insured by a phase lock data recovery circuit (data separator) and adjustable write precompensation circuitry for drives that require precomp. Separate precomp adjustments are provided for 5¼" and 8" drives.

ADDRESSABLE to any 8 byte boundary in the address space (1M byte when extended address decoding is used). The board occupies only 8 bytes of address space.

EXTENDED ADDRESSING control using the SS-50C extended address lines. Control of the extended address lines allows the board to perform DMA transfers to and from any address in the 1M byte address space.

FULLY BUFFERED with separate 5¼" and 8" output buffers and schmidt trigger input buffers for the disk drive signals.

The DMA controller leaves the processor free to perform other tasks once the transfer is initiated, unlike programmed I/O disk controllers which require full time use of the processor during data transfers to and from disk. This is extremely important in a multi-user/ multi-tasking environment as the processor can perform other tasks such as console I/O while a disk transfer is in progress.

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JUMPER OPTIONS

The controller has several option jumpers which must be properly set before the board can be used. Several of the options are related to the type of drives being used. In most cases proper jumper settings for several different drives are given. If the drives being used are not listed, the drive manufacturer's documentation should be consulted to help determine the proper settings. The remaining option jumpers are related to the operating system software and the system hardware configuration. The proper jumper settings for use with GIMIX versions of 6809 FLEX™ are listed in this manual. For other operating systems consult the software documentation for information on proper settings for these jumpers.

5¼" READY OPTION JUMPER (JA-1)

While most 5¼" drive manufacturers use "standard" pinouts for their drive cables, some drives have non-standard pinouts for features not found on all drives. In particular; MICROPOLIS, TEAC, and BASF drives use pin 6 for the READY output from the drive. MICROPOLIS and TEAC use pin 34 for the fourth DRIVE SELECT input. Other drives, such as QUME and the SHUGART SA410/SA460, use pin 34 for READY and pin 6 for the fourth DRIVE SELECT.

Jumper area JA-1 (see sheet 1 of the jumper options drawings), in conjunction with JA-3 (below), reconfigures pins 6 and 34 of the 5¼" drive connector J-1 as required by the drives being used.

When 5¼" drives without a READY output are used this option must be disabled as in Figure B. Figures C and D show the proper jumper settings for several drives that have a READY output.

5¼" HEAD LOAD OPTION (JA-2)

MICROPOLIS and TEAC drives have a separate HEAD LOAD input on pin 2 of the drive cable. JA-2 (see sheet 1, figure E of the jumper options drawings) should be set according to either figure F or G depending on the drives being used.

5¼" DRIVE SELECT #3 OPTION JUMPER (JA-3)

Most 5¼" drives use pin 6 of the drive cable as the fourth DRIVE SELECT input (drive #3). MICROPOLIS and TEAC drives use pin 34 for this input. JA-3 (see sheet 1, figure H of the jumper options drawings) should be set according to either figure I or J depending on the drives being used.

DRIVE SELECT OPTION (JA-4)

This option enables the drive select outputs of the controller either: whenever the MOTOR-ON line is active (drive motors are on), or only when the HEAD-LOAD output of the 1797 is active. In the drive select with motor-on position (see sheet 1, figure L of the jumper options drawings) the drive select outputs of the controller are enabled whenever the motors are on. This configuration is preferred when double headed drives are used, as it limits the number of times the heads are loaded and unloaded. In the drive select with head load position (see sheet 1, figure M of the jumper options drawings) the drive select outputs of the controller are only enabled when the HEAD-LOAD output of the 1797 is active. This configuration is preferred when using single headed drives.

SIDE SELECT OPTION JUMPER (JA-5)

This option allows the side select output, for double headed drives, to be controlled by either the side select output of the 1797 or by bit 6 in the boards DMA CONTROL REGISTER. This option is normally factory jumpered for side select from the DMA CONTROL REGISTER (see sheet 1, figure O of the jumper options drawings). This is the standard configuration for GIMIX 6809 FLEX™ and other operating systems for this controller. If a special application requires side select from the 1797, a trace must be cut and a solder jumper added to connect the pads as shown in sheet 1, figure P.

5¼" and 8" PRECOMP OPTION JUMPER (JA-6)

Write Precompensation (precomp) is recommended by many drive manufacturers, when their drives are used for double density recording. Some drives require precomp on all tracks, while others, certain 8" and 5¼" 96 TPI (80 track), only require precomp on tracks greater than track #43. JA-6 (see sheet 1, figure T of the jumper options drawings) is used to select the proper precomp option(s) for the drives being used. Figures U, V, and W show the options for 5¼" drives and figures X and Y show the options for 8" drives. If a combination of 5¼" and 8" drives is being used, jumpers should be installed to select the proper option for both drive sizes. For example: if 5¼" drives that require precomp on all tracks and 8" drives that require precomp are combined, install jumpers as shown in BOTH figures V AND Y. If only one size drive is used, install the appropriate jumper for that size drive. The second jumper should be installed at any of the positions for the unused drive size.

Drive manufacturers also specify a certain amount of precomp, usually between 100 and 400 ns. The board has provisions for separately adjusting the amount of precomp for 5¼" and 8" drives. If the controller is purchased as part of a complete disk based system, the precomp is factory adjusted for the drives supplied. If purchased separately, the controller is adjusted to 150 ns. for 5¼" drives and 175 ns. for 8" drives, or to the requirements of the drives being used, if specified when the controller was ordered.

The adjustments section explains the procedure for adjusting the board for the desired amount of precomp.

Consult the manufacturers literature to determine the precomp requirements of the drives being used.

8" MOTOR-ON DELAY OPTION JUMPER (JA-7)

Disk drives normally require a certain amount of delay for the motors to come up to speed after they are started. This delay is provided by a timing circuit on the controller. If 8" drives that do not have motor control (the motors are always running) are used this delay can be eliminated. JA-7 (see sheet 1, figure Q of the jumper options drawings) enables or disables the motor-on delay as required.

If 8" drives without motor control are used position the jumper as shown in figure R. If drives with motor control are used position the jumper as shown in figure S.

5¼" HEAD-LOAD DELAY OPTION JUMPER (JA-8)

Most disk drives have a solenoid that loads and unloads the head(s). These drives require a delay, after the heads are loaded, to allow time for the head(s) to settle. This delay is provided by a timing circuit on the controller. Some 5¼", double headed drives do not have a head load solenoid and the head is loaded as soon as the door is closed. These drives do not require any head load delay.

JA-8 (see sheet 2, figure A, of the jumper options drawings) allows the 5¼" head-load delay to be disabled when drives without head-load solenoids are used, figure B, or enabled for drives with a head-load solenoid, figure C.

6800/6809 SLOW MEMORY SELECT OPTION JUMPER (JA-9)

Because of the timing requirements of the 1797, slow memory (MRDY) circuitry is required, at bus speeds above 1 MHz., to stretch the system clock whenever the 1797 is accessed. JA-9 (see sheet 2, figure D, of the jumper options drawing) selects the proper slow memory (MRDY) timing for use with either the 6800 or the 6809 processor. This option is factory jumpered in the 6809 position, figure E, to select the 6800 option see figure F.

SOFTWARE WRITE PROTECT OPTION (JA-10)

JA-10 (see sheet 2, figure G, of the jumper options drawings), in conjunction with bit 4 of the boards DRIVE SELECT REGISTER, allows the disk drives to be write protected under software control. When this option is enabled, figure H, and bit 4 of the DRIVE SELECT REGISTER is set low (0), all drives are write protected and no disk write operations are possible until bit 4 is set high (1). Since all bits in the DRIVE SELECT REGISTER are set low on system power up, bit 4 must be set high (1) after power up to enable disk writes. When this option is disabled, figure I, write protect is controlled only by the write protect signals from the individual drives.

JUMPER AREA (JA-11) is reserved for future use.

BA/BS OPTION JUMPER (JA-12)

DMA transfers to and from the board require a signal from the processor indicating that the bus is available to the controller. This signal is provided by the BUS AVAILABLE (BA) and BUS STATUS (BS) lines of the 6809 or the BUS AVAILABLE (BA) line of the 6800. JA-12 (see sheet 2, figure M, of the jumper options drawings) is used to select either 6809 , figure N, or 6800, figure O, operation. JA-12 is factory jumpered for 6809 operation, figure N.

DMA OPTION JUMPER (JA-13)

The board is designed to use one of two different DMA methods, depending on which processor (6800 or 6809) is being used. JA-13 (see sheet 2, figure P, of the jumper options drawings) connects the DMA request signal from the board to either the BUSRQ line (6809) , figure Q, or to the HALT line (6800), figure R. JA-13 is factory jumpered for 6809 DMA using the cycle steal method.

SLOW MEMORY OPTION JUMPER (JA-14)

Because of the timing requirements of the 1797, slow memory (MRDY) circuitry is required, at bus speeds above 1 MHz.,to stretch the system clock whenever the 1797 is accessed. JA-14 (see sheet 2, figure S, of the jumper options drawings) connects the slow memory signal from the board to the proper bus line for the processor being used.

In systems operating at 1 MHz. (6800 or 6809) JA-14 should be jumpered as shown in figure T (slow memory disabled). For 6809 systems operating above 1 MHz. jumper JA-14 as shown in figure U (slow memory to MRDY). For 6800 systems operating above 1 MHz. JA-14 can be jumpered as shown in either figure V (slow memory to UD-1), or figure W (slow memory to UD-2). The choice between UD-1 and UD-2 will depend on the system configuration and the 6800 processor board being used.

INTERRUPT OPTION JUMPER (JA-15)

JA-15 (see sheet 2, figure X, of the jumper options drawings) is used to connect the interrupt output (INTRQ) from the 1797 to one of the interrupt lines of the bus. If interrupts are not used, jumper JA-15 as shown in figure Y . Figures Z, AA, and BB, show the proper jumper positions for generating interrupts on the NMI, FIRQ (6809 only), or IRQ lines respectively.

DIP-SWITCH OPTIONS

ADDRESSING OPTIONS (S1 and S2 sections 1 through 8)

The board occupies 8 bytes of address space (4 for the board registers and 4 for the 1797 registers) and can be addressed to any 8 byte boundary in the address space. Extended address decoding (SS-50C) is provided. DIP-switch S1 section 1 (S1-1) enables or disables the extended address decoding for the board.

If S1-1 is OFF (OPEN) extended address decoding is disabled and the board only decodes the 16 regular address lines, A0 through A15. DIP-switch S1 sections 6 through 10 correspond to address lines A3 through A7 respectively. DIP-switch S2 sections 1 through 8 correspond to address lines A8 through A15 respectively. These switches must be set to the desired base address of the board. A switch set ON (CLOSED) corresponds to a 1 (HIGH) on that address line and a switch set OFF (OPEN) corresponds to a 0 (LOW).

If S1-1 is ON (CLOSED) the board decodes all 20 SS-50C address lines, A0 through A19 and, in addition to setting the base address of the board, S1-2 through 5 must be set to the desired extended address. DIP-switch S1 sections 2 through 5 correspond to the extended address lines A16 through A19 respectively. A switch set ON (CLOSED) corresponds to a 1 (HIGH) on that address line. A switch set OFF (OPEN) corresponds to 0 (LOW).

STANDARD GIMIX FLEX CONFIGURATION BOOTING ON A 5¼" DRIVE

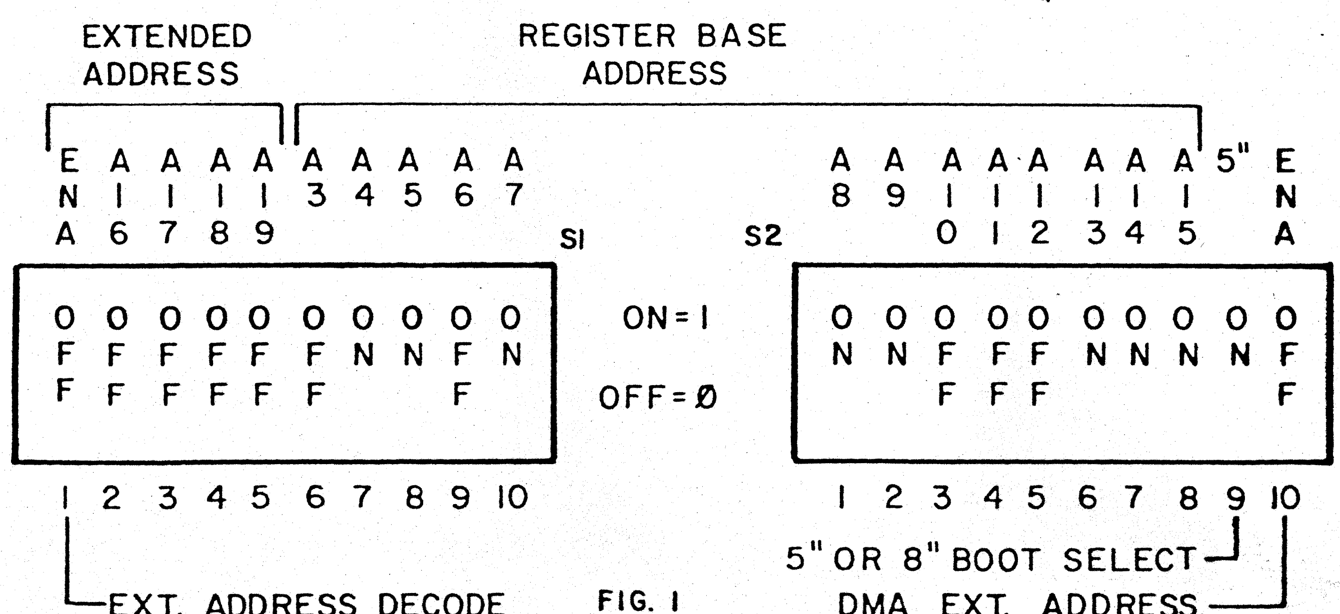


FIG. 1

5¼" or 8" SENSE SWITCH (S2 section 9)

Bit 0 of the DRIVE SELECT REGISTER is provided to allow the size (5¼" or 8") of the drive installed as drive 0 to be determined by software. The status of this bit is determined by setting S2-9. If drive 0 is a 5¼" drive, S2-9 should be set ON (CLOSED). If drive 0 is an 8" drive, set S2-9 OFF (OPEN).

DMA EXTENDED ADDRESS OPTION (S2 section 10)

The board is capable of driving the SS-50C extended address lines, A16 through A19, during DMA transfers. This allows the board to perform DMA transfers to and from any address in the 1M byte address space of the SS-50C bus. If S2-10 is OFF (OPEN) this option is disabled and the controller only drives the 16 regular address lines A0 through A15. If S2-10 is ON (CLOSED) the controller drives all 20 address lines of the S-50C bus. The address presented on the 4 extended address lines is determined by the data stored in the lower 4 bits of the DMA CONTROL REGISTER. Bits 0 through 3 of the DMA CONTROL REGISTER correspond to extended address lines A16 through A19 respectively.

BOARD REGISTERS

The board occupies 8 memory locations and can be addressed to any 8 byte boundary in the address space (1M BYTE with extended addressing). The following table lists the functions of the 8 locations and assumes that the board is set to the standard GIMIX FLEX™ address, $E3B0.

Base address	$E3B0	Drive Select Register	(write)
		DMA Status Register	(read)
	$E3B1	DMA Control Register	(write only)
	$E3B2	DMA Starting Address	(MSB)
	$E3B3	DMA Starting Address	(LSB)
	$E3B4	1797 Command/Status register	
	$E3B5	1797 Track Register	
	$E3B6	1797 Sector Register	
Base address +7	$E3B7	1797 Data Register	

The four 1797 registers are internal registers in the 1797 floppy disk controller I.C. Information on their functions and programming can be found in the manufacturers data sheets for the 1797.

NOTE: Accessing any of the 1797 registers starts the drive motors.

The first four registers control various functions as described below. The addresses in parenthesis are the standard GIMIX FLEX™ addresses for these registers.

DRIVE SELECT REGISTER ($E3B0 Write only)

MSB	BIT 7	RESERVED	Reserved for future use.
	BIT 6	CONNECTOR SELECT 0 = 5¼" 1 = 8"	Selects between the 5¼" and 8" drive connectors. Also selects the proper data separator rate and precomp.
	BIT 5	DENSITY SELECT 0 = Double den. 1 = Single den.	Selects between single and double density operation. Selects proper data separator rate and enables precomp for double den.
	BIT 4	WRITE PROTECT 0 = W/protect 1 = W/enable	Write protects all drives when enabled. SOFTWARE WRITE PROTECT OPTION JA-10 must be enabled to use this feature.
	BIT 3	DRIVE SEL. 3	Bits 0 through 3 perform a 1 of 4 drive select function. Any bit set to a 1 selects the associated drive. Only one of the four drives select bits should be a 1 to prevent multiple drives from being selected. 0 = drive selected 1 = drive deselected
	BIT 2	DRIVE SEL. 2	
	BIT 1	DRIVE SEL. 1	
LSB	BIT 0	DRIVE SEL. 0	

Note: All bits in the DRIVE SELECT REGISTER are cleared to 0 on power up and hardware reset.

DMA STATUS REGISTER ($E3B0 Read only)

MSB	BIT 7	DRQ FLAG	This bit is the same as the DRQ bit in the 1797 status register and the output of the 1797 DRQ signal. See the 1797 data sheet.
	BIT 6	INTRQ FLAG 0 = No INTRQ 1 = INTRQ	Indicates the state of the INTRQ interrupt output from the 1797. This bit is set to a 1 when an interrupt is generated an cleared to 0 when the 1797 status register is read. Active even when bus interrupts are disabled.
	BIT 5	MOTOR DELAY FLAG 0 = Running 1 = Starting	Indicates that the drive motors were stopped then restarted. Used to eliminate software timing when checking for "drives ready".
	BIT 4	DMA ENABLED FLAG 0 = DMA Disabled 1 = DMA Enabled	Indicates that DMA transfers are enabled and an occurence of the 1797 DRQ will cause data to be transfered between the board and memory.
	BIT 3	DMA FAULT FLAG 0 = NO DMA FAULT 1 = DMA FAULT	Indicates that a DMA transfer longer than 16,384 + or - 256 bytes was attempted and the board has stopped the transfer. This can occur because of a hardware fault or if a drive door is opened during a track write (formatting).

NOTE: Data must be written to the DMA STARTING ADDRESS REGISTER (LSB) to reset the DMA FAULT counter and prevent false DMA FAULTS from occuring.

	BIT 2	CONNECTOR SELECT FLAG 0 = 5¼" 1 = 8"	Indicates the drive size, 5¼" or 8", currently selected by the CONNECTOR SELECT bit in the DRIVE SELECT REGISTER.
	BIT 1	RESERVED	Reserved for future use
LSB	BIT 0	SENSE SWITCH FLAG 1 = S2-9 OFF (8") 0 = S2-9 ON (5¼")	Indicates the state of the sense switch, S2-9. Used by GIMIX FLEX™ bootstrap loader to determine what size drive is installed as drive 0.

DMA CONTROL REGISTER ($E3B1 WRITE ONLY)

LSB	BIT 7	INTERRUPT ENABLE 0 = Int. Disable 1 = Int. Enable	Enables the interrupt output from the board to the bus. Interrupt jumper JA-15 must also be set for the desired interupt line. Allows software switch between interrupt and non-interrupt operation.
	BIT 6	SIDE SELECT 0 = Side Zero 1 = Side One	Used to select between side zero and side one when using double-headed drives. Side select jumper JA-5 must be set for side select from control register in order to use this bit.
	BIT 5	DMA DIRECTION 0 = READ FROM DISK 1 = WRITE TO DISK	Sets the direction for DMA transfers between disk and memory.
	BIT 4	DMA ENABLE 0 = DMA DISABLED 1 = DMA ENABLED	Enables the DMA circuitry for transfers between disk and memory. DMA must be enabled before a read or write data command is issued to the 1797.
	BIT 3	A19	Bits 0 through 3 are used to set the extended (bank) address that will be placed on the bus by the controller during DMA transfers. To use extended addressing during DMA transfers these bits must be set to the desired address and switch S2-10 must be ON (CLOSED).
	BIT 2	A18	
	BIT 1	A17	
LSB	BIT 0	A16	

DMA STARTING ADDRESS REGISTERS ($E3B2 and $E3B3 WRITE ONLY)

The source/destination address for a DMA transfer must be written to the DMA STARTING ADDRESS REGISTERS before a transfer is initiated by issuing a read or write command to the 1797. After each byte is transfered the address is automatically incremented and another byte is transfered, until the 1797 read or write operation is complete. The most significant byte of the 16 bit address is stored in the MSB register ($E3B2) and the least significant byte in the LSB register ($E3B3). If extended addressing (20 bit) is used the extended address is written to the DMA CONTROL REGISTER bits 0 through 3 (see above). Since the extended address cannot be changed while a DMA transfer is in progress, a single transfer cannot be made to or from more than one bank.

Writing to the DMA STARTING ADDRESS REGISTER (LSB) resets the DMA FAULT counter. This register must be rewritten before every DMA transfer to a false DMA FAULT from occuring.

PROGRAMMING FOR THE GIMIX DMA CONTROLLER

This section is included as a guide to the features of the board, for the user who wishes to write his own operating system or adapt the board to an existing operating system. Information on programming the 1797 can be found in the manufacturers literature.

DRIVE SELECT REGISTER (WRITE)

The functions of the DRIVE SELECT REGISTER bits are described in the preceeding section. On power up or after a system reset the following conditions exist: 5¼" drives, double density, and write protect of all drives is selected. All drives are deselected. Before a disk transfer is initiated the drive size, density, and write protect should be set as required and one of the drives selected by setting the appropriate drive select bit to a "1".

DRIVE SELECT REGISTER (READ)

Reading the DRIVE SELECT REGISTER indicates the status of various functions of the board. The basic functions of the flags are described in the preceeding section. More detailed information on those that have special significance is given below.

BIT 7: The DRQ flag is not normally used for DMA transfers, it is only required if the board is used as a programmed I/O controller.

BIT 6: In an interrupt driven system, the IRQ flag can be read to determine whether or not an interrrupt was generated by the controller. This bit should also be used, instead of the busy bit in the 1797 status register, to determine when a command has been completed. This eliminates the need for a delay loop that makes the software dependant on system clock speed. The 1797 status register must be read to clear the IRQ flag.

BIT 5: The MOTOR DELAY FLAG can be used in routines that check for "drives ready". Normally these routines must include a delay loop to insure that a "drives not ready" condition is not caused because the drive motors are not yet up to speed. The MOTOR DELAY FLAG eliminates the need for delay loops which make the software dependant on system clock speed. To use the MOTOR DELAY FLAG, first check the "drives ready" status from the 1797. If this indicates that the drives are ready, normal operation can proceed. If the drives are not ready, the MOTOR DELAY FLAG should be checked. If the MOTOR DELAY FLAG is LOW (0), the motors are at speed and the "drives not ready" can be considered valid and proper action taken to handle the error. If the MOTOR DELAY FLAG is HIGH (1), it should be rechecked until it goes LOW (0). The HIGH to LOW transition indicates that the drive motors have been on long enough to come up to speed. The "drives ready" status from the 1797 should again be checked and if it still indicates "drives not ready" the condition can be considered valid (no disk in the selected drive, door open, etc.) and proper action taken to handle the error. If it indicates that the drives are ready, normal operation can proceed.

BIT 3: Because the 1797 track read and track write commands read or write data continuously, starting when one index pulse is received from the drive and ending on the next, it is possible for control of a transfer to be lost because of a hardware failure or because the drive door is opened during a track write. If this were to occur the board would cycle continuously through the entire address range reading from memory. This runaway condition is prevented by a counter which limits the maximum transfer to 16,384 + or - 256 bytes. If the maximum count is reached the transfer is halted and the DMA FAULT FLAG is set HIGH (1) to indicate a DMA FAULT. The DMA FAULT FLAG should be checked at the completion of any 1797 track write commands to determine if a DMA FAULT has occurred. The DMA FAULT COUNTER is reset by writing to the DMA STARTING ADDRESS REGISTER (LSB). Data must be written to this register before each DMA transfer to reset the counter and prevent false DMA FAULTS.

DMA CONTROL REGISTER

The functions of the DMA CONTROL REGISTER are described in the preceeding section. More detailed information for some of the bits is given below. On power up or after a system reset all bits are cleared to 0; interrupts are disabled, side 0 and read are selected, DMA is disabled, the extended address is set to $0. These

BIT 7: This bit enables and disables the interrupt output from the board to the bus. It does not affect the interrupt flags in the DRIVE SELECT REGISTER. In an interrupt driven system, this bit must be set by the software to enable bus interrupts. The desired interrupt must also be enabled by the interrupt jumper JA-15. This option allows switching between interrupt and non-interrupt driven software without reconfiguring the board.

BIT 4: DMA must be enabled by setting this bit HIGH (1) before DMA transfers can take place. It must be set before a read or write command is issued to the 1797 or data will be lost.

DMA STARTING ADDRESS REGISTERS (MSB and LSB)

The source or destnation address for a DMA transfer must be written to these registers before the transfer is initiated. Once the transfer is started the board increments this address each time a byte is transfered. At the completion of a transfer the DMA STARTING ADDRESS REGISTERS point to the address following the last byte transfered. It is not necessary to write a new value to the MSB register if a second transfer is to be made, continuing from this address. The LSB register should be re-written, before each transfer or before 16,128 (16K-256) bytes have been transfered, to reset the DMA FAULT counter. IF THE DMA FAULT COUNTER IS NOT RESET BEFORE MORE THAN 16,128 BYTES ARE TRANSFERED A FALSE DMA FAULT WILL OCCUR, HALTING DMA TRANSFER.

HEAD LOAD DELAY

The board has two separate delay circuits, one for 5¼" drives and another for 8". The proper circuit is selected by the CONNECTOR SELECT BIT. These delays are used to provide the required settling time, after the heads have been loaded. The delay starts whenever the head load output from the 1797 (HLD) becomes active (HIGH). After the delay, the head load timing input to the 1797 (HLT) is made high indicating to the 1797 that thee heads are loaded and have had time to settle. The HLT input is also controlled by another delay circuit that provides a delay for the drive motors to come up to speed. Both the HEAD LOAD DELAY and the MOTOR-ON delay must be completed before the HLD input is made HIGH.

Once the HLD output is made active (HIGH), by issuing a command to the 1797 that loads the heads, it does not become inactive (LOW) again until it is specifically reset by issuing a command that unloads the heads or until 15 revolutions of the disk have occurred since the 1797 completed its last command.

To insure proper operation of the HEAD LOAD DELAY circuit and reliable operation of the controller: the HLD output should be made inactive by issuing a command to unload the head each time a different drive is selected. Issuing a head load command will then restart the HEAD LOAD DELAY and allow the proper head settling time.

ADJUSTMENTS

There are six trimmer potentiometers, located at the top of the board, that are used to adjust the data separator and the precomp circuits. The data separator is factory adjusted and should not require readjustment unless the trimmers are moved accidentally or a component in the data separator circuitry is replaced. The precomp circuits may require adjustment to suit the drives being used or when changing from one type of drive to another. The drive manufacturers literature should be checked to determine the precomp requirements of a particular drive.

The data separator adjustments are factory set and should not be changed. If the data separator requires readjustment please contact the facotory for information.

The following paragraphs describe the proceedure for adjusting the precomp circuits for both 5¼" and 8" drives. These adjustments require an oscilloscope with an accurately calibrated time base. Unless preformed with care and the proper test equipment, making these adjustments can cause more harm than good.

PRECOMP ADJUSTMENT

Precomp adjustment requires that the controller be installed in a functioning system, with a disk operating system that can be used to format a disk. Separate adjustments are provided for 5¼ and 8" drives.

To adjust the 5¼" precomp, connect the oscilloscope to J3 test point TP-5 (FIGURE 2 BELOW). A ground connection is also provided at J3. Set the scope to trigger on the negative going edge of the waveform. Use the operating systes "format" program to format a a 5¼" disk. The controller must be writing data to a 5¼" disk when adjusting the 5¼" precomp. Measure the width of the negative going pulse at TP-5. The width of this pulse is equal to the amount of precomp. Adjust R-28 to obtain the desired pulse-width/precomp.

The proceedure for adjusting 8" precomp is the same as the 5¼" proceedure except that the controller must be writing data to an 8" disk. Use the "format" program to format an 8" disk and adjust R-27 to obtain the desired pulse-width/precomp at TP-5.

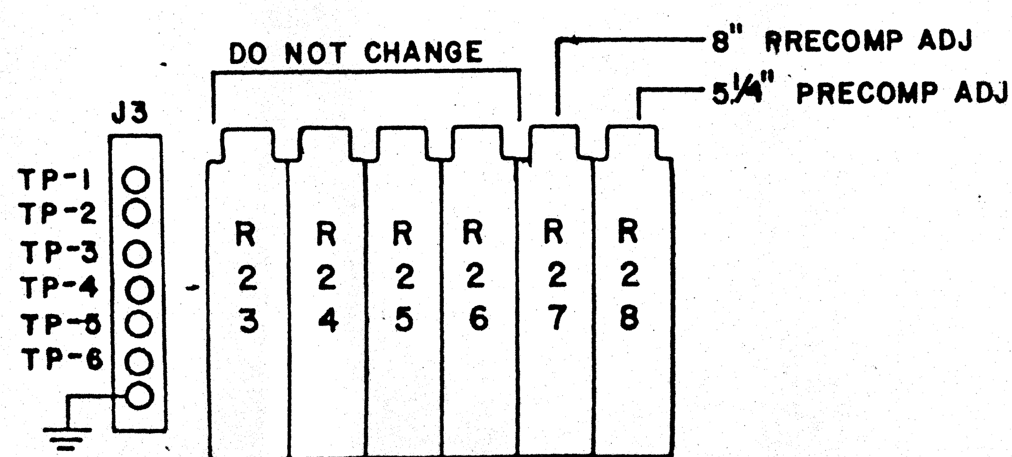


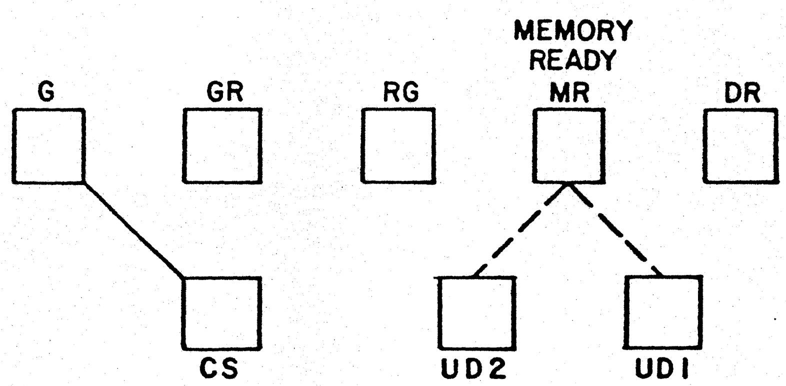
FIGURE 2

BOARD CONFIGURATION

The controller designed to work in both 6809 and 6800 systems. As delivered the boards are configured for 6809 operation and several jumpers must be change to configure the board for 6800 systems. In most cases the jumpers for 6809 operation consist of PC board traces or solder jumpers connecting the pads indicated in the jumper configuration drawings. To reconfigure the board for 6800 systems the PC board traces must be cut or the solder jumpers removed and new jumpers installed to connect the pads indicated for 6800 use. The following jumper areas must be changed for 6800 operation: JA-12 and JA-13. If the board is to be used in 6800 systems running above 1 MHz. jumper area JA-9 must also be changed and JA-14 configured for the proper 6800 slow memory option (see the following section). In 1 MHz. 6800 systems the SLOW MEMORY OPTION jumper JA-14 should be configured as shown in figure T.

6800 SLOW MEMORY

Operation in 6800 systems above 1 MHz. requires that the CPU board have provisions for a MEMORY READY (MR) input on either UD-1 or UD-2. MEMORY READY is available on the GIMIX 6800 CPU BOARD as a jumper option. To enable the MR option on the GIMIX 6800 CPU BOARD connect a wire jumper from the pad labeled "MR" (there is a mistake in the drawing included with the board, use the corrected drawing below) to the desired user defined line; either UD-1 or UD-2. Jumper area JA-14 on the disk controller should be set to match the UD line chosen on the CPU. No other modification to the system is required.



GIMIX 6800 CPU MEMORY READY JUMPER
FIGURE 3

The SWTPc MPA-2 6800 CPU board requires minor hardware modifications to provide the MEMORY READY input. To modify the MPA-2 for use with the controller above 1 MHz.: cut the small trace, on the solder side, connecting pin 6 of IC 6 (the 6875) to the large trace running between the pins of IC 6. This disconnects pin 6 of the 6875 from the +5V supply. Connect a jumper from IC 6, pin 6 to the desired user defined line: UD-1 or UD-2. Finally connect a 4.7K ohm resistor from IC 6, pin 6 to the +5V supply. This completes the MPA-2 modifications. JA-14 on the disk controller board should be set to match the UD line chosen on the CPU. No other modification is required.

DRIVE CONNECTIONS

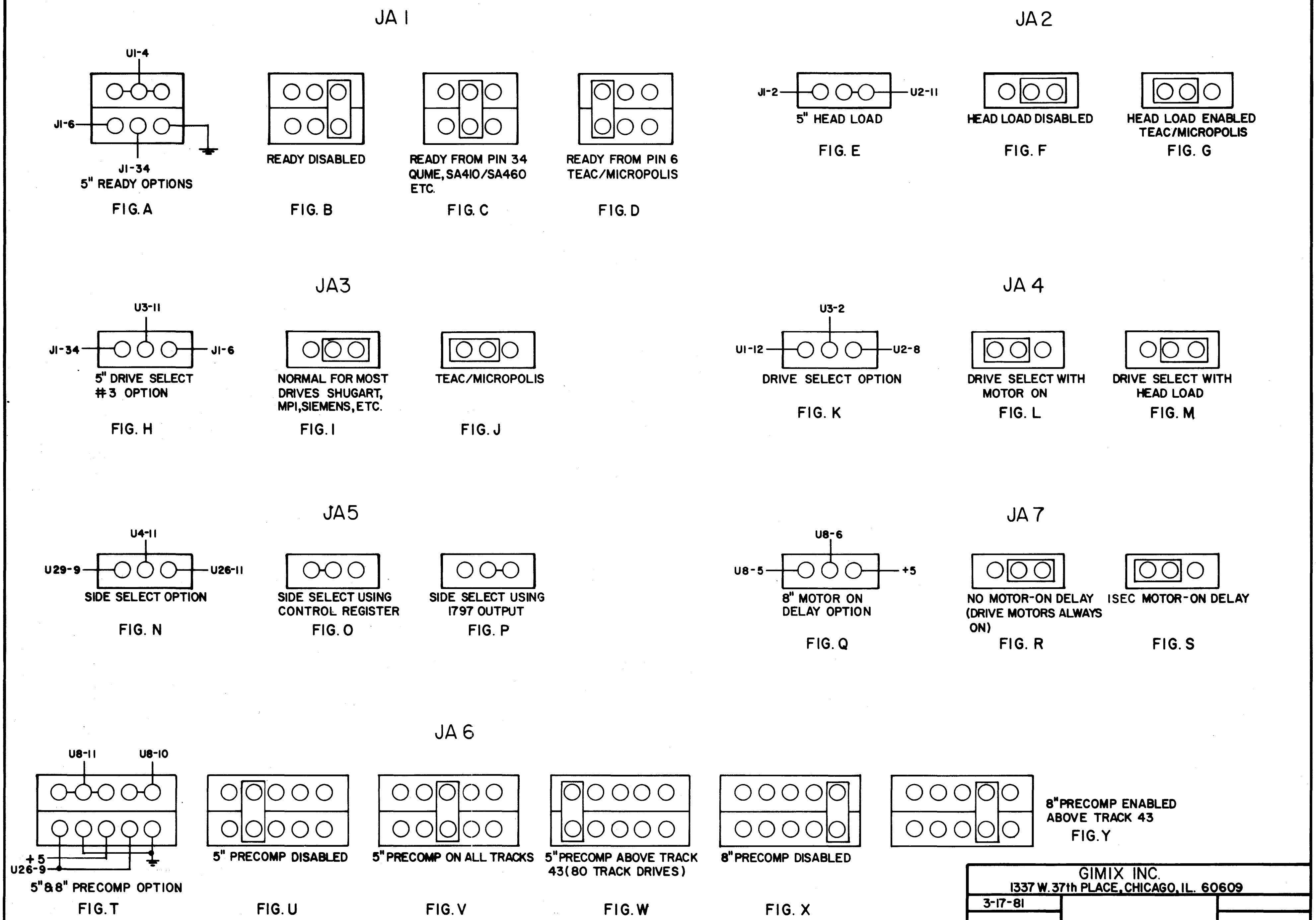
Standard 34 pin (J1) and 50 pin (J2) connectors are provided for the 5¼" and 8" drive cables respectively. The proper connector is selected automatically when the controller is switched between 5¼" and 8" drives using the CONNECTOR SELECT bit in the DRIVE SELECT REGISTER. The length of the cables between the controller and the drives should be to a minimun to reduce noise pickup. Ten feet should be considered an absolute maximum for the length of the drive cables.

DRIVE PROGRAMMING

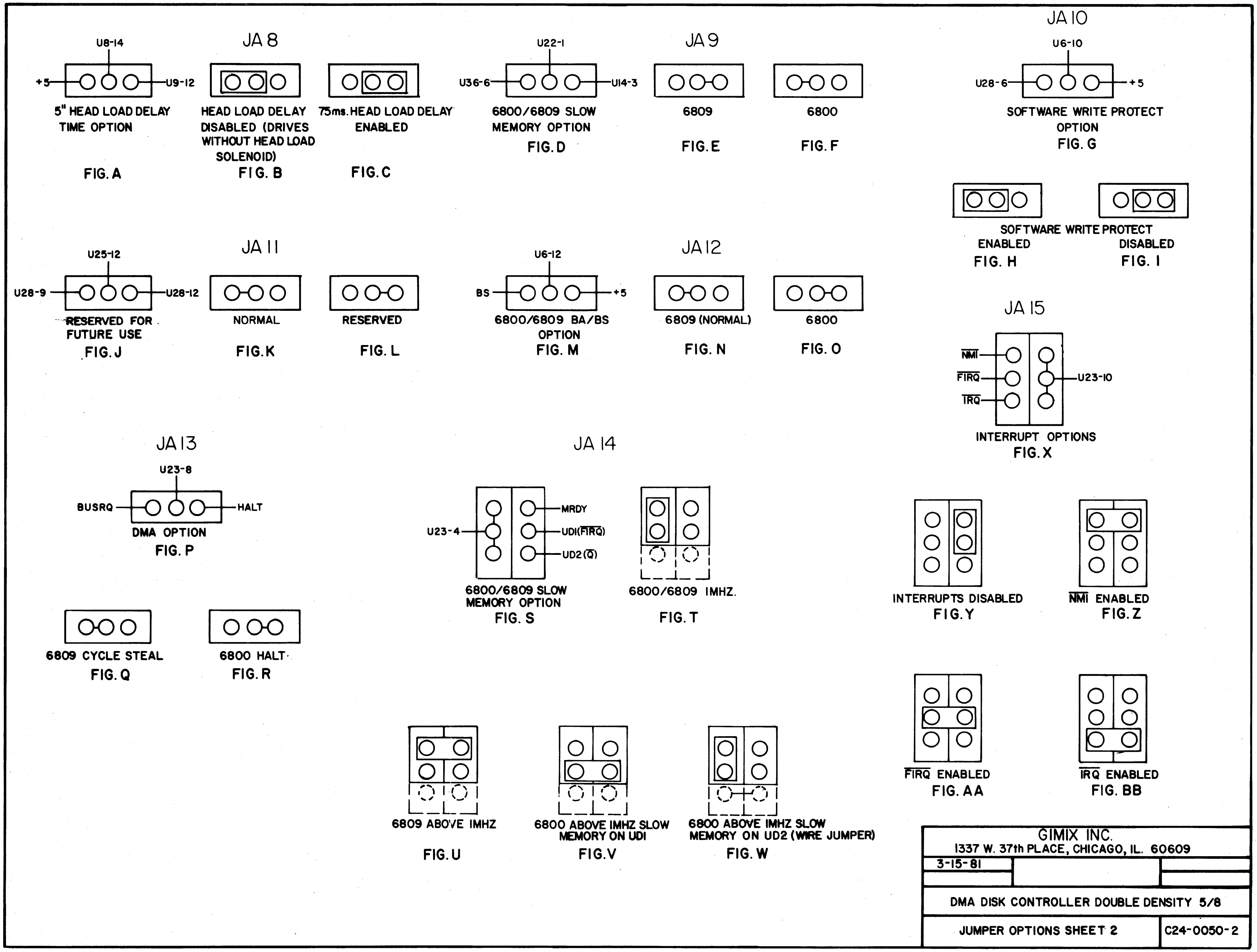
Any combination of 5¼" and 8" drives, up to four drives total, can be connected to the controller. The drives themselves must be programmed to respond to the desired drive number (drive select 0, 1, 2, or 3). See the drive manufacturers documentation for infromation on programming specific drives. If only one size drive is used the drives should be programmed in sequence starting with drive 0. If both 5¼" and 8" drives are used they can be arranged in any desired order starting with drive 0. For example: if two 5¼" and two 8" drives are used, the 5¼" drives could be programmed as drives 0 and 1, the 8" drives would then be 2 and 3, If the 8" drives were programmed as drives 0 and 1, the 5¼" would then be progammed as 2 and 3. They could also be arranged so that drives 0 and 2 are 8" and drives 1 and 3 are 5¼" etc. Regardless of the order chosen, the 5¼" or 8" SENSE SWITCH (S2 section 9) must be set to match the size of the drive programmed as drive 0.

DRIVE TERMINATION

In order for the controller to function properly, the drive cables must be properly terminated. Terminating resistors are provided on the disk drives to terminate the cables. When more than one drive is connected to a single cable the terminating resistors on all drives EXCEPT the last one on that cable (the drive farthest from the controller) must have their terminating resistors removed or disabled. Only the last drive on the cable should have a terminator. If both 5¼" and 8" drives are used the last drive on both cables must have a terminator. Consult the drive manufacturers documentation for information on removing or disabling the terminators.



GIMIX INC. 1337 W. 37th PLACE, CHICAGO, IL. 60609		
3-17-81		
DMA DISK CONTROLLER DOUBLE DENSITY 5/8		
JUMPER OPTIONS SHEET 1		C24-0050-1



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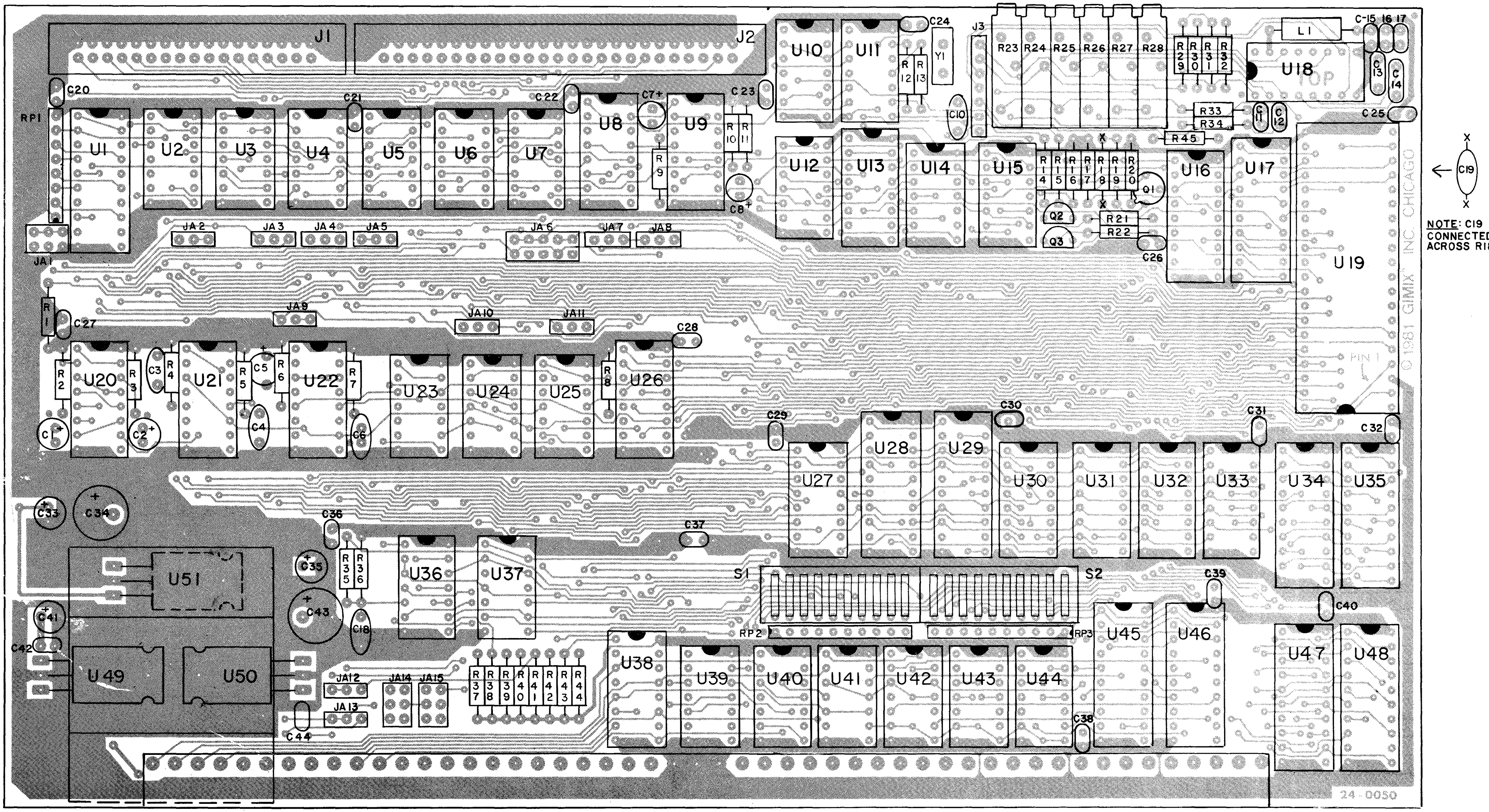
3-15-81

DMA DISK CONTROLLER DOUBLE DENSITY 5/8

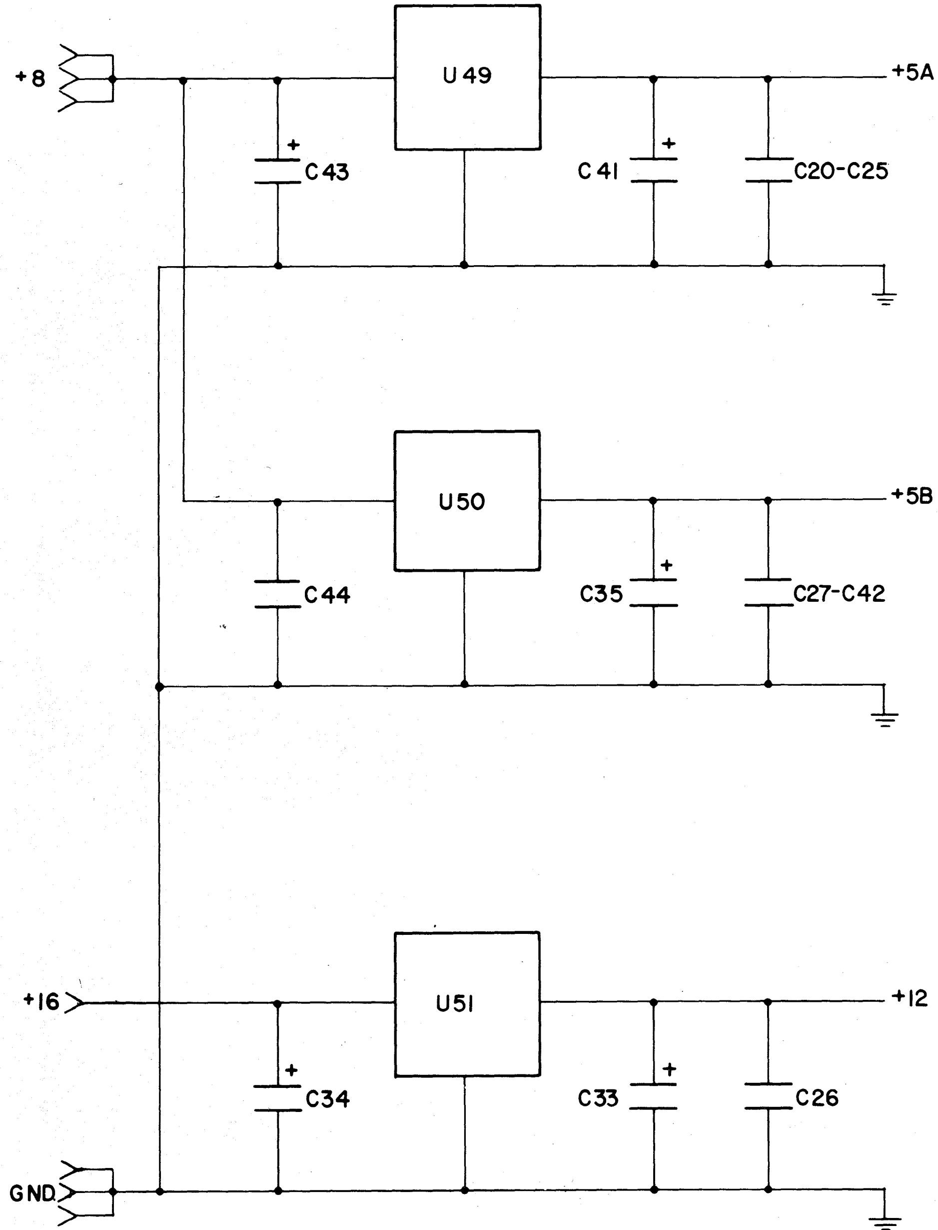
JUMPER OPTIONS SHEET 2 | C24-0050-2



COMPONENT LAYOUT

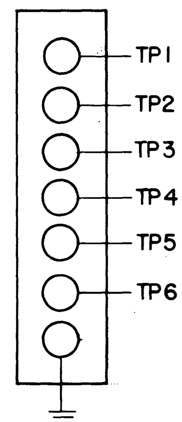
40473H-2

POWER & GROUND PINOUTS



NOTE: U19 PIN 1 CONNECTED TO +12

TEST JACK
J3



IC. NO.	+5 A	+5 B	GND.
U1	20		10
U2	14		7
U3	14		7
U4	14		7
U5	14		7
U6	14		7
U7	14		7
U8	16		8
U9	16		8
U10	14		7
U11	14		7
U12	14		7
U13	16		8
U14	14		7
U15	14		7
U16	18		9
U17	20		10
U18	15 & 16		8 & 9
U19	21		20
U20		16	8
U21		16	8
U22		16	8
U23		14	7
U24		14	7
U25		14	7
U26		16	8
U27		16	8
U28		20	10
U29		20	10
U30		16	8
U31		16	8
U32		16	8
U33		16	8
U34		20	10
U35		20	10
U36		14	7
U37		14	7
U38		16	8
U39		14	7
U40		14	7
U41		14	7
U42		14	7
U43		14	7
U44		14	7
U45		20	10
U46		20	10
U47		20	10
U48		20	10

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3-17-81

DMA DISK CONTROLLER

LOGIC SUPPLY

L24-0050-1

40473H-1

```
                  ******************************************
                  *                                        *
                  *    GIMIX 6809 RELOCATABLE DISK BOOT    *
                  *   ----------------------------------   *
                  *      FOR GIMIX DMA DISK CONTROLLER     *
                  *   ----------------------------------   *
                  *              VERSION 3.2               *
                  *                                        *
                  *           Michael H. Katz              *
                  *                                        *
                  *        Copyright (C) 1980 by           *
                  *          GIMIX, Inc.                   *
                  *          1337 West 37th Place          *
                  *          Chicago, Illinois  60626      *
                  *          (312) 927-5510                *
                  *                                        *
                  *        All rights reserved             *
                  *                                        *
                  ******************************************
                  *
                  *  EQUATES FOR DISK BOARD
                  *
             E3B0 PORT    EQU   $E3B0    BASE ADDRESS OF CONTROLLER
             E3B0 DRVREG  EQU   PORT     CONTROLLER DRIVE SELECT REGISTER
             E3B1 DMAREG  EQU   PORT+1   DMA CONTROL REGISTER
             E3B2 ADDREG  EQU   PORT+2   DMA ADDRESS REGISTER
             E3B4 COMREG  EQU   PORT+4   1797 COMMAND/STATUS REGISTER
             E3B6 SECREG  EQU   PORT+6   1797 SECTOR REGISTER
             E3B7 DATREG  EQU   PORT+7   1797 DATA REGISTER
                  *
                  *  GMXBUG-09 ENTRY POINTS
                  *
             F806 INCHE   EQU   $F806    INPUT W/ECHO
             F810 PSTRNG  EQU   $F810    PRINT STRING
             F812 LRA     EQU   $F812    LOAD REAL ADDRESS
                  *
F000                      ORG   $F000
                  *
                  *  START OF DISK BOOT
                  *
F000 10CE DFFF    BOOT    LDS   #$DFFF   MOVE STACK
                  *
                  *  DELAY TILL MOTORS UP TO SPEED.
                  *  DELAYS UNTIL THE MOTOR DELAY BIT
                  *  GOES LOW OR WHEN DRIVE BECOMES READY.
                  *
F004 34   08              PSHS  DP       PRESERVE DP REGISTER
F006 86   E3              LDA   #$E3     BASE PAGE OF CONTROLLER
F008 1F   8B              TFR   A,DP     SET DP-REG.
F00A 86   D0              LDA   #$D0     CODE FOR CLEAR INTERRUPT
F00C 97   B4              STA   <COMREG  GIVE IT TO FDC
F00E 86   01              LDA   #1       SELECT DRIVE ONE
F010 97   B6              STA   <SECREG  SET FOR SECTOR ONE
```

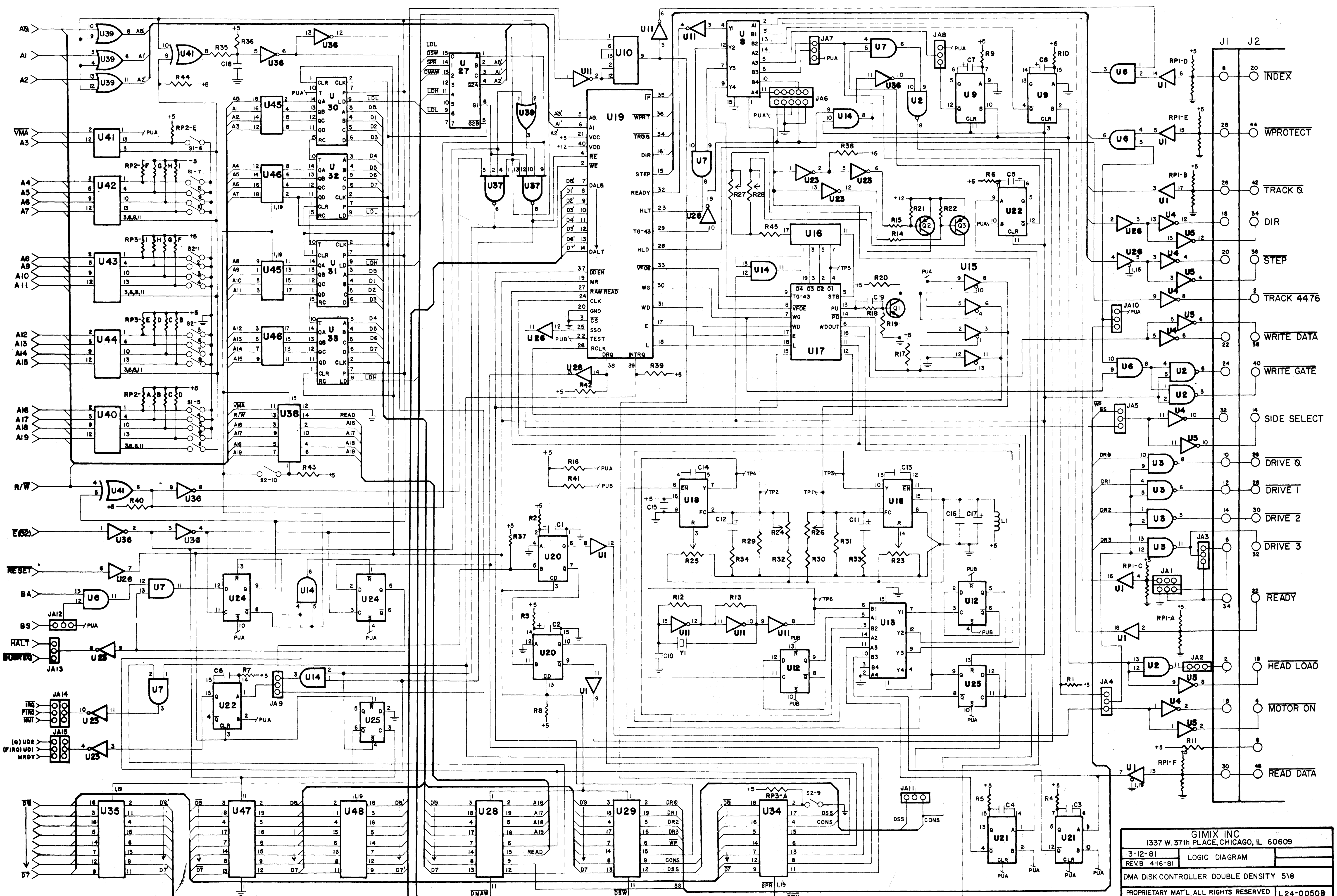
```
F012 97   B0                STA    <DRVREG   GIVE TO CONTROLLER
F014 D6   B4       BOOT1    LDB    <COMREG   GET STATUS FROM 1797
F016 2A   06                BPL    BOOT2     LOOP IF NOT READY
F018 D6   B0                LDB    <DRVREG   GET STATUS
F01A C5   20                BITB   #$20      MOTOR STARTING UP?
F01C 26   F6                BNE    BOOT1     YES:  WAIT FOR BIT TO GO AWAY
F01E 86   21       BOOT2    LDA    #$21      SETUP BITS FOR DRIVE SELECT REGISTER
F020 D6   B0                LDB    <DRVREG   GET DMA STATUS
F022 54                     LSRB             EIGHT INCH DRIVE?
F023 24   02                BCC    DRVOUT    NO:  CONTINUE
F025 8A   C0       EIGHT    ORA    #$C0      SELECT 8", SINGLE DENS & DRIVE 0
F027 97   B0       DRVOUT   STA    <DRVREG   SELECT DRIVE
F029 86   03                LDA    #3        NUMBER OF TRACKS TO STEP IN
F02B 0F   B1                CLR    <DMAREG   DISABLE DMA
F02D C6   5B       LOOP     LDB    #$5B      STEP IN WITH UPDATE
F02F 8D   4D                BSR    CHKRDA    WAIT FOR READY
F031 4A                     DECA             DECREMENT COUNTER
F032 26   F9                BNE    LOOP      LOOP TILL DONE
F034 C6   0B                LDB    #$0B      HOME AT 40ms PER STEPPING PULSE,
                   *                         LOAD HEAD AND VERIFY POSITION
F036 4F                     CLRA             DISABLE DMA
F037 8D   43                BSR    CHKRDY    GIVE COMMAND & WAIT FOR READY
F039 C5   04                BITB   #04       CHECK FOR TRACK ZERO
F03B 27   18                BEQ    ERROR     IF NOT THEN ERROR
F03D 8E   C000              LDX    #$C000    ADDRESS TO LOAD FROM DISK
F040 AD   9F F812           JSR    [LRA]     GET REAL ADDRESS
F044 9F   B2                STX    <ADDREG   GIVE ADDRESS TO CONTROLLER
F046 8A   10                ORA    #$10      SET DMA ENABLE
F048 C6   8C                LDB    #$8C      READ SINGLE RECORD, IBM FORMAT,
                   *                         HLD, HLT AND 10 ms DELAY
F04A 8D   30                BSR    CHKRDY    EXECUTE AND WAIT TILL DONE
F04C C5   9C                BITB   #$9C      ANY ERRORS?
F04E 26   05                BNE    ERROR     YES:  PRINT ERROR MESSAGE
F050 35   08                PULS   DP        RESTORE DP REGISTER
F052 7E   C000              JMP    $C000     NO:  FINISHED, JUMP TO NEXT BOOT
                   *
                   *  ERROR ROUTINE
                   *  CHECKS FOR DRIVES NOT READY
                   *  AND TELLS THE USER IF THAT IS
                   *  THE CASE.
                   *
F055 58            ERROR    ASLB             NOT READY?
F056 24   08                BCC    ERROR1    NO:  PRINT NORMAL MESSAGE
F058 30   8D 0044           LEAX   NRDYMS,PCR POINT TO MESSAGE
F05C AD   9F F810           JSR    [PSTRNG]  PRINT IT
F060 30   8D 0024  ERROR1   LEAX   ERRMSG,PCR POINT TO ERROR MESSAGE
F064 AD   9F F810           JSR    [PSTRNG]  PRINT IT
F068 AD   9F F806           JSR    [INCHE]   WAIT FOR CHARACTER
F06C 84   5F                ANDA   #$5F      MAKE UPPER CASE
F06E 81   59                CMPA   #'Y       IS IT A 'Y'?
F070 27   8E                BEQ    BOOT      YES:  TRY AGAIN
F072 81   4E                CMPA   #'N       IS IT AN 'N'?
F074 26   EA                BNE    ERROR1    RE-PROMPT IF NOT 'Y' OR 'N'
F076 6E   9F FFFE           JMP    [$FFFE]   YES:  GO BACK TO MONITOR THROUGH
```

```
                     *                           HARDWARE RESET VECTOR
 F07A 20   E4                BRA    ERROR1       PRINT ERROR MESSAGE AND GOTO RE-TRY
                     *
                     *  THIS ROUTINE WAITS FOR THE
                     *  FDC TO FINISH EXECUTING
                     *  THE CURRENT COMMAND.
                     *
 F07C 97   B1        CHKRDY  STA    <DMAREG      GIVE TO CONTROLLER
 F07E D7   B4        CHKRDA  STB    <COMREG      GIVE TO 1797
 F080 D6   B0        CHKRD1  LDB    <DRVREG      GET STATUS FROM 1797
 F082 58                     ASLB                DONE?
 F083 2A   FB                BPL    CHKRD1       NO:  WAIT TILL DONE
 F085 D6   B4                LDB    <COMREG      RETURN STATUS IN B
 F087 39                     RTS
                     *
                     *  ERROR MESSAGES
                     *
 F088 45 52 52 4F    ERRMSG  FCC    /ERROR IN BOOT, RE-TRY? /
 F09F 04                     FCB    $04
 F0A0 4E 4F 54 20    NRDYMS  FCC    /NOT READY/
 F0A9 04                     FCB    $04
                             END    BOOT

0 ERROR(S) DETECTED
```


SYMBOL TABLE:

```
ADDREG E3B2   BOOT   F000   BOOT1  F014   BOOT2  F01E   CHKRD1 F080
CHKRDA F07E   CHKRDY F07C   COMREG E3B4   DATREG E3B7   DMAREG E3B1
DRVOUT F027   DRVREG E3B0   EIGHT  F025   ERRMSG F088   ERROR  F055
ERROR1 F060   INCHE  F806   LOOP   F02D   LRA    F812   NRDYMS F0A0
PORT   E3B0   PSTRNG F810   SECREG E3B6
```



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3-12-81
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LOGIC DIAGRAM

DMA DISK CONTROLLER DOUBLE DENSITY 5\8

L24-0050B

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