Evolution of the Harris H-series Computers and Speculations on Their Future

Chuck Crawford
Computer Science
Fort Valley State College (RRC)
Fort Valley GA 31088
912/922-2861

Harris Computer Systems a division of Harris Corporation was acquired via acquisition of Datacraft Corporation in 1979.

Harris Computer Systems currently has several families of computers but this paper will only track the developments of the H-series machines which began with the Slash 4 and Slash 7.

By understanding the early Harris H-series machines and tracing the on-going development of the H-series family it is possible to speculate on the future of the H-series machine architecture. We will examine five stages in the development of the H-series:

1. The Slash 1 - May 1969
2. The Slash 7 - July 1976
3. The H-100 - March 1978
4. The H-800 - August 1979
5. The H-1200 - November 1985

Harris Computer Systems, a division of Harris Corporation, arose from acquisition of Datacraft Corporation in 1974. Datacraft's first computer, the DC-6024 or Slash 1, first shipped in May 1969, was designed to compete with the then rival S.E.L. (Gould Inc.) machine. Its 24-bits were an exceptional fit for floating point instructions and matched that days IC's, which came in 4-bit and 8-bit chip packages. To keep costs as low as possible, only five registers were used. The floating point formats were based on the use of two registers put together (the accumulator and extension registers) and were divided into an 8-bit exponent with sign and 39-bit mantissa with sign. The machine's main markets were scientific and engineering applications. A single CPU cycle for the Slash 1 was just 750 nanoseconds and the machine quickly became popular.

The first computer to bear the Harris label was the Slash 4, released in 1975. Shortly after, in 1976 the Slash 7 was released. Both machines ran Harris Virtual Memory Operating System (VULCAN) and were multi-user, multi-task, and multi-lingual. Both machines had hardware VM and could be configured with shared memory. The company's plan seemed to be a basically simple CPU with very strong software OS and very good memory management. Perhaps strong OS should be clarified. The Vulcan OS was among the first to use the open ended file structure (files expand automatically), and indirection of all I/O through logical file assignments. These were novel ideas in the mid 1970's !

The H-series currently has 3 modes of operation, each more powerful than the previous. The modes are "C-mode", "X-mode", and "F-mode", the letters standing respectively for "Compatibility", "address eXtension", and "Full address". These modes of operation are termed "addressing modes".

As the machines were developed over the years each successive version of the architecture superseded the previous yet maintained compatibility with previous versions. Programs written on older machines could always be moved to the next level or several levels up. All modes of operation follow a rational of a one-accumulator-based architecture. Compatibility mode (C-mode) was based on 8-bit, 24-bit, 48-bit integers using 24-bit instructions and a 16-bit program counter. Address extension mode (X-mode) machines could not only address one-megaword (24-bit words) of memory directly but also had an expanded instruction set, built-in Scientific Arithmetic Unit (SAU), and cache memory. Full address mode (F-mode) machines are completely ECL with 48-bit data paths, a pipelining and prefetching CPU, and hardware transendentals in the instruction set. Each successive mode increased the size of the program counter.

Other features of the H-series further illustrate the standard philosophy of Harris minicomputer manufacture. H-series machines are fast context-switching machines. This is accomplished by using executive trap (non-maskable) interrupts in conjunction with hardware virtual memory (VM). In the CPU all addresses are physical. The VM hardware and OS are totally responsible for all address translation. The CPU is also asynchronous to memory, or in common terminology, cycle steals memory operations with other things on the bus.

In the following sections, each new innovation of H-series architecture is discussed. The discussion is meant to be representative of the architectural developments and will serve as a review of the H-series. For more detailed information, refer to the referenced manuals.

The Harris Virtual Memory Machines

All H-series machines have been virtual memory machines running either Vulcan or VOS virtual memory operating systems.

In a VM system, memory is divided into 1K word "pages". A translation scheme is applied to the most-significant bits of all memory references. This scheme consists of adding a base address to the 10 most significant bits of the effective memory address to select a page of memory. The remaining bits of the original memory reference are used to select a specific word within the selected page. Figure 1 on the next page illustrates the address translation scheme of the VM logic for a Slash 7.

In practice, the user program is assigned (by the software OS) a group of sequential Virtual Address Registers (VARs). The lower limit of the user program area, and the base for computing

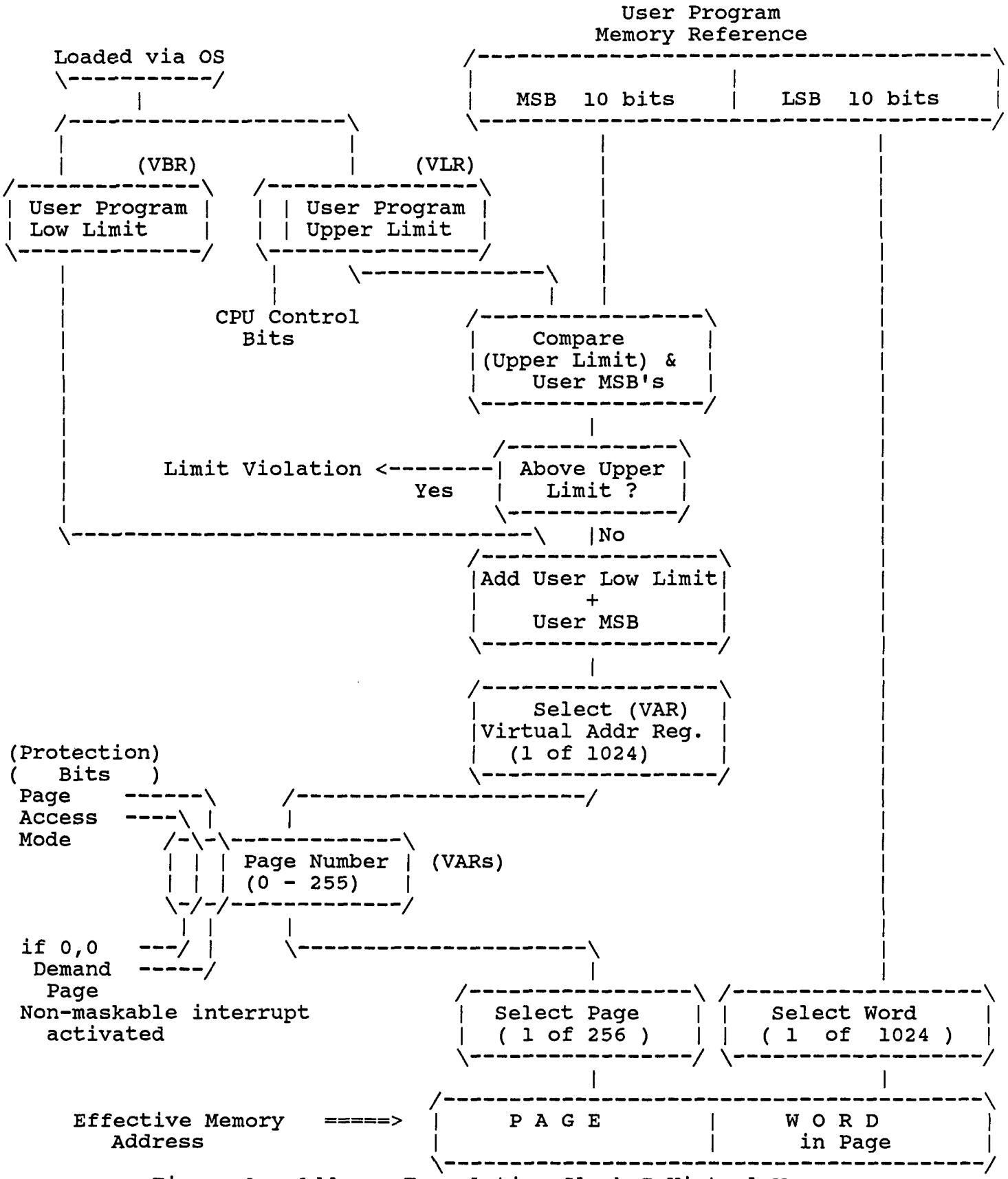


Figure 1 - Address Translation Slash 7 Virtual Memory

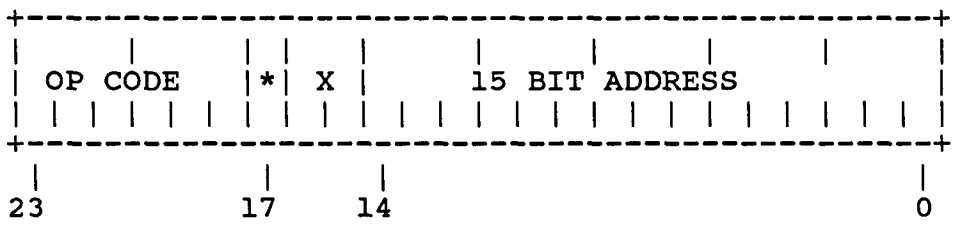
VAR addresses, is established by loading the user lower limit register (VBR) with the first VAR address in the group. The user program upper limit is established by the Virtual Limit Register (VLR) contents corresponding to the number(quantity) of assigned VARs.

THE SLASH 7

The Slash 7 had a variety of powerful features including interleaved memory which always did a double fetch from memory, asynchronous CPU which allowed for shared memory bus, external interrupts for outside world intervention, intelligent I/O (DMA and block command chaining), Scientific Arithmetic Unit (SAU) option supported with special instructions, and virtual memory. The Slash 7 was designed using standard TTL IC's (mostly TI) and used no micro-coding.

The Slash 7's basic instruction format used an unusual 24 bits as shown below: (Power of 2's being usual - 8,16,32, etc.)

Figure 2

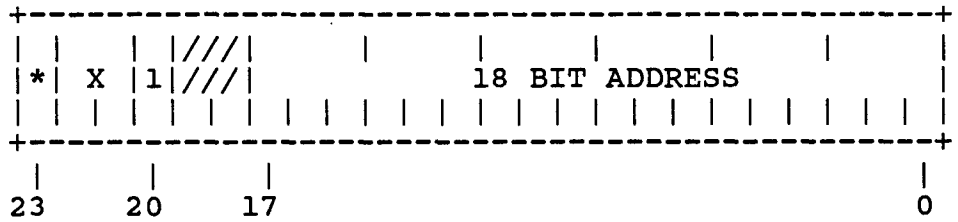


where * = indirect
X = index register selection, 00 = none

This format gave a physical address range of 32K but P15 of the program counter was used as a bias bit thus allowing up to 64K words of executable code.

There was also an indirect format which allowed addressing of up to 256K words of data (Figure 3).

Figure 3



where * = further indirection
X = index register selection, 00 = none
/// = unused bits
1 = bit 20 must be one

The Slash 7's features proved so timely, popular, and cost effective that many manufactures began incorporating these ideas into their machines. The biggest drawback was reliability; the machine's cooling was a problem and overheated connections between boards caused frequent intermittent faults.

THE H-100 SERIES

The H-100 series had all the features of the Slash 7 but with a completely different architecture. Reliability was the main concern in the redesign. The CPU was shrunk down in size to a approximately a 15-inch by 17-inch single board. Semiconductor memory replaced older Core memories. Interleaving was made optional. All major boards were redesigned for the new 15' X 17' inch size and the chassis was redesigned to accommodate these new boards.

The shrink down was made possible by using 6- and 4-bit slice Motorola 2901 chips and micro-code. Although all features were retained and reliability was excellent, execution speed was reduced.

The H-100 led to several other machines based on the Motorola IC's. These machines grew to have 48-bit ALUs and 48-bit data paths, as well as cache memory. The machine's strong points at that time were virtual memory, reliability, and a proven virtual memory operating system - "Vulcan". The machine was still fast though comparable to those of other manufactures.

THE H-800 SERIES

The H-800 was another major design change for Harris. This machine increased performance by increasing the width of the data paths and incorporating a pipelining technique. The H-800s primary differences from previous members of the line were in memory capacity, computational speed, and number of instructions. The CPU became three separate processors:

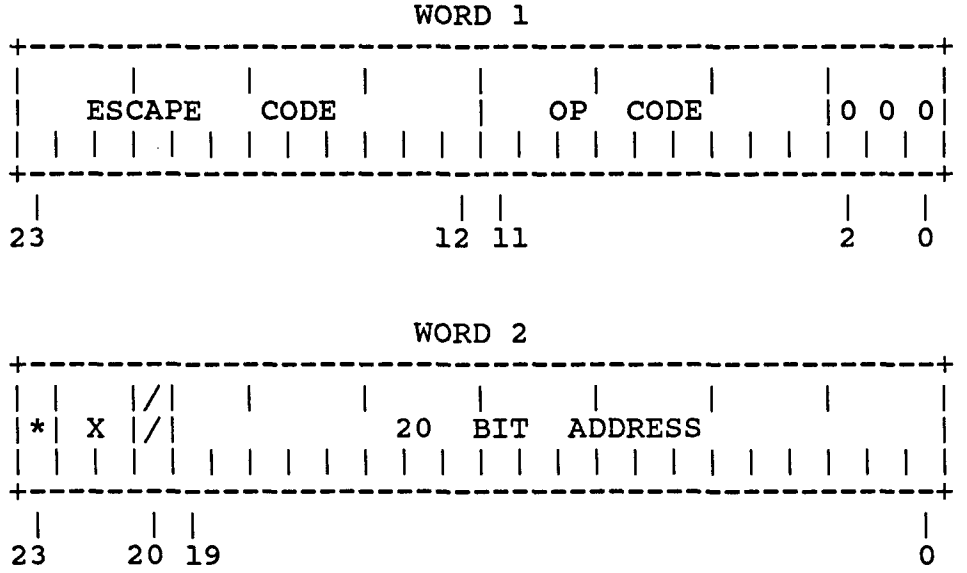
- Instruction Processor
- Execution Processor
- Maintenance Processor

Harris was still placing a major stress on reliability and maintenance, so the maintenance processor was added to the basic machine for service monitoring of machine functions.

The machine now had two defined modes of operation: Compatibility mode "C-mode" and address eXtension mode "X-mode". Two bits of a VM register (a user programmable upper limit register) were used to define the modes. In "X-mode" the user could directly address to one mega-word of memory. The program counter was increased from 16 bits to 20 bits with bits 19-16 being turned off when in "C-mode". The VM hardware was increased in size to allow a maximum logical memory size of 16 megawords or 48 megabytes.

In "X-mode" a new double word instruction format was created to allow for the extended addressing. (Figure 4)

Figure 4



where * = indirection
X = index register selection, 00 = none
/ = unused bit

Decimal arithmetic instructions were added as well as special maintenance processor interaction commands. Once again, Harris had a very fast machine, 180 nanosecond CPU and a 75 nanosecond cache.

THE H-1200 SERIES

By 1985, chip technology had improved unbelievably. ECL ICs were in ready supply and Harris put them to good use. The H-1200 machine used the same principles as the H-800 machine but the H-1200 was completely ECL. Now the execution processor and instruction processor cycle times were only 75 nanoseconds which matched the cache memory's hit cycle time. The direct addressing range was increased (again) to four megawords or 12 megabytes. The VM address range was also increased to 64 megawords or 192 megabytes. Transcendental functions were added to the built-in SAU and the SAU could now perform functions on 96-bit operands.

The H-1200 was an expanded H-800 completely redesigned using ECL chip technology. The simple five-register computer had come a long way.....

SUMMARY

The basic concept and block diagram layout of the H-series has remained alive and thriving for over fifteen years. As

improvements in chip technology came along Harris quickly incorporated these changes into ever improving machines while always maintaining compatibility with previous machines.

Can you imagine taking code you'd compiled on some other computer, say a program you wrote and compiled 12 or 15 years ago, and walking up to a new model in the line and loading and executing that code! Amazing! I can't even remember what I wrote 12 years ago, much less expect it to run on the current machine of any other make.

The H-series has seen many improvements over the years, but the main idea of a fast context switching, virtual-memory machine is, to this day, a powerful and cost effective design.

Each new H-series machine brought fresh ideas to a simple yet elegant machine. The simple 5-register CPU with VM has lived for over 15 years, although the design has been modified for the ever changing technology.

Will the next H-series have a RISC instruction set with micro-code to make the old instructions still compatible or perhaps the next generation of H-series will have 4 modes and 72 bit instruction formats? For greater throughput closely-coupled multiprocessors could be in the H-series future. Yet another possibility would be to shrink the H-series to desktop size and increase the clock speed.

More than likely Harris will follow its long tradition and use the latest in chip technology to again improve the long lasting H-series. Is there a gallium arsenide (GaAs) chip technology machine in the H-series future ?

REFERENCES

REFERENCE MANUAL, SLASH 7, DIGITAL COMPUTER: Harris Corporation, Fort Lauderdale, Florida: July 1976: Manual #0830000-001

REFERENCE MANUAL SERIES 100 COMPUTER SYSTEMS: Harris Corporation, Fort Lauderdale, Florida: March 1978: Manual #0830005-000

REFERENCE MANUAL HARRIS 800 GENERAL PURPOSE DIGITAL COMPUTER:Harris Corporation, Fort Lauderdale, Florida: August 1979: Manual #0830007-000

REFERENCE MANUAL HARRIS 1200 COMPUTER SYSTEM: Harris Corporation, Fort Lauderdale, Florida: November 1985: Manual #0830025-000

ACKNOWLEDGEMENT

I appreciate the efforts of Phillip I. Good, Callaway Professor at Fort Valley State College who suggested the topic and helped in reading and revising this manuscript.