Honeywell

FREESTANDING DPS 8

WCPU68LA/WIOU66LA/WMMU66LA

SYSTEM MANUAL

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DPS 8 FREESTANDING MULTICS

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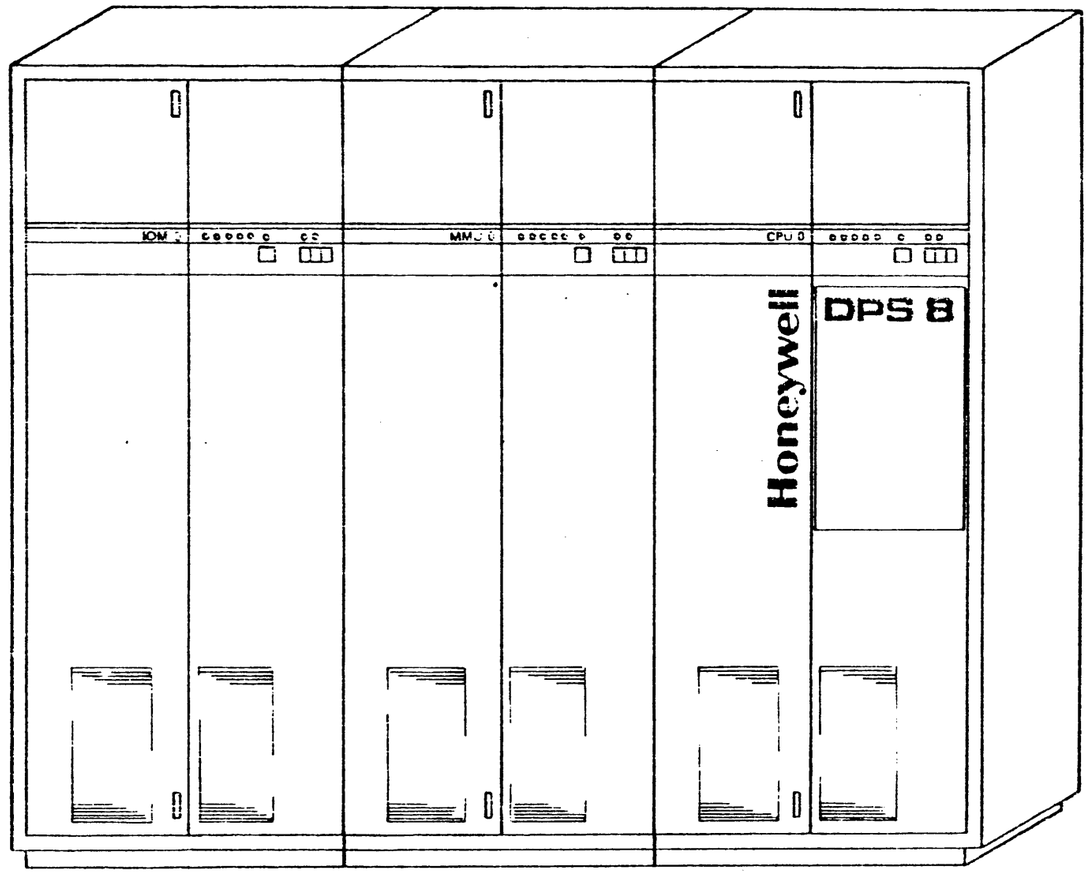

FREESTANDING MULTICS DPS-8 SINGLE SYSTEM MODULE

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1.1 INTRODUCTION

1.1.1 Purpose

This manual is intended as a general system review and maintenance aid for TAC personnel in analyzing and diagnosing system problems beyond Level 1 procedure. This manual may also be used by FED system level students as a reference text.

1.1.2 Scope

This manual presents a general outline of the overall system, a general description and function of each major unit, and interfaces and theory of operation of each unit.

1.1.3 Objective

The intent of this manual is to integrate the system's independent major units and illustrate their interface functions (i.e., interface protocol instructions, data exchange and status signals) under GCOS program management control. Also included are the maintenance aids available to support maintenance and troubleshooting.

1.1.4 Documentation

The documentation of this manual is divided into two parts (A) Support Documentation, (B) Reference Documentation.

A. Support Documentation consists of those documents supplied with the system. Basically, these documents fall into two major categories: 1) Site Preparation and Installation/Deinstallation Manuals, and 2) Maintenance and Specialist Level System/Unit Manuals. Refer to Figure 1-1.

1. The Site Preparation and Installation/Deinstallation Manuals provide the information required to prepare the customers site for the systems installation and the deinstallation instructions.

2. The Freestanding Multics DPS 8 Maintenance and Specialist Level System/Unit Manuals are divided into six major divisions of support documents, as shown in Figure 1-1.

   1) System Manual provides a general description of the overall system.

   2) Power and Cooling Manuals provide a full description and theory of operation of the power supply, control, and distribution. In addition, the cooling system is described.

   3) Central Processor Manuals provide a full description and theory of operation of the independent CPU's. Also, included is a list of options available to improve or expand the system or individual units.

   4) Input/Output Manuals provide a full description and theory of operation of the independent I/O units and a list of options available to improve or expand the systems or its individual units.

   5) The Memory/SCU Manuals provide a full description and theory of operation of the Memory/SCU cabinet units. Also provided are the available options.

   6) Maintenance Manuals provide the operator and maintenance personnel with individual manuals for various maintenance procedures (software, hardware) necessary to test the different functions of the system.

B. Reference Documentation consists of those documents not listed in the Support Documentation Tree from which additional information was extracted in the preparation of this manual. The appropriate reference documents will be listed within each theory section.

1.1.5 Reference Support Documentation

Reference documentation used in this manual, in addition to those listed in Figure 1-1 Documentation Tree, will be listed on theory diagrams or at the end of each theory section.

1.1.6 Feedback

To provide the user with a technically correct and current system manual, it is respectfully requested the reader submit any comments or corrections of errors, omissions or the format presentation of the material in this manual.

Comments submitted will be used in update revisions of this and future system manuals.

Address all comments to:

Honeywell Large System Product Support
Mail Station P.O. Box 6000
Phoenix, AZ 85005
ATT: PMD (System Manuals)

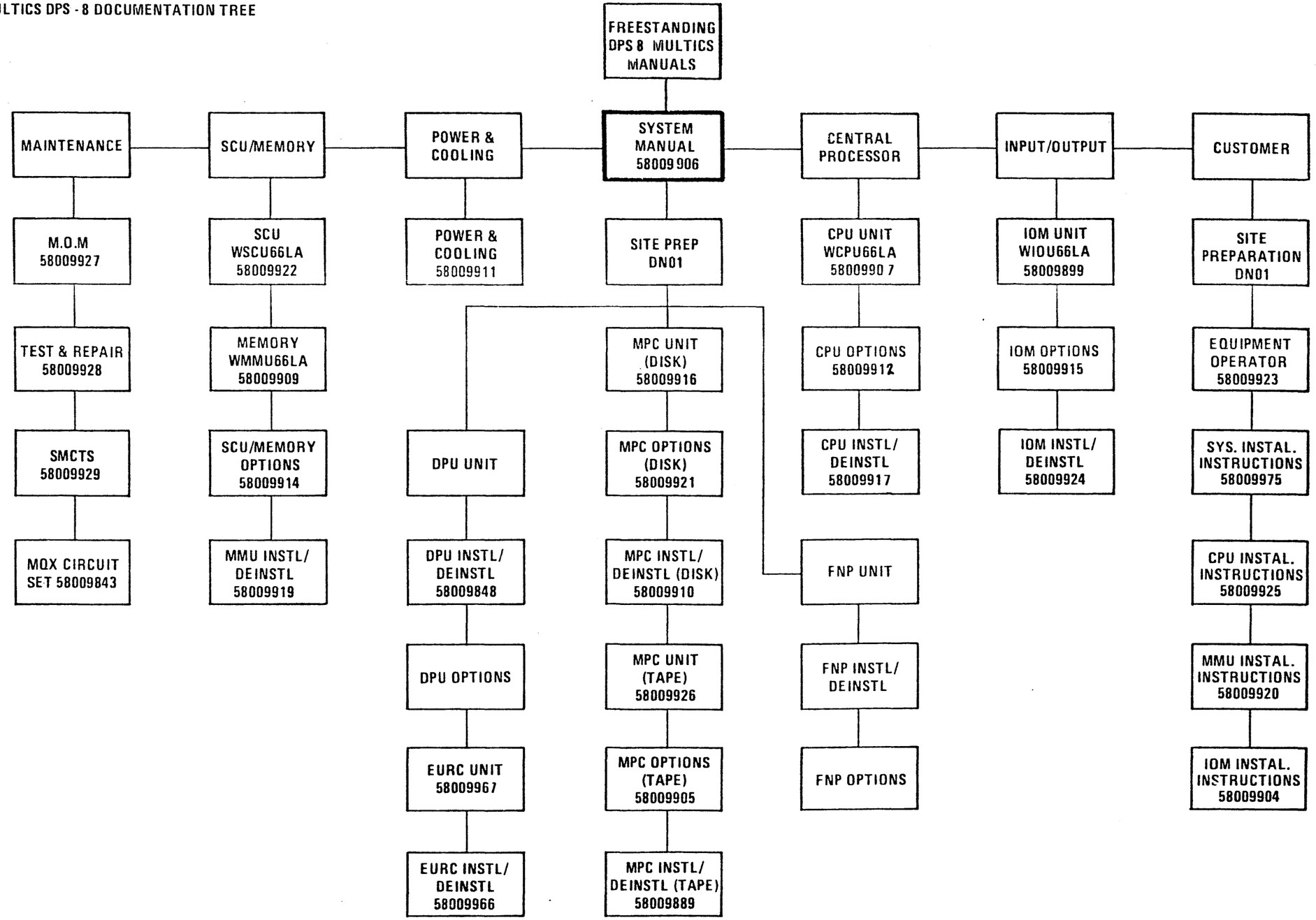


FIGURE 1-1. FREESTANDING MULTICS DPS 8 SUPPORT DOCUMENTATION TREE

1.2 SYSTEM OVERVIEW

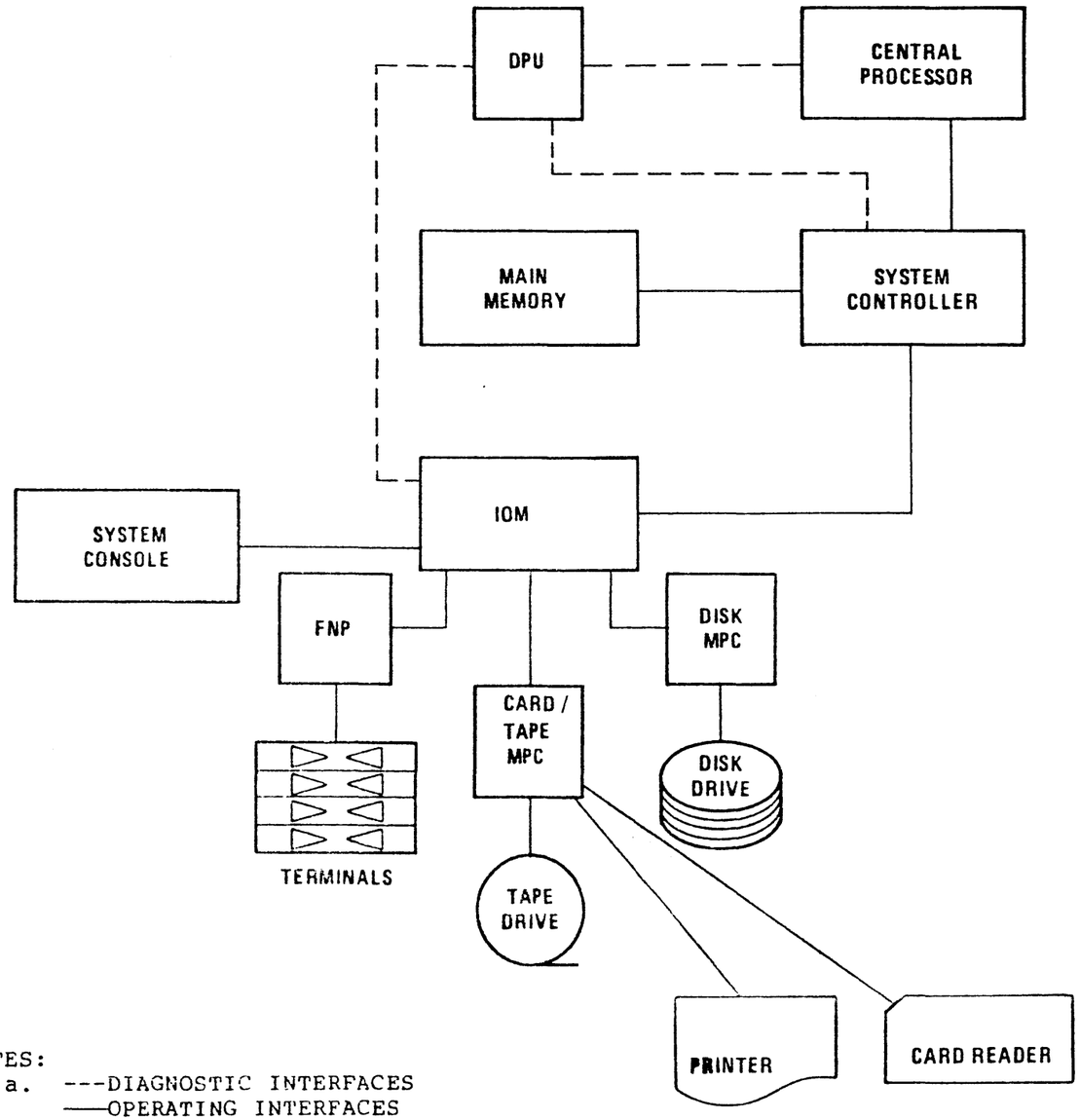
The DPS 8 Freestanding Multics System is basically the Low Profile Freestanding DPS-E with the Central Processor Unit (CPU) redesigned to accept the Multics Operating System Software. Those features that make the Multics System unique from other operating systems are discussed in detail in Paragraphs 3.1.1 and 3.4.2. For more detailed information on the Multics CPU, refer to 58009907 Multics CPU Unit Manual.

The complete system consists of three or more single bay cabinets, plus options and the necessary peripheral equipment. Figure 1-2 shows the system components in their relationship to each other.

The Main Memory Unit (MMU) cabinet contains the System Controller Unit (SCU) in the A0 card cage with the lower four card cages reserved for up to 16MW of memory for each MMU cabinet.

The Central Processor Unit (CPU) and Input/Output Multiplexer (IOM) cabinets house the logic in four card cages. In the IOM cabinet, the IOM Central is located in card cage A0.

Power control and distributing equipment for each cabinet is in locations VC1 thru VK1. Refer to Table 2-1 for locations of discrete components. The Power Entry Module is located in SO3. The circuit breaker panel is located in SO2.



NOTES:
a. ---DIAGNOSTIC INTERFACES
——OPERATING INTERFACES

b. With EURC Option, Card MPC will not be present.

FIGURE 1-2. SYSTEM COMPONENTS

Cooling in each cabinet is provided by a blower in location Z01 and a plenum located between the logic bays and the power components. Cool air intakes are located on the lower portion of the cabinet. Baffles in the plenum force the intake air out into the card cages. After circulation between the logic boards, the heated air is exhausted through louvers in the top of the cabinet.

1.3 SIGNAL FLOW

Generally, an operating signal originates as a command from an operator of either the system console or a remote terminal, via the Front-end Network Processor (FNP), (see Figure 1-2). If bulk data is required to execute the command, the peripheral device (disk drive, tape drive, etc.) containing the bulk data will input through the Microprogrammed Peripheral Controller (MPC) to the input logic of the IOM. The CPU, via the SCU, allocates a block of main memory for use in processing the bulk data to fulfill the command. The bulk data is then transmitted to the block of main memory via the write data bus through the SCU.

When data is ready to be outputted, it is transmitted from main memory on the read data bus, via the SCU, to the output logic of the IOM. From there, it is transmitted to the output device(s) (CRT, printer, etc.). Details concerning the type of command to be executed and the address in main memory to which the data is destined are carried on the Zone, Address, & Command (ZAC) bus.

When fault isolation of the system becomes necessary, the (optional) Diagnostic Processor Unit (DPU) is connected to the Dynamic Maintenance Panel (DMP) on any cabinet (CPU, IOM, MMU). The diagnostic routines and data requests follow the same paths as operating commands and data.

The following paragraphs provide an overview of the main system signals and their overall functions. Refer to Figure 1-3 for the system signal flow.

1.3.1 Read Data

The CPU or IOM obtains data from the main memory by sending a $INT to the SCU (control line), requesting to be serviced. At that time, ZAC information is placed in the port register, giving the details of the request and the address of the data. When the SCU forwards the ZAC information to memory, the data is placed on the read data bus (72 lines plus parity) and transmitted to the SCU port register for the active module.

1.3.2 Write Data

When the CPU or IOM writes data into the main memory, a $INT is sent to the SCU control line requesting service. At that time, ZAC information is placed in the port register defining the request and giving the address for the data word to be written into memory. When the SCU forwards the ZAC information to memory, the write data is placed on the write data bus and sent to the SCU memory port register.

1.3.3 Initialize (INZ)

An INZ signal from any source is routed directly to the SCU for distribution to all units in the system. This clears the system for bootloading.

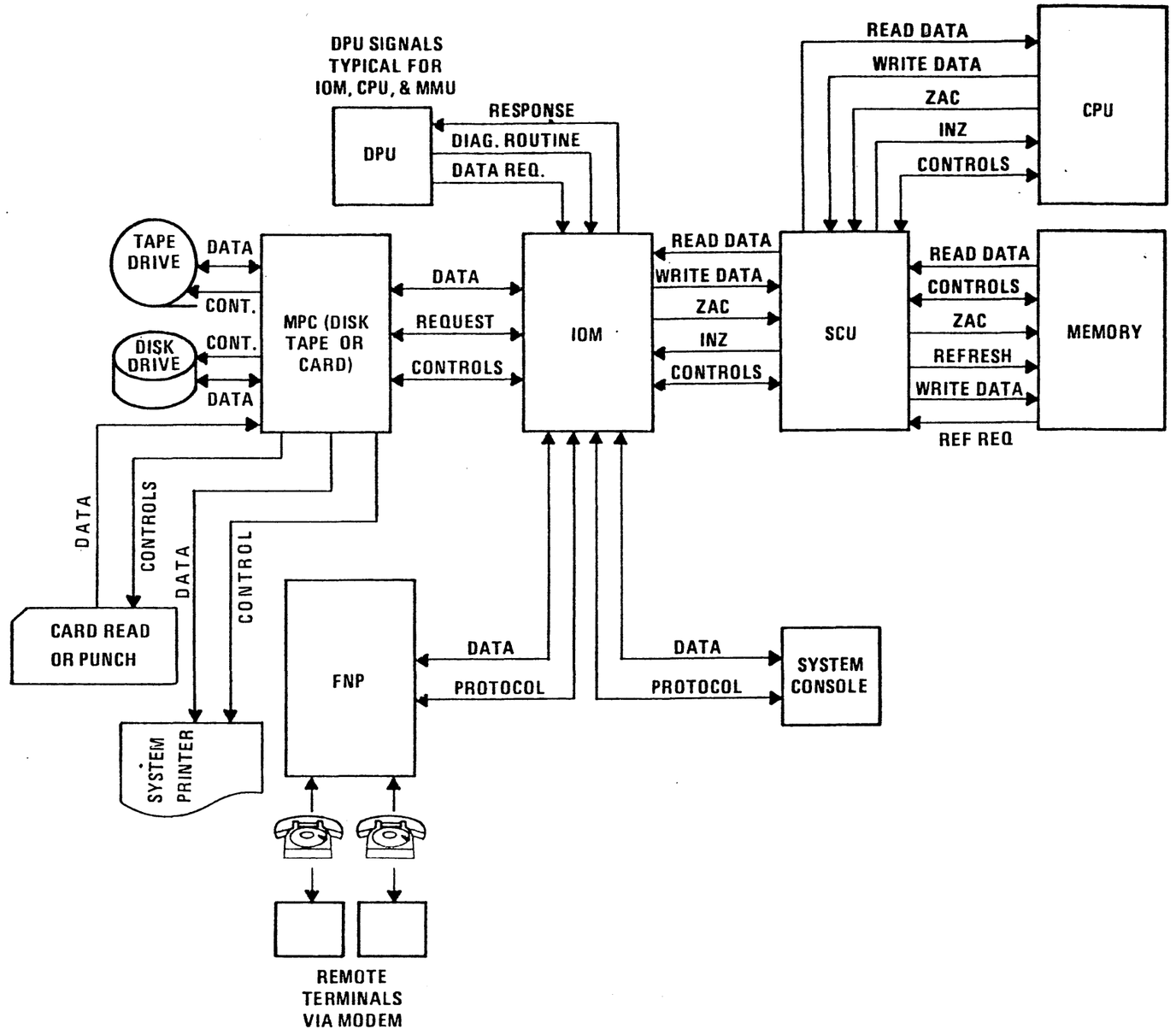


FIGURE 1-3. SIGNAL FLOW

1.3.4 Refresh

The MOS memory chips must be refreshed every two milliseconds. Thus, the memory sends a refresh request for cyclic portions of memory every 16 microseconds. The SCU fills this request by addressing the cells to be refreshed.

1.3.5 ZAC

The ZAC word defines the type of cycle requested by the $INT, whether a single or double precision operation, and the portion of memory to be addressed. Like the data words, the ZAC word also contains parity bits for error detection.

1.3.6 System Console Signals

Signals to and from the System Console consist of the necessary protocol format to access the portions of the system required by the duties of the console operator plus the information passing between operator and system.

1.3.7 FNP Signals

FNP signals consist of the same information to and from the system console except that the signals originate from remote terminals in a network system.

1.3.8 MPC Signals

Signals between the MPC and IOM consist of the bulk data stored on the accessed disk or magnetic tape, address information sufficient to specify/store the data being moved and the necessary information to control operation of the disk drive or tape drive connected to the MPC.

1.3.9 DPU Signals

Signals between the DPU and IOM consist of the diagnostic routine inputted by the Field Engineer or other Computer Engineer troubleshooting the system, the data requests, and the responses from various registers, memory, and other parts of the system units. Requests may originate at the DPU console itself or via modem to the DPU from a remote location (such as the TAC Center).

1.4 TECHNICAL INSTRUCTIONS

Each system, unit, option, and component is covered in detail by an instruction manual. For details of description, installation, deinstallation, theory of operation, maintenance, troubleshooting, site preparation, and a description of each chip used in the system, consult the appropriate instruction manual(s) listed in Figure 1-1. The manual drawing number is listed, along with the functional title, in each block.

2.0 PHYSICAL OUTLINE

2.1 GENERAL INTRODUCTION

The DPS 8 Freestanding Multics System is a composition of three cabinets; the Central Processor Unit (CPU); the Main Memory Unit (MMU); and the Input/Output Multiplexer (IOM). These three cabinets may be physically connected to form a single-system module. Any additional (optional) cabinet may be freestanding or connected to the existing module depending on the customer's requirements.

Figure 2-1 shows the Single System module configuration.

For additional information on these and other units within the system, refer to DN01 Site Preparation manual.

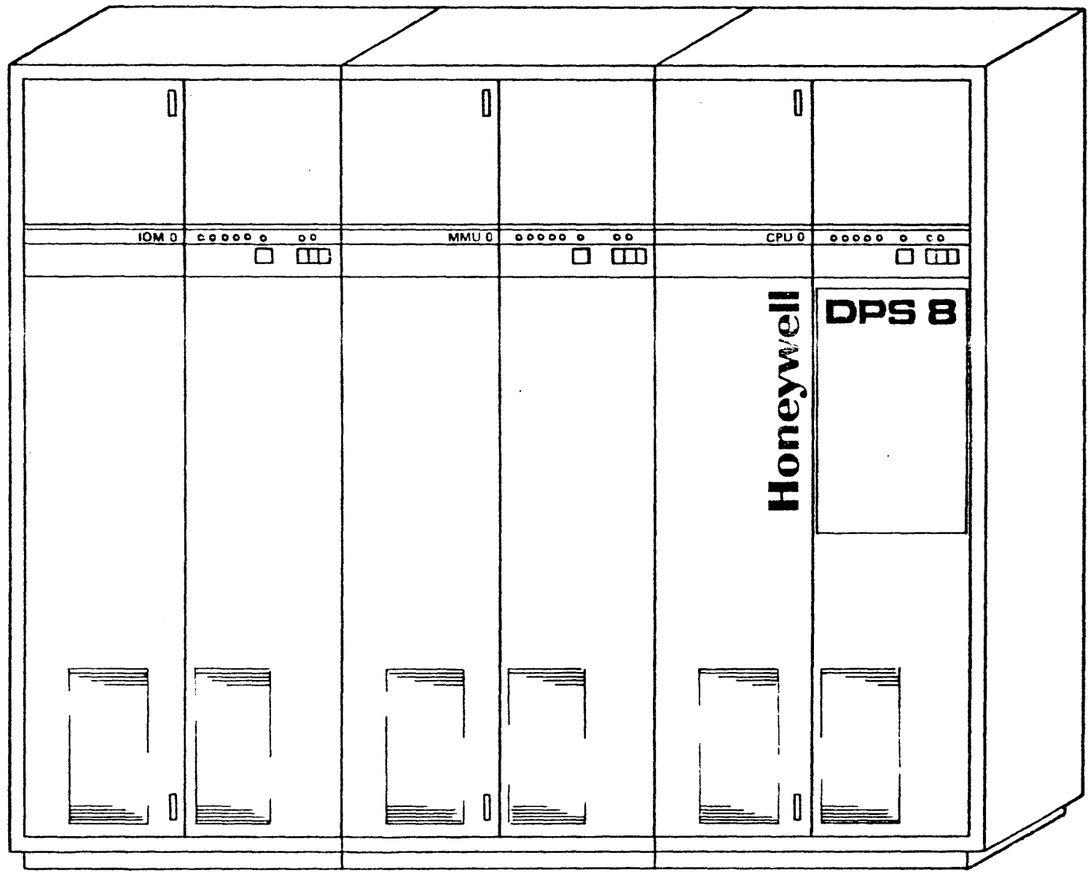


FIGURE 2-1 FREESTANDING MULTICS DPS-8 SINGLE SYSTEM

2.2 PHYSICAL CABINET CONFIGURATION

All system units are hardware constructed in a common configuration. Every physical cabinet contains a power supply and cooling on the left, the logic boards in the center, and an options area on the right. Each cabinet is divided into four vertical zones. Figure 2-2 illustrates this physical cabinet configuration.

2.2.1 Basic Cabinet Outline

Zone V houses the cabinet power supply, blower assembly with controls, and air flow sensor switch.

Zone B is the air flow plenum for air circulation over the power equipment and to the logic boards in Zone A.

Zone A contains the logic boards and back panel.

Zone W is a common option area. Its components and function depends on the cabinet and options.

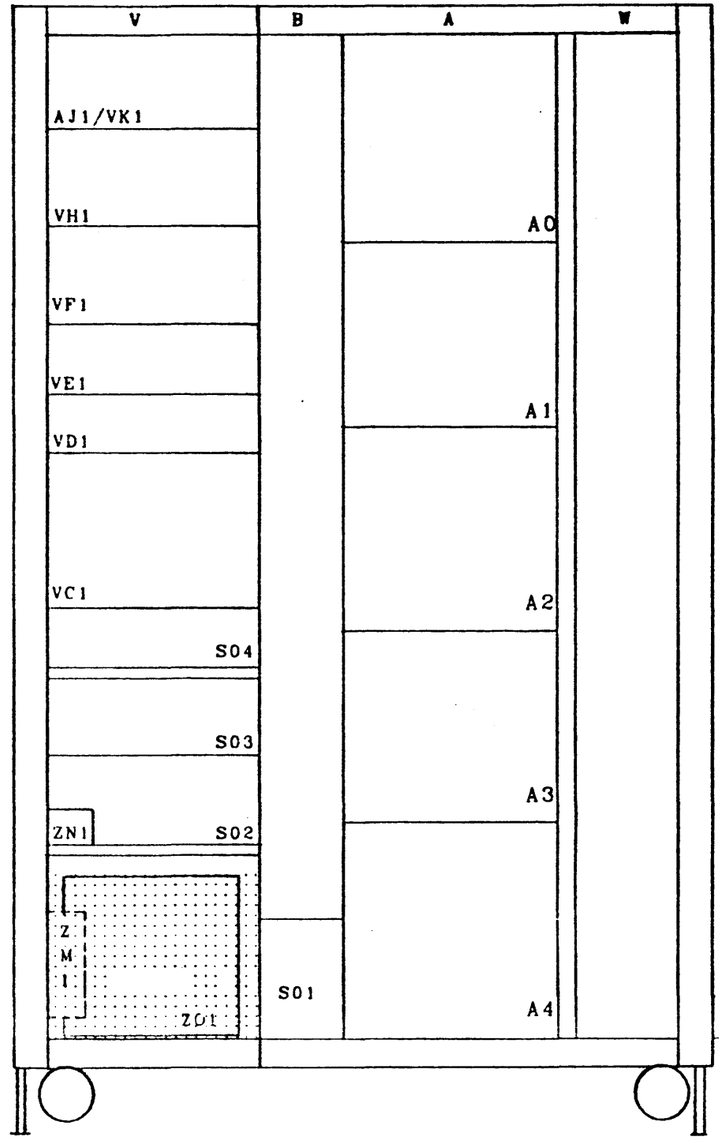


FIGURE 2-2 PHYSICAL CABINET CONFIGURATION

2.2.2 Common Cabinet Components

In addition to having common zones within each cabinet, each zone contains common components. Table 2-1 lists the common components to all cabinets.

The components unique to a specific cabinet, (i.e. CPU unit) will be listed in its respective section.

Table 2-1 COMMON COMPONENTS TO ALL CABINETS

Component Designator	Zone	Description
ZMI/Z01	Bottom portion Zone V	Blower controls assembly and blowers
ZN1	Left from lower position zone V	Airflow sensor and switch assembly
S01	Lower portion of Plenum Zone B	Site power connector terminal board (S01 TB1)
S02	V	Circuit Breaker Module, contains circuit breaker (S02 CB1) that applies power to the cabinet
S03	V	Power Entry Module with circuit breakers (S03-CB2/CB3) for FAN and REG. power on/off control
VC1	V	Power Control Module with Power Control & Configuration switches and indicators
VD1	V	100 Watt Voltage Regulator
Plenum	B	Force air column to circulate air over and around power supplies and logic boards.
Logic Buckets A0-A4	A	Logic card and back panel area.
Depends on type cabinet & options	W	Heat sensors, batteries, and special area depending on cabinet type CPU, MMU, or IOM requirements.

2.3 CPU CABINET CONFIGURATION

The CPU cabinet contains a power and cooling component in Zones V and B, a cable bulkhead area in Zone W, and CPU circuit boards in Zone A.

Figure 2-3 illustrates the major components of the CPU cabinet, their physical location, and their zone designators.

Table 2-2 lists the component designator, zone, and description for each component.

Table 2-3 lists each circuit board in the CPU by module/slot, board mnemonic, and function.

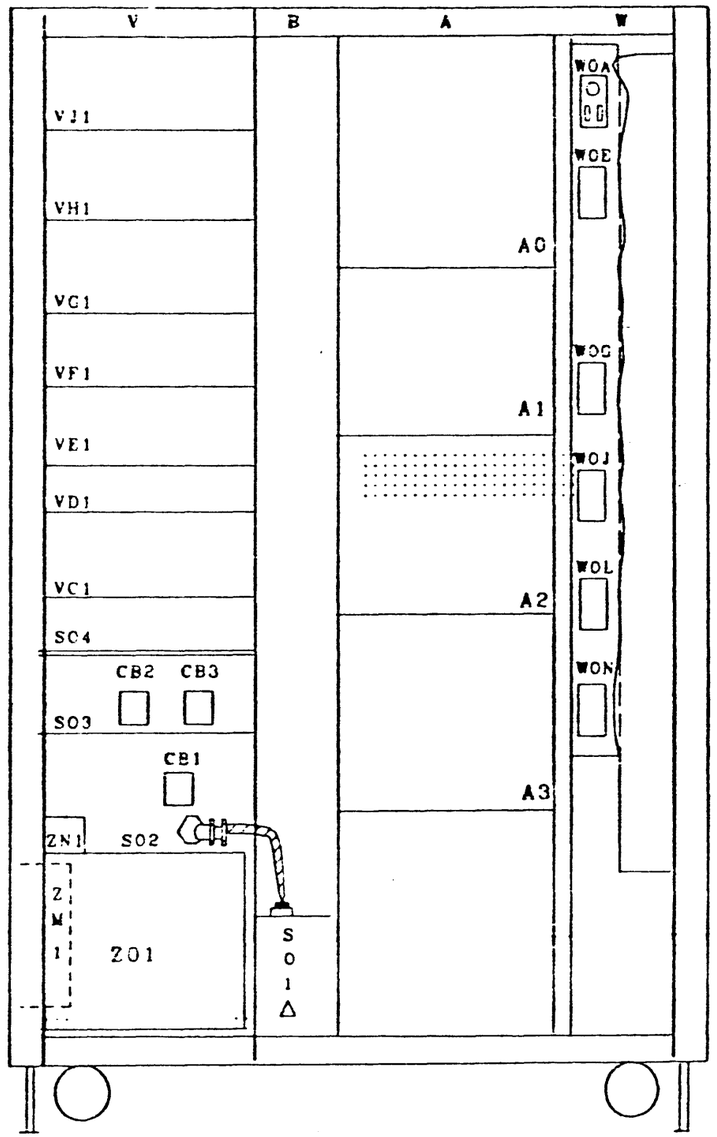


FIGURE 2-3 CPU CABINET FRONT VIEW WITH DOORS REMOVED

2.5.1 IOM Cabinet Components

Table 2-6 IOM CABINET COMPONENTS

Component Designator	Zone	Description
VJ1	V	
VH1	V	Dual +5V Power Regulator
VG1	V	
VF1	V	Dual +12V Regulator
VE1/VE2	V	-5V Power Converter Regulator
VD1	V	Dual +24 Volt Regulator 100 Watt
VC1	V	Power Control Module with Power Control & Configuration switches and indicators
S03	V	Power Entry Module with circuit breakers (S03-CB2/CB3) for FAN and REG. power on/off control
S02	V	Circuit Breaker Module, contains circuit breaker (S02 CB1) that applies power to the cabinet
S01	Lower portion of Plenum Zone B	Site power connector terminal board (S01 TB1)
ZN1	Left from lower position zone	Airflow sensor and switch assembly
Z01	V	Blowers
ZM1	Bottom portion Zone	Blower controls assembly

Table 2-2 CPU CABINET COMPONENTS (continued)

Component Designator	Zone	Description
A0-A3	A*	Card cages A0-A4. *See Table 2-3 for modules, card nomenclature, and slot.
WOA-AON	W	Seven cable connectors ports for external cables.
WOA	W	Maintenance panel connection: J1 = Maintenance panel J2 = Local J3 = Remote
ZAO	W/A1Q	Temp sensors positioned at A1Q
ZA1	W/A2P	Temp sensors positioned at A2P

2.3.2 CPU Circuit Boards By Location

Table 2.3 CPU CIRCUIT BOARDS BY LOCATION

CPU CABINET		
MODULE/SLOT	BOARD	FUNCTION
AO		
A	ETCMP	DMP interface
B		
C	EISDN	Alignment Control
D	ETCDP	Alpha-Numeric Control
E	ETCDG	Timing & Control, #2, 3, 5
F	EISDE	Exponent
G	EISDF	Exponent
H	EISDC	Timing & Control, #2, 3, 5
J	EISDQ	Timing & Control, #2, 3, 5
K	EISDR	Control, #1, 5
L	EISDB	Control, #1, 5
M	EISDM	Alignment Control
N	645DL	
P	EISDK	Character Manipulation
Q	EISDD	Timing & Control, #2, 3, 5
R	EISDA1	Adder Register
S	EISDA2	Adder Register
T	EISDA3	Adder Register
U	EISDA4	Adder Register

Table 2-3 CPU CIRCUIT BOARDS BY LOCATION (continued)

CPU CABINET		
MODULE/SLOT	BOARD	FUNCTION
A1		
A	EISDA5	Adder Register
B	EISDA6	Adder Register
C	EISDA7	Adder Register
D	EISDA8	Adder Register
E	EISDJ	Alignment
F	ETCDH	IPR Decode & Control
G	ETCAK	OU Timing & Control
H		
J	ETCAM	Exponent Control
K	ETCAD	OU Adder Control
L	ETCAJ	OU I/O Data Control
M	ETCAB	Indicators
N	ETCAE	Exp. Adder & Reg., Norm, Shift
P	ETCAF	OU I/O Data Align
Q	ETCAN	OU Adder
R	ETCAP	Reg. Store & OU Output
S	ETMBA	Address Prep
T		
U	ETCBG	Instruction Adder & Track

2.3.2 CPU Circuit Boards By Location (Continued)

Table 2.3 CPU CIRCUIT BOARDS BY LOCATION (continued)

CPU CABINET		
MODULE/SLOT	BOARD	FUNCTION
A2		
A	ETMBL	
B		
C	ETMBB	Address Registers
D		
E	ETMBH	Address Control
F		
G	ETMBD	Tag Cont & Decimal OPS Sequencing
H		
J	ETMCX	
K		
L	ETMPX	
M		
N	ETMCH	IPR Decode & Control
P		
Q	ETMCP	INZ & Fault Control
R		
S	ETMCG	Fault & Mode Registers
T		
U	ETCCU1	History Board

Table 2.3 CPU CIRCUIT BOARDS BY LOCATION (continued)

CPU CABINET		
MODULE/SLOT	BOARD	FUNCTION
A3		
A	ETCCU2	History Board
B	ETCCC	Cache Directory
C	ETMCM	Port Control
D		
E	ETMCQ	Port Sel, Addr Latch & Drive, Config. Registers
F		
G	ETCCD1	Cache Memory, Data Hub
H	ETCCD2	Cache Memory, Data Hub
J	ETCCD3	Cache Memory, Data Hub
K	ETCCD4	Cache Memory, Data Hub
L	ETCCD5	Cache Memory, Data Hub
M	ETCCD6	Cache Memory, Data Hub
N	ETCCZ	Cache Clear
P	ETCCY	Cache Duplicate Directory
Q	ETMPH	
R		
S	ETMPA	
T		
U	ETMPB	

2.3.2 CPU Circuit Boards By Location (Continued)

Table 2.3 CPU CIRCUIT BOARDS BY LOCATION (continued)

CPU CABINET		
MODULE/SLOT	BOARD	FUNCTION
A4		
A	ETMPC	
B		
C	ETMPE	
D		
E	ETMPF	
F		
G	ETMPD	
H		
J		
K		
L		
M		
N		
P		
Q		
R		
S		
T		
U		

2.4 MMU CABINET CONFIGURATION

The MMU cabinet contains a power and cooling component in Zones V and B, a cable bulkhead area in Zone W, SCU and memory circuit boards in Zone A. Zone W would also contain the battery power option if ordered.

Figure 2-4 illustrates the major components of the MMU cabinet, their physical location, and their zone designators.

Table 2-4 lists the component designator, zone, and description of each component.

Table 2-5 lists each circuit board in the MMU by module/slot, board mnemonic, and function.

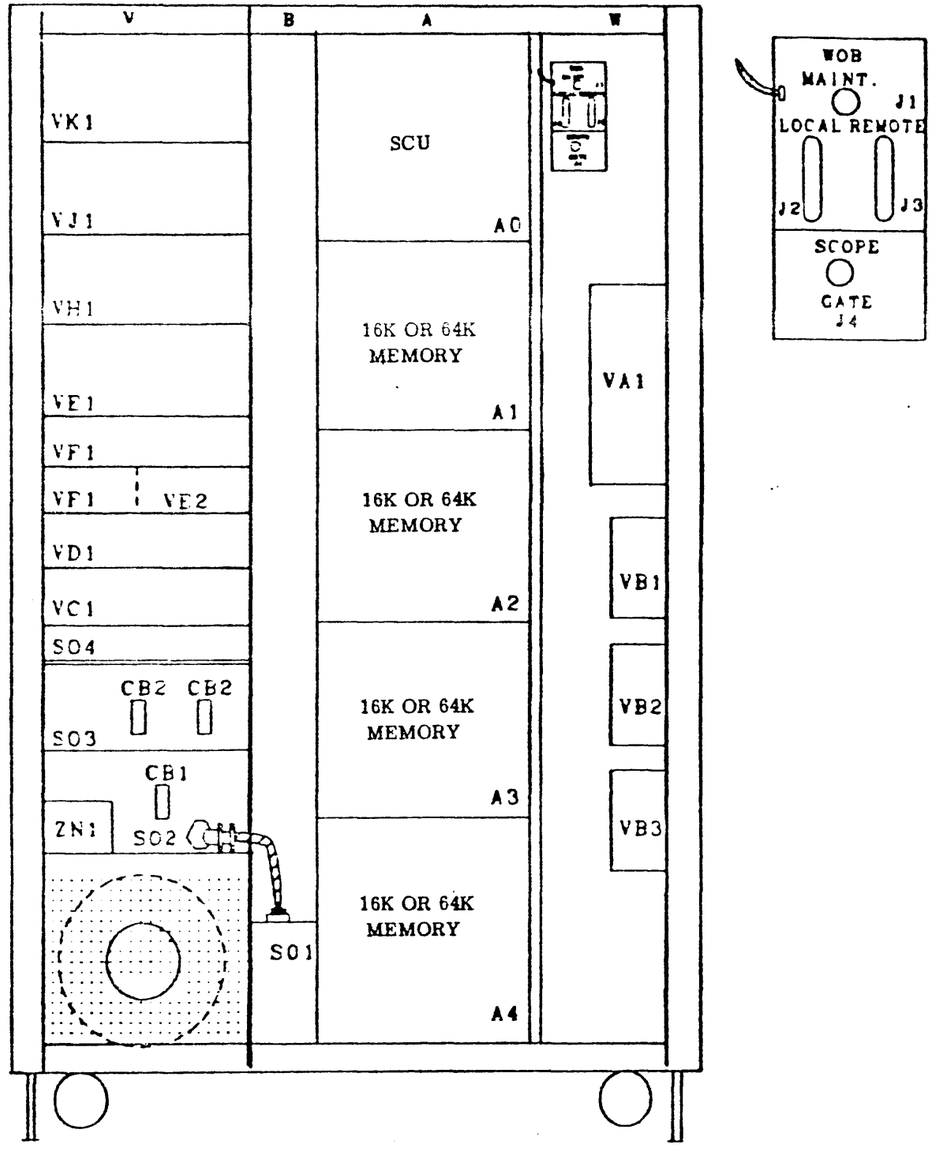


FIGURE 2-4 MMU CABINET FRONT VIEW WITH DOORS REMOVED

2.4.1 MMU Cabinet Components

Table 2-4 MMU CABINET COMPONENTS

Component Designator	Zone	Description
ZM1	Bottom portion Zone	Blower controls assembly
Z01	V	Blowers
ZN1	Left from lower position zone V	Airflow sensor and switch assembly
S01	Lower portion of Plenum Zone B	Site power connector terminal board (S01 TB1)
S02	V	Circuit Breaker Module, contains circuit breaker (S02 CB1) that applies power to the cabinet
S03	V	Power Entry Module with circuit breakers (S03-CB2/CB3) for FAN and REG. power on/off control)
VC1	V	Power Control Module with Power Control & Configuration switches and indicators
VD1	V	124 Volt Regulator 100 Watt
VE1/VE2	V	2 Dual -5V Regulator
VF1	V	Dual +12V Regulator
VG1	V	Dual +12V Regulator
VH2	V	+5V Power Regulator (Slave)
VJ1	V	+5V Power Regulator (Master)
VK1	V	

Table 2-4 MMU CABINET COMPONENTS

Component Designator	Zone	Description
A0	A	SCU logic module
A1-A4	A	Four memory modules
W0B	W	Scope and maintenance connectors
ZA0	W/QA0E	Temperature sensor
ZA1	W/QA1J	Temperature sensor
VA1	W0 right side	Battery control
VB1	W0 right side	Battery
VB2	W0 right side	Battery
VB3	W0 right side	Battery

2.4.2 MMU Circuit Boards By Location

Table 2-5 MMU CIRCUIT BOARDS BY LOCATION

MMU CABINET (SCU Module)			
MODULE/SLOT		BOARD	FUNCTION
A0	A	SCAMM	Early Cycle Timing
A0	B	SCAME	Look Ahead
A0	C	SCAMJ	Mode Register
A0	D	SCUMK	Mask Register
A0	E	SCAMC	Config. Register
A0	F	SCAMF	Early Cycle Flags
A0	G	SCUMY	Memory Interface Port
A0	H	SCUMY	Memory Interface Port
A0	J	SCUMY	Memory Interface Port
A0	K	SCUMY	Memory Interface Port
A0	L	SCAMX	CPU/IOM Interface Port
A0	M	SCAMX	CPU/IOM Interface Port
A0	N	SCAMX	CPU/IOM Interface Port
A0	P	SCAMX	CPU/IOM Interface Port
A0	Q	SCAMX	CPU/IOM Interface Port
A0	R	SCAMX	CPU/IOM Interface Port
A0	S	SCAMX	CPU/IOM Interface Port
A0	T	SCAMX	CPU/IOM Interface Port
A0	U	SCUMH	Cache Clear Option

Table 2-5 MMU CIRCUIT BOARDS BY LOCATION (continued)

MMU CABINET (Main Memory)					
MODULE/SLOT		BOARD	FUNCTION	BOARD	FUNCTION
		16K MEMORY		64K MEMORY	
A1	A	M128	Memory	M64	Memory
A1	B	M128	Memory	M64	Memory
A1	C	M128	Memory	M64	Memory
A1	D	M128	Memory	M64	Memory
A1	E	ML2DD	EDAC	M64	Memory
A1	F	M128	Memory	M64	Memory
A1	G	M128	Memory	M64	Memory
A1	H	M128	Memory	M64	Memory
A1	J	M128	Memory	M64	Memory
A1	K	M128	Memory	M64	Memory
A1	L	M128	Memory	M64	Memory
A1	M	M128	Memory	M64	Memory
A1	N	M128	Memory	M64	Memory
A1	P	ML2DD	EDAC	M64	Memory
A1	Q	M128	Memory	M64	Memory
A1	R	M128	Memory	M64	Memory
A1	S	M128	Memory	ML2DD	EDAC
A1	T	M128	Memory	ML2DD	EDAC
A1	U	ML2PF	SCU Port	ML2RP	SCU Port

2.4.2 MMU Circuit Boards By Location (continued)

Table 2-5 MMU CIRCUIT BOARDS BY LOCATION (continued)

MMU CABINET (Main Memory)					
MODULE/SLOT		BOARD	FUNCTION	BOARD	FUNCTION
		16K MEMORY		64K MEMORY	
A2	A	M128	Memory	M64	Memory
A2	B	M128	Memory	M64	Memory
A2	C	M128	Memory	M64	Memory
A2	D	M128	Memory	M64	Memory
A2	E	ML2DD	EDAC	M64	Memory
A2	F	M128	Memory	M64	Memory
A2	G	M128	Memory	M64	Memory
A2	H	M128	Memory	M64	Memory
A2	J	M128	Memory	M64	Memory
A2	K	M128	Memory	M64	Memory
A2	L	M128	Memory	M64	Memory
A2	M	M128	Memory	M64	Memory
A2	N	M128	Memory	M64	Memory
A2	P	ML2DD	EDAC	M64	Memory
A2	Q	M128	Memory	M64	Memory
A2	R	M128	Memory	M64	Memory
A2	S	M128	Memory	ML2DD	EDAC
A2	T	M128	Memory	ML2DD	EDAC
A2	U	ML2PF	SCU Port	ML2RP	SCU Port

Table 2-5 MMU CIRCUIT BOARDS BY LOCATION (continued)

MMU CABINET (Main Memory)					
MODULE/SLOT		BOARD	FUNCTION	BOARD	FUNCTION
		16K MEMORY		64K MEMORY	
A3	A	M128	Memory	M64	Memory
A3	B	M128	Memory	M64	Memory
A3	C	M128	Memory	M64	Memory
A3	D	M128	Memory	M64	Memory
A3	E	ML2DD	EDAC	M64	Memory
A3	F	M128	Memory	M64	Memory
A3	G	M128	Memory	M64	Memory
A3	H	M128	Memory	M64	Memory
A3	J	M128	Memory	M64	Memory
A3	K	M128	Memory	M64	Memory
A3	L	M128	Memory	M64	Memory
A3	M	M128	Memory	M64	Memory
A3	N	M128	Memory	M64	Memory
A3	P	ML2DD	EDAC	M64	Memory
A3	Q	M128	Memory	M64	Memory
A3	R	M128	Memory	M64	Memory
A3	S	M128	Memory	ML2DD	EDAC
A3	T	M128	Memory	ML2DD	EDAC
A3	U	ML2PF	SCU Port	ML2RP	SCU Port

2.4.2 MMU Circuit Boards By Location (continued)

Table 2-5 MMU CIRCUIT BOARDS BY LOCATION (continued)

MMU CABINET (Main Memory)					
MODULE/SLOT		BOARD	FUNCTION	BOARD	FUNCTION
		16K MEMORY		64K MEMORY	
A4	A	M128	Memory	M64	Memory
A4	B	M128	Memory	M64	Memory
A4	C	M128	Memory	M64	Memory
A4	D	M128	Memory	M64	Memory
A4	E	ML2DD	EDAC	M64	Memory
A4	F	M128	Memory	M64	Memory
A4	G	M128	Memory	M64	Memory
A4	H	M128	Memory	M64	Memory
A4	J	M128	Memory	M64	Memory
A4	K	M128	Memory	M64	Memory
A4	L	M128	Memory	M64	Memory
A4	M	M128	Memory	M64	Memory
A4	N	M128	Memory	M64	Memory
A4	P	ML2DD	EDAC	M64	Memory
A4	Q	M128	Memory	M64	Memory
A4	R	M128	Memory	M64	Memory
A4	S	M128	Memory	ML2DD	EDAC
A4	T	M128	Memory	ML2DD	EDAC
A4	U	ML2PF	SCU Port	ML2RP	SCU Port

2.5 IOM CABINET CONFIGURATION

The IOM cabinet contains a power and cooling component in Zones V and B, a cable bulkhead area in Zone W, and IOM circuit boards in Zone A.

Figure 2-5 illustrates the major components of the IOM cabinet, their physical location, and their zone designators.

Table 2-6 lists the component designator, zone, and description of each component.

Table 2-7 lists each circuit board in the IOM by module/slot, board name, and function.

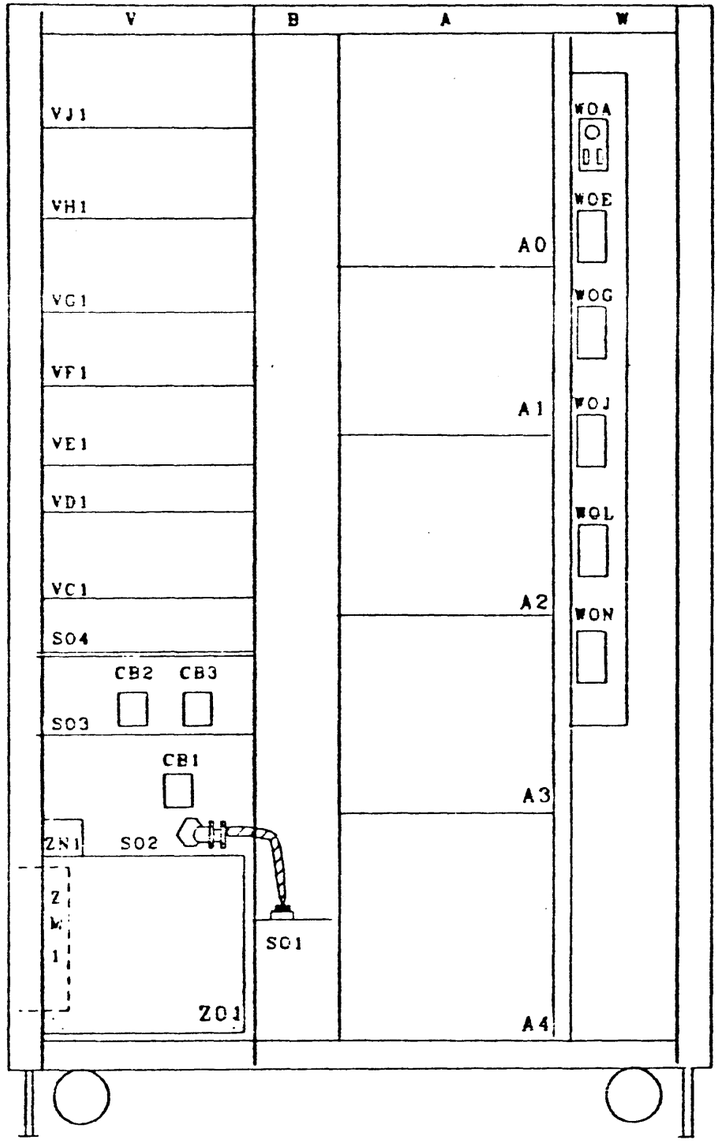


FIGURE 2-5 IOM CABINET FRONT DOORS REMOVED

2.5.1 IOM Cabinet Components

Table 2-6 IOM CABINET COMPONENTS

Component Designator	Zone	Description
ZM1	Bottom portion Zone	Blower controls assembly
Z01	V	Blowers
ZN1	Left from lower position zone	Airflow sensor and switch assembly
S01	Lower portion of Plenum Zone B	Site power connector terminal board (S01 TB1)
S02	V	Circuit Breaker Module, contains circuit breaker (S02 CB1) that applies power to the cabinet
S03	V	Power Entry Module with circuit breakers (S03-CB2/CB3) for FAN and REG. power on/off control
VC1	V	Power Control Module with Power Control & Configuration switches and indicators
VD1	V	Dual +24 Volt Regulator 100 Watt
VE1/VE2	V	-5V Power Converter Regulator
VF1	V	Dual +12V Regulator
VG1	V	
VH1	V	Dual +5V Power Regulator
VJ1	V	
A0-A4	A	Logic modules
W0A	W	Maintenance and scope cable connector
W0A	W	Adapter plate
ZA0	W	Temperature sensor A0B
ZA1	W	Temperature sensor A1B

2.5.2 IOM Circuit Boards By Location

Table 2-7 IOM CIRCUIT BOARDS BY LOCATION

IOM CABINET (IOM)		
MODULE/SLOT	BOARD	FUNCTION
A0		
A	NSBIM1	Scratch Pad
B	NSBIM2	Scratch Pad
C	NSAMY1	SCU Interface
D	NSAMY2	SCU Interface
E	NSAMY3	SCU Interface
F	NSAMY4	SCU Interface
G	NSAIC	IOM Central
H	NSAIE	IOM Central
J	NSAIG	IOM Central
K	645ID	Extended Address
L	DMPIF	Configuration Panel Interface
M	DMPIH	Configuration Panel Interface
N	DMPIJ	Configuration Panel Interface
P	NSAIK	IOM Central
Q	NSAIB	Control Board
R		
S	NSDIA	Control "A"
T		
U	NSAIP	Wraparound

Table 2-7 IOM CIRCUIT BOARDS BY LOCATION (continued)

IOM CABINET (IOM)		
MODULE/SLOT	BOARD	FUNCTION
A1		
A	MQXIU	Bus Driver
B	NSAJP	PSIA
C	MQXJR	Tape MPC Interface Port
D	NSAJC	PSIA
E	MQXJR	Disk MPC Interface Port
F	NSAJP	PSIA
G	NSAJC	PSIA
H	NSAJB	Card MPC Interface Port
J		
K		
L		
M		
N		
P		
Q		
R		
S		
T		
U		

2.5.2 IOM Circuit Boards By Location (continued)

Table 2-7 IOM CIRCUIT BOARDS BY LOCATION (continued)

IOM CABINET (IOM)		
MODULE/SLOT	BOARD	FUNCTION
A2		
A	MQXIN	Bus Driver
B		
C		
D		
E	EURCB	Embedded Unit Record Cont.
F		
G		
H		
J		
K		
L		
M		
N		
P		
Q		
R		
S		
T		
U		

Table 2-7 IOM CIRCUIT BOARDS BY LOCATION (continued)

IOM CABINET (IOM)		
MODULE/SLOT	BOARD	FUNCTION
A3		
A		
B		
C		
D		
E		
F		
G		
H		
J		NOT USED AT THIS TIME
K		
L		
M		
N		
P		
Q		
R		
S		
T		
U		

2.6 MPC CABINET CONFIGURATION

The MPC cabinet contains a power and cooling component in Zones V and B, a cable bulkhead area in Zone W, and MPC circuit boards in Zone A.

Figure 2-6 illustrates the major components of the MPC cabinet, their physical location, and their zone designators.

Table 2-8 lists the component designator, zone, and description of each component.

Table 2-9 lists each circuit board in the MPC by module/slot, board name, and function.

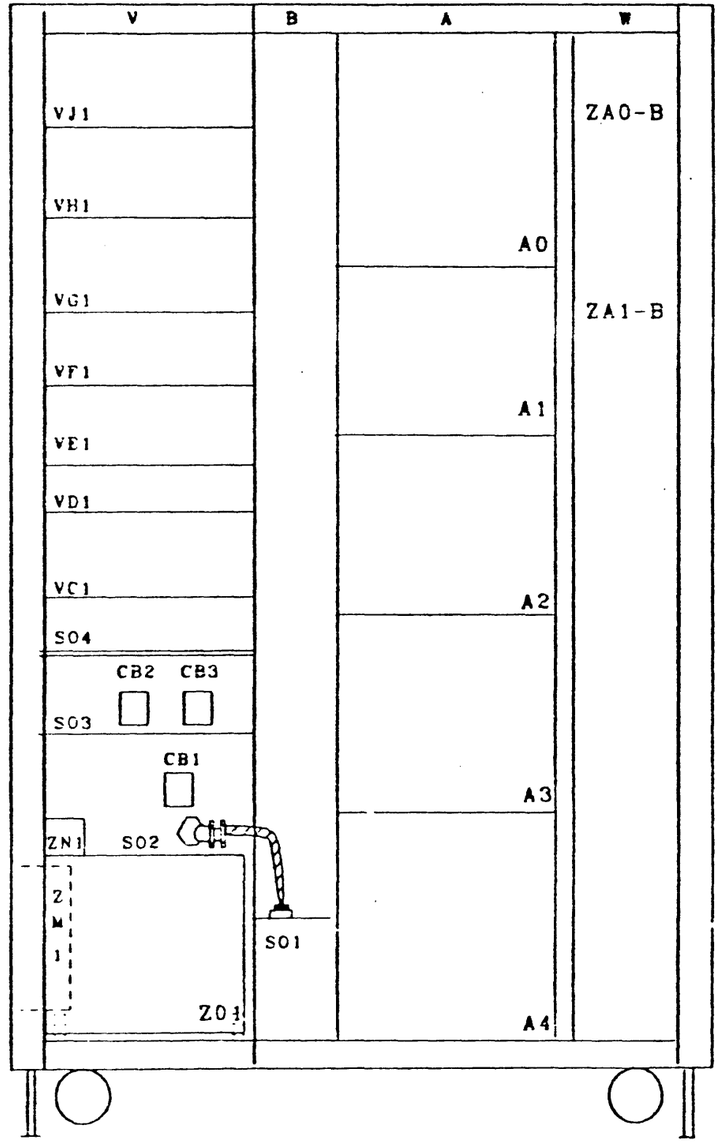


FIGURE 2-6 BASIC MPC (DISC/TAPE) CABINET FRONT DOORS REMOVED

Table 2-8 MPC CABINET CONPONENTS

Component Designator	Zone	Description
ZM1	Bottom portion Zone	Blower controls assembly
Z01	V	Blowers
ZN1	Left from lower position zone V	Airflow sensor and switch assembly
S01	Lower portion of Plenum Zone B	Site power connector terminal board (S01 TB1)
S02	V	Circuit Breaker Module, contains circuit breaker (S02 CB1) that applies power to the cabinet
S03	V	Power Entry Module with circuit breakers (S03-CB2/CB3) for FAN and REG. power on/off control
S04	V	Soft start module
VC1	V	Power Control Module with Power Control & Configuration switches and indicators
VD1	V	100 Watt Voltage Regulator
VE1	V	Front panels
VF1	V	Front panel
VG1	V	Front panel
VH1	V	Front panel
VJ1	V	Capacitor ride thru
A0	A	MPC logic
A1-A4	A	Not used
ZA0-B	W	Temperature sensor
ZA1-B	W	Temperature sensor

2.6.2 MPC Circuit Boards By Location

Table 2-9 MPC CIRCUIT BOARDS BY LOCATION

DISC MPC CABINET		
MODULE/SLOT	BOARD	FUNCTION
A0		
A		
B		
C		
D		
E		
F		
G		
H		
J		
K		
L		
M	MPCLR	IOM Interface
N	MPCLC	MSL Interface
P		
Q	MPCNH	
R	DURIM	Config. Panel Interface
S	MPCFN	Config. Panel Interface
T	UPCRA	Config. Panel Interface
U	DURRO	Config. Panel

Table 2-9 MPC CIRCUIT BOARDS BY LOCATION (continued)

DISC MPC CABINET		
MODULE/SLOT	BOARD	FUNCTION
A1		
A		
B		
C		
D		
E		
F		
G		
H		
J		
K		
L		
M		
N		
P		
Q		
R		
S		
T		
U		

2.7 SYSTEM MAINTENANCE AND CONTROL PANELS

2.7.1 Introduction

The Multics System cabinets may be configured as freestanding or as a single system module consisting of the CPU, MMU, IOM. The following sections will discuss the single system module.

The system panels are classified in the following groups:

- Power/Control Panels
- Configuration Panels
- Maintenance and Test Panels
- Maintenance Panel Connector Plate

These panels will be described in the following cabinet order.

IOM (WIOU66LA) Cabinet

MMU (WMMU66LA) Cabinet

CPU (WCPU68LA) Cabinet

MPC (WMSP645A) Cabinet

Each of these cabinet sections contain a top illustration of the single system module configuration and then the particular cabinet. These figures will also illustrate the operator's control panel, door mounted panels, maintenance panel connector plate, and the cabinet zone location designators.

2.7.2 Power Control Panels

The Power Control Panels on the DPS-8 cabinets are basically the same. They are located in cabinet Zone V and are listed, for all cabinets in Table 2-10.

The illustrations for the Power Control Panels are Figures 2-7 thru 2-10.

Table 2-10 POWER CONTROL PANELS

Location Zone Designator	Description	Located In IOM	MMU	CPU	MPC
SO2	Circuit Breaker Module	X	X	X	X
SO3	Power Entry Module	X	X	X	X
VC1	Power Control Module	X	X	X	X
VD1	+24V 100W Regulator Module	X	[1]X	X	X
VE1/VE2	-5V Converter Regulator Module		X		
VF1	+5V 180W Power Regulator Module	X	[2]X	X	
VG1	+5V 180W Power Regulator Module	X	[2]X	X	X
VH1	+5V 180W Power Regulator Module		X	X	X
VJ1	Capacitor Ride Thru Module	X	[3]X	X	X

[1] +12V 100W Regulator Module
[2] Dual +12 100W Regulator Module
[3] +5V 180W Power Regulator Module

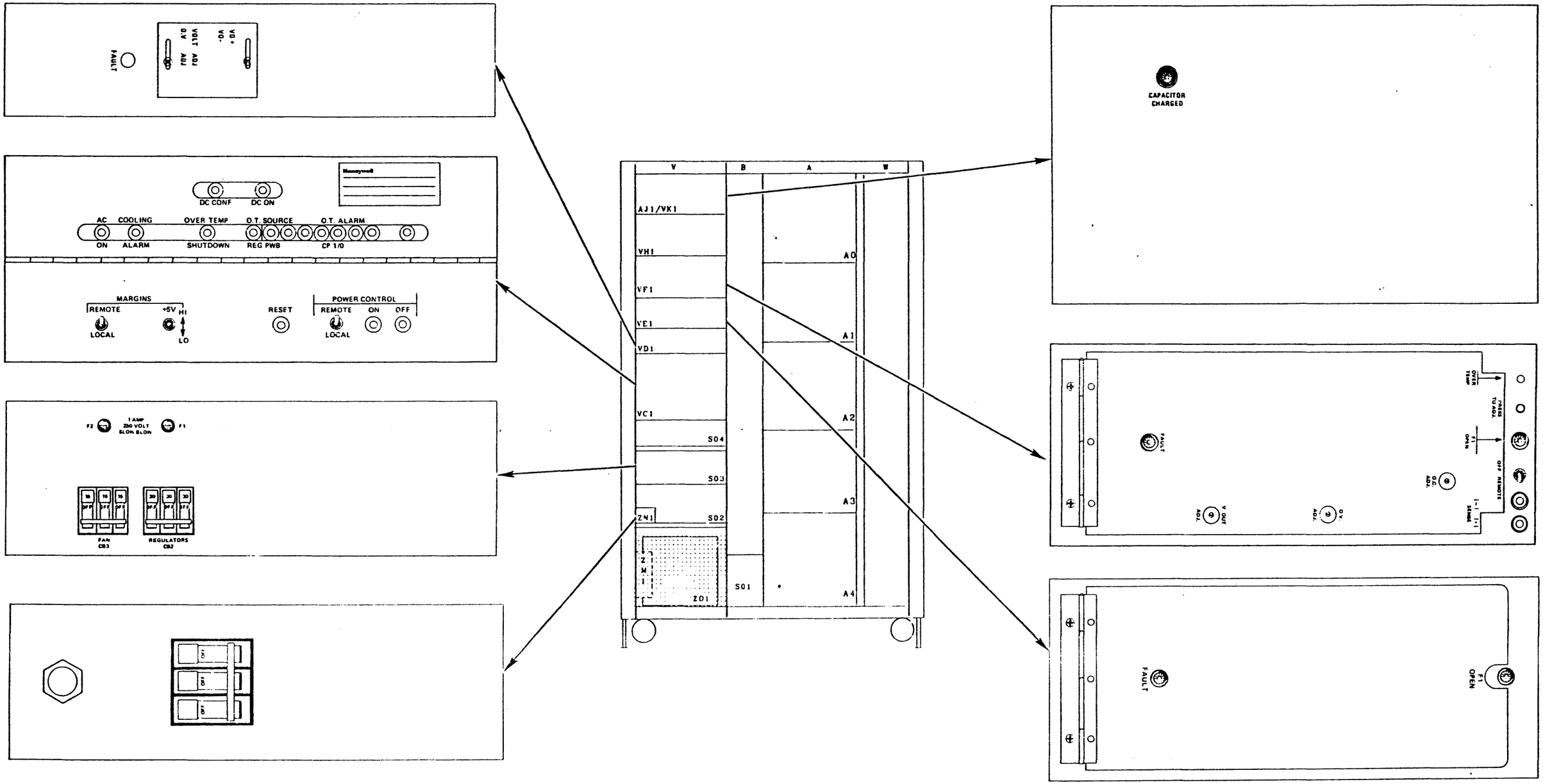


FIGURE 2-7 IOM POWER PANELS

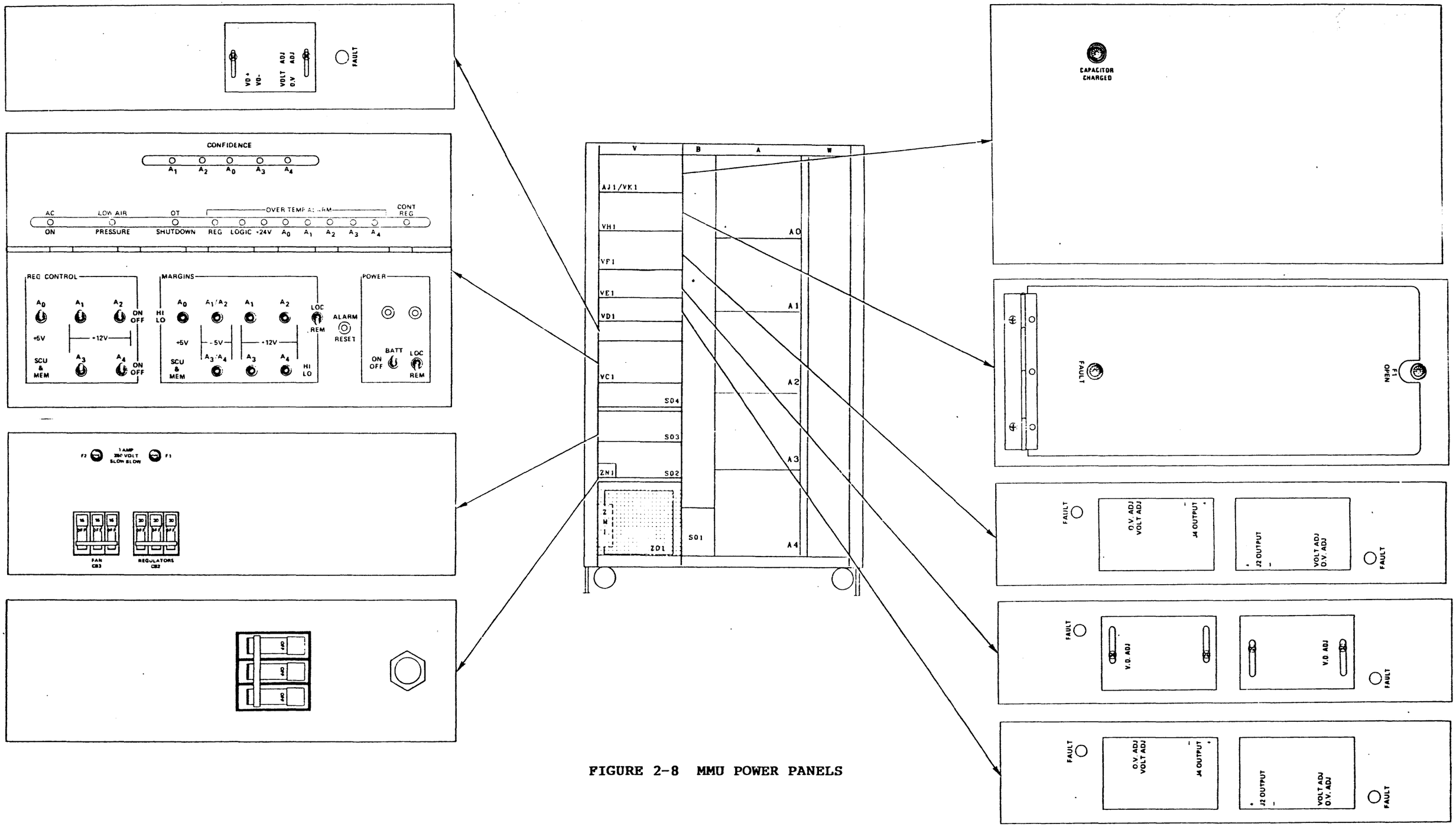


FIGURE 2-8 MMU POWER PANELS

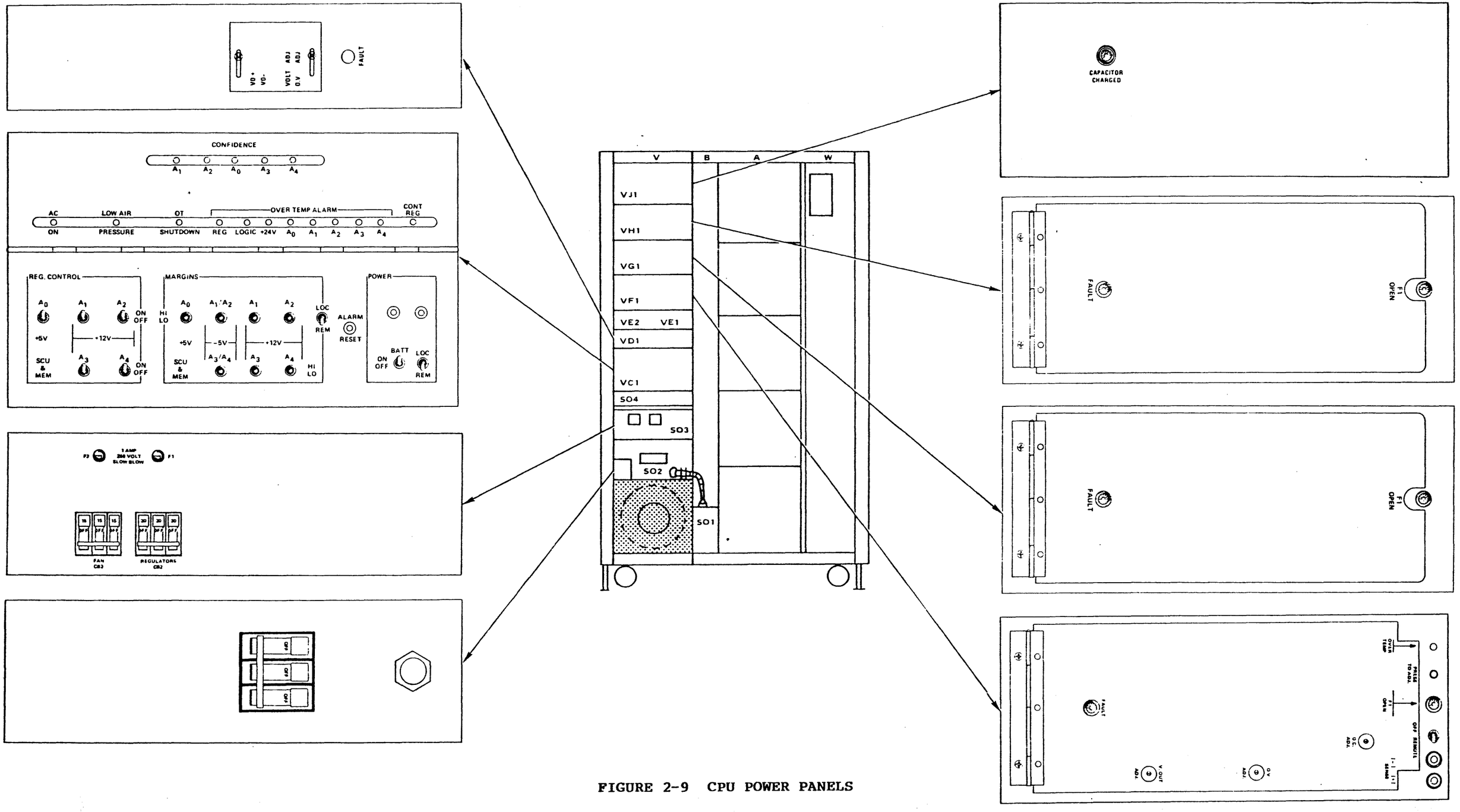


FIGURE 2-9 CPU POWER PANELS

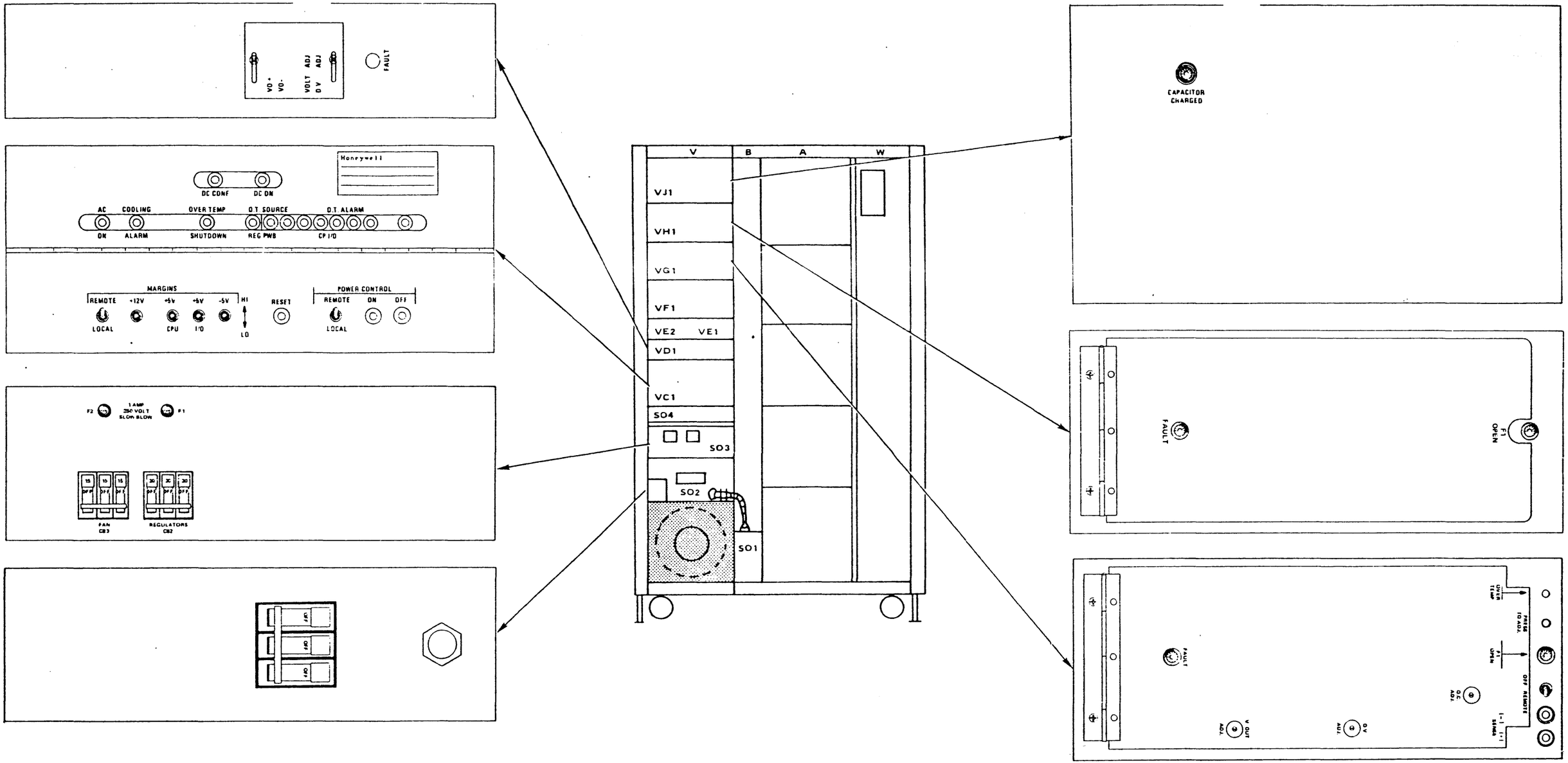


FIGURE 2-10 MPC POWER PANELS

2.7.3 IOM Cabinet Panels

The IOM Cabinet Panel locations, Figure 2-11, illustrates the IOM Cabinet locations in the single system module. Also illustrated are the cabinet zone locations designators, operators control panel, maintenance panel connector, IOM configuration and bootload panels located on the inside of the left door. Refer to the Test and Repair manual, 58009927, for more information.

The IOM Cabinet zone V contains the power panels. They are listed in Table 2-10 and illustrated in Figure 2-7.

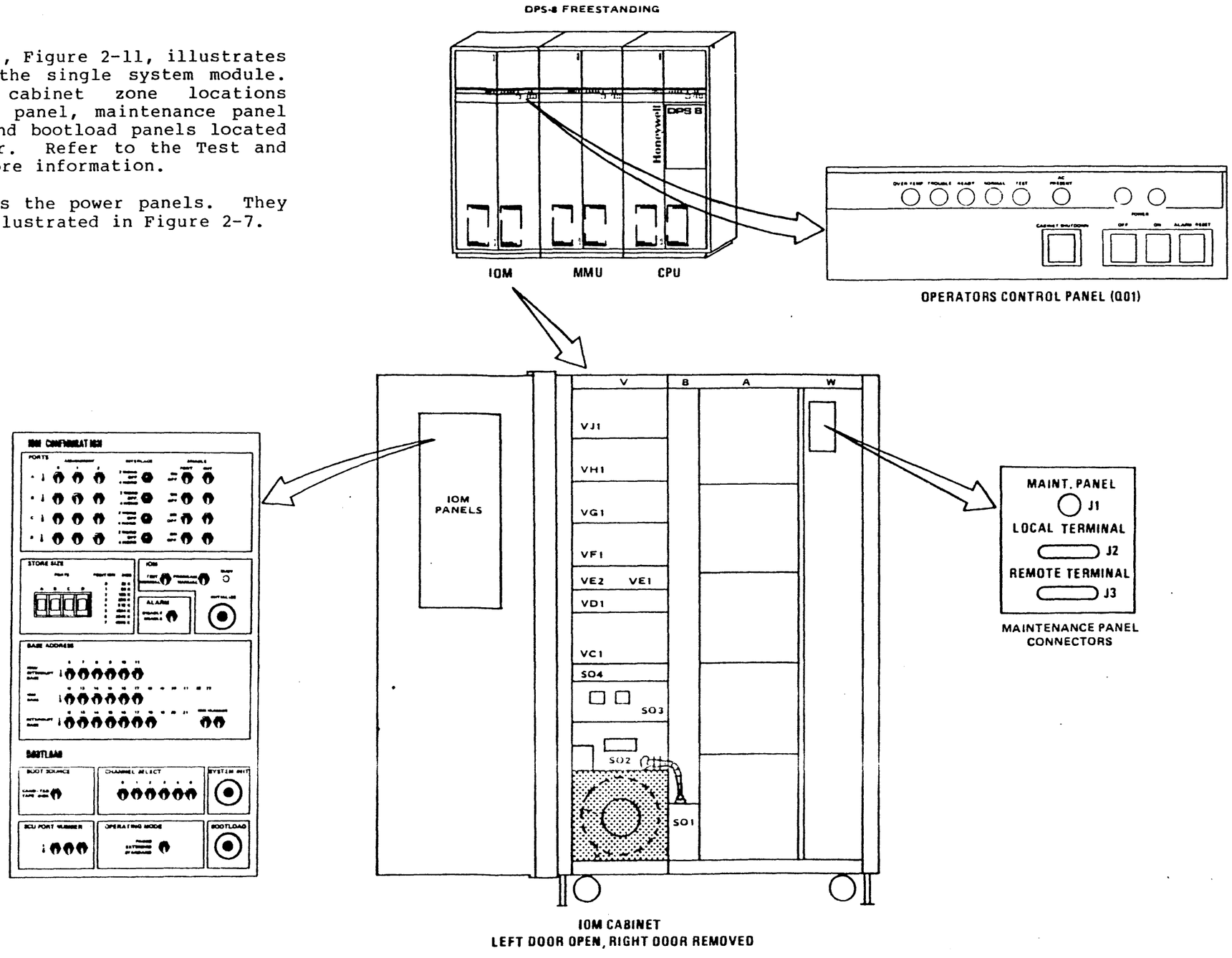


FIGURE 2-11 IOM CABINET PANEL LOCATIONS

2.7.4 MMU Cabinet Panels

In the single system module configuration, the MMU cabinet is the center cabinet. Operators panel, maintenance panel connector plate, syndrome panel, SCU configuration panel, and SCU maintenance panel are illustrated in Figure 2-9. The syndrome and SCU panels are located on the inside of the left door. Refer to the Test and Repair manual, 58009927, for more information. Figure 2-12 illustrated the MMU Cabinet Panel locations. Cabinet zone V contains the cabinet power panels, these are listed in Table 2-10 and illustrated in Figure 2-8.

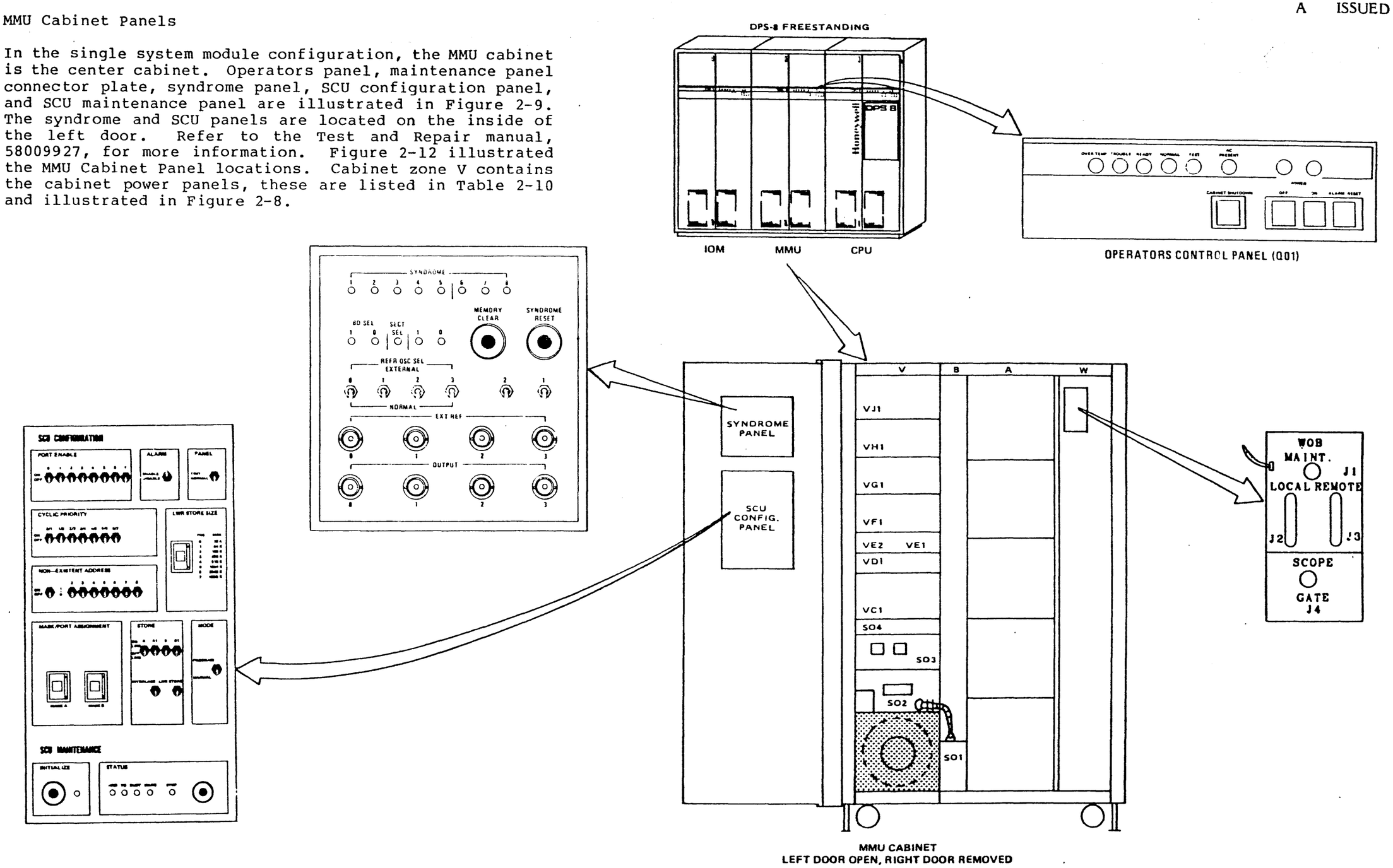


FIGURE 2-12 MMU CABINET PANEL LOCATIONS

2.7.5 CPU Cabinet Panels

In the single system module, the CPU cabinet is to the extreme right as illustrated in Figure 2-13. The operators control panel is mounted on the front of the right door.

Also, illustrated in Figure 2-13 are the Zone location designators, maintenance panel connector, and CPU configuration panel. The CPU configuration panel is located on the inside of the left door. Refer to the Test and Repair manual, 58009927, for more information. The CPU configuration panel is located on the inside of the left door. Refer to the Test and Repair manual, 58009927, for more information. The CPU cabinet Zone V contains the cabinet power panels which are listed in Table 2-10 and illustrated in Figure 2-9.

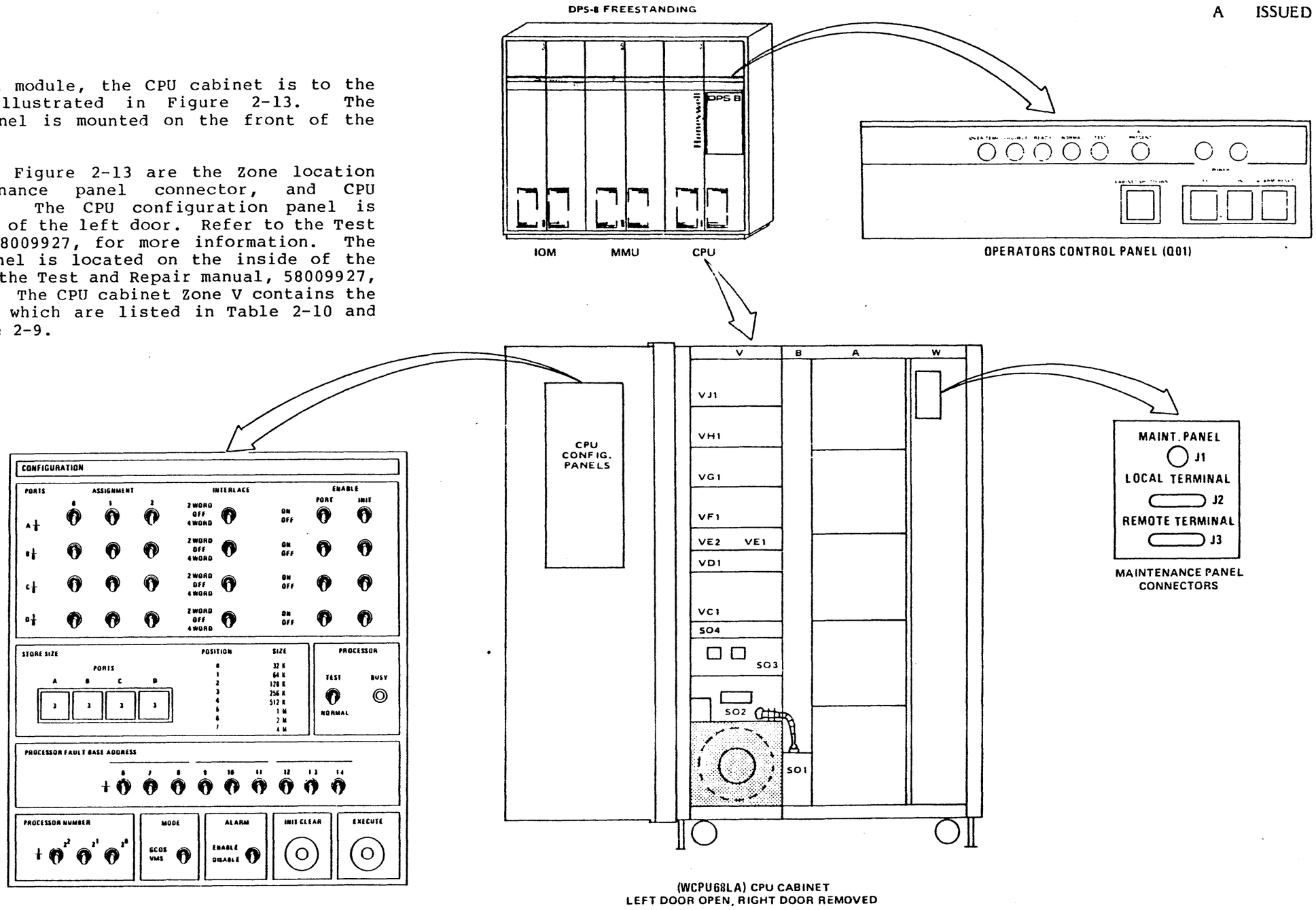
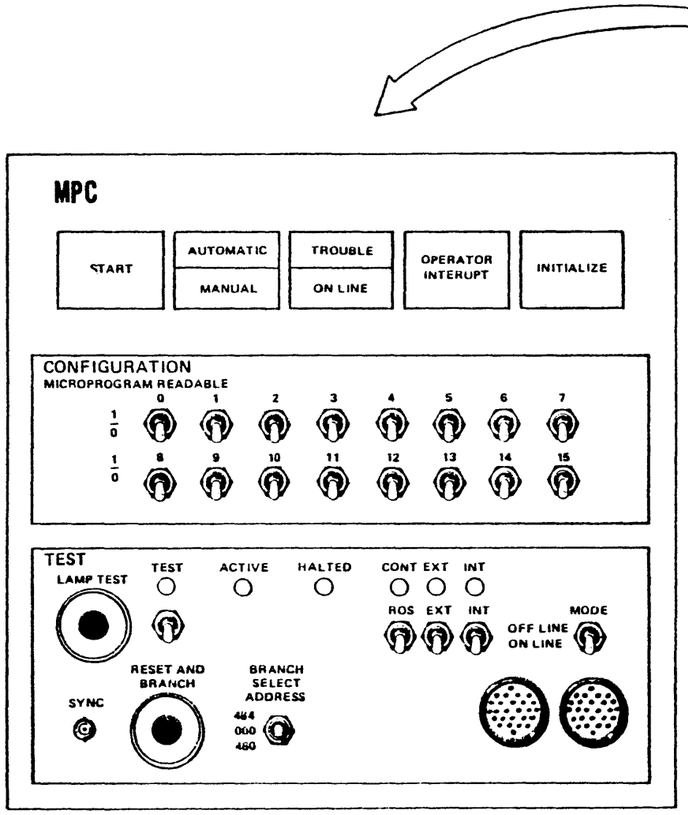


FIGURE 2-13 CPU CABINET PANEL LOCATIONS

2.7.6 MPC Cabinet Panels

The Dual Disc (WMSP645A) MPC Cabinet, Figure 2-14, illustrates the operators control panel and the MPC configuration and test panels. The MPC configuration and test panels are located on the inside of the left door. Refer to the Test and Repair manual, 58009927, for more information.

The MPC cabinet Zone V contains the power panels which are listed in Table 2-10 and illustrated in Figure 2-10.



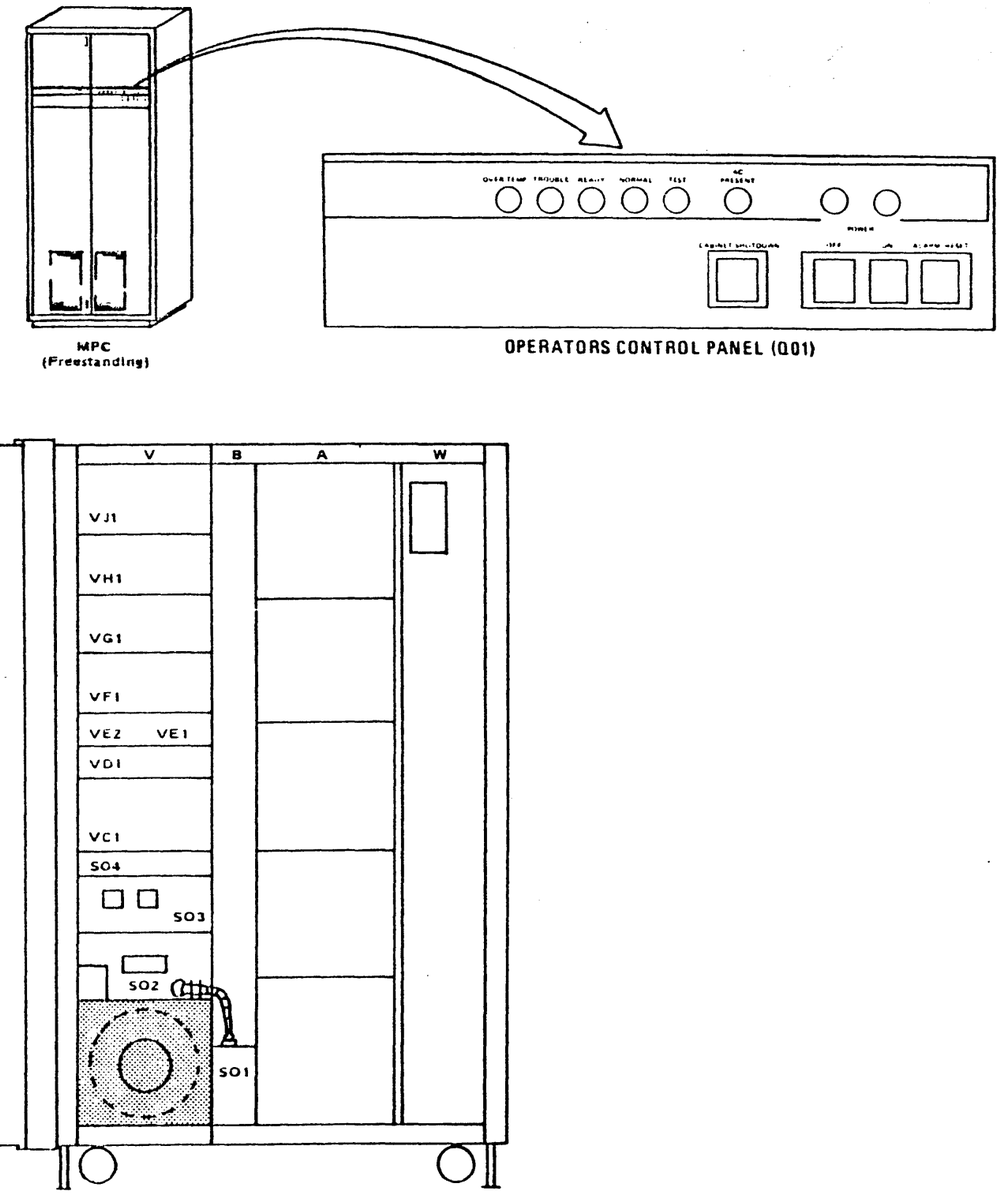


FIGURE 2-14 MPC CABINET PANEL LOCATIONS

2.8 SYSTEM OPTIONS

2.8.1 Introduction

The basic system configuration and functions may be enhanced or expanded by the addition of selected options to provide the customer with additional data processing capability.

Additional available options are listed in Table 2-11 thru 2-14. These options are listed by cabinet.

The selection of options is determined by the customer's system operational requirements. A single option installation may provide the customer with the desired function. Other functions may require more than one option or previously installed option to interface with each other to perform the desired function.

2.8.2 IOM Options

Performance features of the IOM and the system can be enhanced by the selection and installation of options listed in Table 2-11.

Table 2-11 is a listing of additional options available for IOM cabinet installation. General classifications of the features provided by these options are as follows:

- Stabilize and increase cabinet power
- Change input/output data speed between the IOM and its peripheral devices
- Add or change system console interface
- Increase the number of interface ports, channels, and control memory.

Table 2-11 IOM OPTIONS

CAPABILITY & APPLICATION DESCRIPTION	
ACTIVE PORT OPTION (I.O.M. TO S.C.U.)	WIPO66LB-001
ACTIVE PORT INTERFACE WITH THE S.C.U. IS PROVIDED BY THIS OPTION. THE OPTION CONSITS OF A LOGIC BOARD ("NSAMY") INSTALLED IN THE I.O.M., A LOGIC BOARD ("SCAMX") INSTALLED IN THE S.C.U. AND A FREE-EDGE CABLE TO CONNECT BETWEEN THE I.O.M. "NSAMY" BOARD AND THE S.C.U. "SCAMX" BOARD.	
HIGH SPEED P.S.I.A.	WCHO041B-001
THIS OPTION IS A SUB-FEATURE TO THE I.O.M. TO INTERFACE THE HIGH SPEED CONTROL ADAPTER BOARD TO THE I.O.M. BUS. THE OPTION CONSISTS OF THREE CHANNEL BOARDS ("NSAJP", "MQXJR" & "NSAJC") AND A CABLE TO INTERFACE THE TAPE "MT8PS" BOARD OR THE DISK "MPCLR".	
STANDARD SPEED P.S.I.A.	WCHO042B-001
THIS OPTION IS A SUB-FEATURE TO THE I.O.M. AND IS USED TO INTERFACE LINK ADAPTER BOARD TO THE I.O.M. BUS. THE OPTION CONSISTS OF THREE BOARDS ("NSAJP", "NSAJB" & NSAJC") AND A CABLE TO INTERFACE THE TAPE/U.R.C. "MPCLA" BOARD.	
HIGH SPEED P.S.I.A. (I.O.M. TO M.P.C.'S)	WHO041B-001
THIS OPTION IS A SUB-FEATURE TO THE I.O.M. AND IS USED TO INTERFACE THE I.O.M. WITH THE FREE-STANDING M.P.C.'s. THE OPTION CONSISTS OF THREE BOARDS ("NSAJP", "MQXJR", "NSAJC") AND A CABLE FOR DEVICE INTERFACE.	
STANDARD SPEED P.S.I.A. (I.O.M. TO M.P.C.'S)	WHO042B-001
THIS OPTION IS A SUB-FEATURE TO THE I.O.M. AND IS USED TO INTERFACE THE I.O.M. WITH FREE-STANDING M.P.C.'s. THE OPTION CONSISTS OF THREE BOARDS ("NSAJP", "NSAJB", "NSAJC") AND A CABLE FOR DEVICE INTERFACE.	
DIRECT CHANNEL OPTION	WDDC66LA-001
THIS OPTION IS A SUB-FEATURE TO THE I.O.M. FOR INTERFACE WITH THE 18X. IT CONSISTS OF ONE "NSBJM" BOARD AND A CABLE FOR INTERFACE BETWEEN THE FREE-EDGE OF THE "NSBJM" BOARD AND THE 18X.	

Table 2-11 IOM OPTIONS (continued)

CAPABILITY & APPLICATION DESCRIPTION	
SYSTEM CONSOLE OPTIONS	58056588-014 WLCC001A 43C144536G1
THESE OPTIONS INTERFACE THE SYSTEM ENTRY LEVEL CONSOLE (VIP) TO THE MULTICS SYSTEM. THE OPTIONS CONSIST OF THE VIP KEYBOARD AND VIDEO DISPLAY, DC/DC CONVERTER, "CONJK" ADAPTER BOARD, CABLE ADAPTER AND HARNESS, AND INTERFACE CABLE BETWEEN THE VIP AND CABLE ADAPTER.	
SYSTEM CONTROL CENTER ADAPTER	
THIS OPTION INTERFACES THE 4WSCC655AB1 SYSTEM CONTROL CENTER OR 4WEMC655AA1 ENTRY MODEL CONSOLE TO THE I.O.M. THE OPTION CONSISTS OF ONE "MQXJK" BOARD, A FREE-EDGE TO JUNCTION PANEL CABLE, AND NECESSARY BACKPANEL BERG CONNECTORS. TWO OF THESE OPTIONS ARE NECESSARY FOR THE S.C.C. (THE SECOND IS USED TO DRIVE THE STATUS DISPLAY). ONE 4WSCE6555AB1 SYSTEM CONSOLE EXTENDED ADDRESS BOARD MUST BE ORDERED FOR EVERY TWO OPTIONS.	
SYSTEM CONSOLE EXTENDED ADDRESS	
THIS OPTION CONSISTS OF ONE "645JK" BOARD AND IS REQUIRED IF CONSOLE MESSAGES ARE STORED IN MEMORY OTHER THAN THE FIRST 256K OF STORE.	
ADDITIONAL CHANNEL SPACE OPTION	WDCK66LA-001
THIS OPTION ADDS 18 ADDITIONAL CHANNEL SLOTS TO THE I.O.M. IT CONSISTS OF ONE 19 SLOT CARD CAGE WITH INTERCONNECTING CABLE AND ONE "MQXIN" BUS DRIVER BOARD. A MAXIMUM OF TWO ADDITIONAL CHANNEL SPACE OPTIONS MAY BE INSTALLED. THE POWER SUPPLY REGULATOR OPTION (WPSR66LA-001) IS REQUIRED WHENEVER ONE OR TWO "ADDITIONAL CHANNEL SPACE" OPTIONS ARE INSTALLED.	
CHANNEL CONTROL MEMORY (SCRATCH PAD)	SCCM66LA-001
THIS OPTION PROVIDES HARDWARE "SCRATCH PAD" STORAGE FOR I/O CONTROL WORDS FOR 24 CONSECUTIVE PAYLOAD CHANNELS. IT CONSISTS OF ONE "NSBIM" BOARD AND A FREE-EDGE JUMPER CONNECTOR TO CONNECT IT TO THE ADJACENT "NSBIM" BOARD.	
POWER SUPPLY REGULATOR OPTION	WPSR66LA-001
THIS OPTION IS A SUB-FEATURE TO THE I.O.M. AND IS USED TO PROVIDE ADDITIONAL POWER FOR ADDITIONAL CHANNEL OPTIONS.	

Table 2-11 IOM OPTIONS (continued)

CAPABILITY & APPLICATION DESCRIPTION	
CAPACITOR RIDE-THRU (OPTION)	WCAP66LA-001

THIS OPTION IS A SUB-FEATURE OF THE I.O.M. AND IS USED TO INCREASE THE UNIT'S ABILITY TO OPERATE THROUGH POWER INTERRUPTIONS FROM 4 ms TO 100 ms.

I.O.M. CONFIGURATION PANEL OPTION	WICP66LB-001

THIS OPTION PROVIDES FOR MOUNTING OF THE I.O.M. CONFIGURATION PANEL ASSEMBLY ON THE INSIDE OF THE LEFT FRONT DOOR OF AN I.O.M. FREE-STANDING CABINET.

2.8.3 MMU Options

Performance features of the MMU and this system can be enhanced by installation of additional options listed in Table 2-12.

Table 2-12 is a listing of available options for the MMU cabinet installation. General classification of the features provided by the available options are as follows:

- Stabilize and increase cabinet power
- Increase memory size
- Increase SCU interface ports

Table 2-12 MMU OPTIONS

CAPABILITY AND APPLICATION DESCRIPTION	
DPS 8/70 MAIN MEMORY UNIT	WMMU66LA-001
THIS MODEL NUMBER DESCRIBES THE BASIC CABINETRY FOR HOUSING ONE (1) SCU OPTION PLUS FOUR (4) MEMORY OPTIONS. A BATTERY OPTION OR CAPACITOR OPTION IS AVAILABLE WITH ANY COMBINATIONS OF MEMORIES OR SCU'S.	
MEMORY MODULE .75usec	WMQL66LA-001
THIS IS THE MOS MEMORY OPTION (16K 16 PIN) WHICH INCLUDES THE CONTROLLER FOR 75 MICROSECOND CYCLE TIME. THE OPTION CONSISTS OF A 19 CARD BACKPANEL ASSEMBLY, TWO (2) ML2DD (ERROR CORRECTION AND DETECTION BOARDS), ONE (1) ML2PF (.75 MICROSECOND PORT CONTROL BOARD), A REFRESH OSCILLATOR PWB, AND A FEATURE APPLICATION INDEX WHICH OFFERS MOS STORAGE IN INCREMENTS OF 256K X 40 BITS. A QUANTITY OF ZERO (0) TO FOUR (4) OPTIONS MAY BE CALLED FOR IN LOCATIONS A1, A2, A3, AND/OR A4.	
MOS MEMORY	WMOS256A-001
THIS IS A 256K X 40 BIT WORD MEMORY INCREMENT OF M128 MOS MEMORY BOARDS. THE MEMORY MODULE CAN SUPPORT UP TO FOUR (4) OF THESE INCREMENTS. EACH INCREMENT CONSISTS OF FOUR (4) M128 MEMORY BOARDS.	

Table 2-12 MMU OPTIONS (continued)

CAPABILITY AND APPLICATION DESCRIPTION	
SCU OPTION	WSCU66LA-001
A SYSTEM CONTROL UNIT CAPABLE OF INTERFACING UP TO FOUR (4) MILLION WORDS OF MEMORY. THIS 4MW SCU CONSISTS OF A CONFIGURATION PANEL, A 19 CARD BACKPANEL ASSEMBLY, SIX (6) CONTROLLER BOARDS (SCAMM, SCAME, SCAMJ, SCUMK, SCAMC, AND SCAMF), A TERMINATION STRIP ON THE BACKPANEL, AN OPTIONAL MAXIMUM OF FOUR (4) SCUMY MEMORY PORTS, AND AN OPTIONAL MAXIMUM OF EIGHT (8) SCAMX SYSTEM PORTS. ZERO (0) OR ONE (1) SCU MAY BE CALLED FOR IN LOCATION A0.	
CAPACITOR RIDE THRU	WCAP66LA-001
THIS OPTION IS A SUBFRAME OF THE SCU/MEM AND IS USED TO INCREASE THE UNIT'S ABILITY TO OPERATE THROUGH POWER INTERRUPTIONS FROM 4ms TO 100ms. ONE (1) OPTION MAY BE INSTALLED IN LOCATION VK1. THIS OPTION IS NOT REQUIRED IF BATTERY POWER OPTION (WBAT66LA) IS PRESENT.	
BATTERY POWER OPTION	WBAT66LA-001
ADDS BATTERIES AND BATTERY CHARGER TO KEEP CONTENTS OF THE MEMORY VALID DURING LOSS OF POWER.	

Table 2-12 MMU OPTIONS (continued)

CAPABILITY AND APPLICATION DESCRIPTION	
+5V REGULATOR (SLAVE) MODULE	WPSR66LC-001
THIS OPTION PROVIDES A +5V SLAVE REGULATOR AND IS INSTALLED IN LOCATION VH1. THIS OPTION IS ADDED ONLY WHEN THE MOS MEMORY OPTIONS WMOS256A-001 INSTALLED IN THE CABINET EXCEEDS EIGHT OR THE WMOS64KA-001 EXCEEDS 32.	
+12V REGULATOR MODULE	WPSR66LD-001
THIS OPTION PROVIDES A +12V REGULATOR. ONE (1) OR TWO (2) MAY BE INSTALLED IN LOCATION VG1 AND VH1. ONE (1) +12V REGULATOR WILL PROVIDE THE REQUIRED +12V POWER FOR UP TO TWO (2) MEMORY MODULES (WMQL66LA). THE 2ND +12V REGULATOR WILL BE ADDED WHEN THE MEMORY MODULES INSTALLED IN THE CABINET EXCEEDS TWO (2).	
-5V REGULATOR MODULE	WPSR66LE-001
THIS OPTION PROVIDES A -5V REGULATOR. ONE (1) OR TWO (2) MAY BE INSTALLED IN LOCATION VE1 AND VE2. ONE (1) -5V REGULATOR WILL PROVIDE THE REQUIRED -5V POWER FOR UP TO TWO (2) MEMORY MODULES (WMQL66LA). THE 2ND -5V REGULATOR WILL BE ADDED WHEN THE MEMORY MODULES INSTALLED IN THE CABINET EXCEEDS TWO (2).	
SYNDROME PANEL OPTION	WSDM66LA-001
THIS OPTION PROVIDES A SYNDROME DISPLAY FOR FROM ONE (1) TO FOUR (4) MEMORY MODULES. ONE (1) OR TWO (2) MAY BE INSTALLED IN LOCATION Q01 AT THE TOP INSIDE LEFT DOOR.	
MEMORY PORT OPTION	WMPO66LA-001
THIS SCU HAS A MAXIMUM OF FOUR (4) PASSIVE (TWO SIMULTANEOUS) MOS MEMORY PORTS. THIS OPTION CONSISTS OF ONE SCUMY HARD COPPER PWB ASSEMBLY.	
HARDWARE CACHE CLEAR OPTION	WHCC66LB-001
THIS OPTION PROVIDES ONE (1) SCUMH BOARD INSTALLED IN SLOT "U". SEE WHCC66LA-001 OPTION IN TABLE 2-13 FOR CACHE CABLE.	

Table 2-12 MMU OPTIONS (continued)

CAPABILITY AND APPLICATION DESCRIPTION	
MEMORY MODULE .75Uusec	WMQL64KA-001
THIS IS THE MOS MEMORY OPTION (64K 16-PIN) WHICH INCLUDES THE CONTROLLER FOR .75 MICROSECOND CYCLE TIME. THE OPTION CONSISTS OF A 19 CARD BACKPANEL ASSEMBLY, TWO (2) ML2DD (ERROR CORRECTION AND DETECTION BOARDS), ONE (1) ML2PF (.75 MICROSECOND PORT CONTROL BOARD), AND A REFRESH OSCILLATOR PWB. A QUANTITY OF ZERO (0) TO FOUR (4) OPTIONS MAY BE CALLED FOR IN LOCATIONS A1, A2, A3, AND/OR A4.	
MOS MEMORY	WMOS64KA-001
THIS IS A 256K WORD MEMORY INCREMENT OF M64 MOS MEMORY BOARDS. THE WMQL64KA-001 MEMORY MODULE CAN SUPPORT UP TO 16 OF THESE MEMORY INCREMENT BOARDS. THE WSDM64KA-001 SYNDRMOE DISPLAY OPTION MUST BE USED WITH THIS MEMORY OPTION.	
64K SYNDROME PANEL OPTION	WSDM64KA-001
THIS OPTION PROVIDES A SYNDROME DISPLAY FOR FROM ONE (1) TO FOUR (4) MEMORY MODULES WITH 64K CHIPS.	

2.8.4 CPU Options

Performance of the CPU and the system can be enhanced by the installation of additional options listed in Table 2-13.

Table 2-13 is a listing of additional options available for the CPU cabinet. General classification of the features provided by the options listed in Table 2-13 are as follows:

- Addition interface ports to SCU
- Stabilize cabinet power
- Effectively increase memory size

Table 2-13 CPU OPTIONS

CAPABILITY AND APPLICATION DESCRIPTION	
ACTIVE PORT OPTION (C.P.U. TO S.C.U.)	WIPO68LA-001
THIS OPTION CONSISTS OF A ONE-BOARD ("SCAMX") ADDITION TO THE S.C.U. AND A ONE-PORT INTERFACE CABLE TO INTERFACE THE PROCESSOR WITH THE S.C.U. BETWEEN THE C.P.U. FREE-EDGES OF THE "ETCCD", "ETMCQ", "ETMCM" BOARDS, AND THE S.C.U. FREE-EDGE OF THE "SCAMX" BOARD.	
CAPACITOR RIDE-THRU OPTION	WCAP66LA-001
THIS OPTION IS A SUB-FEATURE OF THE C.P.U. AND IS USED TO INCREASE UNIT'S ABILITY TO OPERATE THRU POWER INTERRUPTIONS FROM 4ms TO 100ms.	
CACHE CABLE OPTION	WHCC68LA-001
THIS OPTION CONSISTS OF ONE CABLE FOR INTERFACE OF THE C.P.U. CACHE WITH THE S.C.U. HARDWARE CACHE CLEAR. THE "HARDWARE CACHE CLEAR" OPTION (WHCC66LB) MUST BE INSTALLED IN THE S.C.U. BEFORE INSTALLING THIS OPTION. SEE TABLE 2-12 FOR THE WHCC66LB OPTION.	

Table 2-13 CPU OPTIONS (Continued)

CAPABILITY AND APPLICATION DESCRIPTION	
"ETCMP" BOARD MAINTENANCE FIRMWARE	WPMP002A-001
THIS OPTION PROVIDES BOARD TEST AND PORTABLE MAINTENANCE PANEL CAPABILITY FOR THE "ETCMP" BOARD BY THE ADDITION OF BOARD-PLUGABLE PROGRAMMED E-PROMS.	

2.8.5 MPC Options (Disk)

Performance of the MPC interface between the system and peripheral devices can be enhanced by the installation of additional options listed in Table 2-14. A general classification of the features provided by the options listed in Table 2-14 are as follows:

- Stabilize and increase cabinet power
- Modify present interface
- Expand cabinet configuration for dual disk information
- Increase type of peripheral devices serviced.

Table 2-14 MPC OPTIONS (DISK)

CAPABILITY AND APPLICATION DESCRIPTION	
DUAL DISC CONTROLLER OPTION	WASP645A-001
THIS OPTION CONSISTS OF TWO (2) BACKPANELS (BUCKETS) AND FIVE (5) BASIC MPC PRINTED WIRE BOARDS PLUS ONE (1) MPCLR (LINK ADAPTER) BOARD, THE DISC CONTROL ADAPTER OPTIONS (WMSP001A-001 AND WMSP002A-001) ARE MANDATORY AS WELL AS POWER REGULATOR OPTION (WPSR200D-001).	
500 DISC CONTROL ADAPTER	WMSP001A-001
THIS OPTION CONSISTS OF FOUR (4) 500 CONTROL ADAPTER PWB'S PLUS ONE (1) MPCD1 BOARD ALLOWING CAPABILITY TO CONNECT TO THE "500" OR "501" DISC DRIVES. SEE WADE001A-001 OPTION BELOW FOR ADDITIONAL "MPCDI" BOARDS.	
450 DISC CONTROL ADAPTER	WMSP002A-001
THIS OPTION CONSISTS OF THREE (3) 451 CONTROL ADAPTER PWB'S PLUS ONE (1) MPCD1 BOARD ALLOWING CAPABILITY TO CONNECT TO THE "450" DISC DRIVES. SEE WADE001A-001 OPTION BELOW FOR ADDITIONAL "MPCDI" BOARDS.	
ADDITIONAL DRIVE ELECTRONICS	WADE001A-001
THIS OPTION CONSISTS OF AN ADDITIONAL MPCD1 BOARD AND TWO (2) CONNECTOR GUIDES WHICH PROVIDE THE CAPABILITY TO CONNECT FOUR (4) MSU "500"/"501" or "450" DISC DRIVES. A MAXIMUM OF FOUR (4) MPCD1 BOARDS ARE ALLOWED IN EACH "WMSP" CONTROL ADAPTER.	
CAPACITOR RIDE-THRU OPTION	WCAP66LA-001
THIS OPTION IS A SUB-FEATURE OF THE MPC AND IS USED TO INCREASE UNIT'S ABILITY TO OPERATE THRU POWER INTERRUPTIONS FROM 4ms TO 100ms. (ONE PER CABINET).	
MASS STORE LINK ADAPTER	WNLA001A-001
THIS OPTION PROVIDES INTERFACE CAPABILITY TO LEVEL 66 HI-SPEED PS1A.	

Table 2-14 MPC OPTIONS (DISK) (Continued)

CAPABILITY AND APPLICATION DESCRIPTION	
MASS STORE LINK ADAPTER (MODIFIED)	WMLA001A-001
THIS OPTION PROVIDES INTERFACE CAPABILITY TO 355 OR 18X.	
CONTROL STORE MODIFICATION KIT	58052503-001
THIS MODIFICATION INCREASES THE CONTROL STORE MEMORY FROM 8K TO 16K.	
"BOOT FROM DISC" MODIFICATION KIT	WBFD001A-001
THIS MODIFICATION ADDS "BOOT FROM DISC" CAPABILITY TO THE CONTROL STORE PWB.	
DEVICE PERMIT PLUG OPTION	
THIS OPTION CONSISTS OF ONE (1) WIRED PLUG ALLOWING A MIX OF 500/501/509 DEVICES PLUS ONE OF THE FOLLOWING: PLUS 1 (ONE) 7-TRACK TAPE--TYPE NRZ1 WOPT01LA-001 PLUS 1 (ONE) 9-TRACK TAPE--TYPE NRZ1 WOPT01LA-002 PLUS 1 (ONE) 9-TRACK TAPE--TYPE PE WOPT01LA-003	
DEVICE PERMIT (L) PLUG	
THIS OPTION CONSISTS OF ONE (1) WIRED PLUG ALLOWING A MIX OF 500/501/509 DEVICES (LIMITED TO 16 SPINDLES), PLUS ONE OF THE FOLLOWING: PLUS 1 (ONE) 7-TRACK TAPE--TYPE NRZ1 WOPT02LA-001 PLUS 1 (ONE) 9-TRACK TAPE--TYPE NRZ1 WOPT02LA-002 PLUS 1 (ONE) 9-TRACK TAPE--TYPE PE WOPT02LA-003	
POWER REGULATOR	WPSR200D-001
THIS IS A 200 AMP REGULATOR WHICH IS REQUIRED TO SUPPLY POWER FOR THE DUAL DISC CONTROLLER OPTION (WASP645A-001).	

3.0 SYSTEM THEORY

3.1 GENERAL INFORMATION

This section presents a functional view of the DPS 8 Freestanding Multics System and a system-oriented description of each major unit in the system (IOM, CPU, MMU, DPU, MPC). Included is a functional map of the system.

The DPS 8 Freestanding Multics System is basically the three individual unit cabinets (MMU, IOM, CPU) plus the operating and diagnostic peripheral devices necessary for the specific applications as dictated by the individual user requirements.

Normal operating power for each unit and peripheral device is obtained from the facility and is converted/regulated within the unit/peripheral device itself.

Emergency backup power (in case of facility power interruptions) for uses such as protection of the volatile MOS memory in the MMU cabinet is obtained from optional power equipment located in the MMU cabinet. For details, refer to the Power and Cooling Manual, 58009911.

System earth ground is obtained only at the MMU cabinet. The CPU and IOM cabinets connect to the earth ground lead at the MMU cabinet. Systems containing more than one (1) MMU cabinet have a single earth ground system at the first/primary MMU cabinet.

Figure 3-1, the functional map, shows a minimum Freestanding DPS 8 Central System plus the supporting control devices and peripheral equipment normally available for systems of any size. The following paragraphs describe the system functionally and follow the inter-unit signals through interface cabling.

A maximum central system is configured as follows:

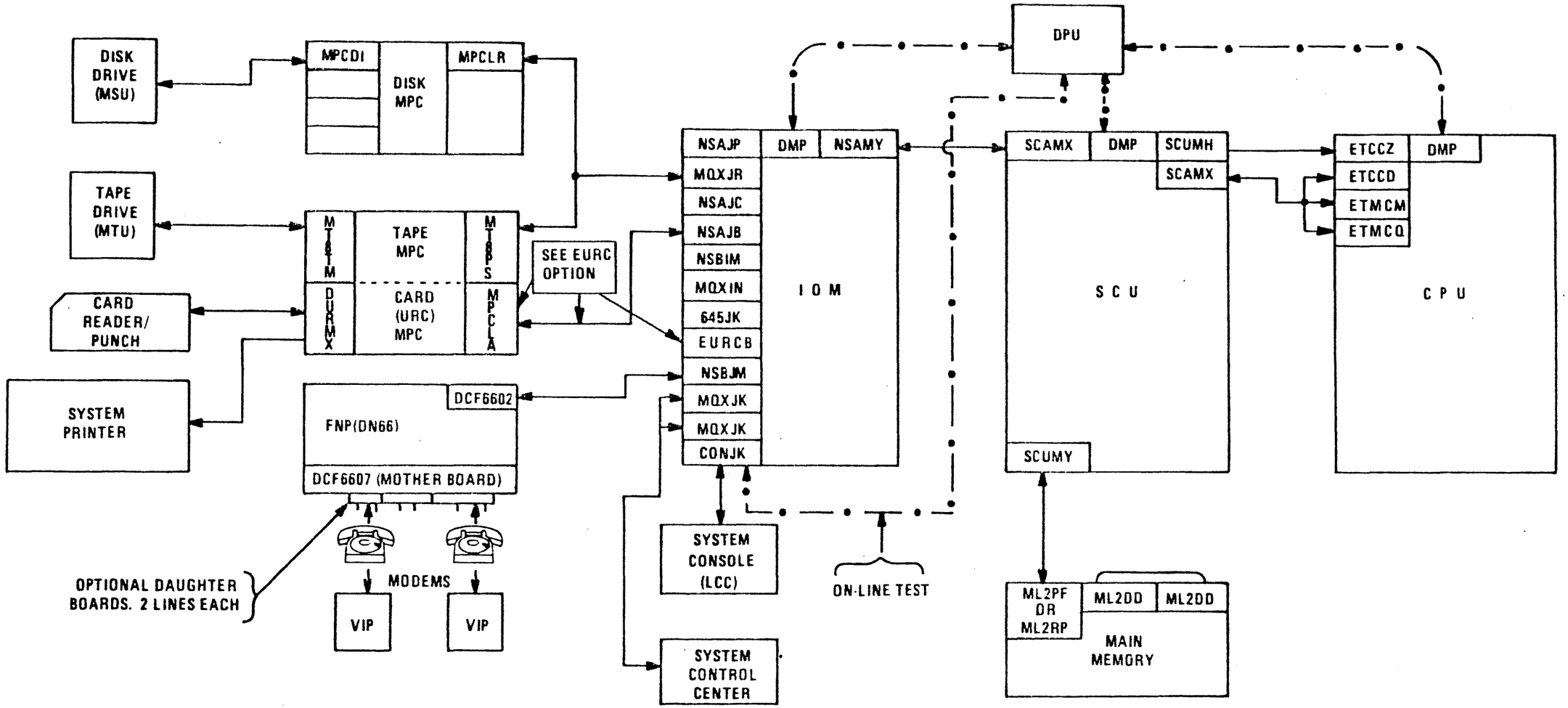
- Four MMU cabinets containing a total of four SCU's and up to 64 megawords of memory.
- Four (4) IOM cabinets (maximum)
- Six (6) CPU cabinets (maximum)

NOTE

IN NO INSTANCE, REGARDLESS OF INDIVIDUAL SYSTEM CONFIGURATION REQUIREMENTS, MAY THE TOTAL OF ALL CPU AND IOM CABINETS EXCEED EIGHT.

NOTE

FOR LENGHTS OF CABLES MENTIONED IN THIS SECTION, REFER TO DN01 SITE PREPARATION MANUAL.



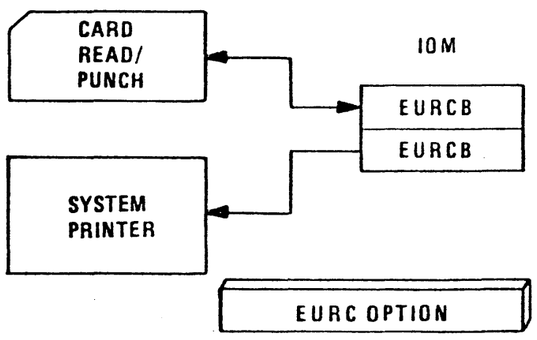


FIGURE 3-1. FREESTANDING MULTICS SYSTEM FUNCTIONAL MAP

3.1.1 Features of the Multics System

The maximum number of CPU's in the Multics system is eight. Effectively, this number is reduced to seven or less since at least one of the SCU active ports must be used to service an IOM. The number of active ports in the SCU remains at eight. Previous recognition of processor ports E, F, G, and H is dropped.

Several instructions which specified the processor port selection by C (TPR.CA)$_{0-2}$ will now ignore bit position 0. Port selection for L68/DPS-E is specified by C (TPR.CA)$_{1-2}$. The affected instructions are:

Op Code	Mnemonic	Name
633(0)	RCCL	Read Calendar Clock
233(0)	RMCM	Read Memory Controller Mask Register
451(0)	SMIC	Set Memory Controller Interrupt Cells
553(0)	SMCM	Set Memory Controller Mask Register

Processor number now occupies three bits in the control unit data, bit positions 27-29 of word 2, rather than 2 bits. The affected instructions are:

Op Code	Mnemonic	Name
657(0)	SCU	Store Control Unit
513(0)	RCU	Restore Control Unit

Reduction in the number of processor ports and the rearrangement of data fields in the Read Switches instruction allows elimination of instructions RSW3 and RSW4.

3.1.1.1 Associative Memories

The Segment Description Word and page Table Word Associative memories are extended to 64 words from 16 words. The 64 word associative memories are organized as four level set-associative.

Existing T&D instructions which loaded the associative memories are deleted. These are not required for new T&D tests. The deleted instructions are:

Op Code	Mnemonic	Name
257(1)	LPTP	Load Page Table Pointers
173(1)	LPTR	Load Page Table Registers
257(0)	LSDP	Load Segment Descriptor Pointers
232(1)	LSDR	Load Segment Descriptor Registers

The T&D instructions which stored contents of the associative memory are modified to accommodate the increase of size to 64 words. These are:

Op Code	Mnemonic	Name
557(1)	SPTP	Store Page Table Pointers
154(1)	SPTR	Store Page Table Registers
557(0)	SSDP	Store Segment Descriptor Printers
254(0)	SSDR	Store Segment Descriptor Registers

3.1.1.2 Hardware-Controlled Cache

The Multics CPU has a built-in 8K word hardware controlled cache memory. This design eliminates the need for certain cache clears and cache bypass modes.

A synchronizing function, whose purpose is to ensure integrity of gated shared data, is provided in the instruction repertoire (see 58009907 CPU Unit Manual). This function is added to the STC2 and STACQ instructions. This addition is needed to support 8K cache processors in multiprocessor, multi SCU systems.

An additional performance improvement involves the group of Read-alter-rewrite instructions. These no longer automatically bypass cache unless a cache bypass mode is in effect. This cache mode is totally controlled by the bypass bit, SDW.C, in the segment descriptor.

Full utilization of the performance capabilities requires changes to Multics software. Among these are replacement of open gate instructions with STC2 or STACQ, and changes to SDW.C to specify cache use instead of bypass.

3.1.1.3 Detailed Description

The Cache bypass option in the segment descriptor word is retained. An overriding bypass enable, bit 68 of the Cache mode register, is added. The cache mode is set as follows:

SDW.C	CMR_{68}	RESULTANT CACHE MODE
Use Cache	X	Use Cache
Bypass Cache	Bypass Cache	Bypass Cache
Bypass Cache	Use Cache	Use Cache

All close gate instructions, LDAC, LDQC, STAC, STACQ, and SZNC automatically bypass Cache. Two features are added to ensure integrity of gated shared data; one is added during the close gate operation and the other during the open gate operation. The instruction following the close gate instruction bypasses cache if the instruction is a Read or a Read-alter-rewrite. The open gate operation must be performed with either a STC2 or STACQ which includes the synchronizing function. The synchronizing function forces the processor to delay the open gate operation until it is notified by the SCU that write completes have occurred and write notifications requesting cache block clears have been sent to the other processors for all write instructions that the processor has previously issued.

Read-alter-rewrite instructions no longer automatically bypass cache. Cache behavior for these instructions is determined fully by SDW.C. If the bypass cache mode is set, these instructions bypass cache and issue read-lock-write-unlock commands to memory. If a cache directory match occurs, the location is cleared.

All accesses to memory by SDW and PTW associative memory hardware continues to bypass cache. Operations used are Reads for SDWs, Read-alter-rewrites with lock for PTWs and setting the page Used bit, and Writes for setting the page Modified and Used bits. For Writes, the hardware also disables the key line so that the SCU lock is honored. This is consistent with dynamic PTW modification by software which also bypasses cache and uses Read-alter-rewrite instructions.

The instructions which clear the associative memories and also clear Cache or selective portions of Cache are changed to eliminate the Cache clear function. Bit C $(TPR.CA)_{15}$ is ignored. These instructions also include disable/enable capabilities for each quarter of the associative memories.

The associative memory replacement is reset upon a CAMP or CAMS so that repeatable behavior occurs under test conditions.

Cache mode register bit 56, which previously controlled Cache bypass for operands, is disregarded. All other Cache control bits are continued. However, maintenance panel cache control function is restricted to Cache half enable/disable functions.

For detailed information on the Multics CPU, refer to paragraph 3.4 and the 58009907 Multics CPU Unit Manual. For detailed information on other units/functions within the Multics System, refer to Figure 1-1 for the appropriate technical manual.

3.2 MMU CABINET

3.2.1 MMU Introduction

The MMU is the principal information storage and retrieval center for the computer. The SCU provides facilities for interfacing with as many as four memory buckets via the memory ports. Since the SCU has interlace capability, more than one memory bucket may be accessed during a memory cycle.

Eight of the logic board locations in the SCU are devoted to active port options to enable communication between the SCU and the IOM/CPU cabinets.

The Main Memory provides customer-selectable information storage capacity for handling the various tasks assigned to the computer system. The Main Memory provides capability of interfacing with the SCU for input and output (read and write cycles) and error detection and correction of all data read from and written into memory.

3.2.2 MMU Description

The MMU cabinet, Figure 3-2, houses the SCU and Main Memory portions of the computer. The one SCU in each cabinet is always located in bucket A0. Main Memory options are located in buckets A1 thru A4. Depending upon the number of options installed, each bucket may contain from 256K words to four megawords. For details on the 16K Main Memory, refer to the 58009909 Main Memory Unit Manual; for details on the 64K Main Memory, refer to Options Installation Manual 58010025 and Unit Manual 58009990. For details on the SCU, refer to the 59009922 SCU Unit Manual.

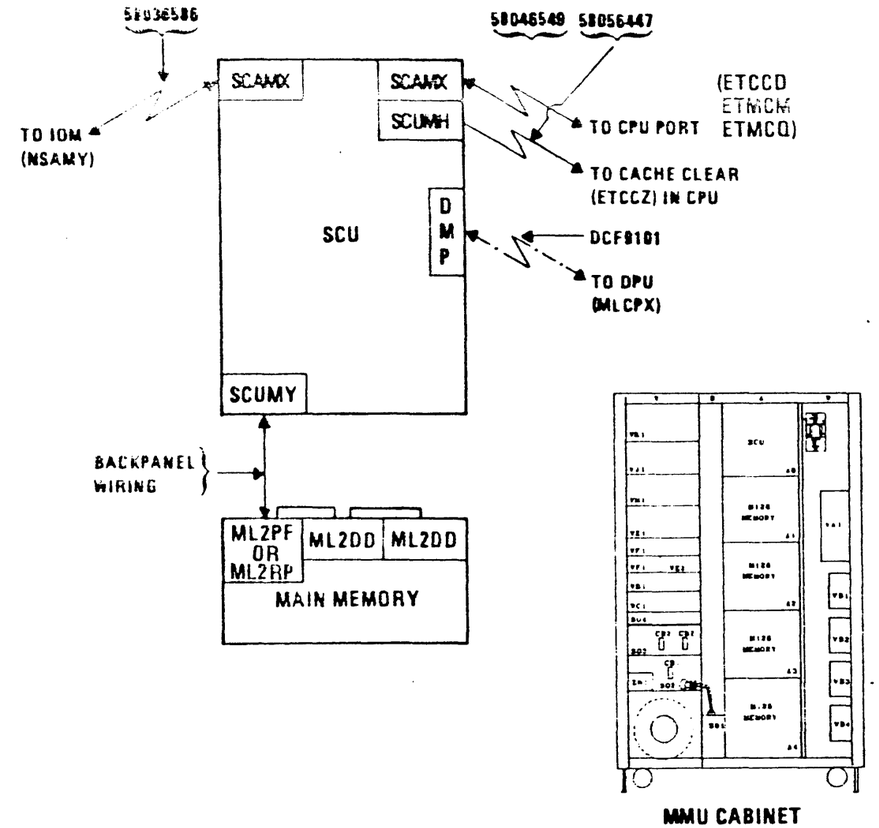


FIGURE 3-2 MMU CABINET INTERFACES

3.2.3 MMU Functions

SCU

Functionally, the System Controller Unit (SCU) is a Main Memory access controller and an interface device between active modules (IOM, CPU). The interrupt signal ($INT) from an active module requesting access to the Main Memory comes from the CPU through the ETMCM board in the CPU and via the 58046549 cable to the SCAMX board in the SCU. A $INT from the IOM is routed through the NSAMY active port board in the IOM and via the 58017984 cable to the SCAMX port board in the SCU.

All signals to/from active modules, except for cache clear signals, are routed to/from the SCU through the SCAMX board. All signals to/from Main Memory utilize the SCUMY memory port board. Cache clear signals to the CPU are routed via the SCUMH cache clear board in the SCU, through the 58056447 cache cable to the ETCCZ board in the CPU.

Main Memory

All signals to and from Main Memory are routed through the 16K memory ML2PF port board or the 64K memory ML2RP port board. Data to and from Main Memory undergoes error detection and correction checks on the ML2DD EDAC boards. During operation of the computer, all access to Main Memory is via the SCU.

3.3 IOM CABINET

3.3.1 IOM Introduction

The Input/Output Multiplexer provides interface capability between the central system computer and the peripheral devices. Most of the signal traffic involves access to memory by a peripheral device. Bulk storage devices connected to the IOM are provided the means to transfer information to and from memory for massaging by an applicable object program in execution.

3.3.2 IOM Description

The IOM is functionally divided into two main areas; the IOM Central and the Channel Section. The Central Section contains the SCU port interface (NSAMY) boards. The NSAMY boards (and associated cabling) provide access to the SCU for memory read and write operations. The same board(s) also provide a link with the CPU's for inter-module communication.

The Channel Section also contains the channel boards which provide connection to and control of various peripheral devices. See Figure 3-3 for the channel boards and the peripheral devices which access the computer via the IOM.

The IOM Central is structured to provide the data paths, control logic, and timing logic necessary to tie the SCU and I/O interfaces together for information exchange.

3.3.2.1 SCU Interface Port

With options available, the IOM may interface with from one to four SCU's. Signals transmitted over the 58017984 interface cable between the IOM (NSAMY port) and the SCU (SCAMX port) are as follows:

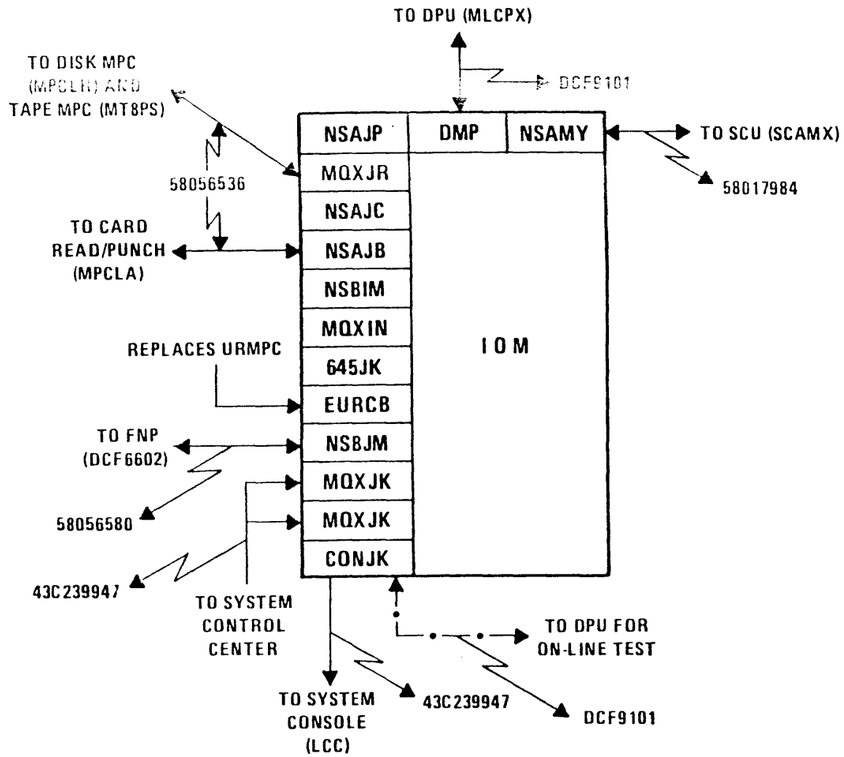


FIGURE 3-3 IOM CABINET INTERFACES

- ZAC information to the SCU
- Read Data from the SCU
- Write Data to the SCU
- Illegal action information from the SCU
- $CON to the SCU
- $XMIT-AP to the SCU
- $XMIT-PA from the SCU
- $DA from the SCU
- INZ Request to the SCU
- INZ from the SCU
- $INT to the SCU
- $PIN from the SCU
- Ready signal from the SCU

3.3.2.2 I/O Interface Port

The number and type of peripheral devices that interface with the IOM depend on the customer options. Figure 3-1 presents a cross section of the devices available and the interface boards used. Signals transmitted between the IOM and the peripheral channels/devices on the I/O bus are presented in Figure 3-4.

Of the signals available at the Channel Ports (Figure 3-4), the transaction command and request for service originate at the System Console or System Control Center. All other signals will be directed to/from the FNP or an MPC.

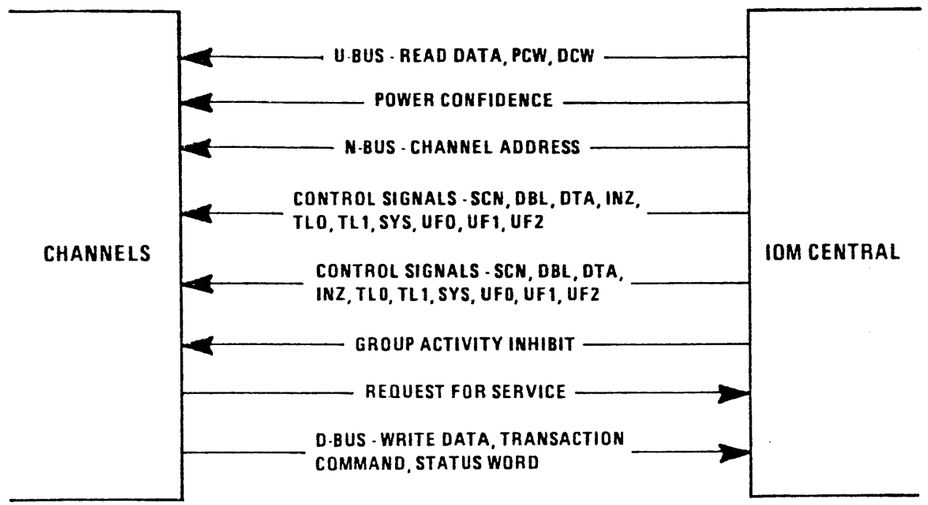


FIGURE 3-4 I/O BUS INTERFACE

3.3.3 IOM Functions

Requests for service and transaction commands are transmitted to/from the LCC to the CONJK board in the IOM via a 43C239947 cable. The same signals from the System Control Center are transmitted to the MQXJK board in the IOM via a 43C239947 cable. When a transaction command involves retrieval of bulk storage data, the IOM accesses the data, as a read data operation, from the bulk data storage equipment (tape drive, disk drive, card reader, etc.) via the 58056536 cable to the NSAJB/MQXJR channel boards (see Figure 3-3).

In read data and write data operations, the NSAMY port control board is the interface point in the IOM, the SCAMX active port control board is the interface point in the SCU, and the 58056586 is the interface cable between the two modules. ZAC information, read data, write data, and all control signals are transmitted/received via the same routing. For details concerning the IOM or any peripheral equipment, consult the appropriate manual listed in Figure 1-1.

3.4 CPU CABINET

3.4.1 CPU Introduction

The Central Processor Unit (CPU) for the Multics system is a freestanding unit that controls program execution and performs computations associated with execution of the programs. Figure 3-5 shows the CPU cabinet profile and a functional view of the interfaces.

The CPU described in this manual is a hardware module designed for use with Multics. The addressing features, in particular, were designed to permit Multics software to compute relative and absolute addresses, locate data and programs in the Multics virtual memory, and retrieve such data and programs as necessary.

3.4.2 CPU Description

3.4.2.1 Features of the Multics CPU

The Multics CPU contains the following general features:

1. Storage protection to place access restrictions on specified segments.

2. Capability to interrupt program execution in response to an external signal (e.g., I/O termination) at the end of any even/odd instruction pair (midinstruction interrupts are permitted for some instructions), to save processor status, and to restore the status at a later time without loss of continuity of the program.

3. Capability to fetch instruction pairs and to buffer two instructions (up to four instructions, depending on certain main memory overlap conditions) including the one currently in execution.

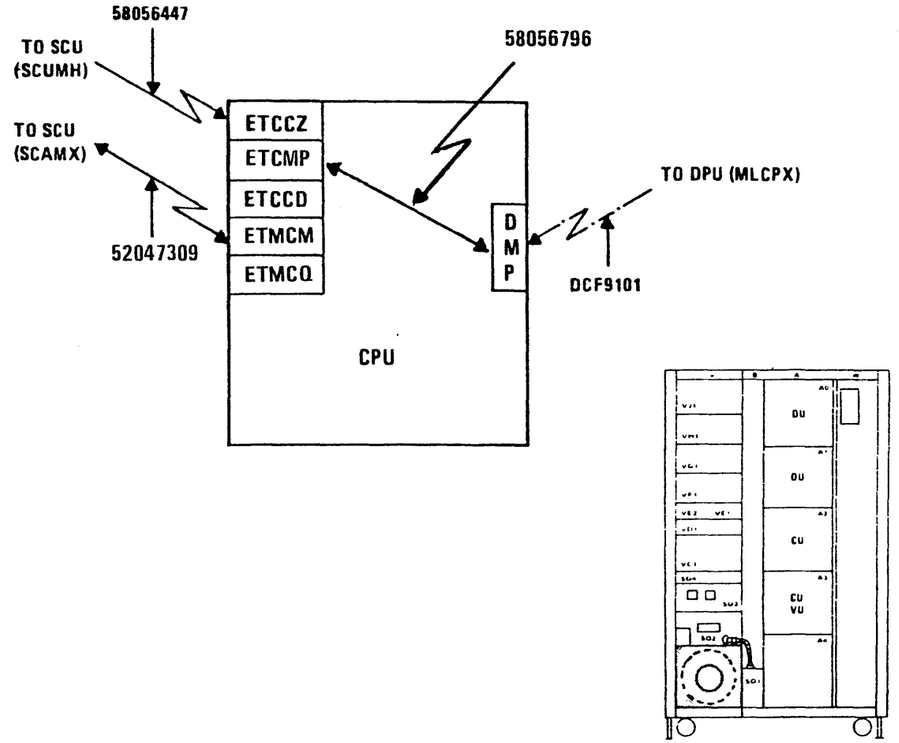


FIGURE 3-5 CPU CABINET INTERFACES

3.4.2.1 (Continued)

4. Overlapping instruction execution, address preparation, and instruction fetch. While an instruction is being executed, address preparation for the next operand (or even the operand following it) or the next instruction pair is taking place. The operations unit can be executing instruction N, instruction N+1 can be buffered in the operations unit (with its operand buffered in a main memory port), and the control unit can be executing instructions N+2 or N+3 (if such execution does not involve the main memory port or registers of instructions N or N+1) or preparing the address to fetch instructions N+4 and N+5. This includes the capability to detect store instructions that alter the contents of buffered instructions and the ability to delay preprocessing of an address using register modification if the instruction currently in execution changes the register to be used in that modification.

5. Interlacing capability to direct main memory accesses to interlaced system controller modules.

6. Intermediate storage of address and control information in high-speed reigsters addressable by content (associative memory).

7. Intermediate storage of base address and control information in pointer registers that are loaded by the executing program.

8. Absolute address computation at execution time.

9. Ability to hold recently referenced operands and instructions in a high-speed look-aside memory (cache memory).

3.4.2.2 CPU Functional Units

The CPU is composed of five functional units:

- Control Unit (CU)
- Operations Units (OU)
- Decimal Unit (DU)
- Appending Unit (AU)
- Associative Memory

3.4.2.2.1 Control Unit

The CU initiates operation of the OU, DU, AU, and Associative Memory and provides operational coordination between these units. The CU contains the following major functional sections.

- Data input/output logic
  - port selection
  - port control
- Instruction buffers and register
- Address preparation and modification logic
- Address basing logic
- Instruction counter and update logic
- Fault and fault-control logic
- Overall timing and control logic
- Timer register
- Cache and cache control logic

3.4.2.2.2 Operations Unit

The OU executes arithmetic and logical operations for most single word instructions. The OU receives operation codes, data formatting information, and operands from the CU. When this information is received, the OU will execute the instructions without further intervention by the CU.

3.4.2.2.3 Decimal Unit

The DU performs decimal arithmetic and bit/character string operations and executes multiword instructions. When the DU has received operation codes, descriptor information, and operands from the CU, it will execute the instruction without further CU intervention unless further operands are requested from the SCU.

3.4.2.2.4 Appending Unit

The appending unit (AU) performs system requirements for segmentation and paging of memory. The appending unit is used to derive a real memory address from a virtual-type address. The virtual memory addresses in a user's program are mapped into pages of real memory. Only those pages of a user's program necessary to sustain operation of the particular user's program need be in memory at any one time. The AU also provides protection of main memory contents. Protection is accomplished through descriptors which determine the memory access rights of programs.

The registers and functions provided by the AU are as follows:

- Provides 24 bit addressing.
- Contains up to 64 segment descriptor words and 64 page table words on a most recently used basis.
- Provides a Descriptor Segment Base Register.
- Provides eight Segment Pointer Registers.
- Provides ring protection hardware.
- Controls fault recognition.
- Controls Main Memory I/O, selection, and interlace.

3.4.2.2.5 Associative Memory Assembly

This assembly consists of 64 (51-bit) page table word associative memory (PTWAM) registers and 64 (108-bit) segment descriptor word associative memory (SDWAM) registers. These registers are used to hold pointers to most recently used segments (SDWs) and pages (PTWs). This unit reduces the need for possible multiple main memory accesses before obtaining an absolute main memory address of an operand or instruction.

3.4.3 CPU Functions

When an operator command or program step requires that the CPU address the SCU (for a write/read data cycle, for example), the ETMCM board in the Control Unit of the CPU issues a $INT to the SCU. The signal is sent via the 58046549 cable to the SCAMX active port control board in the SCU.

With the exception of cache clear information, all signals between CPU and SCU utilize the SCAMX board and the 58046549 cable. Within the CPU, the signal types are always associated with the following boards.

- ETCCZ - Cache Clear
- ETCCD - Data
- ETMCM - Command and Control
- ETMCQ - Zone and Address

In a read data operation, the Zone, Address, and Command (ZAC) word is sent to the SCAMX board in the SCU from the ETMCM board in the CPU, along with any control signals required during the read data request, via the 58046549 cable. In the late cycle, the read data from Main Memory follows the same path.

In a write data operation, the ZAC word is placed in the SCU port register by the ETMCM board. The write data word, whether single or double, is transmitted to the bi-directional data bus in the SCU by the ETMCM board.

All communication between active modules (CPU, IOM) uses the same paths as the data operations.

Write notification information for clearing the CPU cache memory is transmitted from the SCUMH board in the SCU, via the 58056447 Cache Cable, to the ETCCZ board in the CPU.

3.4.3.1 Address Modification and Address Appending

Before each main memory access, two major phases of address preparation take place:

1. Address modification by register or indirect word content, if specified by the instruction word or indirect word.

2. Address appending, in which a virtual memory address is translated into an absolute address to access main memory.

The above two types of modification are combined in most operations. The address modification procedure can go on indefinitely, with one type of modification leading to repetitions of the same type or to other types of modification prior to a main memory access for an operand.

3.4.3.2 Faults and Interrupts

The CPU detects certain illegal instruction usages, faulty communication with the main memory, programmed faults, certain external events, and arithmetic faults. Many of the CPU fault conditions are deliberately or inadvertently caused by the software and do not necessarily involve error conditions. The CPU communicates with the other system modules (IOM's, SCU's, MPC's, and other CPU's) by setting and answering external interrupts. When a fault or interrupt is recognized, a "trap" results. The trap causes the forced execution of a pair of instructions in a main memory location, unique to the fault or interrupt, known as the fault or interrupt vector. The first of the forced instructions may cause safe storage of the CPU status. The second instruction in a fault vector should be some form of transfer, or the faulting program will be resumed at the point of interruption.

Interrupts and certain low-priority faults are recognized only at specific times during the execution of an instruction pair. If, at these times, bit 28 in the instruction word is set ON, the trap is inhibited and program execution continues. The interrupt or fault signal is saved for future recognition and is reset only when the trap occurs.

3.4.3.3 CPU Modes of Operation

There are three modes of main memory addressing (absolute mode, append mode, and BAR mode), and two modes of instruction execution (normal mode and privileged mode).

3.4.3.3.1 Instruction Execution Modes

NORMAL MODE

Most instructions can be executed in the normal mode. Certain instructions, classed as privileged, cannot be executed in normal mode. These are identified in the individual instruction descriptions. An attempt to execute privileged instructions while in the normal mode results in an illegal procedure fault. The CPU executes instructions in normal mode only if it is forming addresses in append mode and the segment descriptor word (SDW) for the executing segment specifies a nonprivileged procedure.

PRIVILEGED MODE

In privileged mode, all instruction can be executed. The CPU executes instructions in privileged mode when forming addresses in absolute mode or when forming addresses in append mode and the segment descriptor word (SDW) for the segment in execution specifies a privileged procedure and the execution ring is equal to zero.

3.4.3.3.2 Addressing Modes

ABSOLUTE MODE

In absolute mode, the final computed address is treated as the absolute main memory address unless the appending hardware mechanism is invoked for a particular main memory reference. During instruction fetches, the procedure pointer register is ignored. The CPU enters absolute mode when it is initialized or immediately after a fault or interrupt. It remains in absolute mode until it executes a transfer instruction whose operand is obtained via explicit use of the appending hardware mechanism.

The appending hardware mechanism may be invoked for an instruction by setting bit 29 of the instruction word ON to cause a reference to a properly loaded pointer register or by the use of indirect-to-segment (its) or indirect-to-pointer (itp) modification in an indirect word.

3.4.3.3.2 (Continued)

APPEND MODE

The append mode is the most commonly used main memory addressing mode. In append mode the final computer address is either combined with the procedure pointer register, or it is combined with one of the eight pointer registers. If bit 29 of the instruction word contains a (0), then the procedure pointer register is selected; otherwise, the pointer register given by bits 0-2 of the instruction word is selected.

BAR MODE

In BAR mode, the base address register (BAR) is used. The BAR contains an address bound and a base address. All computed addresses are relocated by adding the base address. The relocated address is combined with the procedure pointer register to form the virtual memory address. A program is kept within certain limits by subtracting the unrelocated computed address from the address bound. If the result is zero or negative, the relocated address is out of range, and a store fault occurs.

3.5 MPC CABINET

3.5.1 MPC Introduction

The Microprogrammed Peripheral Controller (MPC), is a freestanding unit that accesses and executes firmware microinstructions that are stored in a Read Only Memory (ROM) control store and a read/write main memory. The MPC is basically a general purpose microinstruction processor that is synchronized by a crystal-controlled clock. The MPC configuration panel provides the necessary controls to enable interconnection of the various options into the required operating device (i.e., disk controller, tape controller, URC, etc.).

3.5.2 MPC Description

The MPC is composed of the following units:

- Controller/Processor
- Link Adapter
- Controller Adapter
- Basic MPC

3.5.2.1 Controller/Processor

The controlling device in the MPC (Figure 3-6) is a controller/processor that receives and interprets commands from the IOM. The controller/processor is a firmware driven microinstruction handling device that receives instructions via the Peripheral Subsystem Interface (PSI) and responds to these instructions/commands by read/write operations on magnetic tape/disk devices or a URC.

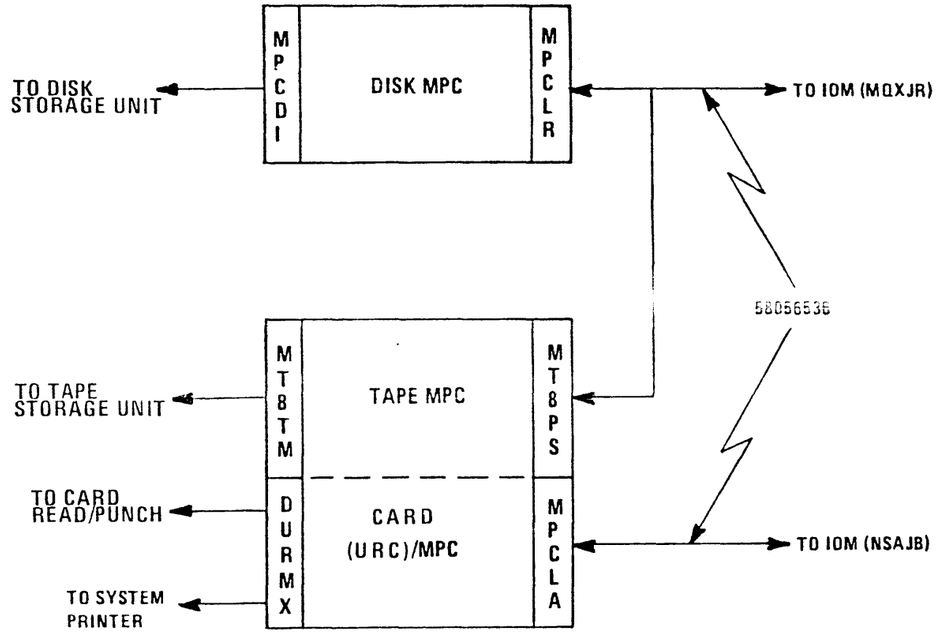


FIGURE 3-6 MPC CABINET INTERFACES

3.5.2.2 Link Adapter

The link adapter is a special purpose, dedicated (disk, tape, or unit record) logic board(s) that connects to the PSI to provide the communications link and data buffering between the MPC and the IOM. A special-purpose microprogram, processed by the MPC, drives the link adapter to initiate the MPC/IOM dialog for transfer of commands and data.

3.5.2.3 Controller Adapter

The controller adapter is a special-purpose, dedicated (disk, tape, or unit record) group of logic boards that provide the custom logic required to buffer data and enable control of the peripheral devices.

3.5.2.4 Basic MPC

The basic MPC is a general purpose microinstruction processor that controls the operation of one or two link adapters and one or two control adapters to access and execute microprograms.

3.5.3 MPC Functions

Requests for service and transaction commands are transmitted from the System Control Center to the MQXJK board in the IOM. In those instances, where the transaction commands involve access to data stored on magnetic tape, disk, or punched cards, the data access instruction portion of the transaction is relayed to the IOM channel boards (NSAJB/C/P,MQXJR). The data access instruction is then transmitted to the link adapter via the 58056536 peripheral device cable for processing by the controller/processor. The controller/processor makes the instructions available to the controller adapter (see MPC Unit Manual, 58009916 or 58009926, as applicable, for details).

When the data is read from the storage medium (disk, tape, cards, etc.), it follows the same path back to the IOM for processing by the central system computer in accordance with the specific transaction command.

In instances where the data is altered (payroll records, etc.) and transmitted back to the storage medium, the path is the same as for the read data operation in the previous paragraph.

If bulk data to be accessed is stored on disk, the disk drive transfers the data to the MPCDI board on the disk MPC. The data is outputted by the MPC through the MPCLR board and, via the 58056536 cable, to the channel boards mentioned in the previous paragraph.

If the data to be accessed is stored on tape, the tape drive will transfer the data, from tape to the MT8TM board on the tape/card MPC. If the data is stored on punched cards, the card equipment will transfer the data, via the Unit Record Controller (URC) to the DURMX board on the tape/card MPC. In either case, the MPC outputs the data through the MT8PS/MPCLA boards and, via the 58056536 cable, to the same channel boards used by the disk MPC.

If hard-copy printing on the system printer is part of the operator command or object program requirement, the IOM outputs the information to be printed through the channel boards to the tape/card MPC (MT8PS/MPCLA boards). The MPC outputs the data through the DURMX board, via the URC, to the system printer.

3.6 DPU CABINET

3.6.1 DPU Introduction

The Diagnostic Processor Unit (DPU) is a freestanding one-meter-tall unit designed to enable/augment automated fault isolation in the DPS 8 Computer System. The unit contains two diskette drives for software input to the DPU, two software interfaces, and an I/O terminal with CRT display (VIP).

The DPU is a Honeywell-owned maintenance tool which is supplied to the site as part of the maintenance contract. As such, the 58009927 Maintenance Operation Manual is an essential part of the DPU maintenance tool.

3.6.2 DPU Description

The basic DPU (Figure 3-7) (WDPU100A) contains the following:

- One MLC9103 Multiline Communications Processor (MLCP) which, in conjunction with the DCM9101 Dual Channel Communication Packs, provide the maintenance interface.
- Two DCM9101 Dual Channel Communication Packs which, in conjunction with the MLCP, provide four maintenance interface channels.
- Two DCF9101 Interconnecting Cables, 50 feet long, to connect the units under test to the MLCP.
- One W17-ØØ1C Direct Connection Cable, one foot long, used as a direct connect interface between the DMP on the unit under test and the DCF9101 cable.

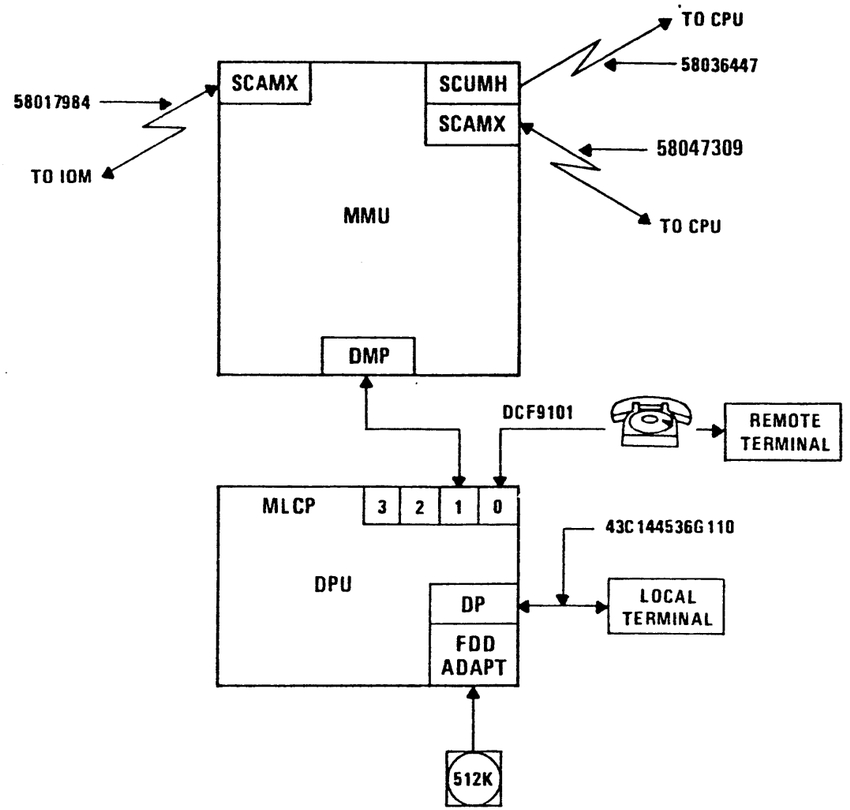


FIGURE 3-7. DPU CABINET INTERFACES

- One, 43C144536G110 Communications Cable, 10 feet long, which provides interface between a local terminal and the MLCP.

Additionally, the DPU incorporates two major software interfaces as follows:

- A control interface for the DPU I/O terminal (VIP) or the remote terminal at the TAC Center (via MODEM) for directing and monitoring of execution of the DPU through commands, messages, and prompts.

- A maintenance interface (the DMP's, MLCP, etc.) through which the input commands, output messages, and software prompts are transmitted during the fault isolation routines.

3.6.3 DPU Functions

When a maintenance problem arises in the central system computer, the DPU is connected to the Dynamic Maintenance Panel on a selected unit cabinet. Using local peripheral equipment and/or a MODEM, plus the necessary diagnostic software, fault isolation may be accomplished on a local or remote basis. See Figure 3-7 for a typical DPU connection to a unit under test. For detailed information on the DPU and maintenance procedures/diagnositc routines, refer to the appropriate manual listed in Figure 1-1.

Signals between the DPU and the Unit Under Test (UUT) consist of the software and operator-originated commands from the DPU and the responses from the UUT to the DPU.

The generalized, modular design of the software facilitates implementation of the DPU to meet the specific needs of any DPS-8 site. Specifically, the DPU software provides, as a minimum, the following services:

- Bootload control
- Configuration support
- Overlay management
- File structure creation and access control
- Memory allocation and management
- System console control
- Peripheral handling
- Loading, execution, suspension, and termination of application modules.

3.7 FNP CABINET

3.7.1 FNP Introduction

The DN66 Front-end Network Processor (FNP), Figure 3-8, is a freestanding unit that enables an entire two-way information network in any combination of local and remote locations to access the computer. In its function as a network enabling device, the FNP also handles the communications control responsibilities, leaving the computer free to process data.

3.7.2 FNP Description

The FNP is composed of the following:

- Processor
- Memory
- IOM
- I/O Linkage
- System Support Channel
- Cache Memory
- Multiline Communications Controllers

The IOM simplifies the FNP's task of providing real time, concurrent service to a variety of terminals by permitting input and output to operate in an interrupt driven fashion. Data can be accessed and processed (Processor) while other communications activities are being carried out.

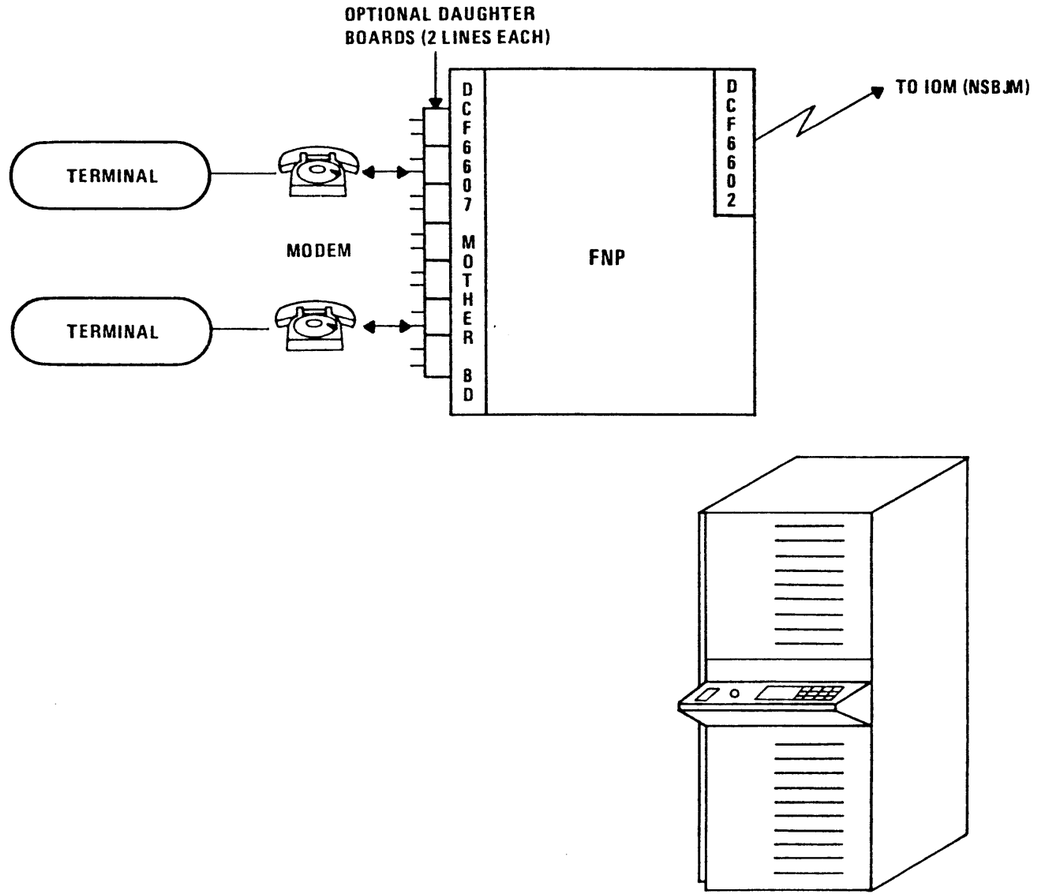


FIGURE 3-8. FNP CABINET INTERFACES

3.7.3 FNP Functions

If the system has network capability, operator commands will also originate at remote MODEM/terminal combinations. These commands to the computer, and the responses and data to the remote location, utilize the DCF6607 Mother Board on the DN66 Front-end Network Processor (FNP) and the optionally selected Daughter Boards.

The FNP outputs the signals through the DCF6602 board, via the 58056536 cable, to the NSBJM board in the IOM. All other operations and signals are handled as previously stated.

4.0 SYSTEM MAINTENANCE

4.1 MAINTENANCE INTRODUCTION

Maintenance and repair of the DPS 8 Low Profile System is governed by the Honeywell Distributed Maintenance Service (DMS) policy described in the Maintenance Operation Manual (58009927). Within the constraints of the DMS policy, system maintenance is divided into two separate categories: General Mainteance and Technical Maintenance. Within each are assigned tasks and responsibilities.

General maintenance is restricted to user responsible, periodic, preventive type tasks that are necessary to ensure the elimination of preventable job outages and equipment failures. The timeliness and completeness in performing these routines is critical to ensuring satisfactory operation of equipment and jobs. Examples of general maintenance tasks are:

1. Care and handling of diskette media.
2. Care and handling of disk packs.
3. Care and handling of magnetic tapes.
4. Cleaning equipment air filters.

Additional general maintenance tasks, if required, are identified within the applicable equipment until manual under the tab entitled "Maintenance Aids."

Technical maintenance encompasses all maintenance tasks that require the implementation of the numerous software tools available for detecting and localizing equipment or job failures. The various tools available allow the maintenance engineer to generate and collect data from either an on-site or remote location, while maintaining the equipment in the on-line or off-line mode of operation.

4.2 GENERAL MAINTENANCE

4.2.1 Care and Handling of Diskette Media

Proper handling and storage of a diskette will increase its life expectancy and reduce the possibility of errors. The following rules are the prerequisites for the proper operation of diskette media.

- Prior to inserting the diskette, visually examine its condition. The removable jacket should not be torn, folded or creased. Do not use a damaged diskette.
- Keep the diskette clean. Dust and dirt smudges, especially on the recording surfaces, can reduce the fidelity of reading or recording data.
- Do not write on the diskette jacket or label as writing pressure from a pencil or pen may damage the diskette. Annotate the label prior to adhering it to the diskette jacket. The use of felt tip pens are preferable to other writing instruments.
- Position labels carefully as to not obstruct the index sensing hole or adhere the diskette to its jacket.
- Do not smoke, eat or drink in the vicinity of diskettes.
- Do not bind diskettes using rubber bands, paper clips or any device that bends or creases the diskette jacket or protective envelope.
- Store diskettes in conditions similar to that of its normal operating environment. Recommended temperature and humidity ranges are:

  Termperature: $50^{o}F$–$115^{o}F$ ($10^{o}C$ to $46^{o}C$)
  Relative Humidity: 5%–90%

- Do not expose diskettes to direct sunlight or intense heat.

4.2.2 Care and Handling of Disk Packs

Proper handling and storage of disk packs is necessary to preclude errors in reading or writing of data. The following rules are prerequisite for the proper operation of the disk pack.

- Always maintain the disk pack within its own carrying case when not in use.
- Always reassemble the disk pack carrying case even though it may be empty.
- Never touch the disk pack recording surfaces.
- Do not expose the disk pack to magnetic fields, excessive pressure, or sharp blows.
- Store a disk pack flat, never on its edge.
- Never stack disk packs.
- Never expose a disk pack to direct sunlight or excessive heat.
- Always store a disk pack in conditions similar to that of its operating environment. Recommended temperature range is:

  Temperature: $60^{o}F–90^{o}F$ ($15^{o}C–32^{o}C$)

NOTE

If the temperature range is exceeded, maintain the disk pack at operating room levels for a minimum of two hours prior to using.

4.2.3 Care and Handling of Magnetic Tapes

To ensure the successful and error-free operation of magnetic tapes, a number of precautions must be observed. The following rules are prerequisite for proper magnetic tape handling and storage:

A. Keep tapes clean. Foreign matter on the recording surface will reduce the fidelity of the data signals. Observe the following precautions:

   - Never touch the recording surface with your fingers.
   - Maintain the tape within its dust-proof container until just prior to mounting it on the tape handler.
   - Keep the tape container clean, dust-free and closed.
   - Do not allow the tape end to touch the floor when loading the tape handler.
   - Do not erase identifying reel labels, change the label.
   - Do not smoke, drink or eat within the vicinity of magnetic tapes.
   - Always keep the tape transport window closed when not in use.

B. Handle and store tapes with care. Avoid damaging tapes and reels or placing tapes where temperature, dust, or magnetic fields affect them adversely by:

   - Exercise caution when rewinding tapes. Do not loosely or tightly wind tapes or damage will result. Wind tension for one-half inch tape should be 168-224 grams.
   - Do not crush or bend the tape leader when returning the tape to its case.
   - Avoid dropping tape reels. Never use a damaged reel.
   - Always store tapes in an upright position using clean, dust-free containers.

- Do not store tape reels on top of tape drive systems or heat exposure and dust contamination will result.

- Never store tape reels in the vicinity of magnetic fields.

- Always store tape reels in a controlled environment. Short term tape storage should include the following conditions:

  Temperature: 68°F–78°F (20°C–26°C)
  Relative Humidity: 40%–60%

  Long term storage should include the use of hermetically sealed and moisture proof containers.

- Handle tape reels by the reel hubs, not by the edges or flanges.

- Never apply pressure to the reel flanges when mounting the tape to the handler.

- Routine tape library inspections should be performed to identify and correct any faulty storage practices.

4.2.4 Cleaning Equipment Air Filters

Equipment air filters should be removed and cleaned, by vacuuming, on a periodic schedule prescribed in the pertinent unit manual. Where vacuuming is not feasible filter replacement will be necessary.

4.2.5 Care and Handling of Punch Cards

Punch cards are precision media. They must be handled with care and stored properly to protect the held information, ensure flawless operation and prevent damage to equipment. Recommended storage and handling procedures are as follows:

A. Storing Punch Cards

- Card decks that are retained for rerun should be kept under pressure to prevent curling, buckling, or bending. Cards in trays or open cartons should be pressure blocked. In open cartons, a piece of metal, wood, or folded cardboard can be used. For small decks, cardboard cut slightly larger than the cards can be used on each end of the deck and the deck bound with a rubber band.

- Store cards on edge, not flat.

- Maintain card within the following climatic conditions:

  Relative Humidity - 40-60 percent
  Temperature - 68-86°F (20-30°C)
  Air - Dust free

B. Handling Punch Cards

- Do not bend, fold, or otherwise damage cards.

- All card edges must remain smooth and free of burrs.

- Do not staple, clip or bend punch cards.

- Never allow cards to become containminated with grease, dirt or food.

- Keep unused cards pressure blocked.

4.3 TECHNICAL MAINTENANCE

4.3.1 Total On-Line Test System (TOLTS)

The Total On-Line Test System (TOLTS) fulfills the requirement of diagnosing minor equipment errors before they affect system operation, and to do so with minimum impact on the processing of user applications.

TOLTS runs in a multiprogramming environment, concurrently with other system and user programs on an optional basis. It performs periodic tests on the system components, and if it finds evidence of errors, calls in specific diagnostic tests and on-line troubleshooting programs to determine their nature. TOLTS also incorporates a remote testing facility that allows maintenance engineers to run tests and diagnostic programs from a remote terminal.

The Total On-Line Test System operates under GCOS supervision and is composed of the following modular subsystems:

SOLTS - System On-Line Test Subsystem

SOLTS provides the on-line capability of functionally testing a suspected faulty system processor. This capability provides a degree of confidence in that the processor under test is indeed operating properly.

COLTS - Communications On-Line Test Subsystem

COLTS provides the functional testing capability for the DN66 and DN8 Front-End Network Processor (FNP) and coupiers in an on-line environment. This capability allows equipment to be tested without the customer losing the use of the host system and aids in more effective scheduling and use of preventive maintenance time. COLTS is capable of testing either an entire FNP or any number of the eight available synchronous or asynchronous lines. In addition, COLTS possesses the capability to verify the integrity of the host/FNP link.

MOLTS - Mainframe On-Line Test Subsystem

MOLTS is comprised of microprograms that are intended to assit the field engineer in isolating failures in Microprogrammable Peripheral Controllers (MPC's) and MPC controlled peripherals. The microprograms are of two types: Isolation Test Routines (ITR's) and Microcoded Device Routines (MDR's).

The ITR's are microprograms that execute from the control store of the MPC and are used to isolate MPC failures. The MDR's also execute from the control store, but are used to isolate failures within the peripherals.

POLTS - Peripheral On-Line Test Subsystem

POLTS provides on-line capability to functionally test and troubleshoot peripheral devices without unduly interferring with the overall system capability of continued job processing. This capability allows the normally scheduled preventive maintenance time to be utilized more effectively in the acutal maintenance of equipment rather than running tests.

4.3.2 Honeywell Error Analysis and Logging Subsystem (HEALS)

The Honeywell Error Analysis and Logging Subsystem (HEALS) provides system monitoring and performance evaluation by operating "invisibly" alongside other software/hardware-detected error conditions, attempts to retry instructions for recovery from transient processor or memory faults, and issues warnings to the operator whenever the error rate of any hardware components approaches an abnormal rate. The intent of HEALS is twofold: (1) to enhance system availability and integrity, and (2) to ensure timely on-line testing and/or maintenance of marginal system components.

4.3.3 Visual Information Display for Efficient Operation (VIDEO)

The VIDEO program displays system-operating statistics on a large-screen video display. This facility allows operations personnel and interested users to monitor system performance on a minute-by-minute basis.

4.3.4 Statistical Collection File (SCF) and Summary Edit Program (GSEP)

The SCF is an on-line repository of operating-statistical records generated by all major system components. GSEP periodically complies and prints a statistical report summarizing the information contained in the current SCF. The GSEP report can be used to analyze and evaluate the effectiveness of past and current system-operation parameters and solftware/hardware configurations. In effect, the report constitutes a detailed history of system performance.

4.3.5 Auto II Field Subset

Field Auto II is a diskette based DPS 8, Models 52, 62 and 70 mainframe test system that is intended for implementation via a freestanding Diagnostic Processor Unit (DPU) subsystem. The test data is contained on a library of diskettes of which the contents may be identified through a control diskette. User versatility of fault localization is ensured by allowing full control of test execution and sequencing. Error displays that include command pairs, line numbers, WAS and SHOULD BE data, and compare masks are furnished the user to aid in fault localization.

4.3.6 Off-Line Test and Diagnostics

The off-line test and diagnostics system allows the user to test all mainframe hardware subsystems and associated peripherals. Normal software environment may be simulated by simultaneous execution of peripheral and mainframe diagnostic programs. A full complement of test program execution and control commands are provided to ensure versatility. Through interpretation of the diagnostic test results it is possible to detect and isolate failures that may occur within the DPS 8, Models 52, 62 and 70 systems.

4.3.7 Integrated Firmware and Diagnostics (IFAD)

The IFAD program has been developed to serve as a tool for better memory management and to provide accelerated system start-up. This has been accomplished by combining both the firmware and T&D (TOLTS) programs on a single IFAD tape, that may be accessed as required. Through the implementation of IFAD methodology, memory area normally required for storage of TOLTS programs is reduced, freeing needed memory to accomplish other tasks. This method of memory usage provides the operating system with a twofold advantage: (1) Elimination of the current requirement of loading the entire T&D contents prior to loading firmware, resulting in accelerated system start-up. (2) Superior memory management is achieved by maintaining not needed data on storage media rather than in memory.