HONEYWELL EDP

HARDWARE MANUAL

SERIES 200

TYPE 270 RANDOM ACCESS DRUM AND CONTROL

SUBJECT: Programming and Operating Procedures for the Type 270 Random Access Drum and Control

SPECIAL INSTRUCTIONS: This hardware manual completely supersedes the information bulletin of the same title (DSI-348) dated December 15, 1964.

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INTRODUCTION

The Type 270 Random Access Drum and Control is a storage device which provides high-speed access to large quantities of data for the Honeywell Series 200 Data Processing System. Up to eight drum units, each with a capacity of 2,621,440 alphanumeric characters, can be operated with a single control. Data is transferred between the central processor and the drum by any of five possible operations: Search and Read, Read, Search and Write, Write, and Read Address Register.

The drum control occupies one central processor drawer and requires two peripheral trunks (one for input and one for output). Each drum unit, with its power supplies and read/write logic rack, occupies a free-standing cabinet (see Figure 1-1).

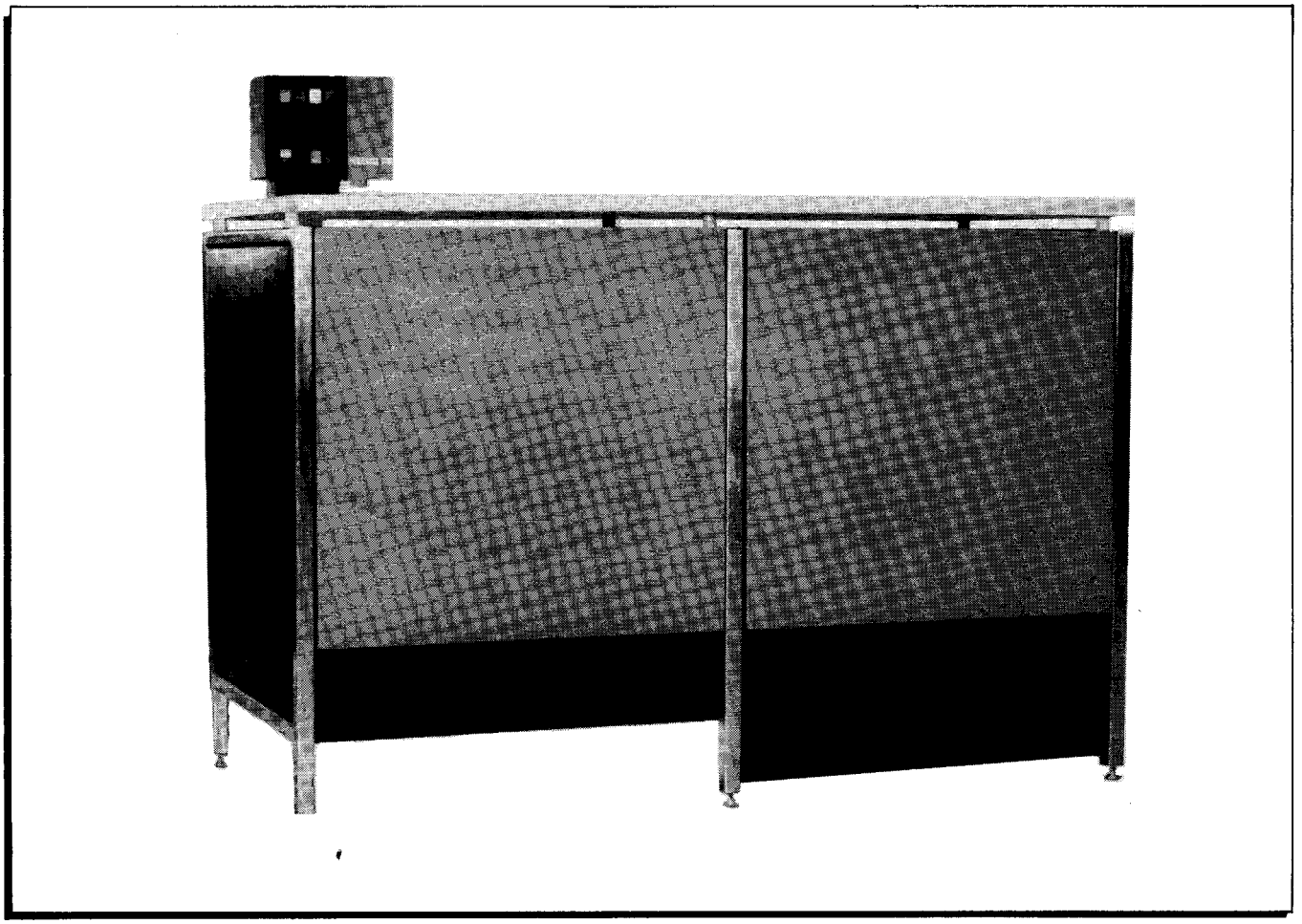


Figure 1-1. 270 Random Access Drum

DRUM FORMAT

The magnetic recording drum itself is 20 inches in diameter and 19.5 inches high. It rotates about its vertical axis at a nominal speed of 1,200 revolutions per minute. The magnetic surface of the drum is divided into 512 tracks (numbered 0-511). Each track, in turn, is divided into 40 sectors (numbered 0-39), as illustrated in Figure 1-2. A sector corresponds to a 128-character record. Each drum has a capacity of 20,480 single-sector records.

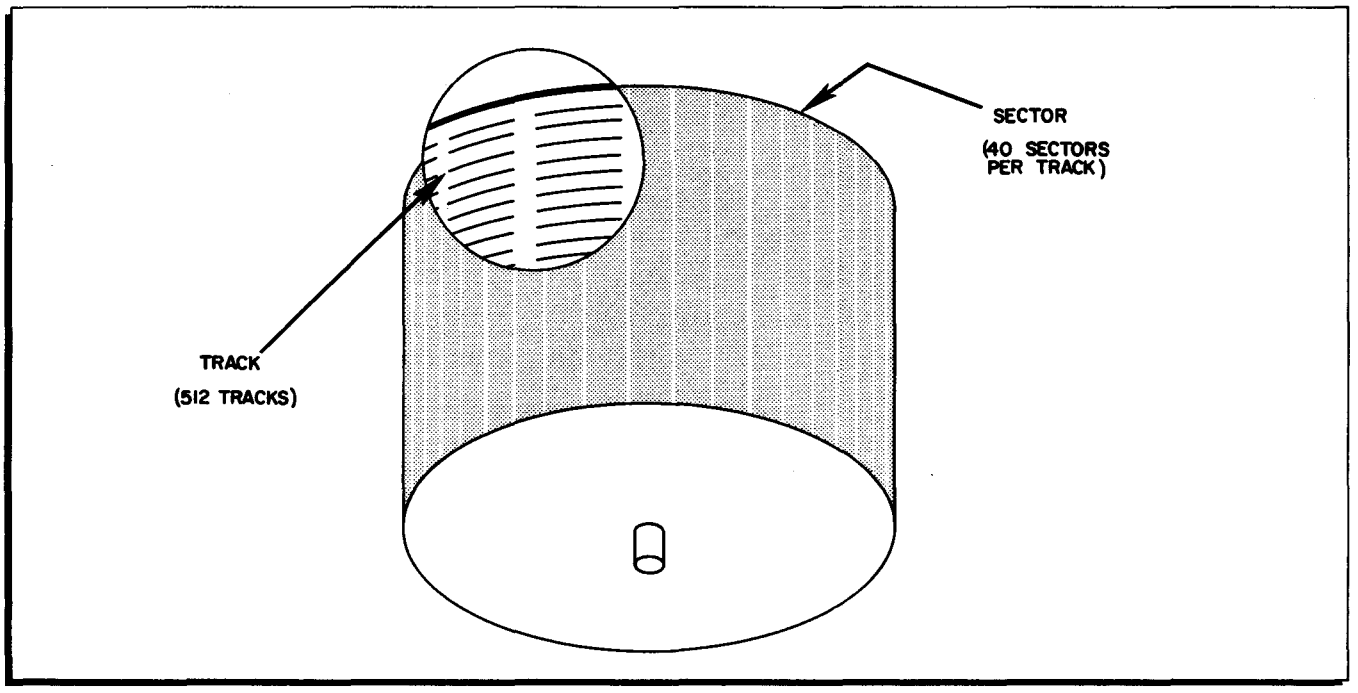


Figure 1-2. Magnetic Drum

In addition to the 512 information tracks, the drum also contains two tracks for the storage of control data. These control tracks are not accessible to the programmer. Data is transferred to and from the magnetic drum surface by 512 read/write heads, one for each information track. Control data is sensed by two control heads.

TIMING CONSIDERATIONS

For timing purposes, the 512 drum tracks can be considered to be divided into 128 zones of four tracks each. Within each zone, switching from track to track (head to head) is performed electronically within the 40-microsecond interval of the inter-sector gap. Between zones, however, switching is accomplished by relay selection and requires approximately five milliseconds.

During the five milliseconds required to switch between zones, the drum rotates past four sectors. To minimize sequential access time, the drum format is arranged with each zone

lagging the preceding one by four sectors. (For example, sector 0 of zone 1 is adjacent to sector 4 of zone 0, and sector 0 of zone 2 is adjacent to sector 4 of zone 1.) Thus, in sequential operation there is only a 40-microsecond gap between the sectors in a zone and a five-millisecond gap between zones (from sector 159 of one zone to sector 0 of the next).

The average latency (time required to locate a record on the drum) is 28 milliseconds, the maximum latency being 55 milliseconds (50 ms for one drum revolution and 5 ms for zone switching). Data is transferred between the drum and the central processor at an approximate rate of 102,000 characters/second. A single-sector record is transferred in approximately 1.20 milliseconds.

RECORD LENGTH AND TERMINATION

Although a record is considered to contain 128 characters and to occupy one sector, records of any size are easily accommodated. For a long record, an override feature permits the reading or writing of multiple-sector records. In this case, data is transferred to or from sectors sequentially within track N; then sector 39 on track N is followed by sector 0 on track N+1 (sector 39 on track 511 is followed by sector 0 on track 0). A record of less than 128 characters (or a multisector record which terminates in the middle of a sector) is filled with valid zeros by the drum control.

Data transfer is terminated either by sensing a record mark in memory or (when the override feature is not used) by the transfer of 128 characters, whichever comes first. The override feature is specified in the Peripheral Data Transfer instruction (see page 2-1). When a read operation is terminated by a record mark, the record-marked location receives the last character transferred, but the punctuation remains unchanged. When a write operation is terminated by a record mark, the record-marked character is not transferred. After a transfer has been terminated by a record mark, the drum address register contains the address of the last sector processed.

A bootstrap operation addressed to the drum automatically resets the Drum Address Register to track 0 sector 0 and transfers the 128 characters of data stored at track 0 sector 0 into the specified main memory locations.

SECTION II

OPERATIONAL DESCRIPTION

DATA TRANSFER OPERATIONS

There are five operations that transfer data between the drum and the central processor: Search and Read, Search and Write, Write, and Read Address Register. These operations are directed by Peripheral Data Transfer (PDT) instructions with the following format:

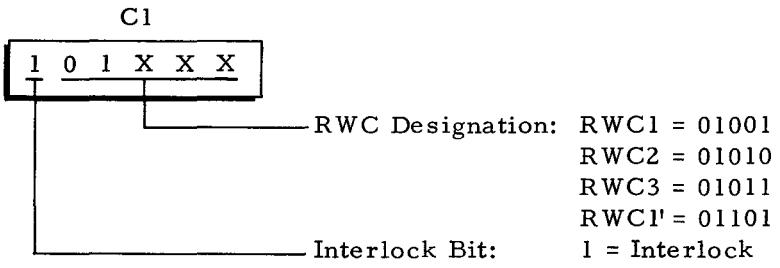
Search and Read, Search and Write

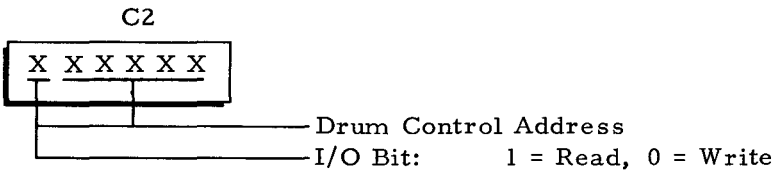
Op Code A Address, C1, C2, C3, C4, C5, C6

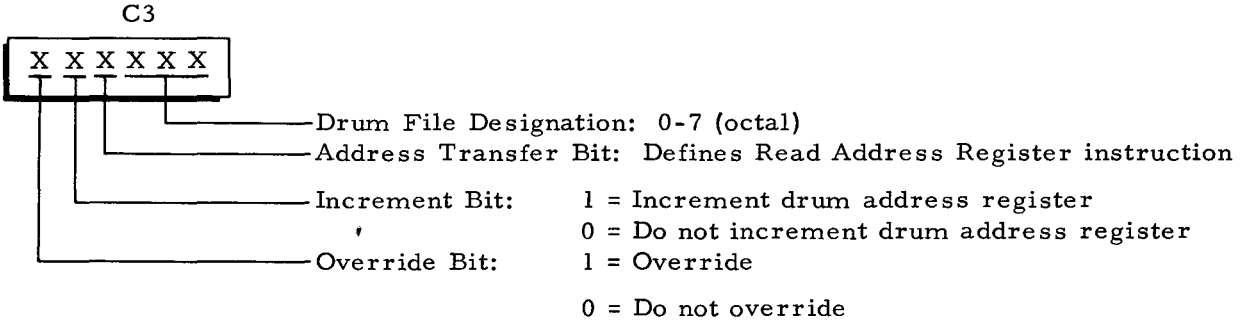
Read, Write, and Read Address Register

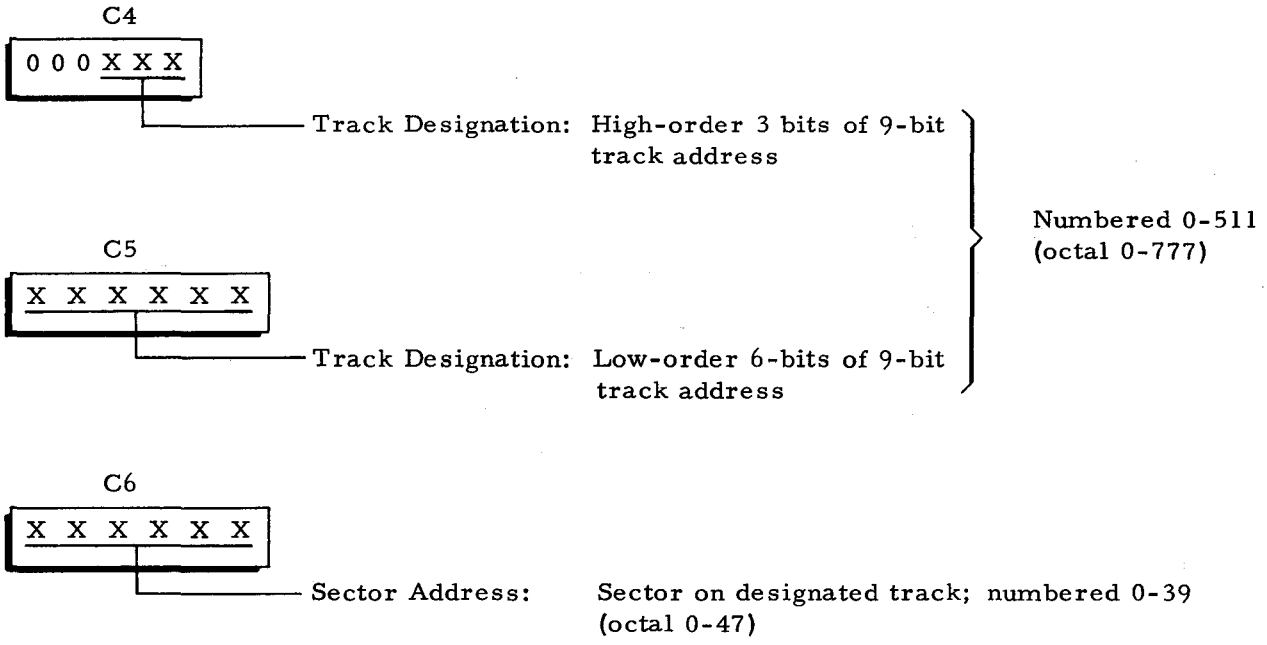
Op Code A Address, C1, C2, C3

The content and meaning of each of the six control characters are shown below. Since the instantaneous data transfer rate of the drum equipment is approximately one character every ten microseconds, the interlock bit in the PDT instruction must be "1" if RWC1 is designated.









Search and Read

A PDT instruction with six control characters and a one in the I/O bit position of C2 (see Table 2-1) initiates a search for the specified sector in the addressed track on the designated drum file. When the last character has been sent to the drum control, program sequencing continues. After the desired record is located (in 0-55 milliseconds), data is transferred, one character at a time, to consecutive memory locations starting with the location specified in the A-address field of the PDT instruction. Central processor activity is suspended for two microseconds for each character transferred.

If the override bit in control character C3 is a zero, data transfer continues until a record mark is sensed in memory or until one sector of information (128 characters) has been transferred. If the override bit is a one, data transfer terminates upon sensing a record mark in memory; in other words, reading can continue from sequential sectors of information without the necessity of issuing another instruction. In those cases where reading is terminated because a record mark has been sensed, the character containing the record mark is replaced by the last character transferred from the drum, but the punctuation is left unchanged.

The value of the address transfer bit in C3 must be zero in the search and read instruction. Since the contents of the drum address register are replaced by the contents of control characters C4, C5, and C6, the increment bit has no significance.

If the drum control receives a sector address higher than octal 47, it reduces this address modulo 32 (the high-order bit of C6 is made zero) and proceeds as described for a normal search and read operation.

Table 2-1. Drum PDT Control Characters

Function	C1	C2	C3	C4	C5	C6
Search and Read	101XXX	1XXXXX	XX0XXX	000XXX	XXXXXX	XXXXXX
Read	101XXX	1XXXXX	XX0XXX			
Search and Write	101XXX	0XXXXX	XX0XXX	000XXX	XXXXXX	XXXXXX
Write	101XXX	0XXXXX	XX0XXX			
Read Address Register	101XXX	1XXXXX	XX1XXX			
The underlined bits are those specifically mentioned in the text.						

Read

A PDT instruction with only three control characters and a one in the I/O bit position of C2 initiates a search on the designated drum file for the track and sector defined by the contents of the drum address register. The operation then proceeds as a search and read.

The value of the address transfer bit in C3 must be zero in the read instruction. The increment bit may be zero or one; if it is one, the contents of the drum address register are incremented by unity prior to starting the search. (The highest address, track 511 sector 39, increments to track 0 sector 0.)

Search and Write

A PDT instruction with six control characters and a zero in the I/O bit position of C2 initiates a search for the specified sector in the addressed track on the designated drum file. When the last control character has been sent to the drum control, program sequencing continues. Upon completion of the search (0-55 milliseconds), data is transferred to the drum, one character at a time, from consecutive memory locations starting with the location specified in the A-address field of the PDT instruction. Central processor activity is suspended for two microseconds for each character transferred.

If the override bit in control character C3 is a zero, data transfer continues until a record mark is sensed in memory or until one sector of information (128 characters) has been transferred. If the override bit is a one, data transfer does not terminate until a record mark is sensed in memory; in other words, writing can continue into the next sequential sector. In those cases where the writing process is terminated by record mark sensing, the character containing the record mark is not written on the drum. When writing is terminated before the end of a sector, the rest of the sector is filled with zeros.

The value of the address transfer bit in C3 must be zero in the search and write instruction. Since the contents of the drum address register are replaced by the contents of C4, C5, and C6, the increment bit has no significance.

If the drum control receives a sector address higher than octal 47, or an attempt is made to write on a protected file, a check condition results.

Write

A PDT instruction with only three control characters and a zero in the I/O bit position of C2 initiates a search on the designated drum file for the track and sector defined by the contents of the drum address register. The operation then proceeds as a search and write.

The value of the address transfer bit in C3 must be zero in the write instruction. The increment bit may be zero or one; if it is one, the contents of the drum address register are incremented by unity before starting the search. (The highest address, track 511 sector 39, increments to track 0 sector 0.) The following condition should be particularly noted. If the increment bit is one and the character position specified by the A-address contains a record mark, the only result is the incrementation of the drum address register; no data transfer takes place.

Read Address Register

A PDT instruction with three control characters (having a one in the I/O bit position of C2 and a one in the address transfer bit position of C3) defines a read address register instruction. When this instruction is issued, the contents of the drum address register are transferred to consecutive locations, starting with the location specified by the A address, in the following format:

A	A+1	A+2
000XXX	XXXXXX	XXXXXX
Track		Sector

The punctuation bits in these locations are not affected.

The override bit in control character C3 has no meaning in this instruction. The increment bit may be zero or one; if it is one, the contents of the drum address register are incremented by unity before transfer. Since the drum control contains only one drum address register, the device bits in C3 have no significance.

Data transfer is immediate. Aside from the time required to execute the instruction, only the time required to transfer three characters to the central processor is involved in the operation.

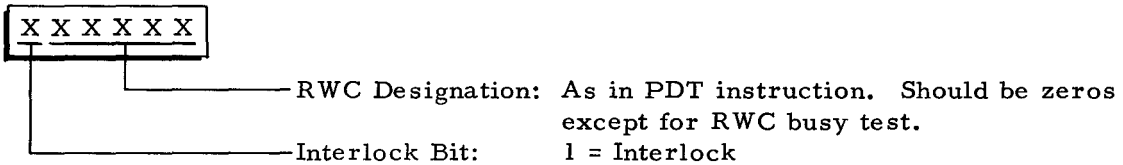
CONTROL AND TESTING

Three drum conditions can be program interrogated: Busy, Error Condition, and Interrupt On. There are three programmed commands that control the two functions used for interrupt operation: Turn OFF the Interrupt Allow, Turn ON the Interrupt Allow, and Turn OFF the Interrupt Signal. These queries and commands are performed by Peripheral Control and Branch (PCB) instructions with the following format:

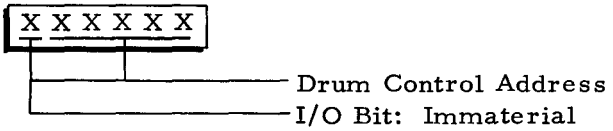
Op Code A Address, C1, C2, C3

The content and meaning of each of the three control characters are shown below:

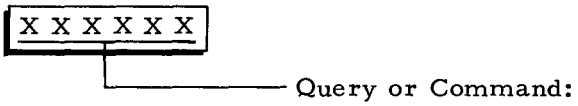
C1



C2



C3



00XXXX = Drum Control Busy Test: Branch to A address if the drum control is busy. The control is considered busy if a read or write operation is in progress on any attached drum unit.

100XXX = Drum Control Check Condition Test: Branch to A address if the error indicator is on. The error indicator is set by any of the check conditions defined below.

1111X1 = Interrupt Test: Branch to A address if the interrupt signal is on.

1110X0 = Turn OFF the Interrupt Allow.

1110X1 = Turn ON the Interrupt Allow.

1111X0 = Turn OFF the Interrupt Signal.

The following points should be noted:

1. Unless a test is being performed for RWC busy, the value of the RWC bits in C1 should be zero. (If C1 contains the octal value 77, a branch to the A address will occur unconditionally after all control characters have been sent to the drum control.)
2. When RWC1 is assigned, or to be assigned, to the drum control in a system having four RWC's, the interlock bit in the RWC busy test should be one to test the availability of the interlocked pair (RWC1 and RWC1 '). In systems having less than four RWC's the PCB interlock bit has no effect.
3. Since the drum control does not permit reading from one drum file while writing on another, the drum control is considered busy if either a read or a write operation is in progress. The value of the I/O bit in C2 is therefore immaterial in this case.

CHECKING

Any of the following conditions will set the error indicator. It remains set until cleared by the PCB error test operation.

Data Check

When writing, the control unit generates cyclic coding and appends two check characters to each record. These characters are used for checking data when reading the drum, and will cause a check condition in the event of error. This check detects all single, double, or triple errors, any odd number of errors, all burst errors of 12 bits or less, 99.9512% of all 13 bit burst errors, and 99.9756% of all burst errors of 14 or more bits.

Write Check

Any attempt to write on a protected drum results in a write check, and the write operation ceases immediately.

Sector Address Check

When a sector address greater than octal 47 is specified in a Write instruction, a check condition results and the write operation ceases immediately.

INTERRUPT OPERATION

In interrupt operation, foreground and background programs are alternated to allow full use of central processor time, which would otherwise be wasted during relatively slow data transfer operations. When the foreground program issues a PDT, central processor time is allocated to the background program until the PDT is completely executed. The drum then sends an interrupt signal to the central processor, which returns control to the foreground program.

An Interrupt Allow function is included to act as a switch to enable or inhibit interrupt operation. The Interrupt Allow can be turned ON (C3 = 71) or OFF (C3 = 70) by issuing a PCB. Initializing the central processor automatically turns the Interrupt Allow OFF.

When the Interrupt Allow is ON and the drum control unit is not busy, a continuous interrupt signal is sent to the central processor. Any PDT to the drum control turns off the interrupt signal until the PDT has been executed, at which time the drum control again sends an interrupt signal.

PCB's can be issued to test for (C3 = 75) or turn off (C3 = 74) the interrupt signal. Setting the Interrupt Allow to OFF turns off and inhibits the interrupt signal.

SECTION III

CONTROLS AND INDICATORS

The control panel for the drum is located atop each drum unit. The control panel (see Figure 3-1) contains four sets of switches and three indicators, as described below. In addition, the AC drawer of each drum unit contains the main AC circuit breaker for the unit.

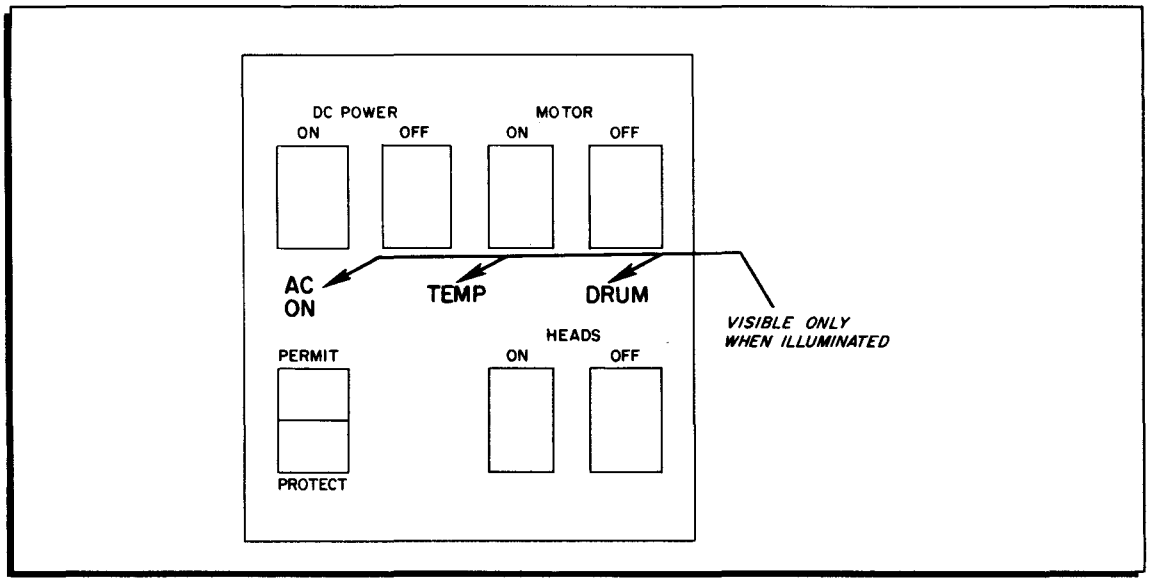


Figure 3-1. Control Panel for Type 270 Random Access Drum Unit

DC POWER	Energizes DC power for the read-write circuitry. The ON switch is illuminated when DC power is on. An interlock inhibits the DC POWER ON switch, when the MOTOR switch is ON, and the DC POWER OFF switch, when the HEADS switch is ON.
MOTOR	Energizes the drum motor. The ON switch is illuminated when power is applied to the drum motor. The OFF switch is not interlocked but should not be pushed when the HEADS switch is ON. The heads should be turned off before the drum motor; the results of doing otherwise are unspecified.
HEADS	Positions and activates the read/write heads. The ON switch is illuminated when the heads are activated and the OFF switch is illuminated when the heads are deactivated. The head circuitry is interlocked so that it can be activated only when the drum is up to speed. When the ON switch is pressed, the OFF indicator is immediately extinguished. After a short delay, the ON indicator lights if the drum is up to speed. The drum is then ready to operate with the central processor.

PERMIT-PROTECT	Permits or inhibits writing on the drum. This alternate position switch is illuminated either at the top or bottom to indicate which mode is selected. The permit mode allows the program to write on the drum. The protect mode prevents any writing; the drum appears busy if a write instruction is attempted. This switch is not interlocked; if it is changed during operation, the effect is unspecified.
AC ON (Indicator)	This green indicator is illuminated whenever the drum unit main AC circuit breaker is ON. The indicator is visible only when illuminated.
TEMP (Indicator)	This red indicator is illuminated when a predetermined high-temperature limit is reached in the drum unit. The heads and drum motor are automatically turned off and the error indicator is set.
DRUM (Indicator)	This red indicator is illuminated whenever a malfunction occurs in the unit. The drum in this case will appear in error to the central processor.

SECTION IV

OPERATING PROCEDURES

The AC circuit breaker, located on the AC drawer under the rear cover, serves as the primary power shut-off for the drum unit. During stand-by periods, i.e., when the drum is rotating but is not in use, the heads should be in the OFF position. The cabinet cooling fans are operating and the AC ON indicator is illuminated whenever AC power is applied. Whenever the DRUM indicator is lit, the drum will appear to be in error to the central processor.

Starting Procedure

1. Turn on AC power with circuit breaker. AC ON, DRUM, and HEADS OFF indicators should light. All others should be off, except PERMIT/PROTECT the setting of which is optional.
2. Press the DC POWER ON switch, which should light immediately.
3. Press the MOTOR ON switch, which should light immediately. The DRUM indicator will be extinguished at this time unless some malfunction is sensed. Wait 3 minutes for the drum to reach proper operating speed before proceeding to step 4.
4. Press the HEADS ON switch. If the drum is up to speed, the HEADS OFF indicator will immediately be extinguished. After a slight delay, the HEADS ON indicator will light. If drum speed is incorrect, the DRUM indicator will light at this time.

Stopping Procedure

1. Press the HEADS OFF switch. The HEADS ON indicator will be extinguished and the HEADS OFF indicator will light, indicating that the heads are de-activated.
2. Press DC POWER OFF and MOTOR OFF. The sequence of these operations is unimportant, but they should not be performed until the HEADS OFF indicator is lit. The drum is now in a cycle-down condition.
3. To completely remove power from the unit, remove the rear panel of the electronics cabinet and turn off the AC circuit breaker.

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USERS' REMARKS FORM

TITLE: Type 270 Random Access Drum and Control

DATED: October 26, 1965

FILE NO: 113.0005.1300.0-009

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SUGGESTIONS FOR IMPROVEMENT:

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