HARDWARE BULLETIN

SERIES 200

TYPE 286-1, -2, -3
MULTI-CHANNEL CCU

SUBJECT: Equipment Specifications for the Types 286-1, -2 and -3 Multi-Channel Communication Controls, including Features 086 and 087.

SPECIAL INSTRUCTIONS: This bulletin supersedes the Customer Information Bulletin 200-31, dated October 23, 1964, which dealt with the discontinued Type 284 Multi-Channel Communication Control. It will, in turn, be superseded by more detailed programming and operating procedures in forthcoming publications.

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EQUIPMENT SPECIFICATIONS FOR THE TYPES 286-1, -2, AND -3 MULTI-CHANNEL COMMUNICATION CONTROLS, INCLUDING FEATURES 086 AND 087

I. BASIC DEFINITION

The Type 286-1, -2 and -3 Multi-Channel Communication Controls provide interconnection of a Series 200 central processor with a maximum of 63 half-duplex communication lines by way of Type 285 Communication Adapter Units, as shown in Figure 1, below. The communication controls operate on the standard Series 200 central processor peripheral bus.

Basically, a Type 286 Multi-Channel Communication Control provides the timing, control, and interface logic required by a particular communication line/remote terminal configuration.

The Type 286-1, -2 or -3 occupies one standard Series 200 logic drawer.

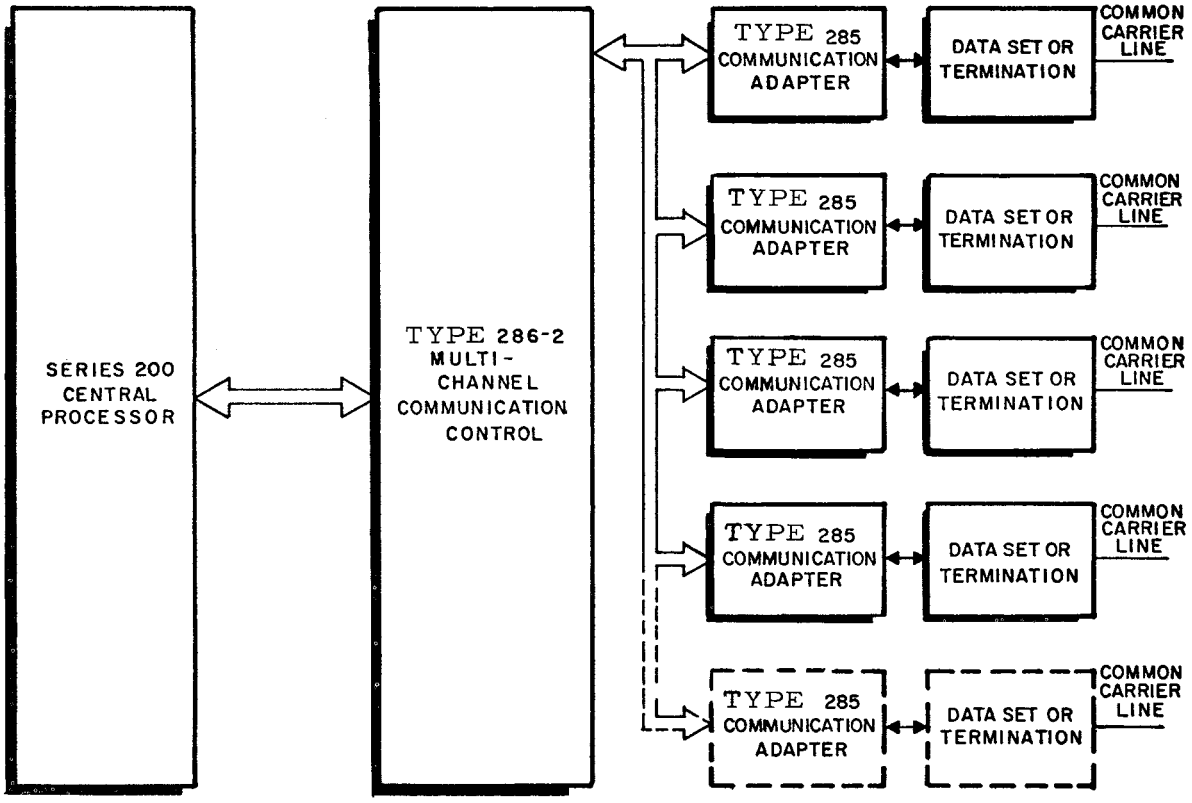

Figure 1. Type 286-2 Application

II. FUNCTIONAL DESCRIPTION

The Type 286-1, -2 or -3 Multi-Channel Communication Control performs numerous functions. It provides buffer storage, assembles into characters all bits received from a line via the Type 285 Communication Adapter Unit, serializes characters received from the central processor for Type 285 transmission, scans the Type 285 for activity, and generates and sends interrupt signals to the central processor when a character is to be transferred. Also, when equipped with optional Feature 086, the Type 286 provides character parity, and with Feature 087 it provides the Longitudinal Redundancy Check (LRC). These features are described in Sections VI, I and H, respectively.

One Type 285 Communication Adapter Unit is required for each half-duplex communication line serviced by the Type 286 Multi-Channel Communication Control; each Type 285 constitutes at least one line address.

The three Type 286's provide for expansion of communication lines serviced in the following manner:

TYPE	NUMBER OF HALF-DUPLEX LINES SERVICED
286-1	2-3
286-2	4-15
286-3	16-63

III. INTERFACE WITH SERIES 200 CENTRAL PROCESSORS

Standard peripheral interface logic for non-simultaneous input and output connects the Types 286-1, -2 and -3 to the standard Series 200 peripheral bus.

IV. INTERFACE WITH TYPE 285 COMMUNICATION ADAPTER UNITS

The Type 286 Multi-Channel Communication Control, equipped with a group of Series 200 interface packages, connects to a Type 285 by way of miniature coaxial cables. All signals are at the voltage level of ground or +5 vdc, nominal. Table I lists the interconnecting lines for each adapter unit used.

Table I. Connecting Cables

Lines	Description
DATA	
1 - Type 286 to Type 285	Information out (serial by bit)
1 - Type 286 from Type 285	Information in (serial by bit)
ADDRESS	
6 - Type 286 to Type 285	Select a particular Type 285
REQUEST	
1 - Type 286 from Type 285	Type 285 requests a bit from Type 286
1 - Type 286 from Type 285	Type 285 requests Type 286 take a bit
TIMING	
1 - Type 286 to Type 285	Bit ready on data-out line
1 - Type 286 to Type 285	Bit received on data-in line
RESET	
1 - Type 286 to Type 285	Reset by INITIALIZE push button on central processor control panel
SPECIAL STROBE	
1 - Type 286 to Type 285	Control information to the Type 285

V. MULTI-LINE OPERATION

A. Priority

No line priority condition exists in the Type 286. To prevent loss of data, an interrupt grants any given line central processor access at least once per character-time. A limitation is imposed upon the number and speed of lines controlled. The limitation on number of lines is a function only of those of highest speed. The following expression determines the number of lines that can be serviced simultaneously when the system includes a variety of line speeds:

$$n \leq \frac{Tc}{Ti} + 1,$$

where

n is the number of connected lines in use;

Tc is the character period (in microseconds) of the highest speed line utilized in the system;

Ti is the length (in microseconds) of the interrupt servicing routine.

Note: This expression is based on the assumption that no other peripheral unit is causing interrupts.

B. Line Scanning

For the purpose of scanning, the communication lines serviced by the Type 286's are classified as follows:

Fast lines — The bit-time is greater than 400 microseconds and less than 4 milliseconds (2500-250 baud);

Slow lines — The bit-time is greater than 4 milliseconds (250 baud).

Within the Type 286, the scanning operation is controlled by two counters. The fast counter (F) scans lines 1_8 - 17_8 at three times the scan rate of the slow counter (S), which scans lines 20_8 - 77_8. The sequence of scanning is FFFSFFFS

VI. PROGRAM REFERENCE DATA

A. Type 286 Multi-Channel Communication Control Memory

The Type 286 magnetic core memory contains 256 eight-bit word locations. Four locations, providing storage and control, are assigned to each of the 63 lines serviced. The remaining four words — assigned are imaginary "line zero" address — are used for line scanning and line address storage.

1. Storage and Control for Lines 1-63

The four 8-bit words assigned to each line perform the following functions:

Word 1 - buffer register,

Word 2 - shift register,

Word 3 - LRC character storage.

Word 4, the control word, functions as follows:

Bits 1-3 — This three-bit register counts the bits of a character;

Bit 4 — Bit 4 creates start-stop coding or, on a bit-stream synchronous line, it indicates that synchronization has been attained;

Bits 5-6 — These two bits identify the receive or transmit state, or recognize that a "Transmit Last Character" PDT instruction or an "Inhibit" PDT instruction has been addressed to the line.

Bits 7-8 — These contain line status information; they designate odd or even parity, an overwrite condition, and call bit.

The call bit is used to test the availability of the line - zero register. It is reset when the mandatory PDT instruction is executed.

The overwrite condition is set if data is not removed from the buffer register and if it is overwritten by the next incoming character. The overwrite condition is reset only when the bit is transferred to the line-zero register. The overwrite bit acts in the same manner, when set, as does a call bit.

2. Line Zero — Scanning and Line Address Storage

The four 8-bit words assigned to the line-zero address function as follows:

Words 1-2 — Fast and slow counters to control line scanning;

Word 3 — Storage for the address and status (transmit, odd or no parity, even parity, overwrite error) of the line requesting service.

Word 4 — Not used at present.

B. Data Control

Single line characters are transferred (six bits in parallel, as two central processor characters) between the central processor and a Type 286 buffer register by means of appropriate PDT instructions.

Within the Type 286, data are handled as single line characters. During transmission, a buffer register line character is transferred in parallel to a shift register, then transferred serially by bit to the associated Type 285 Communication Adapter Unit. The receiving Type 285 transfers such bits, received serially, to the Type 286 shift register for that line. When the character is assembled, it is transferred in parallel to the associated buffer register and the Type 286 makes a call for service.

If Feature 087 (the LRC Option) is present, each character transferred into a buffer register or out of it by a "Sending" or "Receiving Data" PDT instruction is half-added to the present contents of the associated LRC register.

C. Interrupt

The Type 286 interrupt signal indicates that the line whose address and status is currently stored in the Type 286 buffer register of line zero is requesting service. The interrupt signal is reset by a PDT instruction addressed to line zero or by depression of INITIALIZE on the central processor control panel.

Though — in the "initialize" condition — its clock is still running, the Type 286 is neither transmitting data to the Type 285's nor receiving data from them; a "Set Allow" PCB instruction must be sent to allow interrupts to occur so the servicing of the Type 285's may begin.

To service each interrupt properly, a PDT instruction sequence is executed in two steps, as follows:

1. A PDT instruction is sent to line zero to obtain the address of the requesting Type 285;
2. A PDT instruction is issued to move the data or modify the control word.

While sending a "Reset Allow" PCB instruction inhibits any subsequent interrupts, it does not prevent the Type 286 Multi-Channel Communication Control from scanning, servicing lines or starting new interrupts. A "Reset Allow" PCB instruction followed by a "Set Allow" PCB instruction can result in an immediate interrupt.

D. Peripheral Control and Branch (PCB) Instructions

1. Format

Format for the PCB instructions used with the Type 286 is shown in Figure 2, page 5. Listed below the figure is a definition of the information contained in each control character. The PCB instruction initiates the control and testing of the Type 286 Multi-Channel Communication Control.

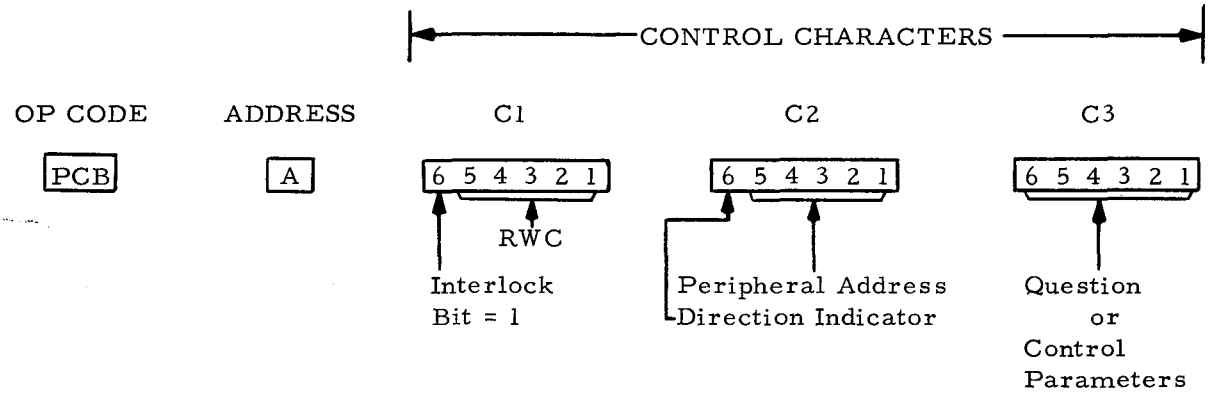

Figure 2. PCB Instruction Format

PCB -

A Address - The memory location to which the program will branch, in a branching PCB, instruction if the condition tested for by the PCB instruction is true.

Interlock Bit - Not interpreted.

Read/Write Channel - This selects the read/write channel (RWC) between main memory and the peripheral control unit. The low-order five bits of C1 contain the number of the RWC being tested for availability and must be set to zero if no RWC is to be tested. The following binary configuration is used for the RWC listed.

RWC1 = 01001 RWC3 = 01011

RWC2 = 01010 RWC1' = 01101

Direction Indicator - Not interpreted.

Peripheral Address - This is the logical address of the control unit on the peripheral bus.

Control Parameters (C3) - The C3 character of the PCB instruction provides questions and control. Multiple queries or actions can be implemented by the use of additional control characters.

2. Control and Test Functions

The three main control and test operations, plus their associated octal code, are listed in Table II, page 6.

Table II. PCB Instructions

Instruction	Function	C3 Octal Code
Set Allow	Sets Allow in the Type 286 to permit program interrupts when a line requests service.	71
Reset Allow	Resets Allow to prevent future interrupts from the Type 286 and allows the Resume Normal Mode instruction (RNM) to be effective in the central processor.	70
Interrupt	Tests the Type 286 for an interrupt-initiated condition. If "yes", the program branches to the A-address of the PCB instruction. If "no", the program continues normal sequence.	75
*Busy	Tests the Type 286 for a busy condition. If "yes", the program branches to the A address of the PCB instruction. If "no", the program continues normal sequence.	10

*The PCB Busy test is not normally used with the Type 286. The 286 is only busy after a PDT instruction for a maximum of 15 memory cycles. If the PCB Busy is executed when the 286 is not busy, the scanner in the 286 stops when the varient character indicating the Busy test is sent to the 286 and remains stopped until the termination of the PCB instruction.

E. Peripheral Data Transfer (PDT) Instructions

1. Format

General format for the PDT instruction used with the Type 286 is illustrated in Figure 3, page 6. Listed below the figure is a description of each character group and its associated function.

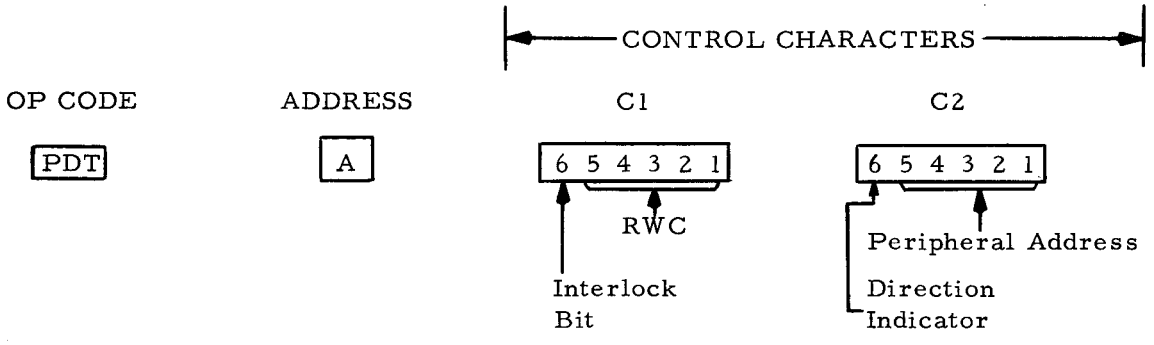

Figure 3. PDT Instruction Format

PDT

A Address - This specifies the leftmost character of a three-character data field used by the PDT instruction.

Interlock Bit - 1 = Memory access is not granted to RWC1'

0 = Memory access is granted to RWC1'

Read/Write Channel (RWC) - This selects the RWC between main memory and the Type 286.

RWC1 = 01001 RWC3 = 01011

RWC2 = 01010 RWC1' = 01101

Direction Indicator - This indicates the direction of data transfer:

0 = OUTPUT 1 = INPUT

Peripheral Address - This is the logical address of the control unit on the peripheral bus.

The PDT instruction is used to initiate data transfer between main memory and peripheral devices controlled by the Type 286. This PDT instruction is addressed to the Type 286 by the C2 control character and to a particular communication line by means of the three-character data field specified by the A address. Location A — the first character of the data field — specifies a particular line in the Type 286; locations A+1 and A+2 contain the transferred character.

All PDT instructions addressing the Type 286 come under one of two classifications: They are either Data Transfer or Control PDT instructions.

2. Data Transfer PDT's

a. Receiving the address and status of the requesting line.

A "Receive" PDT instruction, addressed to the Type 286 line zero, causes the stored line address (bits L) of the line requesting service to be placed in main memory location A+2 and the line status (bits 5) to be placed in location A+1. Figure 4, page 7, illustrates this format. The Type 286 places zeros in all unused bit positions of location A+1.

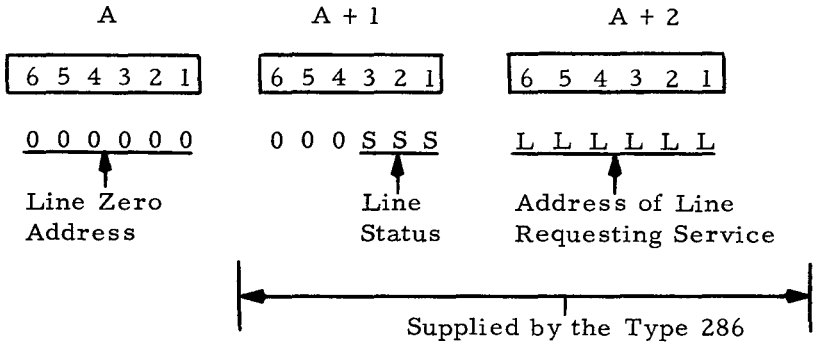

Figure 4. Address and Status Format of "Line Zero" PDT Instruction

The Line Status bits (S) are coded according to the state of the associated Type 285 adapter unit.

000 Indicates receive state and that the character has odd parity if Feature 086, the Parity Option, is present, or that the parity option is not present.

010 Indicates receive state and that an overwrite error has occurred. The CP failed to empty the line buffer register before a new character or characters had been assembled from the line. The character received along with the overwrite error is not predictable.

001 Indicates receive state and that the character has even parity.

011 Indicates transmit state.

111 Indicates duplicate transmission error — this is applicable to synchronous lines only.

This error indicates that a new character was not received in time from the central processor and that the previous character was retransmitted (the number of retransmissions is not predictable).

Start/stop lines wait for the next character from the central processor but they remain in the transmit state.

b. Receiving Data

A "Receive" PDT instruction with the A data-field format shown in Figure 5, page 8 is issued by the Type 286 in response to request for service when data is ready for transfer to the computer.

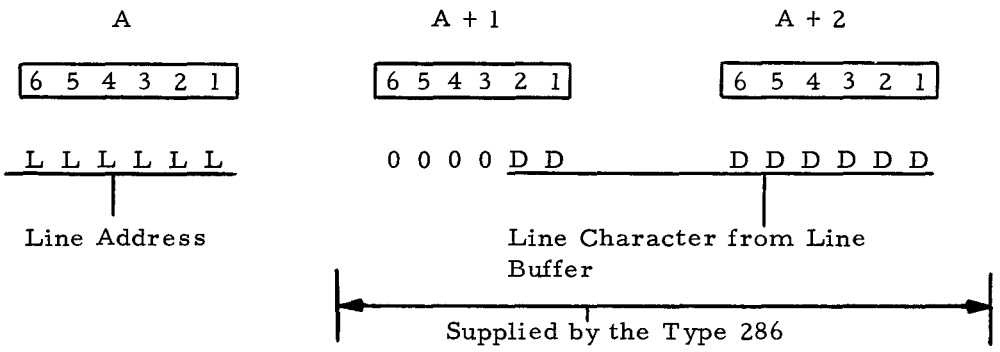

Figure 5. Address and Data Field Format ("Receive" PDT Instruction)

For all line addresses except zero, a line data character (D) is then transferred from the line buffer register to the main memory. The low-order six data bits are placed in A + 2 and the high-order two bits (if any) are placed in A + 1. Zeros are placed in all unused bit positions of A + 1 and A + 2 by the Type 286.

c. Sending Data

A "Send" PDT instruction having the A data-field format shown in Figure 6, page 8, transfers a data character from memory to the buffer register of the addressed line.

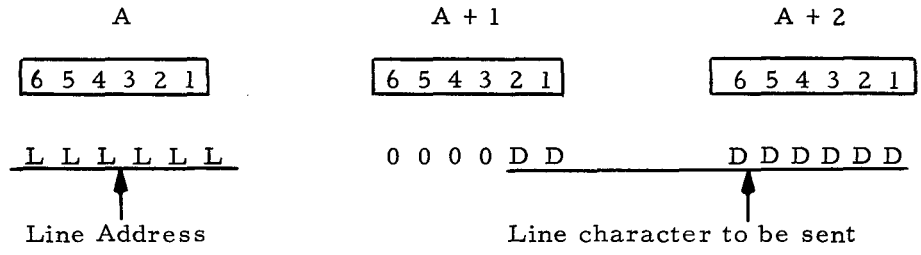

Figure 6. Address and Data Field Format ("Send" PDT Instruction)

This PDT instruction is used to load a line buffer register when initiating a program decision or responding to a line request for service. In response to a request from a line in the transmit state (line buffer register empty), the address of that line is first obtained by issuing a PDT instruction addressed to line zero.

3. Control PDT Instructions

Control PDT instructions have the same general format as do the Data Transfer PDT instructions. Control PDT instructions, except "Special Strobe" and "Move LRC," modify the control word of the line addressed in location A by means of control codes placed in location A+1. The Type 286 does not interpret location A+2.

The A data field of a Control PDT instruction is shown in Figure 7, page 9.

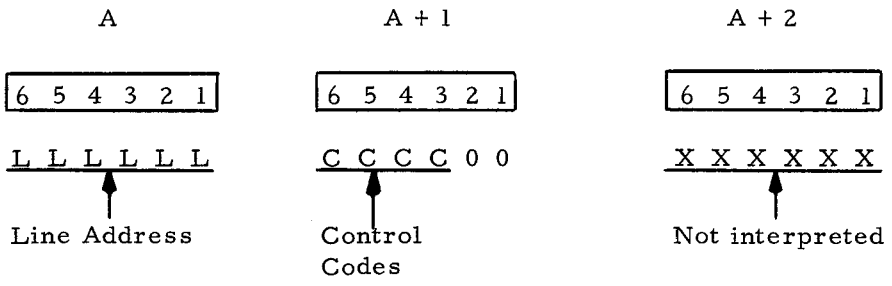

Figure 7. Address and Control Field Format (Control PDT)

Control PDT instructions require the same amount of execution time as normal "Receive" PDT instructions and "Send" PDT instructions. Table III, pages 9 and 10, summarizes control PDT instructions.

Table III. Summary of Control PDT Instructions

INSTRUCTION	DESCRIPTION	A + 1
Receive Clear	The "Receive Clear" PDT instruction resets the control word and shift register bits of the addressed line in the Type 286. This PDT instruction must be addressed to each line; including those not associated with a Type 285 Adapter Unit, after power is initially applied and prior to the execution of an "Allow" PCB instruction. In bit-stream synchronous operation, a "Receive Clear" PDT instruction may have to be executed after a message or block of data has been received to reset the line control word. This enables the unit to resynchronize itself to the line when the next bit stream is received. (Refer to applicable 285 Adapter Unit bulletin.)	110000
Transmit	The "Transmit" PDT instruction, under normal operating conditions (data set ready, etc.),	100000

Table III (cont). Summary of Control PDT Instructions

INSTRUCTION	DESCRIPTION	A + 1
Transmit (cont)	enables the timing of the associated Type 285. When the timing is enabled, the character in the buffer register is transferred to the line shift register, and the request for service from this line is enabled when required. This PDT instruction is executed, in general, from the noninterrupt portion of the program. The LRC register, if the option is included, is not affected by this PDT instruction. If "Transmit" PDT instruction is executed following a "Transmit Last Character" PDT instruction, the control unit will continue to transmit, and the new character in the buffer register will follow, in time, the original last character.	
Transmit Last Character	The "Transmit Last Character" PDT informs the Type 286 unit that the last character, because of a previous interrupt, has been sent from the central processor. This PDT instruction resets the control word, after the character in the line shift register is transmitted. The line reverts back to the receive state, preventing a further request for data. The "Transmit Last Character" PDT instruction can be issued while the Type 285 Adapter Unit is in the receive state. The character in the buffer register is then transferred to the shift register and in turn, transmitted to the line. Only this character will be transmitted, and no interrupt will be generated. The control word returns to the receive state after the character is transmitted.	001000
Transmit Idle Character	The "Transmit Idle Character" PDT instruction continuously transmits a previously provided character without interrupts until the state of the control unit is altered by another "Control" PDT instruction. The request for service from the line is not enabled. This PDT instruction is effective only on synchronous lines. When the PDT instruction is received it enables the timing of the associated Type 285 Adapter Unit, which causes the single character placed in the buffer register by a "Send Data" PDT instruction to be transferred to the shift register and repeatedly transmitted to the line.	101000
Inhibit 285 Unit	The Type 285 "Inhibit" PDT instruction inhibits the interrupt capability of a line that is requesting service, either transmitting or receiving. The control word for that line is set into the receive state and no further interrupts are permitted from that line. Any transmission in progress is	011000

Table III (cont). Summary of Control PDT Instruction

INSTRUCTION	DESCRIPTION	A + 1
Inhibit 285 Unit (cont)	immediately halted. The inhibit condition is cleared by one of the following Control PDT instructions. "Receive Clear;" "Transmit;" "Transmit Last Character;" and, only on synchronous lines, "Transmit Idle Characters".	
Move LRC	The Move LRC PDT instruction transfers the contents of an LRC register to the associated buffer register and resets to zero the LRC register. The line control word is not affected.	111100
Special Strobe	The "Special Strobe" PDT instruction activates the special strobe line to a Type 285 via the Type 286. This signal is interpreted according to the type and state of the Type 285 (reference the individual 285 bulletin).	011100

F. Procedures for Controlling the Action of a Communication Line

The following procedures are used to control line action after all lines have been issued a "Receive Clear" PDT instruction and the allow condition is set in the Type 286.

1. Start Transmission

A normal "Send Data" PDT instruction addressed to the desired line is executed to transfer the first character to the buffer register. When sufficient time has been allowed for completion of the transfer, a "Transmit" PDT instruction is addressed to the same line. If the "Transmit" PDT instruction is issued immediately, it is stalled until the other PDT instruction is completed. These instructions are executed when the central processor is not in the interrupt state. They cause the Type 285 to start transmission of the character and to send an interrupt to the central processor requesting the next character. Timing of the first interrupt is indeterminate.

2. Normal Transmission

Here, in response to an interrupt, the central processor stores its registers, verifies the Type 286 request for service, then addresses a "Receive Data" PDT instruction to line zero. Execution of this PDT instruction obtains the address and status of the line causing the interrupt. If the interrupt was caused by the line set to the transmit mode described in Section VII, F, I, above, a "Send Data" PDT instruction addressed to that line is executed to move the next data character from locations A+1 and A+2 to the buffer register. The procedure continues until the end of message is reached.

3. End of Transmission

In the end-of-transmission procedure, the last character of the message is transferred by a "Send Data" PDT instruction, and the program returns to a non-interrupt mode of operation. In response to the next interrupt from this line, the "Transmit Last Character" PDT instruction is executed. Upon completion of the last character's transmission, the line is again in the receive state. If the PDT instruction to transfer the last data character of

the message to the buffer register and the "Transmit Last Character" PDT instruction are executed in response to the same interrupt, the last data character is not transmitted and the Type 285 is reset to the receive state.

G. Operating with Synchronous Lines

The Type 286 requires two consecutive SYNC characters before the communication line is designated to be in synchronization. The second SYNC character causes the first interrupt from the line and is available to the program.

In certain applications the terminals are required to remain continually in synchronization. In this case, the Type 285 Communication Adapter Unit recognizes the synchronous characters, but the Type 286 recognizes only the control or transient leader character-the first character available to the program.

H. Feature 087 — The Longitudinal Redundancy Check (LRC)

When Feature 087 is present, one Type 286 eight-bit register per line is used to store the generated longitudinal redundancy check (LRC) character. Each time an appropriate PDT instruction transfers a character into the buffer register or out of it, a half-add operation is accomplished with that character and the contents of the LRC register. If the LRC register is initially reset, even parity is generated. The "Move LRC" PDT instruction moves the LRC character from its register to the data buffer register and resets the LRC register to zero. The LRC character parity bit or the character itself may require special handling by the program if the line format demands it. Section VI, I, describes parity check procedures.

1. Transmission of the LRC Character

After the end-of-message or end-of-block character has been transmitted to the Type 286 line buffer register, the "Move LRC" PDT instruction responds to the next interrupt. Any subsequent action depends on the format required by the particular line/remote terminal configuration.

If neither Feature 086 — character Parity — nor Feature 087 — LRC — are present, the program handles both types of checking.

If only Feature 087 is present, the generated LRC character is the half-add sum of all bits of each character transferred into its line buffer register or out of that register.

If only Feature 086 is present, the LRC character — supplied by the program — is transmitted with odd or even parity, depending on the state of the bit in the character's parity-bit position (Section VI, 9).

If Features 086 and 087 are both present, the following operations are performed.

a. When the line format requires odd parity and the LRC character has odd parity —

(1) Each character transferred to the Type 286 has zero in the parity-bit position. At the end of the message, the "Move LRC" PDT instruction is executed and — because it has zero in the parity bit — the generated LRC character is transmitted with odd parity;

(2) If line format requires the LRC character to be the half-add sum of all bits of each character, the message needs only an odd number of characters to be correct.

b. When the line format requires even parity and the LRC character has even-character parity —

(1) The message must have an odd number of characters to provide the correct LRC character;

(2) If the line format requires the LRC character to be the half-add sum of all bits of each character, the message needs an odd number of characters to provide the correct LRC character.

c. When the line format requires a constant in the parity-bit position —

(1) The program examines the LRC character and sets the parity-indicator bit to obtain the proper LRC character when transmitted.

2. Receiving the LRC Character

When an interrupt indicates that an LRC character from the remote terminal is in the buffer register, a "Receive Data" PDT instruction is executed to read the LRC character. The LRC character from the line is included in the locally generated LRC register when this transfer occurs. The "Move LRC" PDT instruction is sent to the Type 286, followed by a "Receive Data" PDT instruction. The last character read from the Type 286 is zero when the two LRC characters are equal (assuming that all characters of the message are included in the received LRC character).

The generated LRC character is always the half-add sum of the line characters, including the parity indicator bit.

I. Feature 086 — The Character Parity Check

Feature 086 provides the Type 286 Multi-Channel Communication Control with automatic character-parity generation and checking. The generated parity bit is inserted into the high-order bit position of the line character.

1. Transmission of the Parity Bit

When a zero is provided by the program in the parity-indicator position (line parity-bit position) of the communication code, the Type 286 calculates odd parity for that character and inserts the proper parity bit into the high-order bit position of the character when it is transferred to the shift register.

When the program provides a one in the parity-bit position of the communication code, even parity is provided.

2. Receiving the Parity Bit

When a character is received from the line with odd or even parity, the status bits received with the line address indicate character parity. Also, the line parity bit is transferred to the central processor with the data bits. No parity-error indicator exists in the Type 286.

J. Type 286 Timing Considerations

Information in locations A+1 and A+2 of a PDT A data field cannot be altered during the 15 main memory cycles occurring after the PDT instruction is extracted.

The timing information discussed above is based upon read/write channel access every six microseconds. If RWC1 is used and not interlocked in the Type 200 computer, access to main memory is granted every twelve microseconds. Thus the information in locations A, A+1 and A+2 of a PDT data field cannot be altered for 30 memory cycles if RWC1 and RWC1' are used. The effective scan rate of the Type 286 is decreased because of the increased time consumed while the scanner is stopped for data transfer.

VII. TRANSLATION

The Move and Translate (MAT) instruction is normally used to perform code translation with the Type 286 communication control.

HONEYWELL EDP TECHNICAL PUBLICATIONS
USERS' REMARKS FORM

TITLE: TYPE 286-1, -2, -3 MULTI-CHANNEL CCU DATED: OCTOBER 29, 1965

FILE NO: 112.0005.1100.00.03

ERRORS NOTED:

Fold

Cut Along Line

SUGGESTIONS FOR IMPROVEMENT:

Fold

FROM: NAME _____ DATE _____

COMPANY _____

TITLE _____

ADDRESS _____

_____

FIRST CLASS
PERMIT NO. 39531
WELLESLEY HILLS
MASS.

BUSINESS REPLY MAIL

No postage stamp necessary if mailed in the United States

POSTAGE WILL BE PAID BY

HONEYWELL
ELECTRONIC DATA PROCESSING DIVISION
60 WALNUT STREET
WELLESLEY HILLS, MASS. 02181

ATT'N: PUBLICATIONS AND WRITING SERVICES DEPARTMENT

Cut Along Line

Honeywell
ELECTRONIC DATA PROCESSING