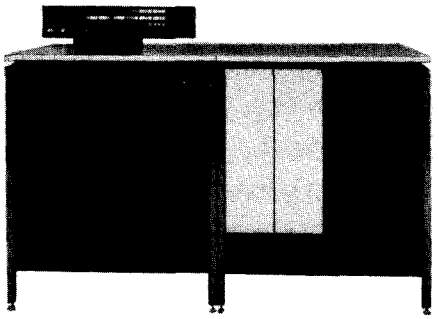
HONEYWELL

HARDWARE BULLETIN

SERIES 200

1201 CENTRAL PROCESSOR



In the Honeywell Series 200 Data Processing System, the 1201 Central Processor is a computing and control center of the Model 1200. It is subdivided into five major units: the arithmetic unit, the main memory, the control, memory, the control unit, and the input/output traffic control. Under the direction of an internally stored program, the central processor monitors and coordinates the various activities of the entire system.

The arithmetic unit performs such operations as comparisons, binary and decimal addition/subtraction, and decimal multiplication/division.

The control memory is a magnetic core storage unit consisting of up to 28 individually addressable control registers (the number of registers actually present depends upon the system configuration). During a program run, the control registers are used to store the main memory addresses that direct the retrieval and execution of all instructions.

Using information stored in control memory, the control unit selects, interprets, and executes all of the instructions in the internally stored program. The Model 1200 repertoire includes editing instructions, code translation instructions, a program interrupt instruction for automatic branching between a main program and servicing routines for all I/O devices, and two general-purpose input/output instructions, all in variable-length, two-address format. This repertoire can be expanded to include binary floating-point arithmetic, as well as binary-to-decimal and decimal-to-binary conversion, by equipping the central processor with the optional Scientific Unit, described in a separate hardware bulletin.

The input/output traffic control directs the time sharing of the main memory among the central processor and as many as four simultaneously operating peripheral devices. The traffic control makes it possible, for example, to read cards, punch paper tape, print, read or write magnetic tape, and compute — all at the same time. Typically, the central processor is free to perform other operations during up to 99.9 percent of processing intervals shared with peripheral operations.

The basic 16,384-character, magnetic core main memory may be expanded by adding up to seven memory modules of 16,384 characters each, for a capacity of 131,072 characters. The Model 1201 is equipped with fifteen index registers, and when the memory storage option is included, fifteen additional index registers are also included. There are no reserved input/output areas; the programmer has complete freedom in specifying both the sizes and the locations of these areas. A memory storage protect capability protects a programmer-specified memory area against unwanted interference from programs occupying unprotected portions of memory.

The interrupt processing facility of the 1201 consists of a hardware program interrupt, which signals a particular condition in a peripheral control, and a set of instructions used in processing interrupts. A program interrupt may occur whenever a peripheral device has completed an input/output operation—for example, when a tape read or write operation is completed or after the receipt of a character from a remote station by a communication control. Peripheral interrupts can be inhibited by the program as necessary.

The multi-level code handling facility enables the processor to bring into memory and manipulate data in many different codes. This feature includes the ability to translate automatically between character codes of up to 12 levels and also to trap special code configurations of up to 12 levels.

An outstanding design feature of the Series 200 permits execution of stored programs in conjunction with a technique known as instruction bypass; this hardware facility provides for automatic changes in program sequence without executing programmed instructions to initiate such changes.

An integral part of the central processor is the operator's control panel. By using various control switches, the operator can start and stop the machine and can load and interrogate main and control memory locations. The control panel is equipped with four "sense switches" which can be used in conjunction with programmed instructions to control the path of program execution.

A significant structural feature is the use of integrated system modules. Each peripheral control and central processor logic unit is housed in a separate logic drawer which tilts out of the central processor housing for easy access.

SPECIFICATIONS

PROCESSING UNIT: Six-bit character.

DATA FORMAT: Variable-length data fields of from one to virtually the maximum number of characters in the main memory.

(Continued on reverse side)

Specifications remain subject to change in order to allow the introduction of design improvements.

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Honeywell
ELECTRONIC DATA PROCESSING

INSTRUCTION FORMAT: Variable-length, two-address instructions. Typical format consists of op code, two addresses, and a variant character.

MAIN MEMORY SIZE: Basic memory, 16,384 characters. Additional memory available consisting of up to seven 16,384-character modules, providing a memory size of 131,072 characters.

INTERNAL OPERATIONS: Decimal and binary add/subtract, decimal multiply/divide, logic, program control, peripheral control, and editing.

INPUT/OUTPUT TRUNKS: Sixteen.

READ/WRITE CHANNELS: Four.

MAIN MEMORY CYCLE TIME: 1.5 microseconds.

CONTROL MEMORY ACCESS TIME: 250 nanoseconds.

CHECKING: Parity bit generated for each character as it is stored in memory. Character parity checked on readout.

ADDRESSING MODES: 2-character address specifies any of 4,096 memory locations, 3-character address specifies any of 32,768 memory locations, 4-character address specifies any of 131,072 memory locations.

TYPICAL OPERATING SPEEDS: See accompanying table.

SPECIAL FEATURES: Silicon semiconductor circuitry, fifteen (or thirty) index registers, four simultaneous input/output operations concurrent with computing, program interrupt, indirect addressing, multi-level code handling, scientific unit, memory protect.

INSTRUCTION REPERTOIRE MODEL 1200

The execution times listed in this table are based on realistic situations involving three-character addressing mode. The data fields referenced by both the A and B addresses are five characters long. Times for **indexed** operations assume that all address fields are indexed. In actual practice, higher speeds will be attained because in many cases abbreviated instruction formats can be used, thus shortening execution times.

NAME OF OPERATION	STANDARD FORMAT	EXECUTION TIME (MICROSECONDS) ADDRESSES NOT INDEXED	ADDRESSES INDEXED
Arithmetic Functions			
Decimal Add[1]	A/A/B	34.5	43.5
Decimal Subtract[1]	S/A/B	34.5	43.5
Binary Add	BA/A/B	34.5	43.5
Binary Subtract	BS/A/B	34.5	43.5
Zero and Add	ZA/A/B	27.0	36.0
Zero and Subtract	ZS/A/B	27.0	36.0
Multiply[2]	M/A/B	315.8	324.8
Divide	D/A/B	164.0	173.0
Logical Functions			
Half Add	HA/A/B	34.5	43.5
Extract	EXT/A/B	34.5	43.5
Compare	C/A/B	28.5	37.5
Substitute	SST/A/B/V	18.0	27.0
Branch	B/A	9.0	13.5
Branch on Condition Test	BCT/A/V	10.5	15.0
Branch on Character Condition	BCC/A/B/V	18.0	27.0
Branch if Character Equal	BCE/A/B/V	18.0	27.0
Branch if Bit Equal	BBE/A/B/V	18.0	27.0
General Control Functions			
Set Word Mark	SW/A/B	13.5	22.5
Set Item Mark	SI/A/B	13.5	22.5
Clear Word Mark	CW/A/B	15.0	24.0
Clear Item Mark	CI/A/B	15.0	24.0
Halt	H/A	9.0	13.5
No Operation	NOP	3.0	
Resume Normal Mode	RNM/A/B	13.5	22.5
Store Variant and Indicators	SVI/V	15.0	
Restore Variant and Indicators	RVI/A/V	13.5	18.0
Monitor Call	MC	3.0	
Store Control Registers	SCR/A/V	15.0	19.5
Load Control Registers	LCR/A/V	15.0	19.5
Change Addressing Mode	CAM/V	4.5	
Change Sequencing Mode	CSM/A/B/V	15.0	24.0
Load Index/Barricade Register	LIB/A	10.5	15.0
Store Index/Barricade Register	SIB/A	10.5	15.0
Data Move Instructions			
Move Characters to Word Mark	MCW/A/B	27.0	36.0
Load Characters to A-Field Word Mark	LCA/A/B	27.0	36.0
Move Item and Translate[3]	MIT/A/B/V_1/V_2/V_3	37.5	46.5
Move and Translate	MAT/A/B/V_1/V_2	36.0	45.0
Extended Move	EXM/A/B/V	28.5	37.5
Editing			
Move Characters and Edit[4]	MCE/A/B	64.5	73.5
Input/Output			
Peripheral Data Transfer	PDT/A/C_1/C_2	13.5	18.0
Peripheral Control and Branch	PCB/A/C_1/C_2	10.5	15.0

Scientific Instructions

See the hardware bulletin entitled: **Scientific Unit for Models 1200 and 2200 (Feature 1100)** — File No. 112.0005.1539.00.01.

1. Times indicate no recomplement cycle required; if required, add 15 microseconds.
2. Based on each multiplier digit having a median value of 4.5.
3. Based on each B-item information unit occupying two six-bit character locations.
4. Based on 5 characters scanned in both second and third passes.