HONEYWELL

HARDWARE BULLETIN

SERIES 200

8201 CENTRAL PROCESSOR

With the introduction of the Model 8200, Honeywell adds a powerful new dimension to the Series 200 Data Processing System. This new computer is designed to meet the requirements of a broad range of large-scale data processing jobs, including business and scientific tasks, real-time communications, and multiprogrammed, time-sharing applications. Such a design objective demands special capabilities for its fulfillment. In the Model 8200, Honeywell combines the latest advances in computer technology with the fruits of experience in designing and producing both word- and variable-length-field-oriented computers. The result is a system which incorporates both the computing power of word-oriented processing and the input/output flexibility of variable-length-field processing.

Specifications remain subject to change in order to allow the introduction of design improvements.

The 8201 Central Processor, the computing and control center of the Model 8200, consists of five functional units: a word processing subsystem, a variable-length-field (VLF) processing subsystem, a memory subsystem, an input/output controller, and a master control facility which coordinates the activities of the other units. Communication between units is effected by means of program interrupts and control instructions.

The word processing subsystem, which incorporates high internal speeds and extremely efficient execution logic, performs three-address instructions at an average rate of 400,000 per second. The word processor performs decimal and binary fixed- and floating-point arithmetic operations, including multiply and divide. Eight independent groups of 32 program control registers (eight of which are index registers) allow up to eight programs to be run in parallel. The control registers enable explicit addressing of all main memory locations and provide facilities for indexed, indirect and indexed indirect addressing. An extended addressing feature allows direct addressing of the entire memory, regardless of its size. This subsystem also includes extensive automatic masking facilities which enable the programmer to handle less-than-word-length operands easily and efficiently. Orthotronic Control, a standard feature of ¾-inch tape units, provides virtually foolproof error detection and automatic regeneration of lost data.

The VLF processing subsystem executes Series 200 instructions. Two subgroups of program control registers allow complete and independent control of two programs, one of which operates in a priority interrupt mode. Control register length enables explicit addressing of all main memory locations. Additional flexibility in accessing operands is provided by indexed (30 index registers are included) and indirect addressing facilities. The VLF processor performs decimal and binary arithmetic operations, including decimal multiply and divide. High internal speeds and efficient implementation of operations enable the VLF processor to attain an average execution rate of 100,000 two-address instructions per second (while the word processor is operating at full speed).

The memory subsystem consists of from two to eight modules of core memory and a memory controller. Each module is four characters in width and either 16,384 or 32,768 four-character groups in length. Data storage capacities of the memory subsystem range from 131,072 to 1,048,576 characters (16,384 to 131,072 words). Cycle time, when the memory is accessed by the word processing subsystem, is 750 nanoseconds per 48-bit

112.0011.0000.0-138
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Printed in U.S.A.

When ordering this publication please specify Title and Underscored portion of File Number.

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ELECTRONIC DATA PROCESSING

word; when memory access is by the VLF subsystem or the input/output subsystem, cycle time is 750 nanoseconds per four characters. Each memory access is automatically parity checked.

The memory controller provides for maximum simultaneity of memory operations by its ability to transfer data to and from a maximum of three memory modules simultaneously. This ability is achieved through the use of interleaved addressing and independent memory modules. The controller can allocate memory accesses to all other functional units, thus allowing word processing, VLF processing, and input/output operations to proceed independently and concurrently. In addition to handling and routing all requests for access to memory, the memory controller resolves conflicting requests and maintains control over the master-control-assigned protected memory areas. Separate protected memory areas may be assigned to each of the eight word-processor program control groups and to the VLF processor. These areas may be designated in blocks of 512 words (4,096 characters), and either write or read/write protection may be specified for each block. Each of the eight word programs, the VLF programs, and the master control facility have unique identification tags which allow access to their associated blocks of protected memory.

The input/output controller directs all peripheral device activity. It provides the path through which peripheral commands are initiated and the means for controlling the resulting data transfers. The basic unit allows up to 16 input/output operations (expandable to 32) to proceed simultaneously with internal word and VLF processing. Read/write channels associated with the controller are capable of variable assignment, thereby affording a maximum degree of I/O efficiency. Address assignments for up to 48 peripheral controls are provided in the basic system; more assignments may be added. All peripheral devices associated with the Series 200 and selected devices of the H-800/1800 systems are employed.

The master control facility, in conjunction with the master system control program, coordinates the over-all system activities. It controls and monitors the interactions of the word and VLF processing subsystems and the memory and input/output controllers. This facility sets memory partitions so as to allocate blocks (512 words or 4,096 characters) of memory to individual program control groups. The master control issues peripheral commands and device assignments, diagnoses program and memory usage violations, and maintains identification information regarding protected memory areas.

SPECIFICATIONS

PROCESSING UNIT: 48-bit word/6-bit character.

DATA FORMAT: Fixed-length-word processing and variable-length-field processing.

INSTRUCTION FORMAT: Fixed-length, three-address for word programs. Two-address for VLF programs.

MAIN MEMORY SIZE: Basic memory, 131,072 characters (16,384 words). Additional memory available for a maximum capacity of 1,048,576 characters. (131,072 words).

ADDRESS ASSIGNMENTS: Forty-eight, expandable to ninety-six.

READ/WRITE CHANNELS: Sixteen read/write channels are standard; sixteen additional read/write channels are available.

MAIN MEMORY CYCLE TIME: 750 nanoseconds per 48-bit word, when accessed by the word processing subsystem; 750 nanoseconds per four characters, when accessed by the VLF processing subsystem.

INTERLEAVED MEMORY: If more than one pair of memory modules is present, successive word addresses are assigned to different pairs of modules. For example, with four pairs of modules, word addresses 0, 4, 8, ... , are assigned to the first pair; 1, 3, 5, 9, ... , are assigned to the second pair, etc. By thus interleaving consecutive locations, instructions and operands are distributed among the pairs of modules so as to allow overlapping of memory accesses, thus reducing instruction execution time.

CONTROL MEMORY READ/WRITE TIME: 125 nanoseconds.

DATA TRANSFER RATE: Peak input/output data transfer of over 2.5 million characters per second.

SIMULTANEITY: Simultaneous memory access by one word program, one VLF program, and one input/output operation. Eight word-oriented programs simultaneous with any one of a set of VLF programs. Either 16 or 32 simultaneous input/output operations.

ADDRESSING: Word processor — Facilities for direct, indirect, indexed, and indexed indirect addressing. VLF processor — Facilities for direct, indirect, indexed, and indirect indexed addressing.

CHECKING: Eight parity bits (one parity bit for each character) are generated as each word is stored in memory. Parity is checked on readout. Other checking includes an instruction parity check, main and control memory address checks, and control and processing checks.

SPECIAL FEATURES: Extensive use of monolithic, integrated circuits, providing compactness, economy, and assured reliability. Time-sharing activities facilitated by a comprehensive interrupt scheme and by the ability to partition memory dynamically, protecting many memory segments. A floating-point arithmetic unit is available which handles decimal values from 10^{-65} to 10^{63} and binary values from 16^{-65} to 16^{63}. Complete compatibility with both the Series 200 and H-800/1800 systems.

INSTRUCTION REPERTOIRE
VARIABLE-LENGTH-FIELD PROCESSING SUBSYSTEM

The execution times given in this table are based on realistic situations involving the three-character addressing mode. The data fields referenced by both the A and B addresses are five characters long. Times for indexed operations are based on indexing of all address fields. In actual practice, higher speeds will be attained because in many cases abbreviated instruction formats can be used.

Name of Operation	Standard Format	Execution Time, Microseconds: Addresses Not Indexed	Execution Time, Microseconds: Addresses Indexed
Fixed-Point Arithmetic			
Decimal Add[1]	A/A,B	11.15	15.45
Decimal Subtract[1]	S/A,B	11.15	15.45
Decimal Multiply[2]	M/A,B	119.1	123.4
Decimal Divide[2]	D/A,B	59.5	63.8
Binary Add	BA/A,B	11.15	15.45
Binary Subtract	BS/A,B	11.15	15.45
Zero and Add	ZA/A,B	9.65	13.95
Zero and Subtract	ZS/A,B	9.65	13.95
Logical Functions			
Half-Add	HA/A,B	10.85	15.15
Extract	EXT/A,B	10.85	15.15
Compare	C/A,B	9.6	13.9
Substitute	SST/A,B,V	7.0	11.3
Branch	B/A	4.1	7.4
Branch on Condition Test	BCT/A,V	4.3	7.6
Branch on Character Condition	BCC/A,B,V	5.8	10.1
Branch if Character Equal	BCE/A,B,V	5.8	10.1
Branch on Bit Equal	BBE/A,B,V	5.8	10.1
General Control Functions			
Set Word Mark	SW/A,B	5.3	9.6
Set Item Mark	SI/A,B	5.3	9.6
Clear Word Mark	CW/A,B	5.3	9.6
Clear Item Mark	CI/A,B	5.3	9.6
Halt	H/A	4.5	7.8
No Operation	NOP	3.4	—
Resume Normal Mode	RNM/A,B	4.5	8.8
Store Variant and Indicators	SVI/V	8.4	—
Restore Variant and Indicators	RVI/A,V	7.1	10.4
Monitor Call	MC	3.4	—
Store Control Registers	SCR/A,V	5.7	9.0
Load Control Registers	LCR/A,V	5.7	9.0
Change Addressing Mode	CAM/V	3.5	—
Change Sequencing Mode	CSM/A,B,V	4.3	8.6
Store Index/Memory Protect Indicators	SIB/A	5.3	8.6
Load Index/Memory Protect Indicators	LIB/A	5.7	9.0
Data Move Instructions			
Move Characters to Word Mark	MCW/A,B	9.25	13.55
Load Characters to A-Field Word Mark	LCA/A,B	9.25	13.55
Move Item and Translate	MIT/A,B,V_1,V_2,V_3	14.8	19.1
Move and Translate	MAT/A,B,V_1,V_2	14.1	18.4
Extended Move	EXM/A,B,V	8.8	13.10
Editing			
Move Characters and Edit[3]	MCE/A,B	13.15	17.45
Input/Output			
Peripheral Data Transfer	PDT/A,C_1,C_2, . . . C_n	—	—
Peripheral Control and Branch	PCB/A,C_1,C_2, . . . C_n	—	—

[1]Based on no recomplement cycle; if recomplement cycle required, add 3.8 microseconds.
[2]Average time.
[3]Based on four characters scanned in both second and third passes.

INSTRUCTION REPERTOIRE
WORD PROCESSING SUBSYSTEM

NAME OF OPERATION	OPERAND SIZE	EXECUTION TIME IN MICROSECONDS[4]				
			APPROXIMATE MEAN TIME WITH INTERLEAVING			
		MINIMUM	4-WAY	2-WAY	1-WAY	MAXIMUM
Fixed-Point Arithmetic						
Binary Add, Subtract	44 Bits + Sign	1.75	2.19	2.48	3.0	3.0
Binary Accumulate	N Words	1.25 + .25N	1.35 + .25N	1.5 + .5N	1.5 + .75N	1.5 + .75N
Binary Multiply	44 Bits + Sign	5.0	5.0	5.0	5.0	5.0
Binary Divide	44 Bits + Sign	14.0	14.0	14.0	14.0	14.0
Decimal Add, Subtract	11 Digits + Sign	1.75	2.19	2.48	3.0	3.0
Decimal Accumulate	N Words	1.25 + .25N	1.35 + .25N	1.5 + .5N	1.5 + .75N	1.5 + .75N
Decimal Multiply	11 Digits + Sign	5.0	5.0	5.0	5.0	5.0
Decimal Divide	11 Digits + Sign	14.0	14.0	14.0	14.0	14.0
Word Add, Difference	48 Bits	1.75	2.19	2.48	3.0	3.0
Scientific Processing Instructions[1]						
Floating Binary Add, Subtract	—	2.25	3.0	3.3	4.15	5.5
Floating Binary Multiply	—	5.0	5.0	5.0	5.0	5.0
Floating Binary Divide	—	13.0	13.0	13.0	13.0	13.0
Floating Decimal Add, Subtract	—	2.25	3.0	3.3	4.15	5.5
Floating Decimal Multiply	—	5.0	5.0	5.0	5.0	5.0
Floating Decimal Divide	—	13.0	13.0	13.0	13.0	13.0
Normalized Less Than Comparison	—	3.0	3.25	3.25	3.25	3.5
Normalized Inequality Comparison	—	3.0	3.25	3.25	3.25	3.5
Multiple Unload	—	1.75	2.19	2.48	3.0	3.0
Fixed-Decimal to Floating-Binary Conversion	—	17.75	17.75	17.75	17.75	17.75
Floating-Binary to Fixed-Decimal Conversion	—	9.5	9.5	9.5	9.5	9.5
Fixed-to-Floating Normalize	—	1.75	2.19	2.48	3.0	3.0
Logical Functions						
Half Add	48 Bits	1.75	2.19	2.48	3.0	3.0
Superimpose	48 Bits	1.75	2.19	2.48	3.0	3.0
Substitute	48 Bits	2.5	2.94	3.23	3.75	3.75
Extract	48 Bits	1.75	2.19	2.48	3.0	3.0
Inequality Comparison, Alphanumeric	48 Bits	3.0	3.25	3.25	3.25	3.5
Inequality Comparison, Numeric	11 Digits or 44 Bits + Sign	3.0	3.25	3.25	3.25	3.5
Less Than Or Equal to Comparison, Alphanumeric	48 Bits	3.0	3.25	3.25	3.25	3.5
Less Than Or Equal to Comparison, Numeric	11 Digits or 44 Bits + Sign	3.0	3.25	3.25	3.25	3.5
Shift Instructions[2]						
Shift Word and Substitute	48 Bits	1.75	2.95	3.26	3.77	4.5
Shift Preserving Sign and Substitute	11 Digits or 44 Bits + Sign	1.75	2.95	3.26	3.77	4.5
Shift Word and Extract	48 Bits	1.75	3.46	3.86	4.13	4.5
Shift Preserving Sign and Extract	11 Digits or 44 Bits + Sign	1.75	3.46	3.86	4.13	4.5
Shift Word and Select	48 Bits	3.0	4.50	5.22	5.58	6.0
Data Move Instructions						
Transfer A to C	48 Bits	1.75	2.1	2.15	2.25	2.25
Transfer A to B and Go to C	48 Bits	1.75	2.1	2.15	2.25	2.25
Multiple Transfer	N Occurrences of Same Word	1.25 + .75N	1.25 + .95N	1.25 + 1.15N	1.25 + 1.3N	1.25 + 1.5N
N-Word Transfer	N Words	1.25 + .75N	1.25 + .95N	1.25 + 1.15N	1.25 + 1.3N	1.25 + 1.5N
Item Transfer	N Words	1.25 + .75N	1.25 + .95N	1.25 + 1.15N	1.25 + 1.3N	1.25 + 1.5N
Record Transfer	N Words	1.25 + .75N	1.25 + .95N	1.25 + 1.15N	1.25 + 1.3N	1.25 + 1.5N
General Control Functions						
Compute Orthocount	N Words	3.75 + .50N	3.75 + .75N	5.25 + 1N	6 + 1.25N	6 + 1.5N
Check Memory Parity	48 Bits	2.5	2.62	2.77	3.0	3.0
Multiprogram Control	—	3.5	3.50	3.50	3.75	3.75
Proceed	—	1.75	1.75	1.75	1.75	1.75
Simulator	—	1.75	2.62	2.77	3.0	3.0
Input/Output and Other Peripheral Functions[3]						
Read Forward	—	—	—	—	—	—
Read Backward	—	—	—	—	—	—
Write Forward	—	—	—	—	—	—
Peripheral Data Transfer	—	—	—	—	—	—
Print Alpha, Decimal, or Octal	—	—	—	—	—	—
Rewind Tape	—	—	—	—	—	—
Peripheral Control and Branch	—	—	—	—	—	—

[1]Single-precision, floating-point operands consist of a 1-bit sign, followed by a 7-bit exponent and a 40-bit mantissa. Times for additions and subtractions are based on no equalization.

[2]Execution times for shift instructions are based on an average shift distribution over 1-48 bits.

[3]Trapping of input/output operations into the master control facility requires approximately 4 microseconds; thereafter, the time required depends upon the operation being performed.

[4]Minimum times are for maximum overlap with 4-way interleaving, all addresses active and direct main memory. Maximum times are for all addresses indexed-indirect with no memory overlap. Mean times are calculated on a weighted distribution of addressing types and assuming random distribution of operands among the available memory banks. All times are exclusive of masking, which can take a maximum of two additional memory cycles, depending on overlap.