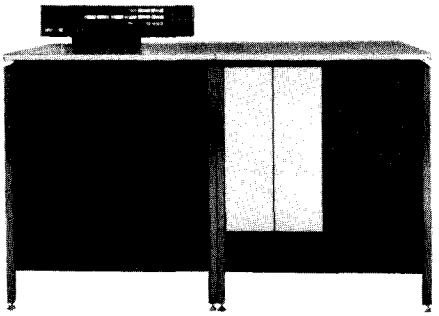
HONEYWELL

HARDWARE BULLETIN

SERIES 200

121 CENTRAL PROCESSOR



The Type 121 Central Processor is the computing and control center of the Model 120, the smallest member of the completely compatible Honeywell Series 200. Under the direction of an internally stored program, the 121 monitors and coordinates the various activities of the entire system. Six major units make up this central processor: the main memory, the control memory, the arithmetic unit, the control unit, the input/output traffic control, and the integrated peripheral controls.

The main memory provides magnetic core storage for instructions and operands, as well as for the new data which results from central processor operations. Having a basic magnetic core storage of 2,048 characters, the main memory may be initially expanded by adding one 2,048-character memory module; following this, one or more (up to a maximum of seven) 4,096-character modules may be added. In systems equipped with the Advanced Programming Instructions (Feature 1011) 24 memory locations are designated as six index registers. There are no reserved input/output areas; the programmer thus has complete freedom in specifying both the sizes and the locations of main memory input/output areas.

The control memory is a magnetic core storage unit consisting of 16 control registers. During a program run, the control registers are used to store the main memory addresses that direct the retrieval and execution of all instructions.

Operations such as binary and decimal addition/subtraction and comparisons are performed by the arithmetic unit.

The control unit, using information stored in the control memory, directs the operation of the entire system. As part of its activities, the control unit selects, interprets, and controls the execution of all instructions; controls the flow of information between the central processor and all input/output devices; and monitors the time sharing of the system to insure maximum operating efficiency.

Coordinating the flow of data (or "traffic") transferred during input and output activities is the function of the I/O traffic control. This coordination is achieved by directing the time sharing of the main memory between the central processor and two operating devices (or as many as three simultaneously operating devices when the system is equipped with Feature 1016, described below). The traffic control makes it possible, for example, to print, read cards, write a magnetic tape, and compute — all at the same time. Typically, the central processor is free to perform other operations during 75 to 99 percent of processing intervals shared with peripheral operations.

The basic input/output configuration of the Type 121 consists of: (1) two integrated peripheral controls — connecting to the Type 122 printer and the Type 214-2 card reader/card punch (or the Type 214-1 card punch and the Type 123 card reader); (2) facilities permitting the simultaneous operation of two out of three read/write channels; and (3) five peripheral address assignments on the central processor.

Addition of the Type 103 Magnetic Tape Control to the system allows the use of the Types 204B-11 and 204B-12 magnetic tape drives.

When the Series 200 Control Unit Adapter (Feature 1015) is added to the system, up to eight peripheral controls (including the standard integrated controls and the magnetic tape control, if used) may be connected to the peripheral interface. Adding the Series 200 Control Unit Adapter and Read/Write Channel (Feature 1016) — in lieu of Feature 1015 — also enables up to eight peripheral controls (including the standard integrated controls and the magnetic tape control, if used) to be connected; addition of this feature also provides the simultaneous use of the third read/write channel.

Processing which involves a combination of input/output operations and computing is supervised simply but efficiently by the automatic program interrupt facility. This facility, a significant feature of the Type 121, has important usage in directing operations such as reading and punching cards in real-time applications (e.g., in data communications). A program interrupt occurs whenever a peripheral device has completed an input/output operation. For example, a program interrupt may occur at the end of data transfer in a tape read operation. The interrupt source (i.e., the tape unit) is identified and a change in program sequence to service the interruption is automatically executed. Interrupts from particular peripheral controls can be inhibited or allowed under program control.

(Continued on reverse side)

Specifications remain subject to change in order to allow the introduction of design improvements.

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Honeywell

ELECTRONIC DATA PROCESSING

The operator's control panel, an integral part of the Model 120, includes the controls and indicators necessary to operate the central processor. Thus the operator, by using various switches, can start and stop the machine, as well as load and interrogate main memory locations. Four "sense" switches, which can be used in conjunction with programmed instructions to stop processing or to select predetermined program paths, are also included on the control panel.

Options available with the Type 121 — in addition to those already described — include Eight-Bit Code Handling (Feature 1014), the Edit Instruction (Feature 1013), and Magnetic Tape Compatibility (Feature 1055). The latter permits the system to read tape and write tape in IBM 1400 even-parity code when installed on the Type 103 Magnetic Tape Control.

SPECIFICATIONS

MAIN MEMORY SIZE: Basic memory, 2,048 characters. Additional memory available consisting of one 2,048-character module, and one or more (up to seven) 4,096-character modules.

PERIPHERAL ADDRESS ASSIGNMENTS: Five, expandable to sixteen via either Feature 1015 or Feature 1016.

EFFECTIVE MAIN MEMORY CYCLE TIME FOR COMPUTING: 3 microseconds.

CONTROL MEMORY ACCESS TIME: 250 nanoseconds.

READ/WRITE CHANNELS: Simultaneous use of any two of the three existing read/write channels is standard; simultaneous use of the third is optional. Data transfer rate is 167,000 characters/second per channel.

OPERATIONS: Decimal and binary arithmetic, program control, logic, and integrated peripheral control. Advanced programming, financial edit, code translation, and nonintegrated peripheral control operations optional.

TYPICAL OPERATING SPEEDS: See accompanying table.

PROCESSING UNIT: Six-bit character.

DATA FORMAT: Variable-length data fields of from one to virtually the maximum number of characters in the main memory.

INSTRUCTION FORMAT: Variable-length two-address instructions. Typical format consists of op code, two addresses, and a variant character.

CHECKING: Parity bit generated for each character as it is stored in memory. Character parity checked on readout.

ADDRESSING MODES: Two-character address specifies any of 4,096 memory locations, three-character address specifies any of 32,768 memory locations.

SPECIAL FEATURES: Silicon semiconductor circuitry, automatic interrupt, integrated control units, up to three simultaneous input/output operations concurrent with computing. Indirect and indexed addressing (includes six index registers) and magnetic tape read backward features are optional.

INSTRUCTION REPERTOIRE MODEL 120

The execution times listed in this table are based on realistic situations involving three-character addressing mode. The data fields referenced by both the A and B addresses are five characters long. Times for **indexed** operations assume that all address fields are indexed. In actual practice, higher speeds will be attained because in many cases abbreviated instruction formats can be used, thus shortening execution times.

NAME OF OPERATION	STANDARD FORMAT	EXECUTION TIME (MICROSECONDS) ADDRESSES NOT INDEXED	ADDRESSES INDEXED
Arithmetic Functions			
Decimal Add[1]	A/A,B	69.0	87.0
Decimal Subtract[1]	S/A,B	69.0	87.0
Binary Add	BA/A,B	69.0	87.0
Binary Subtract	BS/A,B	69.0	87.0
Zero and Add	ZA/A,B	54.0	72.0
Zero and Subtract	ZS/A,B	54.0	72.0
Logical Functions			
Half Add	HA/A,B	69.0	87.0
Extract	EXT/A,B	69.0	87.0
Compare	C/A,B	57.0	75.0
Substitute	SST/A,B,V	36.0	54.0
Branch	B/A	18.0	27.0
Branch on Condition Test	BCT/A,V	21.0	30.0
Branch on Character Condition	BCC/A,B,V	36.0	54.0
Branch if Character Equal	BCE/A,B,V	36.0	54.0
Branch if Bit Equal	BBE/A,B,V	36.0	54.0
General Control Functions			
Set Word Mark	SW/A,B	30.0	48.0
Set Item Mark	SI/A,B	30.0	48.0
Clear Word Mark	CW/A,B	30.0	48.0
Clear Item Mark	CI/A,B	30.0	48.0
Halt	H/A	18.0	27.0
No Operation	NOP	9.0	
Store Control Registers	SCR/A,V	30.0	39.0
Load Control Registers	LCR/A,V	30.0	39.0
Change Addressing Mode	CAM/V	12.0	
Change Sequencing Mode	CSM/A,B,V	33.0	51.0
Interrupt Control Functions			
Resume Normal Mode	RNM/A,B	30.0	48.0
Store Variant and Indicators	SVI/V	30.0	
Restore Variant and Indicators	RVI/A,V	36.0	45.0
Monitor Call	MC	9.0	
Data Move Instructions			
Move Characters to Word Mark	MCW/A,B	54.0	72.0
Load Characters to A-Field Word Mark	LCA/A,B	54.0	72.0
Move Item and Translate[2]	MIT/A,B,V_1,V_2,V_3	75.0	93.0
Move and Translate	MAT/A,B,V_1,V_2	72.0	90.0
Extended Move	EXM/A,B,V	57.0	75.0
Editing			
Move Characters and Edit[3]	MCE/A,B	129.0	147.0
Input/Output			
Peripheral Data Transfer	PDT/A,C_1,C_2,...C_n	21.0	30.0
Peripheral Control and Branch[4]	PCB/A,C_1,C_2,...C_n	21.0	30.0

1. Times indicate no recomplement cycle required; if required, add 30 microseconds.
2. Based on 5 characters read out of translation table.
3. Based on 5 characters scanned in both second and third passes.
4. Add 3 microseconds if a branch occurs.