Honeywell

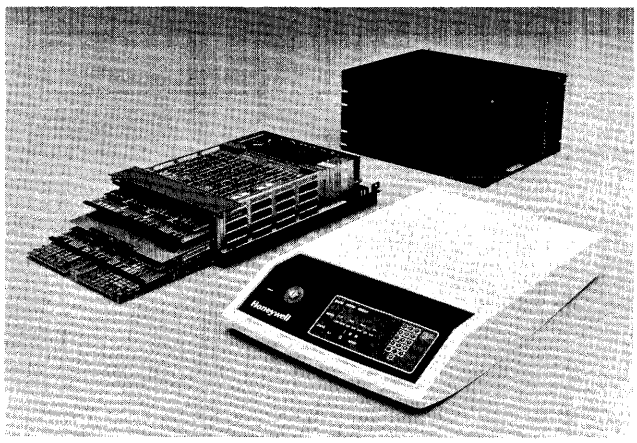
SERIES 60 (LEVEL 6)

Model 6/36 Minicomputer

The Model 6/36 is a solid-state, general-purpose minicomputer that can provide extensive system building capabilities and efficient, real-time handling of communications or control problems. The 6/36 central processor uses transistor-to-transistor logic (TTL) technology, and is state-of-the-art, open-ended, powerful, and flexible. The 16-bit word size makes the most of combined economy and functionality.

The Model 6/36 includes a central processor mounted in a five-slot or ten-slot Megabus chassis that is expandable to 23 slots, a basic or full control panel, multiply/divide hardware, a real-time clock, and a ROM bootstrap loader. Options include a memory controller with either parity or EDAC (Error Detection and Correction) memory, 8192-word Memory-Pacs providing a maximum of 65,536 words, the Multiple Device Controller (MDC9101), the Multiline Communications Processor (MLC9103), the General Purpose DMA Interface (GIS9001), and the Mass Storage Controller (MSC9101) as well as the associated Device- and Communications-Pacs, all Level 6 peripherals and their connector cables, a watchdog timer and the power supply, cabinetry and accessories (see Figure 1).

Physical configuration is flexible, reflecting the variety of uses Level 6 can be put to. The overriding consideration during development has been to provide a low-cost, modular, building-block system with minimal space and power requirements. Functional elements plug into or attach to each other without difficulty, needing little time and skill for assembly, disassembly and replacement.



FEATURES

- Firmware-driven processor:
  - Enables multiple vectored interrupts to 64 levels
  - Provides multiple vectored trap structure
  - Automatically saves and restores vital information in case of interrupts and traps
- Sophisticated addressing mechanism for:
  - Bit/byte/word/multiple word
  - Immediate address
  - PUSH/POP (auto post-increment/ pre-decrement)
  - Base and program counter plus/minus displacement
- Megabus permitting interleaved transfers with a practical six-megabyte throughput rate, 300 nanosecond cycle time
- Direct memory access as standard input/output method
- Up to 65,536 words (in 8K-word Memory-Pacs) of memory; up to four Memory-Pacs per board
- Additional memory or additional/different interface requirements satisfied by simple, plug-in operation
- Automatic quality logic tests (QLT) as part of bootstrap operation
- Exclusive "shoelace circuit" with LED display reports on connect status and QLT
- 18 registers provide for:
  - Eight modes of addressing, including PUSH/POP
  - Multiple accumulators
  - Indexing
- Extensive use of firmware to support task dispatching and input/output control
- Optional attachment of Multiline Communications Processors, Multiple Device Controllers, user-adaptable General Purpose DMA Interface, and Mass Storage Controllers

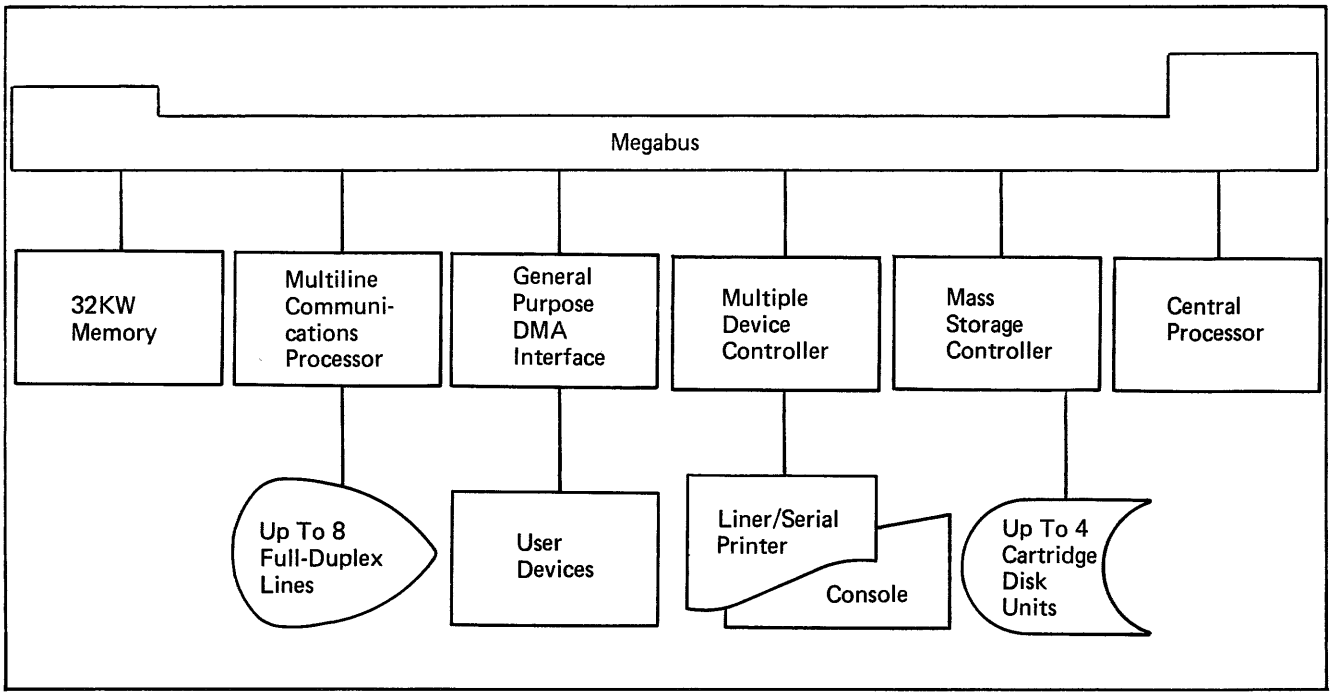


Figure 1. Typical 6/36 System

PROCESSOR COMPONENTS

The Model 6/36 includes, in addition to the central processor itself, the following components:

- Megabus
- Basic or Full Control Panel
- Five-Slot or Ten-Slot Chassis
- Power Supply
- Multiply/Divide
- Real-Time Clock
- ROM Bootstrap Loader

Memory

The two kinds of memory offered with the 6/36 – parity memory and EDAC memory – incorporate the reliability, low cost, and high density of MOS components.

The 6/36 memory uses state-of-the-art semiconductor technology, N-channel, and 4096-bit dynamic RAM as the storage media. Its design emphasizes high reliability, low cost, modularity, and simplified field maintenance. Like other elements of Level 6, the memory is a bus-compatible subsystem that communicates directly with and in the same fashion as any other element on the Megabus. TTL MSI circuitry minimizes power and space requirements for the extensive functionality provided. Self-contained on each Memory-Pac is bus support, refresh and initialization logic.

The parity memory offered includes logic for storing/retrieving two parity bits per word on each 8K-word Memory-Pac. Thus the actual word size in memory is 18 bits.

The EDAC memory includes six additional bits (EDAC code) per word, which are derived from the data bits. When the 22-bit word is read, memory attempts to correct any internally caused data error, reporting the results over two dedicated leads on the Megabus. Each lead sets a specific status bit depending on whether the error has been corrected or not. The EDAC memory is particularly desirable for large systems, where extended reliability is required.

With either kind of memory, address parity accompanies the most significant eight bits on the address bus. When memory detects an error on these bits, it does not respond; the result is a bus timeout. Note also that each device controller/communication processor on the Megabus checks parity on information received from the Megabus and indicates an error by setting a parity error status bit.

Memory Save and Autorestart, available as an option, ensures data retention for 131,072 bytes of memory for a two-hour period. Support circuit power runs are separated to minimize standby power drain. Electronics within the optional unit maintain battery charge, regulate outputs, and indi-

cate holdup failures. Power failures generate an interrupt, after which user-save operations are performed. Following power failures, operations are automatically resumed, starting at memory location zero.

The Watchdog Timer option enables interruption of central processor operations at preset time intervals.

Megabus

The Megabus is the heart of the 6/36 and central to its performance. All elements of Level 6 – central processor, memory, multiple device controllers, communications processors, General Purpose DMA Interfaces, and mass storage controllers – are attached to the Megabus and all transfers (memory, interrupts, and instructions) between them take place on it. Communication among these elements is asynchronous, permitting elements of different speeds to operate efficiently. Because of its versatility, only one Megabus is required for use on Level 6. In addition, the Level 6 Megabus offers an unusually high transfer rate: six million bytes (i.e., halfwords) per second (300 nanoseconds per 16-bit transfer cycle).

The Level 6 Megabus is based on TTL technology. Etched wires join connectors, meaning fewer connections, lower costs, and higher reliability.

Sixty-four vectored-interrupt levels are provided, and an automatic interrupt identification feature causes an interrupting device to identify itself to the central processor. No private wires are provided for interrupts; an interrupt is handled as just one more type of message transmitted on the Megabus. Parity checking ensures the integrity of data transfers.

The Megabus transfers either words or bytes. Memory is used efficiently, and controller transfers can start or end on arbitrary byte boundaries. All transfers are direct memory access; each device controller maintains its own information about the location in memory to/from which data is to be transferred and accesses that location directly. Each unit on the Megabus contains all the control and timing it needs to use the Megabus, without dependence on a central control unit of any kind.

Control Panel

A choice of two types of control panels offers users flexibility, economy, and security of operation:

- Basic Panel – Offers security and economy in multisystem applications. Enables connection to the portable plug-in panel.
- Full Panel – Allows the CP register and main memory contents to be entered and displayed. It controls, in a step-by-step fashion, the system initialization sequence by single-stepping a program, and stopping and starting program execution. Includes 6-digit hexadecimal (hex) display and 16-key hex pad.

A portable plug-in panel option (CPF9408) also provides security, economy, and flexibility of operation in multisystem environments. The panel is self-contained and full control, and can plug into any basic panel.

A vertical panel mounting option (CPF9407) is available for any rack-mountable system where physical space limitations exist. The panel replaces the standard inclined panel mounting and is designed for OEMs with their own cabinetry. If Honeywell cabinetry is desired, the panel can be ordered only with the following:

CAB9004: 60-inch rack without ... panel or doors
CAB9008: Rack panel ... for one side
CAB9009: Rack door ... full rear
CAB9010: Extension table wing

CABINETRY

A variety of cabinetry options are available; all provide easy access and require only front-to-rear airflow for cooling.

- Drawer units 5.25 inches (13.33 cm) and 10.50 inches (26.67 cm) high for standard EIA rack mounting
- Cabinets 60.0 inches (152.40 cm) high for central processor, diskette, and other drawers
- Tabletop configurations, completely enclosed, completely portable, 5.5 inches (13.97 cm) high, 19.5 inches (49.53 cm) wide, 29.7 inches (75.43 cm) deep

OPTIONS

- PSS9001 – Tabletop Memory Save and Autorestart for 8KW to 65KW Memory
- PSS9002 – Rack-mountable Memory Save and Autorestart for 8KW to 65KW Memory
- CMC9001 – Memory Controller with parity plus 8K-word Memory-Pac (CMM9001). Up to three more Memory-Pacs may be added.
- CMM9001 – 8K-word Memory-Pac with Parity
- CMC9002 – EDAC Memory Controller plus 8K-

word EDAC Memory-Pac (CMM9002). Up to three more Memory-Pacs may be added.

- CMM9002 – 8K-word EDAC Memory-Pac
- CPF9401 – Watchdog Timer
- CPF9408 – Portable Plug-in Panel
- CPF9407 – Vertical Panel Mounting

SIMPLIFIED MAINTENANCE

Level 6 provides simplified maintenance via:

- Automatically executed quality logic tests (QLTs) for the processor, memory, MDC, MLCP, and MSC boards permanently resident in their ROMs
- Use of LED indicators on each board to indicate the specific board failing a QLT
- A family of freestanding test and verification programs for the central and I/O subsystems that permit diagnosis to the appropriate level
- Easy replacement of failed system board or Pac by simply unplugging the failed unit and plugging in a replacement

SPECIFICATIONS

LEVEL 6 MEGABUS: Provides bidirectional asynchronous communications path between all boards
Cycle Time – 300 nanoseconds
Throughput – Up to three million words per second
Slots – Up to 23
CENTRAL PROCESSOR: Interrupt-driven; processes bits, bytes, words, and multiwords; real-time clock; ROM bootstrap loader; basic/full control panel; multiply/divide hardware
Addressing modes – Direct (up to 64K words); indirect; base plus displacement; base plus displacement indirect; base plus index; base plus index indirect; base plus index push/pop; base push/pop; program counter plus displacement; program counter plus displacement indirect; indexed; direct register operand; and immediate operand
Registers – 18
Interrupt Levels – 64 (vectored), allowing interrupts to be set at the channel level
Options – Watchdog timer; Portable plug-in panel; Vertical panel mounting
MEMORY: Provides up to 64K words of storage in 8K modules
Type – 4K, N-channel, MOS
Cycle Time – 650 nanoseconds
Size (16-bit words) – 8,192 to 65,536
Options – Memory Save and Autorestart; EDAC (Error Detection and Correction)
MULTIPLE DEVICE CONTROLLER (MDC9101): Controls up to four devices using Device-Pacs (i.e., adapters)
Type – Four levels of simultaneity
Throughput – 32,500 words per second
MASS STORAGE CONTROLLER (MSC9101): Controls up to four disk units with total capacity from 2.5 to 44.8 million bytes
Type – One data transfer operation concurrent with multiple seek operations
Throughput – 312,500 bytes per second
GENERAL PURPOSE DMA INTERFACE (GIS9001): Provides user interface point for attachment of user-designed adapters
Type – Single level of simultaneity
Throughput – 500,000 words per second (memory-to-user device or opposite direction)
MULTILINE COMMUNICATIONS PROCESSOR (MLC9101): Controls up to eight synchronous or asynchronous full-duplex lines or up to four broad band full-duplex lines
Type – Programmable
Interfaces – EIA RS232C, MIL 188C, Broad band CCITT V35, direct connect, Bell 301/303
Throughput – Up to 20,000 characters per second

INSTRUCTION SET

The programmer-oriented instruction set facilitates the writing of compact, efficient programs and offers the right instruction for each function. The multiple word length capability makes it easy to handle data elements of varying size, and the indexing techniques are completely integrated into the architecture.

SINGLE OPERAND INSTRUCTIONS

Modify	Description
INC	Increment
DEC	Decrement
NEG	Negate
CPL	Complement
CL	Clear
CLH	Clear Halfword
CMZ	Compare to Zero
CAD	Add Carry Bit to Contents
Control	**Description**
STS	Store S-Register
JMP	Jump
ENT	Enter
LEV	Change Level
SAVE	Save Context
RSTR	Restore Context
Bit	**Description**
LB	Load Bit
LBF	Load Bit and Set False
LBT	Load Bit and Set True
LBC	Load Bit and Complement
LBS	Load Bit and Swap
Double Word	**Description**
LDI	Load Double Integer
SDI	Store Double Integer

DOUBLE OPERAND INSTRUCTIONS

Word	Description
LDR	Load R-Register
STR	Store R-Register

Word	Description
SRM	Store R-Register through Mask
SWR	Swap R-Register
CMR	Compare Contents to R-Register
ADD	Add Contents to R-Register
SUB	Subtract from R-Register
MUL	Multiply R-Register
DIV	Divide R-Register by Contents of Location
OR	Inclusive OR with R-Register
XOR	Exclusive OR with R-Register
AND	AND Contents with R-Register

Byte	Description
LDH	Load Halfword into R-Register
STH	Store R-Register Halfword
CMH	Compare Halfword to R-Register
ORH	Halfword Inclusive OR with R-Register
XOH	Halfword Exclusive OR with R-Register
ANH	Logically AND Halfword with R-Register
LLH	Load Logical Halfword into R-Register

Mode and Base Register	Description
MTM	Modify or Test M-Register
STM	Store M-Register
LDB	Load B-Register
STB	Store B-Register
CMB	Compare Contents to B-Register
CMN	Compare to Null
SWB	Swap B-Register
LAB	Load Effective Address into B-Register
LNJ	Load B-Register and Jump

BRANCH INSTRUCTIONS

Branch on Register	Description
BLZ	Branch If R-Register Less Than Zero
BGEZ	Branch If R-Register Equal to or Less Than Zero

Branch on Register	Description
BEZ	Branch If R-Register Equal to Zero
BNEZ	Branch If R-Register Not Equal to Zero
BGZ	Branch If R-Register Greater Than Zero
BLEZ	Branch If R-Register Equal to or Less Than Zero
BODD	Branch If R-Register Odd
BEVN	Branch If R-Register Even
BINC	Branch and Increment
BDEC	Branch and Decrement

Branch on Indicator	Description
B	Branch
NOP	No Operation
BE	Branch If Equal
BNE	Branch If Not Equal
BAL	Branch If Algebraically Less Than
BAGE	Branch If Algebraically Greater Than or Equal to
BAG	Branch If Algebraically Greater Than
BALE	Branch If Algebraically Less Than or Equal to
BL	Branch If Less Than
BGE	Branch If Greater Than or Equal to
BG	Branch If Greater Than
BLE	Branch If Less Than or Equal to
BSU	Branch If Signs Unlike
BSE	Branch If Signs Equal
BCT	Branch If Carry
BCF	Branch If No Carry
BBT	Branch If Bit Test Indicator True
BBF	Branch If Bit Test Indicator False
BIOT	Branch If I/O Indicator True
BIOF	Branch If I/O Indicator False

Branch on Indicator	Description
BOV	Branch If R-Register Overflow
BNOV	Branch If No R-Register Overflow

SHIFT INSTRUCTIONS

Shift Short	Description
SOL	Single Shift Open Left
SCL	Single Shift Closed Left
SAL	Single Shift Arithmetic Left
DCL	Double Shift Closed Left
SOR	Single Shift Open Right
SCR	Single Shift Closed Right
SAR	Single Shift Arithmetic Right
DCR	Double Shift Closed Right
Shift Long	**Description**
DOL	Double Shift Open Left
DAL	Double Shift Arithmetic Left
DOR	Double Shift Open Right
DAR	Double Shift Arithmetic Right

GENERIC INSTRUCTIONS

Instruction	Description
HLT	Halt
MCL	Call Monitor via Trap
RTT	Return from Trap
RTCN	Real-Time Clock On
RTCF	Real-Time Clock Off
WDTN	Watchdog Timer On[a]
WDTF	Watchdog Timer Off[a]
BRK	Break Trap

SHORT VALUE IMMEDIATE INSTRUCTIONS

Instruction	Description
LDV	Load Value
CMV	Compare Value to R-Register
ADV	Add Value to R-Register
MLV	Multiply by Value

INPUT/OUTPUT INSTRUCTIONS

Instruction	Description
IO	Input/Output Word
IOH	Input/Output Halfword
IOLD	Input/Output Load

[a]Optional.

Specifications may change as design improvements are introduced.

Honeywell

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