Honeywell

SERIES 60 (Level 6)

Model 6/43 Minicomputer

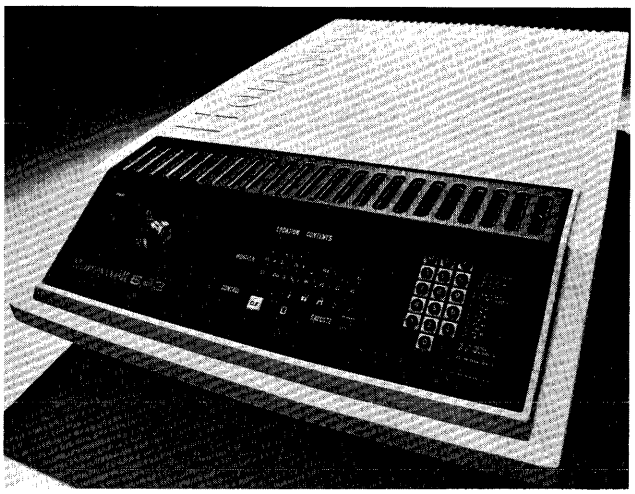
The Model 6/43 is a new member in Honeywell's Level 6 family of state-of-the art minicomputers. The 6/43 offers high levels of functionality and performance to help provide efficient communications and data processing capabilities and extensive system building capabilities. The central processor uses Schottky transistor-to-transistor logic (TTL) technology, and is open-ended, powerful and flexible. The 16-bit word size makes the most of combined economy and functionality.

Included in the Model 6/43 is a central processor mounted in a five-slot or ten-slot Megabus chassis (both expandable to 23 slots), a basic or full control panel, multiply/divide hardware, a real-time clock, a watchdog timer and a ROM bootstrap loader.

The 6/43 offers parity or EDAC (Error Detection and Correction) memory, with a maximum of one million words of directly addressable memory. Users may choose different memory controllers to enable single fetch or double fetch capability with both types of memory. Using the single fetch technique, memory is increased by adding 8K word Memory-Pacs; with the double fetch memory, these Memory-Pacs are added two at a time. Single-fetch and double-fetch memories may not be intermixed on the same system. Core memory is available as an option.

Additional options include the Multiple Device Controller, the Multiline Communications Processor, the Mass Storage Controller, the Magnetic Tape Controller, the Scientific Instruction Processor, the Memory Management Unit and the General Purpose DMA Interface (see Figure 1). There are also the associated Device-Pacs and Communications-Pacs, all Level 6 peripherals and their connector cables, the power supply, cabinetry and accessories.

Physical configuration is flexible, reflecting the variety of uses Level 6 can be put to. The overriding consideration during development has been to provide a low-cost, modular system with minimal space and power requirements. Functional elements plug into or attach to each other without difficulty, needing little time or effort for assembly, disassembly and replacement.



FEATURES

- Firmware-driven processor:
  - Enables multiple vectored interrupts to 64 levels
  - Provides multiple vectored trap structure
  - Automatically saves and restores vital information in case of interrupts and traps
- Sophisticated addressing mechanism for:
  - Bit/byte/word/multiple word
  - Immediate address
  - PUSH/POP (auto post-increment/pre-decrement)
  - Base and program counter plus/minus displacement
- Megabus that permits interleaved transfers with a practical six-megabyte throughput rate, 300 nanosecond cycle time
- Direct memory access as standard input/output method
- Up to one million words of directly addressable memory
- Single-fetch or double-fetch memory technique
- Additional memory or additional/different interface requirements that are satisfied by simple, plug-in operation
- Automatic quality logic tests (QLT) as part of bootstrap operation

- "Shoelace circuit" with LED display that reports on connect status and QLT results
- 24 registers that provide for:
  - 17 modes of addressing, including PUSH/POP
  - Multiple accumulators
  - Indexing
  - Memory to memory (byte-string) move
  - Double word (32 bit) add/subtract
  - Hardware stack/queue
- Extensive use of firmware to support task dispatching and input/output control
- Optional attachment of:
  - Multiline Communications Processors
  - Multiple Device Controllers
  - Mass Storage Controllers
  - Magnetic Tape Controllers
  - Scientific Instruction Processors
  - Memory Management Unit
  - General Purpose DMA Interfaces (user-adaptable)
- Full compatibility with 6/30 models' peripheral controllers, bus, and instruction sets.

PROCESSOR COMPONENTS

The Model 6/43 includes, in addition to the central processor itself, the following components:

- Megabus
- Basic or full control panel
- Five-slot or ten-slot chassis
- Power supply
- Multiply/divide
- Real-time clock
- ROM bootstrap loader
- Watchdog timer

Memory

The 6/43 memory uses state-of-the-art semiconductor technology, N-channel, 4096-bit MOS dynamic RAMs as the storage media. Its design emphasizes high reliability, low cost, modularity and simplified field maintenance. Like other elements of Level 6, the memory is a bus-compatible subsystem that communicates directly with and in the same fashion as any other element on the Megabus. TTL MSI circuitry minimizes power and space requirements for the extensive functionality provided.

The two kinds of memory offered with the 6/43 – parity memory and EDAC memory – incorporate the reliability, low cost and high density of MOS components.

The EDAC memory includes six additional bits (EDAC code) per word, which are derived from the data bits. When the 22-bit word is read, memory corrects any internally caused single-bit data error, reporting the results over two dedicated leads on the Megabus. Each lead sets a specific status bit depending on whether the error has been corrected or not. All single-bit errors are corrected while all double-bit errors are detected. The EDAC memory is particularly desirable for large systems, where extended reliability is required.

With either kind of memory, address parity accompanies the most significant eight bits on the address bus. When memory detects an error on these bits, it does not respond; the result is a bus timeout. Note also that each device controller/communication processor on the Megabus checks parity on information received from the Megabus and indicates an error by setting a parity error status bit.

For both EDAC and parity memory, users may choose to use a memory controller with standard single-fetch memory technique or a memory controller with double-fetch memory technique. Double-fetch memory is available only in 16K increments. Single-fetch and double-fetch memories cannot be mixed on the same system.

An optional Memory Save and Autorestart Unit ensures data retention for two memory boards that can store up to 64K words of memory for a two-hour period. Support circuit power runs are separated to minimize standby power drain. Electronics within the optional unit maintain battery charge, regulate outputs and indicate holdup failures. Power failures generate an interrupt, and the user-save operations are performed. Following power failures, operations are automatically resumed, starting at memory location zero.

To facilitate multi-user systems, the central processor accommodates an optional Memory Management Unit that permits the allocation and assignment of memory among users and provides for segmentation and Read/Write/Execute protection based on four rings of privilege. The unit also provides base relocation and descriptor validation.

Core memory is also available as an option for maximum data retention if main power is down for long periods of time.

Megabus

The Megabus is the heart of the 6/43 and central to its performance. All elements of the 6/43 – central processor, memory, multiple device controllers, communications processors, mass storage controllers, magnetic tape controllers, scientific instruction processor and general purpose DMA interfaces – are attached to the Megabus and all transfers (memory, interrupts and instructions) between them take place on the Megabus. Communication among these elements is asynchronous, permitting elements of different speeds to operate efficiently. Because of its versatility, only one Megabus is required for use on Level 6 systems. In addition, the Level 6 Megabus offers a high transfer

rate of six million bytes (i.e., halfwords) per second (300 nanoseconds per 16-bit transfer cycle).

The Level 6 Megabus is based on TTL technology. Etched wires join connectors, meaning fewer connections, lower costs, and higher reliability.

Sixty-four vectored-interrupt levels are provided. An automatic interrupt identification feature causes an interrupting device to identify itself to the central processor. No private wires are required for interrupts; an interrupt is handled as just one more type of message transmitted on the Megabus. Parity checking ensures the integrity of data transfers.

The Megabus transfers either words or bytes. Memory is used efficiently, and controller transfers can start or end on arbitrary byte boundaries. All transfers are direct memory access; each device controller maintains its own information about the location in memory to/from which data is to be transferred and accesses that location directly. Each unit on the Megabus contains all the control and timing it needs to use the Megabus, without dependence on a central control unit.

Control Panels

A choice of two types of control panels offers users flexibility of operation. The basic panel controls system initialization and offers security and economy in multisystem applications. It also enables connection of the portable plug-in panel.

The full control panel allows the CP register and main memory contents to be entered and displayed. It can control, in a step-by-step fashion, the system initialization sequence by single-stepping a program, and stopping and starting program execution. The full panel includes a 7-digit hexadecimal (hex) display and a 16-key hex pad.

A portable plug-in panel option also provides security, economy, and flexibility of operation in multisystem environments. This option is a self-contained full control panel and can plug into any basic panel.

A vertical panel mounting option is available for any rack-mountable system where physical space limitations exist. The panel replaces the standard inclined panel mounting and is designed for OEMs with their own cabinetry. If Honeywell cabinetry is desired, the panel can be ordered only with the following:

CAB9004: 60-inch (154-centimetre) rack without ... panel or doors
CAB9008: Rack panel ... for one side
CAB9009: Rack door ... full rear
CAB9010: Extension table wing

CABINETRY

A variety of cabinetry options are available; all provide easy access and require only front-to-rear air flow for cooling.

- Drawer units 5.25 in (13.3 cm) and 10.5 in (26.7 cm) high for standard EIA rack mounting
- Cabinets 60 in (152 cm) high for central processor, diskette, and other drawers
- Tabletop configurations, completely enclosed, completely portable, 5.5 in (13.9 cm) high, 19.5 in (49.5 cm) wide, 29.7 in (75.4 cm) deep
- Office packaging, custom-shaped desk 29.5 in (74.9 cm) high; 49 in (124 cm) wide; 33 in (83.3 cm) deep; integrated keyboard (optional); concealed control panel; 29.5 in (74.9 cm) high standard EIA rack space.

OPTIONS

- PSS9001 – Tabletop Memory Save and Autorestart for 8KW to 64KW Memory
- PSS9002 – Rack-mountable Memory Save and Autorestart for 8KW to 64KW Memory
- CMC9001 – Memory Controller with parity plus 8K-word Memory-Pac (CMM9001); up to three more Memory-Pacs may be added
- CMM9001 – 8K-word Memory-Pac with Parity
- CMC9002 – EDAC Memory Controller plus 8K-word EDAC Memory-Pac (CMM9002); up to three more Memory-Pacs may be added
- CMM9002 – 8K-word EDAC Memory-Pac
- CMC9501 – Double-Fetch Memory Controller with 16KW Parity Memory (one more 16KW module can be added)
- CMC9502 – Double-Fetch Memory Controller with 16KW EDAC Memory (one more 16KW module can be added)
- CMM9501 – Additional 16KW module for CMC9501
- CMM9502 – Additional 16KW module for CMC9502
- CMC9005 – Core Memory Controller with 16KW of parity core memory
- CMC9006 – Core Memory Controller with 32KW of parity core memory
- CPF9504 – Portable Plug-in Panel
- CPF9505 – Vertical Control Panel Mounting

SIMPLIFIED MAINTENANCE

Level 6 provides simplified maintenance via:

- Automatically executed quality logic tests (QLTs) for the processor, memory, MDC, MLCP, MSC, MTC and Scientific Instruction Processor boards permanently resident in their ROMs
- Use of LED indicators on each board to indicate the specific board failing a QLT

- A family of freestanding test and verification programs for the central and I/O subsystems that permit diagnosis to the appropriate level
- Easy replacement of a failed system board or Pac by simply unplugging the failed unit and plugging in a replacement

INSTRUCTION SET

The programmer-oriented instruction set (see table) facilitates the writing of compact, efficient programs and offers the right instruction for each function. The multiple word length capability makes it easy to handle data elements of varying size, and the indexing techniques are completely integrated into the architecture.

INSTRUCTION SET

SINGLE OPERAND INSTRUCTIONS

Modify	Description
INC	Increment
DEC	Decrement
NEG	Negate
CPL	Complement
CL	Clear
CLH	Clear halfword
CMZ	Compare to zero
CMN	Compare to null
CAD	Add carry bit to contents

Control	Description
STS	Store S-register
JMP	Jump
ENT	Enter
LEV	Change level
SAVE	Save context
RSTR	Restore context

Bit	Description
LB	Load bit
LBF	Load bit and set false
LBT	Load bit and set true
LBC	Load bit and complement
LBS	Load bit and swap

Double Word	Description
LDI	Load double integer
SDI	Store double integer

DOUBLE OPERAND INSTRUCTIONS

Word	Description
LDR	Load R-register
STR	Store R-register
SRM	Store R-register through mask
SWR	Swap R-register
CMR	Compare contents to R-register
ADD	Add contents to R-register
SUB	Subtract from R-register
MUL	Multiply R-register
DIV	Divide R-register by contents of location
OR	Inclusive OR with R-register
XOR	Exclusive OR with R-register
AND	AND contents with R-register
AID	Double word add
SID	Double word subtract

Byte	Description
LDH	Load halfword into R-register
STH	Store R-register halfword
CMH	Compare halfword to R-register
ORH	Halfword inclusive OR with R-register
XOH	Half-word exclusive OR with R-register
ANH	Logically AND halfword with R-register
LLH	Load logical halfword into R-register

Mode and Base Register	Description
MTM	Modify or test M-register
STM	Store M-register
LDB	Load B-register
STB	Store B-register
CMB	Compare contents to B-register
CMN	Compare to null
SWB	Swap B-register
LAB	Load effective address into B-register
LNJ	Load B-register and jump

SHORT VALUE IMMEDIATE INSTRUCTIONS

Instruction	Description
LDV	Load value
CMV	Compare value to R-register
ADV	Add value to R-register
MLV	Multiply by value

BRANCH INSTRUCTIONS

Branch on Register	Description
BEZ	Branch if R-register less than zero
BGEZ	Branch if R-register equal to or less than zero
BEZ	Branch if R-register equal to zero
BNEZ	Branch if R-register not equal to zero
BGZ	Branch if R-register greater than zero
BLEZ	Branch if R-register equal to or less than zero
BODD	Branch if R-register odd
BEVN	Branch if R-register even
BINC	Branch and increment
BDEC	Branch and decrement

Branch on Indicator	Description
B	Branch
NOP	No operation
BE	Branch if equal
BNE	Branch if not equal
BAL	Branch if algebraically less than
BAGE	Branch if algebraically greater than or equal to
BAG	Branch if algebraically greater than
BALE	Branch if algebraically less than or equal to
BL	Branch if less than
BGE	Branch if greater than or equal to
BG	Branch if greater than
BLE	Branch if less than or equal to
BSU	Branch if signs unlike
BSE	Branch if signs equal
BCT	Branch if carry
BCF	Branch if no carry
BBT	Branch if bit test indicator true
BBF	Branch if bit test indicator false
BIOT	Branch if I/O indicator true
BIOF	Branch if I/O indicator false
BOV	Branch if R-register overflow
BNOV	Branch if no R-register overflow

SHIFT INSTRUCTIONS

Shift Short	Description
SOL	Single shift open left
SCL	Single shift closed left
SAL	Single shift arithmetic left
DCL	Double shift closed left
SOR	Single shift open right
SCR	Single shift closed right
SAR	Single shift arithmetic right
DCR	Double shift closed right

Shift Long	Description
DOL	Double shift open left
DAL	Double shift arithmetic left
DOR	Double shift open right
DAR	Double shift arithmetic right

INPUT/OUTPUT INSTRUCTIONS

Instruction	Description
IO	Input/output word
IOH	Input/output halfword
IOLD	Input/output load

GENERIC INSTRUCTIONS

Instruction	Description
HLT	Halt
MCL	Call monitor via trap
RTT	Return from trap
RTCN	Real-time clock on
RTCF	Real-time clock off
WDTN	Watchdog timer on
WDTF	Watchdog timer off
BRK	Break trap
MMM	Memory to memory move

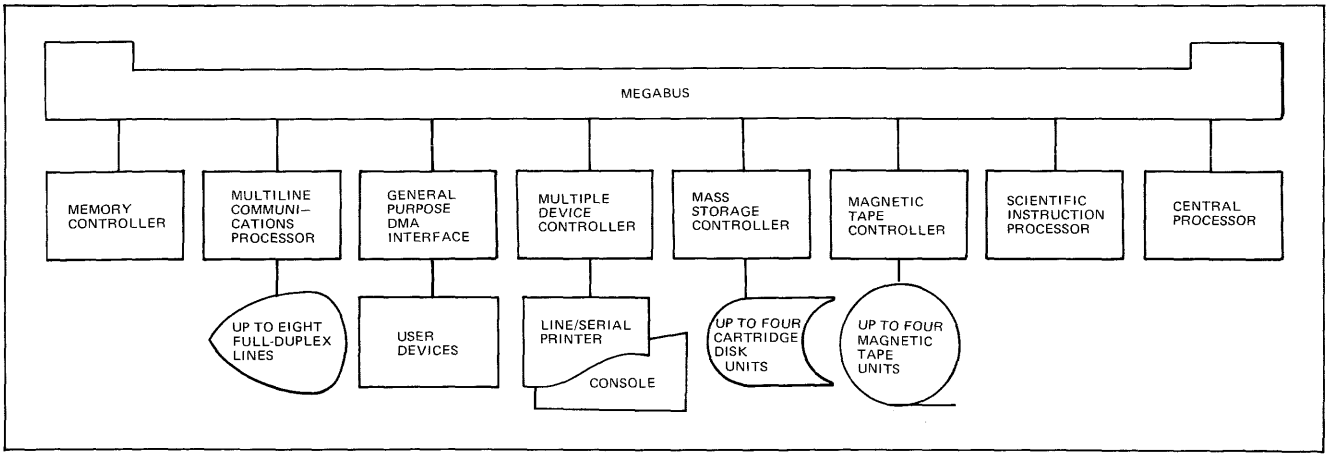


Figure 1. 6/43 System

ASD	Activate segment descriptor
VAL	Validate access rights
QOH	Queue on head
QOT	Queue on tail
DQH	Dequeue from head
DQA	Dequeue on address

SCIENTIFIC INSTRUCTIONS

Single Operand	**Description**
SCZD	Scientific compare to zero two words
SCZQ	Scientific compare to zero four words
SNGD	Scientific negate two words
SNGQ	Scientific negate four words

Double Operand	**Description**
SLD	Scientific load
SST	Scientific store
SCM	Scientific compare
SAD	Scientific add
SSB	Scientific subtract
SML	Scientific multiply
SDV	Scientific divide
SSW	Scientific swap

Scientific Accumulators Branches	**Description**
SBLZ	Branch if SA less than zero
SBGEZ	Branch if SA greater than or equal to zero
SBEZ	Branch in SA equal to zero
SBNEZ	Branch in SA not equal to zero
SBGZ	Branch if SA greater than zero
SBLEZ	Branch if SA less than or equal to zero

Scientific Indicators Branches	**Description**
SBL	Branch if less than
SBGE	Branch if greater than or equal
SBE	Branch if equal
SBNE	Branch if not equal
SBG	Branch if greater than
SBLE	Branch if less than or equal
SBPE	Branch if precision error
SBNPE	Branch if no precision error
SBSE	Branch if significance error
SBNSE	Branch if no significance error
SBEU	Branch if exponent underflow
SBNEU	Branch if no exponent underflow

SPECIFICATIONS

LEVEL 6 MEGABUS: Provides bidirectional asynchronous communications path between all boards
Cycle Time – 300 nanoseconds
Throughput – up to three million words per second
Slots – up to 23

CENTRAL PROCESSOR: interrupt-driven; processes bits, bytes, words, and multiwords; real-time clock; ROM bootstrap loader; basic or full control panel; multiply/divide hardware; watchdog timer
Addressing modes – direct (up to one million words); indirect; base plus displacement; base plus displacement indirect; base plus index; base plus indirect index; base plus index push/pop; base push/pop; program counter

plus displacement; program counter plus displacement indirect; indexed; direct register operand; immediate operand; and interrupt vector plus displacement

Registers – 24

Interrupt Levels – 64 (vectored), allowing interrupts to be set at the channel level

Options – vertical panel mounting: Memory Management Unit

MEMORY: Expands in 8K modules with single-fetch and 16K modules with double-fetch memory

Type – 4K N-channel, MOS

Cycle Time – 550 nanoseconds with double-fetch memory; 650 nanoseconds with single-fetch memory

Options – Memory Save and Autorestart; EDAC (Error Detection and Correction); core memory; single-fetch or double-fetch

MULTILINE COMMUNICATIONS PROCESSOR (MLC9101): Controls up to eight synchronous or asynchronous full-duplex lines or up to four synchronous broadband full-duplex lines or up to four HDLC full-duplex lines

Type – programmable

Interfaces – EIA RS232C, MIL 188C, Broadband CCITT V35, direct connect, Bell 301/303

Throughput – up to 20,000 characters per second

MULTIPLE DEVICE CONTROLLER (MDC9101): Controls up to four devices using Device-Pacs (i.e., adapters)

Type – four levels of simultaneity

Throughput – 32,500 words per second

MASS STORAGE CONTROLLER (MSC9101): Controls up to four disk units with total capacity from 2.5 to 44.8 million bytes

Type – one data transfer operation concurrent with multiple seek operations

MAGNETIC TAPE CONTROLLER (MTC9101): Controls up to four magnetic tape units or up to two magnetic tape units and two unit record devices

Type – Up to three levels of simultaneity (i.e., tape and 2 unit record devices)

Throughput – Up to 100K bytes per second

SCIENTIFIC INSTRUCTION PROCESSOR (CPF9503): Operates on a powerful set of 30 scientific instructions which includes arithmetic operations on single and double precision floating point operands, and single and double word integer operands (64-bit hardware data paths)

Registers – 3 double precision accumulators

MEMORY MANAGEMENT UNIT (CPF9501): Permits allocation/assignment of memory among various users and provides for segmentation and Read/Write/Execute protection based on rings of privilege.

Location – resides in the central processor

GENERAL PURPOSE DMA INTERFACE (GIS9001): Provides user interface point for attachment of user-designed adapters

Type – single level of simultaneity

Throughput – 500,000 words per second (memory-to-user device or opposite direction)

Specifications may change as design improvements are introduced.

Honeywell

Honeywell Information Systems
In the U.S.A.: 200 Smith Street, MS 486, Waltham, Massachusetts 02154
In Canada: 2025 Sheppard Avenue East, Willowdale, Ontario M2J 1W5
In Mexico: Avenida Nuevo Leon 250, Mexico 11, D.F.

17207, 51276, Printed in U.S.A.

AX40, Rev. 0