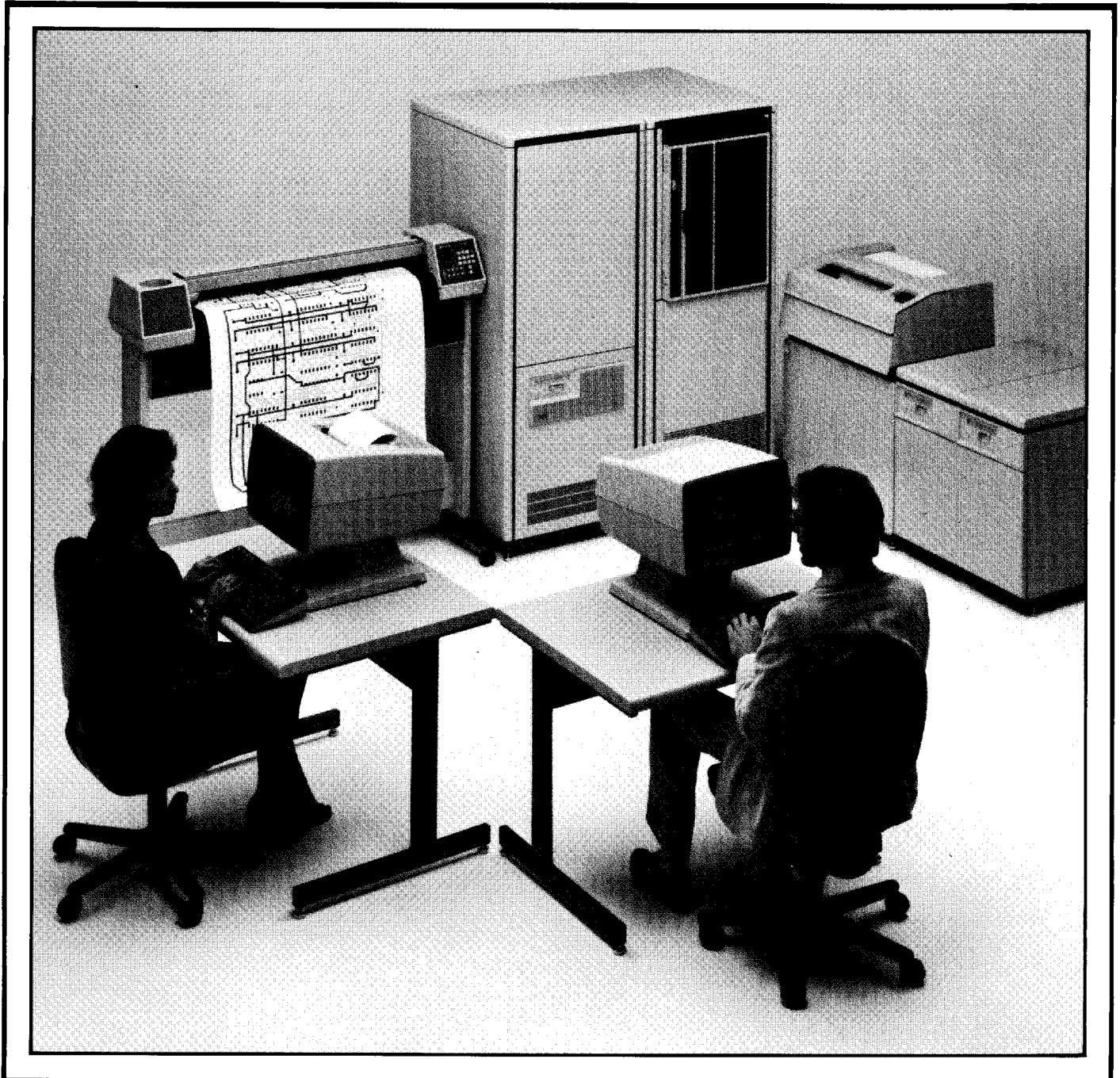# HP 1000 Computer Systems

HP 1000 E/F-Series Hardware Technical Data

Documentation Map for HP 1000 Data Books

I/O Architecture	Centralized Intelligence	Distributed Intelligence
Series	E/F	A/L
Systems and Computers	HP 1000 E/F-Series Hardware Technical Data Book	HP 1000 A/L-Series Hardware Technical Data Book
Interfaces	HP 1000 E/F-Series Interfaces Data Book	HP 1000 A/L-Series Interfaces Data Book
Software	HP 1000 Computer Systems Software Technical Data Book	
Communications	HP 1000 Computer Systems Communications Products Technical Data Book	
Peripherals	HP 1000 Peripherals Selection Guide	
Measurement and Control	HP 2250 Measurement and Control Processor Technical Data	
	HP 2240 Measurement and Control Processor Technical Data	
		Control/1000 Technical Information Package

NOTE: *Data Book Supplements containing new or revised information are sometimes printed between data book revisions. Ask your Hewlett-Packard representative for the current data book or supplement in your area of interest.*

HP 1000 E/F-Series Information Locator

Overview

E/F-Series Systems

E/F-Series Computers, I/O Extender, and Power Fail Recovery Systems

Memory Systems

Active Mainframe Plug-Ins

Active Firmware Products and User Microprogramming Accessories

General Reference Information

Alphabetical and Product Number Indexes are on the rear of this page.

Alphabetical Index

Product Number Index

HP 1000 Computers Overview

The HP 1000 Computers comprise a powerful, modular family of general-purpose small computers that are especially well suited for real-time applications that demand high performance. The HP 1000 family includes a broad range of processors which feature fast, reliable semiconductor memory systems, and multi-user, multiprogramming, Real-Time Executive (RTE) operating systems. The family also includes processors which meet your user-microprogramming needs.

The five members of the HP 1000 family are the A-Series, E-Series, F-Series, L-Series, and M-Series. This data book describes the M-, E-, and F-Series, which are a proven line of Centralized Intelligence I/O Architecture computers. The A- and L-Series contain Hewlett-Packard's unique Distributed Intelligence I/O Architecture, and are described in separate data books. See Table 1 for a summary of the HP 1000 computer family.

Table 1. HP 1000 Computer Family Summary

HP 1000 Series	I/O Architecture	HP 1000 Base Instruction Set	Supported Operating Systems	Implementation
M	Centralized Intelligence	Yes	RTE-II, -IVE, -IVB, and RTE-6/VM	Microprogrammed in STTL/MSI and SSI hardware
E	Centralized Intelligence	Yes	RTE-II, -IVE, -IVB, and RTE-6/VM	Microprogrammed in STTL/MSI and SSI hardware
F	Centralized Intelligence	Yes	RTE-IVE, -IVB, -IVB, and RTE-6/VM	Microprogrammed in STTL/MSI and SSI hardware*
A	Distributed Intelligence	Yes	RTE-A	Horizontally Microprogrammed Schottky bipolar LSI
L	Distributed Intelligence	Yes	RTE-L, -XL	Hardwired with SOS/LSI and MSI hardware

Supplemented by the Floating Point Processor.

The Centralized Intelligence HP 1000 computers provide three classes of computing power within a tightly knit, well-integrated family. The M-Series Computers provide the lowest cost Centralized Intelligence power. E-Series Computers provide roughly twice the computing power of M-Series models at a moderate price premium. The F-Series Computers combine the basic processing speed of the E-Series with dedicated hardware for executing floating point instructions, along with instruction set extensions for extremely fast execution of FORTRAN operations

such as array address calculations. Because HP 1000 family members have upward-compatible instruction sets and use many of the same memory systems, I/O interfaces, and power systems, changing from one system to another can be done with minimal reinvestment in software training and spares provisioning.

HP 1000 M/E/F-Series Computers are available in a wide variety of packages to provide the most cost effective solution for your computing need. The basic computers are available in a variety of stand-alone or rack-mountable chassis sizes, complete with power system and many features, such as hardware multiply/divide, that are optional on other computers of the same size. M-Series and E-Series Computers are also available in board versions for high-volume applications where it is useful to integrate the central processor unit into a product to achieve space and power economies.

HP 1000 E- and F-Series Computers also form the basis for complete HP 1000 Computer systems, which combine computer, mass storage, display terminal, operating software, and cabinetry into an integrated, packaged system. See Table 2 for a performance comparison of M-Series, E-Series and F-Series Computers.

Table 2. HP 1000 Computers Performance Comparison

SERIES	M-Series	E & F Series
CONTROL PROCESSOR		
Address space (instr. words)	4,096	16,384
Micro-instruction execution time	325 ns	175/280 ns
MEMORY CYCLE TIME		
Standard performance memory	650 ns	595 ns*
High performance memory		350 ns*
DCPC (Direct Memory Access)		
INPUT RATES TO		
Standard performance memory	1.23Mb/s	1.95Mb/s
Fault control memory	1.23Mb/s	1.88Mb/s
High performance memory		2.28Mb/s
NON-DMS OUTPUT RATES FROM		
Standard performance memory	1.23Mb/s	1.77Mb/s
Fault control memory	1.23Mb/s	1.67Mb/s
High performance memory		2.28Mb/s
DMS OUTPUT RATES FROM		
Standard performance memory	1.23Mb/s	1.67Mb/s
Fault control memory	1.23Mb/s	1.62Mb/s
High performance memory		2.10Mb/s

All memory cycle times quoted for the E and F Series Computers are subject to ±35 ns variation because memory accesses are asynchronous with respect to the CPU in those machines. Dynamic mapping system (DMS) for addressing greater than 64k bytes of memory adds 70 ns (read only) to these cycle times.

EMI Qualified
Model 60 and 65 Computer Systems

The Model 60 and 65 Systems based on the 2178C and 2179C System Processor Units (SPUs) are E- and F-Series Computer Systems that meet FCC and VDE requirements for Electro-Magnetic Interference (EMI). Only EMI-qualifying peripheral devices should be used with the 2178C and 2179C SPUs to insure EMI compliance.

The Model 60 and 65 Computer Systems are managed by the RTE-6/VM Real-Time Executive operating system, which supports multiprogramming, high-level program languages, virtual memory and sharable extended memory areas for data, data base management, distributed systems networking, graphics software, manufacturing applications software, and memory up to 2 megabytes.

The SPU hardware consists of the E-Series or F-Series Computer with 256k bytes of high performance memory (expandable to 2 megabytes), system console interface and option-specified disc interface, and 10 I/O channels available for the addition of other interfaces. The computer is housed in a 1.6m (63-in.) high cabinet with rack space available for a 7906MR+025 or 79xxR system disc and a 12979B+001 I/O Extender.

To the SPU, users must add a system console and a CS/80 or MAC disc and they may also add other peripherals as needed for their applications. Multiple CS/80 discs with 16.5, 28.1, 65.6, 132.1 or 404 megabyte capacity (up to 3.2 gigabytes via the two CS/80 interfaces that are supportable in the RTE-6/VM primary system) and/or MAC discs with 19.6, 50 or 120 megabyte capacity (up to 1.9 gigabytes via the two MAC disc interfaces that are supportable in the primary system) can be used on the system.

Features

- Integrated system building block for OEMs and end users designing their own E/F-Series based application products
- 1.6m cabinet with rack space for 7906MR or 79xxR disc and an I/O Extender
- Real-time multiprogramming executive operating system
- Choice of program languages (FORTRAN 77, Pascal, BASIC, and Macroassembler) plus interactive screen editor, relocating loader, and Symbolic Debug/1000 to support program development
- Support for Image/1000 Data Base Management, Graphics/1000-II software, DS/1000-IV Distributed Systems Networking, and process monitoring and other manufacturing applications software
- Choice of 16.5, 28.1, 65.6, 132.1, or 404M bytes of CS/80 disc memory, expandable to 3.2G bytes via two disc interfaces or 19.6, 50, or 120M bytes of MAC disc memory, expandable to 1.9 gigabytes via two disc interfaces
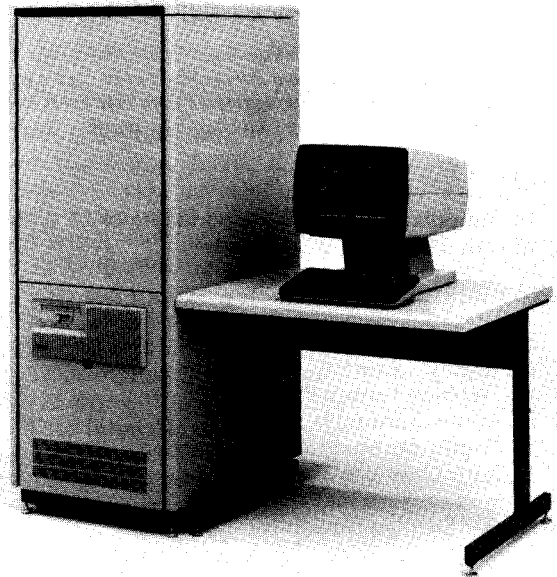
- Virtual memory for data arrays up to 128 megabytes, divided between main memory and disc
- Multiple sharable Extended Memory Areas (EMAs) for data arrays up to 1.9 megabytes resident in main memory. Up to 8 EMAs are supportable, each sharable by as many as 256 programs
- Built-in dynamic mapping system, memory protect, time base generator, and self test
- Power fail detection and auto restart
- On-line system generation
- Boot loaders for boot-up from CS/80 or MAC disc, 264x minicartridges, and mag tape
- A wide choice of interfaces in addition to the standard serial terminal and disc interfaces
- Meets UL, CSA, and IEC safety standards and FCC and VDE EMI standards

Functional specifications

Computer Memory

256k bytes of high performance parity memory, optionally replaceable with up to 2.048M bytes of high performance parity (12788H) or fault control (12789M) memory.

Disc Memory

CS/80 Discs: 16.5, 28.1, 65.6, or 132.1M byte fixed disc with built-in cartridge tape backup or 404M byte fixed or removable media disc without tape backup. Up to four discs per interface.

Multi-Access Controller Discs: 19.6, 50, or 120M byte removable media discs, up to eight discs per interface.

Disc interfaces per system: Drivers for two CS/80 and two MAC disc interfaces are configured into the RTE-6/VM primary system. Drivers for more interfaces can be generated into the system to support more disc capacity (up to 20 gigabytes with multiple 793xH discs).

NOTE: The ability to connect multible disc interfaces to the system does not necessarily mean that two disc interfaces can access memory simultaneously via DCPC. If the aggregate data rate exceeds the capability of the memory system, data loss can result.

Available I/O Channels

Ten in computer mainframe, expandable to 26 with 12979B+001 Dual-Port I/O Extender.

Compatible System Consoles

2621B Interactive Terminal**
2622A Display Terminal*
2623A Graphics Terminal*
2624B Display Terminal*
2626A Display Station*
2627A Color Graphics Terminal*
2635B Printing Terminal**
2645A+007 Display Station†

* *Requires 2178C/2179C cable option 005. EMI qualification is pending on some of these terminals at time of publication of this data book; check with your Hewlett-Packard Sales Representative concerning EMI qualification status.*

** *Requires 2178C/2179C cable option 006.*

† *Requires 2178C/2179C cable option 007.*

Capacity and Performance of Discs (at least one disc is required with 2178C/2179C)

Product Number	Type	Cap. (Mb)	Average Transfer Rate*	Average Access Time
CS/80 DISCS				
7908R	Fixed w/backup	16.5	537kb/s	50ms
7911R	Fixed w/backup	28.1	983kb/s	35ms
7912R	Fixed w/backup	65.6	983kb/s	35ms
7914R/TD	Fixed w/backup	132.1	983kb/s	36ms
7933H**	Fixed	404.4	1.2Mb/s	31.6ms
7935H**	Removable Media	404.4	1.2Mb/s	31.6ms
MULTI-ACCESS CONTROLLER DISCS				
7906M	Removable Media	19.6	740kb/s	33.3mx
7906MR+025†	Removable Media	19.6	740kb/s	33.3ms
7920M**	Removable Media	50.1	740kb/s	33.3ms
7925M**	Removable Media	120.1	740kb/s	36.1ms

* *Average transfer rate is based on the minimum time required to transfer one track without overrun.*

** *This disc requires a 7970E Magnetic Tape Unit or another compatible 79xxR/M/MR disc for system backup, or (with the 7933H/ 7935H disc) for the loading of system software.*

† *Also requires 2178C/2179C cabinet option 050.*

Diagnostic and Utility Loading Requirement

An HP 264x+007 Terminal or HP 7970B/E Mag Tape Unit is required to be available on-site for users who wish to have the ability to load and run diagnostics and/or use the off-line backup utility.

Electrical specifications

Power Requirements of 2178C/2179C System Processor Unit

SPU and Disc Line Voltages and Line Frequencies:

Product Number	Line Voltage	Line Freq.
SPUs (exclusive of disc)		
2178C Standard	120V −23%/+10% (88-132V)*	48 - 66 Hz
Opt 015	220V −20%/+20% (176-264V)	48 - 66 Hz
2179C Standard	120V −10%/+10% (108-132V)*	48 - 66 Hz
Standard†	100V −10%/+10% (90-110V)†	48 - 66 Hz
Opt 015	220V −10%/+10% (198-242V)	48 - 66 Hz
Opt 015‡	240V −10%/+10% (216-264V)‡	48 - 66 Hz
DISCS		
7908R Standard	115V −23%/+10% (88-127V)	47.5 - 66 Hz
Opt 015	230V −22%/+10% (180-255V)	47.5 - 66 Hz
All Standard	120V −10%/+5% (108-126V)	54 - 66 Hz
other Standard†	100V −10%/+5% (90-105V†	54 - 66 Hz
79xx Opt 015	220V −10%/+5% (198-231V)	47.5 - 55 Hz
Discs Opt 015‡	240V −10%/+5% (216-252V)‡	47.5 - 55 Hz

* *2178C/2179C standard System Processor Unit requires split-phase input with the line voltage listed here applied to both phases.*

† *100V/60 Hz is provided by restrapping a Standard unit at time of installation.*

‡ *240V/50 Hz is provided by restrapping Option 015 unit at time of installation.*

Maximum operating current: 16A per phase for 2178C/2179C.

Power cable: A 3m (9.8 ft) power cable with NEMA L14-20 plug is furnished with the standard 2178C or 2179C SPU.

Power Requirements of Terminals and Other Peripherals

See Power Requirements table in the HP 1000 Peripherals Selection Guide.

DC Current Available and Required for Interfaces and Accessories

See pages 7-3 and 7-5.

Environmental specifications

2178C/2179C Temperature

Operating (SPU and disc): 10° to 40°C (50° to 104°F).

Maximum rate of change: <10°C (18°F) per hour for 7908R, 7911R, 7912R, 7914R, 7933H, or 7935H Disc, <20°C (36°F) per hour for 7906MR, 7920M, or 7925M Disc.

Non-operating temperature: −40° to 60°C (−40° to 140°F).

Relative Humidity (SPU and Disc)

20% to 80% non-condensing.

Altitude

Operating: To 4.6km (15,000 ft).

Non-operating: To 15.3km (50,000 ft).

Vibration and Shock

HP 2178C/9C System Processor Units are type tested for normal shipping and handling shock and vibration (contact factory for review of any application that requires operation under continuous vibration).

Safety and EMI qualification

Safety Qualification

The Model 60 and 65 Systems meet Underwriter's Laboratory (UL), Canadian Standards Association (CSA), and International Electrotechnical Commission (IEC) safety standards.

EMI Qualification

The Model 60 and 65 Systems based on the 2178C and 2179C SPUs meet Federal Communications Commission (FCC) and Verband Deutscher Elektrotechniker (VDE) standards for Electro Magnetic Interference (EMI).

HP 1000 Model 60 System ordering information

NOTE: A compatible terminal is required for local operator communication with the 2178C SPU and a 79xxR/M/MR/H disc is required for operating system and program development support. These items must be on the same order as the 2178C SPU.

2178C System Processor Unit

The 2178C System Processor Unit includes:

1. 2113E Computer with 128 base set instructions, 264x Terminal Loader ROM, 12791A Firmware Expansion Module, 14 I/O channels (four of which are used by the SPU), space for 10 memory modules, and also equipped with:
   a. 12788BB 256k byte High Performance Memory Package, including 12892B Memory Protect Module and 12731A Memory Expansion Module
   b. 12991B Power Fail Recovery stem.
   c. 12539C Time Base Generator.
   d. 12821A+001 CS/80 Disc Interface or 13175D MAC Disc Interface, as appropriate.
   e. 12897B Dual-Channel Port Controller.
   f. 12966A Buffered Asynchronous Communications Interface with 2178C Option 005, 006, or 007 cable.
   g. 2 x 12777A Priority Jumper Card.
   h. 12992J CS/80 Disc Loader ROM or 12992B RPL-compatible MAC Disc Loader ROM, as appropriate.
   i. 12992D 7970 Mag Tape Loader ROM.
2. 29431F System cabinet with power control unit and anti-tip feet.
3. 92084A RTE-6/VM operating system on user-specified media, including both software and manuals.
4. Off-line diagnostics package on 264x minicartridges.
5. 91711B On-Line System Verification Package on 264x minicartridges.
6. System Installation and Service Manuals.
7. Site preparation consultation.
8. On-site installation and checkout by a Hewlett-Packard Customer Engineer, including integration and test with primary system.
9. 90-day on-site warranty.
10. Ten 93825A Engineering Units.

2178C Options

005: 12966A Option 105 5m (16.4 ft) cable to 262x system console (except 2621B).

006: 12966A Option 106 5m (16.4 ft) cable to 2621B Interactive Terminal or 2635B Printing Terminal as system console.

007: 12966A Option 107 5m (16.4 ft) cable to 264x system console.

014: Deletes 256kb high performance memory (must order at least 256kb of other HP high performance memory).

015: Operation from 220V ac power. Power options for terminal, disc, and other peripherals must be ordered separately.

022: System software on CS/80 cartridge tape.

031: System software on 7906M/MR disc cartridge. (Option 050 is also required for rack mounting of 7906MR+025 disc.)

032: System software on 7920M disc pack.

033: System software on 7925M disc pack.

050: Cabinet adaptation for rack mounting of 7906MR+025 disc.

053: Solid lower door with ventilation cutouts for cabinet of system that does not use a rack-mounted disc.

060: System software on 800 bpi mag tape in CS/80 format and 12821A+001 interface.

061: System software on 1600 bpi mag tape in CS/80 format and 12821A+001 interface.

HP 1000 Model 65 System ordering information

NOTE: A compatible terminal is required for local operator communication with the 2179C SPU and a a 79xxR/M/MR/H disc is required for operating system and program development support. These items must be on the same order as the 2179C SPU.

2179C System Processor Unit

The 2179C System Processor Unit includes:

1. 2117F Computer with Floating Point Processor, Scientific Instruction Set, Fast FORTRAN Processor, plus 128 base set instructions, dynamic mapping instructions, 264x Terminal Loader ROM, 12791A Firmware Expansion Module, 14 I/O channels (four of which are used by the SPU), space for 10 memory modules, and also equipped with:
   a. 12788BB 256k byte High Performance Memory Package, including 12892B Memory Protect Module, and 12731A Memory Expansion Module
   b. 12991B Power Fail Recovery System.
   c. 12539C Time Base Generator.

   d. 12821A+001 CS/80 Disc Interface or 13175D MAC Disc Interface, as appropriate.
   e. 12829A Vector Instruction Set.
   f. 12897B Dual-Channel Port Controller.
   g. 12966A Buffered Asynchronous Communications Interface with 2179C Option 005, 006, or 007 cable.
   h. 2 x 12777A Priority Jumper Card.
   i. 12992J CS/80 Disc Loader ROM or 12992B RPL-compatible MAC Disc Loader ROM, as appropriate.
   j. 12992D 7970 Mag Tape Loader ROM.

2 through 10. Same as 2 through 10 for 2178C, above.

2179C Options

005 through 061: Same as Options 005 through 061 for 2178C, above.

101: VALUE/65 Value Pack with 1M byte memory instead of 256k byte memory and FORTRAN 77 and Pascal compilers, Graphics/1000-II DGL and AGP software, and Image/1000 Data Base Management System on 1600 bpi mag tape. Prerequisites are Option 061 and **NO** Option 014, 031, 032, or 033.

102: VALUE/65 Value Pack similar to Option 101, but with 2M byte memory instead of 256k byte memory. Same prerequisites as Option 101.

121: VALUE/65-II Value Pack similar to Option 101, but with Symbolic Debug/1000 and Image/1000-II instead of Image/1000. Same prerequisites as Option 101.

122: VALUE/65-II Value Pack similar to Option 101, but with 2M byte memory instead of 256k byte memory, Symbolic Debug/1000, and Image/1000-II instead of Image/1000. Same prerequisites as Option 101.

EMI Qualified
Model 40 and 45 Computer Systems

HEWLETT PACKARD

The Model 40 and 45 Systems based on the 2176E and 2177F System Processor Units (SPUs) are E- and F-Series Computer Systems that meet FCC and VDE requirements for Electro-Magnetic Interference (EMI). Only EMI-qualifying peripheral devices should be used with the 2176E and 2177F SPUs to insure EMI compliance.

The Model 40 and 45 Computer Systems are managed by the RTE-IVB Real-Time Executive operating system, which supports multiprogramming, high-level program languages, extended memory area for data, data base management, distributed systems networking, graphics software, and memory up to 2 megabytes.

The SPU hardware consists of the E-Series or F-Series Computer with 256k bytes of high performance memory (optionally replaceable with 512k bytes, expandable to 2 megabytes), system console interface and option-specified disc interface, and 10 I/O channels available for the addition of other interfaces. The computer is housed in a 1.6m (63-in.) high cabinet with rack space available for a 7906MR+025 disc and a 12979B+001 I/O Extender.

To the SPU, users must add a system console and a MAC disc and they may also add other peripherals as needed for their applications. MAC discs with 19.6, 50 or 120 megabyte capacity can be used on the system, with multiple discs capable of providing up to 1920 megabytes via the two interfaces supported in the RTE-IVB primary system.

Features

- Integrated system building block for OEMs and end users designing their own E/F-Series based application products
- 1.6m cabinet with rack space for 7906MR disc and an I/O Extender
- Real-time multiprogramming executive operating system
- Choice of program languages (FORTRAN 4X, Pascal, BASIC, and assembler) plus interactive screen editor, and relocating loader to support program development
- Support for Image/1000 Data Base Management, Graphics/1000-II software, and DS/1000-IV Distributed Systems Networking
- Choice of 19.6, 50, or 120M bytes of MAC disc memory, the latter expandable to 1920M bytes with multiple discs connected via two interfaces
- Extended Memory Area (EMA) for data arrays up to 1.9 megabytes resident in main memory
- Built-in dynamic mapping system, memory protect, time base generator, and self test
- Power fail detection and auto restart
- On-line system generation
- Boot loader for boot-up from MAC disc, 264x minicartridge, or mag tape
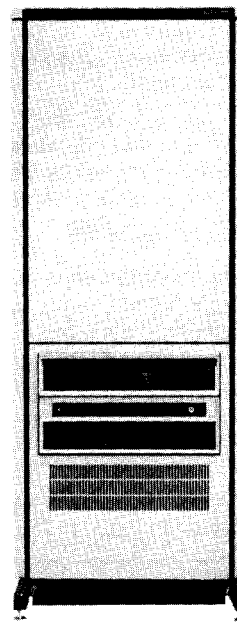
- A wide choice of other interfaces in addition to standard serial terminal and disc interfaces
- Meets UL, CSA, and IEC safety standards and FCC and VDE EMI standards

Functional specifications

Computer Memory

256k bytes of high performance parity memory, optionally replaceable with up to 2M bytes of high performance parity (12788H) or fault control (12789M) memory.

Disc Memory

Disc choices: 19.6, 50, or 120M byte removable media, Multi-Access Controller (MAC) discs, up to eight discs per interface.

Disc interfaces per system: Drivers for two MAC disc interfaces are configured into the RTE-IVB primary system. Drivers for more interfaces can be generated into the system to support more disc capacity.

NOTE: The ability to connect multiple disc interfaces to the system does not necessarily mean that two disc interfaces can access memory simultaneously via DCPC. If the aggregate data rate exceeds the capability of the memory system, data loss can result.

Available I/O Channels

Ten in computer mainframe, expandable to 26 with 12979B+001 Dual-Port I/O Extender.

Compatible System Consoles

2621B Interactive Terminal**
2622A Display Terminal*
2623A Graphics Terminal*
2624B Display Terminal*
2626A Display Station*
2627A Color Graphics Terminal*
2635B Printing Terminal**
2645A+007 Display Station†

* *Requires 2176E/2177F cable option 005. EMI qualification is pending on some of these terminals at time of publication of this data book; check with your Hewlett-Packard Sales Representative concerning EMI qualification status.*

** *Requires 2176E/2177F cable option 006.*

† *Requires 2176E/2177F cable option 007.*

Diagnostic and Utility Loading Requirement

An HP 264x+007 Terminal or HP 7970B/E Mag Tape is required to be available on-site for users who wish to have the ability to load and run diagnostics and/or use the off-line backup utility.

Capacity and Performance of Discs (at least one disc is required with 2176E/2177F)

Product Number	Type	Cap. (Mb)	Average Transfer Rate*	Average Access Time
7906MR+025†	Removable Media	19.6	740kb/s	33.3ms
7906M	Removable Media	19.6	740kb/s	33.3ms
7920M**	Removable Media	50.1	740kb/s	33.3ms
7925M**	Removable Media	120.1	740kb/s	36.1ms

* *Average transfer rate is based on the minimum time required to transfer one track without overrun.*

** *This disc requires a 7970E Magnetic Tape Unit or another compatible 79xxM disc for system backup.*

† *Also requires 2176E/2177F cabinet option 050.*

Electrical specifications

AC Power Requirements of 2176E/2177F System Processor Unit

Maximum operating current: 16A per phase for 2176E/2177F.

Power cable: A 3m (9.8 ft) power cable with NEMA L14-20 plug is furnished with the standard 2176E or 2177F SPU.

DC Current Available and Required for Interfaces and Accessories

See pages 7-3 through 7-5.

SPU and Disc Line Voltages and Line Frequencies:

Product Number	Line Voltage		Line Freq.

SPUs (exclusive of disc)

Product Number		Line Voltage		Line Freq.
2176E	Standard	120V −23%/+10%	(88-132V)*	48 - 66 Hz
	Opt 015	220V −20%/+20%	(176-264V)	48 - 66 Hz
2177F	Standard	120V −10%/+10%	(108-132V)*	48 - 66 Hz
	Standard†	100V −10%/+10%	(90-110V)†	48 - 66 Hz
	Opt 015	220V −10%/+10%	(198-242V)	48 - 66 Hz
	Opt 015‡	240V −10%/+10%	(216-264V)‡	48 - 66 Hz

DISCS

Product Number		Line Voltage		Line Freq.
79xxM	Standard	120V −10%/+5%	(108-126V)	54 - 66 Hz
or	Standard†	100V −10%/+5%	(90-105V)†	54 - 66 Hz
79xxMR	Opt 015	220V −10%/+5%	(198-231V)	47.5 - 55 Hz
	Opt 015‡	240V −10%/+5%	(216-252V)‡	47.5 - 55 Hz

* *2176E/2177F standard System Processor Unit requires split-phase input with the line voltage listed here applied to both phases.*

† *100V/60 Hz is provided by restrapping a Standard unit at time of installation.*

‡ *240V/50 Hz is provided by restrapping Option 015 unit at time of installation.*

Power Requirements of Terminals and Other Peripherals

See Power Requirements table in the HP 1000 Peripherals Selection Guide.

Safety and EMI qualification

Safety Qualification

The Model 40 and 45 Systems meet Underwriter's Laboratory (UL), Canadian Standards Association (CSA), and International Electrotechnical Commission (IEC) safety standards.

EMI Qualification

The Model 40 and 45 Systems based on the 2176E and 2177F SPUs meet Federal Communications Commission (FCC) and Verband Deutscher Elektrotechniker (VDE) standards for Electro-Magnetic Interference (EMI).

Environmental specifications

2176E/2177F Temperature

Operating (SPU and disc): 10° to 40°C (50° to 104°F).

Maximum rate of change: <20°C (36°F) per hour for 7906M/MR, 7920M, or 7925M Disc.

Non-operating temperature: −40° to 60°C (−40° to 140°F).

Relative Humidity (SPU and 79xxM/MR Disc)

20% to 80% non-condensing.

Altitude

Operating: To 4.6km (15,000 ft).

Non-operating: To 15.3km (50,000 ft).

Vibration and Shock

HP 2176E/2177F System Processor Units are type tested for normal shipping and handling shock and vibration (contact factory for review of any application that requires operation under continuous vibration).

Physical characteristics

Dimensions

1.6m (63.4 in.) high, 63.5cm (25 in.) wide, 81.3cm (32 in.) deep.

Weight

2176E SPU only (without disc): 164.1kg (361 lb).

2177F SPU only (without disc): 190.5kg (381 lb).

7906MR Disc adds: 109.5kg (241 lb).

7906M Disc: 151.8kg (334 lb).

7920M Disc: 155kg (341 lb).

7925M Disc: 155.9kg (343 lb).

Ventilation

For rack-mounted system disc: Perforations in the cabinet facilitate front-to-rear ventilation provided by fans in the system disc.

For computer and I/O Extender in upper section of SPU cabinet: Four fans at the top rear of the system cabinet exhaust air drawn in through a filter at the bottom rear of the upper section, providing a bottom-to-top airflow of approximately 11.3 cubic metres per minute (400 CFM). The actual value of air flow depends upon the configuration of equipment racked in the upper section of the cabinet.

HP 1000 Model 40 System ordering information

NOTE: A compatible terminal is required for local operator communication with the 2176E SPU and a 79xxM/MR disc is required for operating system and program development support. These items must be on the same order as the 2176E SPU.

2176E System Processor Unit

The 2176E System Processor Unit includes:

1. 2113E Computer with 128 base set instructions, 264x Terminal Loader ROM, 12791A Firmware Expansion Module, 14 I/O channels (four of which are used by the SPU), space for 10 memory modules, and also equipped with:
   a. 12788BB 256k byte High Performance Memory Package, including 12892B Memory Protect Module and 12731A Memory Expansion Module
   b. 12991B Power Fail Recovery System.
   c. 12539C Time Base Generator.
   d. 13175D MAC Disc Interface.
   e. 12897B Dual-Channel Port Controller.
   f. 12966A Buffered Asynchronous Communications Interface with 2176E Option 005, 006, or 007 cable.
   g. 2 x 12777A Priority Jumper Card.
   h. 12992B RPL-compatible MAC Disc Loader ROM.
   i. 12992D 7970 Mag Tape Loader ROM.
2. 29431F System cabinet with power control unit and anti-tip feet.
3. 92068A RTE-IVB operating system on user-specified media, including both software and manuals.
4. Off-line diagnostics package on 264x minicartridges.
5. 91711B On-Line System Verification Package on 264x minicartridges.
6. System Installation and Service Manuals.
7. Site preparation consultation.
8. On-site installation and checkout by a Hewlett-Packard Customer Engineer, including integration and test with primary system.
9. 90-day on-site warranty.
10. Ten 93825A Engineering Units.

HP 1000 Model 45 System ordering information

NOTE: A compatible terminal is required for local operator communication with the 2177F SPU and a 79xxM/MR disc is required for operating system and program development support. These items must be on the same order as the 2177F SPU.

2177F System Processor Unit

The 2177F System Processor Unit includes:

1. 2117F Computer with Floating Point Processor, Scientific Instruction Set, and Fast FORTRAN Processor, plus 128 base set instructions, dynamic mapping instructions, 264x Terminal Loader ROM, 12791A Firmware Expansion Module, 14 I/O channels (four of which are used by the SPU), space for 10 memory modules, and also equipped with:
   a. 12788BB 256k byte High Performance Memory Package, including 12892B Memory Protect Module, and 12731A Memory Expansion Module
   b. 12991B Power Fail Recovery System.
   c. 12539C Time Base Generator.
   d. 13175D MAC Disc Interface.
   e. 12824A Vector Instruction Set.
   f. 12897B Dual-Channel Port Controller.
   g. 12966A Buffered Asynchronous Communications Interface with 2177F Option 005, 006, or 007 cable.
   h. 2 x 12777A Priority Jumper Card.
   i. 12992B RPL-compatible MAC Disc Loader ROM.
   j. 12992D 7970 Mag Tape Loader ROM.
2 through 10. Same as 2 through 10 for 2176E, above.

2176E/2177F Options

005: 12966A Option 105 5m (16.4 ft) cable to 262x system console (except 2621B).

006: 12966A Option 106 5m (16.4 ft) cable to 2621B Interactive Terminal or 2635B Printing Terminal as system console.

007: 12966A Option 107 5m (16.4 ft) cable to 264x terminal as system console.

014: Deletes 256kb high performance memory (must order at least 256kb of other HP high performance memory).

015: Operation from 220V ac power. Power options for terminal, disc, and other peripherals must be ordered separately.

031: System software on 7906M/MR disc cartridge.

032: System software on 7920M disc pack.

033: System software on 7925M disc pack.

Definition of the Primary Operating System

HP 1000 Computer Systems

The primary operating system provided with HP 1000 Computer Systems is an operating system that is configured with the essential software required in most systems. This primary is a ready-to-use system that provides programming access to the major system features (languages, utilities, common I/O devices). It can also be used as the basis for generation of a custom-configured operating system. In addition to providing a common starting point, the primary can be used at any time to verify that the HP 1000 Computer System will function as it did when it was installed.

Objective of the primary system

The major objective behind the primary concept is to provide the HP 1000 Computer System user with a "getting started" software generation, recognizing that most users may regenerate their system several times to optimize it for their particular application. This getting started primary is included in the price of the HP 1000 Computer System. However, regeneration of the system software is not included in the system price and, therefore, must be quoted separately for users not wishing to do it themselves.

Model 40 and 45 primary systems

Model 40 and 45 primaries are supplied with the configuration that is appropriate for the disc that is ordered for the system. The primary includes the components that are common to most HP 1000 Model 40 and 45 Systems. It is intended to demonstrate to the user the functionality of those hardware and software components that are common to most Model 40 and 45 systems.

Only the primary system (hardware and software components) is system tested at the factory. Add-on I/O cards and peripherals ordered with the system are not installed at the factory. They remain packaged separately and are shipped separately (from other divisions).

The user will receive three 7906 disc cartridges or two 7920 or 7925 disc packs, depending upon the disc drive selected for the system. The first disc is the "grandfather" disc. The second disc is the primary system disc generated and tested at the factory. The third disc cartridge is blank.

Model 60 and 65 primary systems

Model 60 and 65 primary systems are similar to Model 40 and 45 primary systems as described above, but the primary is part of the RTE-6/VM operating systems and not just part of the computer system as with the Models 40 and 45. Also, there is a further choice of media for CS/80 fixed discs. If the CS/80 disc option is selected for a Model 60 or 65 system, a single 7908/11/12/14 compatible cartridge tape of the primary system is supplied. At installation, the primary system is loaded into the 7908/11/12/14 system disc.

Devices and programs supported in the primary systems

Models		Supported Devices and Programs
40 & 45	60 & 65	
X	X	Time Base Generator
		System disc driver (one of the following)
A	A	– 7906M/20M/25M MAC disc driver DVR32 or
A	A	– 7906H/20H/25H ICD driver DVA32 or
	A	– 7908/11/12/14/33/35 CS/80 disc driver DVM33
X	X	System console (264x/262x/2635/2382) driver DVA05
X	X	Eight-channel multiplexer (12792A) drivers DVM00, PVM00, DDV05, DDV12, and &DVTB
X	X	HP-IB interface (59310B) driver DVA37
X	X	Line printer (2617A, 2619A & 2631A/B) driver DVA12
X	X	Line printer (2608A) driver DVB12
X		Printer (9876A) driver DVR37
X	X	Mag Tape (7970B/7970E/7971A) driver DVR23
X	X	Terminals and punched tape I/O driver DVR00
X	X	Multipoint terminal (2645A, 2648A, 2624B, and 2626A) driver DVR07
X	X	File manager
X	X	Relocating loader
	X	Multi-level segmentation loader
X	X	Edit/1000
X	X	Interactive editor
X		FORTRAN-IV compiler
X		RTE-IVB Assembler
	X	Macro/1000 Assembler
X		Cross-Reference Table Generator
X	X	System Switch Program (SWTCH)
X	X	On-line system generator
X	X	Softkey programs
X	X	RTE Utilities
X	X	System Test Programs
X		BASIC/1000D*
X		Image/1000*
X	X	DS/1000-IV*

A = Alternate item; only the selected system disc has an assigned LU and track map table on its primary disc.

*These items are located in file manager type 6 files on the primary system and are purged during system integration if not ordered with the HP 1000 Computer System.

E/F-Series Specifications

This data sheet provides specifications for the 2109E, 2113E, and 2117F computers. All specifications apply to each of these computers, unless otherwise noted. Product descriptions and ordering information can be found in the individual product data sheets.

M-Series data sheets are located in the Mature Products section of this data book. The 2111F computer will not be available after mid-1982, and its data sheet has been omitted from this data book. For information concerning the 2111F, please retain your previous HP 1000 Hardware data book.

Functional specifications

Processor architecture

Implementation: Microprogrammed in MSI and SSI hardware

Data path width: 16 bits

Standard registers:
Accumulators: 2 (A and B), 16 bits each, addressable as registers or memory locations
Index: 2 (X and Y), 16 bits each
Memory control: 3 (T,P) 16 bits each; (M), 15 bits
Supplementary: 2 (overflow and extend), 1 bit each
Manual data: 16-bit (display)

Instruction types:
Memory-to-accumulator   Accumulator-to-I/O
Memory-to-memory   Device control
Direct register modification

Instruction expansion: 176 instruction codes are available to the microprogrammer for instruction set additions.

Addressing modes:
Direct   Double word
Multi-level indirect   Single word
Indexed   Byte
Indirect indexed   Bit
Register implicit

Bus structure: Separate memory data, memory address, and I/O buses tied to the unified internal S Bus

Memory structure: 32 pages of 2048 bytes, with direct access to current or base page (page 0) pages; indirect or indexed access to all pages

Memory expansion: Paged memory address space expandable to 1024 pages of 2048 bytes using the Dynamic Mapping System

Input/Output: Vectored priority interrupt structure for up to four system devices and 46 I/O devices, such as DCPC, power fail, parity, and memory protect.

Control processor

Implementation: Hardwired MSI and SSI TTL

Instruction execution time: Variable, 175 or 280 nsec

Control path: 24 bits

Data path: 16 bits

Registers:
Standard registers: 6 (A,B,X,Y,P,S)
Scratch registers: 12 16-bit registers accessible to the microprogrammer
Iteration counter: 8 bits
Instruction register: 16 bits
Latch register: 16 bits
Status flag: 1 bit
Subroutine levels stack: 3 - 14 bits each

Instruction formats:
TYPE 1 Data transfer and modification
TYPE 2 Constant formation
TYPE 3 Conditional branch
TYPE 4 Unconditional branch

Bus structure: Unified single bus with program access to memory data, memory address, and I/O buses.

Bus speed: 11.4M bytes/sec.

Control memory structure:
Type: Bipolar LSI semiconductor R/W or ROM
Address space: 16,384 words; 64 modules of 256-words each
Word size: 24 bits
Cycle time: Variable, 175 or 280 nsec

Module assignments

F-Series:
(1 module = 256 words of control memory)
0 - 3   assigned to F-Series base instruction set, including Floating Point Processor instructions.
4 - 11   Reserved for HP enhancements.
12 - 15   Reserved for Vector Instruction Set.
16 - 17   Reserved for HP enhancements.
18 - 27   RTE-6/VM Operating System instructions.
28 - 31   Available for user microroutines.
32   Reserved for Dynamic Mapping Instructions.
33 - 35   Reserved for Fast FORTRAN Processor.
36 & 37   Reserved for RTE-IVB Extended Memory Area (EMA) or RTE-6/VM EMA/VMA mapping instructions.
38 & 39   Reserved for DS/1000 firmware.
40 - 43   Reserved for Scientific Instruction Set.
44 & 45   Reserved for HP enhancements.
46 - 63   Available for user microroutines.

E-Series:

(1 module = 256 words of control memory)

0 - 3	Assigned to E-Series base instruction set
4 - 31	Available for user microroutines
32	Reserved for DMS instructions
33 - 35	Reserved for Fast FORTRAN Processor
36 & 37	Reserved for RTE-IVB Extended Memory Area (EMA) orRTE-6/VM EMA/VMA mapping instructions
38 & 39	Reserved for DS/1000 firmware
40 - 43	Reserved for future HP instruction set enhancements
44 & 45	RTE-6/VM Operating System instructions
46 - 63	Reserved for user microroutines

Control processor instructions: 211 total; up to 5 may be combined in 1 instruction.

E/F-Series:

Operations: 15 total.
Special: 32 total.
ALU and conditional: 68 total.
Store (destination): 32 total.
S-bus (source): 32 total.
Reverse Sense: 32 total.

Loader protection

All loaders reside in special ROM's on the CPU board. The loader routines are assembly code routines which are loaded into the last 64 words of main memory by activating front panel switches. Four switch-selectable loader spaces are provided to accommodate four different loader routines. User-generated loaders may be written in assembly language, written into PROMS, and mounted in any of the four available sockets on the CPU board.

Volatility protection

AC standby mode and sustaining power for line loss of 8 milliseconds before entering power fail routine. Power fail recovery system provides a minimum of 1.6 hours of battery-supplied memory standby power.

Memory parity check

Monitors all words read from memory. Utilizes 17th bit in memory. Switch programmable to halt, interrupt, or ignore parity error when detected. Interrupt on error requires memory protect option. Indication of a parity error is displayed by a light on the front panel.

Approximate instruction execution times for E/F-Series Computers

Instruction	Execution Time (μsec) in F-Series
Single-precision Floating Point (32 bit) Instructions (8 total)	
Add/Subtract	7.7
Multiply	6.4
Divide	9.3
Conversion to single integer	5.3
Conversion to double integer	6.3
Conversion from single integer	4.6
Conversion from double integer	5.7
Extended-precision Floating Point (48 bit) Instructions (8 total)	
Add/Subtract	13.8
Multiply	13.0
Divide	17.4
Conversion to single integer	6.8
Conversion to double integer	8.7
Conversion from single integer	6.6
Conversion from double integer	8.1
Double-precision Floating Point (64 bit) Instructions (8 total)	
Add/subtract	14.9
Multiply	13.7
Divide	19.7
Conversion to single integer	7.3
Conversion to double integer	9.2
Conversion from single integer	7.0
Conversion from double integer	8.5
Single-Precision (32 bit) Scientific Instruction Set Instructions (9 total)	
SIN (Sine) function	51.8
COS (Cosine) function	52.0
TAN (Tangent) function	53.7
ATAN (Arc Tangent) function	52.6
TANH (Hyperbolic Tangent) function	66.5
SQRT (Square Root) function	37.8
EXP (e_x) function	51.9
ALOG (Natural Logarithm) function	46.3
ALOGT (Base 10 Logarithm) function	52.6
Double-Precision (64 bit) Scientific Instruction Set Functions♦	
SIN (Sine) function	217.0
COS (Cosine) function	217.0
TAN (Tangent) function	212.0
ATAN (Arc Tangent) function	189.0
TANH (Hyperbolic Tangent) function	211.0
EXP (e_x) function	219.0
SQRT (Square Root) function	135.0
ALOG (Natural Logarithm) function	179.0
ALOGT (Base 10 Logarithm) function	214.0

♦The double-precision Scientific Instruction Set functions are a combination of firmware (approximately 90%) and software (approximately 10%); the software is included in the relocatable libraries of all compatible RTE operating systems.

Fault control memory and dynamic mapping system may each add 0 to 0.2 microsecond to these instruction execution times.

Asynchronous memory may cause variations of ±0.035 microseconds per memory reference.

More detailed instruction times are supplied in the HP 1000 F-Series reference manual (02111-90001).

The maximum non-interruptible time for any instruction is 12.2 milliseconds.

All execution times are worst case figures.

Approximate instruction execution times for E/F-Series Computers (Continued)

Instruction	Execution Time (μsec) in F-Series
Double Integer (32 bit) Instructions	
Add	4.9
Subtract	5.7
Multiply	19.2
Divide	24.4
Reverse-order subtract	6.5
Reverse-order divide	24.4
Negate	2.3
Increment (A, B)	2.0
Decrement (A, B)	2.5
Increment and skip if zero	5.3
Decrement and skip if zero	5.1
Compare	4.4
Polynominal Evaluation Instruction	
Set-up time	19.0+
Additional time (base on M+N, when M = degree of numerator, N = degree of denominator)	9x(M+N)
Fast FORTRAN Processor Instructions (12 total)	
Moves to new locations:	
– Extended precision variable	12.81
– Address of parameters from calling sequence into subroutine list	13.9 +3.7*NP
Calculate X*2N for real X and integer N	8.4
Unpacking of real variable	3.1
Normalization, rounding, and packing of mantissa of extended precision variable	29.5
Complementing of extended precision variable	12.1
Complementing and normalization of extended precision variable	33.4
Transfer of control to destination of FORTRAN computed GOTO statement	10.6
Computes address of specified element of 2 or 3-dimensional array	27.2
Complementing and normalization of single precision variable	5.1
Complementing and normalization of double precision variable	9.8
Computation of (1−x)/(1+x)	28
Four-word transfer	10.3

Approximate instruction execution times for E/F-Series computers (Continued)

Instruction	Execution Time (μsec) with High Perf Memory E/F-Series	with Std Perf Memory E-Series
Memory reference group (14 total)		
Add/load/AND/IOR/XOR	0.91	1.19
Store	1.26	1.85
Jump	0.74	0.74
Jump to subroutine	1.61	1.85
Compare (normal/skip)	1.09/1.43	1.23/1.72
Increment, skip if zero	1.54/1.61	2.03
Indirect address, per level	0.46	0.575
Register reference group (43 total)		
Normal/skip	0.91/1.26	1.19/1.29
Input/Output group (13 total)		
SFS/SFC/SOS/SOC (normal)	2.28	2.28
SFS/SFC/SOS/SOC (skip)	2.66	2.73
All others	2.28	2.28
Floating point instructions (6 total); (E-Series only)		
Add	27.44	27.65
Subtract	29.22	29.44
Multiply	34.90	35.11
Divide	47.11	47.32
Fix	7.35	7.6
Float	10.82	10.82
Extended instruction group (10 total)		
Integer multiply	6.0	6.72
Integer divide	9.1	9.63
Double load	2.07	3.185
Double store	2.7	3.71
Shift/rotate (basic)	1.47	2.065
Additional per shift	0.175	0.175
Indirect addressing/level	0.81	1.19
Index instructions (32 total)		
Copy	1.29	1.435
Exchange	1.92	2.065
Decrement/increment (normal/skip)	1.75/2.0	2.03/2.52
Load or add index	2.66	3.05
Store index	2.94	3.43
Load indexed	3.19	3.745
Store indexed	3.46	3.815
Jump and load Y	2.67	2.8
Jump and index X	2.28	2.625
Data communications (10 total)		
Load byte	3.36	3.5/3.78
Store byte	3.89	4.45/4.83
Move bytes or words (basic)	3.75	4.27
Additional per byte	4.05	4.235
Additional per word	1.68	1.75
Compare bytes or words (basic)	3.75	4.27
Additional per byte	3.78	3.5/3.78
Additional per word	2.38	2.87
Scan for byte (basic)	1.92	2.17
Additional per byte	2.735	2.735
Set or clear bits	4.48	5.215
Test bits (normal/skip)	4.73/4.94	5.36/5.67

Microprogrammable processor port (E-Series only)

Addressable devices: 2

I/O lines: 16

Control lines: 9

Maximum burst transfer rate: 11.4M bytes/sec for 32 bytes

Maximum continuous transfer rate: 3.18M bytes/sec*

Maximum cable length: 1.2M (4ft), properly terminated

User-microprogram dependent.

Microprogrammable block I/O

I/O control lines: 3 special lines on I/O backplane

NOTE: Requires user-designed I/O cards

Maximum synchronous transfer rate: 2.28M bytes/sec (input); 3.17M bytes/sec (output).*

User-microprogram dependent.

Remote program load

Load device selection: 1 of 9 devices in a 2109E, 1 of 14 devices in a 2113E and 2117F

Loader selection: Choice of RPL-compatible optional loader ROMs.

Operating modes: a) Automatically on power-up; b) Remote forced load with 12966A or 12968A interface (Hardwired); c) Load after certain halts under program control.

Configuration information

Input/output capacity:	2109E	2117F 2113E
I/O channels in mainframe	9	14
With first I/O extender	25	30
With two I/O extenders	41	46
Standard memory:	64 kb	128 kb
Memory capacity: **Memory module spaces**		
In computer only	5	10
In computer and extender	14	19
Max. non-fault control memory*		
In computer only	2.048 Mb	2.048 Mb
In computer and extender	2.048 Mb	2.048 Mb
Max. fault control memory*		
In computer only	1.024 Mb	2.048 Mb
In computer and extender	1.024 Mb	2.048 Mb

Based on use of 512k byte memory modules.

Compatibility

Instruction set: The HP 1000 E/F-Series instruction set is backwards compatible with other HP 1000 computers.

Program: Most programs written for HP 1000 Centralized Intelligence Architecture computers are compatible among the M-, E-, and F-Series computers, except those with timing loop dependence.

Control processor address space

Total address space: 16k 24-bit words.

F-Series:
Net address space available to the user: 5.5k words
WCS overlay address space using 1k WCS boards: 3k**
User PROMs address space using 8k FEM board: 5.5k**

E-Series:
Net address space available to the user: 11.5k words
PROM address space available on option 003 FAB board: 3.5k
WCS overlay space using 1k WCS boards: 3k**
User PROMs address space using 8k FEM boards: 11.5k**

**Mounted on board(s) in I/O backplane, using I/O slots; total cannot exceed net address space available to the user. One 12791A FEM board is standard in E- and F-Series computers.*

Scientific instruction set (F-Series only)

Data Formats: Single and double precision.

Execution times and function definitions: See approximate instruction execution times table.

Accuracy: RMS relative error for the various Scientific Instructioin Set functions is as follows for single precision (sp) and double precision (dp)

Function	RMS Rel. Error (sp)	RMS Rel. Error (dp)	Function	RMS Rel. Error (sp)	RMS Rel. Error (dp)
SIN	9.2E-8	1.2E-16	SQRT	6.7E-8	1.6E-17
COS	7.7E-8	1.3E-16	EXP	3.2E-7	8.8E-17
TAN	1.5E-7	1.9E-16	ALOG	1.2E-7	1.3E-16
ATAN	1.5E-7	2.3E-16	ALOGT	1.6E-7	1.3E-16
TANH	2.2E-7	5.5E-17			

Floating Point Processor (F-Series only)

Floating point data formats:

Single-precision: 32 bits (4 bytes), providing at least 6 significant decimal digits in mantissa
Extended precision: 48 bits (6 bytes), providing at least 11 significant decimal digits in mantissa
Double precision: 64 bits (8 bits), providing at least 16 significant decimal digits in mantissa.

Exponent range: Exponent range: 2^{-128} to 2^{+127} in all floating point data formats; decimal equivalent is approximately $10^{\mp 38}$.

Fixed point data formats:
Single-precision: 16 bits (2 bytes), twos complement integer
Double-precision: 32 bits (4 bytes), twos complement integer

Execution times: See Approximate instruction execution times table

Computation times applicable to direct, chained micro-programming use of the Floating Point Processor: The following computation times apply to directly microprogrammed use of the Floating Point Processor for chained floating point calculations in which intermediate results are not transferred to and from the F-Series Computer memory.

Instruction	Computation Time (μsec)		
	Min.	Typ.	Max.
Single-precision Floating Point Operations (8 total)			
Add/Subtract	0.680	0.860	3.440
Multiply	1.960	2.210	2.460
Divide	2.120	3.010	5.175
Conversion to single integer	0.680	1.380	2.000
Conversion to double integer	0.670	2.450	3.270
Conversion from single integer	0.630	1.250	1.780
Conversion from double integer	0.500	2.330	2.930
Extended-precision Floating Point Operations (8 total)			
Add/Subtract	0.800	1.200	4.480
Multiply	2.750	3.130	3.520
Divide	2.940	4.780	7.900
Conversion to single integer	0.680	1.380	1.850
Conversion to double integer	0.670	2.450	3.270
Conversion from single integer	0.630	1.250	1.780
Conversion from double integer	0.500	2.330	2.930
Double-precision Floating Point Operations (8 total)			
Add/subtract	0.800	1.200	5.580
Multiply	3.550	4.100	4.620
Divide	3.680	7.200	10.70
Conversion to/from single or double integer	Same as for extended precision, listed above.		

Electrical specifications

AC power required

Line voltage: 88-132V (110V ± 20%); 176-264V (220V ± 20%) with option 015. Input line voltage range is easily changed in the field by moving jumper connections.

Note that the 2117F Floating Point Processor voltage selector offers choice of 90-110V (100V ± 10%), 108-132V (120V ± 10%), 198-242V (220V ± 10%), and 216-264V (240V ± 10%) input line voltage ranges.

Line frequency: 47.5-66 Hz.

Maximum power required:
2109E and 2113E: 625W
2117F: 825W

Current available (+) required (−) for memory, I/O interfaces and accessories

See power specifications and applicability summary tables, page 7-3.

Power supply

Storage after line failure: Sustains computer through a line loss of 8 milliseconds when operating at the nominal ac line voltage

Input line overvoltage protection: Circuit breaker protects against surge caused by connecting computer to twice nominal line voltage

Input line transients: Withstands power line transients up to ±500V for 50μsec wide pulse, up to ±1000V for 100 nsec wide pulse, without damage

Output voltage regulation: ±5%, except −2V is ±10%

Output protection: All voltages are protected for over-voltage and over-current

Thermal sensing: Monitors internal temperature and automatically shuts down computer if temperature exceeds specified level.

Safety

Models 2109E, 2113E, and 2117F are recognized by Underwriters Laboratories, Inc., and certified by the Canadian Standards Association (with the exception of option 015).

Physical characteristics

	2117F	2109E	2113E
Panel width, cm (in.)		48.3 (19)	
Behind-panel width, cm (in.)		42.6 (16.75)	
Overall depth, cm (in.)		62.2 (24.5)	
Depth behind panel, cm (in.)		58.4 (23)	
Height, cm (in.)	44.5 (17.50)	22.2 (8.75)	(12.25)
Weight, kg (lb)	50 (110)	20.4 (45)	29.5 (65)
Heat dissipation $\frac{\text{kg-cal}}{\text{hr}}$ $\frac{\text{(BTU)}}{\text{hr}}$	752 (2986)	580 (2303)	580 (2302)
Air flow $\frac{\text{cubic meters}}{\text{minute}}$ $\frac{\text{(cubic ft)}}{\text{minute}}$	11 (390)*	5.7 (200)	7.9 (280)
Ventilation	Air intake is on the left side, facing the computer. Exhaust is on the right hand side.		

2117F air flow includes flow through the computer mainframe and through the floating point processor, which is a separate package.

E-Series Computers

The HP 1000 E-Series computers are intermediate-performance members of the HP 1000 Computer Family. Combining successful HP 1000 architecture with a unique design philosophy, the E-Series has the power to meet tough computing demands.

A comprehensive range of software is available for both models, including compilers, and operating systems. In addition, a full line of HP-manufactured peripherals and data communications interface kits is offered, enabling complete systems to be tailored around these members of the HP 1000 Family.
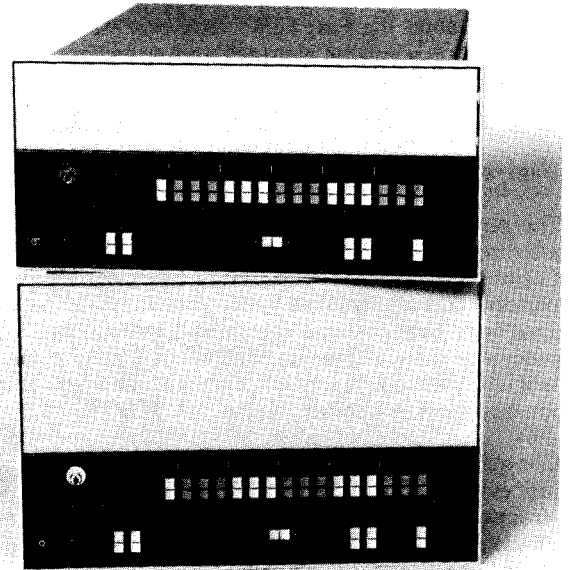
Features

- Proven HP 1000 architecture, providing extensive compatibility with HP 1000 Series processor options, peripherals, operating systems, and software
- Variable microcycle timing (VMT) for improved processor speed
- Powerful instruction set with 128 instructions
- 2.28 million byte/second direct memory access transfer rate available with Dual Channel Port Controller (DCPC)
- User microprogrammable, with complete user-microcode support
- Two models to choose from:
  - 2109E, with space for up to 2M bytes of memory and nine I/O channels in 8-3/4 inch mainframe
  - 2113E, with space for up to 2M bytes of memory and fourteen I/O channels in 12-1/4 inch mainframe
- Standard performance main memory is standard: 64k bytes in 2109E, 128k bytes in 2113E. 350 nanosecond High performance memory and/or fault control capability is optional
- Dynamic mapping system, optional in 2109E, standard in 2113E, provides for accessing up to two megabytes of memory
- Remote program load capability
- Self test for CPU and memory
- Microprogrammable processor port, permitting external processors to be interfaced directly to the E-Series control processor
- Microprogrammable block I/O for intelligent microprogrammed I/O channels
- Disc loader ROM is standard

Description

Architecture

HP 1000 E-Series architecture features a fully micro-programmed processor, which includes all arithmetic functions, I/O, and full operator control panel. Four general-purpose registers are available, two of which may be used as index registers.

Standard E-Series instructions include indexed instructions, integer and floating point arithmetic, data communications, I/O, and a full complement of instructions for logical operations and bit/byte manipulation.

The E-Series offers extensive software program and I/O compatibility with other HP 1000 computers. E-Series processors have been optimized for performance with a microprogrammed control processor that directs operations of the other functional units. The control processor speed has been increased for certain operations by a sophisticated technique that varies microinstruction cycle time, depending on the complexity of the operation.

Efficiency of the microprogrammed routines that determine the machine language operation has also been increased through the mechanisms of instruction and operand prefetch. The CPU-memory interface is totally asynchronous in the E-Series, adding flexibility to the powerful memory structure.

All I/O channels are fully-powered, buffered, and bidirectional. Because of modular design, mainframe memory capacity is completely independent of I/O capacity, so that either memory or I/O modules may be added without taking valuable mainframe space from the other. Mainframe memory capacity is 2M bytes in the 2109E and 2113E.

A full line of I/O interface controllers is available to interface HP-manufactured peripherals, instrumentation, communications devices, or specialized devices.

For applications which demand even higher performance, E-Series users can expand their instruction repetoire with HP-supplied microprogrammed subroutines. Enhancements include the Fast FORTRAN processor for fast handling of scientific routines and operating system mapping routines.

User-microprogramming

The power and flexibility of control processor microprogramming is readily available to E-Series users. Control processor access provides users with the ability to perform commonly-used subroutines 2-to-20 times faster than with conventional computing techniques. Control processor subroutines are written in a simple assembly language, stored in control processor memory, and called directly from Assembly, BASIC, or FORTRAN programs.

Control processor programmers have access to a powerful processor within E-Series computers that executes instructions in 175-to-280 nanoseconds, and provides multilevel nested subroutines, 211 instructions, 12 high-speed scratchpad registers, and an 11.5k word user address space, of which up to 3k words can be writable control store implementing a control processor program overlay arrangement. Control program overlays provide a flexible system able to react to dynamic changes in speed requirements dictated by user program mix.

Control processor program development is aided by HP's complete software development tools, which include an assembler, debug editor, program overlay utility, and PROM tape generator, as well as a complete documentation package.

Memory system

The E-Series includes a standard performance memory system that utilizes the same field-proven semiconductor memory modules as the HP 1000 M-Series. Based on 16k or 64k bit MOS/RAM semiconductor chips, this system combines speed, reliability, and economy. High-speed, 420 ns cycle time memory (without Fault Control) is available to increase performance by up to 30%. For data integrity, memory parity check is standard and fault control capability may be added to improve the MTBF of memory systems. Memory is easily expandable by plug-in 64k, 128k, and 512k byte modules.

For efficient handling of large memory systems, the dynamic mapping system (DMS) is standard. A combination of hardware and control processor programs, DMS is a powerful memory manager that allows E-Series users to address up to 2048k bytes of memory, and provides read and/or write protection of each individual 2,048 byte page.

Four independent memory maps are provided — one for the system, one for the user, and two port controller maps for direct memory access operations. DMS adds 38 powerful memory management instructions to the standard E-Series instruction set. This capability is fully supported by HP's RTE-6/VM and RTE-IVB real-time executive operating systems which offer multi-user access to as many as 64 multi-user program partitions. In RTE-6/VM, support of large-memory systems also gives the user access to data arrays up to 128 megabytes in Virtual Memory.

Input/output

The E-Series I/O system features a multilevel vectored priority interrupt structure. There are 50 distinct interrupt levels, each with a unique priority assignment. Any I/O device can be selectively enabled or disabled or the entire interrupt system (except power fail and parity error interrupts) can be enabled or disabled under program control.

Data transfer between the computer and I/O devices may take place under program control, dual channel port controller (DCPC) control, or microprogram control. The DCPC provides two direct links between memory and I/O devices, and is program-assignable to any two devices. DCPC transfers occur on an I/O cycle-stealing basis, not subject to the I/O priority interrupt structure.

For applications where higher transfer rates are desirable, the E-Series has a special Microprogrammable Block I/O capability that allows transfer rates up to 3.1 million bytes/second. This capability can be implemented through user-designed I/O cards and block I/O control microprograms.

Remote and local program load

The initial binary-loading (IBL) function is easily performed on E-Series computers. For local bootstrap loading, a 64-word ROM-resident IBL program is called by a pushbutton switch on the front panel. Disc loader ROM is standard. Up to two additional HP or user-supplied loader ROMs may be added to any E-Series computer. The user can plug in up to four different loader ROMs if the standard loader ROMs are removed.

Computers at remote sites can be force-loaded from a central location through the use of a remote program load (RPL) capability. Information normally keyed into the front panel is set in switches on the CPU board, so the bootstrapping sequence may be initiated from a remote site, or automatically initiated on power-up from a local peripheral.

Self test

A comprehensive set of diagnostic routines permanently stored in read-only memory (ROM) is standard in the E-Series. Two of these routines, executed each time the IBL/TEST function is executed, provide quick tests of the processor and first 64k bytes of physical memory for verification of operating condition. A third test, executed whenever the machine is powered up, thoroughly tests the processor and all installed memory. This test may also be run manually.

Microprogrammable processor port (MPP)

The microprogrammable processor port provides a direct interface to the CPU for user-designed hardware processors. The MPP provides address, data, and control capability, so external processors can be controlled and can transfer data at burst rates up to 11.4M bytes/second.

Power system

HP 1000 E-Series power systems will operate normally in environments where power fluctuates widely. Input line voltages and frequencies may vary considerably without affecting computer operations. The optional power fail recovery system provides a minimum of 1.6 hours of memory sustaining power for the largest memory configuration, in the event of complete power failure.

Software

The HP 1000 E-Series maintains extensive program compatibility with earlier members of the HP 1000 Family, so users can take advantage of many man-years of software development.

A wide range of operating system software is available. Real-time executive (RTE) systems, available in disc and main memory-resident versions, are multi-programming systems that permit priority scheduling of several real-time programs while concurrent background processing takes place.

The memory-based RTE-M and disc-based RTE-IVB and RTE-6/VM operating systems can support up to 2.048M bytes of memory, managed by DMS. Comprehensive software systems are also available for computer networking.

Languages supported by HP operating systems include FORTRAN 4X, FORTRAN 77, Pascal, HP BASIC, Assembler, and user microprogramming. Utility software includes a debugging routine, a powerful screen editor, and an extensive library of commonly-used computational routines.

E-Series users may also take advantage of a wide variety of thoroughly-tested and documented programs that have been contributed to the HP User Library, PLUS/1000.

Specifications

All E-Series specifications can be found in the E/F-Series Specifications data sheet located at the beginning of this section.

Ordering information

2109E computer

The 2109E includes:

1. 2109B computer
2. 2102B standard performance memory controller and one 12746A 64k byte standard performance memory module
3. 12791A Firmware Expansion Module
4. 02109-90001 HP 1000 E-Series reference manual
5. 02109-90002 HP 1000 E-Series installation and service manual
6. 02109-90014 Microprogramming manual
7. DMI ROMs (13307B) and non-RPL 79xxM Disc Memory and 264x Minicartridge Loader ROMs

2113 computer

The 2113E Computer includes:
1. 2113 computer
2. 12786A 128k byte Standard performance memory package, including 2102B Memory controller, 12747A 128k byte memory module and 12731A Memory Expansion Module and 12892B Memory Protect Module
3-7. Same as items 3 through 7 of 2109E Computer, above.

2109E and 2113E options

003: 13304A Firmware Accessory Board instead of 12791A Firmware Expansion Module

2109E opt. 012: Replaces 64k bytes of standard performance memory with 64k bytes of high performance memory.

2113E opt.012: Replaces 128k bytes of standard performance memory with 64k bytes of high performance memory (deletes 12731A Memory Expansion Module and 12892B Memory Protect Module).

2113E opt. 013: Deletes 64k bytes of memory and Dynamic Mapping System, leaving 64k bytes of memory in computer.

014: Deletes standard memory, item 2, above, from 2109E or 2113E, to permit its replacement with another HP 1000 E-Series compatible standard performance or high performance memory system, with or without fault control, which must be ordered separately.

015: 220V (176-264V) operation

2109E and 2113E accessories

See power specifications and applicability summary on page 8-3, referring to the E-Series applicability column.
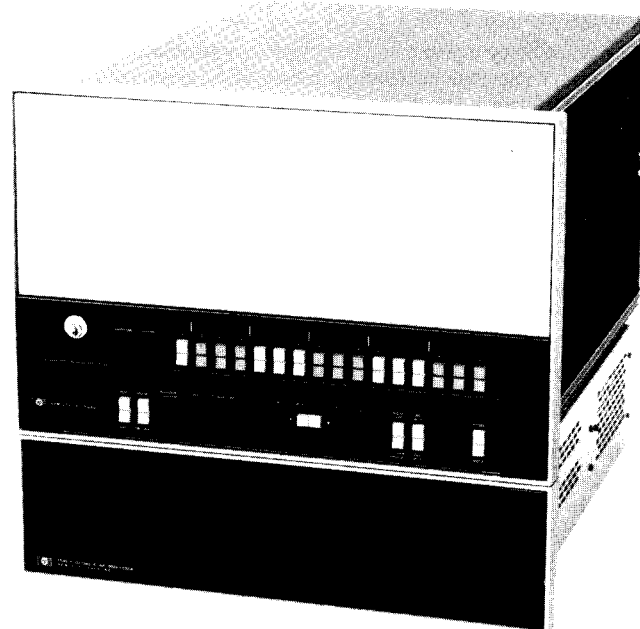
F-Series Computer

The F-Series are the most powerful of the Centralized Intelligence HP 1000 Computers. These machines combine the basic speed of the E-Series Computers with a high-performance Floating Point Processor, Scientific Instruction Set, a polynomial evaluation instruction, double-precision integer instructions, and the FORTRAN accelerator routines of the Fast FORTRAN Processor to provide a high level of processing speed in a compact, economical package. The F-Series Computers are suitable for real-time applications that require exceptional processing speed and extended arithmetic precision. Even more power can be provided for very fast vector and matrix arithmetic by adding the optional Vector Instruction Set.

A comprehensive range of software is available for the F-Series, including program development support software and operating systems. Particularly noteworthy for computational applications involving large data arrays is HP's disc-based RTE-6/VM operating system in which data arrays can be defined up to 128 million bytes in size. For complete information of HP 1000 software, see the HP 1000 Software Technical Data book.

In addition, a full line of HP-manufactured peripherals and data communications interface kits is offered, enabling complete systems to be tailored around this powerful member of the HP 1000 family of computers.

2117F Computer

Features

- **Instruction set extensions, and high speed central and floating point processors provide high performance for computation intensive applications**
- **Scientific Instruction Set for extremely fast computation of trigonometric, logarithmic functions.**
- **Polynomial evaluation instruction**
- **Double integer instructions.**
- **Fast FORTRAN Processor greatly accelerates FORTRAN operations by performing commonly used operations, such as array address calculations at hardware speed**
- **Dynamic mapping system provides for accessing up to 2 megabytes of memory computer plus extender.**
- **High speed direct memory access available via the Dual Channel Port Controller, with transfer rates up to 2.3 million bytes per second**
- **Fully user microprogrammable**
  - **— Complete microprogramming support software available**
  - **— Floating point processor is available as a computing resource to the microprogrammer**
- **Auto bootup and remote program load capability**
- **Self test for CPU and memory**
- **Disc loader ROM is standard**

The HP 1000 F-Series — more processing speed and precision for your computational applications

A hardware-implemented Floating Point Processor, included with the F-Series, slashes processing times for single, extended, and double-precision operations. Single-precision add/subtract takes as little as 4.8 microseconds; multiply/divide as little as 6.1 microseconds. Extended and double precision add/subtract takes 15 microseconds or less, multiply/divide as little as 12.9 microseconds. This provides the high level of floating point computational performance required for many real-time applications.

A Scientific Instruction Set consisting of nine instructions for single precision operations also supports the same operations in double precision format. It works with the Floating Point Processor to achieve execution speeds for trigonometric, logarithmic and other transcendental functions that are 6 to 24 times faster for single precision, 6 to 42 times faster for double precision than comparable software routines. Execution time for square root is under 38 microseconds for single precision, under 136 microseconds for double precision. Sine and cosine average less than 48 microseconds for single precision, less than 175 microseconds for double precision.

A polynominal evaluation instruction is provided for evaluation, at hardware speed, of polynomials of the form:

$$Z(x) = \frac{a_0 + a_1x + a_2x^2 \ldots + a_nx^n}{b_0 + b_1x + b_2x^2 \ldots + b_nx^n}$$

This capability is useful in function approximation, such as in curve fitting or correction of non-linearity in a sensor such as a strain gage or thermocouple.

In addition, the polynomial instruction can also be used to calculate the quotient of two polynomials (M/N), each having the same general form noted above.

A Fast-FORTRAN Processor, a set of routines that accelerate the performance of FORTRAN programs, is also standard in the F-Series computers. Parameter passing, array address calculation floating point conversion operations, and other commonly-used FORTRAN routines are speeded up by a factor of 2 to 20.

Double integer instructions provide for addition, subtraction, multiplication, division, reverse-order subtraction and division, incrementing and decrementing with or without skipping, and comparisons.

Architecture

The HP 1000 F-Series architecture features a fully-microprogrammable control processor, which includes all arithmetic functions in addition to the calculation capabilities described above, as well as I/O, self test, and full operator control panel. Four general-purpose registers are available to the assembly code programmer, two of which may be used as index registers.

Standard F-Series instructions provide for indexing; single and double integer calculations and conversions; single, extended, and double precision floating point arithmetic; single and double precision trigonometric and logarithmic functions; a powerful polynominal evaluation instruction; double integer instructions; and a full complement of instructions for logical operations and bit/byte manipulation.

The F-Series offers extensive software program and I/O compatibility with HP 1000 M- and E-Series Computers. F-Series processors have been optimized for performance with a microprogrammed control processor that directs operations of the other functional units. The control processor speed has been increased by a sophisticated technique that varies microinstruction cycle time, depending on the complexity of the operation.

Efficiency of the microprogrammed routines that determine the machine language operation has also been increased through the mechanism of instruction and operand pre-fetch. The CPU-memory interface is totally asynchronous in the F-Series, adding flexibility to the powerful memory structure.

All I/O channels are fully-powered, buffered, and bi-directional. Because of modular design, mainframe memory capacity is completely independent of I/O capacity, so that either memory or I/O modules may be added without taking valuable mainframe space from the other. Mainframe memory capacity is 2M bytes in the 2117F.

A full line of interface controllers is available to interface HP-manufactured peripherals, instrumentation, communications devices, or specialized devices.

For applications which demand even higher performance, F-Series users can expand their instruction repertoire with HP-supplied microprogrammed subroutines. For exceptionally fast vector and matrix arithmetic, there is the Vector Instruction Set. Other optional enhancements include the RTE-IVB Extended Memory Area (EMA) firmware, and RTE-6/VM Virtual Memory Area (VMA) Operating System firmware.

User microprogramming

The advantage of microprogramming. The power and flexibility of control processor microprogramming is readily available to F-Series users. Control processor access provides users with the ability to perform commonly-used software routines 2 to 20 times faster in microcode. Control processor routines are written in an assembly-like language, stored in control processor memory, and called directly from Assembly, FORTRAN, or BASIC programs.

The control processor and control store capacity. Control processor programmers have access to a powerful processor within F-Series computers that executes instructions in 175-to-280 nanoseconds, and provides three-level nested subroutines, 211 instructions, 16 high-speed scratchpad registers, 2 accumulators, and a 5.5k word address space available to the user. Up to 3k words of user microprograms may be implemented in Writable Control Store for microprogram development and dynamic loading of microprograms. Fully-developed microprograms may be stored in Programmable Read-Only Memory (PROM), a more permanent and secure storage medium for microprograms.

Microprogrammed use of the Floating Point Processor. Microprogrammers can use the Floating Point Processor (FPP) as a control processor computing resource to obtain significant performance increases over normal microprogramming. To the microprogrammer, the FPP provides a very high speed processor for floating point and extended precision integer operations. An example of the combined power of the Floating Point Processor and direct microprogramming is given by execution of a Sine(X) library function. With FPP, the execution time is 127.5 microseconds. With FPP and direct microprogramming, the execution time is 51.8 microseconds, more than 2.5 times faster.

Software support for microprogram development. Control processor program development is aided by HP's complete

software development tools, which include a micro-assembler, microdebug editor, program overlay load utility, and PROM tape generator, as well as a complete documentation package.

Memory system

Much of the speed of the F-Series Computer is due to the high speed of its primary memory systems. The F-Series Computer includes a memory system that cycles in 420 nanoseconds (without Fault Control Memory) and with a capacity up to 2 million bytes. Parity checking is standard in all HP 1000 memory systems. Fault control memory systems, which are capable of detecting and correcting all single-bit memory errors, and detecting all double bit errors, are optionally available.

For efficient handling of large memory systems, the dynamic mapping system (DMS) is standard. A combination of hardware and control processor programs, DMS is a powerful memory manager that allows F-Series users to address up to 2048k bytes of memory and provides read and/or write protection of each individual 2048-byte page. Four independent memory maps are provided — one for the operating system, one for the user, and two port controller maps for direct memory access operations. DMS adds 38 powerful memory management instructions to the standard F-Series instruction set. This capability is fully supported by HP's RTE-IVB and RTE-6/VM real-time executive operating systems which offer multi-user access to as many as 64 multi-user program partitions. In RTE-6/VM support of large-memory systems also gives the user access to data arrays up to 128 megabytes in Virtual Memory.

Input/output

The F-Series I/O system features a multi-level, vectored priority interrupt structure. There are 50 distinct interrupt levels, each with a unique priority assignment. Any I/O device can be selectively enabled or disabled, or the entire interrupt system (except power fail and parity error interrupts) can be enabled or disabled under program control.

Data transfer between the computer and I/O devices may take place under program control, dual channel port controller (DCPC) control, or microprogram control. The DCPC provides two direct links between memory and I/O devices, and is program assignable to any two devices. DCPC transfers occur on an I/O cycle-stealing basis, not subject to the I/O priority interrupt structure.

For applications where higher transfer rates are desirable, The F-Series has a special Microprogrammable Block I/O capability that allows transfer rates up to 3.1 million bytes/second. This capability can be implemented through user-designed I/O cards and block I/O control microprograms.

Remote and local program load

The initial binary loading (IBL) function is easily performed on F-Series Computers. For local bootstrap loading, a 64-word ROM-resident IBL program is called by a push-button switch on the front panel. Disc loader ROM is standard. Up to two additional HP or user-supplied loader ROMs may be added to any F-Series Computer. The user can plug in up to four different loader ROMs if the standard loader ROMs are removed.

Computers at remote sites can be force-loaded from a central location through the use of a remote program load (RPL) capability. Information normally keyed into the front panel is set in switches on the CPU board, so the bootstrapping sequence may be initiated from a remote site, or automatically initiated on power-up from a local peripheral.

Self test

A comprehensive set of diagnostic routines permanently stored in read-only memory (ROM) is standard in the F-Series. Two of these routines, executed each time the IBL/TEST function is executed, provide quick tests of the processor and first 64k bytes of physical memory for verification of operating condition. A third test, executed whenever the machine is powered up, thoroughly tests the processor and all installed memory. This test may also be run manually. Other tests, executed from the front panel, provide quick verification checks of the Floating Point Processor and all firmware.

Power fail recovery system

The optional power fail recovery system provides a minimum of 1.6 hours of memory sustaining power for the largest memory configuration in the event of complete power failure.

Software

The HP 1000 F-Series maintains extensive program compatibility with earlier members of the HP 1000 family, so users can take advantage of many man-years of software development.

A wide range of operating system software is available. Real-time executive (RTE) systems, available in disc and main memory-resident versions, are multiprogramming systems that permit priority scheduling of several real-time programs while concurrent background processing also takes place.

Languages supported by HP operating systems include FORTRAN 77, FORTRAN 4X, Pascal, HP real-time BASIC, Assembly language, and micro-assembly language. Utility software includes a debugging routine, interactive editors,

and an extensive library of commonly-used computational routines. The F-Series also supports the full range of HP 1000 applications software, including data base management, graphics, and distributed networking.

F-Series users may also take advantage of a wide variety of thoroughly-tested and documented programs that have been contributed to the HP User Library PLUS/1000.

Specifications

All F-Series specifications can be found in the E/F-Series Specifications data sheet, located at the beginning of this section.

Ordering information

2117F computer

The 2117F Computer consists of:

1. Computer with separate mainframe, including non-RPL disc and 264x Minicartridge Loader ROMs, and 02117-60001 Floating Point Processor, including Scientific Instruction Set and Fast FORTRAN Processor.
2. 12791A Firmware Expansion Module.
3. 12788A 128k byte High Performance Memory package, including 2102E Memory Controller, 12747H 128k byte High Performance Memory Module, 12731A Memory Expansion Module, and 12892B Memory Protect Module.
4. 02109-90014 Microprogramming manual.
5. 2111-90002 HP 1000 F-Series installation and service manual.
6. DMI ROMs (13307B)

2117F options

014: Deletes standard memory to permit its replacement, with another HP high performance memory system, with or without fault control, which must be ordered separately.

015: 220V operation

2117F accessories

For list of accessories that are compatible with the 2117F computer, see the power specifications and applicability summary on page 7-3, referring to the Series F applicability column.

12823S Firmware Subscription Service

Provides firmware updates of Dynamic Mapping Instructions, Scientific Instruction Set, and Fast FORTRAN Processor firmware in HP 1000 F-Series Computers as required to keep those firmware items up to date with respect to changes as they are released by Hewlett-Packard. The 12823S service is priced in monthly units and is billable quarterly.

Dual-Port I/O Extender and Dual CPU Kit

HEWLETT PACKARD

The 12979B Dual-Port I/O Extender expands the I/O capacity of HP 1000 computers by offering additional channels to house standard interface cards. Integral to the 12979B is a programmable I/O bus switch that provides the capability to develop configurations for peripheral sharing between two computers.

Features

- Provides 16 additional I/O slots per extender, with up to two extenders per computer
- Integral I/O bus switch provides capability for peripheral sharing
- Solid state switching logic for speed and high reliability
- Optional direct memory access with dual-channel port controller accessory
- Full continuity of interrupt locations

Functional description

I/O expansion

The 12979B extender provides 17 I/O slots for standard interface cards. Adding the 12979B to any HP 1000 computer provides a net addition of 16 slots, since one mainframe slot is required for the extender buffer card. Space is also provided in the extender for mounting the 12898A Dual-Channel Port Controller accessory, which provides direct memory access capability for any peripheral connected via the I/O extender.

The I/O extender, when used in the single port mode, is transparent to the programmer. Any select code (I/O device address) may be programmed into it, and I/O cards will operate with the same speed and flexibility as those in the computer mainframe.
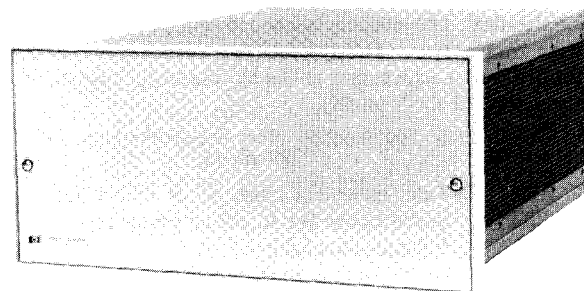
The first I/O slot in the extender can be programmed to any select code, so devices can be moved from the computer to the extender to balance power consumption or to share with another CPU without losing select codes.

I/O bus switch

Integral to the extender is a programmable I/O bus switch that can transfer control of I/O devices connected to the extender between two HP 1000 M-Series, E-Series, or F-Series computers. This capability makes it easy to set up a variety of configurations for peripheral sharing.

The switch is operable under either manual or program control, and has three positions, defined as follows:

Connected to CPU port A: In this position, the I/O extender is connected to the computer associated with port A, and all devices interfaced via the extender are available to that computer. When connected, operations are totally transparent to the computer program.

Connected to CPU port B: Operation is the same as described for port A, above, except that the computer connected to port B has exclusive access to the extender and the devices connected to it.

Neutral: Neither computer is connected.
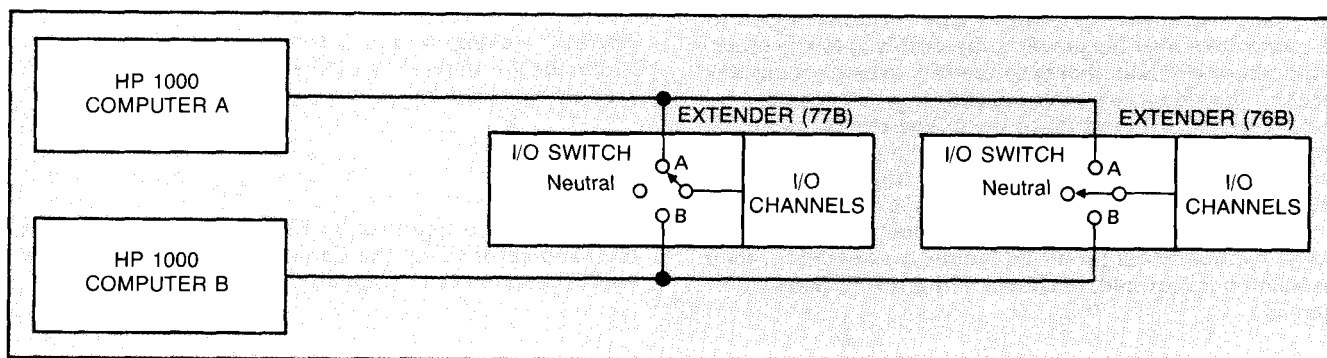
Two-computer connection to two dual-port I/O extenders

I/O bus switch programming

Switch programming is addressed to a select code (I/O device address), which can be any number from 70 to 77 octal, that is set by selector switches beneath the deck of the extender. The switch is controlled by the four input/output instructions defined below, which have a unique meaning when addressed to the I/O extender select code (in range from 70 to 77 octal).

Instruction	Purpose
STC EXT*	Take extender from other computer
CLC EXT*	Force extender to other computer
CLF EXT*	Release extender (puts switch in Neutral position)
SFC EXT*	Take extender if released. Skip indicates switch was in neutral position and has been connected to the computer issuing the instruction

*EXT = *select code in range from 70 to 77 octal.*

Functional specifications

Capacity

Extender: 17 I/O channels (16 additional).

Extenders per computer: Two, maximum.

Computer I/O channels used: One per extender.

I/O switch characteristics

Number of computer ports: Two.

Switching time: One I/O instruction.

Configuration information

Maximum separation between computer and extender: 1.8m (6 ft), cable length limited.

Minimum clearances; 7.6 cm (3 in) for rear cable; 5.7 cm (2-1/4 in) air intake inside clearance.

Power fail communication: Status of the power supplies in HP 1000 computers and I/O extenders is communicated via power control cables. A power failure or power shut-down in a computer or extender causes a power down signal to be transmitted over the power control cable(s) to any other computer or extender that is connected. When a computer receives the signal, a power fail interrupt is generated in that computer. Connection of the power control cables is required for orderly shutdown because a power failure or power down in an extender will cause unpredictable control and data signals that **may** cause loss of control over the computer's operation. Therefore, although use of the power control cables prohibits redundant operation, their installation is required, as shown in the 12979B installation manual.

Installation: To install, mount the 12979B in a rack less than 1.8m (6 ft) from the HP 1000 computer(s). Connect the power control cable between the extender and computer. Install an I/O buffer card in the first unused I/O slot in the computer(s). Configure the I/O extender control card to the first select code desired in the extender, the desired select code for the I/O switch, and the source of the priority chain for both computer ports (if both are used). Connect the I/O control signal flat cable(s) between the extender and the cpu board(s) in the computer(s) and connect the I/O data cable(s) between the I/O buffer card(s) in the computer(s) and the I/O extender control card. If only one computer is connected to the extender, the extender configuration switches can be set to lock the switch to that machine, avoiding the necessity of issuing STC EXT each time the system is powered up.

Electrical specifications

AC power required

88-132V, 47.5-66 Hz, 625W, maximum; 176-264V, 47.5-66 Hz with option 015. Input line voltage range is easily changed in the field by moving jumper connections.

Current required from computer

2A(+5V) and 1.35A(−2V) for I/O buffer card.

Current available to I/O slots

4.5A(+12V),47A(+5V),5A(−2V), 2.5A(−12V), 0.25A(+28V)

Power supply

Storage after line failure: I/O extender continues normal operation through temporary power interruptions of up to 8 milliseconds when operating at the minimum ac line voltage.

Output protection: All voltages are protected for over voltage and over current.

Thermal sensing: Monitors internal temperature and automatically shuts down I/O extender if temperature exceeds specified level.

Safety

The 12979B is recognized by Underwriters Laboratories, Inc., and certified by the Canadian Standard Association (with the exception of option 015).

Physical characteristics

Dimensions

Width: 48.3 cm (19 in) panel; 42.6 cm (16-3/4 in) behind panel casting.

Depth: 62.2 cm (24-1/2 in) overall; 58.4 cm (23 in) behind panel casting.

Height: 22.2 cm (8-3/4 in).

Weight

16 kg (35 lb)

Heat dissipation

538 kilogram-calories/hr (2138 BTU/hr).

Ventilation

Air flow is 5.7 cubic meters/min (200 cubic feet/min), intake on left side, exhaust on right side.

Ordering information

12979B Dual port I/O extender

The 12979B includes:

1. 12979B Dual port I/O Extender.
2. 12979-60029 I/O Buffer Assembly.
3. 12979-60028 I/O Data Cable, 2.1m (7 ft) long.
4. 12979-60008 I/O Control Cable.
5. 12979-60025 Power Control Cable.
6. 12979-90016 Installation and Service Manual.
7. 12979-90014 Operating and Reference Manual.
8. 12979-60026 Power Control Cable Adaptor.
9. 02100-60060 I/O Terminater Assembly.
10. 02112-60021 CPU Power Cable.

12781A dual cpu kit

The 12781A dual cpu kit includes:

1. 12979-60029 I/O Buffer Assembly.
2. 12979-60028 I/O Data Cable 2.1m (7 ft) long.
3. 12979-60008 I/O Control Cable.
4. 12979-60025 Power Control Cable.
5. 12979-60026 Power Control Cable Adapter.

12898A dual channel port controller for 12979B

The 12898A dual channel port controller for the 12979B includes:

1. 12898-60001 dual channel port controller assembly.
2. 12898-90001 installation manual.

I/O extender option

001: Modification for use in 2176E, 2177F, 2178C, or 2179C EMI-Qualified System Processor Unit.

015: 220V (176-264V) operation.

016: 220V (176-264V) operation and Option 001.

Power Fail Recovery Systems

**HP 1000 M/E/F-Series Computers
and Memory Extenders**

product numbers 12944B and 12991B

The 12944B and 12991B power fail recovery systems provide battery sustaining power for memory during line power outages, as well as battery charging circuitry, and battery charge state testing. If a line power outage does not last long enough to deplete available battery charge, the power fail/auto restart feature of HP 1000 computers may be used to resume processing. If, on the other hand, a line power outage lasts long enough to deplete available battery charge, the power fail recovery system prevents automatic power up and signals the operator that this condition exists.

Features

- Sustains memory through power failures
- Tests battery charge state and provides a low battery warning indicator
- Provides automatic memory clear on power failures lasting longer than available battery charge
- Operates throughout the entire range of HP 1000 environmental specifications

Functional specifications

Application

12944B is used for battery backup of 2108M and 2109E Computers. It contains one 14-volt sealed lead-acid battery with a rating of 5 ampere-hours.

12991B is used for battery backup of 2112M, 2113E, and 2117F Computers and Memory extenders. It contains two 14-volt sealed lead-acid batteries, each with a rating of 5 ampere-hours.

Memory Sustaining Time

Memory sustaining time is determined by the standby power load of the memory controller, memory modules, and fault control check bit array boards (if applicable) on the memory power provided by the power fail recovery system battery. Power fail recovery system power loadings of the various currently active HP 1000 M/E/F-Series memory components are given in Table 1. To determine memory sustaining time for any given configuration, add up all the loads (current x voltage) for products not listed here imposed on the power fail recovery system to get a total, P. Then you can calculate sustaining time, T, with the appropriate equation, below.

Sustaining Time for 12944B: $T = 10^{((32.9 - P)/43.9)}$ hours

Sustaining Time for 12991B: $T = 10^{((53.8 - P)/50.0)}$ hours

If you wish to determine sustaining time for several different memory configurations, you can prepare a graph of time vs power with the end points tabulated below that can be used to determine memory sustaining time graphically for several different power loads.
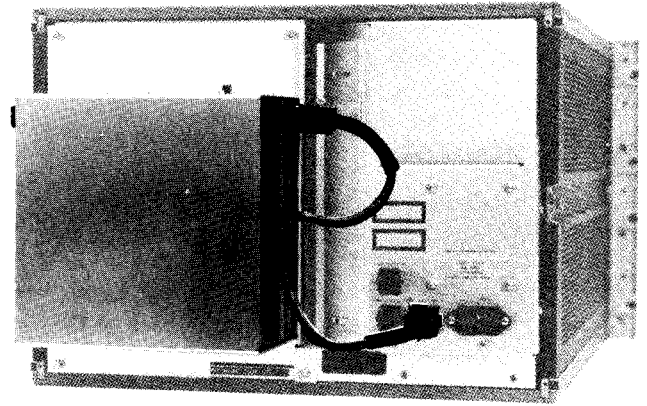
12991B power pack mounted on rear of 2113 computer

End Points	For 12944B		For 12991B	
Power	55.9W	6.5W	58.7W	3.8W
Time	0.3 hr	4.0 hr	0.8 hr	10 hr

Table 1. Memory Power Loading of HP 1000 Memory Components

Product Number	Description	Load
MEMORY CONTROLLERS		
2102B	Std Perf Parity Memory Controller	2.50W
2102C	Std Perf Fault Control Memory Controller	3.40W
2102E	High Perf Parity Memory Controller	3.20W
2102C	High Perf Fault Control Memory Controller	3.45W
MEMORY MODULES		
12746A/H	64kb Memory Module (16k RAMs)	2.85W
12747A/H	128kb Memory Module (16k RAMs)	2.85W
12699H	256kb Memory Module (64k RAMs)	2.65W
12749H	512kb Memory Module (64k RAMs)	3.25W
FAULT CONTROL CHECK BIT ARRAY BOARDS		
12779A/H	256kb Check Bit Array Board (16k RAMs)	3.90W
12780A/H	512kb Check Bit Array Board (16k RAMs)	3.90W
12666H	1.0Mb Check Bit Array Board (64k RAMs)	3.80W

Power restart

Detects resumption of power and generates an interrupt to trap cell for user-written restart program which has been protected in memory by the sustaining battery.

Power control and charge unit

Monitors battery charge status and provides slow charge.

Sustaining battery

Type: 14 volt, 5 amp-hr (12944B) or 10 amp-hr (12991B) sealed lead acid.

Charging rate: 2A, maximum.

Battery charge time

Approximately 16 hours to fully-charge.

Figure Caption

12991B power pack mounted on rear of 2113 computer

Installation

To install, secure the battery pack to the back of the computer or memory extender, plug the printed circuit cards into the power supply, and connect the battery cable to the extender's input battery connector.

Environmental specifications

All environmental specifications coincide with those of the M-, E-, and F-Series CPUs except for non-operating temperature, which is as follows:

Non-operating: −40° to 60°C (−40° to 140°F).

Physical characteristics

12944B: Adds 11.1 cm (4-3/8 in) to overall depth, 4.3 kg (9.5 lb) to weight of the Computer.

12991B: Adds 11.1 cm (4-3/8 in) to overall depth, 7.3 kg (16 lb) to weight of the Computer or Memory extender.

Ordering information

12944B power fail recovery system

The 12944B power fail recovery system includes:

1. 12944-60001 battery pack.
2. 5061-1348 battery charging assembly.
3. 5061-1349 battery backup assembly.
4. 12944-60002 cable.
5. 12944-90005 installation manual.

12991B power fail recovery system

The 12991B power fail recovery system includes:

1. 12991-60001 battery pack and mounting hardware.
2-4. Same as 2 through 4 of 12944B, above.
5. 12991-90004 installation manual.
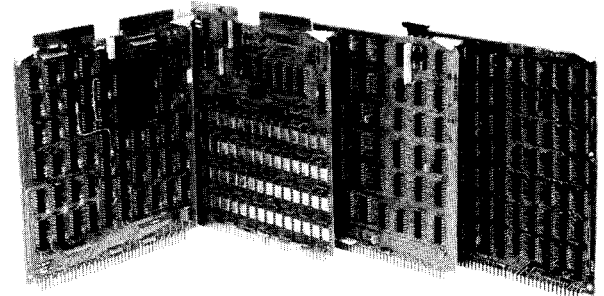
Parity and Fault Control Memory Systems

product numbers
HP 2102B/C/E/H, 12699H, 12746H, 12747H, 12749H,
12779H, 12780H, 12666H, 12784A-D, 12785A-D,
12786A-D, 12787A-D, 12788A-H, and 12789A-M

For HP 1000 M/E/F-Series Systems

Parity and fault control memory systems for HP 1000 M/E/F-Series computers encompass standard performance memory for M/E-Series Computers and high performance memory for E/F-Series Computers. HP 1278x Memory Packages (Table 1, next page) provide convenient means of obtaining complete memory systems in memory sizes from 128k bytes to 2048k bytes.

Features

- **Choice of parity or fault control memory**
- **Up to 2 Megabytes of high-density memory in computer mainframe using 512kb memory modules and 1Mb fault control check bit array boards**
- **Automatic correction of single-bit errors with fault control memory**
- **Convenient, economical large memory packages**

Functional specifications

Maximum Mainframe Memory Capacity

Computer	2108M, 2109E, or 2111F	2112M, 2113E, or 2117F
Memory Module Slots	5	10
Max. Parity Memory	2048kb*	2048kb*
Max. Fault Control Memory	1536kb*	2048kb*

* With 12749H 512kb Memory Modules, and 12666H 1Mb Fault Control Check Bit Array Boards. Use of other memory modules or fault control check bit boards reduces total memory capacity.

Memory Organization

Parity memory organization and cycle time:

Computer (System Model)	Memory Control	One or More Memory Modules	Capacity	Cycle Time
2108M or 2112M	2102B	12746A*/H 12747A*/H 12699H 12749H	64kb 128kb 256kb 512kb	650ns
2109E or 2113E (40 or 60)	2102B	12746A*/H 12747A*/H 12699H 12749H	64kb 128kb 256kb 512kb	665ns ±35ns
2109E, 2111F, 2113E (40 or 60) or 2117F (45 or 65)	2102E	12746H 12747H 12699H 12749H	64kb 128kb 256kb 512kb	420ns ±35ns

NOTE: Dynamic mapping system is required for >64kb memory.

* Identifies product to be obsoleted listed here for reference only.

12788E 512kb High performance memory package, including, left to right: 2102E Memory controller, 12749H 512kb Memory Module, 12892B Memory protect module, and 12731A Memory expansion module.

Fault control memory organization and cycle time:

Computer (System Model)	Memory Control	One or More Memory Modules	Check Bit Boards	Capacity	Cycle Time
2108M or 2112M	2102C	12746A*/H 12747A*/H 12699H 12749H	12779A*/H 12780A*/H 12666H	64kb 128kb 256kb 512kb 1024kb	650ns
2109E or 2113E (40 or 60)	2102C	12746A*/H 12747A*/H 12699H 12749H	12779A*/H 12788A*/H 12666H	64kb 128kb 256kb 512kb 1024kb	735ns ±35ns
2109E, 2111F, 2113E (40 or 60) or 2117F (45 or 65)	2102H	12746H 12747H 12699H 12749H	12779H 12788H 12666H	64kb 128kb 256kb 512kb 1024kb	490ns ±35ns

NOTE: Dynamic mapping system is required for >64kb memory.

* Identifies product to be obsoleted listed here for reference only.

Basic Word Size: 17 bits (2 bytes plus parity bit provided in memory modules).

Fault Control Memory Word Size: Check bit array cards add 5 check bits to basic word size.

Intermixing of Memory Modules: Memory modules of differing capacities can be intermixed on the same controller. Also, 1274xH and 12699H memory modules may be used with 1274xA memory modules on the same 2102B or 2102C controller, but 1274xA memory modules are not usable on the 2102E or 2102H controller.

Table 1. Summary of 12784/5/6/7/8/9x Memory Packages

NOTE: The preferred memory packages for each memory size are listed first.

Computers Supported		High Performance Memory Packages 2109E, 2111F, 2113E, and 2117F		Standard Performance Memory Packages				Memory Modules and FC Check Bit Boards Included (NOTE A)					
				2109E and 2113E		2108M and 2112M		Memory Modules			FC Check Bit Bds*		
Type of Memory		Parity	FC	Parity	FC	Parity	FC	12747H	12699H	12749H	12779H	12780H	12666H
Memory Controller		2102E	2102H	2102B	2102C	2102B	2102C						
Memory Size	128kb	12788A	12789A	12786A	12787A	12784A	12785A	1	0	0	1	0	0
	256kb	12788BB						0	1	0	0	0	0
	256kb	12788B	12789B	12786B	12787B	12784B	12785B	2	0	0	1	0	0
	512kb	12788E	12789J					0	0	1	0	0	1
	512kb		12789E					0	0	1	0	1	0
	512kb	12788C	12789C	12786C	12787C	12784C	12785C	4	0	0	0	1	0
	1024kb	12788F	12789K					0	0	2	0	0	1
	1024kb		12789F					0	0	2	0	2	0
	1024kb	12788D†‡	12789D†‡	12786D†‡	12787D†‡	12784D†‡	12785D†‡	8	0	0	0	2	0
	1536kb	12788G	12789L					0	0	3	0	0	2
	1536kb		12789G†					0	0	3	0	3	0
	2048kb	12788H	12789M†					0	0	4	0	0	2
	2048kb		12789H†‡					0	0	4	0	4	0

NOTE A: The memory packages also include the 12731A Memory Expansion Module and 12892B Memory Protect Module for dynamic mapping of memory above the lowest 64k bytes. In addition, the 12784x and 12785x Memory Packages include the 12778B Dynamic Mapping Instructions for M-Series Computers. Dynamic Mapping Instructions for the E/F-Series Computers are now included with the computer.

* = Item included with fault control memory package only.

† = 12990B Memory Extender is required to furnish additional memory module slots for this package used in a 2108M, 2109E, or 2111F Computer.

‡ = 12990B Memory Extender is required to provide additional +5V memory current for 12785D, 12787D, 12789D, or 12789H Memory Package used in a 2112M, 2113E, or 2117F Computer with 12991B Power Fail Recovery System.

Fault Control Check Bit Array Board Configurability:
Within their maximum capacity, the check bit boards can be configured to support 64kb, 128kb, 256kb, and 512kb of fault control memory.

Intermixing of Fault Control Check Bit Array Boards:
12779H, 12780H, and 12666H Fault Control Check Bit Array Boards can be used with 12779A and 12780A Check Bit Boards on the same 2102C Controller, but 12779A and 12780A Check bit boards are not usable on the 2102H controller.

Refresh: Each memory location is refreshed automatically every 2 milliseconds.

Memory Data Integrity Provisions

Standard memory power supply: Provides power during line failure that does not exceed 8 milliseconds.

Battery backup: The optional 12944B (for 2108M or 2109E) or 12991B (for 2111F, 2112M, 2113E, or 2117F) Power Fail Recovery System provides memory power in case of total line failure exceeding 8 milliseconds. However, use of the Power Fail Recovery System restricts the memory module and fault control check bit board configurations that can be used. (See 'Configuration Restrictions for Computers with Power Fail Recovery System' below.)

Parity memory: The 2102B or 2102E Memory Controller monitors all words read from memory, utilizing the 17th bit in each word for parity checking. Switch selectable response to parity error can be to halt, interrupt the RTE operating system, or ignore a detected parity error. The 12892B Memory Protect Module (part of the dynamic mapping system required to address more than 64kb memory) is required for parity error address detection for the RTE operating system.

Fault control memory error detection and correction: The 2102C or 2102H Fault Control Memory Controller in conjunction with the fault control check bit array boards executes a Hamming error correction code. Using this code, all single-bit errors are detected and automatically corrected so that processing is not interrupted. All double-bit and most multiple-bit errors are detected and flagged to the RTE operating system.

Configuration Restrictions for Computers with Power Fail Recovery System

In HP 1000 M/E/F-Series Computers with 12944B or 12991B Power Fail Recovery System (PFRS), the +5M memory supply has a maximum available current of 6A, which cannot be exceeded by the combined +5M current requirements of the memory controller, memory modules, and fault control check bit array boards installed in the computer. The maximum parity and fault control memory configurations that are supportable in the mainframe of 2112M, 2113E, 2117F computers within this current limitation are summarized below. The +5M current limitation is not important in 2108M, 2109E, or 2111F Computers because they have only five memory module slots. The memory capacity of HP 1000 M/E/F-Series computers without a power fail recovery system is not subject to the +5M 6A current limitation, since both +5V and +5M current requirements are taken from the +5V CPU supply.

Large memory configurations that are supportable in 2112M, 2113E, or 2117F Computer Mainframe with 12991B Power Fail Recovery System (NOTE A).

	Parity Memory		Fault Control Memory			
	Mem. Modules		Mem. Modules		FC Check Bit Bds	
Memory Size	12747H	12749H	12747H	12749H	12780H	12666H
1024kb	8	0	4	1	2	0
1024kb	4	1	4	1	0	1
1408kb	7	1	n/s	n/s	n/s	n/s
1536kb	4	2	0	3	3	0
1536kb	0	3	0	3	0	2
1792kb	6	2	n/s	n/s	n/s	n/s
2048kb	4	3	0	4	0	2
2048kb	0	4				

NOTE A: Other configurations this size or larger require 12990B Memory Extender with 12991B Power Fail Recovery System, which provides +5M current to memory modules and check bit boards installed in it.

n/s = Fault Control Memory size Not Supported in Computer mainframe; will require 12990B Memory Extender.

Ordering information

NOTE: For the hardware supplied in 12784A-D, 12785A-D, 12786A-D, 12787A-D, 12788A-H and 12789A-M Memory Packages and the memory sizes of each package, see Table 1. For installation manuals provided, see Table 2.

12784x Standard Performance Memory Packages for M-Series Computers

12785x Standard Performance Fault Control Memory Packages for M-Series Computers

12786x Standard Performance Memory Packages for E-Series Computers

12787x Standard Performance Fault Control Memory Packages for E-Series Computers

12788x High Performance Memory Packages for E/F-Series Computers

12789x High Performance Fault Control Memory Packages for E/F-Series Computers

2102B Standard Performance Memory Controller

2102C Standard Performance Fault Control Memory Controller

2102E High Performance Memory Controller

2102H High Performance Fault Control Memory Controller

12746H 64kb Memory Module

12747H 128kb Memory Module

12699H 256kb Memory Module

12749H 512kb Memory Module

12779H 256kb Fault Control Check Bit Array Board

12780H 512kb Fault Control Check Bit Array Board

12666H 1024kb Fault Control Check Bit Array Board

Table 2. Installation Manuals (by HP Part Number) Supplied with HP 1000 M/E/F-Series Memory Packages and Components

Components		Memory Packages		
Name	Product Numbers	12784A-D 12785A-D	12786A-D 12787A-D	12788A-H 12789A-M
Memory Control	2102B and 2102C	5955-4310	5955-4310	Not Appl.
	2102E and 2102H	Not Appl.	Not Appl.	5955-4311
Memory Modules	12746H, 12747H, 12699H, & 12749H	5955-4311	5955-4311	5955-4311
FC Check Bit Bds	12779H, 12780H, & 12666H	5955-4311	5955-4311	5955-4311
Mem Exp Module	12731A	12731-90001	12731-90001	12731-90001
Memory Protect	12892B	12892-90007	12892-90007	12892-90007
Dyn Map Instr.	12778B	12976-90005	Not Appl.	Not Appl.

Time Base Generator

HEWLETT PACKARD

The 12539C Time Base Generator provides a system software clock for interfacing time-dependent equipment. All time base generator functions are contained on a single, plug-in card that has its own select code. The card provides command and interrupt logic, a 100k Hz oscillator, eight decade frequency dividers, and output selection logic.

Features

- **Multiple time bases**
- **Built-in error detection**
- **Easy assembly-language programming**
- **Operates with interrupt or skip routines**
- **Plugs into I/O slot of any HP 1000 computer**

Description

The time intervals are generated in decade steps from 100 microseconds to 1000 seconds (16.67 minutes) and are derived from the crystal oscillator. Any interval (in 100 microsecond increments) may be selected by use of a simple, assembly-language program loop. Built-in error detection provides an error status bit to the computer when a time interval is not acknowledged.
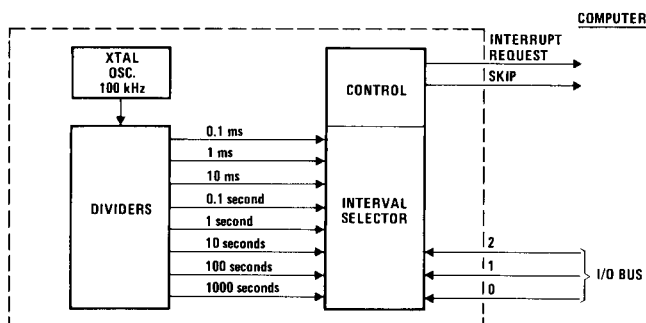
A signal from the computer enables the generator. The 100k Hz oscillator signal is formed into eight time base intervals by the divider circuit. The appropriate time base is selected by using one of the following interval codes:

Binary code	000	001	010	011
Interval (millisec)	0.1	1.0	10	100
Binary code	100	101	110	111
Interval (seconds)	1.0	10	100	1000

When the selected interval is elapsed, the control logic requests an interrupt or enables a skip signal to the counter.
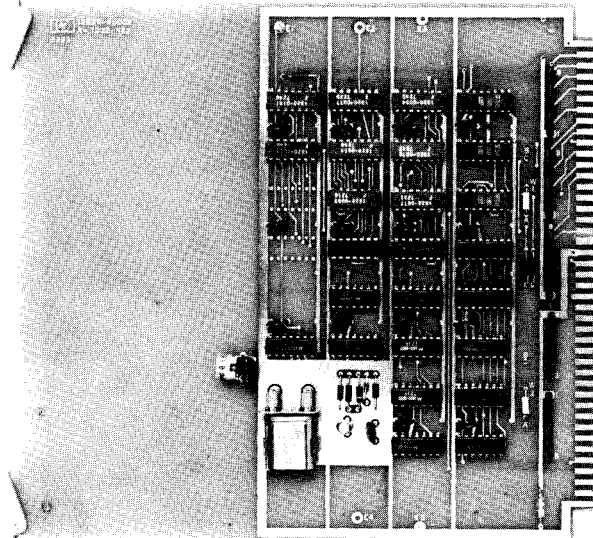
Functional specifications

Base intervals

0.1, 1, 10, and 100 milliseconds and 1, 10, 100, and 1000 seconds.

Accuracy

Stability: 2 parts in 10^6/week.

Temperature effects: 20 parts in 10^6 over temperature range of 15° to 35°C (59° to 95°F).

Total stability: 1/2 second/24-hour day

Electrical specifications

Current required from computer power supply

0.75A (+5V), 0.016A (−2V)

Ordering information

12539C Time base generator

The 12539C Time base generator includes:

1. 12539-60005 Time base generator.
2. 12539-90008 Operating and service manual.

Memory Protect

The 12892B Memory Protect, when installed in the memory section, provides an operating system with the capability to protect itself from alteration, and preserve system control of I/O functions. It also offers capability to detect parity error operations by generating a parity interrupt, prevents infinite indirect addressing loops from holding off interrupt servicing, and identifies user violations when operating with DMS.

Features

- **Memory protect logic prevents memory alteration below a programmable fence address**
- **I/O protect logic provides vectored interrupt on attempted execution of I/O instructions and prevents I/O operation until interrupt is serviced, thus giving system exclusive control of I/O and DMS operations**
- **Parity error interrupt logic provides an interrupt on occurrence of a parity error in memory and saves the parity error address**
- **Parity and memory protect features separately enabled/disabled by standard I/O instructions**
- **Computer may be switch-selected to interrupt or halt on parity error**
- **Operates in conjunction with dynamic mapping to provide interrupts for paged memory violations, privileged instruction violations, or parity errors**
- **Indirect level counter enables interruption of long indirect address loops**

Functional description

Memory protect fence

Memory protect provides capability to protect a selected block of memory from a programmable fence downward, against alteration by programmed instructions (EXCEPT those directly involving the A and B registers.) Any programmed instruction except JMP may freely address the A and B registers as locations 00000 and 00001, respectively. By removing the appropriate jumper, it is possible to prevent a JSB to A or B.

I/O control

With an STC 05 instruction, memory protect logic prohibits the execution of all I/O instructions except those involving the operator panel SC01. This feature limits I/O operations to interrupt on DCPC only. Programming the system to direct all I/O interrupts to an executive program provides exclusive control of the I/O system. Memory protect logic is disabled automatically by any interrupt and must be reenabled by an STC 05 instruction at the end of each interrupt subroutine.
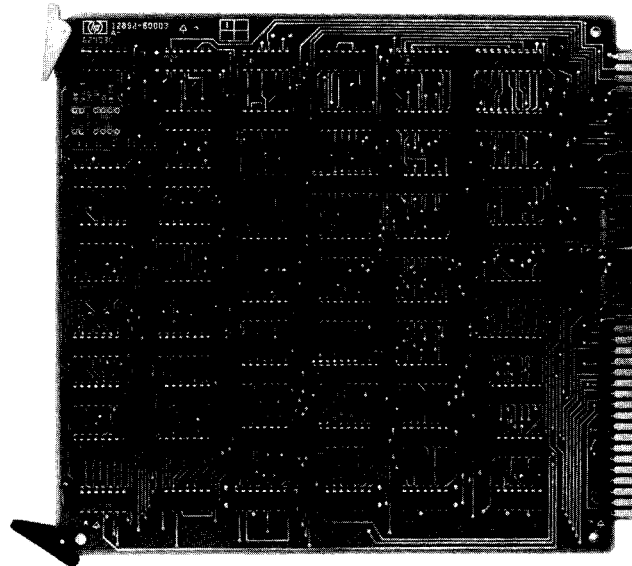
Programming

The following programming rules pertain to the use of memory protect, assuming an STC 05 instruction has been given:

A. Location 00002 is the lower boundary of protected memory. Locations 00000 and 00001 are the A and B register addresses.

B. JMP instructions may not reference the A or B register; however, a JSB instruction may do so. By removing the appropriate jumper, it is possible to prevent a JSB to A or B.

C. The upper boundary, memory address, is loaded into the fence register from A or B register by an OTA 05 or OTB 05 instruction, respectively. Memory locations below but not including this address are protected.

D. Execution will be inhibited and an interrupt to location 00005 will occur if a JMP, JSB, ISZ, STA, STB or DST instruction (also CBT, JLY, JPY, MVB, MVW, SAX, SAY, SBX, SBY, STX, and STY of the extended instruction group) directly addresses a location in protected memory. Execution will also be inhibited if any instruction is attempted, including HLT but excluding those addressing select code 01, the S register, and the overflow register.

After three successive levels of indirect addressing, the memory protect logic will allow a pending I/O interrupt. The 12892B can be jumper-configured to permit I/O instructions to any select code. HLT is still inhibited and all other protection features remain unchanged.

E. Any instruction not mentioned in step D is legal, even if the instruction directly references a protected memory address. Indirect addressing through protected memory by those instructions listed in step D is also legal provided that the ultimate effective address is outside the protected memory area.

Functional specifications

Compatibility

The 12892B is compatible with 2108, 2109, 2111, 2112, 2113, and 2117 Computers.

Configuration information

Slots required: 1 dedicated slot in computer mainframe.

Software recommended: 24396F diagnostic package on mini-cartridge.

Installation: To install, insert the 12892B board directly into dedicated slot in memory backplane. No cables required.

Electrical specifications

Current required from computer power supply

Model	+5V	−2V	+12V	−12V
12892B	1.25A	.05A	—	—

Ordering information

12892B Memory protect includes:

1. 12892-60003 Memory protect card.
2. 12892-90007 Installation manual.

Dual Channel Port Controllers

HEWLETT PACKARD

The 12897B Dual Channel Port Controller (DCPC) provides a direct port between computer interfaces and memory. Two programmable channels can connect any I/O device to memory; these channels are program-assignable and reassignable, operating on a cycle-stealing basis with the processor.

When operating with the Dynamic Mapping System (DMS), each channel is allocated a separate, automatically-enabled memory map to provide logical-to-physical memory translation.

DCPC operation in the 12979B Dual-port I/O extender requires the 12898A extender DCPC. Operation and software are identical for devices in the extender and computer.

Features

- Program-assignable to any I/O channel
- Independent word count and address register for each channel
- Common DMA controller for lower interfacing costs
- Direct data transfers to and from memory
- Operating system can interrogate word count registers to monitor transfer progress

Functional specifications

DCPC transfer rates (megabytes/second)

Transfer Operations and Memory Controller Models	Computer Models 2108 2112	Computer Models 2109 2111 2113 2117
Input		
2102B (Std performance memory)	1.23	1.95
2102C (Std perf fault ctrl memory)	1.23	1.88
2102E (High performance memory)		2.28
Output, non-Dynamic mapping		
2102B (Std performance memory)	1.23	1.77
2102C (Std perf fault ctrl memory)	1.23	1.67
2102E (High performance memory)		2.28
Output with Dynamic mapping		
2102B (Std performance memory)	1.23	1.67
2102C (Std perf fault ctrl memory)	1.23	1.62
2102E (High performance memory)		2.1
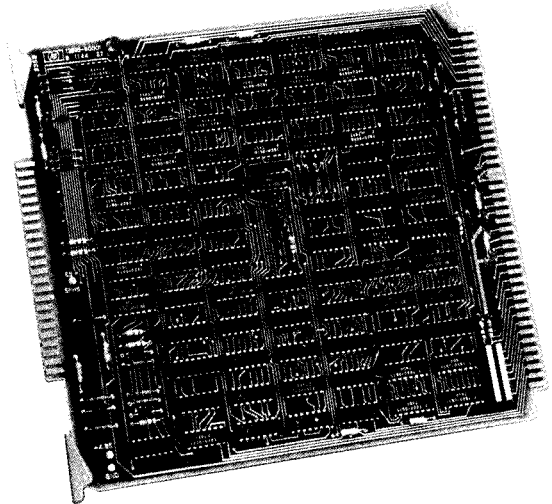
Capacity

Number of channels: 2

Number of memory ports: 1

Registers: 2 word count registers; 2 address registers; 2 select code registers

Word size: 16 bits (2 bytes)

Maximum block size: 65,536 bytes

Program-assignable: To any I/O channel

Configuration information

Slots required: 1, dedicated

Software recommended: Diagnostic package on paper tape (24396A), or minicartridges (24396F).

Installation; To install the 12897B, insert it directly into slot 110 of the memory backplane. For the 12898A, insert it directly into a dedicated slot in the 12979B I/O extender.

Electrical specifications

Current required from computer/extender power supply

Model	+5V	−2V
12897B	2.4A	.08A
12898A	.5A	.04A

Ordering information

12897B Dual channel port controller includes:

1. 12897-60004 Dual channel port controller assembly.
2. 12897-60002 Cable
3. 12897-90005 Installation manual

12898A Dual channel port controller for 12979B Dual-port I/O extender includes:

1. 12898-60001 Dual channel port controller assembly.
2. 12898-90001 Installation manual.

Firmware Accessory Board

HEWLETT PACKARD

The 13304A Firmware Accessory Board (FAB) is optional in HP 1000 E/F-Series Computers (except E-Series Board Computer) to provide space for 3.5k words of non-volatile control store. This space is used for HP-supplied enhancements, such as the 13307B Dynamic Mapping Instruction ROMs, the Scientific Instruction Set in the F-Series, DS/1000 firmware, RTE-6/VM or RTE-IVB firmware, and the 13306B Fast FORTRAN Processor ROMs. It accommodates both 4k (512 x 8) and 1k (256 x 4) bipolar ROMs or PROMs and is configured into four different address spaces.

Features

- **Four individually-configurable blocks (3.5k words) of non-volatile address space provided for HP 1000 E- and F-Series computers**
- **Utilizes 4k and 1k ROM's or PROM's**
- **Routines execute with no performance degradation from standard processor cycle times**
- **Compatible with HP microprogramming support software**
- **Easy configuration with plug-in jumpers**
- **ROM's current switched for low standby power**

Functional description

The 13304A Firmware Accessory Board is arranged in four configurable address spaces (blocks) as shown in the diagram. Three of these blocks are 1k words (four each of 256 word modules) and use six 4k ROM's/block. These blocks can also be loaded with three 4k ROM's if only two modules are needed. The remaining block contains up to 512 words (two each of 256 word modules) and uses 12 1k ROM's. This block can also be loaded with six 1k ROM's if only one module is needed.

One jumper determines whether the FAB will be used in the upper or lower 8k of the E-Series 16k control store address space (Modules 0-31 vs. 32-63).
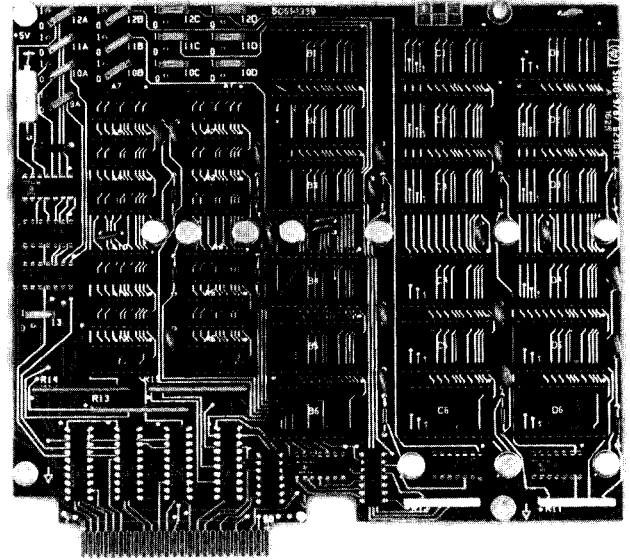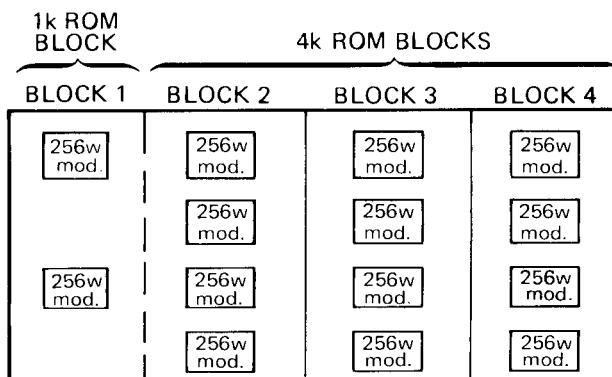
Once the upper or lower 8k address space is selected, each block can be jumpered to independently configure it to any address space within that 8k.

Functional specifications

Organization

Word size: 24 bits

Module size: 256 words

Board capacity: Three 1k word blocks of 4 modules each (4k ROM's), and one 512 word block of 2 modules (1k ROM's), each block individually configurable

Processor capacity: One 13304A Board

Cycle time: 175 nsec

ROM's or PROM's/module: 12 for 1k ROM block, 6 for each 4k ROM block

Reserved modules: HP 13306B, fast FORTRAN processor and dynamic mapping system instructions use 2 modules of 4k ROM's; Scientific Instruction Set uses four modules of 4k ROMs; DS/1000 and RTE-IVB or RTE-6/VM firmware each use 2 modules of 4k ROMs.

Recommended PROM's

4k: HP 1816-1142, Signetics 82S141, or Harris HM7641

1k: HP 1816-0782, or Harris 7611-5

1k ROM BLOCK	4k ROM BLOCKS		
BLOCK 1	BLOCK 2	BLOCK 3	BLOCK 4
256w mod.	256w mod.	256w mod.	256w mod.
	256w mod.	256w mod.	256w mod.
256w mod.	256w mod.	256w mod.	256w mod.
	256w mod.	256w mod.	256w mod.

Configuration information

The 13304A Firmware Accessory Board is configured as described in installation and reference manual. Check CPU +5V power supply current capacity prior to installation.

Installation: After the ROM's or PROM's are correctly installed and configured on the FAB board, it is secured beneath the E-Series CPU by four screws. Electrical connection is made by attaching the flat cable from the FAB connector to connector J2 on the CPU (and UCS or WCS if installed).

Software recommended:
92061A   RTE microprogramming software package.

Electrical specifications

Current required from +5V computer power supply

Power saver circuit limits current to 1.8A, maximum, regardless of the number of ROMs installed.

Ordering information

The 13304A is optional in the 2109E, 2113E, and 2117F Computers. The 12791A Firmware Expansion Module (FEM) is now standard.

13304A Firmware accessory board

The 13304A Firmware accessory board includes:
1. 5061-1339 Firmware accessory board.
2. 5061-3419 Cable assembly.
3. Four 2360-0113 screws.
4. 12791-90001 Installation and reference manual.

Dynamic Mapping System

The Dynamic Mapping System (DMS) for HP 1000 E/F-Series computers provides for expansion of memory beyond the 64k bytes that is normally the maximum addressable by 16-bit computers.

Features

- Two million byte address space
- Read and/or write protection for each page
- Four dynamically alterable memory maps; two for program execution and two for the dual channel port controller
- Program execution from non-contiguous page locations
- DCPC communication with a memory area separate from program space concurrently with program execution
- DCPC transfers to/from non-contiguous segments of memory
- Compatibility with previous software for HP 1000 family computers
- 38 instructions for memory management
- Provision of independent and shared base page semgnets using programmable fence
- Parity error interrupt logic that permits removal of erring memory pages from active use under program control
- Provision for sharing of programs and data between concurrent users
- Installation in dedicated slots in computer mainframe, so additional rack space is not needed
- Field or factory installability

Dynamic mapping description

The basic addressing space of the HP 1000 E/F-Series is 65,536 bytes, called the "logical" memory. The amount of semiconductor memory actually installed in the computer is called the "physical" memory. An HP 1000 E/F-Series computer with Dynamic Mapping System (DMS) has an address space of two million bytes for physical memory. Dynamic mapping allows physical memory to be mapped into logical memory via four dynamically alterable memory maps, a capability that is fully software supported by HP's RTE-6/VM and RTE-IVB operating systems.

The basic memory addressing scheme of the HP 1000 provides for addressing of 32 pages of memory, each page being 2048 bytes. This memory is addressed through a 15 bit memory address bus. The upper five bits of this bus provide the page address, and lower ten bits provide the relative word address within the page.

```
|14  PAGE ADDRESS  10 | 9    RELATIVE WORD ADDRESS    0 |
         ↓                              ↓
        15 BIT MEMORY ADDRESS BUS
```
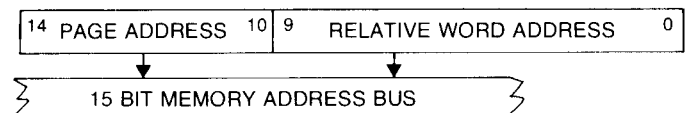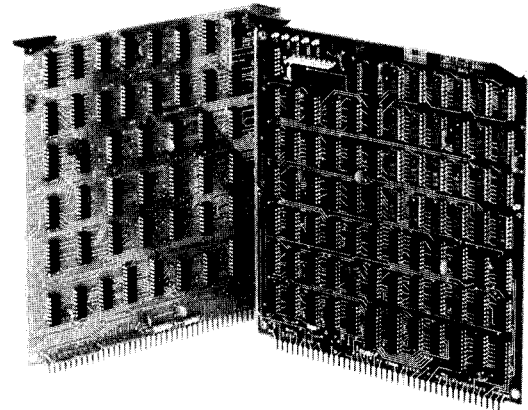
The Memory expansion module of the dynamic mapping system converts the 5-bit page address into a 10-bit page address and thereby allows 2^{10} or 1024 pages to be addressed. The conversion is accomplished by allowing the original 5-bit page address to identify one of 32 registers within a "memory map". Each of these memory map registers contains the new, user specified 10-bit page address. This new page address is then joined with the original 10-bit relative word address to form a 20-bit memory address.

```
|14  PAGE ADDRESS  10 | 9      RELATIVE WORD     0 |
         ↓
|19                          10|
        32 REGISTER
        MEMORY MAP
         ↓                              ↓
        20 BIT MEMORY ADDRESS BUS
```
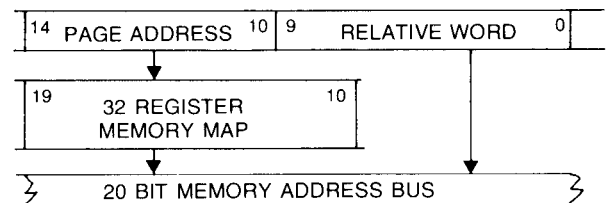
All registers within the memory map are dynamically alterable. To maximize system performance capability, there are four separate memory maps in the memory expansion module, selectable under program control: user map, system map, and two dual channel port controller (DCPC) maps.

Functional specifications

Memory address space provided

2048k bytes (2,097, 152 bytes)

Dynamic mapping instructions

All 38 DMS instructions are microprogrammed and assigned to control store module 32.

MNEM	Description	Typical Execute Times (μsec)‡	OP CODES
MBI	Move Bytes Into	4.94+1.82/wd	105702
MBF	Move Bytes From	+2.66 for	105703
MBW	Move Bytes Within	odd byte	105704
MWI	Move Words Into	2.59 +	105705
MWF	Move Words From	1.82/word	105706
MWW	Move Words Within		105707
SYA/B	Load/Store System	46-50.5–	101710/105710
USA/B	Load/Store User	46-50.5	101711/105711
PAA/B	Load/Store Port A	46-50.5	101712/105712
PBA/B	Load/Store Port B	46-50.5	101713/105713
SSM	Store Status in Memory	3.71*	105714
JRS	Jump and Restore Status	5.32-6.06*	105715
XMM	Transfer Map or Memory	4.27†	105720
XMS	Transfer Map Sequentially	4.10†	105721
XMA/B	Transfer Maps Internally	29.35	101722/105722
XLA/B	Cross Load	3.57*	101724/105724
XSA/B	Cross Store	4.17*	101725/105725
XCA/B	Cross Compare	3.57-4.24	101726/105726
LFA/B	Load Fence	2.17	101727/105727
RSA/B	Read Status	2.17	101730/105730
RVA/B	Read Violation	2.17	101731/105731
DJP	Disable and JMP	3.75*	105732
DJS	Disable and JSB	4.41*	105733
SJP	Enable System and JMP	3.75*	105734
SJS	Enable System and JSB	4.41*	105735
UJP	Enable User and JMP	4.17*	105736
UJS	Enable User and JSB	4.17*	105737

*Add 1.26 μsec for each level of indirect addressing.

†Add 1.62 μsec for each map loaded.

‡Using std performance memory, without fault control.

Dynamic mapping power fail characteristics

Power failure automatically enables the system map, and a minimum execution time of 500 μsec is assured the programmer. A power fail routine should include routines to save as many maps as desired.

Upon restoration of power, all maps are disabled and none are considered valid. It is the responsibility of the power fail recovery software to restore the maps as desired.

Violation register

The memory expansion module violation register contains information so the programmer can detect where a fault occurred in hardware or software and what steps must be taken to correct it:

15	14	13	12		7	6	5	4 ◄——► 0
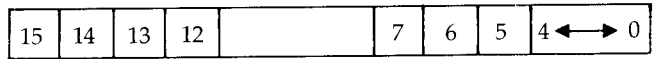
15	Read violation
14	Write violation
13	Base page violation
12	DMS privileged instruction
7	ME-bus enabled at violation
6	Maps enabled at violation
5	System user enabled at violation
0 - 4	Map register

Status register

The memory expansion module status register allows the programmer to determine whether the MEM is on or off currently, and at time of the last interrupt, as well as indicates the address for the base page fence.

15	14	13	12	11	10	9 ◄————► 0
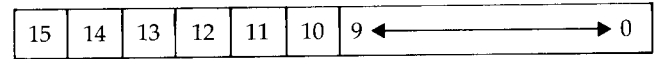
15	MEM enabled at last interrupt
14	System/user map selected at last interrupt
13	MEM currently enabled
12	System/user map currently selected
11	DMS protected mode
10	Portion mapped
0 - 9	Base page fence

Base page fence register

10	9 ◄————————► 0
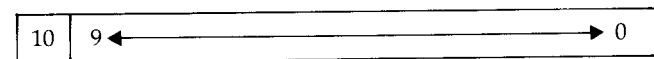
0 - 9	Fence address
10	Portion of base page mapped

Bit 10 = 0: Fence $\leq$ M < 2000_R is mapped

Bit 10 = 1: 1 < M < Fence is mapped

Memory protect

The memory protect feature of DMS provides all the capability of HP's 12892B memory protect plus the capability to read and/or write protect each individual page of physical memory.

Memory protect allows a block of logical memory of any size, from a selectable fence downward, to be protected against alteration by programmed instructions except those directly involving the A and B registers. This is in addition to the page-by-page protection provided within DMS.

Memory protect logic, when enabled, prohibits the execution of all I/O instructions except those referencing the switch register and the overflow register. This feature allows I/O to be controlled by interrupt only.

Although the memory expansion module performs its mapping function without the memory protect board installed, memory protect is required if the protection features are to be used.

Configuration information
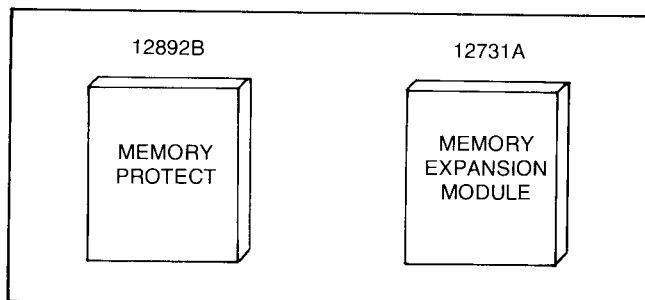
Compatibility: This Dynamic Mapping System is compatible with 2109, 2113, and 2117 computers.

Computer locations used: One dedicated slot each for the 12892B memory protect module and the 12731A memory expansion module in 2109, 2113, or 2117 Computer.

Software recommended: RTE-6/VM or RTE-IVB Real-Time Executive operating system (92084A or 92068A).

Installation: Plug the 12892B and 12731A modules into the memory section of the computer to complete installation.

Electrical specifications

Current required from +5V computer power supply

Model	12731A	12892B	13307A
+5V current	3.9A	1.25A	(A)

(A) Current used by 13307B is included in current used by the 12791A Firmware Expansion Module or the 13304A Firmware Accessory Board and is not included in the current requirement for the E/ F-Series Dynamic Mapping System.

Ordering information

NOTE: The 12892B and 12731A are included with 12786-94 memory packages. The 13307B Dynamic Mapping Instructions are included in 2109E/13E and 2117F and need not be ordered separately.

12731A Memory expansion module includes:
1. 12731-60001 Memory expansion module.
2. 12791-90001 M/E/F-Series Firmware Installation and Reference Manual.

12892B Memory protect

The 12892B Memory protect, also available separately (see separate data sheet), includes:
1. 12892-60003 Memory protect module.
2. 12892-90007 Installation manual.

13307S Firmware Subscription Service

Provides firmware updates of the 13307B Dynamic Mapping Instructions as they are released by Hewlett-Packard. The 13307S service is priced in monthly units and is billable quarterly.

Priority Jumper Card

The HP 12777A provides a means of completing the I/O priority chain when blank I/O slots are configured into a system. This card passes the interrupt priority chain through to I/O cards which follow the blank space, thus making it possible for them to cause an interrupt.

Features

- Completes I/O priority chain
- Allows blanks to be configured into I/O backplane
- Saves moving I/O cards and reconfiguration to complete interrupt priority chain

Functional specifications

Application

This card provides a direct short between RPL (Pin 3) and PRH (Pin 23). It may also be used to tie +5V to PRL (Pin 3).

Installation

To install, plug into HP 1000 computer I/O slot where needed to complete the I/O priority chain.

Two 12777A priority jumper cards

Ordering information

12777A Priority Jumper Card

The 12777A priority jumper card provides the 02116-6110 priority jumper card.
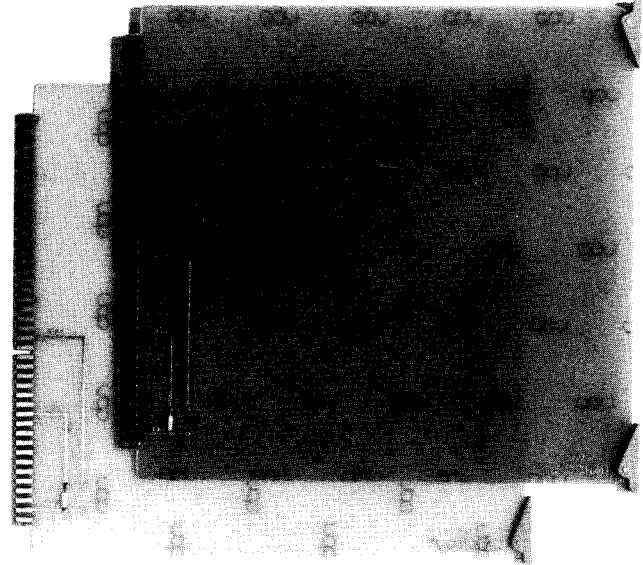
Loader ROMs

The HP 1000 optional loader ROMs each consist of one 256 x 4 bit PROM. Two of the ROMs allow absolute binary programs to be loaded into HP 1000 memory from a 264x cartridge tape or a 797x 9-track magnetic tape unit. The remaining ROMs are used to load programs in disc boot format from 7908/11/12/35 CS/80 discs, 7900/7901/2883 discs, 7906/7920/7925 cartridge/top-loading disc, or a 9885 Flexible disc.

Features

- Provides a choice of program loading from disc, magnetic tape, or tape cassette
- Each of the installed loader ROMs can be selected using the switch register
- Up to three optional loader ROMs may be used in an HP 1000 Computer

Functional specifications

Application

12992A: Bootstrap loader for 7900/7901/2883 disc.

12992B: Bootstrap loader for 7906/7920/7925 disc. [1]

12992C: Minicartridge loader for 264x CRT Terminals.

12992D: Loader for 9-track 7970B/E Magnetic Tape Unit (must be unit 0).*

12992E: 9885 Flexible disc loader ROM. [1]

12992F: Bootstrap loader for 7900A disc. [1]

12992J: Bootstrap loader for 7908/11/12/33 CS/80 discs. [1]

[1] *Identifies RPL-compatible ROM.*

* *7970E tape speed with HP 1000 M-Series must be 37.5 ips or less when used with 12992D loader ROM.*

NOTE: *12992 loader ROM's ordered with an HP 1000 computer are installed at the factory.*

Configuration information

Optional loader CPU sockets required: 1 per loader

Prerequisites: HP 1000 with 16k bytes or more memory

3HP 1000 M-Series installation: To install, remove CPU board from mainframe, insert 12992 loader ROM in one of three optional loader ROM sockets, and reinstall CPU board.

HP 1000 E/F-Series installation: To install loader ROMs in the two unoccupied sockets, unplug modules from the lower half of the memory card cage, plug in the ROMs, and reinstall the removed modules in the memory card cage. Access to replace the standard disc bootstrap loader ROM with other ROMs requires removal and reinstallation of the CPU board.
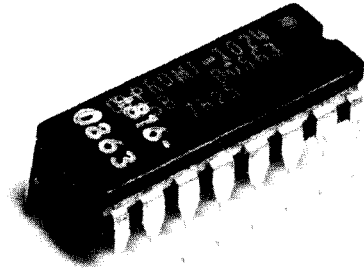
Typical loader ROM

Electrical specifications

Current required from +5V computer power supply

130 mA per loader ROM

Ordering information

12992A 7900A disc loader ROM

12992B 7906M/7920M/7925M disc loader ROM

12992C 264x cartridge loader ROM

12992D 7970B/E 9 track mag tape loader ROM

12992E 9885 Flexible disc loader ROM

12992F 7900A disc loader ROM

12992H 7906H/20H/25H disc loader ROM [1]

12992J CS/80 disc loader ROM

Each loader ROM includes an installation manual (12992-90001).

M-SERIES OPTIONAL LOADER ROM SOCKETS

Fast FORTRAN Processor (FFP)

HEWLETT PACKARD
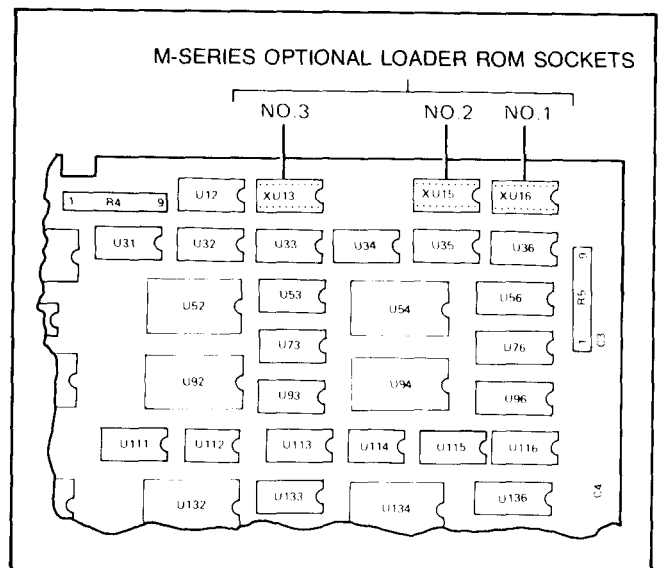
The HP 13306B Fast FORTRAN Processor consists of 20 microcoded subroutines which enhance performance of FORTRAN programs, assembly language programs, and scientific application programs. These routines are stored in bipolar ROMs mounted on the 12791A Firmware Expansion Module or the 13304A Firmware Accessory Board and executed by the HP 1000 E-Series control processor. The Fast FORTRAN Processor is standard in HP 1000 F-Series computers.

Features

- Firmware microcode for 20 instructions and subroutines:
  - Extended precision floating point addition, subtraction, multiplication, and division
  - Single precision to extended floating point conversion
  - Extended precision to single precision conversion
  - Extended precision move
  - Extended precision normalization and pack
  - Two and three dimensional array mapping
  - Subroutine parameter transfer
  - Conditional control transfer
- Can be used with FORTRAN and assembly language
- Provides 2 to 20-fold faster program execution

Functional description

Each fast FORTRAN subroutine has a unique instruction code associated with it. When a high-level language program is compiled, a subroutine call to the program library is generated by the compiler. The loader then replaces the subroutine call with the appropriate fast FORTRAN machine code. Execution of the fast FORTRAN code calls a firmware routine, allowing the control processor to execute the instruction.

In assembly language, the machine opcodes of the fast FORTRAN processor and the appropriate parameter lists are used instead of the overlay library, to execute fast FORTRAN instructions (refer to the manual "Relocatable Subroutine," HP part number 24998-90001). For example, when the extended precision divide routine, XDIV, is to be executed in FFP microcode, a programmer simply replaces the assembly language statement JSB XDIV by the corresponding opcode 105204 as follows:

Assembly language	Assembly language
JSB.XDIV (Call subroutine)	OCT 105204 (Call FFP microcode subroutine)
DEF X (Result)	DEF X (Result)
DEF Y (1st operand)	DEF Y (1st operand)
DEF Z (2nd operand)	DEF Z (2nd operand)
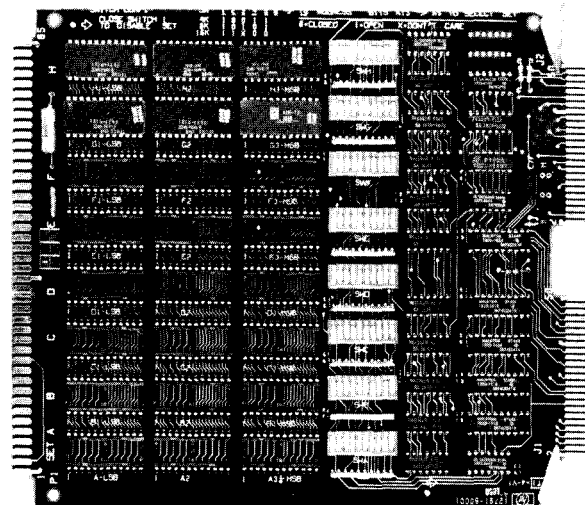
13306B Fast FORTRAN Processor mounted on 12791A Firmware Expansion Module

Functional specifications

Microcoded routines

See next page

Control store locations required: One 256 word module in 1k section and 512 words in the 4k section of the Firmware Expansion Module or the Firmware Accessory Board.

Accessory required: 12791A Firmware Expansion Module or 13304A Firmware Accessory Board

Software recommended: 24396F/A Diagnostic package on Minicartridges/paper tapes

Installation: The 13306B ROM IC's are inserted into sockets on the 12791A FEM (Firmware Expansion Module — see photo) or the 13304A FAB (Firmware Accessory Board); then, the board is installed in the E-Series CPU.

Electrical specifications

Current required from +5V computer power supply

Included in electrical specifications of the 12791A Firmware Expansion Module or 13304A Firmware Accessory Board.

Ordering information

13306B Fast FORTRAN processor includes:
1. 5090-0589 through 0591, three 4k ROM instruction ICs.
2. 12791-90001 M/E/F-Series Firmware Installation and Reference Manual

Microcoded routines

Microcoded routines	Description	Execution time in μsec[†]		Max Non-interruptible	Opcode
		Min	Max		
DBLE	Converts single to extended precision	13.02	13.02		105201
SNGL	Converts extended to single precision	18.2	18.2		105202
[1].XMPY and .XMPY	Extended multiply	56.0 56.7	64.8 65.5	36.4μs max	105203 and 105211
[1].XDIV and XDIV	Extended divide	80.0 80.7	92.4 93.1	37.8μs max	105204 and 105212
[1].XADD and XADD	Extended add	37.5 38.0	50.2 50.7	25.7μs max	105213 and 105207
[1].XSUB and XSUB	Extended subtract	37.5	50.2	25.7μs max	105214 and 105210
[2].DFER and XFER	Transfers an extended precision variable to another location	12.810 8.96	12.8 12.7		105205 and 105220
.CFER	Four word move	14.9	14.9		
.PWR2	Calculates X*2N for real X and integer N	8.4	8.4		105225
.FLUN	Unpacks a real variable	3.1	3.1		105226
.XPAK	Normalizes, rounds and packs mantissa of an extended precision number	18.9	29.5	11.6μs max	105206
.PACK	Normalizes a real variable	19.2	27.2		105230
.XCOM	Complements an extended precision number	11.7	12.1		105215
..DCM	Complements and normalizes an extended precision number	22.1	33.4	12.2μs max	105216
DDINT	Converts extended precision real to extended integer	23.9	58.6	30.6μs max	105217
.GOTO	Transfers control to location indicated by FORTRAN computed GOTO statement	10.6	10.6		105221
..MAP	Computes the address of a specified element of 2 or 3 dimensional array	17.7	27.2		105222
[3].ENTR	Transfers address of parameters from a	13.9 + 3.7 *NP'			105223
.ENTP	calling sequence into a subroutine list	13.6 + 3.7 *NP'			105224
.SETP	Sets a table of increasing values for DOS-III	6.4 + 1.2 *count Interruptible for count > 30			105227

[†]Using standard performance memory

[1]The difference between .AA and AA is a return address as follows:

```
JSB.AA      JSB AA
DEF X       DEF *+N (return address)
DEF Y       DEF X
Etc.        DEF Y
 .           .
 .           .
 .           .
            Etc. (Nth arguments)
```

[2]The difference between .DFER and .XFER is as follows:

```
LDA (address of N)    JSB .DFER
LDB (address of Y)    DEF Y
JSB .XFER             DEF X
```

[3]The difference between .ENTR and .ENTP is:

```
.ENTR                 .ENTP
For all BCS subrou-   .For all privileged routines and
tines, all DOS/RTE    re-entrant routines
utility routines
```

13306B opt. 100 Fast FORTRAN processor includes:

1. 13307-80033 through 80035, three 4k ROM instruction ICs

Additional equipment required for installation

1. 12791A Firmware Expansion Module or 13304A Firmware Accessory Board
2. If the Fast FORTRAN Processor is ordered for a machine which does not have the 13307B Dynamic Mapping Instructions, 13306B option 100 must be ordered; the 13307B contains part of the FFP.

13306S Firmware Subscription Service

Provides firmware updates of the 13306B Fast FORTRAN Processor as required to keep it up to date with respect to changes as they are released by Hewlett-Packard. The 13306S service is priced in monthly units and is billable quarterly.

Vector Instruction Set (VIS)

The 12829A and 12824A are powerful Vector Instruction Sets, each containing 38 firmware instructions that work with the hardware floating point processor in HP 1000 F-Series Computers to provide extremely fast processing of data arrays. The 12829A VIS is used with the RTE-6/VM operating system and the 12824A VIS is used in an RTE-IVB environment. Software equivalent routines are also provided for use on HP 1000 M/E-Series Computers.

Features

- **Four to ten times faster processing than software**
- **Easy interface to Virtual Memory for data and to Extended Memory Area for processing of megabyte-sized data arrays**
- **Simplified programming of vector/matrix operations**
- **Single or double precision floating point arithmetic**
- **Software equivalent routines provide program compatibility with HP 1000 M/E-Series Computers**

Applications

- **Image processing**
- **Process optimization**
- **3-dimensional graphics**
- **Simulations of physical and chemical systems**
- **Linear programming**
- **Signal and vibration analysis**

Functional description

VIS Firmware

The vector instructions of the Vector Instruction Set (VIS) are used to replace FORTRAN DO loops performing interative scalar operations. The VIS instructions are functionally equivalent, but execute much faster because they run pipelined floating point operations under fast microcode control and eliminate FORTRAN DO loop overhead. For example, the FORTRAN DO loop:

```
    DO 999 I = 1, 100
999 V3(I) = V1(I) + V2(I)
```

is replaced with VIS by the single statement:

```
    CALL VADD (V1,1,V2,1,V3,1,100)
```

Where VADD is a vector addition instruction that executes much faster than the DO loop it replaces.
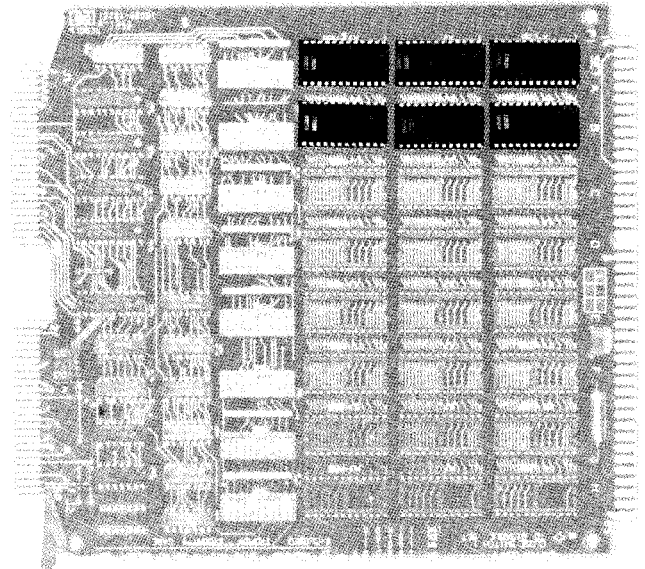
12824A Vector Instruction Set mounted on 12791A Firmware Expansion Module

Matrix addition provides another example. To process V3 = V1 + V2, where V1, V2, and V3 are all 50 x 50 matrices the respective codings are:

FORTRAN DO Loop (Execution time = 230 milliseconds)

```
    DO 100  J = 1, 50
    DO 100  I = 1, 50
100 V3(I,J)=V1(I,J)+V2(I,J)
```

VIS Instruction (Execution time = 20 milliseconds)

```
100 CALL VADD(V1,1,V2,1,V3,1,2500)
```

VIS software equivalents

VIS software equivalents are FORTRAN subroutines that perform the same computational functions as the VIS firmware instructions, thus making it possible to develop and execute programs which call VIS routines on HP 1000 M- and E-Series Computers as well as F-Series Computers. This program compatibility is especially useful in DS/1000 networks. The VIS software equivalents require at least four times as long to execute as the firmware instructions. They are Type II software.

Functional specifications

Data types

Single-precision and double precision floating point.

VIS instructions, execution times, and interrupts

See table on next page.

VIS instructions and typical execution times for VIS firmware

OPERATION		SINGLE PRECISION			DOUBLE PRECISION			
			Execution Times (μsec)				Execution Times (μsec)	
	MNEM	Fixed	Loop*	MNI†	MNEM	Fixed	Loop*	MNI†
Vector ADDition	VADD	14.6	7.7	21	DVADD	15.8	11.1	24
Vector SUBtraction	VSUB	14.6	7.7	21	DVSUB	15.8	11.1	24
Vector Multiplication	VMPY	14.8	7.7	21	DVMPY	18.0	11.1	24
Vector DIVision	VDIV	16.0	7.7	21	DVDIV	20.5	12.7	24
Vector Scalar Addition	VSAD	13.6	7.7	21	DVSAD	15.6	12.2	24
Vector Scalar SuBtraction	VSSB	13.6	7.7	21	DVSSB	15.6	12.2	24
Vector Scalar Multiplication	VSMY	13.9	7.7	21	DVSMY	17.6	12.6	24
Vector Scalar DiVide	VSDV	14.0	7.7	21	DVSDV	18.8	11.1	24
Vector PIVot (basic operation for matrix inversion)	VPIV	16.6	10.2	26	DVPIV	18.5	14.6	31
Vector ABSolute value (of each vector element)	VABS	12.4	6.9	19	DVABS	13.3	9.4	23
Vector SUM (sum of all vector elements)	VSUM	19.7	5.9	23	DVSUM	21.1	6.1	23
Vector NoRM (sum of element absolute values)	VNRM	20.0	5.9	23	DVNRM	21.2	6.1	23
Vector DOT product (basic operation for matrix multiplication	VDOT	19.7	10.5	29	DVDOT	21.2	12.5	31
Vector MAXimum (to find maximum element in vector)	VMAX	8.5	7.9	17	DVMAX	8.4	9.8	18
Vector MAximum aBsolute value	VMAB	7.6	8.4	17	DVMAB	7.4	10.6	18
Vector MINimum (to find minimum element in vector)	VMIN	8.5	7.9	17	DVMIN	8.4	9.9	18
Vector MInimum aBsolute value	VMIB	7.6	8.4	17	DVMIB	7.4	10.5	18
Vector MOVe (basic operation for matrix transposition)	VMOV	11.7	4.4	17	DVMOV	12.5	6.4	19
Vector SWaP	VSWP	11.8	7.5	20	DVSWP	13.0	11.3	25

* Fixed time is the basic instruction start-up time; loop time is the processing time per vector element. Total time = fixed time + the number of elements times loop time.

† MNI = the maximum period of non-interruptible instruction execution. When a VIS instruction is interrupted, the current state of execution is saved. Following the interrupt, VIS instruction execution resumes from the point of suspension.

Configuration information

Control store locations required: Four 256 word modules (12 through 15) in 2117F Computer.

Accessory required: 12791A Firmware Expansion Module.

Software recommended: 12829A is used with the 92084A RTE-6/VM operating system, which provides Virtual Memory for data and Extended Memory Area capability for processing megabyte-sized data arrays. 12824A is used with the 92068A RTE-IVB operating system, which provides Extended Memory Area capability for processing megabyte-sized data arrays.

Installation: Insert the VIS firmware ROMs into the appropriate sockets on the 12791A Firmware Expansion Module (FEM) as shown in the photo, configure address switches on the FEM, then install the FEM in the F-Series computer.

Electrical specifications

Current required from +5V computer power supply

2.36A, including 1.2A base requirement for the 12791A Firmware Expansion Module and 1.06A for the 1k words of ROM storage represented by the Vector Instruction Set.

Ordering information

12829A Vector Instruction Set for use with RTE-6/VM

The 12829A Vector Instruction Set includes:
1. 12824-80001 through 80006 six VIS instruction ROMs.
2. 12791-90001 M/E/F-Series Firmware Installation and Reference Manual.
3. 12824-90001 VIS User's Manual.
4. Firmware interface library, software equivalents library, and VIS on-line diagnostic on one of media options 020 through 051, **which must be ordered.**

12829A Options

001: Provides discount for upgrade from 12824A VIS software equivalents to 12829A VIS software equivalents for customer not on 12824T/S. Deletes VIS firmware.

002: Provides discount for upgrade from 12824A VIS software equivalents to 12829A VIS software equivalents for customer supported under 12824T/S. Deletes VIS firmware.

020: Provides 12829A software equivalents on 264x Mini cartridge.

022: Provides 12829A software equivalents on 7908/11/12 compatible tape cartridge.

050: Provides 12829A software equivalents on 800 bpi mag tape.

051: Provides 12829A software equivalents on 1600 bpi mag tape.

12824A Vector Instruction Set for use with RTE-IVB

12824A Vector Instruction Set includes:
1. 12824-80007 through 80009, three VIS instruction ROMs.
2. 12791-90001 M/E/F-Series Firmware Installation and Reference Manual.
3. 12824-90001 VIS User's Manual.
4. 12824-13301 Firmware interface library, software equivalents library, and VIS on-line diagnostic on Mini cartridge.

12824A options

001: Provides discount for upgrade to latest version of VIS software equivalents for customer not enrolled in 12824T/S. Prerequisite is 12824A option 002.

002: Deletes VIS firmware and firmware installation manual. Provides VIS software equivalents and VIS User's manual only.

Firmware and software support products available

12829T Customer Support Service for 12829A firmware and software, including S.E. support and firmware, software and manual updates. Same software equivalent media option as 12829A.

12829V Central Support Service for additional VIS package, including one set of firmware updates and extension of 12829T S.E. consulting to an additional 12829A VIS package.

12829S Software Subscription Service for 12829A firmware and software, including firmware, software, and manual updates. Same software equivalent media option as 12829A.

12829W Additional set of 12829A firmware updates.

12829Q Manual update service for 12829A manuals.

12824T Customer Support Service for 12824A firmware and software, including S.E. support and firmware, software, and manual updates. (Software updates are on Mini cartridges.)

12824V Central Support Service for an additional VIS package, including one set of firmware updates and extension of S.E. consulting service to an additional 12824A VIS package. (Prerequisite is 12824T service for first 12824A package supported.)

12824S Software Subscription Service for 12824A firmware and software, including firmware, software, and manual updates. (Software updates are on Mini cartridges.)

12824W Additional set of 12824A firmware updates.

12824Q Manual update service for 12824A manuals.

12824T/V/S options

002: Deletes firmware updates, so only software and manual updates are provided with the 12824T/S product and only extension of S.E. consultation service is included with the 12824V product.

020: Software equivalent updates on 264x Mini cartridges (12824T/S only).

Writable Control Store and Firmware Expansion Modules

HP 1000 M/E/F-Series Computer Systems   product numbers 13197A and 12791A

Two control store boards offer comprehensive support for user microprograms in HP 1000 M/E/F computer systems. One of these is the 13197A 1k word Writable Control Store (WCS) board, which supports development, testing, dynamic overlaying, and output of user's microprograms to the HP 1000 Control Processor. The other is the 12791A 8k Firmware Expansion Module (FEM) board, which provides mounting for PROMs containing user's microcode. In addition to hardware support provided by these control store boards, development of user's microprograms and dynamic loading and overlaying of WCS is software supported by the 92061A RTE Microprogramming Package.

Features

- **Software support with 92061A RTE Microprogramming Package**
- **Writable Control Store (WCS) support for microcode development, testing, dynamic overlaying, and output, 1024 words of WCS per card**
- **Up to 3 WCS's or 2 FEM's per HP 1000 computer (except 1 FEM per M-Series)**
- **WCS can override installed PROM-based microcode**
- **Control processor programs sharable among multiple users**

Functional specifications

Capacity

13197A WCS Board: 1k word, 2 modules of 512 words each

12791A FEM Board: Mounting for 8k words, eight modules of 1024 words, three PROMs per module

Word size

24 bits

Microinstruction cycle time

175-280 ns in 2109/2113/2117, 325 ns in 2108/2112

Recommended PROMs for 12791A FEM Board

4k PROMs: HP Part No. 1816-1163, MMI 6341, Signetics 82S141, and Harris HM 7681

8k PROMs: HP Part No. 1816-1160, MMI 6381, Signetics 82S181, and Harris HM 7681

Priority

E/F-Series priority (1 is highest priority):
1. 1k WCS
2. 8k FEM
3. FAB
4. E/F-Series

M-Series priority (1 is highest priority):
1. 1k WCS/8k FEM
2. Base Set and 12945A UCS
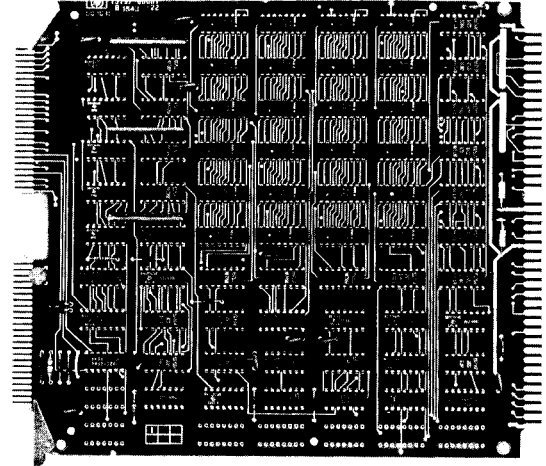
13197A Writable Control Store
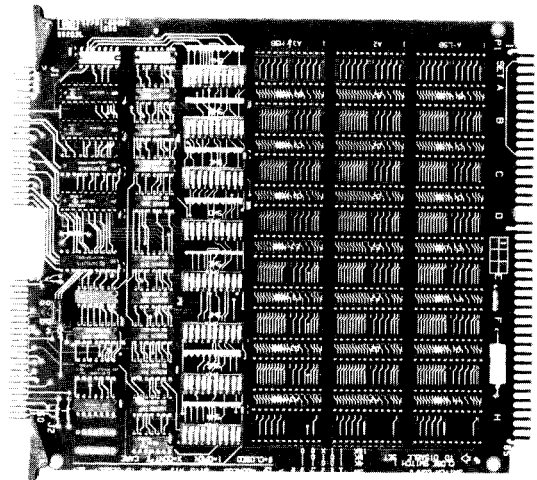
12791A Firmware Expansion Module

Configuration information

I/O slots required: One for each control store board

Software recommended: 92061A Microprogramming Package

WCS description

The 13197A WCS board is a dual-port memory. One port connects to the control processor's control store interface and the other to the computer backplane. Control processor instructions can be loaded into the WCS using either programmed I/O or DCPC transfers at full bandwidth via the I/O backplane memory port. Standard I/O instructions are then used to configure control store module addresses

and enable the control processor's memory port, thereby granting access to the loaded subroutines by the control processor.

If the WCS is configured with the same control store module address as a FEM module address, the WCS microcode is executed, taking priority over the FEM microcode. In this manner, the effective number of available control processor entry points is significantly increased.

FEM description

The 12791A FEM board provides up to 8k words of non-volatile control memory storage capacity for user-written instruction set enhancements. Module addresses are switch selectable, with a given module configurable to any address within control store address space. Users can supply recommended vendors with necessary information for generating PROM chips that are compatible with the 12791A, or can "burn" their own. The microprograms in PROMs are mounted on the FEM board, which is conveniently installed in the card cage of the HP 1000 computer system.

Electrical specifications

Current required from computer power supply

WCS: 2.2A (+5V), 0.007A (−2V)

FEM: 1.2A plus 0.525A (+5V) for each block of ROM control store installed on the module, 5.4A maximum, when fully loaded

Ordering information

13197A WCS Board

The 13197A WCS Board includes:
1. 13197-60001 Writable Control Store Board
2. 5061-3419 Flat Cable Assembly
3. 13197-90001 WCS Driver Manual
4. 12791-90001 Installation and Reference Manual

12791A Firmware Expansion Module

12791A Firmware Expansion Module includes:
1. 12791-60001 Firmware Expansion Module
2. 5061-3419 Flat Cable Assembly
3. 12791-90001 HP 1000 M/E/F-Series Firmware Installation and Reference Manual

NOTE: One 12791A FEM is included in the standrd 2109/13E and 2117 computers.

Environmental Specifications and
Product Support Information

HP 1000 M/E/F-Series Computers

Environmental specifications

Except where otherwise specified in the individual data sheets, all products in this data book meet Hewlett-Packard Environmental Specifications, as follows:

Temperature

Operating: 0° to 55°C (32° to 131°F)

Storage: −40° to 75°C (−40° to 167°F)

Relative humidity

5% to 95% at 40°C (104°F), non-condensing

Altitude
Operating: to 4500 metres (15,000 ft)
Non-operating: to 15300 metres (50,000 ft)

Vibration and shock

Type tested to qualify for normal shipping and handling shock and vibration (contact factory for review of any application that requires operation under continuous vibration).

Vibration: 0.38 mm (0.015 in) p-p, 10-55 Hz, 3 axis.
Shock: 30g, 11 Ms, 1/2 sine, 3 axis.

Product support

Support offered for HP 1000 Computers and accessories includes:

1. User training services.
2. Installation assistance.
3. Warranty.
4. Diagnostics subscription service.
5. Hardware history library.
6. Hardware notification subscription service.
7. Hardware service agreements.
8. Software notification service.
9. Manual Update Service.
10. Software subscription service.
11. Customer Support Service.
12. Software consulting service.

User training services

Regularly-scheduled training is available on HP 1000 software and on hardware maintenance. The courses offered are listed in the HP Computer Systems Group Course Schedule, along with registration information and course locations. The course schedule is available from your Hewlett-Packard Sales Representative.

Installation assistance

All items in this data book are customer-installed products when ordered as components (not in an HP 1000 Computer System). Installation assistance is available on request at prevailing service rates.

Warranty

All Hewlett-Packard computers, components, and systems are covered by warranty. For specific information, contact your Hewlett-Packard Sales Representative.

Diagnostics Subscription Service

The 24396S Diagnostics Subscription Service provides quarterly distribution of update information and revised diagnostic routines necessary to keep the 24396A/D/E/F Diagnostics Library up to date with respect to diagnostic improvements by the factory. Updated diagnostic routines are available on paper tape, Mini cartridges, or 800 bpi or 1600 bpi magnetic tape. Documentation is updated by providing revised diagnostic manuals or updating supplements to affected manuals. The 24396S service is ordered in monthly units for a minimum of six months, billable quarterly, or it can be prepaid for an entire year.

Hardware history library

The 92851A HP 1000 Hardware history library is intended for OEMs and other users who desire in-depth information on HP 1000 Computer hardware and engineering changes to that hardware. The 92851A product includes:

Engineering Reference Documentation, which contains the theory of operation, timing information, and schematics of many of the HP 1000 Computer products.

The HP 1000 Hardware and manual index log, which provides a current index to all hardware manuals. It also includes engineering change descriptions and documentation for many of the HP 1000 hardware products and their respective update and enhancement histories. This coverage is further supplemented by instructions on how to perform the actual modifications.

The current Service Notes fiche, which contains historical information on important product changes and status regarding warranty behind each change.

Hardware notification subscription service

The 92851Q HP 1000 Hardware notification subscription service provides updates to the 92851A Hardware history library that reflect HP 1000 hardware changes as they are released by Hewlett-Packard. These updates include:

- Updates to the HP 1000 Hardware and manual index log and the Engineering Reference Documentation as required to reflect hardware changes.

- The latest printed Service Notes to provide users with the most up-to-date information available.

- The latest Service Notes fiche when it is issued (every 6 months); this fiche will incorporate all previously issued printed Service Notes.

Hardware service agreements

Service agreements are available for coverage of HP 1000 Computers and accessories. Because Hewlett-Packard treats support as a product, you buy only the level that you need. Support levels range from on-call support seven days a week, 24 hours a day, to a service where support is provided through a network of HP field repair centers, located regionally throughout the world. See your HP sales person for a complete description of hardware service agreements.

Software support services

HP 1000 Software, described in the HP 1000 Computers and Systems Active Software and Mature Software data books, is supported by the following services:

Software Notification Service. Gives periodic information on software changes.

Manual Update Service. Provides updates as required to keep software manuals current with respect to changes by Hewlett-Packard.

Software Subscription Service. Provides software updates on user-specified media as well as update to documentation. Includes Software Notification Service when ordered for a software operating system.

Customer Support Service. Combines Software Subscription Service with a Phone-In Consulting Service that provides for answering customer's questions on HP 1000 software covered by this service and on-site resolution of problems with covered software if required.

Software Consulting service. Provides the on-site services of a trained HP System Engineer in daily units for helping customers better understand how to apply their software.

Ordering information

Product numbers and prices for all HP 1000 Systems Computer interfaces, peripherals, and hardware and software support services are given in the HP 1000 Ordering Information, which is available from your Hewlett-Packard Sales Representative.

Power Specifications and Applicability Summary

HP 1000 M/E/F-Series Computers

Power Specifications and Applicability Summary (Available resource is indicated by +, Requirement by -)

Product Number and Name	For Ser	AC Power	I/O Ch	Direct Current at +5V	+5V(M)	+12V	-12V	-2V
COMPUTERS, SYSTEMS, I/O EXTENDER, AND POWER FAIL RECOVERY SYSTEMS								
2108M Computer with 64kb memory	M	1071VA	+9	+35.3A	-1.07A	+2.5A	+2.0A	+5.9A
2108M Opt 014: Deletes 64kb memory				+1.7A	+1.07A	0A	0A	+0.1A
2109E Computer with 64kb memory and 12791A FEM*	E	1071VA	+8	+29.9A*	-1.07A	+2.5A	+2.0A	+5.9A
2109E Opt 003: 13304A FAB instead of 12791A FEM			+1	+3.6A	0A	0A	0A	0A
2109E Opt 012: 64kb high performance memory instead of 64kb standard perf mem			nnc	-1.4A	0A	0A	0A	+0.1A
2109E Opt 014: Deletes 64kb std performance mem			nnc	+1.7A	+1.07A	0A	0A	+0.1A
2109EK Board Computer -- CPU and 64kb memory	E	n/a	0	-9.5A	-1.07A	0A	0A	-0.2A
2109EK Opt 014: Deletes 64kb std performance mem			nnc	+1.7A	+1.07A	0A	0A	0A
2112M Computer with 128kb memory	M	1071VA	+14	+28.9A	-1.07A	+2.5A	+2.0A	+5.9A
2112M Opt 012: 64kb memory instead of 128kb			nnc	+5.2A	0A	0A	0A	0A
2112M Opt 014: Deletes 128kb std performance mem			nnc	+8.1A	+1.07A	0A	0A	+0.1A
2113E Computer with 128kb memory and 12791A FEM*	E	1071VA	+13	+24.7A*	-1.07A	+2.5A	+2.0A	+5.9A
2113E Opt 003: 13304A FAB instead of 12791A FEM			+1	+3.6A	0A	0A	0A	0A
2113E Opt 012: 64kb high performance memory instead of 128kb standard perf mem			nnc	+3.8A	0A	0A	0A	+0.1A
2113E Opt 013: 64kb memory instead of 128kb			nnc	+5.2A	0A	0A	0A	+0.1A
2113E Opt 014: Deletes 128kb std performance mem			nnc	+6.9A	+1.07A	0A	0A	+0.1A
2117F Computer with 128kb high performance memory	F	1357VA	+13	+23.3A*	-1.21A	+2.5A	+2.0A	+5.9A
2117F Opt 013: 64kb memory instead of 128kb			nnc	+5.2A	0A	0A	0A	+0.1A
2117F Opt 014: Deletes 128kb high performance mem			nnc	+8.3A	+1.21A	0A	0A	+0.1A
2176C Model 40 Sys Proc Unit with 128kb memory	E	1143VA	+11	+22.1A	+5.93A	+2.5A	+1.9A	+5.9A
2176C Opt 014: Deletes 128kb std perf mem			nnc	+6.9A	+1.07A	0A	0A	+0.1A
2176E Model 40 Sys Proc Unit with 256kb memory	E	1143VA	+11	+17.0A*	+5.29A	+2.5A	+1.9A	+5.9A
2176E Opt 014: Deletes 256kb high perf memory			nnc	+8.3A	+1.71A	0A	0A	+0.1A
2176E Opt 031/032/033: MAC Disc I/F and media			-1	-2.5A	0A	0A	0A	0A
2177C Model 45 Sys Proc Unit w/128kb memory	F	1429VA	+11	+16.9A*	+5.79A	+2.5A	+1.9A	+5.9A
2177C Opt 014: Deletes 128kb High perf mem			nnc	+8.3A	+1.21A	0A	0A	+0.1A
2177F Model 45 Sys Proc Unit with 256kb memory	F	1429VA	+11	+17.0A*	+5.29A	+2.5A	+1.9A	+5.9A
2177F Opt 014: Deletes 256kb high perf memory			nnc	+8.3A	+1.71A	0A	0A	+0.1A
2177F Opt 031/032/033: MAC Disc I/F and media			-1	-2.5A	0A	0A	0A	0A
2178A Model 60 Sys Proc Unit with 256kb memory	E	1143VA	+11	+17.9A*	+5.36A	+2.5A	+1.9A	+5.9A
2178A Opt 014: Deletes 256kb std perf memory			nnc	+7.4A*	+1.64A	0A	0A	+0.1A
2178C Model 60 Sys Proc Unit with 256kb memory	E	1143VA	+11	+17.0A*	+5.29A	+2.5A	+1.9A	+5.9A
2178C Opt 014: Deletes 256kb high perf memory			nnc	+8.3A	+1.71A	0A	0A	+0.1A
2178A/C Opt 022/060/061: CS/80 Disc I/F and cartridge tape or mag tape media			-1	-3.5A	0A	0A	0A	-0.1A
2178A/C Opt 031/032/033: MAC Disc I/F and media			-1	-2.5A	0A	0A	0A	-0.1A
2179A Model 65 Sys Proc Unit w/256kb memory	F	1429VA	+11	+16.4A*	+5.22A	+2.5A	+1.9A	+5.9A
2179A Opt 014: Deletes 256kb high performance mem			nnc	+8.8A*	+1.78A	0A	0A	+0.1A
2179C Model 65 Sys Proc Unit w/256kb memory	F	1429VA	+11	+16.9A*	+5.29A	+2.5A	+1.9A	+5.9A
2179C Opt 014: Deletes 256kb high performance mem			nnc	+8.3A	+1.71A	0A	0A	+0.1A
2179A/C Opt 022/060/061: CS/80 Disc I/F and cartridge tape or mag tape media			-1	3.5A	0A	0A	0A	-0.1A
2179A/C Opt 031/032/033: MAC Disc I/F and media			-1	-2.5A	0A	0A	0A	-0.1A
2179A/C Opt 101/111/121: Value Pack w/1Mb memory			nnc	nnc	-0.7A	0A	0A	-0.1A
2179A/C Opt 102/112/122: Value Pack w/2Mb memory			nnc	-2.0A	-2.0A	0A	0A	-0.1A
12979B Dual-Port I/O Extender	MEF	730VA	+16	-2.0A	0A	0A	0A	-1.4A
12944B Power Fail Recovery System for 2108M or 2109E Computer	ME		n/a	0A	+7.0A	0A	0A	0A
12991B Power Fail Recovery System for 2112M, 2113E, or 2117F Computer	MEF		n/a	0A	+7.0A	0A	0A	0A
INTERFACES, MEMORY, AND OTHER ACCESSORIES								
12250A DSN/X.25 Network Interface	MEF		-1	-1.9A	0A	-0.3A	-0.2A	0A
12260A Multi-Use Prog Ser I/F for DSN/MRJE 1000	MEF		-1	-1.9A	0A	-0.3A	-0.2A	0A
12261A Multi-Use Programmable Multiplexer	MEF		-1	-2.0A	0A	-0.3A	-0.4A	0A

FOOTNOTES:

nnc = no net change; n/a = not applicable

* = Available +5V current specified here is that available after provision of 5.4A for fully-loaded 12791A Firmware Expansion Module in 2109E, 2113E, or 2117F Computer or in 2176E, 2177C/F, 2178A/C, or 2179A/C SPU or that available after provision of 1.8A for fully-loaded 13304A Firmware Accessory Board in 2176C SPU.

(M) = +5V Memory current requirements for memory controller, memory modules, and fault control check bit array boards. In computer without power fail recovery system, this current is drawn from the available +5V current, reducing current available for I/O interfaces. All 217x System Processor Units include a power fail recovery system.

Power specifications and applicability summary (continued)

Power Specifications and Applicability Summary, continued (Available resource is indicated by +, Requirement by -)

Product Number and Name	For Ser	AC Power	I/O Ch	Direct Current at				
				+5V	+5V(M)	+12V	-12V	-2V
INTERFACES, MEMORY, AND OTHER ACCESSORIES, continued								
12531C Teleprinter Interface	MEF		-1	-0.8A	0A	-0.1A	-0.1A	-0.1A
12531D Terminal Interface	MEF		-1	-0.8A	0A	-0.2A	0A	-0.1A
12551B Relay Output Register	MEF		-1	-0.6A	0A	-0.2A	0A	-0.4A
12551B Opt 001: Adds read-back			nnc	-0.5A	0A	nnc	0A	-0.2A
12554A 16-Bit Duplex Register	MEF		-1	-1.1A	0A	-0.3A	-0.3A	-0.1A
12556B 40-Bit Register	MEF		-1	-0.9A	0A	-0.2A	-0.1A	-0.1A
12566C Microcircuit Interface	MEF		-1	-0.7A	0A	0A	0A	-0.1A
12587B Async Communications Interface	M		-1	-1.6A	0A	-0.1A	-0.1A	-0.1A
12589B Auto Calling Unit Interface	M		-1	-0.7A	0A	-0.1A	-0.1A	-0.1A
12597A 8-Bit Duplex Register	MEF		-1	-0.8A	0A	-0.1A	-0.1A	-0.1A
12604B Data Source Interface	M		-1	-1.1A	0A	0A	0A	0A
12618A Synchronous Communications Interface	MEF		-2	-2.2A	0A	-0.1A	-0.1A	-0.2A
12620A Breadboard Interface/RTE Privileged Interrupt Fence (a)	MEF		-1	-0.4A	0A	0A	0A	0A
12666H 1Mb Fault Ctrl Check Bit Bd (oper) (b)	MEF		0	-0.5A	-0.91A	0A	0A	0A
12666H 1Mb Fault Ctrl Check Bit Bd (standby) (b)	MEF		0	-0.5A	-0.76A	0A	0A	0A
12699H 256kb Memory Module (operating) (b)	MEF		0	-0.5A	-1.07A	0A	0A	0A
12699H 256kb Memory Module (standby) (b)	MEF		0	-0.5A	-0.53A	0A	0A	0A
12728G Control Panel Assembly (2109EK accessory)	E		0	-1.5A	-1.1A	-0.1A	0A	0A
12728J 18-Slot Card Cage Kit (2109EK accessory)	E		+9	n/a	n/a	n/a	n/a	n/a
12731A Memory Expansion Module	MEF		0	-3.9A	0A	0A	0A	0A
12746A/H 64kb Memory Module	MEF		0	-0.5A	-0.57A	0A	0A	0A
12747A/H 128kb Memory Module	MEF		0	-0.5A	-0.57A	0A	0A	0A
12749H 512kb Memory Module (operating) (b)	MEF		0	-0.5A	-1.19A	0A	0A	0A
12749H 512kb Memory Module (standby) (b)	MEF		0	-0.5A	-0.65A	0A	0A	0A
12771A Computer Serial Interface	MEF		-1	-1.6A	0A	-0.9A	-0.1A	-0.1A
12773A Computer Modem Interface	MEF		-1	-1.6A	0A	-0.4A	0A	-0.1A
12777A Priority Jumper Card	MEF		-1	0A	0A	0A	0A	0A
12779A/H 256kb Fault Control Check Bit Array Bd	MEF		0	-0.3A	-0.78A	0A	0A	0A
12780A/H 512kb Fault Control Check Bit Array Bd	MEF		0	-0.3A	-0.78A	0A	0A	0A
12784A 128kb Parity Memory Package	M		0	-8.1A	-1.07A	0A	0A	-0.1A
12784B 256kb Parity Memory Package	M		0	-8.6A	-1.64A	0A	0A	-0.1A
12784C 512kb Parity Memory Package	M		0	-9.6A	-2.78A	0A	0A	-0.1A
12784D 1.0Mb Parity Memory Package	M		0	-11.6A	-5.06A	0A	0A	-0.1A
12785A 128kb Fault Control Memory Package	M		0	-10.5A	-2.03A	0A	0A	-0.1A
12785B 256kb Fault Control Memory Package	M		0	-11.0A	-2.60A	0A	0A	-0.1A
12785C 512kb Fault Control Memory Package	M		0	-12.0A	-3.74A	0A	0A	-0.1A
12785D 1.0Mb Fault Control Memory Package	M		0	-14.3A	-6.80A	0A	0A	-0.1A
12786A 128kb Std Performance Parity Memory Pkg	E		0	-6.9A	-1.07A	0A	0A	-0.1A
12786B 256kb Std Performance Parity Memory Pkg	E		0	-7.4A	-1.64A	0A	0A	-0.1A
12786C 512kb Std Performance Parity Memory Pkg	E		0	-8.4A	-2.78A	0A	0A	-0.1A
12786D 1.0Mb Std Performance Parity Memory Pkg	E		0	-10.4A	-5.06A	0A	0A	-0.1A
12787A 128kb Std Perf Fault Control Memory Pkg	E		0	-9.3A	-2.03A	0A	0A	-0.1A
12787B 256kb Std Perf Fault Control Memory Pkg	E		0	-9.8A	-2.60A	0A	0A	-0.1A
12787C 512kb Std Perf Fault Control Memory Pkg	E		0	-10.8A	-3.74A	0A	0A	-0.1A
12787D 1.0Mb Std Perf Fault Control Memory Pkg	E		0	-13.1A	-6.80A	0A	0A	-0.1A
12788A 128kb High Performance Parity Memory Pkg	EF		0	-8.3A	-1.21A	0A	0A	-0.1A
12788B 256kb High Performance Parity Memory Pkg	EF		0	-8.8A	-1.78A	0A	0A	-0.1A
12788BB 256kb High Performance Parity Memory Pkg	EF		0	-8.3A	-1.71A	0A	0A	-0.1A
12788C 512kb High Performance Parity Memory Pkg	EF		0	-9.8A	-2.92A	0A	0A	-0.1A
12788D 1.0Mb High Performance Parity Memory Pkg	EF		0	-11.8A	-5.2A	0A	0A	-0.1A
12788E 512kb High Performance Parity Memory Pkg	EF		0	-8.3A	-1.83A	0A	0A	-0.1A
12788F 1.0Mb High Performance Parity Memory Pkg	EF		0	-8.8A	-2.48A	0A	0A	-0.1A
12788G 1.5Mb High Performance Parity Memory Pkg	EF		0	-9.3A	-3.13A	0A	0A	-0.1A
12788H 2.0Mb High Performance Parity Memory Pkg	EF		0	-9.8A	-3.78A	0A	0A	-0.1A
12789A 128kb High Perf Fault Control Memory Pkg	EF		0	-9.3A	-2.04A	0A	0A	-0.1A
12789B 256kb High Perf Fault Control Memory Pkg	EF		0	-9.8A	-2.61A	0A	0A	-0.1A
12789C 512kb High Perf Fault Control Memory Pkg	EF		0	-10.8A	-3.75A	0A	0A	-0.1A
12789D 1.0Mb High Perf Fault Control Memory Pkg	EF		0	-13.1A	-6.81A	0A	0A	-0.1A
12789E 512kb High Perf Fault Control Memory Pkg	EF		0	-9.3A	-2.66A	0A	0A	-0.1A
12789F 1.0Mb High Perf Fault Control Memory Pkg	EF		0	-10.1A	-4.09A	0A	0A	-0.1A
12789G 1.5Mb High Perf Fault Control Memory Pkg	EF		0	-10.9A	-5.52A	0A	0A	-0.1A
12789H 2.0Mb High Perf Fault Control Memory Pkg	EF		0	-11.7A	-6.95A	0A	0A	-0.1A

FOOTNOTES:

nnc = no net change; n/a = not applicable

(M) = +5V Memory current requirements for memory controller, memory modules, and fault control check bit array boards. In computer without power fail recovery system, this current is drawn from the available +5V current, reducing current available for I/O interfaces. All 217x System Processor Units include a power fail recovery system.

(a) = Does not include current required by circuits added by the user to the Breadboard Interface.

(b) = Operating current requirement applies only to one Fault control check bit array board or memory module at a time; all others draw standby current.

Power specifications and applicability summary (continued)

Power Specifications and Applicability Summary, continued (Available resource is indicated by +, Requirement by -)

Product Number and Name	For Ser	AC Power	I/O Ch	Direct Current at				
				+5V	+5V(M)	+12V	-12V	-2V

INTERFACES, MEMORY, AND OTHER ACCESSORIES, continued

Product Number and Name	For Ser	AC Power	I/O Ch	+5V	+5V(M)	+12V	-12V	-2V
12789J 512kb High Perf Fault Control Memory Pkg	EF		0	-9.5A	-2.79A	0A	0A	-0.1A
12789K 1.0Mb High Perf Fault Control Memory Pkg	EF		0	-10.0A	-3.44A	0A	0A	-0.1A
12789L 1.5Mb High Perf Fault Control Memory Pkg	EF		0	-11.0A	-4.85A	0A	0A	-0.1A
12789M 2.0Mb High Perf Fault Control Memory Pkg	EF		0	-11.5A	-5.5A	0A	0A	-0.1A
12790A Multipoint Terminal/Data Link interface	MEF		-1	-3.0A	0A	0A	-0.1A	-0.1A
12791A Firmware Expansion Module	MEF		-1	(c)	0A	0A	-0.1A	-0.1A
12792B 8-Channel Async Multiplexer Interface	MEF		-1	-2.0A	0A	0A	-0.3A	-0.4A	0A
12793B/12794B DS/1000-IV Bisync/HDLC Modem I/Fs	MEF		-1	-1.9A	0A	0A	-0.3A	-0.2A	0A
12821A Disc/Printer Interface	MEF		-1	-3.3A	0A	0A	0A	-0.1A
12825A DS/1000-IV Direct Connect HDLC Interface	MEF		-1	-1.8A	0A	-0.3A	-0.4A	0A
12826B Programmable Serial (Modem) Interface	MEF		-1	-1.9A	0A	-0.3A	-0.2A	0A
12834A DS/1000-IV Direct Connect Bisync Interface	MEF		-1	-1.8A	0A	-0.3A	-0.4A	0A
12845B Line Printer Interface	MEF		-1	-1.2A	0A	0A	0A	0A
12892B Memory Protect Module	MEF		0	-1.3A	0A	0A	0A	-0.1A
12897B Dual-Channel Port Controller	MEF		0	-2.4A	0A	0A	0A	-0.1A
12920B 16-Channel Asynchronous Multiplexer I/F	MEF		-3	-5.5A	0A	-0.2A	-0.5A	-0.3A
12920B Opt 001: Adds hardware support for Bell 202 Dataset	MEF		-1	-1.4A	0A	-0.2A	-0.2A	-0.1A
12925A Punched Tape Reader Subsystem (12597A I/F)	MEF		-1	-0.8A	0A	-0.1A	-0.1A	-0.1A
12926A Tape Punch Subsystem (12597A interface)	MEF		-1	-0.8A	0A	-0.1A	-0.1A	-0.1A
12930A Universal Interface	MEF		-1	-1.8A	0A	0A	0A	-0.1A
12930A Opt 001/002: Change to TTL input	MEF		nnc	-0.4A	0A	0A	0A	nnc
12966A Buffered Asynchronous Communications I/F	MEF		-1	-3.0A	0A	0A	-0.1A	-0.1A
12967A Synchronous Communications Interface	MEF		-1	-1.8A	0A	0A	0A	-0.1A
12968A Asynchronous Communications Interface	MEF		-1	-1.3A	0A	0A	0A	-0.1A
12985A Punched Card Reader Subsystem (12924A I/F)	MEF		-1	-1.0A	0A	0A	0A	0A
12992_ Any add'l Loader ROM	MEF		0	-0.2A	0A	0A	0A	0A
13175B MAC Disc Interface Card	MEF		-1	-2.3A	0A	0A	0A	0A
13178C Multi-CPU Interface to MAC Disc	MEF		-1	-2.3A	0A	0A	0A	0A
13197A 1k Writable Control Store (WCS)	MEF		-1	-2.2A	0A	0A	0A	0A
13304A Firmware Accessory Board (FAB)	E		0	-1.8A	0A	0A	0A	0A
2102B Std Performance Parity Memory Controller	ME		0	-1.2A	-0.5A	0A	0A	0A
2102C Std Perf Fault Control Memory Controller	ME		0	-3.3A	-0.68A	0A	0A	0A
2102E High Performance Parity Memory Controller	EF		0	-2.6A	-0.64A	0A	0A	0A
2102H High Perf Fault Control Memory Controller	EF		0	-3.3A	-0.69A	0A	0A	0A
2608A Line Printer with Option 210 (26099A I/F)	MEF		-1	-0.8A	0A	0A	0A	0A
2608S Line Printer with Option 210 (12821A I/F)	MEF		-1	-3.3A	0A	0A	0A	-0.1A
2611A/2619A Line Printer w/Opt 100 (12845B I/F)	MEF		-1	-1.2A	0A	0A	0A	0A
2631B Printer with Option 210 (12845B interface)	MEF		-1	-1.2A	0A	0A	0A	0A
59310B HP-IB Interface	MEF		-1	-3.0A	0A	0A	0A	-0.1A
7970B +226/236 Mag Tape Unit (13181B I/F)(d)	MEF		-2	-2.9A	0A	0A	0A	0A
7970E +226/236 Mag Tape Unit (13183B I/F)(d)	MEF		-2	-2.6A	0A	0A	0A	0A
91000A Plug-In 20kHz A-to-D Interface	MEF		-1	-2.4A	0A	0A	0A	-0.1A
91200B TV Interface (3 cards req'd for color)	MEF		-1	-1.2A	0A	-0.3A	0A	-0.1A
91780A RJE/1000 Package (12618A Interface)	MEF		-2	-2.2A	0A	-0.1A	-0.1A	-0.2A

FOOTNOTES:

nnc = no net change; n/a = not applicable

(M) = +5V Memory current requirements for memory controller, memory modules, and fault control check bit boards. In computer without power fail recovery system, this current is drawn from the available +5V current, reducing current available for I/O interfaces. All 217x System Processor Units include a power fail recovery system.

(c) = 12791A uses 1.2A plus 0.525A for each ROM installed (up to 8 possible); -5.4A when fully loaded.

(d) = This 7970B/E data also applies to 7971A Mag Tape Subsystem in upright cabinet with an equivalent option.

HEWLETT PACKARD