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HP 2115/2116 DMA DIAGNOSTIC

HP Product No. 24185

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HP 2115/2116 DMA DIAGNOSTIC

The test program for the Direct Memory Access Option, HP 12578, can be used in two modes. In the Long Test Mode, all functions of the DMA are tested, and any functions specific to the select code under test are tested. The Short Test Mode tests only the functions of the select code being tested. All select codes can be tested by installing the proper register card in the I/O slot for the select code to be tested.

HARDWARE REQUIREMENTS

This diagnostic test program runs on any size HP 2115 or 2116 computer. To test the DMA thoroughly, a Micro-Circuit Register must be used. Although the test program can run with only a teleprinter, certain restrictions are imposed. (See Program Limitiations.) A special edge connector is required for the Micro-Circuit Register.

The Micro-Circuit Register, HP 12566, must have the following jumper configuration:

W1-B W2-C

W3-B W4-B

W5 through W8 - IN

W9-A

The special edge connector must be wired as follows:

A-1	K-9	U-17
B-2	L-10	V-18
C-3	M-11	W-19
D-4	N-12	X-20
E-5	P-13	Y-21
F-6	R-14	AA-22-23
H-7	S-15	BB-24
J-8	T-16	

Connector HP 1251-0332 can be used, with pin 22 shorted to pin 23.

FUNCTIONAL AND OPERATIONAL CHARACTERISTICS

When a teleprinter is used, the SIO teleprinter driver is loaded and configured before the diagnostic program. Then the diagnostic test is configured.

A permanent copy of the configured diagnostic (and the SIO teleprinter driver, if included) eliminates repeating the configuration steps for subsequent uses of the diagnostic. To make a copy, load the SIO SYSTEM DUMP program and run it before running the diagnostic program.

After test options are selected, the program halts to allow the operator to change the select code of the I/O slot under test if Function Test Option bit 6 has been set.

The Long Test, selected by resetting Function Test Option bit 7, should be done for at least one select code to check all DMA functions; using the Micro-Circuit register this diagnostic test requires over three minutes of run time. After operation of the DMA functions is confirmed, the remaining select codes can be checked with the Short Test. In the Short Test mode functions specific to the select code being tested are checked (SRQ lines to each DMA channel and select code lines generated by each DMA channel).

If an error is detected during operation, the program prints a message on the teleprinter, then halts with a value in the MEMORY DATA register. (Exceptions to this are trap cell halts $1060xx_8$ located in low memory 2_8-77_8 and halts for which a printed message is not appropriate or necessary.) The cause of any of these halts should be determined before the diagnostic can be run or restarted.

To repeat any test, set Function Test Option bit 13 after an error halt.

To reconfigure after running the program, start at location 111_8 instead of location 2_8.

SPECIAL SITUATIONS

To use this diagnostic test to check the ability of the DMA to deny priority to DMA1:

1. Remove the Parity Check and Memory Protect options if installed. If neither option is installed, tape off pin 31 on the DMA control card and pin 58 on the DMA address encoder card.
2. Run the Long Test and expect an E15 (102015) diagnostic message. If the message does not occur, then DMA1 cannot be denied interrupt priority.

LIMITATIONS

When the Micro-Circuit Register is not available, the teleprinter interface board can be used; however, 8-bit data transfers are made rather than 16-bit transfers, checking only the eight low-order bits. If the register board is used without the teleprinter, the diagnostic test program tests all sixteen bits; but errors must be interpreted from the MEMORY DATA, A-, and B-Registers according to Table DMA-3.

The Short Test, tests T-17 through T-21, tests only the functions of the select code being tested, so the Long Test should be performed on at least one select code.

This diagnostic program does not check the maximum data rate specification of the DMA.

Since each channel is tested individually, no simultaneous operation testing is done.

PROGRAM ORGANIZATION

This diagnostic program performs the following routines.

CONFIG	Inputs and stores hardware information supplied by the operator through the SWITCH REGISTER during configuration time. Also stores selected Function Test Options in an internal SWITCH REGISTER.
INIT	Sets trap cell halts in locations 2_8-77_8 and prints the start-of-diagnostic message on the teleprinter.
T.1	Tests the DMA flag instructions.
T.2	Tests the ability to enable and disable the interrupt system.
T.3	Tests the DMA interrupt capability by forcing an interrupt, checking the return address for the correct location, and checking the interrupt acknowledge.
T.4	Tests the control reset instructions.

T.5 Tests the PRESET functions unless option bit 9 is set. Before the PRESET test starts, the diagnostic halts with 102027 in the MEMORY DATA Register to allow the user to press PRESET.

T.6 Tests DMA interrupt priority. Checks priority of DMA channel 1 (DMA1) over DMA channel 2 (DMA2) and over the I/O select code under test (which contains MCR or teleprinter interface card). Checks ability of DMA PH5 signal to inhibit I/O interrupts. Checks DMA 2 priority over I/O select code under test. (See Special Situations section concerning the procedure necessary to check the ability to deny priority to DMA1.)

T.7 Tests the ability to set and read the word count registers for all numbers up to the maximum word count (16,383).

T.10 Tests the word count increment function (rollover) by setting the word count registers to minus one and forcing a data transfer which should cause the DMA to interrupt.

T.11 Tests the direct memory address registers by making DMA output transfers from every available location in memory.

T.12 Tests the ability of the DMA to set an interface control flip-flop when bit 15 of the DMA program control word has been set to a one.

T.13 Tests the ability of the DMA to clear an interface control flip-flop when bit 13 of the DMA program control word has been set to a one.

T.14 Tests the ability of DMA generated signal to clear interface flag after transfer.

T.15 Tests the DMA output capability with all possible 16-bit data patterns and their complements if MCR is used, or with all possible 8-bit patterns and their complements if TTY interface is used.

T.16 Tests the DMA input capability with the same data patterns used in T.15

NOTE: The Long Test (option Bit 7 reset) performs all tests, the Short Test (Bit 7 set) performs only tests T-17 through T-21.

T.17 Tests the DMA character unpacking function in the output mode.

T.20 Tests the DMA character packing function in the input mode.

T.21 Tests the DMA for illegal response to incorrect select codes.

END Prints the end-of-diagnostic message on the teleprinter and halts if bit 12 is set, or restarts the diagnostic if bit 12 is reset.

NOTE: This END routine has provisions for return of execution control to a suitable executive program, if present.

OPERATING INSTRUCTIONS

NOTE: This procedure presumes the use of a Micro-Circuit Register. The register card must have jumpers wired as described under HARDWARE CONFIGURATION and must be connected through an edge connector, also described in that section. If the register card is not used, install the teleprinter interface card in the slot to be tested; limitations described will apply.

a. Install the register card in the I/O slot to be tested. If a Long Test is being performed, make sure that all I/O slots of higher priority have either an interface card or a priority jumper installed.

b. If the test program is being run for the first time, use the Basic Binary Loader (BBL) to load the teleprinter driver if a teleprinter is available. Configure the driver. Then use BBL again to load this diagnostic test. If a configured DMA diagnostic tape is available, skip the following configuration procedure (steps c through f); load the configured tape using BBL, and start at step g.

c. Set the SWITCH REGISTER to 2_8; then press LOAD ADDRESS.

d. Set the select code into the SWITCH REGISTER (Table DMA-1) and press RUN. The program should halt with 107076_8 in the MEMORY DATA Register.

e. Refer to Table DMA-2 and set Function Test Options into the SWITCH REGISTER; press RUN. The program should halt with 107077 in the MEMORY DATA Register.

f. To punch a configured diagnostic tape, use SIO SYSTEM DUMP, then continue with the procedure. If a configured tape is not required, skip this step.

g. LOAD ADDRESS 100_8.

h. If Function Test Options other than those in the internal switch register are to be used, set SWITCH REGISTER bit 0, then select the desired Function Test Options by setting the SWITCH REGISTER as listed in Table DMA-2.

i. Press PRESET and RUN. The diagnostic executes according to the Function Test Options selected. If Function Test Option bit 6 is set, the diagnostic halts with 103013 in the MEMORY DATA Register. Enter the select code to be tested into SWITCH REGISTER bits 0-5 and press RUN.

j. If the PRESET test (Test T.5) is to be performed, the program halts with 102027_8 in MEMORY DATA. Press PRESET then RUN.

NOTE: A teleprinter driver (step b) is required for SIO System Dump.

k. Upon completion of all tests, the diagnostic prints a message and/or halts with 102077 in the MEMORY DATA Register. Turn computer POWER off. Move the register card to the next select code to be tested. Turn POWER on. (If the teleprinter card has been moved, reload and reconfigure the SIO driver.) Begin test on new select code at step g. Repeat steps g through k until all select codes have been tested.

ERROR ANALYSIS

All halts display a value in the MEMORY DATA Register. Refer to Table DMA-3 to analyze the halt conditions, then press RUN to continue the diagnostic program.

If a trap cell halt occurs on the teleprinter select code, change the Function Test Option to suppress all teleprinter messages (see Table DMA-2), then restart at location 100_8.

Table DMA-1

Hardware Configuration--Switch Register Settings

Bits	Function
0-5	Set to the Select Code of the Register Card (or teleprinter interface).
6	Set on if teleprinter is not available.

Table DMA-2

Function Test Options--Switch Register Settings

Bits	Function If Set
0	The external switch register overrides the internal switch register, allowing the operator to select options other than those selected at configuration time. (Used in external switch register only; has no effect if set to one in internal switch register.)
1-5	Spare.
6	The program will halt at the beginning to allow operator to enter the new select code.
7	A Short Test is performed. (If not set, a Long Test is performed).
8	A teleprinter interface card is being used to test the select code. (If not set, a register card is assumed.)
9	PRESET test is omitted.
10	Non-error messages are suppressed.
11	All messages are suppressed.
12	The program will halt after a complete cycle of the program.
13	The program loops on the current test instead of advancing to the next test.
14	Error halts are suppressed.
15	Spare.

TABLE DMA-3
Diagnostic Messages

MEMORY DATA	Test	Message*	Comments
(no halt)	INIT.	HØ. START DMA DIAGNOSTIC	Initial Message.
102001	T.1	E1. CLF6 OR SFS6 ERR	DMA1--Test the ability to clear the flag and test the SFS instruction.
102002	T.1	E2. CLF6 OR SFC6 ERR	DMA1--Test the ability to clear the flag and test the SFC instruction.
102003	T.1	E3. STF6 OR SFC6 ERR	DMA1--Test the ability to set the flag and test the SFC instruction.
102004	T.1	E4. STF6 OR SFS6 ERR	SMA1--Test the ability to set the flag and test the SFS instruction.
102005	T.1	E5. CLF7 or SFS7 ERR	DMA2--Test the ability to clear the flag and test the SFS instruction.
102006	T.1	E6. CLF7 OR SFC7 ERR	DMA2--Test the ability to clear the flag and test the SFC instruction.
102007	T.1	E7. STF7 OR SFC7 ERR	DMA2--Test the ability to set the flag and test the SFC instruction.
102010	T.1	E10. STF7 OR SFS7 ERR	DMA2--Test the ability to set the flag and test the SFS instruction.
102011	T.2	(none)	CLF Ø did not disable interrupts or SFS Ø caused a bad skip.
102012	T.2	(none)	CLF Ø did not disable interrupts or SFCØ did not skip.
102013	T.2	E13. STFØ OR SFCØ ERR	STF Ø did not enable interrupts or SFC Ø caused bad skip.

*"H" Message is informational
"E" Message indicates an error.

TABLE DMA-3 (Cont.)

MEMORY DATA	Test	Message	Comments
102014	T.2	E14. STFØ OR SFSØ ERR	STF Ø did not enable interrupts or SFS Ø did not skip.
102015	T.3	E15. NO D1 INT	Test the interrupt capability of DMA1.
102016	T.3	E16. NO D2 INT	Test the interrupt capability of DMA2.
102017	T.3	E17. D1 RTN ADDR ERR	DMA--The return address that resulted from the interrupt is incorrect.
102020	T.3	E20. D2 RTN ADDR ERR	DMA--The return address that resulted from the interrupt is incorrect.
102021	T.3	E21. D1 IAK ERR	DMA1--Interrupt acknowledge failed.
102022	T.3	E22. D2 IAK ERR	DMA2--Interrupt acknowledge failed.
102023	T.4	E23. D1 CLCØ ERR	DMA1--CLC Ø instruction failed to reset the control flip-flop.
102024	T.4	E24. CLC6 ERR	DMA1--Test ability of CLC 6 instruction to clear the control flip-flop.
102025	T.4	E25. D2 CLCØ ERR	DMA2--CLC Ø instruction failed to reset the control flip-flop.
102026	T.4	E26. CLC7 ERR	DMA2--Test ability of CLC 7 instruction to clear the control flip-flop
102027	T.5	(None)	Press PRESET switch, then press RUN to test PRESET functions.
102031	T.5	(None)	PRESET switch failed to set DMA1 flag.

TABLE DMA-3 (Cont.)

MEMORY DATA	Test	Message	Comments
102032	T.5	(None)	PRESET switch failed to set DMA2 flag.
102035	T.6	E35. D1-D2 PRIORITY ERR	DMA1 failed to take priority over DMA 2.
102036	T.6	E36. D2-IO PRIORITY ERR	DMA2 failed to take priority over I/O select code being tested.
102037	T.6	E37. D1-IO PRIORITY ERR	DMA1 failed to take priority over I/O select code being tested.
102040	T.7	E40. WC1 IS *xxxxxx*, SHOULD BE *xxxxxx*	Word count readback from DMA1 is different from output word. A-Register contains output word, B-Register contains input word.
102041	T.7	E41. WC2 IS *xxxxxx*, SHOULD BE *xxxxxx*	Word count readback from DMA2 is different from output word. A-Register contains output word, B-Register contains input word.
102042	T.10	E42. NO D1 INT	With interrupt system enabled, DMA1 failed to interrupt after word transfer.
103043	T.10	E43. NO D2 INT	With interrupt system enabled, DMA failed to interrupt after word transfer.
102044	T.10	E44. WC1 IS *xxxxxx*, SHOULD BE ZERO	DMA1 word count register was not zero when interrupt occurred. B-Register contains word count.
102045	T.10	E45. D1 INT LOC IS *xxxxxx*, SHOULD BE *xxxxxx*	DMA1 interrupted from wrong location after transfer. A-Register contains correct location, B-Register contains incorrect location.

TABLE DMA-3 (Cont.)

MEMORY DATA	Test	Message	Comments
102046	T.10	E46. WC2 IS *xxxxxx*, SHOULD BE ZERO	DMA2 word count register was not zero when interrupt occurred. B-Register contains word count.
102047	T.10	E47. D2 INT LOC IS *xxxxxx*, SHOULD BE *xxxxxx*	DMA2 interrupted from wrong location after transfer. A-Register contains correct location, B-Register contains incorrect location.
102050	T.11, T.15-T.20	E50. D1 FLG CLR	DMA1 flag was not set after output word transfer. A-Register contains program return address.
102051	T.11	E51. D1 OUT=*xxxxxx*, IN=*xxxxxx*, ADDR=*xxxxxx*	DMA1 made a bad output word transfer, or is not transferring data from every memory location. A-Register contains expected output, B-Register contains read-in from MCR. Pressing RUN will display address if a TTY is not used.
102052	T.11	(None)	Non-TTY display of E51 output address. A-Register contains address.
102053	T.11, T.15-T.20	E53. D2 FLG CLR	DMA2 flag was not set after output word transfer. A-Register contains program return address.
102054	T.11	E54. D2 OUT=*xxxxxx*, IN=*xxxxxx*, ADDR=*xxxxxx*	DMA2 made a bad output word transfer, or is not transferring data from every memory location. A-Register contains expected output, B-Register contains read-in from MCR. Pressing RUN will display address if a TTY is not used.
102055	T.11	(None)	Non-TTY display of E54 output address. A-Register contains address.

TABLE DMA-3 (Cont.)

MEMORY DATA	Test	Message	Comments
102056	T.12	E56. D1 CTL WRD ERR	DMA1--Bit 15 of Control Word = 1, but DMA did not set interface control flip-flop after transfer.
102057	T.12	E57. D1 CTL WRD ERR	DMA1--Bit 15 of Control Word = Ø, but DMA set interface control flip-flop after transfer.
102060	T.12	E60. D2 CTL WRD ERR	DMA2--Bit 15 of Control Word = 1, but DMA did not set interface control flip-flop after transfer.
102061	T.12	E61. D2 CTL WRD ERR	DMA2--Bit 15 of Control Word = Ø, but DMA set interface control flip-flop after transfer.
102062	T.13	E62. D1 CTL WRD ERR	DMA1--Bit 13 of Control Word = 1, but DMA did not clear interface control flip-flop after transfer.
102063	T.13	E63. D1 CTL WRD ERR	DMA1--Bit 13 of Control Word = Ø, but DMA cleared interface control flip-flop after transfer.
102064	T.13	E64. D2 CTL WRD ERR	DMA2--Bit 13 of Control Word = 1, but DMA did not clear interface control flip-flop after transfer.
102065	T.13	E65. D2 CTL WRD ERR	DMA2--Bit 13 of Control Word = Ø, but DMA cleared interface control flip-flop after transfer.
102067	T.15	E67. D1 OUT. GOOD=*xxxxxx*, BAD=*xxxxxx*	DMA1 made a bad output transfer in the word mode. A-Register contains expected output, B-Register contains read-in from MCR.

TABLE DMA-3 (Cont.)

MEMORY DATA	Test	Message	Comments
102071	T.15	E71. D2 OUT. GOOD=*xxxxxx*, BAD=*xxxxxx*	DMA2 made a bad output transfer in the word mode. A-Register contains expected output, B-Register contains read-in from MCR.
102073	T.16	E73. D1 IN. GOOD=*xxxxxx*, BAD=*xxxxxx*	DMA1 made a bad input transfer in the word mode. A-Register contains expected input, B-Register contains actual input.
102074	T.14	E74. D1--I/O FLG SET	DMA1--I/O Flag should be cleared by DMA after a transfer.
102075	T.17	E75. D1 OUT. GOOD= *xxxxxx*, BAD= *xxxxxx*	DMA1 made a bad upper byte output transfer. A-Register contains expected output, B-Register contains read-in from MCR.
102076	T.17	E76. D1 OUT. GOOD= *xxxxxx*, BAD= *xxxxxx*	DMA1 made a bad lower byte output transfer. A-Register contains exptected output, B-Register contains read-in from MCR.
102077	END	H77. END DIAGNOSTIC	End of diagnostic. To repeat on same I/O select code, set Function Test Options and press RUN.
103000	T.3	E1ØØ. D1 IAK ERR	IAK should only clear DMA1 flag buffer, not flag.
103001	T.17	E1Ø1. D2 OUT. GOOD= *xxxxxx*, BAD= *xxxxxx*	DMA2 made a bad upper byte output transfer. A-Register contains expected output. B-Register contains read-in from MCR.
103002	T.17	E102. D2 OUT. GOOD= *xxxxxx*, BAD=*xxxxxx*	DMA2 made a bad lower byte output transfer. A-Register contains expected output, B-Register contains read-in from MCR.
103003	T.3	E103. DR IAK ERR	IAK should only clear DMA2 flag buffer, not flag.

TABLE DMA-3 (Cont.)

MEMORY DATA	Test	Message	Comments
103004	T.20	E104. D1 IN. GOOD=*xxxxxx*, BAD=*xxxxxx*	DMA1 made a bad input byte transfer. A-Register contains expected input, B-Register contains actual input.
103005	T.6	E105. PH5 ERR	PH5 signal did not inhibit I/O interrupts.
103006	T.20	E106. D2 IN. GOOD=*xxxxxx*, BAD=*xxxxxx*	DMA2 made a bad input byte transfer. A-Register contains expected input, B-Register contains actual input.
103012	T.14	E112. D2--I/O FLG SET	DMA2--I/O Flag should be cleared by DMA after a transfer.
103013	INIT.	(None)	Enter new select code to be tested into Switch Register bits Ø-5 and press RUN.
103014	INIT.	(None)	Enter options into switch Register (Table 2) and press RUN.
103015	T.16	E115. D2 IN. GOOD=*xxxxxx*, BAD=*xxxxxx*	DMA2 made a bad input transfer in the word mode. A-Register contains expected input, B-Register contains actual input.
103016	T.2	E116. D1 CLFØ ERR	DMA1 interrupted with interrupt system disabled.
103017	T.2	E117. D2 CLFØ ERR	DMA2 interrupted with interrupt system disable.
103020	T.7	(None)	A-Register contains data resulting from LIA Ø. Should be zero.
103021	T.21	E121. D1 SC ERR	STF 1 set the DMA1 flag flip-flop.
103022	T.21	E122. D1 SC ERR	STF 16 set the DMA1 flag flip-flop.

TABLE DMA-3 (Cont.)

MEMORY DATA	Test	Message	Comments
103023	T.21	E123. D2 SC ERR	STF 1 set the DMA2 flag flip-flop.
103024	T.21	E124. D2 SC ERR	STF 17 set the DMA2 flag flip-flop.
103025	T.21	E125. D1 SC ERR	OTA 1 set the DMA1 word count register.
103026	T.21	E126. D1 SC ERR	OTA 12 set the DMA1 word count register.
103027	T.21	E127. D2 SC ERR	OTA 1 set the DMA2 word count register.
103030	T.21	E130. D2 SC ERR	OTA 13 set the DMA2 word count register.
103031	T.7	E131. D1 CRS ERR	CRS did not clear DMA1 register card control flip-flop.
103032	T.7	E132. D2 CRS ERR	CRS did not clear DMA2 register card control flip-flop.
103033	T.14	E133. STF6 ERR	STR6 failed to turn off DMA1.
103034	T.14	E134. STF7 ERR	STF7 failed to turn off DMA2.
103035	T.6	E135. NO I/O INT	No interrupt on I/O select code. Check PRL7 signal.
1060*xx*	All	(None)	Trap cell interrupt. MEMORY ADDRESS register = memory address when interrupted, *xx* = trap cell location.
107074	CONFIG	(None)	Set LOADER switch to PROTECTED and press RUN.
107075	CONFIG & INIT	(None)	The select code (SWITCH REGISTER bits Ø-5) is invalid. (Valid codes are 10_8-77_8.) Reset the SWITCH REGISTER and press RUN.

TABLE DMA-3 (Cont.)

MEMORY DATA	Test	Message	Comments
107076	CONFIG	(None)	Set internal switch register for desired Function Test Options (see Table DMA-2) and press RUN.
107077	CONFIG	(None)	Configuration complete. Use SIO SYSTEM DUMP or LOAD ADDRESS $10\emptyset_8$, set desired options, then press PRESET and RUN.