HP 12794A
HDLC Modem Interface
installation and service manual

Card Assembly: 5061-3418
Date Code: 2022

HEWLETT PACKARD

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Update 1 January 1982
MANUAL PART NO. 12794-90001
Printed in U.S.A. September 1980

PRINTING HISTORY

The Printing History below identifies the Edition of this Manual and any Updates that are included. Periodically, update packages are distributed which contain replacement pages to be merged into the manual, including an updated copy of this printing history page. Also, the update may contain write-in instructions.

Each reprinting of this manual will incorporate all past updates; however, no new information will be added. Thus, the reprinted copy will be identical in content to prior printings of the same edition with its user-inserted update information. New editions of this manual will contain new information, as well as all updates.

To determine what manual edition and update is compatible with your current software revision code, refer to the appropriate Software Numbering Catalog, Software Product Catalog, or Diagnostic Configurator Manual.

First Edition .....September 1980
Update 1 .....January 1982

SAFETY CONSIDERATIONS

GENERAL - This product and relation documentation must be reviewed for familiarization with safety markings and instructions before operation.

SAFETY SYMBOLS

Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect the product against damage.

Indicates hazardous voltages.

Indicates earth (ground) terminal (sometimes used in manual to indicate circuit common connected to grounded chassis).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

CAUTION

STATIC SENSITIVE DEVICES

Some of the semiconductor devices used in this equipment are susceptible to damage by static discharge. Depending on the magnitude of the charge, device substrates can be punctured or destroyed by contact or mere proximity to a static charge. These charges are generated in numerous ways such as simple contact, separation of materials, and normal motions of persons working with static sensitive devices.

When handling or servicing equipment containing static sensitive devices, adequate precautions must be taken to prevent device damage or destruction. Only those who are thoroughly familiar with industry accepted techniques for handling static sensitive devices should attempt to service the cards with these devices. In all instances, measures must be taken to prevent static charge buildup on work surfaces and persons handling the devices. Cautions are included through this manual where handling and maintenance involve static sensitive devices.

SAFETY EARTH GROUND - This is a safety class I product and is provided with a protective earthing terminal. An uninterruptible safety earth ground must be provided from the main power source to the product input wiring terminals, power cord, or supplied power cord set. Whenever it is likely that the protection has been impaired, the product must be made inoperative and be secured against any unintended operation.

BEFORE APPLYING POWER - Verify that the product is configured to match the available main power source per the input power configuration instructions provided in this manual.

If this product is to be energized via an auto-transformer (for voltage reduction) make sure the common terminal is connected to the earth terminal of the main power source.

SERVICING

WARNING

Any servicing, adjustment, maintenance, or repair of this product must be performed only by qualified personnel.

Adjustments described in this manual may be performed with power supplied to the product while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.

Capacitors inside this product may still be charged even when disconnected from its power source.

To avoid a fire hazard, only fuses with the required current rating and of the specified type (normal blow, time delay, etc.) are to be used for replacement.

WARNING

EYE HAZARD

Eye protection must be worn when removing or inserting integrated circuits held in place with retaining clips.

Definition of Terms

The following terms are defined as they are used in this manual.

asynchronous transmission - No timing signals are sent with the data. Start and stop bits serve to define transmitted words.

buffer - A segment of contiguous Random-Access memory locations used for temporary storage of input/output messages.

card - The interface PCA (Printed Circuit Assembly).

CRC-16 (Cyclic Redundancy Check) - An error detection scheme used in data communications.

DIP (Dual In-line Package) - A type of integrated circuit package.

driver - In a hardware sense, a driver refers to a circuit which is capable of supplying specific current and voltage requirements. In a software sense, a driver is a program that is capable of controlling a specific input/output device.

DS (Distributed System) - A term used to refer to networks using Hewlett-Packard Distributed Systems hardware and software products.

firmware - Software code packaged in read-only memory (ROM).

frame - A transmitted message that is formatted according to HDLC protocol.

full-duplex - Communications system or equipment capable of simultaneous two way data communication.

half-duplex - Communications system or equipment capable of transmission in either direction, but not both directions simultaneously.

handshaking - The alternating exchange of predetermined signals between two communicating devices for purposes of control.

host - The computer housing the communication card.

interface - A device providing electrical and mechanical compatibility between two communicating devices. The HP 12794A also provides other control features for the associated communication link.

LED (Light Emitting Diode) - A component used on many printed circuit assemblies to provide a visible indication of desired information.

link - Communication lines, modems, and other equipment which permit the transmission of information in data format between two or more devices.

modem (modulator-demodulator) - Equipment capable of digital-to-analog and analog-to-digital signal conversion for transmission and reception via common carrier telephone lines.

PCA (Printed Circuit Assembly) - Interface cards are commonly referred to as PCAs.

primary - The portion of the interface responsible for transmission processes.

Primary System - A preconfigured operating system included with all HP 1000 Computer systems. It can be reconfigured to meet specific system I/O and memory requirements.

receiver - Any device capable of reception of electrically transmitted signals.

secondary - The portion of the interface responsible for reception processes.

synchronous transmission - Timing signals are transmitted with the data. No start and stop bits are used. Defined protocol characters must be used to define message blocks or frames.

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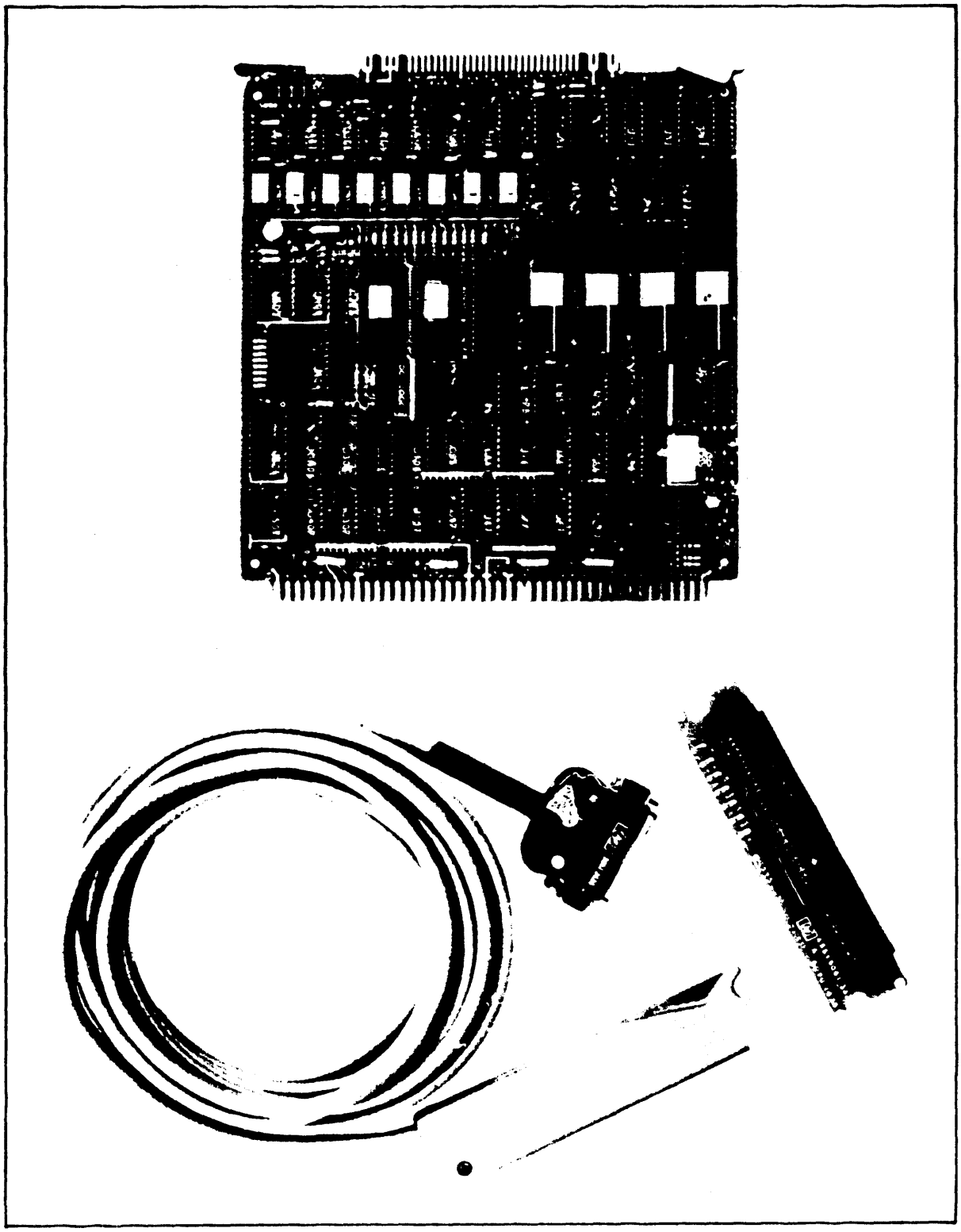


Fig. 1-1. 12794A HDLC Modem Interface Kit Contents

Section 1
General Information

Introduction

This manual provides general information, installation procedures, HDLC protocol information, principle of operation, maintenance instructions, replaceable parts information, and servicing diagrams for the HP 12794A HDLC Modem Interface Kit. This section contains general information concerning the HP 12794A including a description and specifications.

Description

The HP 12794A (see Figure 1-1) provides an HP 1000 M/E/F-Series Computer with the capability to support a synchronous modem communications link to another HP 1000 M/E/F-Series computer, or to an HP 1000 L-Series computer. It is used in conjunction with DVR66 of the HP 91750A DS/1000-IV Software.

The HP 12794A card plugs into a single I/O slot of an HP 1000 M/E/F-Series Computer and is assigned a single select code. The card contains a Z-80A CPU chip with associated Z-80A support chips and two ROMs containing firmware to implement HDLC protocol. Due to this on-board intelligence, the card is able to relieve a large amount of CPU overhead. Functions such as HDLC protocol generation, CRC-16 block check error control, modem control, and a hardware self-test are all handled on the interface card. The Z-80A and on-board RAM also enable the card to maintain long term communications line statistics, and input and output data buffering.

Equipment Supplied

The standard HP 12794A HDLC Modem Interface Kit consists of the following items (see Figure 1-1):

1. Programmable serial interface card, HP part number 5061-3418.

2. HDLC firmware ROMs, HP part numbers 91750-80008 and 91750-80009.

3. EIA RS-232-C modem cable (5 meter, 16.4 feet), HP part number 5061-3424.

4. Loop-back verifier hood, HP part number 5061-3425.

5. Installation and Service Manual, HP part number 12794-90001.

The following options are available with the HP 12794A:

1. Option 001: Upgrade discount for latest revision of interface firmware (for previously purchased firmware only).

2. Option 002: Replace the EIA RS-232-C cable and loop-back hood with one EIA RS-449 modem cable (5 meter, 16.4 feet), HP part number 5061-3436, and RS-449 loop-back hood, HP part number 5061-3441.

Identification

The Product

Five digits and a letter (12794A in this case) are used to identify Hewlett-Packard products used with HP computers. The five digits identify the product and the letter indicates the revision level of the product.

The Circuit Card

The circuit card supplied with the kit is identified by a part number marked on the card. In addition to the part number, the card is further identified by a letter and a date code consisting of four digits (e.g., A-2022). This designation is placed below the part number. The letter identifies the version of the etched circuit on the card. The date code (the four digits following the letter) identifies the electrical characteristics of the card with components mounted. Thus, the complete part number on the interface card could be:

5061-3418
A-2022

If the date code stamped on the HDLC interface card does not agree with the date code on the title page of this manual, there are differences between your card and the card described herein. These differences are described in manual supplements available at the nearest Hewlett-Packard Sales and Service Office (offices are listed at the back of this manual).

Installation and Service Manual

The manual supplied with the kit is identified by its name and part number. Part number, 12794-90001, and publication date are printed on the title page. If the manual is revised, the publication date is changed and the List of Effective Pages (page iii) reflects the pages involved in the change. The Print History page (page ii) records the reprint dates.

Specifications

Table 1-1 lists the specifications of the HP 12794A HDLC Modem Interface Kit.

Table 1-1. Specifications

TRANSMISSION MODE:	Bit serial; synchronous.
TRANSMISSION LINK:	Full-duplex only.
INTERFACE:	Conforms to EIA Standard RS-232-C and RS-449.
DATA TRANSFER LENGTH:	Selectable frame size (128 or 1024 byte information field length).
DATA TRANSFER RATE:	Approximately 300, 1200, 2400, 4800, 9600, 19200, 57600, or 230000 bps.
MODEM TYPES:	Full-duplex, synchronous modems only.
MODEM COMPATIBILITY:	Refer to the data sheet for the HP 12794A.
ERROR DETECTION:	CRC-16 check controlled on the interface.
ERROR CORRECTION:	Retransmission under firmware control.
POWER:	Supplied by host computer as follows: 1.923A at +5V, 0.315A at +12V, 0.175A at -12V. The total power dissipated is 15.495 Watts.

Section 2
Installation

Introduction

This section provides information on unpacking, inspecting, installing, and checking the operation of the HP 12794A HDLC Modem Interface Kit.

Unpacking and Inspection

Inspect the shipping package immediately upon receipt to detect any evidence of mishandling during transit. If the package is damaged, ask that the carrier's agent be present when the kit is unpacked. Carefully unpack the card and accessories and inspect for damage (scratches, broken components, etc.). If damage is noticed, notify the carrier and the nearest Hewlett-Packard Sales and Service Office listed at the back of this manual. Return the carton and packing material for the carrier's inspection.

After inspecting all components, refer to the equipment supplied paragraph in Section 1 of this manual to ensure that the kit is complete. Also check the part numbers listed in that section against the part numbers on the kit components. If the kit is incomplete, or if an incorrect component has been furnished, notify the nearest Hewlett-Packard Sales and Service Office.

After unpacking, inspecting, and checking part numbers of all parts of the kit, follow installation and check-out procedures as defined in this section.

Computation of Current Requirements

The circuit card in the HP 12794A obtains its operating voltages from the computer power supply through the backplane. Before installing the card, it is necessary to determine whether the added current will overload the power supply. The current requirements of the HP 12794A are listed in the power entry of Table 1-1. Current specifications for all other interfaces can be found in the appropriate Reference or Installation and Service Manuals.

Firmware Installation

CAUTION

STATIC SENSITIVE DEVICES

THE ROMS, RAMS, AND Z-80A COMPONENTS USED IN THIS PRODUCT ARE SUSCEPTIBLE TO DAMAGE BY STATIC DISCHARGE. REFER TO THE SAFETY CONSIDERATIONS INFORMATION AT THE FRONT OF THIS MANUAL BEFORE REPLACING.

The firmware ROMs (HP part numbers 91750-80008 and 91750-80009) are factory installed in sockets on the card. Make sure that the ROMs are installed as shown in Figure 2-1, and that the part numbers on them match those given in this paragraph.

ROM Configuration Jumpers

A set of jumpers on the interface card provides the option of using different ROM parts in the future. The set consists of a 14 pin socket housing seven removable jumpers (XW1A through XW1G), and two hardwired jumpers on the interface card itself. Check to see that XW1A through XW1G are configured as described in Tables 2-1 and 2-2 for the specific ROMs that are installed. The hardwired jumpers, W5 and W6, are configured at the factory. W5 should be open (not installed) and W6 should be closed (installed). Refer to Figure 2-2 for the location of the socketed jumpers on the interface card, and the parts location diagram given in Section 7 for the location of the hardwired jumpers.

Table 2-1. ROM Categories According to Part Type

CATEGORY	HP PART #	PART TYPE
A	1818-0762	TI 2532
B	1818-0498	TI 2516 Intel 2716
C	1818-0850	Intel 2732 Intel 2332 Intel 2364

Table 2-2. Jumper Requirements for all ROM Combinations
(X denotes a required jumper)

ROM CATEGORY		XW1A	XW1B	XW1C	XW1D	XW1E	XW1F	XW1G
U93	U203							
C	C					X		
A	A				X	X	X	X
C	A			X		X	X	
B	A			X		X	X	X
B	B			X	X	X	X	X
A	C	X				X		X
C	B	X			X	X	X	
A	B	X		X	X	X	X	X
B	C	X		X		X		X

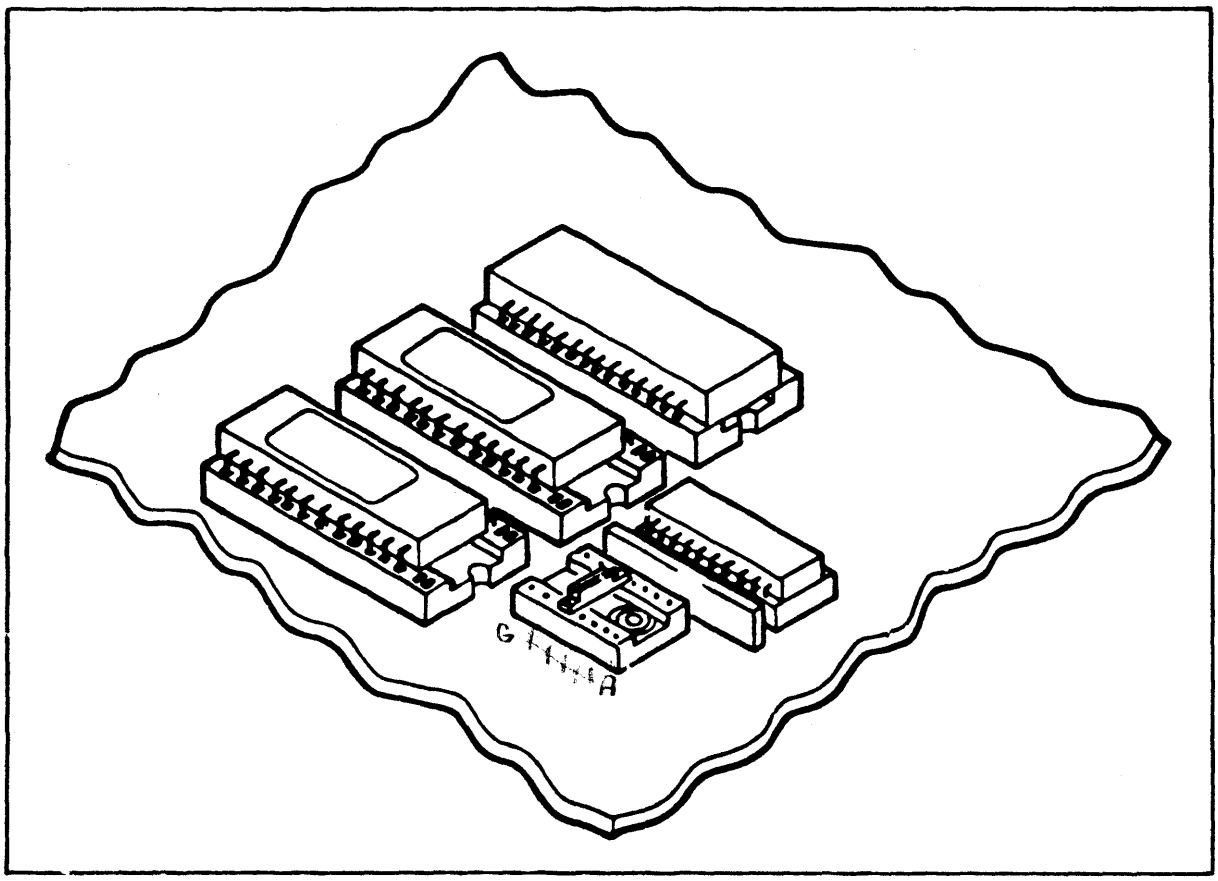


Fig. 2-1. ROM Installation

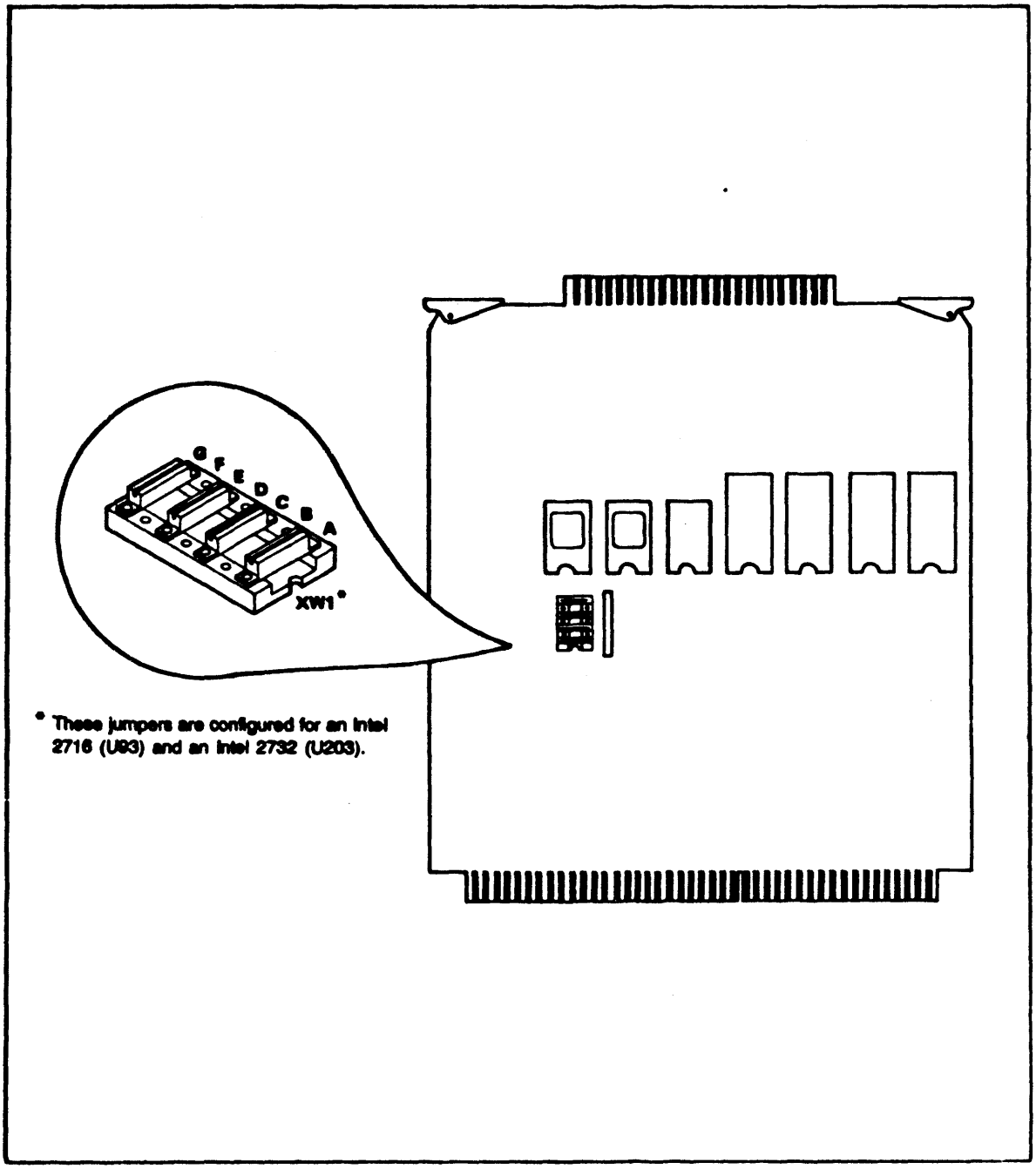


Fig. 2-2. ROM Configuration Jumper Positions

DIP Switch Configuration

The HP 12794A provides a Dual In-line Package (DIP) containing eight switches which may be sensed by the firmware. This set of switches is used to determine the information field size, and the transmitting clock rate and associated time-out values (time-outs are firmware controlled and not user programmable). The transmission clock rate should be set to indicate the clock rate that is supplied by the modem being used. In addition, switch number 1 physically enables the ability to control a forced cold load from a remote node. Configure the switch as necessary using the switch assignments given in Tables 2-3 and 2-4. Refer to Figure 2-3 for switch position on the card.

Table 2-3. Switch Assignments

SWITCH	FUNCTION
1	Closed to enable forced cold load (FCL)/slave request. Open to disable.
2	Closed to select 1024 byte information field. Open to select *128 byte information field. BOTH ENDS OF THE LINK MUST HAVE THIS SWITCH SET THE SAME TO AVOID DATA OVERRUN.
3,4,5	Not used.
6,7,8	Transmission clock rate. See Table 2-4.

* 128 byte information field is the recommended configuration for minimizing frame retransmissions.

Table 2-4. Transmission Clock Rate

SWITCH SETTINGS 6,7,8	CLOCK RATE (bps)	
000	300	NOTE:
00X	1200	X = closed = logic "1"
0X0	2400	0 = open = logic "0"
0XX	4800	
X00	9600	
X0X	19200	
XX0	57600	
XXX	230000	

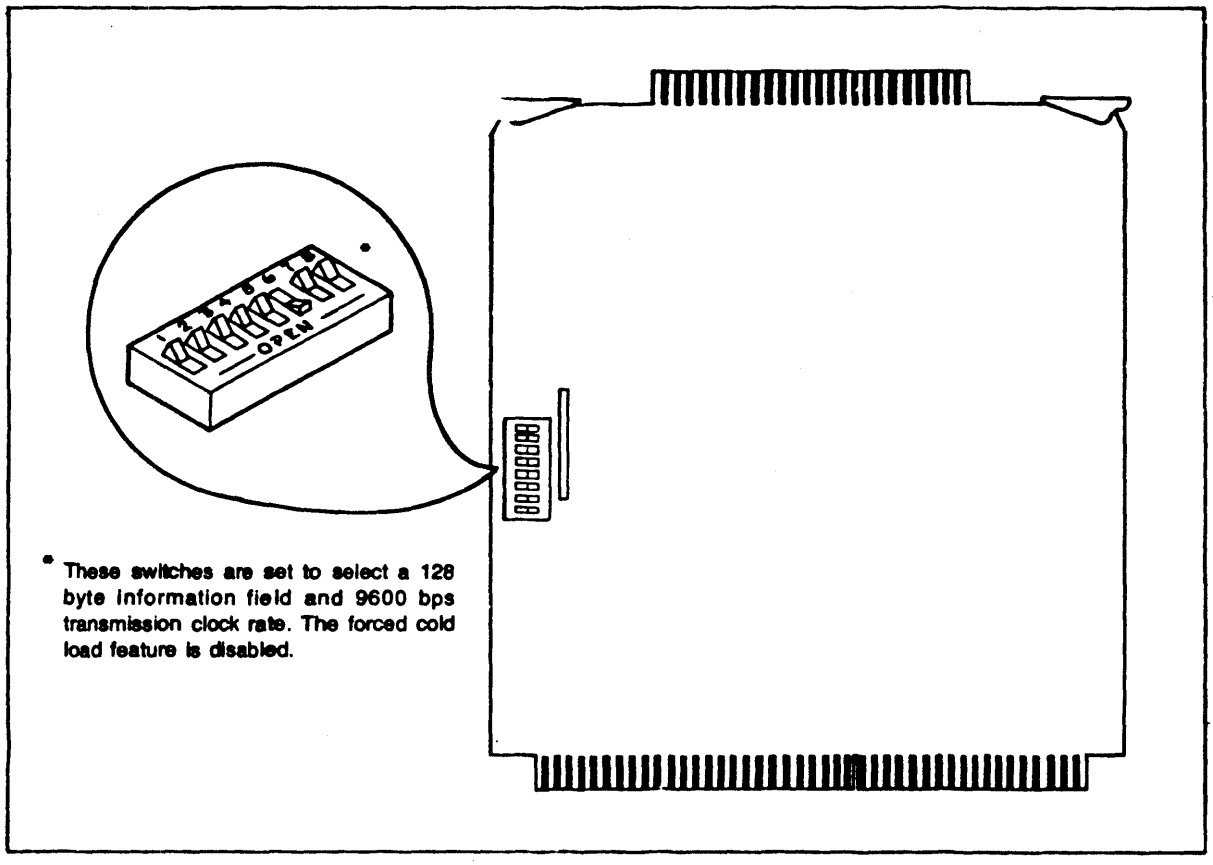


Figure 2-3. DIP Switch Position

Card and Cable Installation

CAUTION

ALWAYS TURN POWER OFF TO THE COMPUTER AND OTHER ASSOCIATED EQUIPMENT WHEN INSERTING OR REMOVING INTERFACE CARDS OR CABLES. FAILURE TO DO SO COULD RESULT IN DAMAGE TO THE EQUIPMENT.

After ensuring that the computer power supply can handle the added load, the ROMs are properly installed, and the DIP switches are configured properly, perform the following steps:

1. Turn off power at the computer and the modem. Install the interface card in the desired slot in the computer card cage, noting the select code. The card should be oriented the same as all other cards in the computer: components on the top side of the card. Press the card firmly into place.

2. Connect the cable supplied with the kit to the interface card and modem.

3. Restore power to the computer and the modem.

4. Initialize the new link into the network as specified in the HP 91750A DS/1000-IV Network Manager's Manual, HP part number 91750-90003.

5. Perform the check-out procedure on the card as specified in the next paragraph.

Checkout Procedure

For check-out after installation, perform the interface card and communication link checks described below.

Interface Card Configuration Check

Since the interface card self-test is run each time that power is applied to the card or the card is reset, the first part of check-out is automatically performed. The following procedure will verify that the card passed the self-test and that the backplane interface circuitry is operational. It also provides a way to check the card configuration switch settings. To perform the check, enter the following commands:

1. RU,DSINF<cr>

   DSINF is a DS/1000-IV utility program that can be used to obtain information such as network configuration, communications parameters, etc. For more information on DSINF, refer to the DS/1000-IV Network Manager's Manual, HP part number 91750-90003.

2. LU,##,AL<cr>

   LU will return information on the configuration of a specified DS/1000 interface card, where ## is the LU (Logical Unit number) of that card. Information will only be returned if the card passed the self-test.

In this way, DSINF will return card configuration information as well as other useful parameters. Check to see that the returned information complies with desired card configuration. If the returned values are unexpected, check the switch settings on the interface card. If in error, reconfigure the switch and reinstall the card, going through all check-out procedures again.

Communication Link Check

Before following the procedure described in this paragraph, it is important to understand the message re-routing capabilities of the network. If there is an alternate path to the remote node being tested, message re-routing must be disabled to ensure that the desired link is being exercised. Check with the network manager about network topology and message re-routing before proceeding.

A good check of the communication link is accomplished by exercising a few REMAT commands. To do this, type in the following commands after the system prompt (:):

1. :RU,REMAT<cr>

   REMAT is the program that handles operator commands for communications from one HP 1000 to another in a Distributed Systems network. It schedules the appropriate monitors to handle all outgoing and incoming requests. REMAT will prompt with a dollar sign ($) when commands are referred to the local node only. When a remote node is referenced (another HP 1000), the prompt will become a number sign (#).

2. $SW,NODE1,NODE2,SC<cr>

   The SW (Switch) instruction defines the action and destination nodes. Set NODE1 to the node number of the neighbor node that is to be exercised. Set NODE2 to the local node's number. SC is the security code for the network. It is defined when the network is initialized.

3. #TI<cr> OR #TM<cr>

   The TI and TM (Time) commands will obtain the time from the remote node and display it on the local terminal being used for this exercise. The TI command should be used if the remote node is an HP 1000 M/E/F-Series computer. The TM command should be used if the remote node is an HP 1000 L-Series computer. If the remote node does not have the necessary monitor to handle the TI or TM command, or does not have a real-time clock, try a DL (Directory List) command or a CL (Cartridge List) command.

4. #EX<cr>

   The EX (EXit) command will end REMAT.

If the above procedure is carried out successfully, the described results will be displayed with no error messages returned. If an error message is returned, refer to error code information supplied in the DS/1000-IV User's Manual, HP part number 91750-90002. For troubleshooting procedures, refer to Section 5 of this manual or the troubleshooting section of the DS/1000-IV Network Manager's Manual, HP part number 91750-90003.

Interface Card LEDs

There are four LEDs installed on the interface card. Located on the left side of the card next to the front edge connector, the LEDs are visible when the card is installed in the computer and are referenced as 0 through 3 with 0 being the LED on the right. During normal operation, LED0 being lit indicates that the interface is logically connected to the other interface on the link. LED1 being lit indicates that a transfer of data is taking place over the backplane. The LEDs are also used to indicate successful completion of the self-test with all four being off after the test and before DS software has been initialized.

Section 3
Protocol

Introduction

There are several levels of protocol involved in an HP DS/1000-IV communications link. Two of these levels are handled on the HP 12794A: line protocol and communications protocol. The first level involves timing and control signals, and electrical specifications for computer-to-modem connections. The second level involves the more complex set of rules used to control the flow of data over the communication link. Both line and communications protocols are firmware controlled on the HP 12794A. This section will present an abbreviated discussion of the communications protocol. For information on the line protocol, refer to the Communication Line Interface paragraphs in Section 4 of this manual. For a more thorough understanding of HDLC, refer to the HP Computer Systems Group Data Communications Standard, October 1977.

Communications Protocol

The HP 12794A is programmed via the read-only memory (ROM) on the ca d to implement High Level Data Link Control (HDLC) protocol. HDLC is a bit oriented protocol designed for use over full-duplex communications channels. The following paragraphs discuss the main characteristics of HDLC.

HDLC Frames

Data transfers using HDLC protocol are bit oriented as opposed to character oriented. Blocks of data are transmitted in frames, a frame being a bit stream starting and ending with a flag character. For this implementation, the flag character is the following bit pattern:

01111110

A frame may or may not contain data but always contains control information. There can be any number of frames in a single transmission.

A frame consists of several fields as illustrated in Figure 3-1 and described in the following paragraphs.

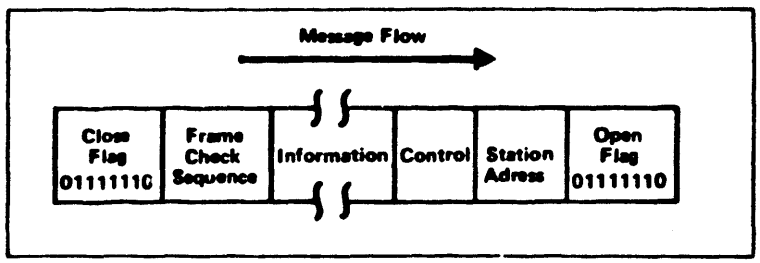


Figure 3-1. HDLC Frame Format

Flag Field

HDLC uses positional significance, not control characters, to identify the various elements of a message. The flag field is the first eight bits of a frame and the receiver uses it to count down the incoming bit stream to identify the other fields within the frame. The close flag is used to indicate the end of the frame. The firmware also uses the close flag to count back to the frame check sequence field.

Zeroes are inserted and deleted as required to prevent a flag bit pattern from appearing within the frame. When five 1's appear, a 0 is inserted in the bit stream after the last 1. The receiver detects the five 1's followed by a 0 and deletes the 0. The inserted and deleted zeroes are not included in the frame check sequence. This zero insertion/deletion scheme is controlled by the Z-80A SIO chip on the HP 12794A card.

Each interface on the link is continuously seaching for the flag pattern. During lulls in message flow, a series of flags is transmitted to keep the link active and synchronized.

Station Address Field

Since all links in a DS network are point-to-point, station address information is not needed as such. Instead, this field is used to convey whether the frame contains a response or a command. This information is necessary due to the data handling organization at each station on the link. Outgoing commands and incoming responses are handled by the primary portion of the firmware driver. Incoming commands and outgoing responses are handled by the secondary portion of the driver. This primary/secondary scheme is one way of implementing a full-duplex communications protocol.

Control Field

The control field consists of eight bits containing a command or response pattern required for control of the data link. The primary station uses the field to command the secondary to perform an operation. The secondary uses it to respond to the primary. The control field has three formats, indicating the contents and purpose of the frame as follows (refer to Table 3-1 also):

1. Information Transfer. This control field format indicates that the present frame contains information being transfered from the local primary to the remote secondary.

2. Supervisory Response. A frame with a supervisory format in the control field contains no information (the information field is interpretted to be of zero length and is used to regulate traffic and request retransmissic of missed or erroneous frames.

3. Unnumbered Command/Response. This format consists of commands and responses used to establish or disconnect the communications channel, or reject commands (those not recoverable by retransmission).

Information Field

A non-zero length information field only exists in frames designated as information transfer frames by the control field. When used, the information field is the vehicle for moving data between stations and it is unrestricted in format and contents. Information field length is selected to be 128 or 1024 bytes (corresponding to external and internal clock selection) using one of the configuration switches on the card.

Frame Check Sequence Field

This field is 16 bits in length and preceeds the closing flag. When information is present in the frame, it follows the information field, otherwise it follows the control field. Its purpose is to detect errors that occur during transmission. For the HP 12794A, the frame check sequence is computed under firmware control using the CRC-16, cyclic redundancy check, block check method. This consists of dividing a constant into the first group of bits being transmitted after the opening flag. The quotient is discarded and the remainder added to the next group of bits, which is again divided by the same constant. This continues until the closing flag is detected and the 16-bit CRC-16 remainder is sent in the frame check sequence field before the closing flag..

Table 3-1. HDLC Protocol Bytes (Control Field)

TYPE	MNEMONIC	DESCRIPTION	ENCODING 7	6	5	4	3	2	1	0
INFO.	I	Information	Nr			P	Ns			0
SUPRV.	RR	Receiver Ready	Nr			P	0	0	0	1
	RNR	Receiver Not Ready	Nr			P	0	1	0	1
	REJ	Reject	Nr			P	1	0	0	1
UNNUM.	SARM	Set Asynchronous	0	0	0	0	1	1	1	1
	DISC	Disconnect	0	1	0	0	0	0	1	1
	UA	Unnumbered Acknowl.	0	1	1	0	0	0	1	1
	CMDR	Command Reject	1	0	0	0	0	1	1	1
	SIM	Set Initial. Mode	0	0	0	0	0	1	1	1

Abbreviations:
P - Poll bit
F - Final bit
Nr - Send Sequence Number
Ns - Receive Sequence Number

Error Control

As described in a previous paragraph, CRC-16 is used by the HP 12794A to detect errors in transmitted frames. There are other types of error control methods used on the link as described in the following paragraphs.

Frame Sequencing Checks

Sequencing counts are kept on each interface card and transmitted as necessary to acknowledge frames received correctly. The values of these counts are sent in the control field as the following variables:

Ns - Send Sequence Number.
Ns is only transmitted in information frame control words and is used to tell the receiver the number of the frame being sent.

Nr - Receive Sequence Number.
Nr is transmitted in the control field for supervisory and information frames only and is used to acknowledge correct frame reception. The value of Nr sent is equal to the number of the next frame that is expected.

The counts kept for Nr and Ns are only incremented when frames containing information are sent or received. Supervisory and unnumbered command/response frames do not affect these counts. These frames are acknowledged by proper response words. By keeping track of frames sent and received in this manner, it is possible for transmitting stations to transmit frames before the response is returned for previously transmitted frames. Also, one response can serve to acknowledge more than one received frame. This scheme increases overall link throughput. The number of unacknowledged frames allowed in this implementation of HDLC is seven. After that, outgoing messages are put in a queue and sent only when the proper response is received.

If a sequence error is detected by a transmitting station, it will retransmit the frame after the last acknowledged frame and set the P (Poll) bit to signal that it is a retransmission. The P bit set also demands that the receiving station respond with a supervisory frame instead of the standard information frame acknowledgement. In the response supervisory frame, the F (Final) bit is set to indicate that it is responding to a received poll.

Severe Error Processing

The HP 12794A card is capable of detecting other types of errors besides invalid frames (CRC-16 detected errors) and sequence errors. The other detectable errors are referred to as severe errors and include such cases as:

* Unknown frame type
* Information field larger than available frame buffer
* Ns greater than seven
* Failure to acknowledge after maximum allowable retries

These errors are reported to the software driver by the firmware on the card, and then an attempt is made to recover. For failure to acknowledge, the link is reset. This is similar to the original connect sequence (see Section 4, Principles of Operation, of this manual). For the other severe errors, a command reject frame is sent.

Section 4
Principles of Operation

Introduction

This section contains a description of the operation of the interface card included in the HP 12794A HDLC Modem Interface Kit. The hardware is described in terms of five major funcitonal areas. A brief explanation of the command and status words used in communication between the card and the host computer is also given. The last part of this section is devoted to a functional-level description of the operation of the card.

Hardware Functional Description

The card, HP part number 5061-3418, includes the following major functional areas:

* HP 1000 M/E/F-Series Computer I/O backplane interface
* Z-80A Microprocessor family subsystem (CPU, SIO, DMA and CTC)
* Read-Only Memory (ROM)
* Random-Access Memory (RAM)
* Communication line interface

A block diagram illustrating the major functional areas of the card is presented in Figure 4-1.

Host Computer I/O Backplane Interface

The card communicates with the HP 1000 host computer over the I/O backplane. The backplane interface circuitry can be logically divided into two major sections: the I/O data latches and the control circuitry section.

The I/O data latches consist of two 8-bit input latches and two 8-bit output latches. The input latches hold 16-bit data or command words from the host computer until the card is ready to accept them. Likewise, the output latches hold 16-bit data or status words output from the card to the host computer.

The control circuitry is made up of five flip-flops and other gate-level logic elements. The primary function of this section is to handle the control signals to and from I/O backplane. These signals are used to generate and acknowledge interrupts, to handshake data between the host and the card and to conform to the standard HP 1000 computer I/O backplane signal conventions. For a more detailed discussion of these signals, refer to the HP 1000 I/O Interfacing Guide, HP part number 02109-90006.

The Z-80A Microprocessor Subsystem

The heart of the card is the Z-80A CPU (Central Processing Unit). This MOS LSI microprocessor operates from a single 5 volt supply, uses a single phase clock and has a typical instruction execution time of 1.0 microsecond. The data bus is eight bits wide and the address bus is 16 bits wide. All CPU pins are TTL compatible.

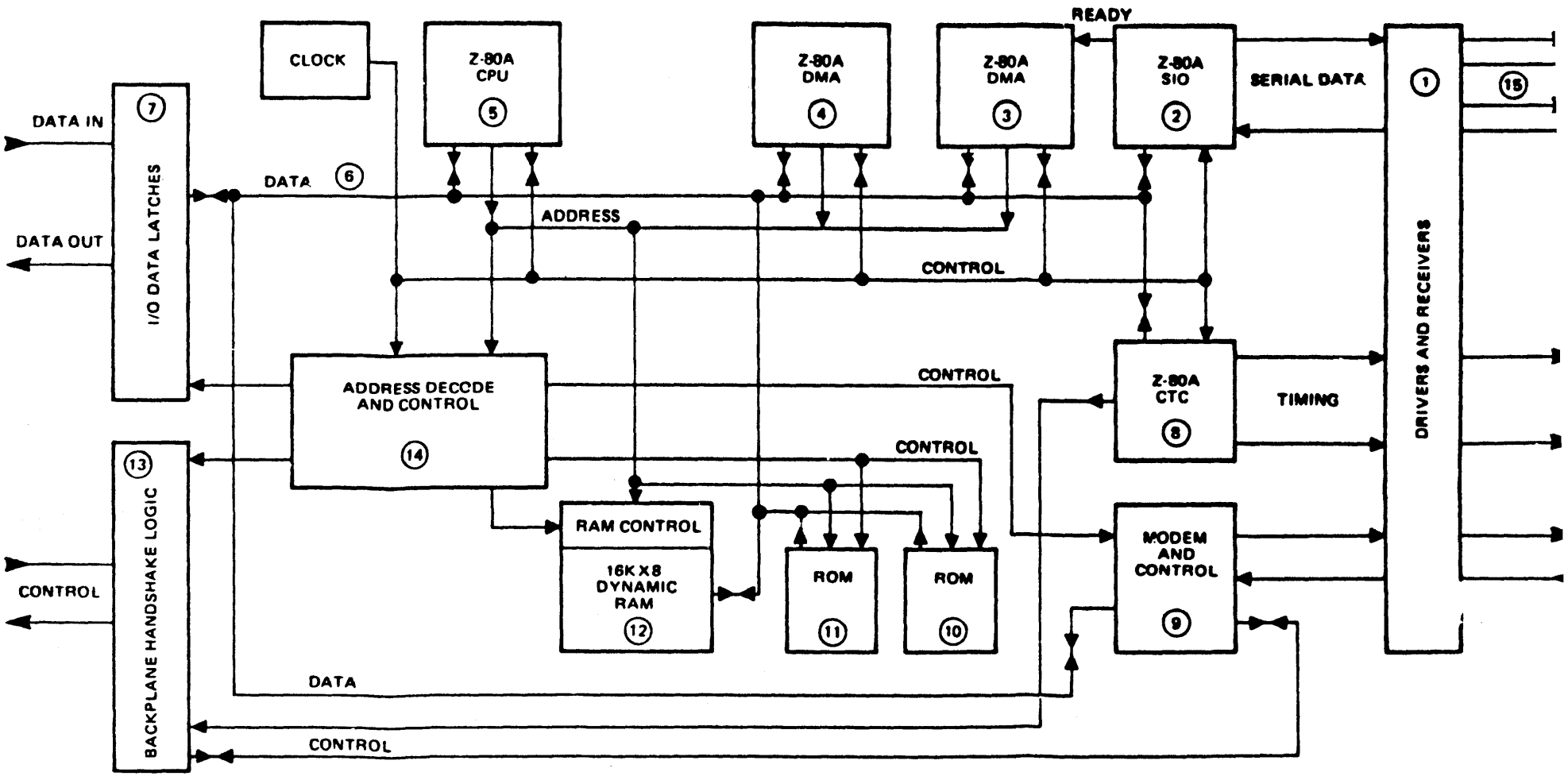
The Z-80A CPU employs a register-based architecture which includes two sets of six general-purpose registers which can be used as 8-bit registers or 16-bit register pairs. Additional 8-bit registers include two sets of accumulator and flag registers, and the interrupt vector and memory refresh registers. Additional 16-bit registers include the stack pointer, program counter and two index registers. The Z-80A CPU provides the intelligence for the card to function as a preprocessor to relieve the host computer of a majority of the protocol processing.

An important pin on the Z-80A as far as this card is concerned is the NMI (Non-Maskable Interrupt) input pin. By pulling this input low with an STC instruction, the host computer can "get the attention of" the Z-80A. An NMI is the highest priority interrupt to the Z-80A and forces it to start fetching and executing instructions from a predetermined location in the firmware. The host software driver uses this feature to inform the card that it requires service.

Various support chips are used in conjunction with the Z-80A CPU to facilitate the card's operation as an intelligent serial interface. These chips are discussed in the paragraphs that follow.

Serial Input/Output (SIO)

A Z-80A SIO chip is used on the card to provide the serial data communications channel. The major functions performed by the SIO chip are serial-to-parallel conversion of input data and parallel-to-serial conversion of output data.



HP 12794A HDLC MODEM INTERFACE

Figure 4-1. HDLC Modem Interface Functional Block Diagram

Direct Memory Access (DMA)

The card uses two Z-80A DMA chips which are LSI DMA controllers. One of these DMA chips is used to transfer data from the SIO Channel to the card memory; the other is used to transfer data between the host computer and the card memory. The primary function of the DMA logic is to transfer bytes of data in a manner that will be transparent to the Z-80A CPU software. This enables the card to achieve higher throughput rates.

Counter Timer Circuit (CTC)

The card uses one Z-80A CTC chip which provides four independent counter/timers. Two of the counter/timers are used as a baud rate generators and one is used as a timer for the HDLC protocol. The fourth is used to maximize the effective card throughput by controlling the frequency of DMA cycle stealing.

Read-Only Memory (ROM)

The card uses 6k bytes of ROM on two chips. All of the software required to implement the functions of HDLC protocol generation, backplane interaction control and modem control is contained in these chips and is referred to as firmware. The self-check routine is also contained in ROM.

Random-Access Memory (RAM)

The card has 16k bytes of dynamic RAM. This memory is used for data buffers and the storage of firmware variables. The refresh capability of the Z-80A CPU is used to provide the appropriate refresh signals to the dynamic RAM chips.

Communication Line Interface

The communication line interface is the point at which the card "talks" to the serial I/O transmission line. The card is capable of supporting EIA RS-232-C, CCITT V.24 and EIA RS-449 serial I/O implementations. For the purposes of this discussion, the various communications circuits are referred to by their RS-449 names. A comparison of EIA RS-232-C, CCITT V.24 and EIA RS-449 circuits and their respective signal connector pin assignments are given in Section VII.

The EIA RS-449 standard consists of a combination of single-ended (EIA RS-423) and differential (EIA RS-422) drivers and receivers. The card uses both single-ended and differential drivers on some lines and only single-ended drivers on others. All of the receivers on the card are differential although some are connected in such a way that they can only receive single-ended signals. The manner in which each signal is driven or received is illustrated in Figure 4-2.

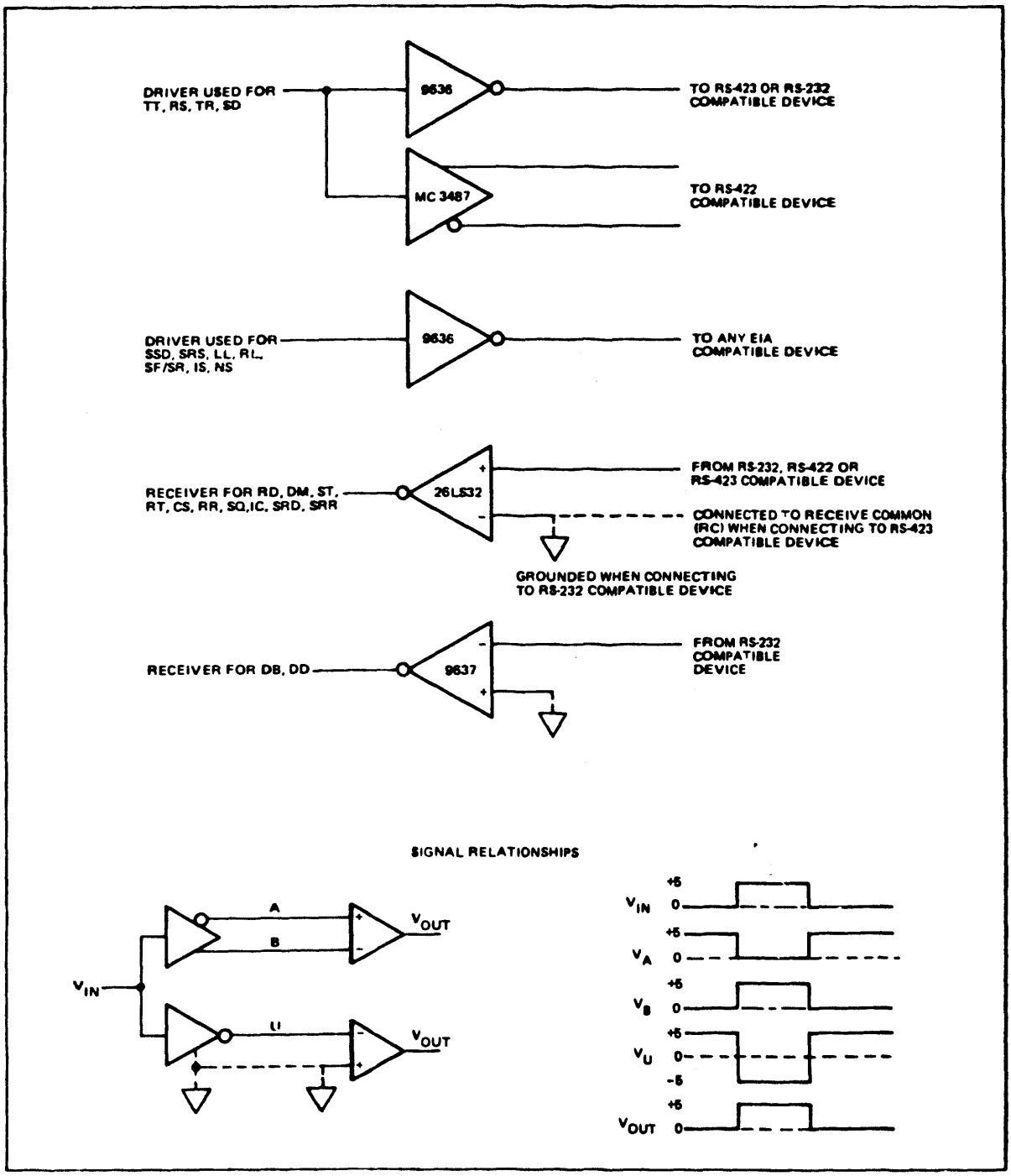


Figure 4-2. Driver/Receiver Combinations

A single-ended driver produces one inverted output whereas its differential counterpart drives both the inverted and non-inverted signals. It is important to note that the mark and space conventions of the protocol are preserved in both cases. The advantage of differential drivers and receivers is that they offer higher noise immunity, thus allowing longer cable lengths and higher data signalling rates.

When a differential receiver is connected to a single-ended driver, the remaining input is connected to ground (RS-232) or to the Receiver Common (RC) circuit of the driving device (RS-449). The various driver/receiver combinations are illustrated in Figure 4-2. The combination used depends on the modem requirements. The receivers on the card can withstand an input voltage range of +/- 25 volts and can operate with a maximum common mode input voltage of +/- 7 volts.

Command and Status Words

In addition to data words, command and status words are also exchanged between the host computer and the card. These additional words are transferred across the data bus and the data latches to aid in the process of communication between the host and the card.

Command words are initiated by the host driver and fall into the following four basic categories:

Type 0 - initiates a data transfer from a card buffer to a host computer buffer.

Type 1 - a single word command sent directly to the card firmware. Examples include disconnect, abort current operation, etc.

Type 2 - initiates a data transfer from a host computer buffer to a card buffer.

Type 3 - specifies that a multiple-word command is to follow.

Status words are generated by the card to inform the host of events that have occurred, are occurring or will be occurring on the card or communications line. Examples of these messages include transfer buffer ready, connect complete, error condition, message block size and modem input line status.

Functional-Level Description

The description given in this section is of a typical operation of the card. The host computer assumed for this discussion is an HP 1000 M/E/F-Series Computer and the communications device is a modem. A modem on the other end of the communications line is connected to an HP 1000 M/E/F/L-Series Computer, employing its own interface card.

Power-Up

Initially, the HP 1000 has been powered up and the communications line is not yet operational. At power-up, a reset signal is asserted that resets all the logic on the card, including the Z-80A components. The resetting of the Z-80A CPU invokes a ROM-resident self-test routine which makes its pass/fail message available to the host driver.

Connect Sequence

The communications line is powered-up with TR (Terminal Ready) asserted for those modems possessing an Auto-Answer feature.

After the physical connection has been made, the two ends must be logically connected. The primary sends a SARM frame and waits for a UA frame from the secondary. In our HP 1000 to HP 1000 configuration, each card sends a SARM frame and waits for a UA frame. When this handshake sequence is complete, a logical connection exists between the two computers.

The "send" handshake involves asserting RS (Request to Send) and waiting for CS (Clear to Send) from the modem. The "receive" handshake involves waiting for RR (Receiver Ready) from the modem and then hunting for the SYN bytes for synchronization.

I/O Backplane Processing

The steps involved in a transfer from the host computer to the communications line (i.e., an output transfer) are as follows (the numbers in parentheses reference the various data paths and functional areas in Figure 4-1):

1. The host (software) driver issues a request for for output buffers (command type 1) onto the data latches (7) and then causes a Z-80A NMI (5). Because of the NMI, the firmware interprets the data in the latches as a command.

2. When a buffer becomes available, the host driver requests a transfer (command type 2) and enables the DCPC (Dual Channel Port Controller) hardware of the host.

3. The card writes zeros to the output latches (7). This starts the DCPC transfer from the host involving the backplane latches (7), control logic (13), data bus (6), DMA chip (4) and RAM (12).

4. The card interrupts the host (13) when the data transfer is complete.

5. The host may transfer additional blocks of data to the the card as buffer space becomes available. Steps 2 through 4 are repeated until the message is transferred from the host to the card in its entirety.

6. Each data block in the RAM buffer on the card is transferred via DMA (3) to the SIO (2) when the SIO chip becomes ready for the transfer. The SIO transmits the data as it is received. The CRC frame check sequence is sent as required.

Keep in mind that the CPU (5) is controlling all of the processing on the card by executing instructions that it fetches from ROM (10) and (11).

The steps involved in a transfer from the communications line to the host computer (i.e., an input transfer) are as follows:

1. The host driver enables inputs from the card by enabling a command word (command type 1) into the data latches (7).

2. The card firmware then sends a status word via the data latches (7) to the host driver informing it that an input buffer is available.

3. The host driver issues a request for input data command type 0) and enables the DCPC hardware of the host computer.

4. The card enables the first data word into the data latches (7) and asserts SRQ via the backplane logic (13).

5. The host driver begins the data transfer and the data block is transferred from the RAM (13) on the card to the host via a DMA chip (4), the data bus (6), the backplane latches (7) and the backplane handshake logic (13). Steps 2 through 5 are repeated until the entire message has been transferred.

6. The host is interrupted when the transfer is complete.

Disconnect Sequence

The communications line is logically disconnected after each station sends a DISC frame and receives a UA frame. Either end of the DS link can initiate the disconnect sequence. The line is physically disconnected after TR and RS have been dropped.

Section 5
Maintenance

Introduction

This section provides maintenance information for the HP 12794A HDLC Modem Interface Kit. Included are preventive maintenance instructions and troubleshooting information.

Preventive Maintenance

There is no preventive maintenance (PM) necessary for the HP 12794A other than a routine inspection of the equipment which can be performed at the same time that PM is done for the entire system. The card and cables should be checked for broken components, or the presence of foreign objects.

A self-test, residing in the firmware, is executed each time that power is applied to the card or the card is reset. In this manner, the interface card is checked automatically and only requires more thorough testing when specific failures occur.

Troubleshooting Techniques

CAUTION

ALWAYS TURN POWER OFF TO THE COMPUTER AND OTHER ASSOCIATED EQUIPMENT WHEN INSERTING OR REMOVING INTERFACE CARDS OR CABLES. FAILURE TO DO SO COULD RESULT IN DAMAGE TO THE EQUIPMENT.

CAUTION

STATIC SENSITIVE DEVICES

THE ROMS, RAMS, AND Z-80A COMPONENTS USED IN THIS PRODUCT ARE SUSCEPTIBLE TO DAMAGE BY STATIC DISCHARGE. REFER TO THE SAFETY CONSIDERATIONS INFORMATION AT THE FRONT OF THIS MANUAL BEFORE REPLACING.

Once it has been determined that the hardware of the HP 1000-to-HP 1000 link is failing, proceed as follows to localize the failure to the specific component failing:

1. Run the following tests at both HP 1000s on the link:

   a. DSINF Card Configuration Check. (Follow the procedure outlined in the interface card configuration check paragraphs in Section 2 of this manual.)

   b. Firmware self-test.

   c. Loop-back verifier hood test.

2. If the above procedures are carried out successfully, it is reasonably certain that the interface cards and software/firmware at the HP 1000 nodes are operational. This implies that the failure is due to the cabling, the modems used, or the line quality. The modems in the link should be checked out at this time if possible. Refer to the appropriate manuals for self-test/diagnostic information.

Other troubleshooting aids for investigating line quality and use are discussed in the last paragraphs of this section.

3. If a failure is found using one of the above test procedures, replace the failing card or firmware and repeat the test that failed to verify that the problem has been properly corrected. If the problem is still present with new equipment, refer to the last paragraph of this section for further troubleshooting procedures.

Firmware Self-Test

A self-test is available for the interface card included with the HP 12794A. The test examines CPU operation, on-board DMA operation (channels 0 and 1), counter/timer chip performance, RAM and ROM memory, and some parts of the receiver/driver circuits and controller. The test does not check the backplane circuitry on the card.

The self-test is located in the firmware ROMs on the interface card and is run at power up or whenever the card is reset (whenever a CLC 0 is sent to the card). It can be run by pressing the PRESET button on the front panel or by cycling power on the computer. Note that these procedures require system and DS software reinitialization after running the test. It is recommended that the node is quiesced before running self-test. This will allow all pending DS transactions to be completed and prevent new ones from starting. To quiesce the node, enter the commands RU,DSMOD<cr> and, after DSMOD prompts for a command, enter /Q. (For a description of DSMOD, refer to the DS/1000-IV Network Manager's Manual, HP part number 91750-90003.) DSMOD prompts for the network security code which can be obtained from the network manager. The default security code is DS. Once the "NODE IS QUIESCENT" message appears on the screen, cycle power on the computer.

Self-test results are made available to the driver once the test is complete. To find out if the card passed the self-test, try executing the LU command after running DSINF as described in the interface card configuration check given in Section 2. The LEDs on the card will also indicate successful completion of the tests with all of them being turned off after the test is finished and before DS software has been initialized.

Loop-Back Verifier Hood Test

Run the loop-back verifier hood test by proceeding as follows:

1. Quiesce the node. This allows all pending transactions to be completed and prevents new ones from starting before running the test. Follow the same procedure used in the self-test section for quiescing the node. Remove power from the computer once the node is quiescent.

2. Remove the cable from the front edge connector and install the loop-back verifier hood, HP part number 5061-3425, in its place, orienting the connector the same as all other connectors in the card cage.

3. Restore power ot the system. When this occurs, the self-test is automatically executed on the card. The results of the test are returned to the software driver. Restore the operating system and check that the self-test completed successfully and that the hood was sensed by running DSINF and checking the information returned with the LU command.

4. Once it has been established that the card passed the self-test and that the hood has been sensed, a further check or the card can be accomplished by sending a message to the card and having it looped back on itself. This will thoroughly check out all message sending and receiving capabilities of the card and card/computer interaction capabilities. To configure the card to talk to itself, start by running DSMOD. Enter the command CN. DSMOD will prompt for the network security code which can be obtained from the network manager. After that has been entered, DSMOD will prompt for the node number to be changed. Enter the local node number. DSMOD will display the current routing vector for the local node which should specify LU 0. Then after the prompt for the new configuration, enter the LU # of the card that has the loop-back verifier hood installed on it. Now enter /E in response to the prompt for the next node number to be changed, and another /E to exit DSMOD. The card is now configured to talk to the local node.

5. Run REMAT and execute some REMAT commands such as TI or DL. When this happens, the routing vector will specify that all commands to be executed at the local node should be sent out to the configured interface card. The card will transmit the data, it will be looped back through the hood, and the card will receive the data and send it back to the local CPU. If no errors are returned, this is a very good indication that the interface card and backplane circuitry are operational.

6. Once the test is complete, run DSMOD and reconfigure the local node routing vector to again specify LU 0.

7. To remove the loop-back verifier hood, remove power from the system and replace the hood with the cable.

8. Restore power to the computer and reinitialize the system and DS software.

Since the loop-back verifier hood test checks more areas of the card (specifically the line drivers and receivers area of the interface, and the backplane interface circuitry), it is possible for the card to pass the self-test and fail the loop-back hood test. Therefore it is important that both the self-test and the loop-back verifier hood test are run.

Other Troubleshooting Aids

If problems occur that cannot be identified using the hardware tests described above, there are other troubleshooting tools available. However, these tools require more familiarity with hardware operations, HDLC protocol, and characteristics of line use for the link being tested. Therefore, a review of the Theory of Operation and Protocol sections of this manual is recommended before proceeding. Detailed troubleshooting techniques are further discussed in the DS/1000-IV Network Manager's Manual, HP part number 91750-90003. Refer to that manual for information on DS utility programs availble and their use as troubleshooting aids.

Section 6
Replaceable Parts

Introduction

This section contains information for ordering replaceable parts for the HP 12794A HDLC Modem Interface Kit. Table 6-1 gives a list of replaceable parts, and Table 6-2 contains names and manufacturers of the parts.

Replaceable Parts

Table 6-1 contains a list of replaceable parts in reference designation order. The following information is listed for each part:

1. Reference designation of the part. Refer to Table 6-1 for an explanation of the abbreviations used in the "REFERENCE DESIGNATION" column.
2. The Hewlett-Packard part number.
3. Part number check digit (CD).
4. Total quantity (QTY).
5. Description of the part.
6. A five-digit manufacturer's code number of a typical manufacturer of the part.
7. The manufacturer's part number.

Ordering Information

To order replacement parts or to obtain information on parts, address the order or inquiry to the local Hewlett-Packard Sales and Service Office (Sales and Service Offices are listd at the back of this manual).

To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number (with the check digit), and indicate the quantity required. The check digit will insure accurate and timely processing of your order.

To order a part that is not listed in the replaceable parts table, specify the following information:

1. Identification of the kit containing the part (refer to Section 1 of this manual).
2. Description and function of the part.
3. Quantity required.

Table 6-1. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	9041-3418	5	1	MI PROGRAM DEP IP	28480	9041-3418
C95	1990-0662	0	1	LED-VISIBLE LUM-INT=200UCD IF=5MA-MAX	28480	1990-0662
Q1	1853-0015	7	1	TRANSISTOR PNP SI PD=200MW FT=60MHZ	28480	1853-0015
Q2	1854-0019	3	1	TRANSISTOR NPN SI TO-18 PD=360MW	28480	1854-0019
R5	1810-0276	2	3	NETWORK-RES 10-SIP1.5K OHM I O	01121	210A152
R6	1810-0279	5	4	NETWORK-RES 10-SIP4.7K OHM I O	01121	210A472
R7	1810-0279	5		NETWORK-RES 10-SIP4.7K OHM I O	01121	210A472
R12	1810-0279	5		NETWORK-RES 10-SIP4.7K OHM I O	01121	210A472
R13	1810-0279	5		NETWORK-RES 10-SIP4.7K OHM I O	01121	210A472
R14	1810-0276	2		NETWORK-RES 10-SIP1.5K OHM I O	01121	210A152
R16	1810-0276	2		NETWORK-RES 10-SIP1.5K OHM I O	01121	210A152
R19	1810-0280	6	2	NETWORK-RES 10-SIP10.0K OHM I O	01121	210A103
R20	1810-0280	6		NETWORK-RES 10-SIP10.0K OHM I O	01121	210A103
S1	3101-1903	9	1	SWITCH-DIP, 8-ROCKER	28480	3101-1903
U11	1820-2203	0	4	IC RCVR TTL LS LINE RCVR QUAD	34335	AM26LS32PC
U12	1820-1729	3	2	IC LCH TTL LS COM CLEAR 8-BIT	01295	SN74LS259N
U13	1820-2300	3	1		28480	1820-2300
	1200-0654	7	4	SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
U15	1820-1430	3	1	IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
U21	1820-2203	0		IC RCVR TTL LS LINE RCVR QUAD	34335	AM26LS32PC
U22	1820-1298	1	1	IC MUXR/DATA-SEL TTL LS 8-TO-1-LINE	01295	SN74LS251N
U25	1820-1216	3	1	IC DCDR TTL LS 3-TO-8-LINE INV	01295	SN74LS138N
U26	1913-0129	0	1	IC DSC HYBRID	34364	R1100A
	1200-0638	7	1	SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
U27	1820-1989	7	1	IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
U31	1820-2203	0		IC RCVR TTL LS LINE RCVR QUAD	34335	AM26LS32PC
U33	1820-2299	4	2		28480	1820-2299
	1200-0654	7		SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
U35	5090-1610	0	1	IC-4300=1	28480	5090-1610
U36	1820-1197	9	3	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U37	1820-1988	9	11	IC DRVR TTL LINE DRVR DUAL 4-INP	18324	N8T13N
U38	1820-1799	5	1	IC DRVR TTL NAND DUAL 2-INP	01295	SN75452BP
U41	1820-2203	0		IC RCVR TTL LS LINE RCVR QUAD	34335	AM26LS32PC
U42	1820-1112	8	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U43	1820-2299	4			28480	1820-2299
	1200-0654	7		SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
U45	1820-0693	8	2	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U46	1820-1201	6	2	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U47	1820-1988	9		IC DRVR TTL LINE DRVR DUAL 4-INP	18324	N8T13N
U51	1820-2145	9	1	IC DRVR TTL LINE DRVR QUAD	04713	MC34079
U52	1820-2024	3	1	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U55	1820-0083	4	1	IC INV TTL S HEX 1-INP	01295	SN74S04N
U56	1820-1440	5	1	IC LCH TTL LS QUAD	01295	SN74LS279N
U57	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U61	1820-1244	7	2	IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS153N
U62	1820-1729	3		IC LCH TTL LS COM CLEAR 8-BIT	01295	SN74LS259N
U63	1820-2298	3	1		28480	1820-2298
	1200-0654	7		SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
U65	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U66	1820-1616	5	1	IC SCHMITT-TRIG TTL LS INV HEX 1-INP	01295	SN74LS14N
U67	1820-1988	9		IC DRVR TTL LINE DRVR DUAL 4-INP	18324	N8T13N
U71	1820-1244	7		IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS153N
U72	1810-0341	8	8	IC NMOS 16384-BIT RAM DYN 200-NS 5-V	00013J	UPD416D-2
	1200-0607	8	8	SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
U74	1820-2301	9	1		28480	1820-2301
	1200-0567	1	3	SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0567
U75	1820-1208	3	2	IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U76	1820-1202	7	1	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
U77	1820-1988	9		IC DRVR TTL LINE DRVR DUAL 4-INP	18324	N8T13N
U81	1820-2198	2	1	IC RCVR TTL S LINE RCVR DUAL	07263	9637ATC
U82	1810-0341	8		IC NMOS 16384-BIT RAM DYN 200-NS 5-V	00013J	UPD416D-2
	1200-0607	8		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
U85	1820-1208	3		IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U86	1820-1201	6		IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U87	1820-1988	9		IC DRVR TTL LINE DRVR DUAL 4-INP	18324	N8T13N
U91	1820-2117	5	6	IC DRVR TTL LINE DRVR DUAL	07263	9636ATC
U92	1810-0341	8		IC NMOS 16384-BIT RAM DYN 200-NS 5-V	00013J	UPD416D-2
	1200-0607	8		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
	1200-0567	1		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0567

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-1. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U95	5090-0999	8	1	IC-NOM	28480	5090-0999
U96	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U97	1820-1880	9		IC DRVR TTL LINE DRVR DUAL 6-INP	18324	N8T13N
U101	1820-2117	5		IC DRVR TTL LINE DRVR DUAL	07263	9636ATC
U102	1818-0341	8		IC MMOS 16384-BIT RAM DYN 200-NS 3-0	0003J	UPD4108-2
	1200-0007	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0007
	1200-0883	0	1	SOCKET-IC 14-CONT DIP-SLDR	28480	1200-0883
U106	1820-1184	4	1	IC GPR TTL NOR QUAD 2-INP	01295	SN74S02N
U107	1820-1880	9		IC DRVR TTL LINE DRVR DUAL 6-INP	18324	N8T13N
U201	1820-2117	5		IC DRVR TTL LINE DRVR DUAL	07263	9636ATC
U202	1818-0341	8		IC MMOS 16384-BIT RAM DYN 200-NS 3-0	0003J	UPD4108-2
	1200-0007	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0007
	1200-0507	1		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0507
U204	1820-1997	7	4	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U205	1820-1880	9		IC DRVR TTL LINE DRVR DUAL 6-INP	18324	N8T13N
U301	1820-2117	5		IC DRVR TTL LINE DRVR DUAL	07263	9636ATC
U302	1818-0341	8		IC MMOS 16384-BIT RAM DYN 200-NS 3-0	0003J	UPD4108-2
	1200-0007	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0007
U303	1820-1478	1	2	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
U304	1820-2075	6	1	IC MISC TTL LS	01295	SN74LS240N
U305	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U306	1820-1880	9		IC DRVR TTL LINE DRVR DUAL 6-INP	18324	N8T13N
U307	1820-2117	5		IC DRVR TTL LINE DRVR DUAL	07263	9636ATC
U401						
U402	1818-0341	8		IC MMOS 16384-BIT RAM DYN 200-NS 3-0	0003J	UPD4108-2
	1200-0007	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0007
U403	1820-1478	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
U404	1820-1917	1	1	IC GPR TTL LS LINE DRVR UCTL	01295	SN74LS240N
U405	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U407	1820-1880	9		IC DRVR TTL LINE DRVR DUAL 6-INP	18324	N8T13N
U501	1820-2117	5		IC DRVR TTL LINE DRVR DUAL	07263	9636ATC
U502	1818-0341	8		IC MMOS 16384-BIT RAM DYN 200-NS 3-0	0003J	UPD4108-2
	1200-0007	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0007
U503	1820-1207	2	1	IC GATE TTL LS NAND 8-INP	01295	SN74LS30N
U504	1820-0220	9	1	IC V REGTR 70-3V	27014	LM320M-05
	1200-0185	9	1	INSULATOR-REGTR MTLDN	28480	1200-0185
U506	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U507	1820-1880	9		IC DRVR TTL LINE DRVR DUAL 6-INP	18324	N8T13N
				MISCELLANEOUS PARTS		
	1480-0110	8	1	PIN-SPR .062-IN-DIA .25-IN-LG STL	28480	1480-0110
	9001-3031	2	1	AXIAL INSERTION	28480	9001-3031

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Manufacturer's Code List

CODE NO.	MANUFACTURER ADDRESS	CODE NO.	MANUFACTURER ADDRESS
0003J	Nippon Electric Co.	07263	Fairchild Semiconductor Div. Mt View, CA 94042
01121	Allen-Bradley Co. Milwaukee, WI 53204	18324	Signetics Corp. Sunnyvale, CA 94086
01295	Texas Instr. Inc. Semicond. Cmpnt. Div. Dallas TX 75222	27014	Natl Semiconductor Corp. Santa Clara, CA 95051
03508	General Electric Co., Semiconductor Prod. Dept. Syracuse, NY 13201	28480	Hewlett-Packard Co. Corporate Hq. Palo Alto, CA 94304
04713	Motorola Semiconductor Prod. Phoenix, AZ 85062	34335	Advanced Micro Dev. Inc. Sunnyvale CA 94086
		91344	Motorola Inc. Franklin Park, IL 60131

Section 7
Servicing Diagrams and Information

Introduction

This section contains servicing diagrams and information for the HP 12794A HDLC Modem Interface Kit.

Table 7-1. Backplane Connections (Connector P1)

PIN NO.	SIGNAL MNEMONIC	SIGNAL NAME
1	GND	Ground
2	GND	Ground
3	PRL	Priority Low
4	FLAGL	Flag Signal, Lower Select Code
5	SFC	Skip if Flag is Clear
6	IRQL	Interrupt Request, Lower Select Code
7	CLF	Clear Flag
8	IEN	Interrupt Enable
9	STF	Set Flag
10	IAK	Interrupt Acknowledge
11	T3	I/O Time Period 3
12	SKF	Skip on Flag
13	CRS	Control Reset
14	LSCM	Select Code Most Significant Digit (Lower Address)
15	IOG	I/O Group
16	LSCL	Select Code Least Significant Digit (Lower Address)
17	POPIO	Power On Preset to I/O
18	BIOS	"Not" Block I/O Strobe (E-series only)
19	SRQ	Service Request
20	IOO	I/O Data Output Signal
21	CLC	Clear Control
22	STC	Set Control
23	PRH	Priority High
24	IOI	I/O Data Input Signal
25	SFS	Skip if Flag is Set
26	IOBI 0	I/O Bus Input, bit 0

Table 7-1. Backplane Pin Connector P1 (Continued)

27	IOBI 8	I/O Bus Input, bit 8
28	IOBI 9	I/O Bus Input, bit 9
29	IOBI 1	I/O Bus Input, bit 1
30	IOBI 2	I/O Bus Input, bit 2
31	IOBI 10	I/O Bus Input, bit 10
32	SIR	Set Interrupt Request
33	IRQH	Interrupt Request (Higher Select Code)
34	HSCL	Select Code Least Significant Digit (Higher Address)
35	IOBO 0	I/O Bus Output, bit 0
36	+28 Volts	
37	HSCM	Select Code Most Significant Digit (Higher Address)
38	IOBO 1	I/O Bus Output, bit 1
39	+5 Volts	
40	+5 Volts	
41	IOBO 2	I/O Bus Output, bit 2
42	IOBO 4	I/O Bus Output, bit 4
43	+12 Volts	
44	+12 Volts	
45	IOBO 3	I/O Bus Output, bit 3
46	ENF	Enable Flag
47	-2 Volts	
48	-2 Volts	
49	FLGH	Interrupt Flag Signal (Higher Select Code)
50	RUN	Run
51	IOBO 5	I/O Bus Output, bit 5
52	IOBO 7	I/O Bus Output, bit 7
53	IOBO 6	I/O Bus Output, bit 6
54	IOBO 8	I/O Bus Output, bit 8
55	IOBO 11	I/O Bus Output, bit 11
56	IOBO 9	I/O Bus Output, bit 9
57	IOBO 12	I/O BUs Output, bit 12
58	IOBO 10	I/O Bus Output, bit 10
59	NOT USED	
60	IOBI 11	I/O Bus Input, bit 11
61	IOBO 13	I/O Bus Output, bit 13
62	EDT	End Data Transfer (DCPC)
63	NOT USED	
64	IOBI 3	I/O Bus Input, bit 3
65	IOBO 14	I/O Bus Output, bit 14

Table 7-1. Backplane Pin Connector P1 (Continued)

66	PON	Power On Normal
67	BIOO	"Not" Block I/O Output (E-Series only)
68	NOT USED	
69	-12 Volts	
70	-12 Volts	
71	NOT USED	
72	NOT USED	
73	BIOI	"Not" Block I/O Input (E-Series only)
74	IOBO 15	I/O Bus Ouput, bit 15
75	NOT USED	
76	NOT USED	
77	IOB 4	I/O Bus Input, bit 4
78	IOB 12	I/O Bus Input, bit 12
79	IOB 13	I/O Bus Input, bit 13
80	IOB 5	I/O Bus Input, bit 5
81	IOB 6	I/O Bus Input, bit 6
82	IOB 14	I/O Bus Input, bit 14
83	IOB 15	I/O Bus Input, bit 15
84	IOB 7	I/O Bus Input, bit 7
85	GND	Ground
86	GND	Ground

Table 7-2. Communication Line Connector (Connector J1).

PIN NO.	SIGNAL MNEMONIC*	SIGNAL DEFINITION
1A	---	No Connection
1B	+12V	+12 Volts Power
2A	---	No Connection
2B	+12V	+12 Volts Power
3A	SSD	Secondary Send Data
3B	---	No Connection
4A	---	No Connection
4B	-12V	-12 Volts Power
5A	---	No Connection
5B	-12V	-12 Volts Power
6A	---	No Connection
6B	---	No Connection
7A	SRS	Secondary Request to Send
7B	TR(A)	Terminal Ready
8A	SD(U)	Send Data
8B	TT(B)	Terminal Timing
9A	RS(U)	Request to Send
9B	TT(U)	Terminal Timing
10A	TR(B)	Terminal Ready
10B	DAMPRT(B)	
11A	RS(A)	Request to Send
11B	TR(U)	Terminal Ready
12A	TT(A)	Terminal Timing
12B	---	No Connection
13A	SD(B)	Send Data
13B	SD(A)	Send Data
14A	---	No Connection
14B	RS(B)	Request to Send
15A	DAMPST(B)	
15B	RT(B)	Receive Timing
16A	CS(B)	Clear To Send
16B	DAMPRD(B)	
17A	CS(A)	Clear to Send
17B	---	No Connection
18A	SQ	Signal Quality
18B	RC	Receive Common
19A	ST(B)	Send Timing
19B	---	No Connection
20A	RD(B)	Receive Data
20B	ST(A)	Send Timing
21A	---	No Connection
21B	**BX16IN	
22A	SRR	Secondary Receiver Ready
22B	---	No Connection

Table 7-2. Communication Line Connector J1 (Continued)

PIN NO.	SIGNAL MNEMONIC*	SIGNAL DEFINITION
23A	RD(A)	Receive Data
23B	TM	Test Mode
24A	RR(B)	Receiver Ready
24B	IC	Incoming Call
25A	SG	Signal Ground
25B	SC	Signal Common
26A	RR(A)	Receiver Ready
26B	**BDATACLK+	
27A	DM(A)	Data Mode
27B	DM(B)	Data Mode
28A	SF/SR	Select Frequency/Signaling Rate
28B	DD	Receive Timing
29A	**ASYNCCLK+	
29B	DA	Terminal Timing
30A	**X16IN	
30B	RT(A)	Receive Timing
31A	SCS	Secondary Clear to Send
31B	DB	Send Timing
32A	SRD	Secondary Receive Data
32B	RL	Remote Loopback
33A	LL	Local Loopback
33B	NS	New Signal
34A	IS	Terminal In Service
34B	---	No Connection
35A	---	No Connection
35B	GND	Power Ground
36A	---	No Connection
36B	GND	Power Ground
37A	---	No Connection
37B	GND	Power Ground
38A	(SHIELD)	
38B	---	No Connection
39A	---	No Connection
39B	+5V	+5 Volts Power
40A	---	No Connection
40B	+5V	+5 Volts Power

* The (A) or (B) after a mnemonic indicates portions of a differential input or output.
The (U) after a mnemonic indicates a single ended version of a signal that appears elsewhere as differential.

** These are TTL level signals for compatibility, they should be used only to loop back for proper firmware operation.

Table 7-3. Serial I/O Circuits and Equivalents

SIGNAL RS-449	SIGNAL RS-232	CCITT V.24	DEFAULT VALUE*	FUNCTION
RD	BB	104	—	RECEIVE DATA
SD	BA	103	1	SEND DATA
CS	CB	106	—	CLEAR TO SEND
RS	CA	105	0	REQUEST TO SEND
TR	CD	108.2	0	TERMINAL READY
RR	CF	109	—	RECEIVER READY
ST	DB	114	—	SEND TIMING
RT	DD	115	—	RECEIVE TIMING
TT	DA	113	—	TERMINAL TIMING
IC	CE	125	—	INCOMING CALL
DM	CC	107	—	DATA MODE
TM	—	142	0	TEST MODE
LL	—	141	0	LOCAL LOOPBACK
RL	—	140	0	REMOTE LOOPBACK
SQ	CG	110	—	SIGNAL QUALITY
SF	CH	126	0	SELECT FREQUENCY
SR	CH	111	0	SELECT SIGNALING RATE
IS	—	—	1	TERMINAL IN SERVICE
NS	—	—	0	NEW SIGNAL
SRD	SBB	119	—	SEC. RECEIVE DATA
SSD	SBA	118	1	SEC. SEND DATA
SRS	SCA	120	0	SEC. REQUEST TO SEND
SCS	SCB	121	—	SEC. CLEAR TO SEND
SRR	SCF	122	—	SEC. RECEIVER READY
SG	AB	102	—	SIGNAL GROUND
SC	—	102a	—	SEND COMMON
RC	—	102b	—	RECEIVE COMMON
—	AA	101	—	PROTECTIVE GROUND

* Pertains to the HP 12794A Interface only.

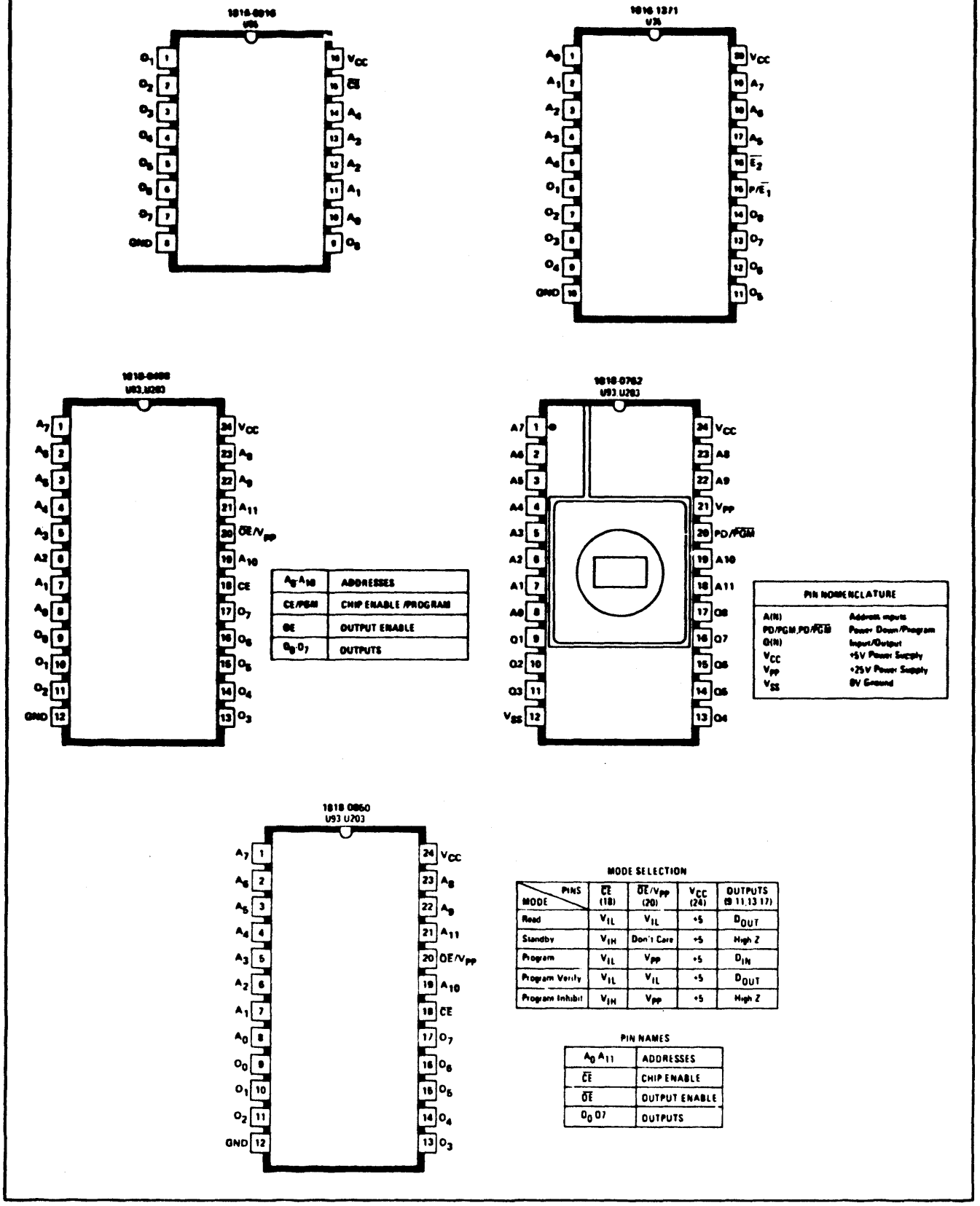


Figure 7-1. Integrated Circuit Base Diagrams.

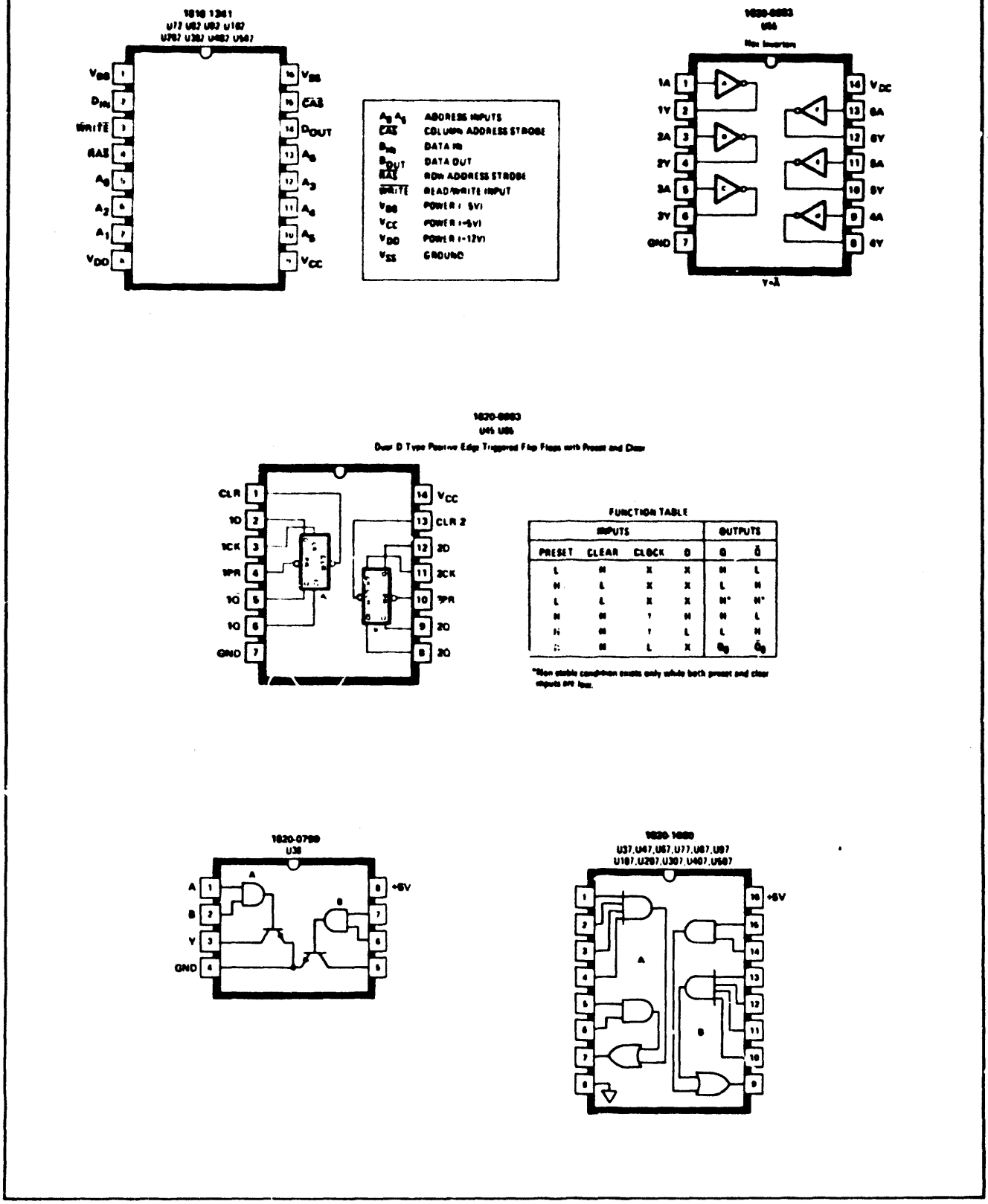


Figure 7-1. Integrated Circuit Base Diagrams (Continued)

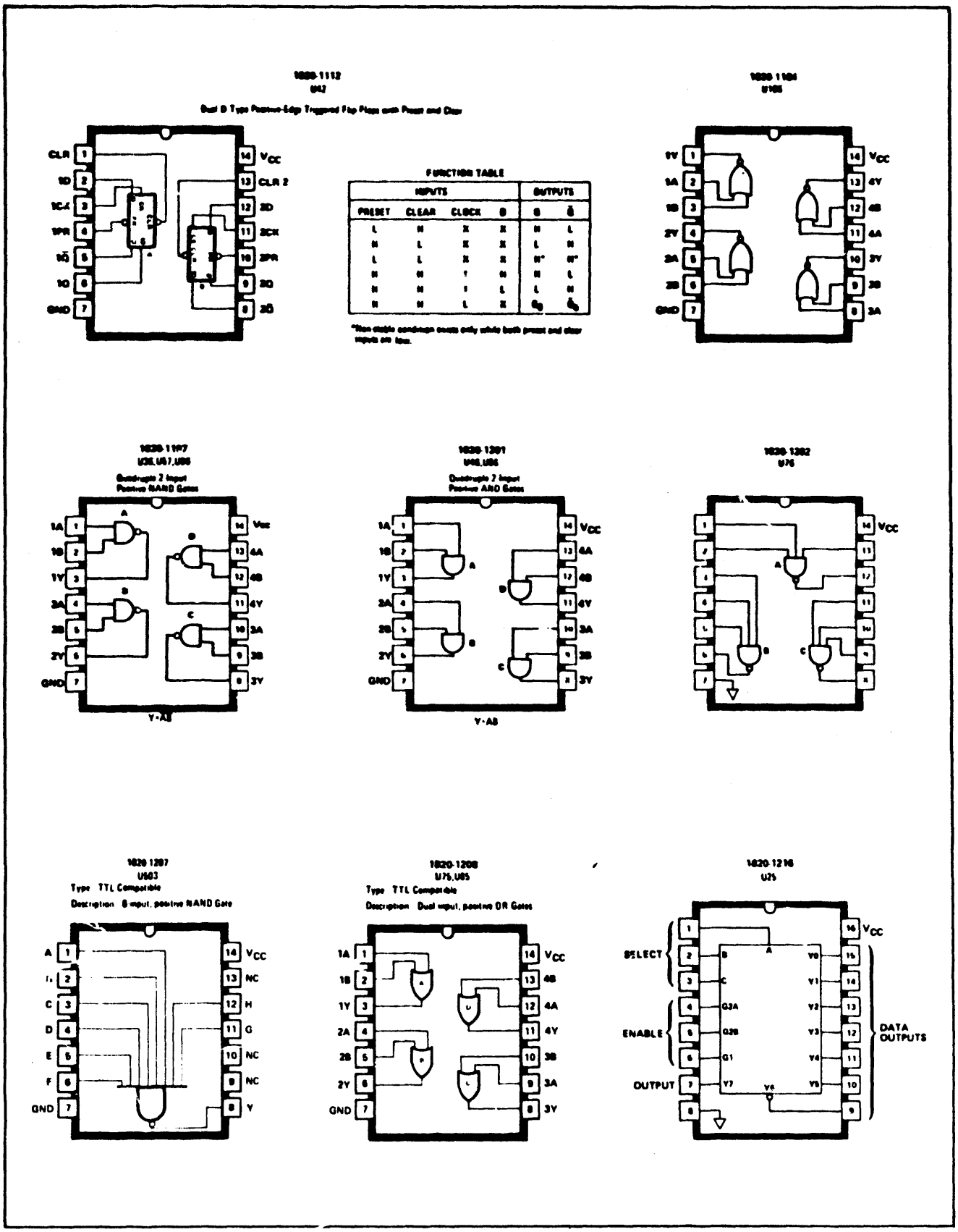


Figure 7-1. Integrated Circuit Base Diagrams (Continued)

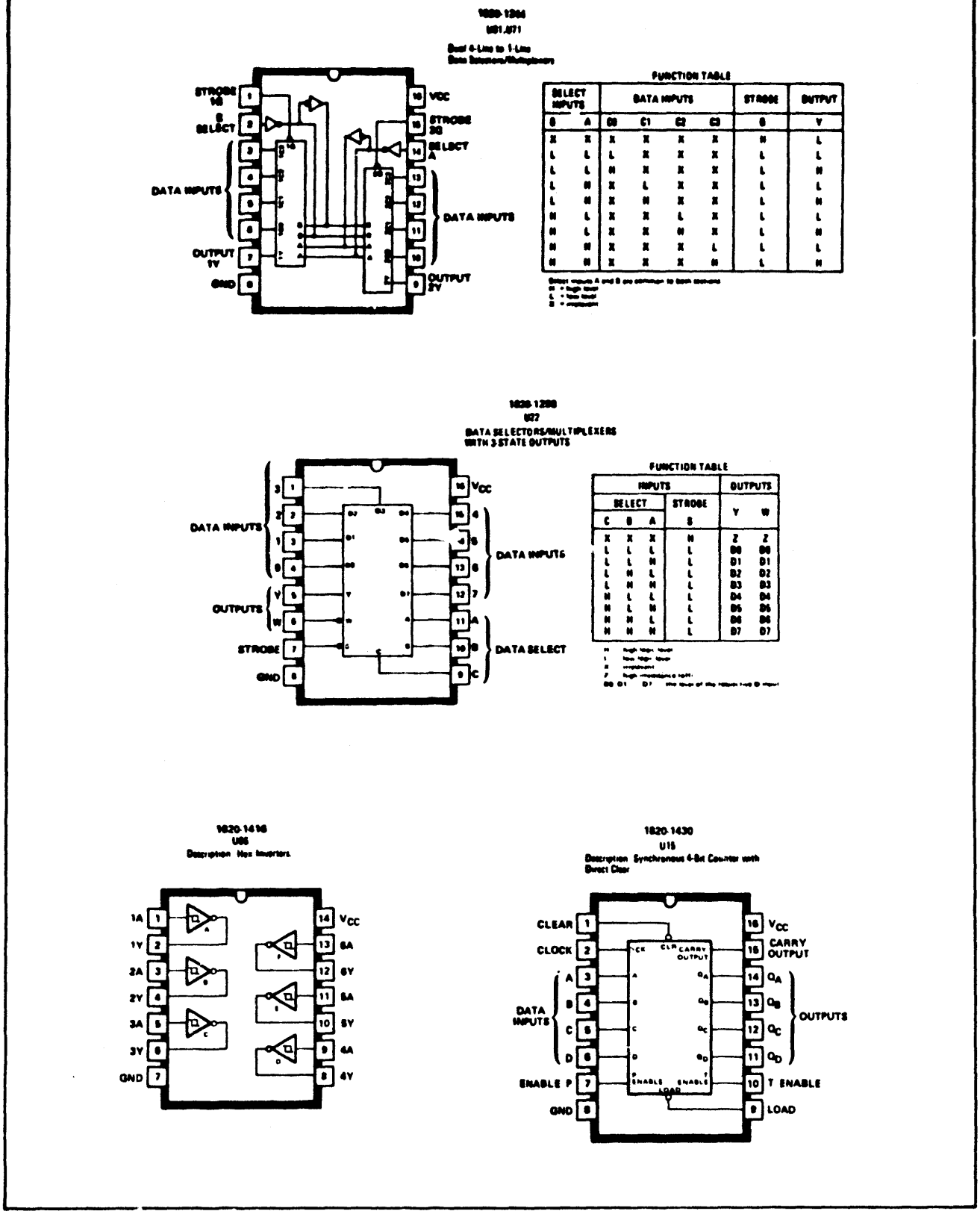


Figure 7-1. Integrated Circuit Base Diagrams (Continued)

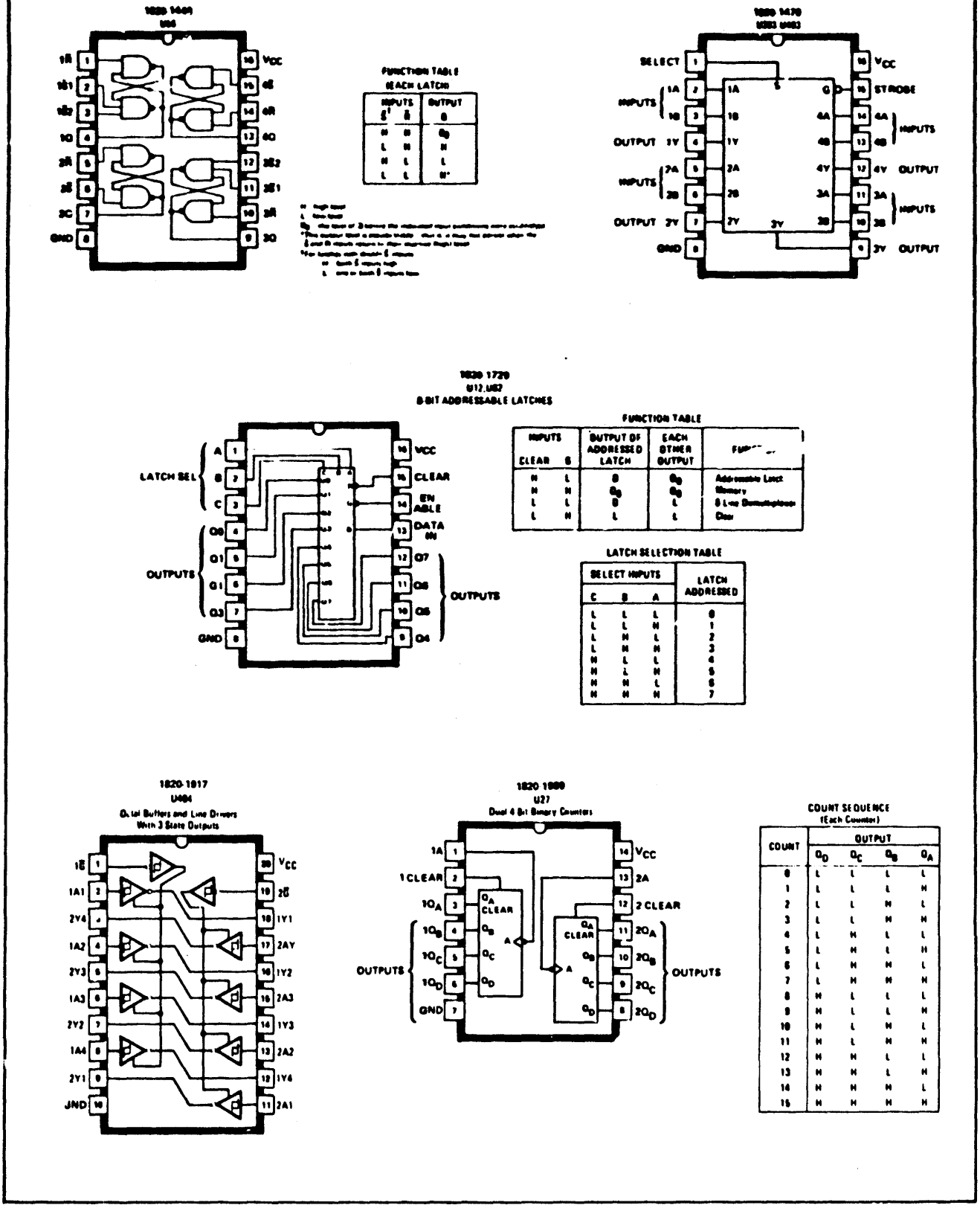


Figure 7-1. Integrated Circuit Base Diagrams (Continued)

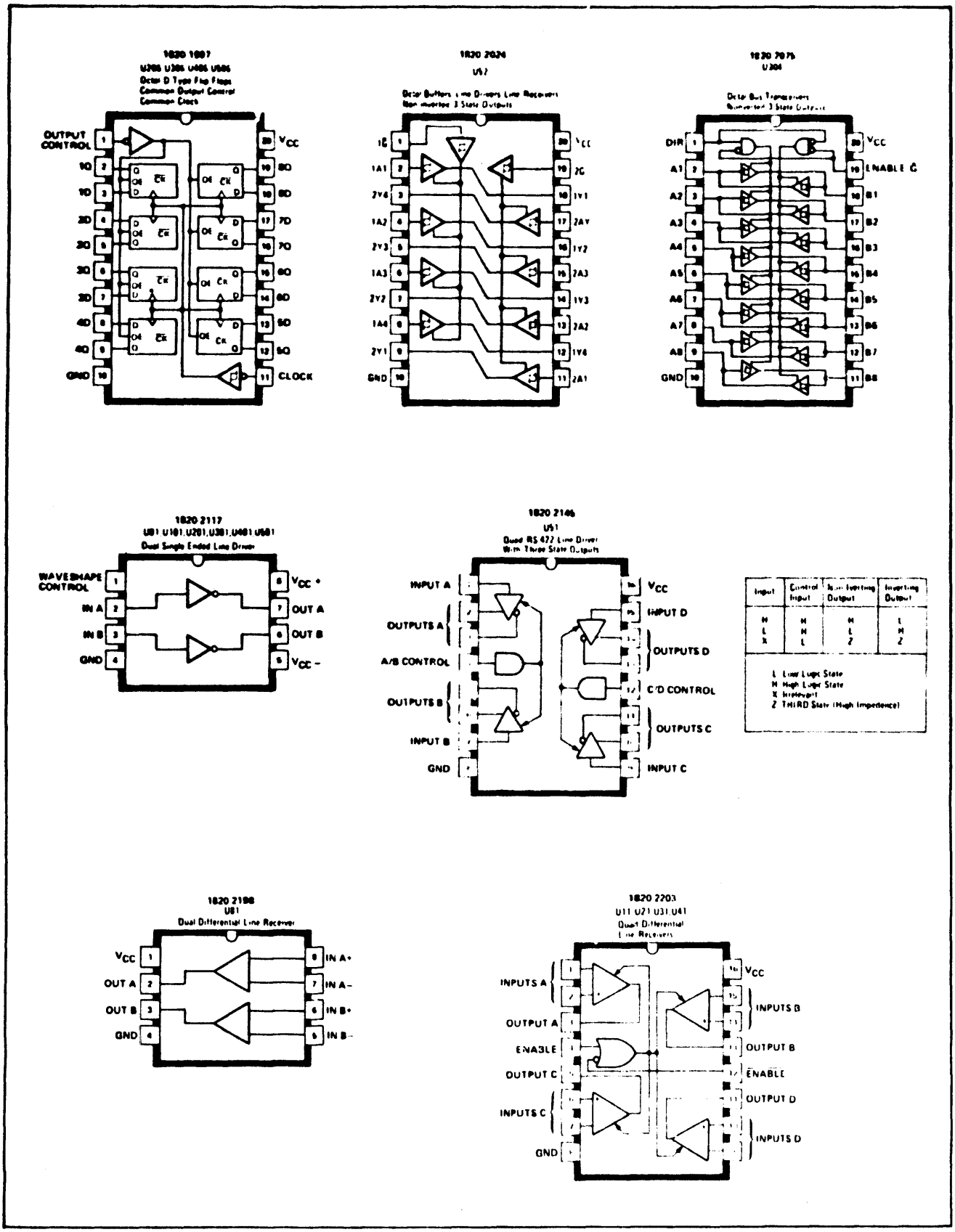


Figure 7-1. Integrated Circuit Base Diagrams (Continued)

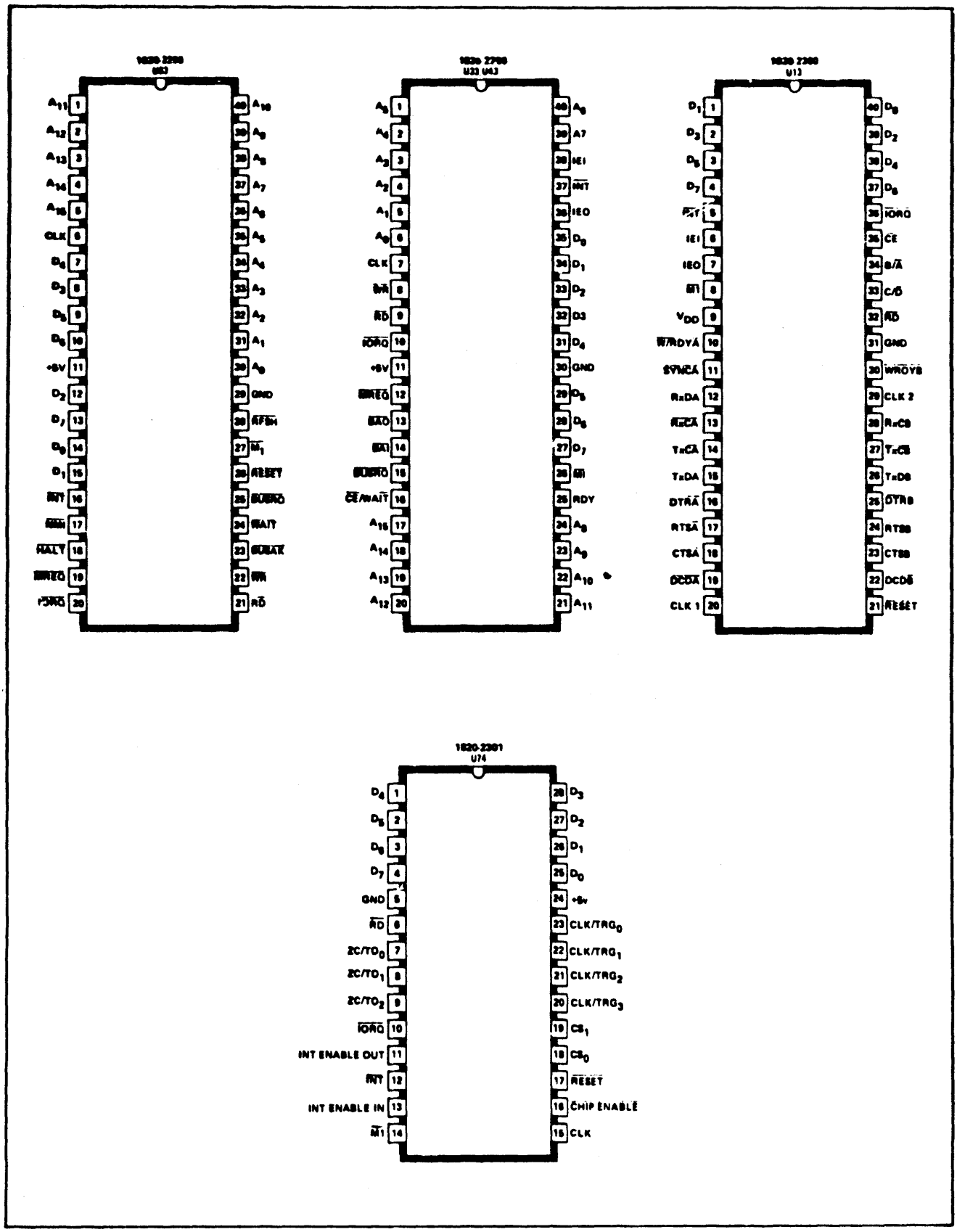


Figure 7-1. Integrated Circuit Base Diagrams (Continued)

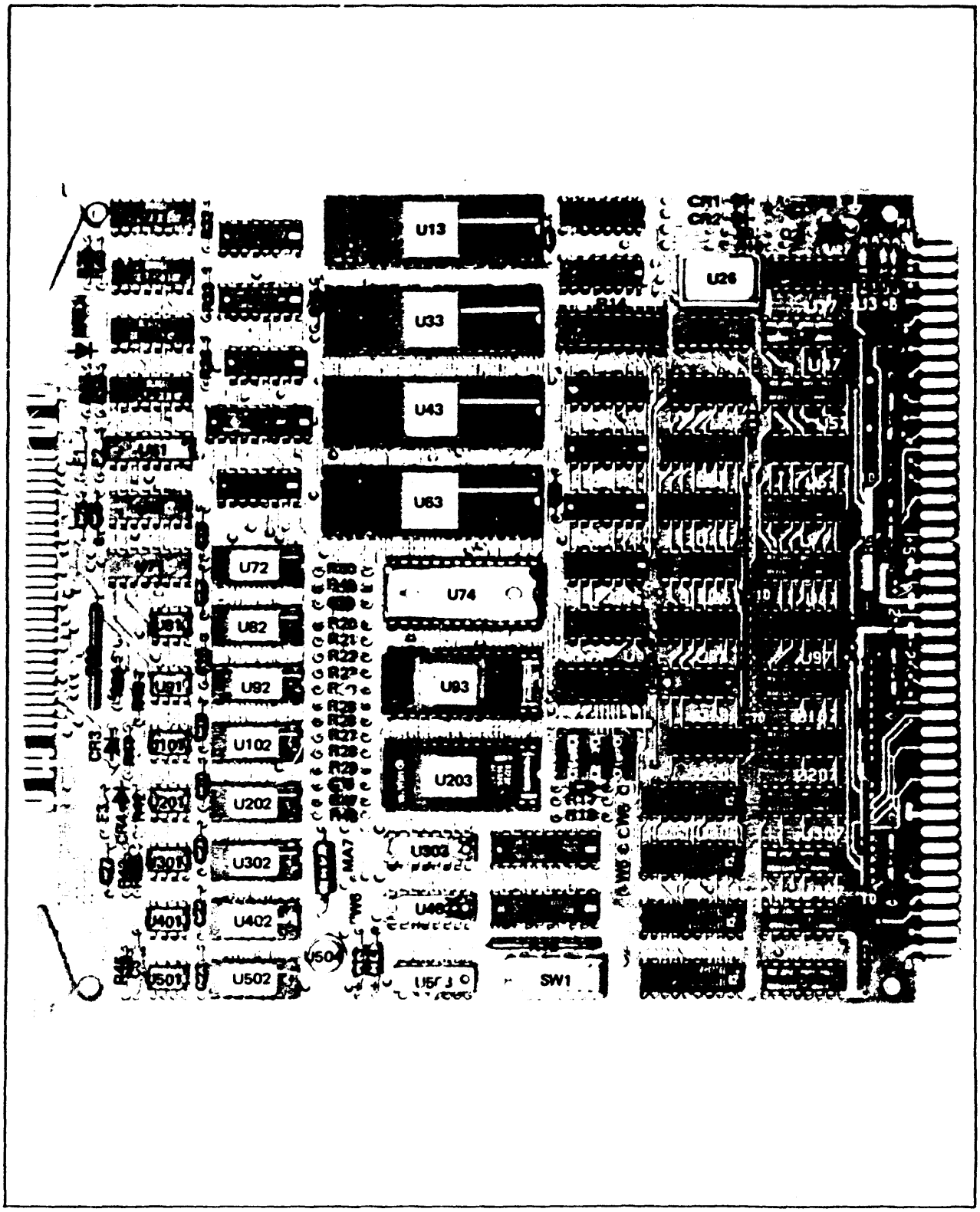


Figure 7-2. HP 12794A HDLC Modem Interface Parts Location Diagram.

Figure 7-3. HP 12794A HDLC Modem Interface Schematic Logic Diagram.

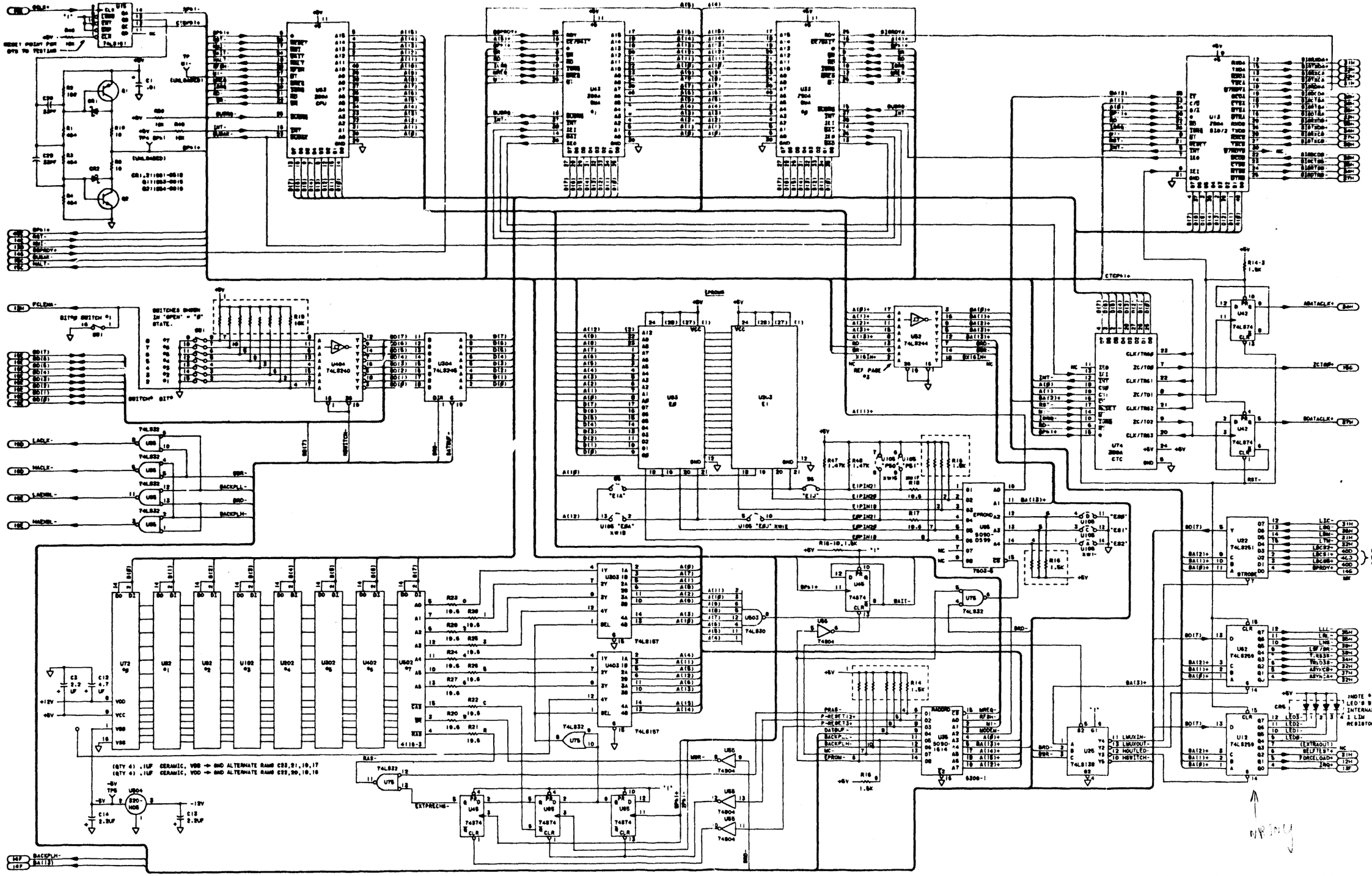
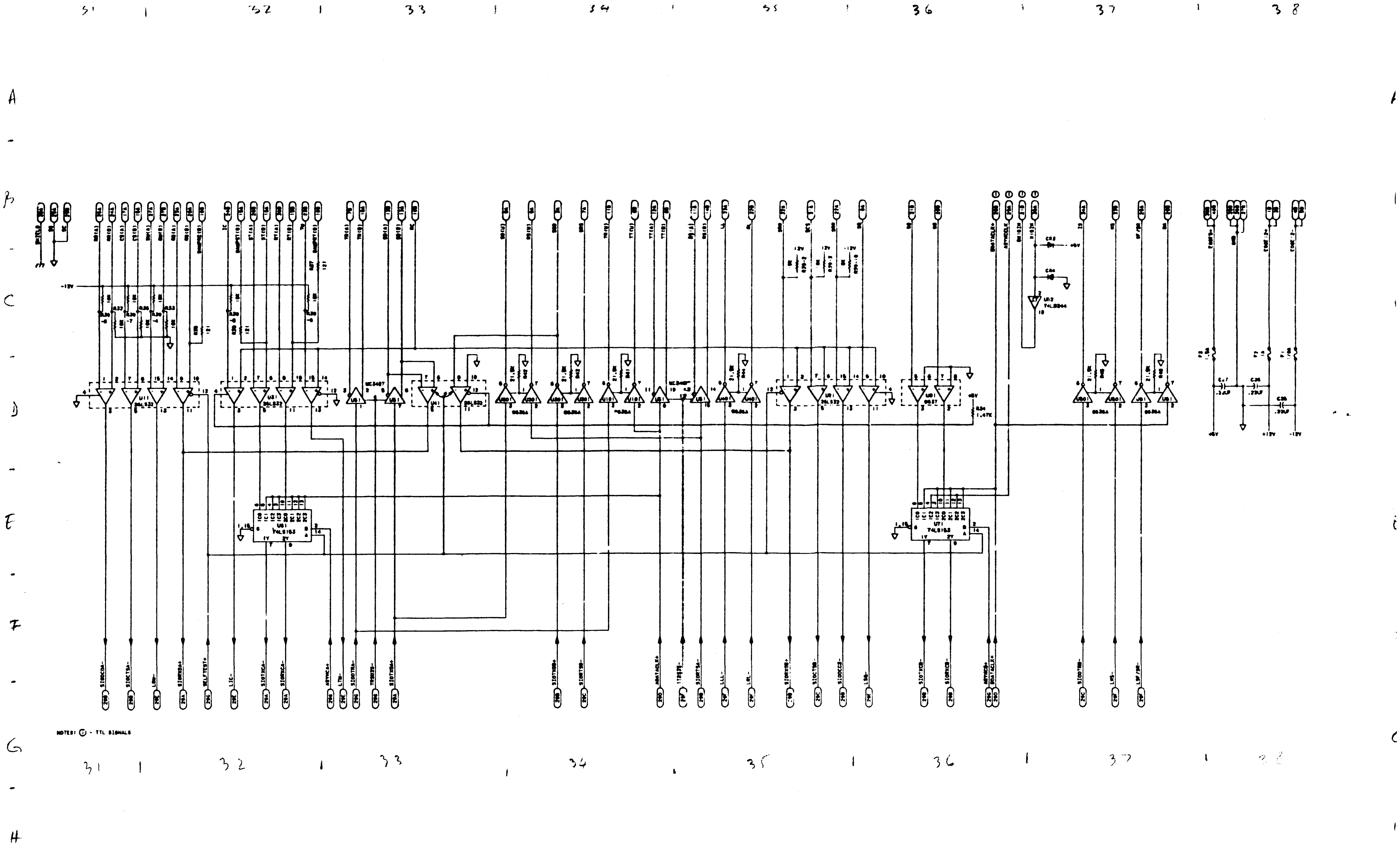


Figure 7-3. HP 12794A Interface Schematic Logic Diagram (Cont.)
7-19/7-20



NOTES: ① - TTL SIGNALS

Figure 7-3. HP 12794A Interface Schematic Logic Diagram (Cont.)

Appendix A
Compatible Modems and Recommended Options

GDC 212A MODEM

The GDC (General DataComm Industries, Inc.) 212A Modem provides full-duplex, synchronous or asynchronous data communications over 2-wire switched networks. It will operate at 0 to 300 bits per second with 103, 113, and 212A types of modems, or 1200 bits per second with other 212A modems. The options available and recommended for use with the HP 12794A HDLC Modem Interface Kit are:

CUSTOMER SPECIFIED OPTIONS

GDC CODE	FEATURE SELECTION	RECOMMENDATION
2a	Async/Start-Stop	
2b	Sync Tx/Rx Clk	2b (required)
5a	9 bits per asynchronous character.	Don't Care
5b	10 bits per asynchronous character.	
6a	Dir. conn. between signal and chassis ground.	6a
6b	100 ohm resistor between signal and chassis ground.	
7a	CC on during analog loopback test.	7a
7b	CC forced off during analog loopback.	
9a	CB off whenever CF is off.	9a
9b	CF has no effect on CB.	
10a	CE remains on in Answer Mode.	
10b	CE on only during ringing.	10b
11a	CI speed indicator signal enabled.	
11b	CI speed indicator signal disabled.	11b
12a	CN circuit controls make busy and analog loopback.	
12b	CN inactive.	12b

GDC 212A MODEM (CONTINUED)

TELEPHONE COMPANY SPECIFIED OPTIONS

GDC CODE	FEATURE SELECTION	RECOMMENDATION
1a	Call is dropped upon receipt of 1.5 second steady space.	
1b	Steady space has no effect on modem.	1b
3a	No steady space transmitted before disconnecting.	3a
3b	Steady space transmitted before disconnecting.	
4a	Disconnect upon loss of carrier signal.	4a
4b	No disconnect upon loss of carrier signal.	
8a	Auto-answer enabled.	8a
8b	Manual answer required.	
13a	Timing from DD receive clock (slave timing).	
13b	Timing from DB transmit clock in modem (internal timing).	13b (required)
13c	Timing from DA external source (external timing).	
14a	Tip-ring busy during analog test.	
14b	Tip-ring not busy during analog test.	14b
15a	High-speed (1200 bits per second only)	Don't care
15b	Either high-speed (1200) or low-speed (300 bits per second)	
16a	Receiver responds to digital loopback test command from remote modem.	Don't care
16b	Receiver responds to digital loopback test command from local modem only.	

GDC 212A MODEM (CONTINUED)

OTHER OPTIONS

GDC CODE	FEATURE SELECTION	RECOMMENDATION
17a	TM signal enable.	17a
17b	TM signal disable.	
18a	565/2565 Telephone.	
18b	502/RTC Telephone.	18b
19a	CN line to business machine on pin 18.	19a
19b	CN line not connected.	
20a	RDL line on pin 19.	
20b	RDL line on pin 21.	20b
20c	RDL line disconnected.	
21a	CH from business machine connected.	21a
21b	CH from business machine disconnected.	

BELL 212A MODEM

The Bell 212A Modem provides full duplex, synchronous or asynchronous communications over a 2-wire switched network. It can operate at 0 to 300 bits per second in an asynchronous mode for operation with 103, 113, or 212A types of modems, or at 1200 bits per second with other 212A modems. The options available and recommended for use with the HP 12794A HDLC Interface are:

CUSTOMER OPTIONS

OPTION	DESCRIPTION	RECOMMENDATION
ZF	CC circuit on during AL test.	ZF
ZE	CC circuit off during AL test.	
XJ	CH circuit controls speed.	
XK	HS button controls speed.	XK
YE	AL/Make Busy controlled by CN circuit or AL button.	Don't Care
YF	AL/Make Busy controlled only by AL button, CN internally held off.	
YC	1200 BPS transmitter driven by internal clock.	YC (required)
YD	1200 BPS transmitter driven by DA circuit.	
WI	1200 BPS transmitter driven by Receive clock (DD).	
YG	Character-oriented operation in the high speed mode.	
YH	Bit synchronous operation in the high speed mode.	YH (required)
YI	9-bit character for 1200 bps async./start-stop operation.	
YJ	10 bit character for 1200 bps async./start-stop operation.	YJ
YK	Digital loop can be remotely activated in the high speed mode.	YK
YL	No response to remote request for a digital loop.	
XL	RL circuit enabled to activate remote digital loop.	XL
XM	RL circuit not connected to interface.	

CUSTOMER OPTIONS (CONT.)

OPTION	DESCRIPTION	RECOMMENDATION
S	Call is dropped if Loss of Carrier occurs.	S
R	Loss of Carrier does not drop call.	
V	Call is dropped if steady space is received.	
Y	Space signal has no effect on modem.	Y
A	CB circuit is turned off whenever CF circuit goes off.	Don't care
B	CB circuit isnot affected by CF circuit.	
T	Steady space transmitted before disconnecting.	
U	No space transmitted before disconnecting.	U
ZH	Auto answer enabled.	ZH
ZG	No response to ringing indication.	
X	Circuit CE remains on after call is answered.	
W	Circuit CE turns off after call is answered.	W
YO	Data can cross interface only in the high speed mode.	
YP	Data can cross the interface in both speed modes.	YP
YQ	Circuit CI indicates speed mode.	
YR	Circuit CI disconnected from interface.	YR
XO	CN on pin 25, TM not connected.	Don't care
XN	CN on pin 18, TM not connected.	
XR	CN on pin 18, TM on pin 25.	
Q	Protective ground and signal ground tied together.	Q
P	No connection between protective ground and signal ground.	

HP 37210T MODEM

The Hewlett-Packard 37210T modem provides half-duplex via dial-up or full-duplex via leaded lines at transfer rates to 4800 bits per second. The options available (determined by assembly switches) and recommended for use with the HDLC Modem Interface are (full-duplex operation only):

FUNCTION OF SWITCHES (O=OPEN, C=CLOSED)	4-WIRE (LEASED) LINE
CONTROL ASSEMBLY	
Factory Set Switches. Must remain as set at factory.	
S10-1, S10-6, S10-7	O O O
S11-4, S11-5	O C
S11-7, S11-8	C C
S12-1 thru S12-4	O O O O
Train Sequence.	
S10-2	C
Receiver Turn-on Delay.	
S10-3	C
External Rate Control Enable/Disable.	
S10-4	C
24 Pushbutton Enable/ Disable.	
S10-5	O
Auto Answer Telephone Select.	
S10-8, S10-9	O C
Transmit Clock.	
S11-1, S11-9	O O
Request-to-Send Delay.	
S11-2	O
2-wire/4-wire Mode.	
S11-3	O

HP 37210T MODEM (CONTINUED)

FUNCTION OF SWITCHES (O=OPEN, C=CLOSED)	4-WIRE (LEASED) LINE
Carrier Select.	
S11-6	C
DISPLAY/PROCESSOR ASSEMBLY	
Factory Set Switches. Must remain as set at factory.	
S1-1 thru S1-6	all OPEN
S1-7	C
S1-8, S1-9	O O
ANALOG/MEMORY ASSEMBLY	
Amplitude and Delay Equalizers.	
S1-1, S1-2	O C
S2-1 thru S2-4	C O O C
Output Power Programming Resistor.	
S1-3	C
Receiver Threshold Level.	
S1-4	O
Transmitter Output Power Level.	
S3-1 thru S3-4	C O C O
Secondary Channel Select.	
S4-1 thru S4-3	O C C
Phone Line Loop-back.	
S4-1	C
4-wire/2-wire Operation.	
wire link, P/R	R

FUNCTION OF SWITCHES (O=OPEN, C=CLOSED)	4-WIRE (LEASED) LINE
SECONDARY CHANNEL	
Receiver threshold S3-1,S3-2	O O
Tx/Rx Interlock Trans. S3-3	O
2-wire,4-wire S3-4	C
Secondary Tx O/P Power Level S2-1 thru S2-9	C00000000
Constant/Controlled Carrier S1-1	C
Secondary channel Enable S1-2	C
Primary channel Enable S1-3	C
Secondary channel Analog Loop-back enable S1-4	O
REMOTE COMMAND ASSEMBLY	
Receive Address. S1-1 thru S1-4	Master O O O O Slave any number
Receiver Input Attenuation. S2-1	O

HP 37210T MODEM (CONTINUED)

FUNCTION OF SWITCHES (C=OPEN, C=CLOSED)	4-WIRE (LEASED) LINE
Remote Command Transmitter Output Level.	
S2-2, S2-3, S2-4	C O O
Address Thumbwheel.	
Front Panel Control	0 (Slave)

Notes:

* Refer to the HP 37210T Operating and Service Manual for the correct switch setting.

** OPEN - The modem has the auto-answer option (003).
CLOSED - The modem does not have auto-answer.

*** With auto-answer, always set to 0 dbm (C O C O).
Without auto-answer, refer to the HP 37210T Operating and Service Manual for the correct setting.

HP 37220T MODEM

The HP 37220T Modem provides full-duplex, synchronous communications via leased lines at transfer rates to 9600 bits per second. The options available (determined by strapping configurations) and recommended for use with the HP 12794A HDLC Modem Interface Kit are:

SWITCH FUNCTION	SWITCH SETTINGS	(O=OPEN, C=CLOSED)
TRANSMITTER STRAPPING		
Factory Set Switches. Must remain as set at factory.	S1-1 S1-8, S1-9 S2-2, S2-3, S2-9	C O O O O O
Request-to-Send/ Clear-to-Send Delay.	S1-2, S1-3, S1-4	C O C
Data-Set-Ready Control.	S1-5, S1-6, S1-7	O O O
Auto-Retain Enable/ Disable.	S2-1	O
Transmit Clock.	S2-4, S2-5, S2-6	O C O
Remote Loop-back Selection.	S2-7, S2-8	O C
Transmit Power Level.	S3-1 thru S3-8	all OPEN
Telephone Line Loop-back Amplifier.	S3-9	O
RECEIVER STRAPPING		
Input Threshold Level.	S1-1, S1-2	C O
Factory Set Switches. Must remain as set at factory.	S1-3 thru S1-6 S1-7, S1-8, S1-9	O O O O C C O
EXTERNAL RATE SELECT VIA THE RS232C/V24 INTERFACE	Jumper Wire	Out (disabled)

HEWLETT PACKARD

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TITLE: 12794A HDLC Modem Interface
Installation and Service Manual

PART NUMBER: 12794-90001

MICROFICHE:

PRINT DATE: 9/80

UPDATE: 1/82

PRINTED IN THE U.S.A.

* *
*   *
* The product related to this manual is no longer in production   *
* at the Hewlett-Packard Corporation. The manual is maintained   *
* on a microfiche master at Direct Marketing Division. As a   *
* service to our customers we are providing a hardcopy print of   *
* the microfiche. The print is produced at Direct Marketing   *
* Division using a TAMERAN 1800-F Autoprint Microfiche Printing   *
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* microfiche to provide maximum flexibility for our customers.   *
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* *

MANUAL UPDATE

MANUAL IDENTIFICATION

Title: HP 12794A HDLC Modem Interface installation and service manual

Part Number: 12794-90001

UPDATE IDENTIFICATION

Update Number: 1

This Update Goes With: First Edition (September 1980)

THE PURPOSE OF THIS MANUAL UPDATE
is to provide new information for your manual to bring it up to date. This is important because it ensures that your manual accurately documents the current version of the product.

THIS UPDATE CONSISTS OF
this cover sheet, a printing history page, all replacement pages, and write-in instructions (if any). Replacement pages are identified by the update number at the bottom of the page. A vertical line (change bar) in the outside margin indicates new or changed text material. The change bar is not used for typographical or editorial changes that do not affect the text.

TO UPDATE YOUR MANUAL
identify the latest update (if any) already contained in your manual by referring to the printing history page. Incorporate only the updates from this packet not already included in your manual. Following the instructions on the back of this page, replace existing pages with the update pages and insert new pages as indicated. If any page is changed in two or more updates, such as the printing history page which is furnished new for each update, only the latest page will be included in the update package. Destroy all replaced pages. If "write-in" instructions are included they are listed on the back of this page.

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TECHNICAL MANUAL UPDATE

(12794-90001)

DESCRIPTION

Title Page/Print History Page:

Replace the title page/print history page provided in this update supplement.

Page 1-2:

In item 3, under Equipment Supplied, change the RS-232-C Modem Cable to part number 5061-4914.

In the description of Option 002, change HP part number 5061-3436 to 5061-4923.

Page 2-5, Table 2-3:

Change the function of switch number 2 to read as follows:

Closed to select *128 byte information field.
Open to select 1024 byte information field.

Page 2-6:

Reverse the order of the switch segment numbers in the first column heading of table 2-4 to read:

"8,7,6"

Change the paragraph enclosed in Figure 2-3 to read as follows:

*These switches are set to select a 1024 byte information field and 1200 bps transmission clock rate. The forced cold load feature is disabled.

Page 2-7:

Change the part number of the Network Manager's Manual, in step 4, to 91750-90010 (Volume 1).

Page 2-8:

Change the part number of the Network Manager's Manual, in step 1, to 91750-90011 (volume 2).

Under Interface Card Configuration Check, note that DSINF senses the presence of a Diagnostic Hood. However, this should not be confused with the Loop-back Verifier Hood, which is the only hood supplied with the HDLC product. DSINF does not sense the loop-back verifier hood.

Page 2-9:

In the last sentence on the page, change the number of the Network Manager's Manual to 91750-90011 (Volume 2).

Page 3-3:

Change the fourth sentence under Frame Check Sequence Field to read as follows:

"...the frame check sequence is computed under Z-80A SIO chip control..."

Page 5-3:

In the second paragraph under Firmware Control, correct the part number of the Network Managers manual to 91750-90010 (volume 1).

Page 5-4:

Delete the phrase from step 3 and step 4 that references the "the hood" being "sensed".

It should be noted that DSINF only senses an installed Diagnostic Hood, not the Loop-back Verifier Hood.

HP 12794A Manual Update

Page 5-5/5-6:

In the last paragraph, correct the part number of the Network Manager's Manual to 91750-90011 (Volume 2).

Page 6-3, Table 6-1:

Change:

U27	1820-2096	9	IC CNTR TTL BIN DUAL 4-BIT	01295	SN74LS393N
U72	1818-1396	4	IC NMOS 16384 (16K) DYN RAM	50088	MK4116N-3
U82	1818-1396	4	IC NMOS 16384 (16K) DYN RAM	50088	MK4116N-3
U92	1818-1396	4	IC NMOS 16384 (16K) DYN RAM	50088	MK4116N-3
U102	1818-1396	4	IC NMOS 16384 (16K) DYN RAM	50088	MK4116N-3
U202	1818-1396	4	IC NMOS 16384 (16K) DYN RAM	50088	MK4116N-3
U302	1818-1396	4	IC NMOS 16384 (16K) DYN RAM	50088	MK4116N-3
U402	1818-1396	4	IC NMOS 16384 (16K) DYN RAM	50088	MK4116N-3
U502	1818-1396	4	IC NMOS 16384 (16K) DYN RAM	50088	MK4116N-3

Add:

XW1	1200-0483	0	SOCKET IC 14-CONT DIP SLDR		
U93	91750-80008		BURN IN 1818-0498	28480	91750-80008
U203	91750-80009		BURN IN 1818-0850	28480	91750-80009

Page 7-4:

Replace Table 7-2 with the table provided in replacement pages 7-3 through 7-6.

Page A-4/A-5:

Correct CUSTOMER OPTIONS as follows:

Option XK is required.
Option YF is required.
Option XM is required.
Option B is recommended.
Option XO is recommended.