HEWLETT hp PACKARD

OPERATING AND SERVICE MANUAL

12924A

CARD READER INTERFACE KIT

(FOR 2100, 2114, 2115, AND 2116 COMPUTERS)

Printed-Circuit Assembly:

12924-60001, Series 1212

Note

This manual should be retained with the applicable computer documentation.

12924-90001

HEWLETT-PACKARD COMPANY
11000 WOLFE ROAD, CUPERTINO, CALIFORNIA, U.S.A.

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1-1. INTRODUCTION.

1-2. This operating and service manual covers general information, installation, programming, theory of operation, maintenance, and replaceable parts for the HP 12924A Card Reader Interface Kit (figure 1-1).

1-3. GENERAL DESCRIPTION.

1-4. The HP 12924A Card Reader Interface Kit provides the necessary equipment to enable using the HP 2892A Card Reader with an HP 2100, 2114, 2115, or 2116 Computer. The kit contains the following items:

a. Card reader interface printed-circuit assembly (PCA), part no. 12924-60001.

b. Cable assembly, part no. 12924-60002.

c. *Operating and Service Manual*, part no. 12924-90001.

1-5. The card reader interface kit uses a printed-circuit assembly with integrated circuits to transfer data and status information between the card reader and the computer. In addition, the interface PCA contains control and interrupt logic circuits that permit programming of the card reader operations using the I/O interrupt or the direct memory access (DMA) method.

1-6. Twelve parallel bits of data are transferred to the computer. Twelve bits of status information are available to monitor operation of the card reader. The first 10 bits are transferred through a 12-bit register on the interface PCA and the remaining two bits are transferred through two separate gate circuits on the PCA.

1-7. IDENTIFICATION.

1-8. Printed-circuit assembly revisions are identified by a revision letter, a series code, and a division code stamped on the board (e.g., A-1024-22). The revision letter identifies the version of the etched trace pattern on the unloaded PCA. The series code (four middle digits) refers to the electrical characteristics of the loaded PCA and the positions of the components. The division code (last two digits) identifies the Hewlett-Packard division that manufactured the PCA. If the series code stamped on the printed-circuit assembly does not agree with the series code shown on the title page of this manual, there are differences between your PCA and the PCA described in this manual. These differences are described in manual supplements available at the nearest HP Sales and Service Office. (Sales and Service Offices are listed at the back of this manual.)

1-9. SPECIFICATIONS.

1-10. Specifications for the card reader interface kit are given in table 1-1.

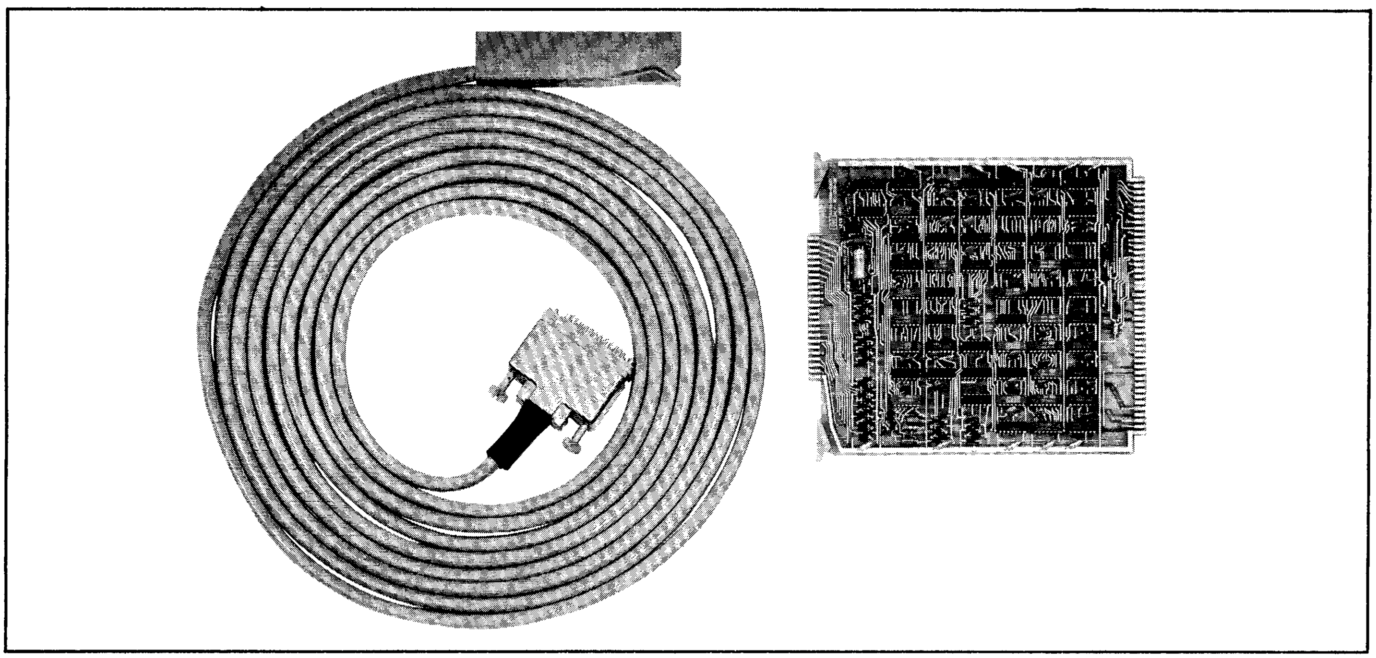

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Figure 1-1. HP 12924A Card Reader Interface Kit

Table 1-1. Interface Kit Specifications

CHARACTERISTICS	SPECIFICATIONS
CURRENT REQUIRED FROM COMPUTER:	
+4.85 Volt Supply:	0.970 ampere
- 2 Volt Supply:	0.43 ampere
DATA TRANSFER:	
Media:	80-column tabular cards per Electronic Industries Standard RS-292.
Rate:	600 cards per minute ± 10 percent.
Code:	Hollerith (12 bits parallel per column, 1 column per character).
LOGIC VOLTAGE LEVELS:	
To and from Computer:	
Logic 1:	+2.4 volts dc (minimum)
Logic 0:	+0.4 volts dc (maximum)
To Card Reader:	
POPIO Signal:	
Logic 1:	+0.4 volts dc (maximum)
Logic 0:	+2.4 volts dc (minimum)
Pick Command Signal:	
Logic 1:	+0.7 volts dc (maximum)
Logic 0:	+4.0 volts dc (minimum)
From Card Reader:	
Logic 1:	+0.25 volts dc (maximum)
Logic 0:	+4.5 volts dc (minimum)

SECTION II

INSTALLATION AND PROGRAMMING

2-1. INTRODUCTION.

2-2. This section provides information on unpacking, inspection, installation, reshipment, and programming for the HP 12924A Card Reader Interface Kit.

2-3. UNPACKING AND INSPECTION.

2-4. If the shipping carton is damaged upon receipt, request that the carrier's agent be present when the kit is unpacked. Inspect the kit for damage (cracks, broken parts, etc.). If the kit is damaged and fails to meet specifications, notify the carrier and the nearest Hewlett-Packard Sales and Service Office immediately. (Sales and Service Offices are listed at the back of this manual.) Retain the shipping container and the packing material for the carrier's inspection. The Hewlett-Packard Sales and Service Office will arrange for the repair or replacement of the damaged kit without waiting for any claims against the carrier to be settled.

2-5. INSTALLATION.

2-6. Install the interface PCA and cable assembly as follows:

a. Determine if the computer power supplies will provide the additional current required for operation of the interface PCA. Refer to the Hewlett-Packard computer documentation for a listing of current available from the computer power supplies.

b. Turn off computer and card reader power.

CAUTION

Computer power must be off before installing the interface kit, or damage to the computer may result.

c. Open computer for access to I/O PCA slots.

Note: The card reader requires a high priority I/O slot in the computer. In most systems, devices with a data transfer rate of 1000 16-bit words per second or faster are the only devices that should be placed in a higher priority slot.

d. Plug interface PCA into the I/O slot assigned for the particular computer system. Make certain that all higher priority slots have either another I/O PCA or a priority jumper PCA installed.

e. Pass the interface PCA connector of the cable assembly through opening at rear of computer. Slide connector onto interface PCA and close computer.

f. Connect other end of cable assembly to the mating connector at the rear of the card reader.

g. Run diagnostic test as described in the Diagnostic Program Procedure, part number 02892-90006, contained in the *Manual of Diagnostics* to verify that the interface PCA is functioning properly.

2-7. RESHIPMENT.

2-8. If an item of the kit is to be shipped to Hewlett-Packard for service or repair, attach a tag to the item identifying the owner and indicating the service or repair to be accomplished. Include the accessory number of the kit.

2-9. Package the item in the original factory packaging material, if available. If the original material is not available, standard factory packaging material can be obtained from a local Hewlett-Packard Sales and Service Office.

2-10. If standard factory packaging material is not used, wrap the item in Air Cap TH-240 Cushioning (or equivalent) manufactured by Sealed Air Corp., Hawthorne, N.J., and place in a corrugated carton (200 pound test material). Seal the shipping carton securely and mark it "FRAGILE" to ensure careful handling.

Note: In any correspondence, identify the kit by accessory number. Refer any questions to the nearest Hewlett-Packard Sales and Service Office.

2-11. PROGRAMMING.

2-12. The following paragraphs provide information for programming the card reader interface PCA and card reader. This information consists of the card reader characteristics, and status and timing considerations. Additional programming information is available in the software manuals provided with the computer.

2-13. CARD READER CHARACTERISTICS.

2-14. The card reader reads up to 600 punched cards per minute at 60 Hz or 50 Hz. Each card contains 80 columns of data. Columns are arranged in 12 rows to represent a 12-bit Hollerith-coded character. Card reading is enabled by a "not" Pick Command signal from the computer and continues as long as cards are in the hopper and the command is available. A card reading sequence starts when a card is picked from the input hopper and committed to the read station. The card then moves through the read station without stopping, and all 80 Hollerith-coded characters are read out at a constant rate. These characters are transferred from the card reader data storage register to the interface card one column at a time. An automatic stop occurs if a device error is detected in the card reader operation. The cause of the error is displayed on the card reader control panel and relayed to the computer for program control through the status circuitry. To continue operation after an error indication, press the card reader RESET switch after the cause of the error has been corrected.

2-15. STATUS SIGNALS.

2-16. The card reader supplies eight status signals that are sent to the interface PCA. In addition, five status signals are developed by the interface PCA. These signals appear as bits 0 through 3, 5 through 9, 11, 12, and 15 of each status word transferred from the interface PAC to the computer (bits 4, 10, 13, and 14 are unused). To determine the card reader status, the signals for bits 0 through 3, 5 through 9, and 11 of the status word are first loaded into the interface PCA data register. Then, the full 14-bit (bits 0 through 11, 12, and 15) word is transferred to the computer register by an LIA or LIB instruction and the card reader select code. The signals for bits 12 and 15 are transferred through the interface PCA output gates whenever a load instruction is programmed with a card reader select code. Bits 0 through 11 are loaded into the interface PCA data register by one of the following four methods:

a. An OTA, or OTB instruction (I/O output instruction) is programmed with the card reader select code.

b. An end-of-operation (EOP) interrupt occurs.

c. Computer power turn-on or preset occurs.

2-17. Bits 0 through 11 of the status word remain loaded in the interface PCA data register until one of the following three conditions occur:

a. The status word is replaced with a new status word by one of the four methods listed in paragraph 2-16.

b. The next card is picked to pass through the card reader read station.

c. An LIA/LIB or MIA/MIB instruction is programmed with the card reader select code to transfer the status information to the computer. This allows the next data word to replace the status word in the interface PCA register when a "not" Index Mark signal is received from the card reader.

2-18. Table 2-1 lists the status signals by name and bit position, and also lists the logic indications at the interface PCA output pins.

2-19. TIMING.

2-20. Card reader operation is synchronized through "not" Pick Command and "not" Index Mark signals. These signals, and all other signals routed between the card reader and the interface PCA, are ground-true at the card reader. The "not" Pick Command signal is initiated on the interface PCA and sent to the card reader when the computer is ready to accept data. This is done for each card to be read. If the card reader is on-line and ready to read cards, it responds to the "not" Pick Command signal by starting a card through the card reader read station. Once a card is started (picked), it continues through the read station at a constant speed. As the card passes through the read station, the reader generates a "not" Index Mark signal. The "not" Index Mark signal is a pulse that occurs as each data column of the card passes through the read station. Therefore, each card causes 80 "not" Index Mark signals to be generated. These pulses are sent to the interface PCA to synchronize the transfer of each data column from the card reader with the interface PCA signals.

2-21. Figure 2-1 is a timing diagram showing the timing of a card reading sequence. A card reading sequence is initiated by a Set Control, Clear Flag (STC,C) instruction. If the card reader is on-line and ready to read, the STC portion of the instruction causes the "not" Pick Command signal to go low and also causes the Data signal from the Status/Data FF to go high. When the first card column enters the read station, the "not" Index Mark signal is sent to the interface PCA, causing the "not" Pick Command signal to go high. The "not" Pick signal then remains high until the next STC instruction. The "not" Index Mark signal is gated with the Data signal to enable the interface PCA data register. An input signal from each data row on the punched card is also gated with the Data signal. These gated inputs are then loaded into the enabled register. The "not" Index Mark signal strobes each data column successively into the interface PCA data register.

2-22. To transfer a column of data from the interface PCA data register to the computer, a load instruction such as LIA, LIB, MIA, or MIB (I/O input instruction) is required. The load instruction generates the IOI signal that is sent to the interface PCA. This IOI signal enables the interface PCA output gates so that data is transferred through the gates to the computer. To prevent loss of data, each column of data must be transferred to the computer before the next column of data is loaded into the interface PCA data register.

2-23. The "not" Index Mark signal also causes the Flag signal to go high and the IOI signal causes the Flag signal to go low. The high Flag signal initiates a Request for Service (SRQ) signal and also enables the interface PCA interrupt circuits. If conditions are met for the computer to accept data from the card reader, the computer enables the data transfer and causes the Flag signal to go low. Three methods are available to meet the computer requirements for data transfer. The three methods are discussed in the following paragraphs.

Table 2-1. Card Reader Status Signals

BIT	STATUS SIGNAL	LOGIC
0	"not" Ready or Off-Line or Busy	Logic 1 indicates card reader is on-line and is ready to send data. Logic 0 indicates card reader is not on-line or not ready to send data.
1	Trouble During Read	Logic 1 indicates that one or more of the following troubles occurred: a. Card motion error. b. Light/Dark error. c. Data loss. Logic 0 indicates that no trouble indication occurred.
2	Off-Line	Logic 1 indicates that the card reader is operating in the off-line mode. Logic 0 indicates that the card reader is not operating in the off-line mode.
3	Data Lost	Logic 1 indicates that data was lost due to one of the following conditions: a. A data word was loaded into the interface PCA register by an STC instruction but was not transferred to the computer by an LIA or LIB instruction before the next "not" Data Strobe signal was received from the card reader. b. A data word was contained in the interface PCA register when the EOP signal went high or an OTA or OTB instruction was issued. c. A status word was loaded into the interface PCA register by an OTA or OTB instruction but was not transferred to the computer by an LIA or LIB instruction before the next "not" Data Strobe signal was received from the card reader. Logic 0 indicates that no data was lost due to a timing error.
4	Not used	
5	Hopper Empty or Stacker Full	Logic 1 indicates that the card reader hopper is empty or the stacker is full. Logic 0 indicates that the hopper is not empty and the stacker is not full.
6	Stacker Full	Logic 1 indicates that the card reader stacker is full. Logic 0 indicates that the stacker will accept cards.
7	End-of-File and Hopper Empty	Logic 1 indicates that the card reader End-of-File signal was high and the hopper is empty. Logic 0 indicates that the End-of-File signal was low or there is a card in the hopper.
8	Pick	Logic 1 indicates that the card reader is not in the off-line mode, the first data column has not been read, and an STC instruction was issued with the card reader select code. Logic 0 indicates that one of the following condition has occurred: a. Card reader sent "not" Index Mark signal to interface PCA. b. An EOP interrupt occurred. c. Card reader was in off-line mode. d. Computer power turn-on or preset occurred. e. A CLC instruction was issued with the card reader select code.
9	"not" Error (L/D)	Logic 1 indicates the card reader detected a leading edge dark check or trailing edge dark check or light check. Logic 0 indicates that all read station photocells were functioning before and after a card was read.
10	Not used	
11	Motion/Pick Check	Logic 1 indicates that the last card failed to move from the card reader read station to the stacker station or was not picked from the input hopper. Logic 0 indicates normal card motion.

Table 2-1. Card Reader Status Signals (Continued)

BIT	STATUS SIGNAL	LOGIC
12	"not" Read In Progress	Logic 1 indicates that computer power turn-on, computer preset, or an EOP interrupt has occurred. Logic 0 indicates the card reader was on-line and ready and the Pick signal went high.
13	Not used	
14	Not used	
15	End of Operation	Logic 1 indicates that one of the following conditions has occurred: a. Computer power turn-on or preset. b. Pick signal was high when reader was switched to off-line mode. c. Card reader was on-line and ready but Pick signal did not go high. d. Card reader went to ready mode at end of card reading sequence. Status is now contained in data-register. e. Card reader failed to read a card within 875 ± 150 milliseconds after the Pick signal went high. Logic 0 indicates that no end-of-operation (EOP) interrupt has occurred.

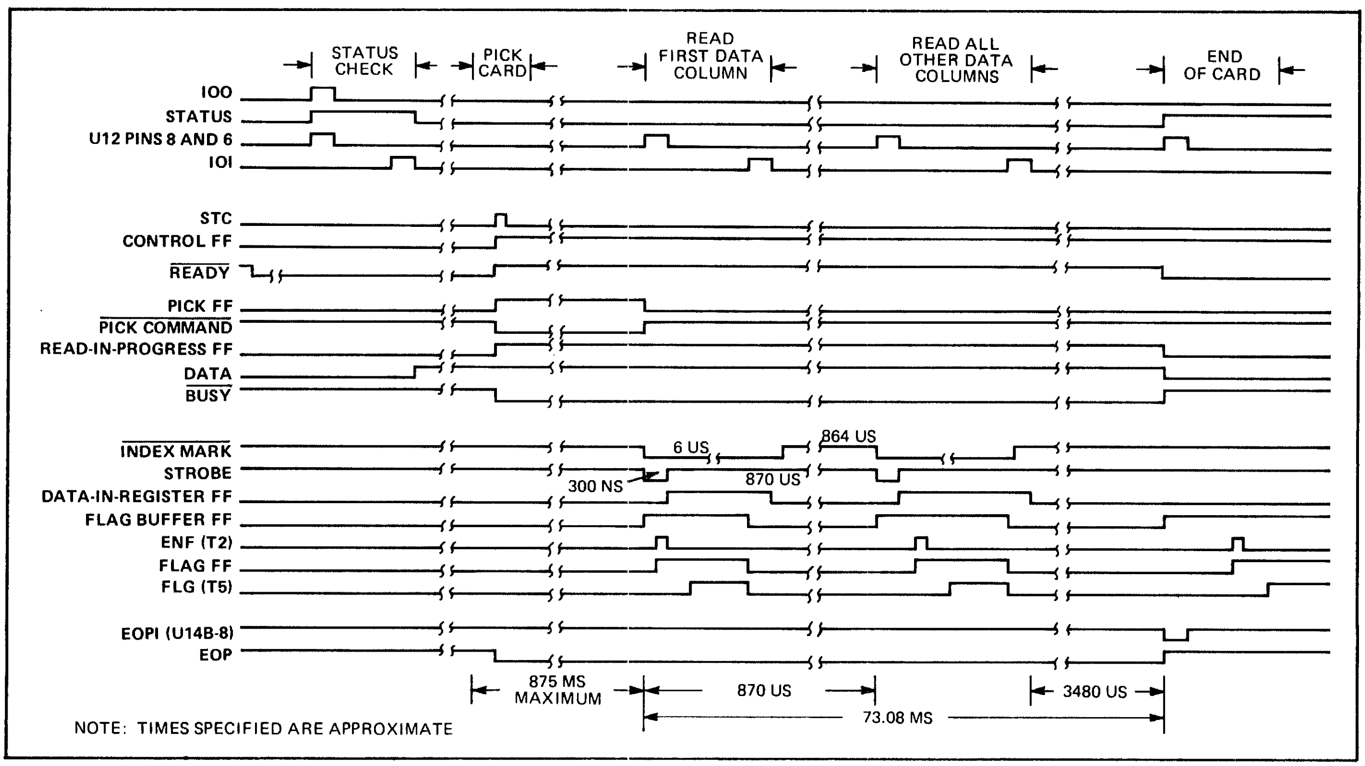

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Figure 2-1. Card Reader Interface Timing Diagram

2-24. NON-INTERRUPT. The non-interrupt method is the simplest method of programming the card reader. With this method the computer is held in a program loop by a skip flag instruction until all 80 columns of data have been transferred to the computer memory. Thus, the computer central processor is caused to wait a few milliseconds (normally 1.25 milliseconds) between each transfer of data while the card reader is getting the data ready for transfer. This is the most inefficient method of data transfer and computer time utilization.

2-25. INTERRUPT. The interrupt method allows the computer to service other I/O devices on a priority basis between each card column data transfer. This provides more efficient use of computer time but may cause data to be lost if the computer fails to service each column of data at the proper time.

2-26. DIRECT MEMORY ACCESS. Direct memory access (DMA) provides increased speed in handling the transfer of data from the card reader to the computer. When transferring data under DMA control, the computer central processor operation is frozen, the 80 columns of data are transferred directly to the computer memory, then the computer central processor resumes operation as though no interruption had occurred. This is the most efficient method of data transfer for high speed devices.

THEORY OF OPERATION SECTION III

3-1. INTRODUCTION.

3-2. This section contains a functional description and a detailed circuit description of the card reader interface PCA. Also included at the back of this section is an operational flow diagram (figure 3-3) of the interface PCA.

3-3. FUNCTIONAL DESCRIPTION.

3-4. The card reader interface PCA contains a 12-bit data register and the necessary control circuitry to transfer data and status information from the card reader to the computer. All functions of the interface PCA are performed under the control of programmed instructions and result in data being read from punched cards and stored in the computer. (See figure 3-1.) Initial operating conditions for the interface PCA are established when the POPIO signal and CRS signal are received from the computer. The POPIO signal is generated by the computer when power is turned on. The CRS signal is generated by the computer when the PRESET switch is pressed. The POPIO signal is also inverted and sent to the card reader as the "not" EOF Clear signal to clear the End-of-File FF.

3-5. Programmed instructions initiate the control signals that are sent from the computer to the interface PCA, controlling the card reader and the data transferring process. If the status signals from the card reader indicate that the card reader is on-line, ready to read cards, and not in the process of reading a card, the control signals from the computer cause the interface PCA to generate a "not" Pick Command signal. This signal causes the card reader to pick the bottom card from the input hopper and start it through the read station. Once a card is started along the read path, it automatically continues through the read station to the output stacker without interruption. If a malfunction has occurred during the card's progress through the read path, it will be sensed by the error circuitry of the card reader causing the card reader to halt after the card is in the output stacker. The error condition is sent to the interface PCA and will be registered in the next status word sent to the computer. A "not" Pick Command signal is required to pick each card and start it through the read station. A status word is sent to the computer by the card reader interface after each card is read.

3-6. Data is read from each punched card as the card passes through the read station. On the punched cards, data is arranged in 80 columns and 12 rows. Each column of 12 rows represents one character (computer word) and each row represents one bit of the character. As each column of data enters the read station, the 12 data bits are stored in the card reader character buffer the outputs of which are impressed on the interface PCA data input lines. When the character buffer output lines have become stable, the card reader generates a "not" Index Mark signal that is sent to the interface PCA. The "not" Index Mark signal enables the interface PCA data register, causing the 12 data bits to be loaded into the data register. This 12-bit data word is then transferred from the interface PCA data register to the computer before the next data word is ready to be loaded into the interface PCA data register.

3-7. A low "not" Index Mark signal also results in a Skip on Flag (SKF), Interrupt Request (IRQ), or Service Request (SRQ) signal, depending upon the programmed method of transferring data from the interface PCA to the computer. Any one of these signals condition the computer for data transfer. To complete the data transfer, a load instruction such as LIA, LIB, MIA or MIB (I/O input instruction) must be programmed for each data word (80 per card). When these instructions are used with normal software driver programs, each 12-bit character is converted to an equivalent 8-bit ASCII coded character. Two eight-bit characters can then be placed in one computer location. This process is referred to as character packing.

3-8. Operation of the card reader is monitored by eight "not" status signals (Busy, Off-Line, Ready, Hopper Empty, Stacker Full, End-of-File, Error L/D, and Motion/Pick Check) that are routed to the interface PCA. Five additional status signals ("not" Read-in-Progress, Lost Data, Pick, End-of-Operation, and Trouble During Read) are developed on the interface PCA to monitor the interface PCA operation. Eleven of these signals are routed to the status input gates of the interface PCA data register. When the status input gates are enabled by an OTA or OTB instruction (I/O output instruction), the status signals are loaded into the data register and the data inputs are inhibited until the status word is transferred to the computer. Status information is transferred from the interface PCA to the computer by an I/O input instruction. Two status bits, bits 12 and 15, are not routed through the data register but are transferred to the computer whenever an I/O input instruction is processed (during data or status transfers).

3-9. DETAILED CIRCUIT DESCRIPTION.

3-10. The card reader interface PCA uses integrated circuits with positive-true logic. A logic diagram and parts location diagram for the interface PCA are provided in figure 4-1. Individual diagrams for the integrated circuits are provided in figure 4-2. To describe operation of the interface PCA circuits, the circuits are divided into the following functional groups:

a. Turn-On and Preset.

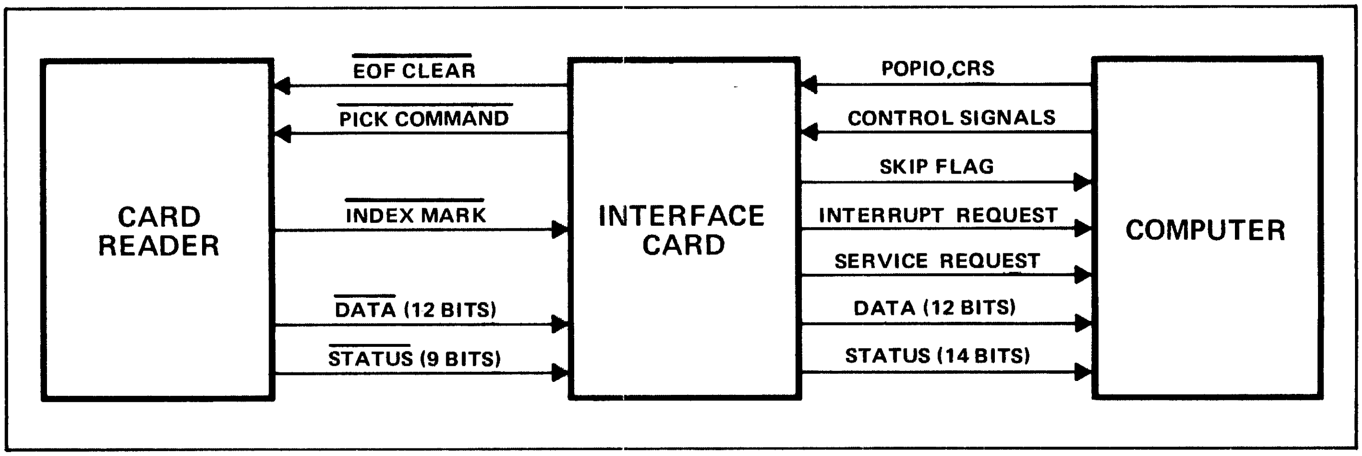

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Figure 3-1. Card Reader Interface Signal Flow, Block Diagram

b. Select Code Detector.

c. Pick Command.

d. End-of-Operation

e. Status/Data.

f. Lost Data.

g. Status Signal.

h. Data Register. (Refer to paragraphs 3-13 and 3-25 through 3-27.)

3-11. TURN-ON AND PRESET CIRCUIT.

3-12. The turn-on and preset circuit establishes the initial conditions for the interface PCA logic circuits and clears the End-of-File FF in the card reader. When the computer power is turned on or when the computer PRESET switch is pressed, the computer sends POPIO and CRS signals to the interface PCA. The POPIO signal sets the Flag Buffer FF, which enables the Flag FF and causes it to be set at the next I/O time T2 with the ENF signal. Also, the POPIO signal is inverted by gate U73A and routed to the card reader as the "not" EOF Clear signal where it clears the End-of-File FF. The End-of-File FF generates the status signal ("not" EOF) which is routed back to the interface PCA.

3-13. The CRS signal causes the data register to be cleared and initiates a status check by first clearing the Control, Pick, Read-In-Progress, Lost Data, and Data-In-Register FFs, and then setting the EOP and Status/Data FFs. When the Status/Data FF sets, status bits 0 through 11 are gated to the data register set inputs. The CRS signal is then routed through gates U12A and U12B to the clock inputs of the register. This enables the data register and loads it with the current status information. If the status word is subsequently transferred to computer memory by an I/O input instruction, status bits 12 and 15 must be logic 1s and bit 3 must be logic 0, indicating no read is in progress, the interface is currently in the end-of-operation status, and no data has been lost. All other bits depend upon the current status of the card reader.

3-14. SELECT CODE DETECTOR CIRCUIT.

3-15. The select code circuit enables the card reader interface PCA control circuits. When the card reader is addressed by the instruction being processed by the computer, the SCM and SCL signals become high at the interface PCA. Since any instruction referencing an external device is in the computer I/O group instruction set, the IOG signal is also high at the interface PCA. These three signals being high enable the control circuits on the interface PCA in such a way as to allow the instruction being processed to activate the necessary interface circuits, thus completing the instruction. The select code necessary to address a certain interface PCA and I/O device is determined by the physical location of the interface PCA within the I/O section of the computer.

3-16. INTERRUPT CIRCUIT.

3-17. Computer operation is interrupted by the interrupt circuit on a priority basis. During the interrupt, data is transferred to computer memory by the card reader. The interrupt circuit consists of IRQ FF (U24A and U24B) and associated circuits. Initial conditions are established when the Flag FF (U25A and U35A) and Control FF (U24C and U34B) are set and an IEN signal is received to enable gate U35B. An IEN signal is received when an STF instruction is programmed with select code 00. The low output of gate U35B is inverted and applied to gate U14A with the SIR signal (T5) from gate U26C, a signal from the Flag Buffer FF (U15A and U15B), and the PRH signal. The PRH signal indicates that there are no higher priority devices requesting an interrupt. The low output of gate U35B causes the output of gate U17B to go low, sending a low PRL signal to all lower priority device interface PCAs. The PRL signal inhibits all lower priority interface PCAs from interrupting the card reader. If all inputs to gate U14A are high, the output is low, setting the IRQ FF, providing the FLG and IRQ signals to the computer to initiate an interrupt.

3-18. At the next T2 time, the ENF signal clears the IRQ FF to allow any higher priority device to request service during the interrupt. If no higher priority device requests service the PRH signal remains high, as do the other inputs to gate U14A, and at time T5, the SIR signal sets the IRQ FF a second time. The FLG and IRQ signals are then used to indicate the interrupt address.

3-19. The computer sends an IAK signal to the interface PCA to clear the Flag Buffer FF and executes the instruction contained in memory at the interrupt address. At time T2, the ENF signal clears the IRQ FF. Clearing the Flag Buffer FF prevents the IRQ FF from being set again after the requested interrupt is enabled. The Flag FF remains set, however, to maintain the low PRL signal to lower priority devices until processing of the requested interrupt is complete. To clear the Flag FF and enable lower priority devices, a CLF instruction must be programmed.

3-20. PICK COMMAND CIRCUIT.

3-21. The pick command circuit generates the "not" Pick Command signal that starts the punched card through the card reader read station. This circuit includes the Pick and Read-In-Progress FFs and transistor Q1 and uses the "not" Index Mark, "not" Ready, and "not" Off-Line signal inputs from the card reader and the PON signal input from the computer.

3-22. The Pick FF is set by an STC instruction if the card reader is on-line but is not in the process of reading a card. (See figure 3-3.) When the card reader is in the ready condition, the Ready · "not" Off-Line · "not" Busy signal and the set side of the Pick FF combine to set the Read-In-Progress FF. The set-side outputs from the Pick and Read-In-Progress FFs are then combined at U73B to provide a ground potential at the emitter of transistor Q1. Q1 is an NPN transistor with a positive potential on its base via the PON signal which is high as long as computer power is turned on. Ground potential on the emitter and a positive potential on the base of Q1 causes Q1 to conduct so that a low "not" Pick Command signal is sent to the card reader.

3-23. The low "not" Pick Command signal causes the card reader to pick a card and start it through the read station. When the first character has been read and is in the character buffer of the card reader, the card reader sends a low (ground) "not" Index Mark signal to the interface PCA. When the "not" Index Mark signal goes low, pin 11 of gate U44C goes high and pin 10 remains high until capacitor C16 discharges. Since pin 9 of gate U44C is high when the Read-In-Progress FF is set, the "not" Index Mark signal transition from high to low causes a 300-nanosecond negative-going pulse (Strobe signal) to be generated at the output pin 8 of gate U44C. This Strobe signal is used to generate the clock input signal to the interface PCA data register and also clears the Pick FF. Clearing the Pick FF causes the "not" Pick Command signal to go high and conditions the interface PCA for the next STC instruction.

3-24. The Pick FF is also cleared if the card reader is placed in the off-line mode or if a CLC instruction is processed by the computer. Both the Pick and Read-In-Progress FFs are cleared by a CRS signal or an end-of-operation interrupt. An end-of-operation interrupt normally occurs as each card leaves the read station and the card reader becomes not busy.

3-25. END-OF-OPERATION CIRCUIT.

3-26. The end-of-operation circuit generates the End-of-Operation Interrupt (EOPI) signal and the End-of-Operation (EOP) status signal. This circuit includes the Pick Time-Out Delay one-shot, the EOP FF, and the Read-In-Progress FF, and is controlled by the pick command circuits and the "not" Busy signal from the card reader. A normal End-of-Operation Interrupt signal is generated as each card leaves the card reader read station. Gate U14B generates this normal interrupt signal as follows: A high signal is applied to U14B, pins 9 and 12, when the Pick FF is cleared by the Strobe signal. While the card is being read, a high signal is applied to U14B, pin 13. When the card leaves the read station and the card reader becomes not busy, a high signal is applied to U14B, pin 10, and the signal at pin 13 remains high until capacitor C18 discharges. This provides a 300-nanosecond negative-going pulse at output pin 8 of U14B. The negative-going pulse causes the output of U52 to go high, resulting in setting the End-of-Operation FF.

3-27. An EOPI signal is also generated by either of two malfunctions. Gate U32A causes an EOPI signal to be generated if the card reader is placed in the off-line mode when the Pick FF is set. Also, the Pick Time-Out Delay one-shot causes an EOPI signal to be generated if a normal EOPI signal does not occur within 875 ± 150 milliseconds after the Read-In-Progress FF was set. This 875-millisecond delay time is greater than the time required to read a card; therefore, the Read-In-Progress FF would normally be cleared before the delay one-shot has timed-out. Each time the Read-In-Progress FF is set, the Pick Time-Out Delay one-shot is set for the 875-millisecond time delay. If a pick fail occurs, the Read-In-Progress FF does not get cleared and the time delay expires. A high signal is then applied to U32D, pin 9. Since pin 10 of U32D is high due to the Read-In-Progress FF being set, U32D provides a low output at pin 8. The low output at pin 8 causes the EOPI signal to be generated, clearing the Read-In-Progress FF. Pin 8 of U32D remains low for 300 nanoseconds after the clearing of the Read-In-Progress FF, due to the discharging of capacitor C5 through resistor R3.

3-28. Whenever an end-of-operation interrupt occurs, the low output from U45A causes the following actions:

a. The EOP FF is set to provide a logic 1 at IOBI 15.

b. The Pick and Read-In-Progress FFs are cleared.

c. The Lost Data FF is set if there was data in the register.

d. The Status/Data FF is set to enable the status input gates to the data register.

e. The data register clock input is enabled to load the current status word in the data register.

f. If the Flag FF was cleared, the Flag Buffer FF is set and the Flag FF is set at the next time T2 by the ENF signal.

3-29. STATUS/DATA CIRCUIT

3-30. The status/data circuit selects either status information or data for loading into the interface PCA data register. This circuit includes the Status/Data FF and is controlled by programmed I/O instructions from the computer, the EOPI signal, and the CRS signal from the computer PRESET switch. To load status information into the data register, an I/O output instruction is processed by the computer. The computer then develops an IOO signal that is sent to the interface PCA to set the Status/Data FF, thus generating the Status signal. The Status signal gates the status information from the card reader to the input of the interface PCA data register. When the Status signal is generated, the Enable 1 and Enable 2 signals are also generated by the IOO signal. The Enable signals clock the status information into the data register. An I/O input instruction must now be processed by the computer in order to transfer the information in the data register to the computer. The EOPI signal causes the Status signal to be generated at the end of each card as the card passes through the card reader read station. Also, when the preset switch on the computer is pressed, the Status signal is generated.

3-31. The STC signal from the computer causes the Status/Data FF to generate the Data signal when a data word is to be transferred from the card reader to the interface PCA data register. At the same time the Data signal is generated, the Pick FF is set and the Data-In-Register FF is cleared as long as the card reader is not in the Off-Line mode or the Read-In-Progress FF is set. A true IOI signal is received from the computer whenever an I/O input instruction such as LIA or LIB is processed by the computer. The IOI signal enables the interface PCA output gates and applies a high signal to pin 9 of U21D. When the IOI signal subsequently goes low, pin 10 of U21D goes high and pin 9 remains high until capacitor C3 discharges. This causes a 50-nanosecond negative-going output pulse from U21D that causes the Status/Data FF to generate the Data signal that gates the data from the card reader to the input of the interface PCA data register.

3-32. LOST DATA CIRCUIT.

3-33. The lost data circuit causes a lost data indication to be generated when status or data transfers are not programmed and processed in the proper order. The circuit includes the Data-In-Register FF and the Lost Data FF. The Data-In-Register FF and the Lost Data FF are cleared by the same signal that sets the Pick FF or by the CRS signal, if the computer preset switch is pressed. This ensures that both flip-flops are clear as each card starts through the read station. The set and clear inputs to the Data-In-Register FF are both tied to +4.85V so that the flip-flop changes state each time the clock goes through a high-to-low transition. This transition occurs at the trailing edge of the Strobe signal from gate U45D if the Data-In-Register FF is clear, or at the trailing edge of the IOI signal if the Data-In-Register FF is set. A Strobe signal is required to enable the data register. Therefore, the Data-In-Register FF is set each time the data register is loaded with a data word. An IOI signal is required to transfer the data register contents from the data register to the computer. So, the Data-In-Register FF is cleared each time a transfer has occurred. When the Data-In-Register FF is set, indicating that there is a data word in the data register, the high set-side output is applied to gates U33A and U23B. All the input signals to gate U33A being high cause the output to go low. The low output from gate U33A clears both the Flag Buffer FF and Flag FF. If an EOPI signal is generated or an I/O output instruction is processed to load a status word into the data register, while the Data-In-Register FF is set, the output of U23B will go low. This low output from gate U23B sets the Lost Data FF, indicating that the status information being sent to the computer is invalid. If the Data-In-Register FF is set or the Data signal is low, the "not" IOI signal is low at the time that the Strobe signal is low (indicating a data word is being transferred from the card reader), a low output will be generated at the output of gate U23D. This will set the Lost Data FF, indicating that the data word being sent to the computer is invalid. These conditions cause the Lost Data signal to be generated which provides a logic 1 at data register bit 3 (IOBI 3) during the status checking process.

3-34. STATUS SIGNAL CIRCUITS.

3-35. The status signal circuits condition the card reader status signals and develop the interface PCA status signals. Eight status signals are received from the card reader and five status signals (including the Lost Data signal explained in paragraph 3-28) are developed by the interface PCA. The relative bit positions of these status signals are shown in figure 3-2. All status signals coming from the card reader are first inverted by the status signal circuits and then routed to the status input gates of the data register. The "not" Hopper Empty signal, which indicates when the last card has been taken from the input hopper, is combined with the "not" Stacker Full signal, which indicates that the output stacker is carrying the maximum number of cards it can hold to provide status bit 5. The "not" Hopper Empty signal is also combined with the "not" End-of-File signal, which indicates that the end-of-file switch on the card reader has been pressed, to provide bit 7. The "not" Motion/Pick Check signal, which indicates that a card has not been stacked in the output stacker within the allotted length of time or that the card has not been picked from the input hopper after six attempts have been made, provides bit 11. The "not" Off-Line signal, which indicates that the OFF-LINE/ON-LINE switch on the card reader is

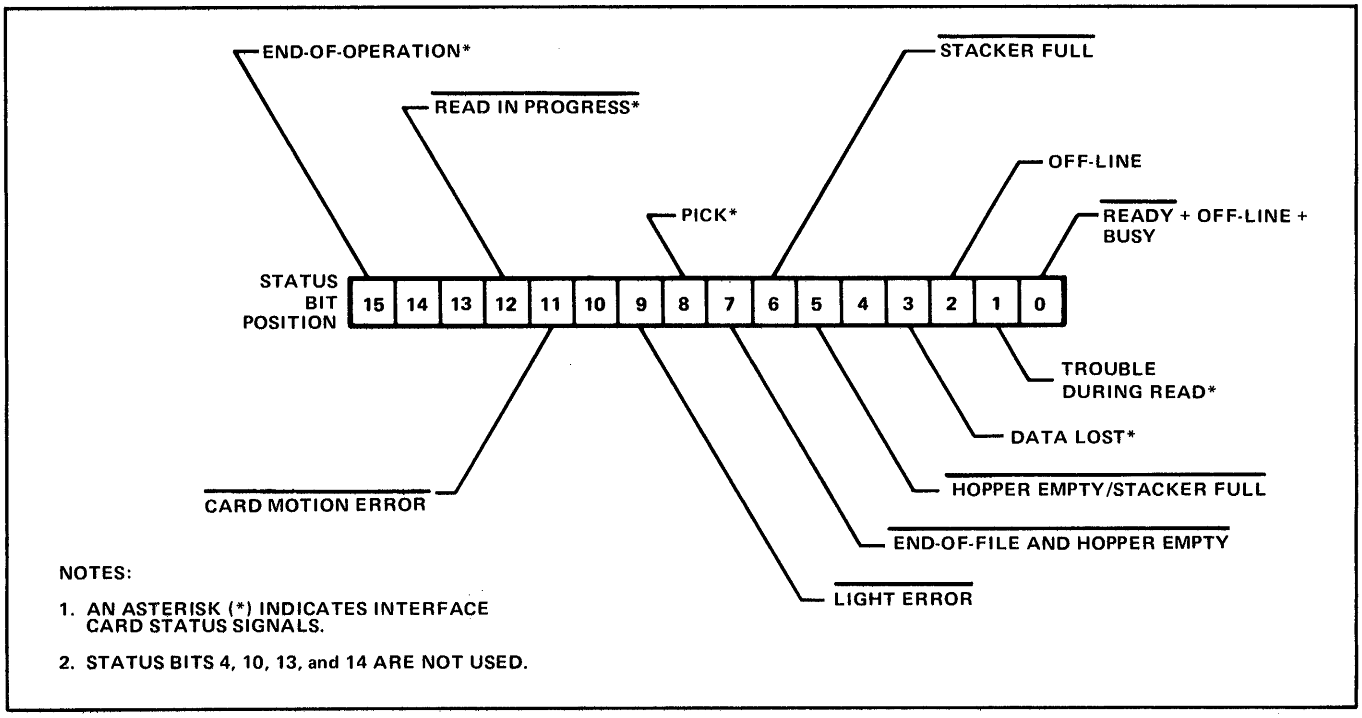
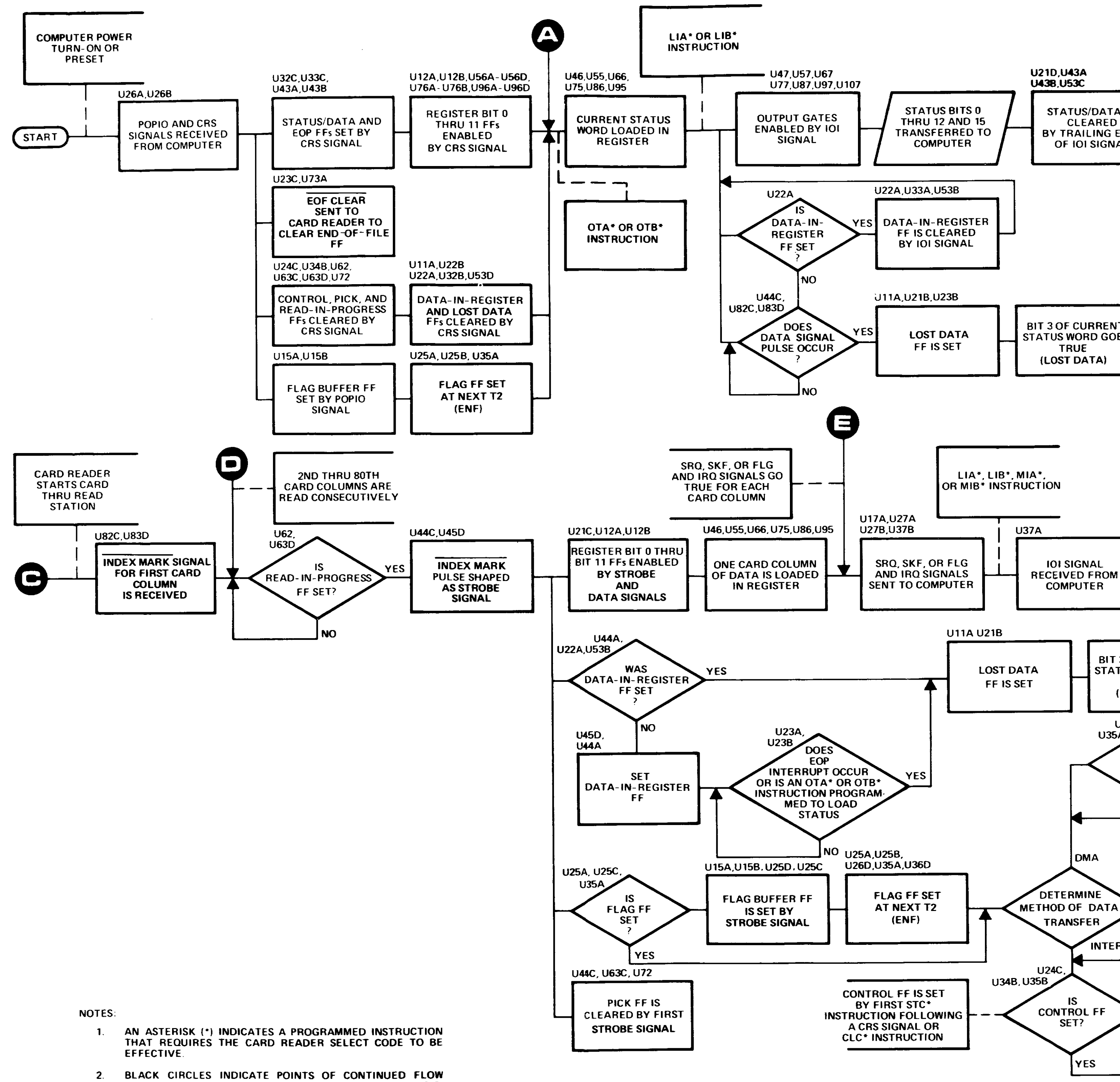


Figure 3-2. Card Reader and Interface PCA Status Signals

in the OFF-LINE position, provides bit 2. The "not" Ready signal, which indicates that the card reader circuitry is in the proper state to start processing cards, is combined with the "not" Off-Line signal and the "not" Busy signal, which indicates that the card reader is currently processing a card, provides status bit 0. Bit 0 will be high if the card reader is either not ready, busy, or off-line. The "not" Light Error signal, which indicates that the light sensors of the card reader read station are functioning properly, provides status bit 9.



NOTES:

1. AN ASTERISK (*) INDICATES A PROGRAMMED INSTRUCTION THAT REQUIRES THE CARD READER SELECT CODE TO BE EFFECTIVE.
2. BLACK CIRCLES INDICATE POINTS OF CONTINUED FLOW FROM ALL OPEN CIRCLES WITH THE SAME LETTER DESIGNATION.

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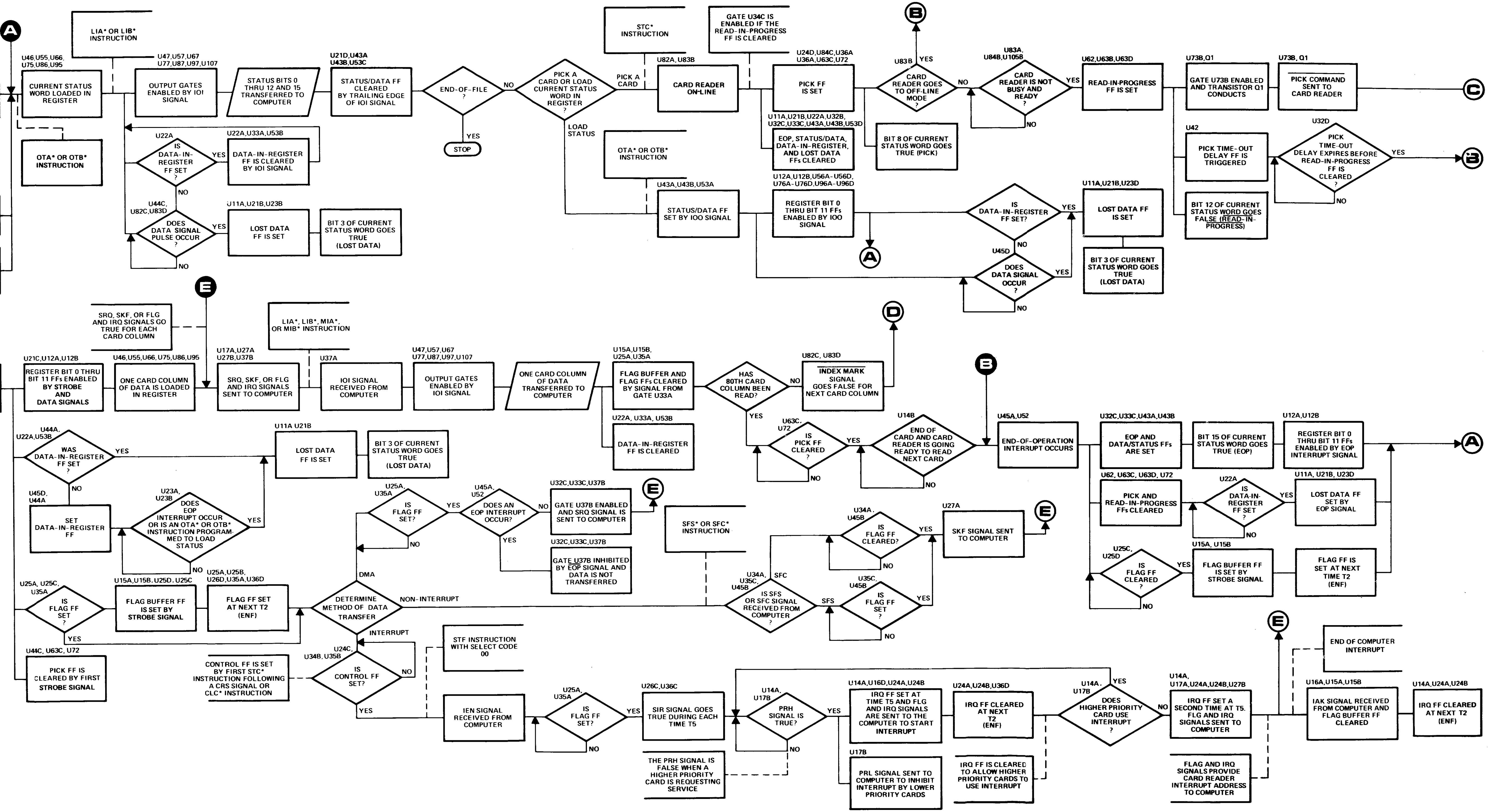

Figure 3-3. Operational Flow Diagram

4-1. INTRODUCTION.

4-2. This section contains information on diagnostics and troubleshooting for the card reader interface kit.

4-3. PREVENTIVE MAINTENANCE.

4-4. Detailed preventive maintenance procedures and schedules are provided in the applicable Hewlett-Packard computer documentation. There are no separate preventive maintenance procedures to be performed on the interface kit.

4-5. DIAGNOSTICS.

4-6. The interface PCA may be checked using the Diagnostic Program Procedures, part no. 02892-90006, contained in the *Manual of Diagnostics*. The diagnostic will check all of the status and data circuits on the interface card. This diagnostic test requires that the card reader be connected in the normal operating configuration.

4-7. TROUBLESHOOTING.

4-8 Troubleshooting for the interface PCA is accomplished by performing the tests in the diagnostic program and analyzing any error halts that occur as the test is being run. Continuity checks of the interconnecting cable are performed by using table 4-1. To further isolate the trouble, refer to the schematic diagram and parts location view in figure 4-1. Table 4-2 contains a parts list for the interface PCA with the parts listed in alphanumeric order by reference designation. Logic and pin location diagrams for the integrated circuits used on the interface PCA are contained in figure 4-2. Table 4-3 gives the integrated circuit input levels, output levels, and delay times which correspond to the integrated circuit characteristic number shown below each diagram in figure 4-2.

Table 4-1. Cable Assembly Connector Pin Assignments

48-Pin Connector	50-Pin Connector	Signal Name	Card Reader Signal Mnemonic
1	A	Data Column 12	"not" D12
2	B	Data Column 11	"not" D11
3	C	Data Column 0	"not" D0
4	D	Data Column 1	"not" D1
5	K	Data Column 2	"not" D2
6	L	Data Column 3	"not" D3
7	M	Data Column 4	"not" D4
8	N	Data Column 5	"not" D5
9	U	Data Column 6	"not" D6
10	V	Data Column 7	"not" D7
11	W	Data Column 8	"not" D8
12	d	Data Column 9	"not" D9
15	X	Ready	"not" RDY
17	e	Hopper Empty	"not" HCK
18	y	Stacker Full	"not" STF
20	x	End-of-File	"not" EOF
21	z	Off-Line	"not" TEST
22	f	Pick Command	"not" PC
23	r	Index Mark	"not" IM
24/BB	CC/HH	Ground	GND
U	w	End-of-File Clear	"not" EOF CLEAR
V	n	Busy	"not" BSY
W	p	Motion/Pick Check	"not" MOCK
X	c	Error (light/dark)	"not" ERROR

4-9. CABLE ASSEMBLY CONNECTOR PIN FUNCTIONS.

4-10. Table 4-1 contains a list of cable assembly pin assignments for the interface PCA and the card reader connectors.

Table 4-2. Card Reader Interface PCA, Replaceable Parts

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1,2,C8 thru C13, 15,C19 thru C22, C25 thru C28, C30 thru C33, C35 thru C40, C44 thru C48	0160-2055	CAPACITOR, fxd, cer, 0.01 uF, +80 −20%, 100 Vdcw	56289	C023F101F103ZS22-CD
C3	0160-0939	CAPACITOR, fxd, Mica, 430 pF, 5%, 200 Vdcw	28480	0160-0939
C4,5,14,16,18	0160-0154	CAPACITOR, fxd, My, 2200 pF, 10%, 200 Vdcw	56289	192P22292-PTS
C6	0180-0137	CAPACITOR, fxd, Ta, 100 uF, 20%, 10 Vdcw	56289	5C10A7-CML
C7,17,23,24,29, 34,C41 thru C43, C49 thru C51	0180-0197	CAPACITOR, fxd, Ta, 2.2 uF, 10%, 20 Vdcw	56289	200P27
C52	0160-0153	CAPACITOR, fxd, My, 0.001 uF, 10%, 200 Vdcw	56289	192P10292-PTS
CR1	1910-0030	DIODE, Ge, 100 mA, 0.65V	14433	G694
CR2	1901-0081	DIODE, Si, 50V	07263	FD1415
Q1	1854-0071	TRANSISTOR, Si, NPN	01295	SKA1124
R1,2,3,34,36, 37,55	0689-3440	RESISTOR, fxd, flm, 196 ohms, 1%, 1/8W	28480	0689-3440
R4	0698-3158	RESISTOR, fxd, flm, 23.7k, 1%, 1/8W	28480	0698-3158
R5,7,9,11,13, 15,17,19,21, 23,25,27,29, 38,40,42,45, 47,49,50,52	0757-0416	RESISTOR, fxd, flm, 511 ohms, 1%, 1/8W	28480	0757-0416
R6,8,10,12,14, 16,18,20,22, 24,26,28,30, 39,41,43, 44,46,48, 51,53	0757-0274	RESISTOR, fxd, flm, 1.21k, 1%, 1/8W	28480	0757-0274
R32	0698-3445	RESISTOR, fxd, flm, 348 ohms, 1%, 1/8W	28480	0698-3445
R33	0757-0290	RESISTOR, fxd, flm, 6.19k ohms, 1%, 1/8W	28480	0757-0290
R35	0698-0082	RESISTOR, fxd, flm, 464 ohms, 1%, 1/8W	28480	0698-0082
R54,56	0698-3445	RESISTOR, fxd flm, 196 ohms, 1%, 1/8W	28480	0698-3445
R57,59	1810-0020	RESISTOR, network (7 fxd registers)	28480	1810-0020
R58,R60 thru R62	0757-0427	RESISTOR, fxd, flm, 1.50k, 1%, 1/8W	28480	0757-0427
U11,14,15	1820-0069	INTEGRATED CIRCUIT, TTL	01295	SN4344
U12,43,73,92	1820-0071	INTEGRATED CIRCUIT, TTL	01295	SN4345
U16,21,23, U24 thru U26, 32,36,45,53, 63,65,74, 82 thru 85, 94,105	1820-0054	INTEGRATED CIRCUIT, TTL	01295	SN4342
U17,27,37,47,57, 67,77,87,97,107	1820-0956	INTEGRATED CIRCUIT, CTL	07263	SL3459
U22	1820-0075	INTEGRATED CIRCUIT, TTL	01295	SN4353
U33 thru U35,44	1820-0068	INTEGRATED CIRCUIT, TTL	01295	SN4343
U42	1820-0207	INTEGRATED CIRCUIT, TTL	07263	SL4463
U46,55,66,75, 86,95	1820-0063	INTEGRATED CIRCUIT, TTL	01295	SN4348
U52,62,72,106	1820-0070	INTEGRATED CIRCUIT, TTL	01295	SN4345
U56,76,96	1820-0301	INTEGRATED CIRCUIT, TTL	01295	SN4463

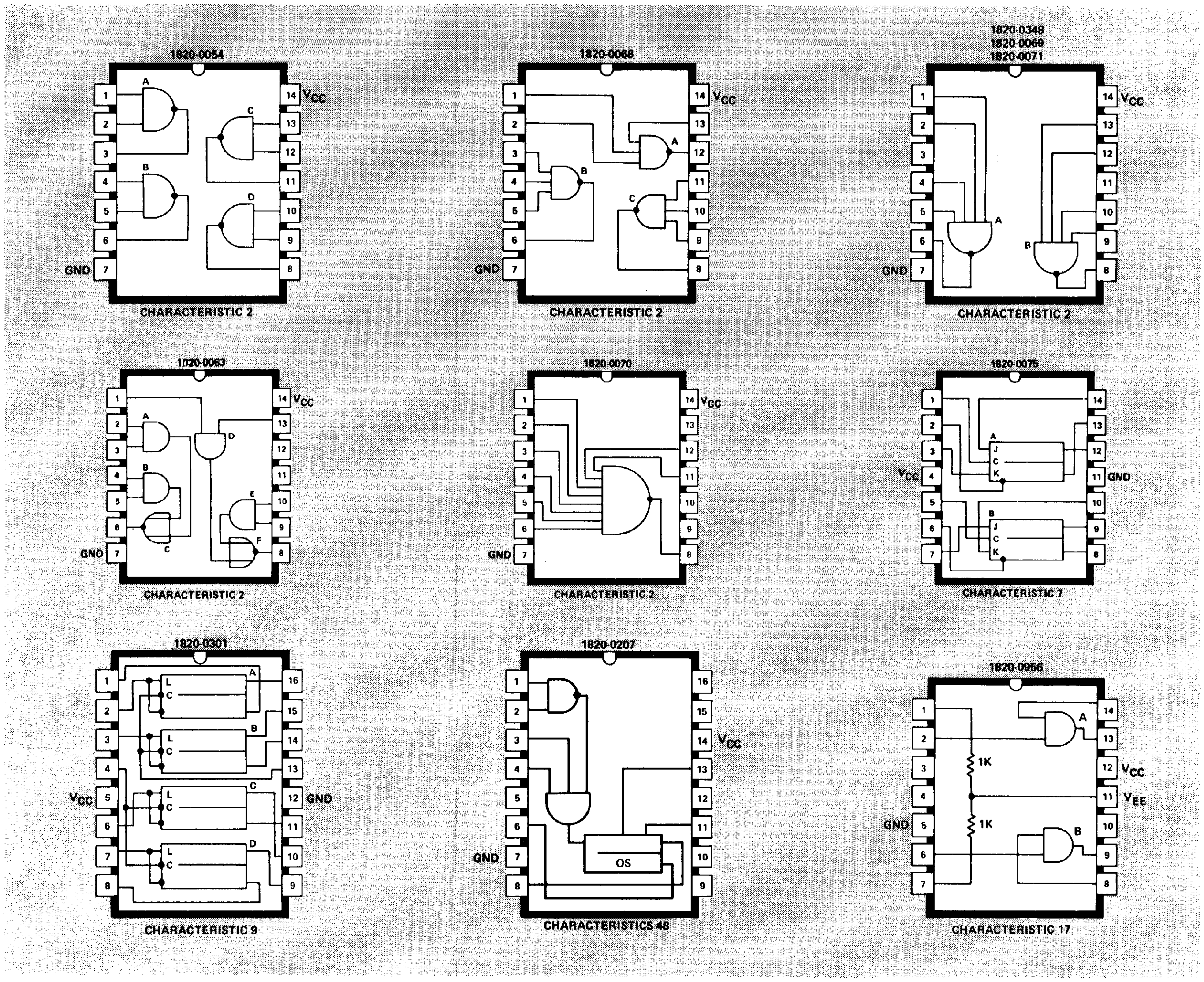

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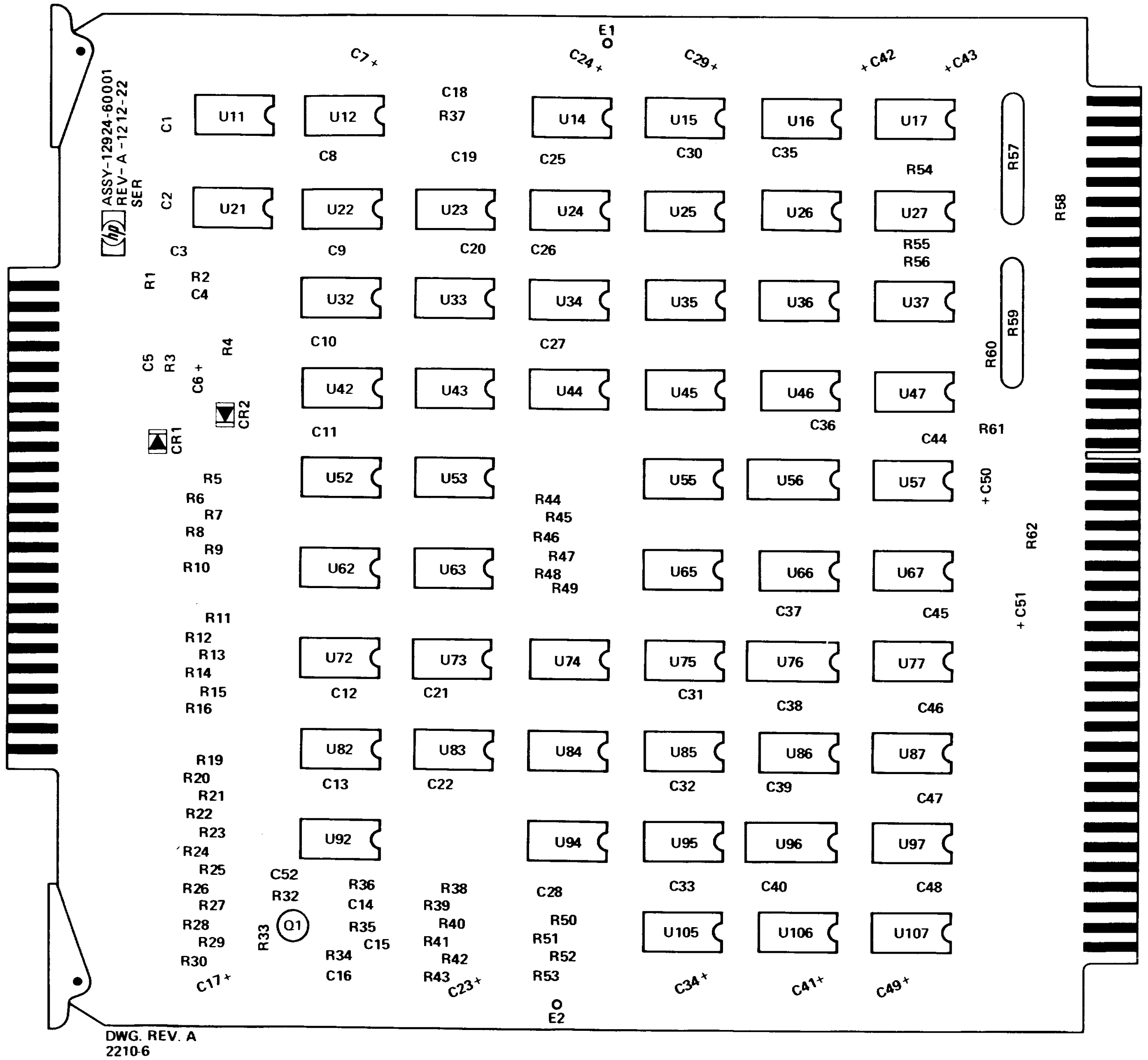
Figure 4-2. Integrated Circuit Diagrams

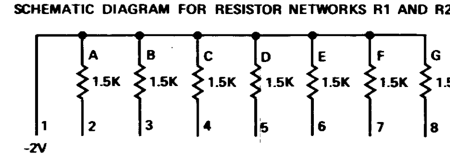
Table 4-3. Integrated Circuit Characteristics

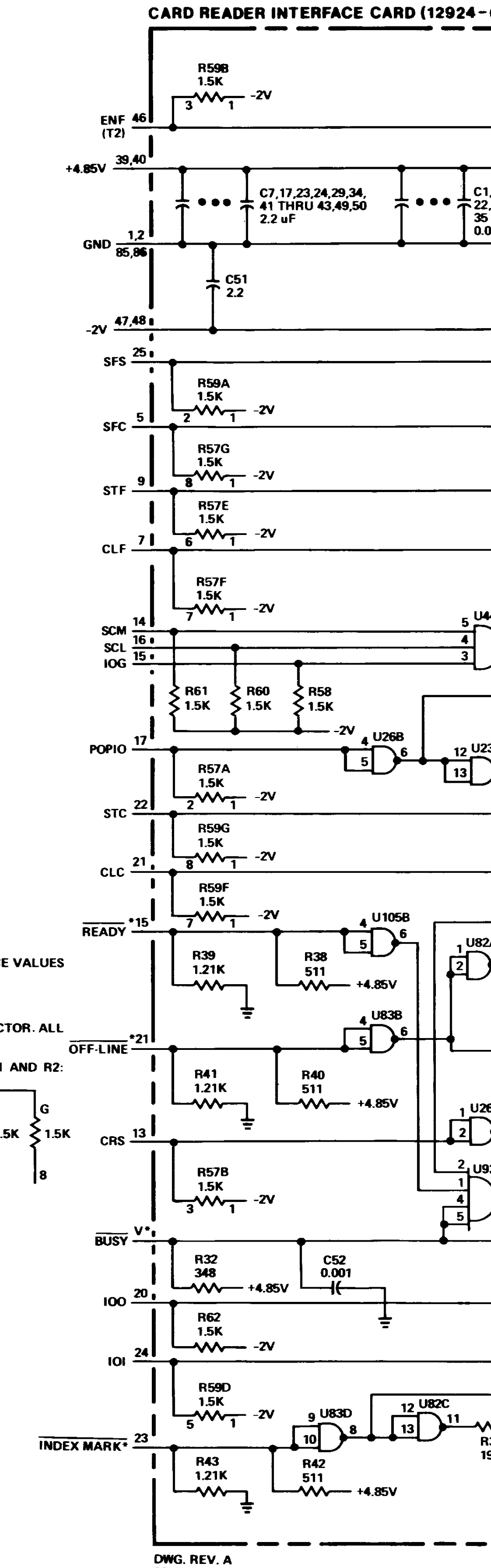
CHARACTERISTIC	INPUT LEVEL		OUTPUT LEVEL		OPEN INPUT ACTS AS:	MAXIMUM PROPAGATION DELAY	
	LOGIC 1 (VOLTS, MIN)	LOGIC 0 (VOLTS, MAX)	LOGIC 1 (VOLTS, MIN)	LOGIC 0 (VOLTS, MAX)		TO LOGIC 1 (NANOSECONDS)	TO LOGIC 0 (NANOSECONDS)
2	+2.0	+0.8	+2.4	+0.4	Logic 1	29	15
7	+2.0	+0.8	+2.4	+0.4	Logic 1	50	50
9	+2.0	+0.8	+2.4	+0.4	Logic 1	40	25
17	+1.25	+0.5	+2.25	-0.36	Logic 0	18	18
48	+1.9	+0.85	+2.4	+0.45	Logic 1	40	–

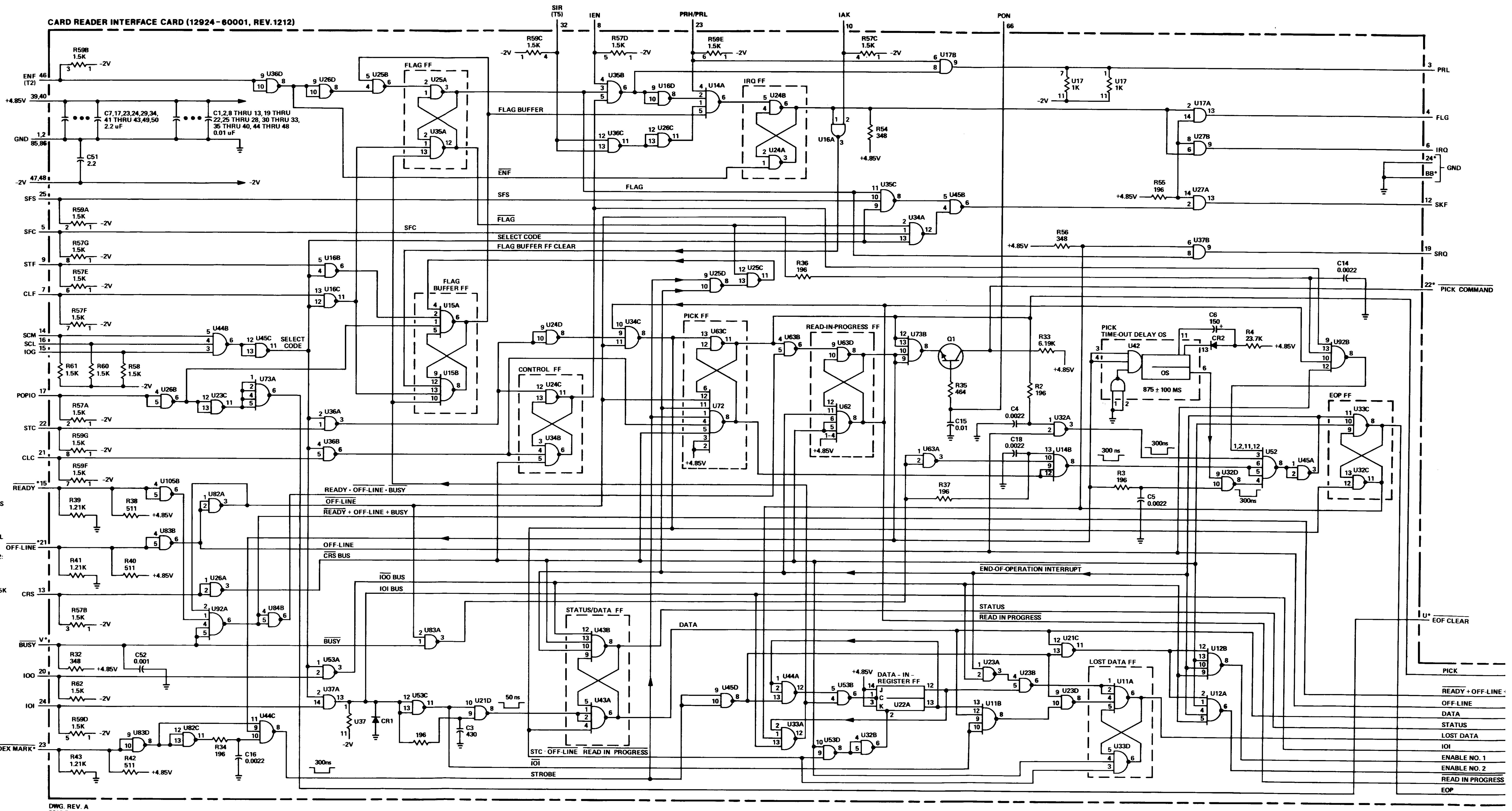


NOTES:

1. RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. ALL LOGIC IS POSITIVE TRUE.
3. AN ASTERISK (*) DENOTES PINS ON THE 48-PIN CONNECTOR. ALL OTHER PINS ARE ON THE 86-PIN CONNECTOR.
4. SCHEMATIC DIAGRAM FOR RESISTOR NETWORKS R1 AND R2:







CARD READER INTERFACE CARD (12924-60001, REV.1212)
FLAG FF
FLAG BUFFER FF
CONTROL FF
PICK FF
READ-IN-PROGRESS FF
PICK TIME-OUT DELAY OS
875 ± 100 MS
EOP FF
STATUS/DATA FF
DATA - IN - REGISTER FF
LOST DATA FF
FLAG BUFFER
SELECT CODE
FLAG BUFFER FF CLEAR
READY · OFF-LINE · BUSY
READY + OFF-LINE + BUSY
CRS BUS
IOO BUS
IOI BUS
END-OF-OPERATION INTERRUPT
STATUS
READ IN PROGRESS
DATA
STROBE
PRL
FLG
IRQ
GND
SKF
SRQ
PICK COMMAND
EOF CLEAR
PICK
OFF-LINE
LOST DATA
IOI
ENABLE NO. 1
ENABLE NO. 2
EOP
ENF
SFS
SFC
STF
CLF
SCM
SCL
IOG
POPIO
STC
CLC
READY
CRS
BUSY
IOO
INDEX MARK
DWG. REV. A
2210-7

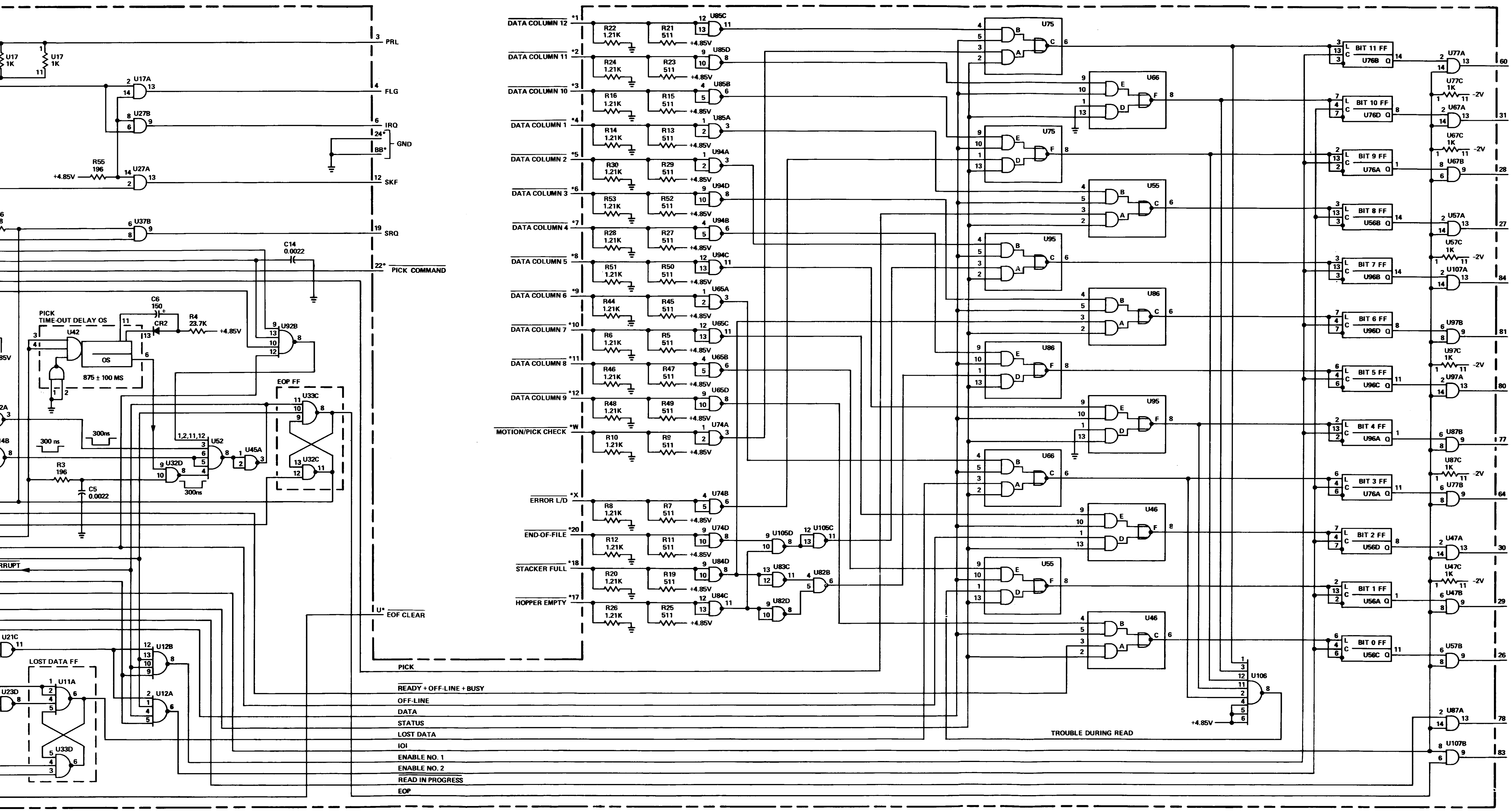


Figure 4-1. Card Reader Interface PCA
Parts Location and Logic Diagrams

REPLACEABLE PARTS

SECTION V

5-1. INTRODUCTION.

5-2. This section contains information for ordering replacement parts for the HP 12924A Card Reader Interface Kit. Table 5-1 lists parts in alphanumeric order by HP part number and lists the following information for each part.

a. Description of the part. (Refer to table 5-3 for an explanation of abbreviations and reference designations used in the DESCRIPTION column.)

b. Typical manufacturer of the part in a five-digit code; refer to the list of manufacturers in table 5-2.

c. Manufacturer's part number.

d. Total quantity of each part used in the interface kit.

5-3. A separate parts list is provided along with the parts location view for the interface card in section IV of this manual. This parts list presents the parts in alphanumeric order by reference designation.

5-4. ORDERING INFORMATION.

5-5. To order replacement parts, address the order or inquiry to the local Hewlett-Packard Sales and Service Office. (Refer to the list at the end of this manual for addresses.) Specify the following information for each part ordered:

a. Unit model and serial number.
b. Hewlett-Packard stock number for each part.
c. Description of each part.
d. Circuit reference designation.

Table 5-1. Card Reader Interface Kit Replaceable Parts

HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	TQ
0160-0153	CAPACITOR, fxd, My, 0.001 uF, 10%, 20 Vdcw	56289	192P10292-PTS	1
0160-0154	CAPACITOR, fxd, My, 2200 pF, 10%, 200 Vdcw	28480	0160-0154	5
0160-0939	CAPACITOR, fxd, Mica, 430 pF, 5%, 200 Vdcw	28480	0160-0939	1
0160-2055	CAPACITOR, fxd, cer, 0.01 uF, +80 -20%, 100 Vdcw	56289	C023F101F103ZS22-CD	32
0180-0137	CAPACITOR, fxd, Ta, 100 uF, 20%, 10 Vdcw	28480	0180-0137	1
0180-0197	CAPACITOR, fxd, Ta, 2.2 uF, 10%, 20 Vdcw	28480	0180-0197	12
0698-0082	RESISTOR, fxd, flm, 464 ohms, 1%, 1/8W	28480	0698-0082	1
0698-3158	RESISTOR, fxd, flm, 23.7k ohms, 1%, 1/8W	28480	0698-3158	1
0698-3440	RESISTOR, fxd, flm, 196 ohms, 1%, 1/8W	28480	0698-3440	7
0698-3445	RESISTOR, fxd, flm, 348 ohms, 1%, 1/8W	28480	0698-3445	2
0757-0274	RESISTOR, fxd, flm, 1.21k, 1%, 1/8W	28480	0757-0274	22
0757-0290	RESISTOR, fxd, flm, 6.19k ohms, 1%, 1/8W	28480	0757-0290	1
0757-0416	RESISTOR, fxd, flm, 511 ohms, 1%, 1/8W	28480	0757-0416	22
0757-0427	RESISTOR, fxd, flm, 1.50k, 1%, 1/8W	28480	0757-0427	4
1810-0020	RESISTOR, network (7 fxd flm resistors)	28480	1820-0020	2
1820-0054	INTEGRATED CIRCUIT, TTL	01295	SN4342	19
1820-0063	INTEGRATED CIRCUIT, TTL	01295	SN4348	6
1820-0068	INTEGRATED CIRCUIT, TTL	01295	SN4343	4
1820-0069	INTEGRATED CIRCUIT, TTL	01295	SN4344	3
1820-0070	INTEGRATED CIRCUIT, TTL	01295	SN4345	4
1820-0071	INTEGRATED CIRCUIT, TTL	01295	SN4345	4
1820-0075	INTEGRATED CIRCUIT, TTL	01295	SN4353	1
1820-0207	INTEGRATED CIRCUIT, TTL	07263	SL12895	1
1820-0301	INTEGRATED CIRCUIT, TTL	01295	SN4463	3
1820-0956	INTEGRATED CIRCUIT, CTL	07263	SL3459	10
1854-0071	TRANSISTOR, Si, NPN	01295	SKA1124	1
1901-0081	DIODE, Si, 50V	07263	FD1415	1
1910-0030	DIODE, Ge, 100 mA, 0.65V	14433	G694	1
12924-60001	CARD READER INTERFACE PRINTED-CIRCUIT ASSEMBLY	28480	12924-60001	1
12924-60002	CABLE ASSEMBLY	28480	12924-60002	1
12924-90001	CARD READER INTERFACE KIT OPERATING AND SERVICE MANUAL	28480	12924-90001	1

Table 5-2. Code List of Manufacturers

The following code numbers are from the Federal Supply Code for Manufacturers Cataloging Handbooks H4-1 and H4-2, and the latest supplements.

Code No.	Manufacturer	Address	Code No.	Manufacturer	Address
01295	Texas Instruments, Inc. Transistor Products Division	Dallas, Texas	28480	Hewlett-Packard Co.	Palo Alto, Cal.
07263	Fairchild Camera & Inst. Corp., Semiconductor Division	Mt. View, Cal.	14433	ITT Semiconductor, a Div. of Int. Telephone and Telegraph	West Palm Beach, Fla.
			56289	Sprague Electric Co.	North Adams, Mass.

Table 5-3. Reference Designations and Abbreviations

REFERENCE DESIGNATIONS

A	= assembly
B	= motor, synchro
BT	= battery
C	= capacitor
CB	= circuit breaker
CR	= diode
DL	= delay line
DS	= indicator
E	= Misc electrical parts
F	= fuse
FL	= filter
J	= receptacle connector
K	= relay
L	= inductor
M	= meter
P	= plug connector
Q	= semiconductor device other than diode or integrated circuit
R	= resistor
RT	= thermistor
S	= switch
T	= transformer
TB	= terminal board
TP	= test point
U	= integrated circuit, non-repairable assembly
V	= vacuum tube, photocell, etc.
VR	= voltage regulator
W	= jumper wire
X	= socket
Y	= crystal
Z	= tuned cavity, network

ABBREVIATIONS

A	= amperes
ac	= alternating current
Ag	= silver
Al	= aluminum
ar	= as required
adj	= adjust
assy	= assembly
b	= base
bp	= bandpass
bpi	= bits per inch
blk	= black
blu	= blue
brn	= brown
brs	= brass
Btu	= British thermal unit
Be Cu	= beryllium copper
cpi	= characters per inch
coll	= collector
cw	= clockwise
ccw	= counterclockwise
cer	= ceramic
com	= common
crt	= cathode-ray tube
CTL	= complementary-transistor logic
cath	= cathode
Cd pl	= cadmium plate
comp	= composition
conn	= connector
compl	= complete
dc	= direct current
dr	= drive
DTL	= diode-transistor logic
depc	= deposited carbon
dpdt	= double-pole, double-throw
dpst	= double-pole, single-throw
em	= emitter
ECL	= emitter-coupled logic
ext	= external
encap	= encapsulated
elctlt	= electrolytic
F	= farads
FF	= flip-flop
flh	= flat head
flm	= film
fxd	= fixed
filh	= fillister head
G	= giga (10^9)
Ge	= germanium
gl	= glass
gnd	= ground(ed)
gra	= gray
grn	= green
H	= henries
Hg	= mercury
hr	= hour(s)
Hz	= hertz
hdw	= hardware
hex	= hexagon, hexagonal
ID	= inside diameter
IF	= intermediate frequency
in.	= inch, inches
I/O	= input/output
int	= internal
incl	= include(s)
insul	= insulation, insulated
impgrg	= impregnated
incand	= incandescent
ips	= inches per second
k	= kilo (10^3), kilohm
lp	= low pass
m	= milli (10^{-3})
M	= mega (10^6), megohm
My	= Mylar
mfr	= manufacturer
mom	= momentary
mtg	= mounting
misc	= miscellaneous
met. ox.	= metal oxide
mintr	= miniature
n	= nano (10^{-9})
nc	= normally closed or no connection
Ne	= neon
no.	= number
n.o.	= normally open
np	= nickel plated
NPN	= negative-positive-negative
NPO	= negative-positive zero (zero temperature coefficient)
NSR	= not separately replaceable
NRFR	= not recommended for field replacement
OD	= outside diameter
OBD	= order by description
orn	= orange
ovh	= oval head
oxd	= oxide
p	= pico (10^{-12})
PC	= printed circuit
PCA	= printed-circuit assembly
PWB	= printed-wiring board
phh	= phillips head
pk	= peak
p-p	= peak-to-peak
pt	= point
prv	= peak inverse voltage
PNP	= positive-negative-positive
pwv	= peak working voltage
porc	= porcelain
posn	= position(s)
pozi	= pozidrive
rf	= radio frequency
rdh	= round head
rms	= root-mean-square
rwv	= reverse working voltage
rect	= rectifier
r/min	= revolutions per minute
RTL	= resistor-transistor logic
s	= second
SB, TT	= slow blow
Se	= selenium
Si	= silicon
scr	= silicon controlled rectifier
sst	= stainless steel
stl	= steel
spcl	= special
spdt	= single-pole, double-throw
spst	= single-pole, single-throw
Ta	= tantalum
td	= time delay
Ti	= titanium
tgl	= toggle
thd	= thread
tol	= tolerance
TTL	= transistor transistor logic
U(μ)	= micro (10^{-6})
V	= volt(s)
var	= variable
vio	= violet
Vdcw	= direct current working volts
W	= watts
ww	= wirewound
wht	= white
WIV	= working inverse voltage
yel	= yellow

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TWX: 810-726-2204

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Phoenix 85034
Tel: (602) 252-5061
TWX: 910-951-1330

5737 East Broadway
Tucson 85716
Tel: (602) 298-2313
TWX: 910-952-1162

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TWX: 910-499-2170

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TWX: 910-373-1280

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Sacramento 95825
Tel: (916) 482-1463
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TWX: 710-465-2029

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Ft. Lauderdale 33307
Tel: (305) 731-2020
TWX: 510-955-4099

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TWX: 810-850-0113

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450 Interstate North
Atlanta 30328
Tel: (404) 436-6181
TWX: 810-766-4890

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Tel: (312) 677-0400
TWX: 910-223-3613

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Indianapolis 46205
Tel: (317) 546-4891
TWX: 810-341-3263

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1942 Williams Boulevard
Kenner 70062
Tel: (504) 721-6201
TWX: 810-955-5524

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Baltimore 21207
Tel: (301) 944-5400
TWX: 710-862-9157

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Rockville 20850
Tel: (301) 948-6370
TWX: 710-828-9684

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Lexington 02173
Tel: (617) 861-8960
TWX: 710-326-6904

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21840 West Nine Mile Road
Southfield 48075
Tel: (313) 353-9100
TWX: 810-224-4882

MINNESOTA
2459 University Avenue
St. Paul 55114
Tel: (612) 645-9461
TWX: 910-563-3734

MISSOURI
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Kansas City 64137
Tel: (816) 763-8000
TWX: 910-771-2087

148 Weldon Parkway
Maryland Heights 63043
Tel: (314) 567-1455
TWX: 910-764-0830

NEW JERSEY
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Paramus 07652
Tel: (201) 265-5000
TWX: 710-990-4951

1060 N. Kings Highway
Cherry Hill 08034
Tel: (609) 667-4000
TWX: 710-892-4945

NEW MEXICO
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Station C
6501 Lomas Boulevard N.E.
Albuquerque 87108
Tel: (505) 265-3713
TWX: 910-989-1665

156 Wyatt Drive
Las Cruces 88001
Tel: (505) 526-2485
TWX: 910-983-0550

NEW YORK
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Tel: (518) 869-8462
TWX: 710-441-8270

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Tel: (607) 754-0050
TWX: 510-252-0890

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OKLAHOMA
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Oklahoma City 73112
Tel: (405) 848-2801
TWX: 910-830-6862

OREGON
Westhills Mall, Suite 158
4475 S.W. Scholls Ferry Road
Portland 97225
Tel: (503) 292-9171
TWX: 910-464-6103

PENNSYLVANIA
2500 Moss Side Boulevard
Monroeville 15146
Tel: (412) 271-0724
TWX: 710-797-3650

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King of Prussia Industrial Park
King of Prussia 19406
Tel: (215) 265-7000
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TWX: 710-956-0157

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Edmonton
Tel: (403) 452-3670
TWX: 610-831-2431

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Hewlett-Packard (Canada) Ltd.
4519 Canada Way
North Burnaby 2
Tel: (604) 433-8213
TWX: 610-922-5059

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Tel: (204) 786-7581
TWX: 610-671-3531

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CENTRAL AND SOUTH AMERICA

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S.A.C.e.I
Lavalle 1171 - 3°
Buenos Aires
Tel: 35-0436, 35-0627, 35-0431
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Rua Frei Caneca 1119
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Tel: 288-7111, 287-5858
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Carrera 7 No. 48-59
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Telex: 017-74-507

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Apartado Postal 689
Edificio Terán
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Caracas
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Telex: 31617

Hewlett-Packard France
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F-31 **Blagnac**
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Telex: 51957

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D-6 Nieder-Eschbach/Ffm 56
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D-1000 **Berlin W.** 12
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Athens 126
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Telex: 21 59 62 rkar gr

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Telex: 32046 via Milan

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I-10129 **Turin**
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Telex: 32046 via Milan

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Avenue du Col-Vert, 1
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Telex: 23 494

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Telex: 13 216 hepa nl

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Nesveien 13
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Telex: 16621

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Rua Rodrigo da Fonseca 103
P.O. Box 2531
P-**Lisbon** 1
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Cable: TELECTRA Lisbon
Telex: 1598

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Jerez No 8
Madrid 16
Tel: 458 26 00
Telex: 23515 hpe

Hewlett-Packard Española, S.A.
Milanesado 21-23
E-**Barcelona** 17
Tel: (3) 203 62 00

SWEDEN
Hewlett-Packard Sverige AB
Enighetsvägen 1-3
Fack
S-161 20 **Bromma** 20
Tel: (08) 98 12 50
Cable: MEASUREMENTS Stockholm
Telex: 10721

Hewlett-Packard Sverige AB
Hagakersgatan 9C
S-431 41 **Mölndal**
Tel: (031) 27 68 00/01
Telex: 21 312 hpmindl s

SWITZERLAND
Hewlett Packard (Schweiz) AG
Zürcherstrasse 20
P.O. Box 64
CH-8952 **Schlieren** Zurich
Tel: (01) 98 18 21/24
Cable: HPAG CH
Telex: 53933

Hewlett-Packard (Schweiz) AG
Rue du Bois-du-Lan 7
P.O. Box 85
1217 Meyrin 2 **Geneva**
Tel: (022) 41 54 00
Cable: HEWPACKSA Geneva
Telex: 27333 hpsa ch

TURKEY
Telekom Engineering Bureau
P.O. Box 376
Karaköy
Istanbul
Tel: 49 40 40
Cable: TELEMATION Istanbul

UNITED KINGDOM
Hewlett-Packard Ltd.
224 Bath Road
Slough, SL1 4 DS, Bucks
Tel: Slough (0753) 33341
Cable: HEWPIE Slough
Telex: 84413

Hewlett-Packard Ltd.
"The Graftons"
Stamford New Road
Altrincham, Cheshire
Tel: (061) 928-8626
Telex: 668068

SOCIALIST COUNTRIES PLEASE CONTACT:
Hewlett-Packard Ges.m.b.H
Innstrasse 23/2
Postfach 45
A-1204 **Vienna**, Austria
Tel: (0222) 33 66 06-09
Cable: HEWPACK Vienna
Telex: 75923 hewpak a

ALL OTHER EUROPEAN COUNTRIES CONTACT:
Hewlett-Packard S.A.
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P.O. Box 85
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Switzerland
Tel: (022) 41 54 00
Cable: HEWPACKSA Geneva
Telex: 2.24.86

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Tel: 43-7866
Cable: HEWPARD Sydney
Telex: 21561

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Prospect 5082
South Australia
Tel: 65-2366
Cable: HEWPARD Adelaide

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2nd Floor, Suite 13
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196 Adelaide Terrace
Perth, W.A. 6000
Tel: 21-3330
Cable: HEWPARD Perth

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Dickson A.C.T. 2602
Tel: 49-8194
Cable: HEWPARD Canberra ACT

Hewlett-Packard Australia Pty. Ltd.
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Kenmore 4069 Queensland
Tel: 70-4050

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Yahala Building
Staples Street
Colombo 2
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Cable: BLUESTAR

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Lajpat Nagar
New Delhi 24, India
Tel: 62 32 76
Telex: 463
Cable: BLUESTAR

Blue Star, Ltd.
Blue Star House
11/11A Magarath Road
Bangalore, 25
Tel: 51473
Telex: 430
Cable: BLUESTAR

Blue Star, Ltd.
1-1-117/1
Sarojini Devi Road
Secunderabad 3
Tel: 7 63 91, 7 73 93
Cable: BLUEFROST

Blue Star, Ltd.
23/24 Second Line Beach
Madras 1, India
Tel: 2 39 55
Telex: 379
Cable: BLUESTAR

Blue Star, Ltd.
1B Kaiser Bungalow
Dindli Road
Jamshedpur, India
Tel: 38 04
Cable: BLUESTAR

INDONESIA
Bah Bolon Trading Coy. N.V.
Djalah Merdeka 29
Bandung
Tel: 4915; 51560
Cable: ILMU
Telex: 08-809

IRAN
Multicorp International Ltd.
Avenue Soraya 130
P.O. Box 1212
Teheran
Tel: 83 10 35-39
Cable: MULTICORP Tehran
Telex: 2876 service tn

ISRAEL
Electronics & Engineering Div. of Motorola Israel Ltd.
17 Aminadav Street
Tel-Aviv
Tel: 36941 (3 lines)
Cable: BASTEL Tel-Aviv
Telex: MOTIL IL

JAPAN
Yokogawa-Hewlett-Packard Ltd.
Ohashi Building
1-59-1 Yoyogi
Shibuya-ku, **Tokyo**
Tel: 03-370-2281/92
Telex: 232-2024YHP
Cable: YHPMARKET TOK 23-724

Yokogawa-Hewlett-Packard Ltd.
Nisei Ibaragi Bldg.
2-2-8 Kasuga
Ibaragi-Shi
Osaka
Tel: (0726) 23-1641
Telex: 5332-385 YHP OSAKA

Yokogawa-Hewlett-Packard Ltd.
Ito Building
No. 59, Kotori-cho
Nakamura-ku, **Nagoya** City
Tel: (052) 551-0215

Yokogawa-Hewlett-Packard Ltd.
Nitto Bldg.
2-4-2 Shinohara-Kita
Kohoku-ku
Yokohama 222
Tel: 045-432-1504
Telex: 382-3204 YHP YOK

JORDAN
Constantin E. Macridis
Clemenceau Street
P.O. Box 7213
Beirut, Lebanon
Tel: 220846
Cable: ELECTRONUCLEAR Beirut

KENYA
Kenya Kinetics
P.O. Box 18311
Nairobi, Kenya
Tel: 57726
Cable: PROTON

KOREA
Amtraco Corporation
Industrial Products Div.
Seoul P.O. Box 1103
8th floor, DaeKyung Bldg.
107 Sejong Ro
Chongro-Ku, Seoul
Tel: 73-8924-7
Cable: AMTRACO Seoul

LEBANON
Constantin E. Macridis
Clemenceau Street
P.O. Box 7213
Beirut
Tel: 220846
Cable: ELECTRONUCLEAR Beirut

MALAYSIA
MECOMB Malaysia Ltd.
2 Lorong 13/6A
Section 13
Petaling Jaya, **Selangor**
Cable: MECOMB Kuala Lumpur

MOZAMBIQUE
A. N. Goncalves, LDA.
4.1 Apt. 14 Av. D. Luis
P.O. Box 107
Lourenco Marques
Cable: NEGON

NEW ZEALAND
Hewlett-Packard (N.Z.) Ltd.
94-96 Dixson St.
P.O. Box 9443
Wellington, N.Z.
Tel: 56-559
Cable: HEWPACK Wellington

Hewlett Packard (N.Z.) Ltd.
Box 51092
Pukuranga
Tel: 56-9837
Cable: HEWPACK, Auckland

PAKISTAN
Mushko & Company, Ltd.
Oosman Chambers
Abdullah Haroon Road
Karachi 3
Tel: 511027, 512927
Cable: COOPERATOR Karachi

Mushko & Company, Ltd.
38B, Satellite Town
Rawalpindi
Tel: 41924
Cable: FEMUS Rawalpindi

PHILIPPINES
Electromex Inc.
5th Floor, Architects Center Bldg.
Ayala Ave., Makati, Rizal
C.C.P.O. Box 1028
Makati, Rizal
Tel: 86-18-87, 87-76-77
Cable: ELEMEX Manila

SINGAPORE
Mechanical and Combustion Engineering Company Ltd.
9, Jalan Kilang
Red Hill Industrial Estate
Singapore, 3
Tel: 642361-3; 632611
Cable: MECOMB Singapore

Hewlett-Packard Far East Area Office
P.O. Box 87
Alexandra Post Office
Singapore 3
Tel: 633022
Cable: HEWPACK SINGAPORE

SOUTH AFRICA
Hewlett Packard South Africa (Pty.), Ltd.
P.O. Box 31716
Braamfontein Transvaal
Milnerton
30 De Beer Street
Johannesburg
Tel: 725-2080, 725-2030
Telex: 0226 JH
Cable: HEWPACK Johannesburg

Hewlett Packard South Africa (Pty.), Ltd.
Breecastle House
Bree Street
Cape Town
Tel: 3-6019, 3-6545
Cable: HEWPACK Cape Town
Telex: 5-0006

Hewlett Packard South Africa (Pty.), Ltd.
641 Ridge Road, Durban
P.O. Box 99
Overport, Natal
Tel: 88-6102
Telex: 567954
Cable: HEWPACK

TAIWAN
Hewlett Packard Taiwan
39 Chung Shiao West Road
Sec. 1
Overseas Insurance Corp. Bldg. 7th Floor
Taipei
Tel: 389160,1,2, 375121, Ext. 240-249
Telex: TP824 HEWPACK
Cable: HEWPACK Taipei

THAILAND
UNIMESA Co., Ltd.
Chongkolnee Building
56 Suriwongse Road
Bangkok
Tel: 37956, 31300, 31307, 37540
Cable: UNIMESA Bangkok

UGANDA
Uganda Tele-Electric Co., Ltd.
P.O. Box 4449
Kampala
Tel: 57279
Cable: COMCO Kampala

VIETNAM
Peninsular Trading Inc.
P.O. Box H-3
216 Hien-Vuong
Saigon
Tel: 20-805, 93398
Cable: PENTRA, SAIGON 242

ZAMBIA
R. J. Tilbury (Zambia) Ltd.
P.O. Box 2792
Lusaka
Zambia, Central Africa
Tel: 73793
Cable: ARJAYTEE, Lusaka

MEDITERRANEAN AND MIDDLE EAST COUNTRIES NOT SHOWN PLEASE CONTACT:
Hewlett-Packard
Co-ordination Office for Mediterranean and Middle East Operations
Via Marocco, 7
I-00144 Rome-Eur, Italy
Tel: (6) 59 40 29
Cable: HEWPACKIT Rome
Telex: 61514

OTHER AREAS NOT LISTED, CONTACT:
Hewlett-Packard
INTERCONTINENTAL
3200 Hillview Ave.
Palo Alto, California 94304
Tel: (415) 326-7000
(Feb. 71 493-1501)
TWX: 910-373-1267
Cable: HEWPACK Palo Alto
Telex: 034-8300, 034-8493

CERTIFICATION

The Hewlett-Packard Company certifies that this instrument was thoroughly tested and inspected and found to meet its published specifications when it was shipped from the factory. The Hewlett-Packard Company further certifies that its calibration measurements are traceable to the U.S. National Bureau of Standards to the extent allowed by the Bureau's calibration facility.

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