Microprogram Development Subsystem

Model 64276A/B/C
Model 64320S 25 MHz Logic State/Software Analyzer
Model 64861A User-definable Microassembler

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Description

The HP 64276 Microprogram Development Subsystem and the HP 64320S 25 MHz Logic State/Software Analyzer provide run control and real-time analysis for microprogrammable systems. As integrated subsystems of the HP 64000 Logic Development System, the HP 64276 and the HP 64320S add the power of run control and analysis to all phases of the design, development, and maintenance of microprogram-based products.

The Microprogram Development Subsystem consists of three components: a Run Control module, a Writable Control Store (WCS), and a 25 MHz Logic State/Software Analyzer (figure 1). Run Control provides program flow control, clock control, and break event detection. Writable Control Store provides high-speed RAM for storing the microcode to be executed. A 25 MHz Logic State/Software Analyzer monitors system buses and provides trigger, store, and sequencing functions for locating problems in the microprogram.

The Microprogram Development Subsystem supports software development for a wide variety of microprogrammable processors and sequencers. Integration of the Microprogram Development Subsystem with other powerful HP 64000 analysis and emulation tools allows for interactive, cross-triggered measurements in complex multiprocessor environments.

Features

- The choice of clock control or real-time address jam at break detection offers flexible target system control.
- Address ranging and two-level sequencing provide powerful break event specification.
- Real-time, nonintrusive analysis of microprogrammed system activity reduces software development time.
- Flexible user-definable microassembler provides support for a wide variety of microprogrammable devices.
- Microcode source interleaved with analyzer trace data speeds software debugging.
- Linking of separately assembled microcode modules accelerates software turnaround time.
- MACRO instruction feature of the microassembler improves software engineering productivity.
- Modular architecture permits specific Writable Control Store configurations for customized development tool needs.
- Integration of Run Control and analysis capabilities simplifies operation.
- Interaction with other HP 64000 system emulators and analyzers provides real-time analysis in multiprocessor environments.

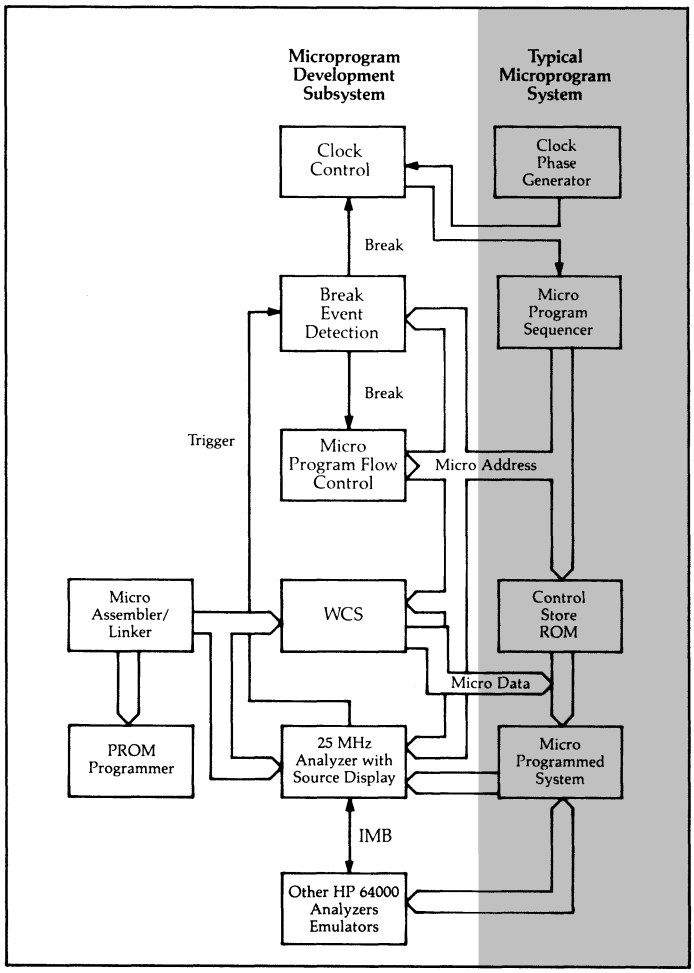

Figure 1. *The Microprogram Development Subsystem consists of a Run Control Module, a Writable Control Store, and a 25 MHz Logic State/Software Analyzer.*

Run Control

Run Control provides system clock control, break event specification, and address jamming. These important features improve debugging of microprogram-based systems.

Architecture

The Run Control module taps into the clock lines on the target system to obtain the greatest level of clock control. Clock control functions allow you to start and stop the clock, single step, and break on a specific clock edge or pattern. The configuration menu for the Microprogram Development Subsystem shows the flexibility available with Run Control (figure 2).

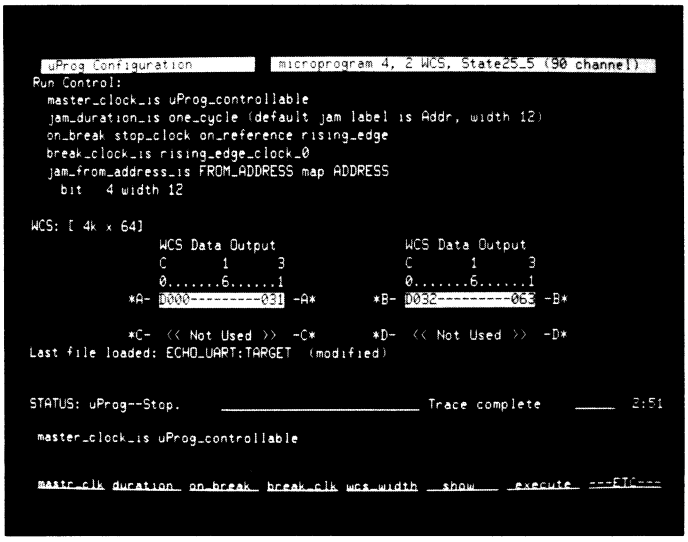

Figure 2. *The configuration menu for the Microprogram Development Subsystem shows the flexibility available with Run Control.*

The Run Control module provides 20 I/O lines to probe the address bus, monitor status bits, or drive control lines. These I/O lines are bused internally to the Writable Control Store and the state analysis data probe connectors on the Run Control module.

Both single lead or coaxial cable leads are supplied for probing the clock and control lines between the target system and the Run Control module. Coaxial leads are recommended for use with higher clock rates to ensure better signal quality.

Clock Control

Precise specification of clock edges and relationships is critical for breaking or halting the clock in target systems with multiple clock signals. The Run Control module allows you to specify complex clock signal characteristics for use in break events (figure 3).

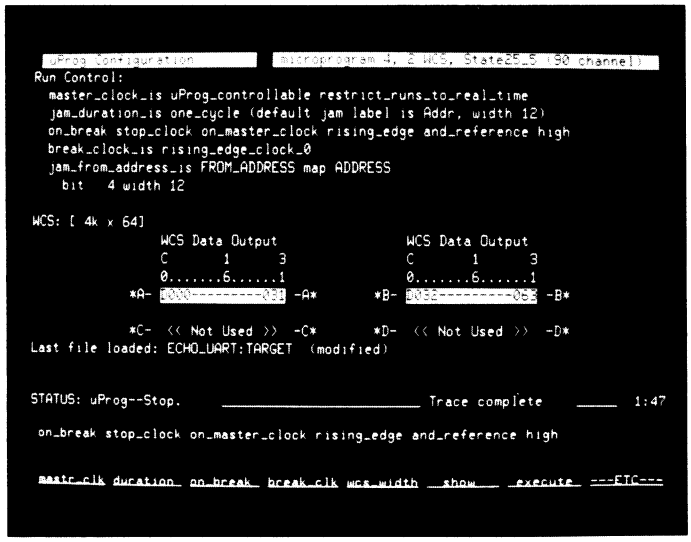

Figure 3. *The Run Control Module allows you to specify complex clock signal characteristics for use in break events.*

Address Jamming

Address jamming forces program execution at a specific address if a starting point other than a system reset vector location is desired. For example, to force the execution of a monitor routine that displays the registers, an address is jammed onto the address bus, causing the program to jump to the monitor routine. With the HP 64276 Microprogram Development Subsystem, you can jam either 8, 12, 16, or 20 address lines.

Break Events

The HP 64276 allows you to initiate a break event after the detection of any of the following occurrences: an address pattern (up to four can be specified), an address range, or a two-term sequence of an address pattern, range, or both. The state analysis trigger also can enable break event detection. When a break event occurs, an address can be jammed onto the address bus (e.g., to a monitor program) or the system clock can be stopped (figure 4).

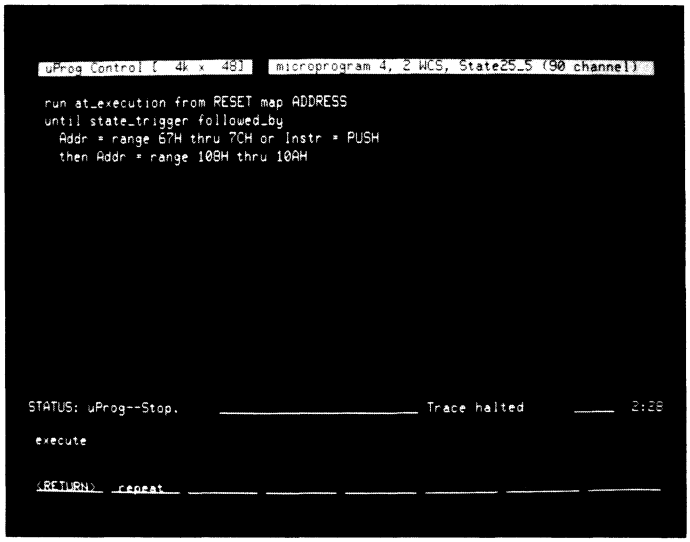

Figure 4. *Complex break events can be specified using patterns, ranges, or sequences. When a break event occurs, an address can be jammed onto the address bus, or the system clock can be stopped.*

Writable Control Store

The Writable Control Store (WCS), the memory array for the system microcode, consists of a dual port RAM that allows easy microcode downloading from the assembly environment and high-speed access of the microcode by the microprogram target system. Target system development and debugging is more efficient using the WCS instead of the target system control store.

Architecture

The Writable Control Store (WCS) contains either one or two 32 kbyte memory boards. Each board can be configured into one of three array sizes: (bits wide by words deep) 16 by 16k, 32 by 8k, or 64 by 4k. With two WCS boards in the subsystem, the microword widths are doubled.

The WCS address is obtained from the Run Control module, eliminating the need to probe the target system a second time. By using one of the WCS address lines as an enable control to tristate the WCS output, you can toggle between target memory and subsystem memory.

Load

Once microcode has been assembled and linked, it is downloaded from the software development environment to the Writable Control Store for execution. Transferring microcode is fast and easy with the integrated development and hardware execution environments of the Microprogram Development Subsystem.

List

When debugging microcode, you can examine the contents of the WCS and list them to a destination file, a printer, or a display. A single list command specifies from one to four addresses or groups of contiguous WCS addresses. Displaying the address ranges allows you to examine and compare the microcode in different subroutines (figure 5).

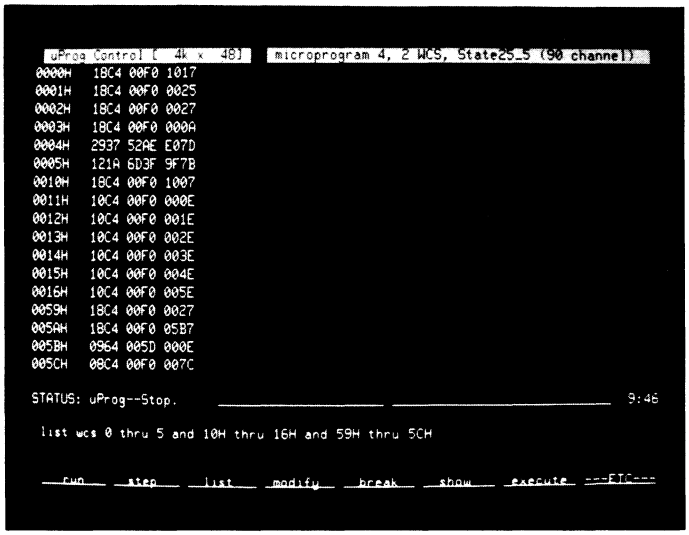

Figure 5. *Four different WCS address ranges may be displayed at one time.*

Modify

While debugging, you can modify the absolute code and continue debugging (figure 6). Modify can be specified for up to 32 bits at a time for either a single WCS address or a range of addresses.

Save

The absolute code stored in WCS can be saved to a disc file for later reloading or for verifying the correctness of changes to source microcode.

User-defined

You can design a custom WCS array and combine it with the other modules of the Microprogram Development Subsystem. The combination of the HP 64000 Logic Development System, the HP 64276 Run Control, and the user-defined WCS array provides an integrated development solution for all micro-program target systems.

The user-defined WCS interface supports any array size between 16 by 512k and 1024 by 8k (bits wide by words deep). The interface between the HP 64000 mainframe and the user-definable WCS consists of control lines and parallel address and data buses that allow data to be written to, or read from, the WCS. User-definable control sequences can be transmitted to the user's WCS preceding and following an upload or download operation.

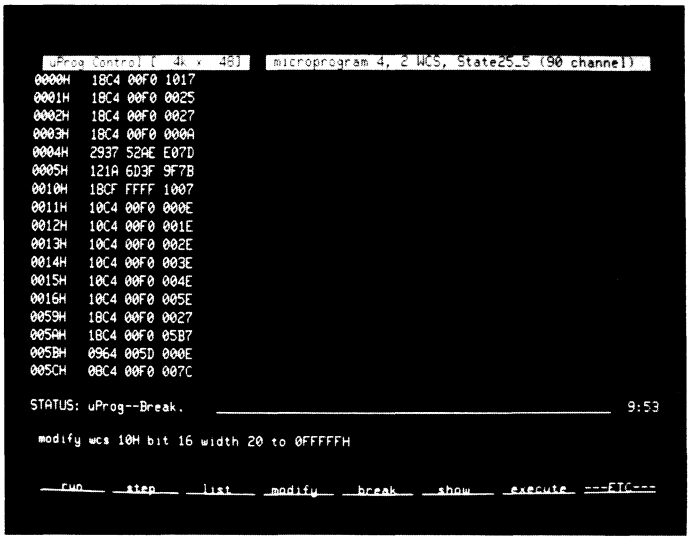

Figure 6. *Up to 32 bits of a microword may be modified at one time for a single address or a range of addresses.*

25 MHz Logic State/Software Analyzer

The HP 64320S 25 MHz Logic State/Software Analyzer adds high-speed, real-time, nonintrusive software analysis to the HP 64000 Logic Development System. This flexible analyzer works well in microprogram software analysis, general-purpose software analysis, and system integration.

Measurement results are displayed in source microcode (including MACROs and comment lines) or in user-defined symbols that minimize the need to decode captured data. The analyzer can also reference symbols from the microprogram source files for easy specification and interpretation.

Architecture

The analyzer can be configured for 30, 60, or 90 channels of data acquisition. Each configuration must have a control card and from one to three data acquisition cards containing 30 data acquisition channels. The following table contains the analyzer's configurations.

number of input channels	control cards	30-channel cards
30	1	1
60	1	2
90	1	3

Format Specification

The Format Specification establishes the conditions and relationships of target system signals transmitted to the analyzer through the clock and data input channels (figure 7). User-defined labels up to fifteen characters long can be assigned to signal groups from one to 32 contiguous channels wide. Saving the Format Specification to the disc eliminates respecifying data channel labels, threshold levels, and clock characteristics each time the analyzer is used. After a label is assigned to a group of input channels, it also appears on the analyzer softkeys.

To avoid confusion caused when both positive and negative true data are present in the system under test, the 25 MHz analyzer can automatically complement any group of data channels. You do not need to invert these signals on the target system or complement data as measurements are specified and results are interpreted.

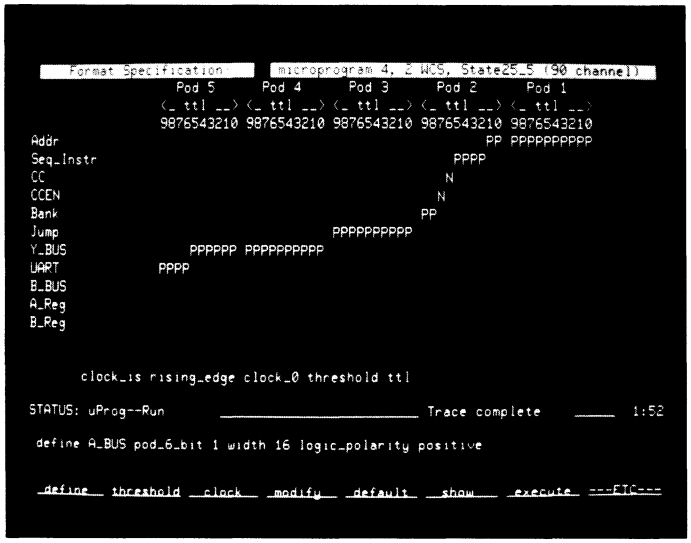

Figure 7. *Clock and data input channels can be assigned labels, threshold levels, and clock characteristics.*

The analyzer has two separate clock inputs. Data can be captured on the positive and negative edges of both clocks. With two clocks, you can analyze systems with multiple CPUs by capturing data on each processor's address strobe signal.

Data and clock signal switching threshold voltages can also be varied. Appropriate thresholds for TTL and ECL logic families have been preprogrammed. You can also select other values between −10 and +10 volts, in 100 mV increments for monitoring several different logic families. Independent threshold specifications can be made for each acquisition board (30 data channels).

Map Specification

The Map Specification greatly simplifies measurement setups and trace data interpretation by replacing raw captured data with user-defined symbols (figure 8). A "symbol map" can be associated with any labeled input channel via the Format Specification. Entries in a symbol map appear as part of the analyzer's softkey syntax and in the displays of measurement results. Map symbols are defined as constants, patterns, or ranges. A map symbol can be defined in terms of source file line numbers or user-symbols from microprogram source files.

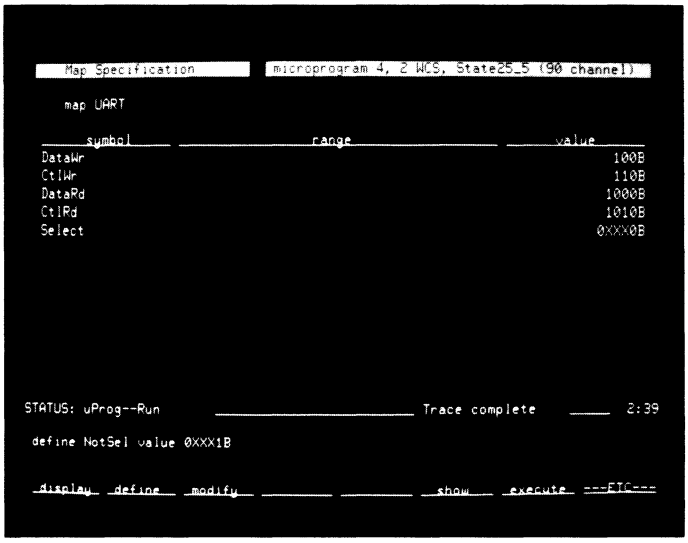

Figure 8. *User-defined symbols can be assigned to values or ranges. These symbols can then be used in trace measurement setups and displays.*

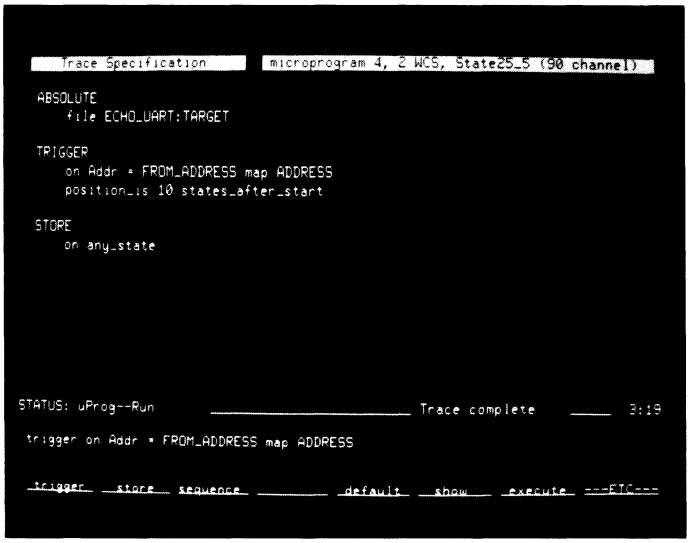

Figure 9. *The trigger function determines WHEN the analyzer will capture data.*

Trace Specification

The Trigger function determines WHEN the analyzer will capture data (figure 9). Complex triggering conditions can be implemented using sequence terms. A "term" is defined as "AND'ed" constants and patterns. A constant can be an integer, map symbol, or symbol from the microprogram source file. A

pattern is an integer with embedded "don't cares" (e.g., 0100xxxxB). Four sequence terms (trigger being the fourth) are available. Each sequence term can be set up to occur from 1 to 65 536 times before it is satisfied. A restart term is also available for resetting the sequencer (figure 10).

The Trigger Enable function specifies when the analyzer monitors data for a trigger event. The trigger event can be stored anywhere within the trace memory buffer, allowing trace data to be stored either preceding, surrounding, or following the trigger event.

The Store function determines WHAT data should be stored (figure 11). You can specify up to four OR'ed terms with each term consisting of AND'ed constants and patterns. When the restart term is used for sequencing, the maximum number of OR'ed terms is three. The optional store with "sequence protect" specifies that the sequence events be saved before any pre-trigger events are stored.

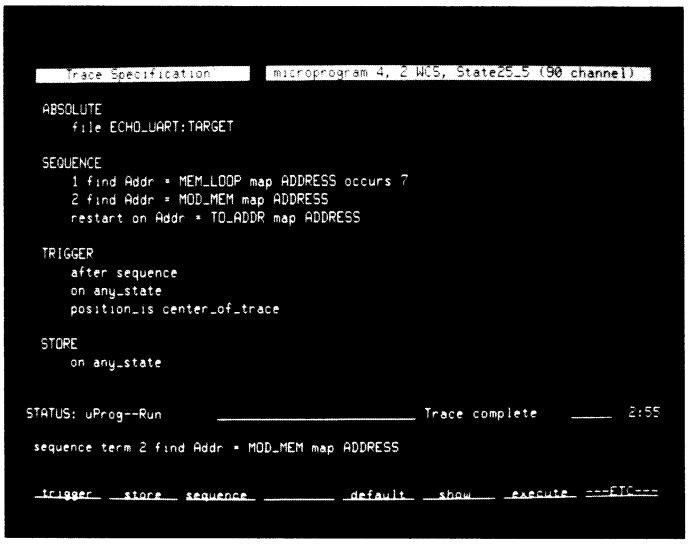

Figure 10. *Complex triggering conditions can be implemented using sequence terms. Each sequence term can be set up to occur from 1 to 65 536 times before it is satisfied.*

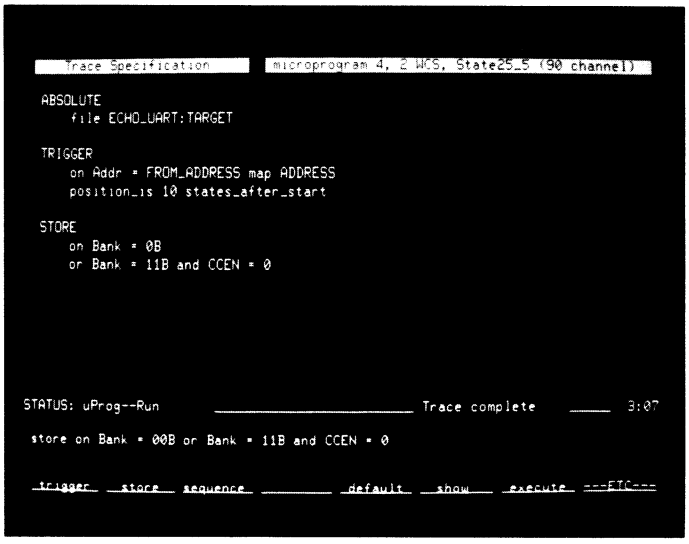

Figure 11. *Four OR'ed terms may be specified to determine WHAT data should be stored.*

Measurement Results

The HP 64320S 25 MHz Logic State/Software Analyzer provides a high degree of display flexibility. When using source display, the microcode is visible without having to probe the microword: microword fields, MACRO invocations, and comments from source files are displayed. The display shows these source level statements combined with target data probed by the analyzer (figure 12). This combination of program and data makes microcode debug more productive and efficient. Displays can also include user-defined symbols specified in the symbol maps and can automatically reference microassembler symbol tables generated during software development. These symbols can be displayed in the trace listings (figure 13).

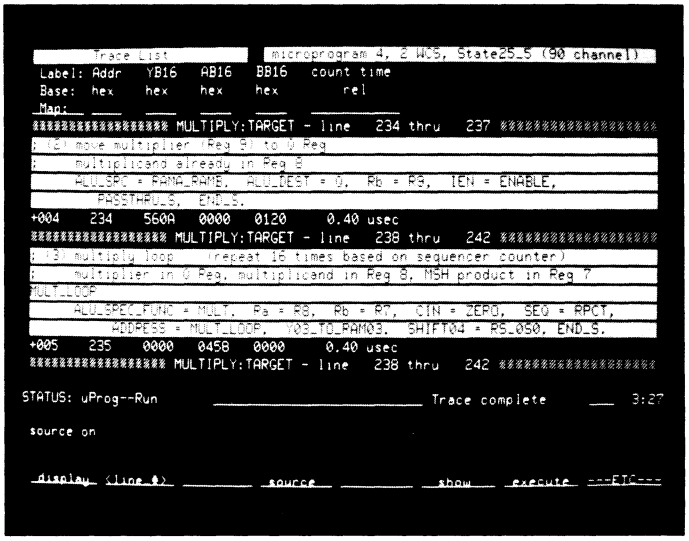

Figure 12. *Microcode source interleaved with trace data provides for very efficient debugging.*

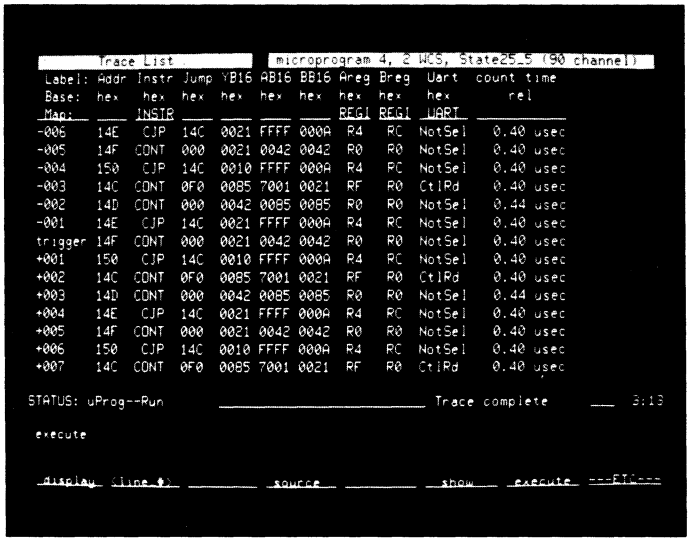

Figure 13. *User-defined map symbols displayed in trace data simplify microprogram debugging.*

Flexible Probing Capability

The HP 64320S analyzer's clock cable and two of its data probes plug directly into the HP 64276 Microprogram Development Subsystem to eliminate double probing of the target system. Run Control, WCS, and the other state analysis data probes connect to the target system by general-purpose wire grabbers or D-type coaxial cables. The coaxial cables offer better high-frequency signal quality and a more reliable connection to the target system.

Measurements Involving Multiple Analyzers

Measurements with the HP 64320S and other HP 64000 analysis subsystems relate microcode execution to other software and hardware events. These interactive measurements are conducted via the high-speed intermodule bus (IMB). The IMB carries the following five signals between the analysis subsystems:

IMB Signal	Received by HP 64320S	Driven by HP 64320S
Master Enable	yes	yes
Trigger Enable	yes	yes
Trigger	yes	yes
Storage Enable	yes	no
Delay Clock	no	yes

The Master Enable signal coordinates measurement starts with other analyzers and emulators. When the analyzer is set up to receive this signal, and the Master Enable is "false," the analyzer is completely disabled and will not capture data. When Master Enable becomes "true," the analyzer begins examining data.

The Trigger Enable operates in the same way as Master Enable by informing the receiving analysis module when it can begin looking for its trigger condition.

The Trigger signal, when received, causes the analyzer to immediately trigger and complete its measurement. For example, this is valuable for using the HP 64610S High-speed Timing/State Analyzer in conjunction with the 25 MHz Logic State/Software Analyzer to determine if a spurious signal pulse is related to a microcode event. By triggering the 25 MHz analyzer on a hardware event, the microcode execution surrounding the pulse is quickly pinpointed and evaluated (figure 14).

The Storage Enable signal exercises hierarchical control over the store specification.

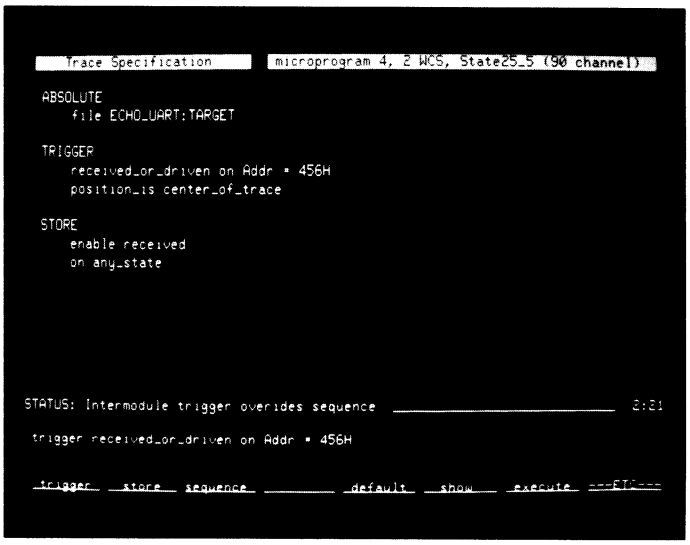

Figure 14. *Cross-triggering capabilities allow interactive measurements with the many other HP 64000 analysis and emulation subsystems.*

Microassembler

The HP 64276 Microprogram Development Subsystem includes a user-definable microassembler and linker capable of generating microwords up to 128 bits in width. The microassembler supports a wide range of microprogrammable devices. The linker allows assembly of separate modules, reducing turn-around time for source microcode changes.

The definition language operates on a 32 bit, 40 register pseudo-machine with standard instructions for the movement and manipulation of data. In addition, higher level commands for standard tasks are also provided (i.e., commands such as GET_TOKEN, FIND_DELIMITER, and GET_OPCODE support lexical analysis). The user-definable microassembler can also generate relocatable code with the use of the GEN_CODE command. The ERROR and WARNING commands print messages from a fixed table to the listing file to simplify error detection and correction. Field names and their values are easily specified (e.g., SEQ = CONT).

The definition language is powerful enough to allow the creation of a customized microassembler capable of:

- Generating code
- Specifying default values for missing fields
- Issuing errors for missing fields not having a default value
- Issuing errors for overlapping field definitions
- Issuing errors and warnings for architectural inconsistencies, such as a microinstruction that could cause bus contention

The resulting customized microassembler recognizes the syntax specified in the definition stage. Standard capabilities are predefined for the microassembler and need not be explicitly specified in the definition stage. For example, standard pseudo-ops are provided for storage allocation, location counter control, and listing format control. In addition, a powerful MACRO facility is supported.

Specifications and Ordering Information

25 MHz Logic State/Software Analyzer (HP 64320S)

Clock Inputs

Clock Channels: 2 edge-sensitive clocks.
Resistance: approx 100 kohm.
Capacitance: approx 5 pF at probe tip.
Input Voltage: −40 Vdc to +40 Vdc.
Dynamic Voltage Range: threshold voltage +10 Vdc to −10 Vdc.
Thresholds: software programmable from −10 Vdc to +10 Vdc in 100 mV increments.
Clock Rate: up to 25 MHz.
Clock Pulse Width: 10 ns minimum.

Data Inputs

Data Channels: 30, 60, or 90 input channels.
Resistance: approx 100 kohms.
Capacitance: approx 5 pF at probe tip.
Input Voltage: −40 Vdc to +40 Vdc.
Dynamic Voltage Range: threshold voltage +10 Vdc to −10 Vdc.
Thresholds: software programmable from −10 Vdc to +10 Vdc in 100 mV increments.
Data Setup Time: valid data must be present at least 20 ns prior to the active clock edge.
Data Hold Time: zero.

Analyzer Outputs

General Signal Characteristics: TTL pulse with programmable polarity.
BNC Port 1 (Active for any event satisfying the trigger condition).
BNC Port 2 (Active only for the first trigger condition).

Measurement Functions

Data Depth: 256 states.
Data Width: 30, 60, or 90 channels.
Sequence Terms: 4.
Occurrence Count: 65 536 max.
Time Stamping Interval: 40 ns.
Map Symbols: 127 max.
Store Qualification: 4 terms, 3 with restart sequence.

Writable Control Store

Memory Specifications

Memory Per Board: 32 kbytes.
Memory Array Sizes: softkey selectable array sizes (bits wide by words deep) 16 by 16k, 32 by 8k, or 64 by 4k.
Memory Array Sizes (two WCS cards): softkey selectable array sizes (bits wide by words deep) 16 by 32k*, 32 by 16k, 64 by 8k, or 128 by 4k.
Maximum Access Time (measured at connectors on HP 64276 module): 50 ns.
Address Disable (A19 control line): 47 ns.
Data Hold Time After Address Change: 9 ns.

*WCS array of 16 by 32k requires a special cable for connection to the target. This cable is supplied with the HP 64276C and the HP 64275A.

Supplemental Information

Data Output (Drive Capability): High 3 mA, Low 12.8 mA.

User WCS

Memory Array Sizes: (bits wide by words deep) 16 by 512k, 32 by 256k, 64 by 128k, 128 by 64k, 256 by 32k, 512 by 16k or 1024 by 8k.
User-definable Control Sequences: yes.

Run Control

Specifications

Sequencing: two terms.
Breakpoints: four Or'ed terms or one address range.
I/O lines: 20.
Lines Jammed: 8, 12, 16, or 20.
Clock Start/Stop On Command
  Master Clock rate: 50 MHz.
Clock Stop On Pattern (Before next microcycle)
  Microinstruction rate: 25 MHz.
Address Jamming (No clock pause)
  Microinstruction rate with HP 64275A WCS: 10 MHz.
  Microinstruction rate with user WCS (access time less than 27 ns): 13 MHz.

Supplemental Information

Address Output (Drive Capability): High −8 mA, Low 30 mA.
Address Input (load): High 20 μA, Low −1.6 mA.
Clock and Clock Control Output (Drive Capability): High −1 mA, Low 15 mA.
Clock Inputs:
  Resistance: 50 kohms.
  Capacitance (coaxial): 10 pF.
  Capacitance (wire): 14 pF.

Environmental

Temperature: operating, 0° to +40°C (32° to 104°F); nonoperating, −40° to 75°C (−40° to 167°F).
Altitude: operating, 4600 m (15 000 ft); nonoperating, 15 300 m (50 000 ft).
Relative Humidity: up to 95% at +40°C, noncondensing.

Power Requirements

Module	+5V	−5V	+12V	−12V	−3V
State Control	1.7 A	3.2 A	6 mA	9 mA	1.9 A
State Acquisition	1.4 A	3.3 A	9 mA	14 mA	1.5 A
Run Control	1.3 A	2.1 A	0.1 A	0.8 A	—
WCS	3.5 A	—	—	—	—
User WCS Control	0.1 A	—	—	—	—

Microassembler

Specifications

MACRO Support: yes.
Word Width: up to 128 bits wide.
Field Width: 32 bits max.
Relocatable code generated: yes.
Linker: yes.
Source Display With HP 64320S: yes, with user-defined Host Pascal Utility.
Definition on Host Computer: no.
User-defined Assembler on Host Computer: yes.

Ordering Information

Model	Description
64320S*	**30-channel 25 MHz Logic State/Software Analyzer**
Opt 010	**60-channel 25 MHz Logic State/Software Analyzer**
Opt 011	**90-channel 25 MHz Logic State/Software Analyzer**
64276A	**Run Control**
64276B	**Run Control with 32 kbytes WCS**
64276C	**Run Control with 64 kbytes WCS**
64861A	**User-definable Microassembler**

Components

64321A*	**25 MHz State Analyzer Control Card**
64321AX	**One-time Update** (25 MHz Logic State Analyzer software)
64322A*	**30-channel 25 MHz State Acquisition Board**
64324A*	**10-channel 25 MHz State Data Probe**
64325A*	**25 MHz State Clock Probe**
64275A	**32 kbyte WCS Board**
64276AX**	**One-time Update** (run control software)
64277A	**User-defined WCS control card**
64277AX	**One-time Update** (user WCS control software)
64861AR	**Right-to-copy** (microassembler software)
64861AX	**One-time Update**
64964A	**IMB Cable**

Note: The memory expansion board (HP 64032A) is required for use of the HP 64276 and/or the HP 64320S in any HP 64100/64110 station with a serial number prefix less than 2309A. The necessary memory is standard on stations with higher serial numbers.

*State Probes (HP 64324A and HP 64325A) are included in HP 64320S, 64321A, 64322A products and do not have to be ordered separately except as individual replacement probes.

**One-time software update is the same for any of the Microprogram Development Subsystem configurations. If you have the HP 64276A, 64276B, or 64276C, order the HP 64276AX for the one-time software update.

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Data subject to change.

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