64000

HP64000 Logic Development System

Model 64302A Wide Logic Analyzer

HEWLETT PACKARD

CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY

This Hewlett-Packard system product is warranted against defects in materials and workmanship for a period of 90 days from date of installation. During the warranty period, HP will, at its options, either repair or replace products which prove to be defective.

Warranty service of this product will be performed at Buyer's facility at no charge within HP service travel areas. Outside HP service travel areas, warranty service will be performed at Buyer's facility only upon HP's prior agreement and Buyer shall pay HP's round trip travel expenses. In all other cases, products must be returned to a service facility designated by HP.

For products returned to HP for warranty service. Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instructions when properly installed on that instrument. HP does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted or error free.

LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. HP SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

EXCLUSIVE REMEDIES

THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. HP SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

ASSISTANCE

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

CW&A 2/81

HEWLETT-PACKARD

SERVICE MANUAL

MODEL 64302A

WIDE LOGIC ANALYZER

REPAIR NUMBERS

This manual applies directly to models with repair numbers prefixed 2139A.

With changes described in Section VII, this manual also applies to repair numbers prefixed 2133A.

Manual Part Number: 64302-90902
Microfiche Part Number: 64302-90802

PRINTED: MAY 1982

SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements.

GROUND THE INSTRUMENT.

To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting.

SS-1-1/76

QUICK REFERENCE GUIDE - 64302A WIDE LOGIC ANALYZER

OPERATION.

The wide logic analyzer operates in two modes: HALT and RUN. During the HALT mode the analyzer is configured by the mainframe processor to trigger on a certain trace specification. During the RUN mode the analyzer is released to monitor the emulation bus for the configured trace specification.

When using an 8-bit emulator, an analyzer is an option; but, when using a 16-bit emulator, the wide logic analyzer is required. If, when using an 8-bit emulator, an analyzer is NOT detected in the mainframe card cage, the trace defaults to software analysis, ie. non-real time analysis.

PERFORMANCE VERIFICATION.

When the wide logic analyzer is selected under option_test PV, the following tests are displayed:

HALT MODE....configures RAMS, flip-flops, and counters and then checks to see if this occurred correctly. No emulator connection is required.

RUN MODE.....configures the board for a certain trace specification and releases it to run. Data being monitored is supplied by the mainframe processor. No emulator connection is required.

IMB.....checks communication of enabling and triggering information. For Internal IMB tests no other board is needed. For External IMB tests another wide logic analyzer is required. In either case, no emulator connection is required.

EMULATOR.....checks the emulator subsystem and the analyzer. This test
STIMULUS is only displayed when the emulators shown below are in the card cage:

8080, 8085, Z80, 6800, or 6802.

For other emulators, this type of test is contained within the emulator option_test PV.

TIME/STATE...checks the 24-bit Time/State Counter and is similar to
COUNTER tests in the HALT MODE. This test is separate because it requires about one minute to run. No emulator connection is required.

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SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This service manual contains information required to install, test and service the Hewlett-Packard Model 64302A Wide Logic Analyzer. Operating instructions are provided in a separate operating manual supplied with the instrument. It should be kept with the instrument for use by the operator.

1-3. Shown on the title page is a microfiche part number. This number can be used to order 4X6-inch microfilm transparencies of the manual. Each microfiche contains up to 96 photoduplicates of the manual pages.

1-4. INSTRUMENTS COVERED BY THIS MANUAL.

1-5. Attached to the instrument or printed on the printed circuit board is the repair number. The repair number is in the form: 0000A0000. It is in two parts; the first four digits and the letter are the repair prefix, and the last four are the suffix. The prefix is the same for all identical instruments. The suffix, however, is assigned sequentially and is different for each instrument. The contents of this manual apply to instruments with the repair number prefix(es) listed under REPAIR NUMBERS on the title page.

1-6. An instrument manufactured after the printing of this manual may have a repair number prefix that is not listed on the title page. This unlisted repair number prefix indicates that the instrument is different from those described in this manual. The manual for this newer instrument is accompanied by a Manual Changes supplement. This supplement contains change information that explains how to adapt the manual for the newer instrument.

1-7. In addition to change information, the supplement contains information for correcting errors in the manual. To keep this manual as current as possible, Hewlett-Packard recommends that you periodically request the latest Manual Changes supplement. The supplement for this manual is identified with the manual print date and part number, both of which appear on the manual title page. Copies of the supplement are available from Hewlett-Packard.

1-8. For information concerning a repair number prefix that is not listed on the title page or in the Manual Changes supplement, contact your nearest Hewlett-Packard office.

1-9. DESCRIPTION.

1-10. The Hewlett-Packard Model 64302A Wide Logic Analyzer provides logic analysis for 16 and 8 bit emulators in the 64000 Logic Development System. The entire analyzer is contained on one printed circuit

board that fits in the mainframe's card cage (figure 2-2).

1-11. It simultaneously captures address, data, and control states from the emulated target processor via the emulation bus and is capable of storing the states as 256, 48 bit words. The analyzer is also capable of displaying the information on the mainframe CRT in easy to read mnemonic format. The wide logic analyzer has the ability to specify trace points in combinations of address, data, and status, making the wide logic analyzer a valuable addition for debugging the target system's hardware and software.

Table 1-1. Specifications

Power dissipation 22.2 watts (typical). Board ID 0102H.

Power up configuration:
- No IMB lines driven, except Gated Master Clock.
- IMB configuration invalid.
- BNC1 and BNC2 not driven.

Storage capabilities:
- Pre-store, post-store and combination pre/post-store.
- 256, 48 bit words at a maximum 6 MHz acquisition rate.
  - 48 Parallel channels.
    - 24 Emulator address bits.
    - 16 Emulator data bits.
    - 8 Emulator control bits.
  - 24 Count bits.
    - State (number of occurrences), or
    - Time (time measurement between states).

Break capabilities:
- Trace Point and Measurement Complete.
- Time to break 165 ns maximum.

Indexing capabilities:
- Eight modes using Range, AME1, AME2 and Count Qualify signals. Range is 24 bit emulator address in 1, 0, or X (don't care). Others are 48 bit emulator bus in 1, 0, or X.

Analysis clock cycle time 165 ns minimum.

Trigger on Nth occurrence, N = 1 to 65,535.

Inter Module Bus (IMB) capabilities:
- Receive and drive Master Enable.
- Receive or drive Trigger Enable.
- Receive and/or drive Trigger.
- Drive Gated Master Clock.

1-12. The wide logic analyzer communicates with the following areas of the 64000 Logic Development System.

Table 1-2. Analyzer I/O

Emulator Bus: Monitors the address, data, and control lines of the target microprocessor. Generates emulation break.
Mainframe Bus: Sends and receives control commands to and from the mainframe's central processing unit (CPU). At the CPU's request, sends all stored information to the CPU to be formated and displayed.
Inter Module Bus (IMB): Sends and receives control signals to other modules.
Output Ports: Places pulse on Port 1 BNC connector when trigger is encountered. Places pulse on Port 2 BNC connector when measurement is complete.

1-13. REAL TIME ANALYSIS

1-14. The wide logic analyzer does not work with all emulators, because the software does not recognize the analyzer. Table 1-3 shows emulator compatibility.

1-15. LEVEL OF SERVICE.

1-16. This is a final component-level manual. It contains information that provides component-level servicing of the Model 64302A. Detailed schematics and parts lists are provided to assist in the servicing of the board.

1-17. CONVENTIONS.

1-18. The following conventions are used in the text and schematics.

a. Component designators are assigned according to the upper left to lower right method.

b. Logic symbology, see table 8-2.

c. Logic levels (in volts):

	Input high threshold	Input low threshold	Output high threshold	Output low threshold
TTL	+2.0	+0.8	+2.4	+0.2
ECL	-1.1	-1.5	-1.1	-1.5

d. Mnemonics (signal names); see table 8-1.

The letters to the left of the slash (/) indicate the electrical status of the signal. The letters to the right of the slash show the signal function. For example, L/STB is low/strobe. Typical status indicators are:

L=low, or latched, H=high, B=buffered, E=ECL

Both TTL and ECL level signals are used. The ECL signal mnemonics have an E in the electrical status. For example, EL/ANAL is the ECL version of the TTL signal L/ANAL. Mnemonics that do not have electrical status are assumed to be TTL and have no predominant active level. For example, POL is a polarity signal.

e. Abbreviations, see table 6-1.

f. Softkeys are indicated by arrow brackets, while normal keys are shown in square brackets. For example, <stop> indicates the software labeled stop key, while [RETURN] indicates the keyboard labeled return key.

Table 1-3. Analyzer/Emulator Compatibility

Emulator	Compatible with Wide Logic Analyzer
8080	No
8085	No
Z80	No
6800	No
6802	No
68000	Yes
8086	Yes
8088	Yes
Z8001	Yes
Z8002	Yes
6809	No
8048	No

SECTION II

INSTALLATION

2-1. INTRODUCTION.

2-2. This section contains information for installing and removing the Model 64302A. Included are initial inspection procedures and instructions for repacking the instrument for shipment.

2-3. INITIAL INSPECTION.

2-4. Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until contents of the shipment have been checked for completeness and the instrument has been checked mechanically and electrically. Procedures for checking electrical performance are given in Section IV. If the contents are complete, if there is mechanical damage or defect, or if the instrument does not pass the performance tests, notify the nearest Hewlett-Packard office. If the shipping container is damaged, or if the cushioning material shows signs of stress, notify the carrier as well as the Hewlett-Packard office. Keep the shipping materials for carrier's inspection. The HP office will arrange for repair or replacement at HP's option without waiting for claim settlement.

2-5. MAINFRAME CONFIGURATION.

2-6. The wide logic analyzer must be installed next to the emulator control card to allow the emulator bus to be connected to it. Board order, from highest slot number to lowest, is shown below.

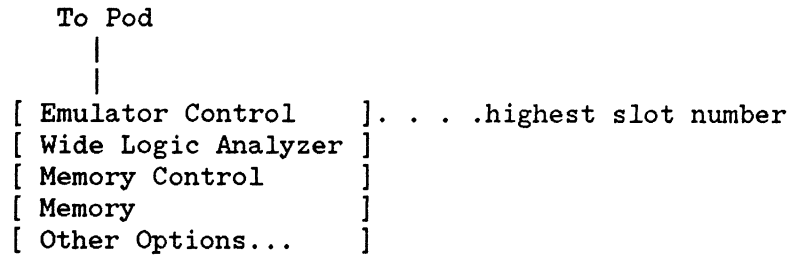


Figure 2-1. Mainframe Card Cage

```
********************  CAUTION  ********************
*                                                 *
*  The  Model 64302A Wide Logic Analyzer  must    *
*  be installed and removed with the mainframe    *
*  power turned off.                              *
*                                                 *
***************************************************
```

2-7. INSTALLATION.

2-8. To install the wide logic analyzer board proceed as follows:

a. Be certain that the emulator control board and the emulator pod are installed. If they aren't this must be done. (See the emulator control and emulator pod service manuals.)

b. Leave a slot open next to the component side of the emulator control board.

c. Insert the analyzer board into the open slot next to the emulator control board. Insure that it is completely seated in the motherboard connector.

d. Install the emulator bus cables (two 50 pin ribbon connectors) to interconnect the emulator control board, the analyzer board, and the memory control board (if present).

e. The inter module bus (IMB) of the analyzer board may not be connected. If used, it is connected to another option card.

2-9. REMOVAL.

2-10. To remove the wide logic analyzer proceed as follows:

a. Remove the card cage cover. Position the mainframe so there is clear access to the card cage.

b. Locate the analyzer board. The extraction tabs on the analyzer board are labeled WD. ANL and 64302A.

c. Remove the two 50 pin ribbon cables (emulator bus) and the inter module bus (IMB) cable.

d. Unseat the analyzer board by lifting up the outside edges of the extractor tabs.

e. The wide logic analyzer board may now be removed by sliding it out of the card cage slot.

Figure 2-2. Model 64302A Wide Logic Analyzer

SECTION III

OPERATION

The operation of the 64302A is a function of the system software. Complete operation from the keyboard of the system is beyond the scope of the service manual. Please refer to the operator's manuals for the procedures.

SECTION IV

PERFORMANCE TESTS

4-1. INTRODUCTION.

4-2. This section describes the performance verification (PV) for the Model 64302A Wide Logic Analyzer. It also includes information on how to use PV results in conjunction with signature analysis to troubleshoot to component level. Signature analysis tables are located in Appendices A through F.

4-3. SYSTEM CONSIDERATIONS.

4-4. Failure isolation must be performed to eliminate other sections of the Logic Development System as the source of the failure. It is assumed in this manual that the mainframe PV has been successfully conducted and that other option cards have also been checked. It is also assumed that the target system being emulated has been disconnected from the emulator, thus eliminating it as a possible source of the failure.

4-5. EMULATOR/ANALYZER PV COMPATIBILITY.

4-6. The Emulator Stimulus and Analysis Stimulus Tests verify that the analyzer board can collect data from the emulator. During these tests the emulator places data onto the emulation bus and the analyzer is set up for a 'don't care trigger' and is released to run. The data contained in the analyzer RAMs is unloaded and checked against a table. Any discrepency is indicated as a failure in the appropriate bit position. Tables 4-1 and 4-2 show compatibility between the analyzer and various emulators.

4-7. Emulator Stimulus Testing.

4-8. The only analyzer PV test which requires an emulator is the Emulator Stimulus Test. All other analyzer PV tests should be performed without the emulation bus cables attached, in other words, with the analyzer connected only to the motherboard. In this configuration more than 90% of the board is checked out.

4-9. The Emulator Stimulus Test is a complete emulation subsystem checkout rather than a test which checks out the analyzer only. But, assuming that the emulator is operating correctly, the Emulation Stimulus Test can be used to check out the emulation bus latches; U12, 8, 10, 14, 16, 18. It also checks out the word/byte select circuitry and U96 which is enabled during data byte operations.

Table 4-1. Analyzer Emulator Stimulus Test Compatibility

Does the analysis PV display an Emulator Stimulus Test and does that test run ?	
Emulator	Wide Logic Analyzer
8080	Test displayed & runs
8085	Test displayed & runs
Z80	Test displayed & runs
6800	Displayed but doesn't run
6802	Displayed but doesn't run
68000	Test not displayed
8086	Test not displayed
8088	Test not displayed
Z8001	Test not displayed
Z8002	Test not displayed
6809	Test not displayed
8048	Test not displayed

Table 4-2. Emulator Analysis Stimulus Test Compatibility

Does the emulator PV display an Analysis Stimulus Test and does that test run?	
Emulator	Wide Logic Analyzer
8080	Test not displayed
8085	Test not displayed
Z80	Test not displayed
6800	Displayed but doesn't run
6802	Displayed but doesn't run
68000	Test displayed & runs
8086	Test displayed & runs
8088	Test displayed & runs
Z8001	Test displayed & runs
Z8002	Test displayed & runs
6809	Test not displayed
8048	Displayed but doesn't run

4-10. Also checked in the Emulator Stimulus Test is the timing circuitry which is synchronized to L/ANAL, the valid-data signal coming from the emulator. This circuitry is not tested during any of the other analyzer PV tests. During these other tests, trace data is supplied by the mainframe processor rather than by the emulator.

4-11. Analysis Stimulus Test.

4-12. Within some of the emulator's PV there is an Analysis Stimulus Test which does some of the same tests as the Emulator Stimulus Test. Here the same circuitry as listed above is checked. For more detail, refer to the paragraphs on Analysis Stimulus Test Display in this section.

4-13. PERFORMANCE VERIFICATION TESTS.

4-14. The performance verification for the wide logic analyzer is a subsection of the system Option Test Performance Verification. The system level PV tests all option modules that are located in the mainframe card cage. The following paragraphs describe how to perform the wide logic analyzer PV and what is checked.

4-15. REQUIRED EQUIPMENT.

a. Logic development system mainframe with most recent PV software.

b. To test IMB external stimulus, another wide logic analyzer is required.

c. To test 8 bit emulator stimulus an 8 bit emulator and memory controller are required. The 16 bit emulator stimulus is performed by the emulator PV.

d. To print PV results, a printer must be attached to the system.

4-16. PERFORMANCE VERIFICATION FOR COMPONENT-LEVEL REPAIR.

4-17. Generally, the 64302A PV is sequenced so that complex tests follow simple tests. That is, the tests build on each other. When a test fails, it is almost certain that later tests will fail. So, when a failure is indicated while cycling through all the tests, select the Halt Mode Control Logic Tests and proceed from there.

4-18. Signature analysis tables are provided (in the appendices) for most tests along with a suggested list of IC's to check. A description of what the test is doing is also included. Tests, such as the Emulator Stimulus Test and the External Stimulus IMB Test, cannot support signature analysis. The Counting Time and States Test does not include signature analysis. However, the counting state function control circuitry is tested as a subtest of the Run Mode Tests. The SA loops are:

LOOP A...Halt Mode, Control Logic Tests
LOOP B...Halt Mode, Storage Ram Tests
LOOP C...Halt Mode, Index Ram Data Tests
LOOP D...Halt Mode, Index Ram Address Tests
LOOP E...Run Mode Tests
LOOP F...IMB, Internal Stimulus Tests

4-19. When taking signatures, keep track of which IC's have been checked, because many IC's are checked in more than one test; in particular, the host processor's latches and buffers. These IC's are:

```
Host CPU control latches....U108, 109.
Control buffers.............U111, 113.
Host CPU Status Buffers.....U77, 112.
Host CPU Read Buffers.......U114, 112, 80.
```

```
********************  NOTE  ********************
*                                               *
*  Signatures on U108, 109, 111, and 113 can    *
*  be incorrect when there is a fault on the    *
*  board. The fault is indicated to the main-   *
*  frame via U112 and U114, which are simul-    *
*  taneously monitored by the chips listed      *
*  above.                                       *
*                                               *
************************************************
```

4-20. Sometimes, when taking signatures on the suggested chip, a bad signature is found that leads to a long string of bad signatures. The path may lead to the faulty node, but only after a considerable number of signatures. If it seems this is occurring, stop, and check signatures on the next chip given in the suggested chips to check.

4-21. During a trace, the signal L/ANAL from the emulator, is the synchronizing clock for the analyzer. During performance verification L/ANAL is disabled and the synchronizing clock is supplied by the mainframe host processor. In the following text, this signal is called a 'PV strobe'.

4-22. STARTING PERFORMANCE VERIFICATION.

4-23. To test the analyzer proceed as follows.

a. With the operating system initialized and awaiting a command (figure 4-1), enter:

option_test [RETURN]

b. The PV now displays a directory of the installed option boards and their card slot numbers (figure 4-2). Certain tests can only be performed by selecting appropriate card slots at the beginning of the PV. The first step in the PV is to locate the card slot of the analyzer to be tested and enter the slot number. For example, if the analyzer to be tested is in slot 8 of a mainframe, enter:

8 [RETURN]

c. When there is only one wide logic analyzer and one or no emulator or memory controller in the card cage, the Total PV Display appears and indicates emulator, memory and IMB source status for testing. If this is the case, proceed to the Total PV Display paragraph.

d. When two or more emulators are located in the card cage, the display requests choice of emulator (figure 4-3). To choose an emulator enter the slot number of the desired emulator. When no entry is made, the emulator in the lowest numbered slot is chosen by default. Be certain the emulator bus cables are connected.

e. When two or more memory controllers are located in the card cage, the display requests choice of memory (figure 4-4). To choose a memory controller, enter the slot number of the desired controller. When no entry is made, the memory controller in the lowest numbered slot is chosen by default. Be certain the memory controller cables are connected.

f. When there is a second wide logic analyzer in the card cage, the display requests a choice for IMB External Stimulus (figure 4-5). If no stimulus is desired press the <No Stim> softkey. To choose the stimulus, enter the slot number of the second wide logic analyzer. When valid, the recommended procedure is to select External Stimulus. Be certain the IMB cable is connected.

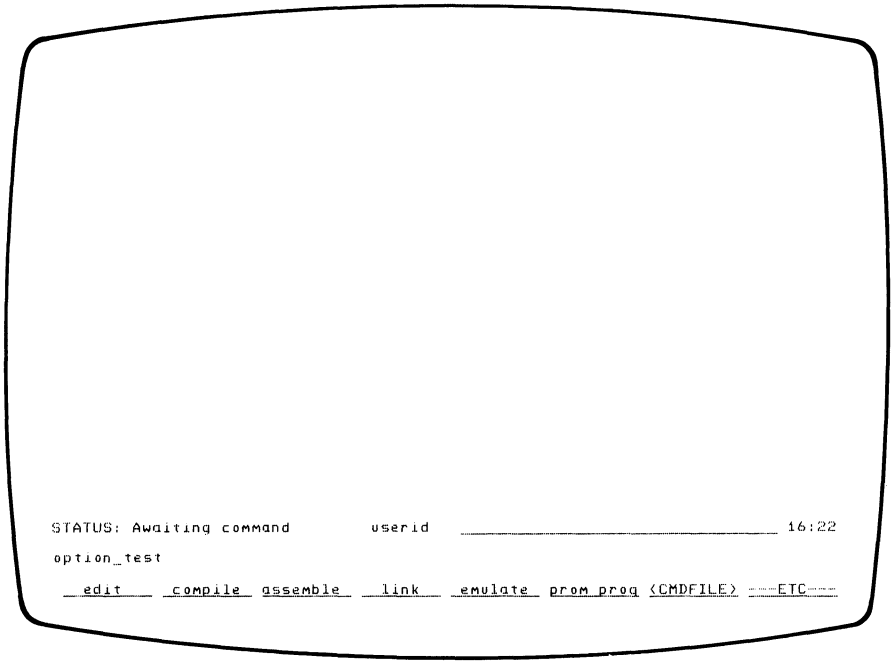


Figure 4-1. System Awaiting Command

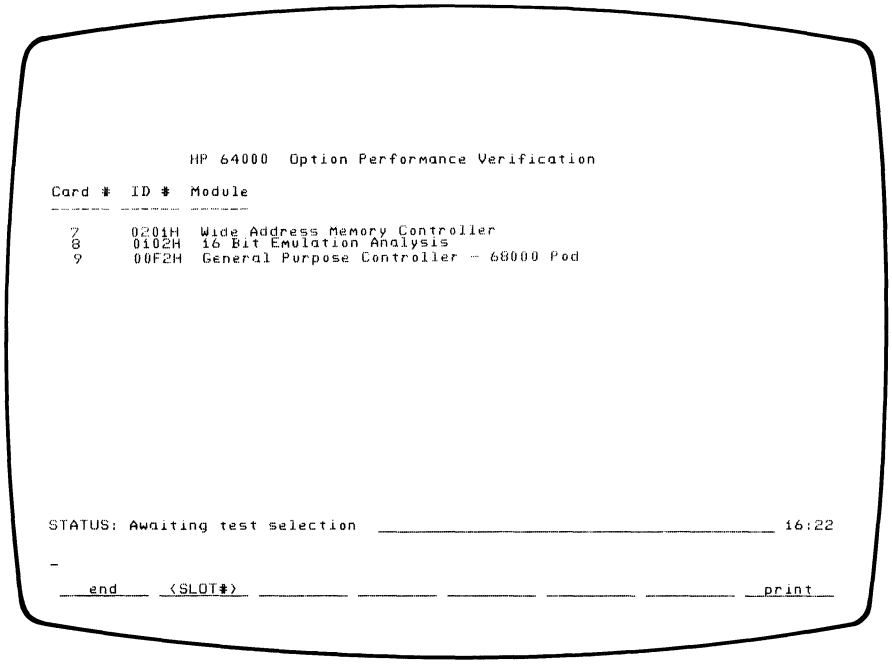


Figure 4-2. Card Cage Directory

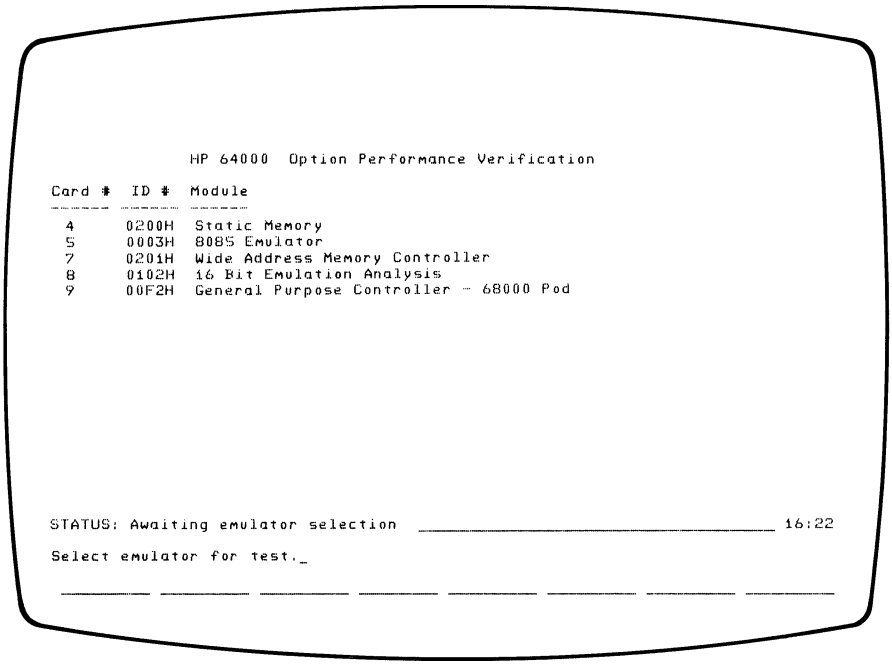


Figure 4-3. Emulator Selection

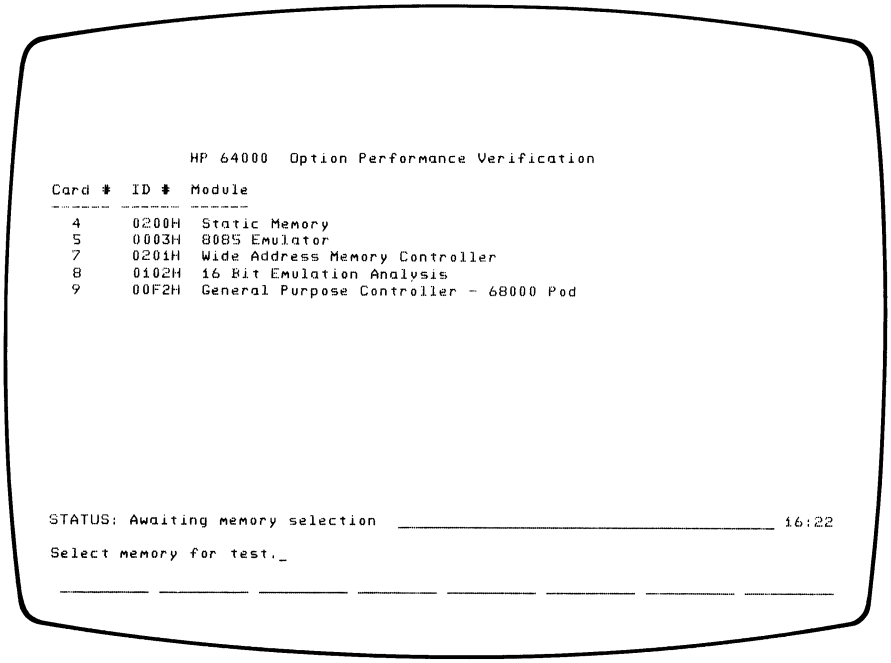


Figure 4-4. Memory Controller Selection

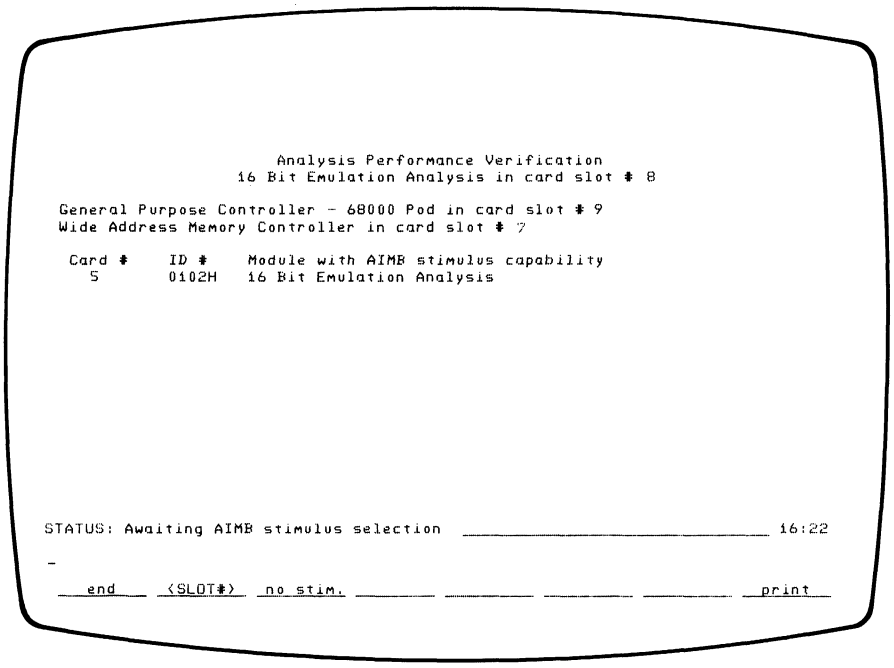


Figure 4-5. IMB External Stimulus Selection

4-24. PERFORMANCE VERIFICATION COMMANDS.

4-25. Each PV display provides prompting for the commands that can be executed. These commands are selected by 'softkeys' which are defined in table 4-3.

4-26. Calibration.

4-27. Procedures for calibrating the analyzer and checking the external port signals are presented in Section V, Adjustments.

Table 4-3. Performance Verification Softkeys

<calib>	enables calibration mode.
<cycle>	starts highlighted test and continues through other tests until another softkey is pressed.
<end>	terminates test activity and returns display to next higher level. At Total PV Display also resets failure counters to zero (Figure 4-6).
<next test>	moves highlight line to following test category.
<print>	outputs display to attached printer, including suppressed video lines.
<select>	presents highlighted test display.
<start>	begins execution of selected test.

4-28. TOTAL PV TEST DISPLAY.

4-29. Purpose. All test categories available for the card cage configuration are shown in this display. When one or more test catagories have been executed the results are displayed. Use the display to choose the test categories to be performed or to review the overall results of the PV.

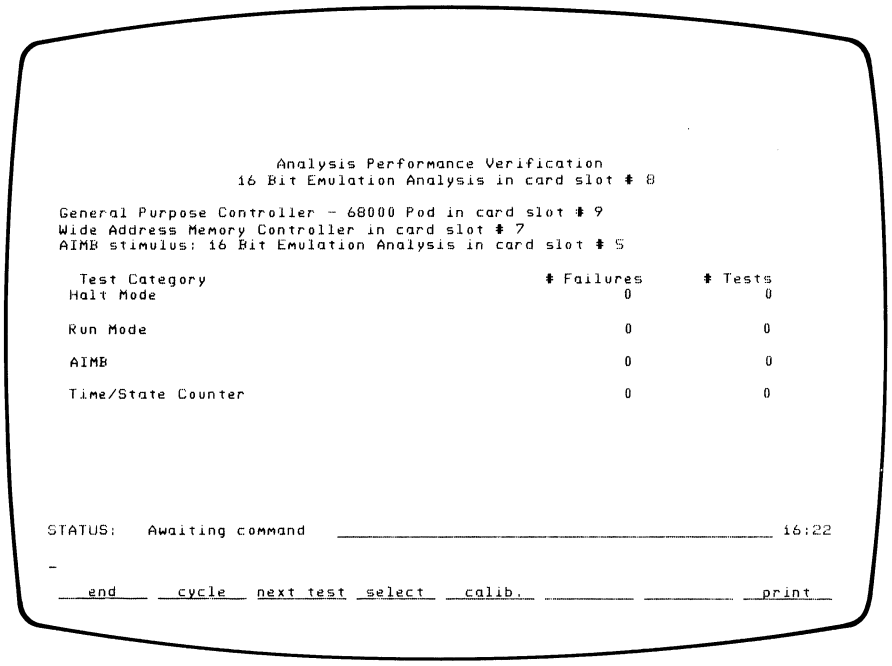


Figure 4-6. Total PV Test Display

4-30. Running the Total PV. To run all the tests shown on the display press the <Cycle> softkey. Each test category is executed and the results are displayed. A complete cycle requires approximately one minute. To stop the iterations, press the <Cycle> softkey again.

4-31. Using the Total PV Results. When the tests are complete, examine the # Failures column. When all entries are zero it indicates approximately 90% of the circuitry has been checked and no errors have been found.

4-32. A non-zero value represents the number of errors detected in the test category. Determine the exact cause of the error by reviewing the failed test category in detail. Do this by positioning the highlight line over the failed test category and pressing the <Select> softkey.

4-33. HALT MODE TEST DISPLAY.

4-34. Purpose. This display shows the four Halt Mode test categories available and their test results. Use the display to review test conditions or to select an individual test for more detailed review or further execution.

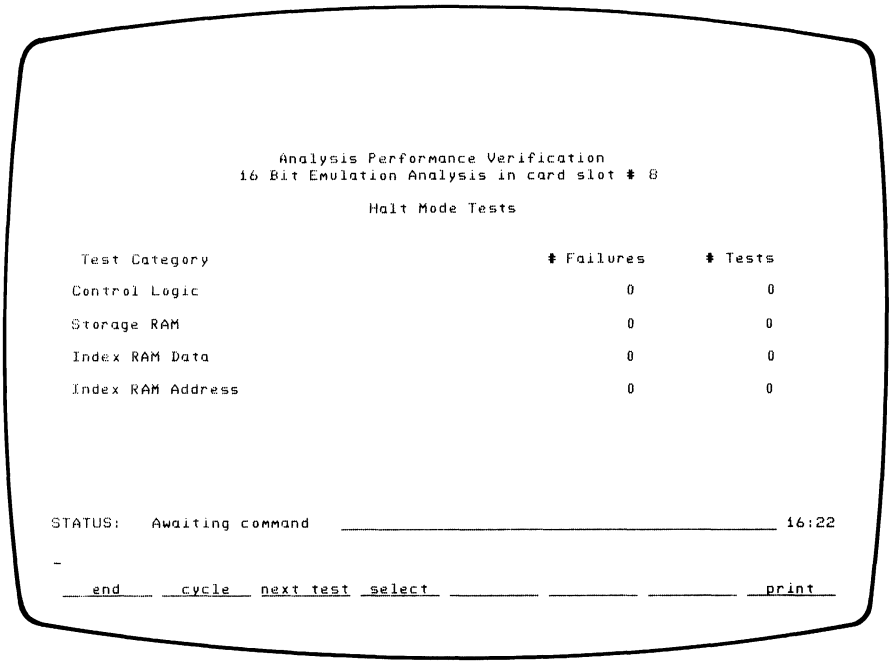


Figure 4-7. Halt Mode Display

4-35. Running the Halt Mode Tests. Press the <Cycle> softkey to run all the test categories shown on the display; execution time is less than one second per iteration. To stop the iterations press the <Cycle> softkey again.

4-36. Using the Halt Mode Results. The # Failures column shows the total number of errors detected during the tests. Determine the specific cause of the error by reviewing the failed test category in detail; it is reached by moving the highlight line to the test category and pressing the <Select> softkey.

4-37. CONTROL LOGIC TEST DISPLAY.

4-38. Purpose. The six tests shown on this display test the most basic control capabilities of the board. When any of these tests fail, the remaining tests need not be executed.

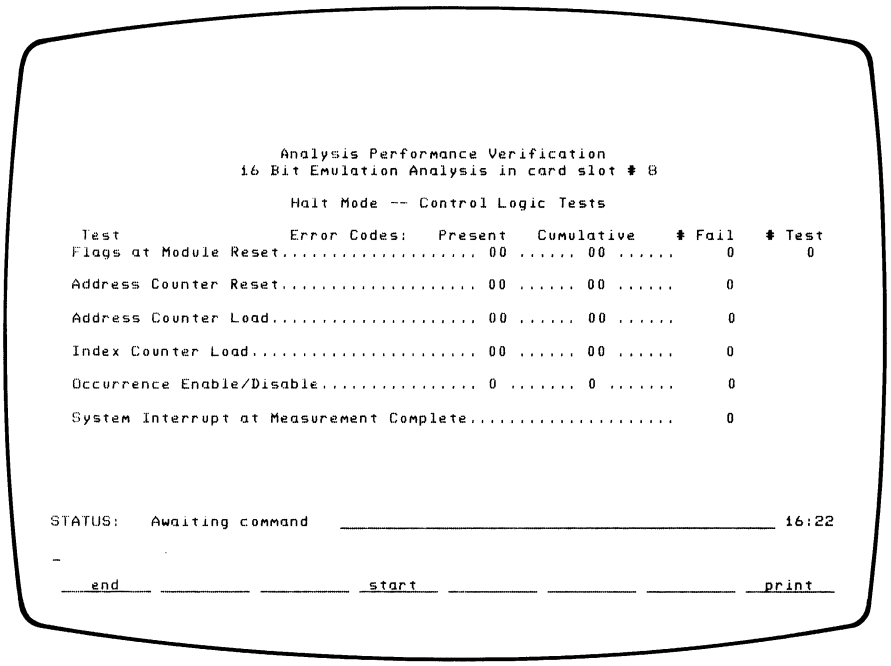


Figure 4-8. Control Logic Display

4-39. Running the Control Logic Tests. Press the <Start> softkey to begin execution. The tests continue to run until the <Start> softkey is pressed again. Each iteration takes less than one second.

4-40. Using the Control Logic Results. The total number of errors detected during the tests is shown in the # Fail column. Each error code in the Present column represents a single failure encountered during the last iteration. Each error code in the Cumulative column represents the sum of all errors detected during the test. Cumulative error codes that differ from Present error codes indicate multiple, or intermittent errors. When the error codes are the same, the errors are systematic.

4-41. How. The analyzer is halted for the Control Logic tests and the State Recognition RAMs are loaded with 'don't cares' for store qualification and trigger.

4-42. FLAGS AT MODULE RESET.

4-43. How. The control word is set so the IMB lines are not driven or received; then, the analyzer is reset. The flags are read by the host CPU and all flags except H/TEF (trigger enable flag) should be reset.

4-44. Results. Errors are decoded as follows:

Hex	Binary	Signal in error	Source
xx =	0000 0000	None	
	---- ---1	H/TP	U72-7
	---- --1-	H/MC	U88-7
	---- -1--	H/WP	U89-10
	---- 1---	H/OV	U88-9
	---1 ----	H/TEF	U39-3
	--1- ----	H/XTR	U24-4
	-1-- ----	H/TEP	U72-9
	1--- ----	H/RUN	U41-3

4-45. Signature Analysis Path. Use Loop A signatures.

a. If H/TP (trace point flag), check:
U108, 113, 77, 72, 71, 107, 73, 74.

b. If H/MC (measurement complete flag), check:
U108, 113, 77, 71, 61, 107, 115, 6.

c. If H/WP (memory wrap flag), check:
U108, 113, 77, 89, 71, 107.

d. If H/OV (time/state counter overflow flag), check:
U108, 113, 77, 88, 71, 107.

e. If H/TEF (IMB trigger enable flag), check:
U108, 113, 77, 39, 19, 71, 107.

f. If H/XTR (IMB external trigger flag), check:
U108, 113, 77, 24, 19, 71, 107.

g. If H/TEP (Trigger enable point flag), check:
U108, 113, 77, 72, 71, 107.

i. If H/RUN (Run/halt latch flag), check:
U108, 113, 77, 41, 5, 110, 88, 71, 61, 107, 115, 6.

4-46. MEMORY ADDRESS COUNTER RESET AND LOAD.

4-47. How. The Memory Address Counter (MAC) is reset by resetting the analyzer. The MAC is then read by the host CPU and an error code bit is set for any bit position of the MAC that is not zero.

4-48. Results. Errors are decoded as follows:

Hex	Binary	Signal in error	Source
xx =	0000 0000	None	
	---- ---1	H/MAC0	U76-14
	---- --1-	H/MAC1	U76-13
	---- -1--	H/MAC2	U76-12
	---- 1---	H/MAC3	U76-11
	---1 ----	H/MAC4	U93-14
	--1- ----	H/MAC5	U93-13
	-1-- ----	H/MAC6	U93-12
	1--- ----	H/MAC7	U93-11

4-49. Signature Analysis Path. Use Loop A signatures and check:

U108, 114, 80, 93, 76, 71, 107.

4-50. MEMORY INDEX COUNTER LOAD.

4-51. How. Every combination between 0 and 255, inclusive, is tested. The MAC is loaded with a value between 0 and 255 and then is read back to verify that the load executed properly. The MAC is loaded by reading from the emulation status storage area with the lower byte of host CPU address determining the value loaded to the MAC. Any discrepancy between what is loaded and what is read is shown by setting an error code bit at the position(s) of conflict.

4-52. Results. Errors are decoded as follows:

Hex	Binary	Signal in error	Source
xx =	0000 0000	None	
	---- ---1	L/MIC0	U94-14
	---- --1-	L/MIC1	U94-13
	---- -1--	L/MIC2	U94-12
	---- 1---	L/MIC3	U94-11
	---1 ----	L/MIC4	U95-14
	--1- ----	L/MIC5	U95-13
	-1-- ----	L/MIC6	U95-12
	1--- ----	L/MIC7	U95-11

4-53. Signature Analysis Path. Use Loop A signatures and check:

U119, 117, 116, 108, 114, 80, 110, 93, 76, 71, 107.

4-54. OCCURRENCE ENABLE/DISABLE.

4-55. How. The control word is set for a 'range trigger', and the Occurrence Counter is loaded with 65,535 so that a single trigger sets Trace Point. The analyzer is reset and a PV strobe is sent to clock the Trace Point flip-flop. The Trace Point Flag is checked to make sure it is set. If it is not, range cannot be enabled as the trigger.

4-56. The Occurrence Counter is then loaded with 65,534 so that more than one trigger is needed to set Trace Point. A single PV strobe is sent to clock the Trace Point flip-flop. The Trace Point Flag is checked and should be reset. If it is not, range cannot be disabled as the trigger.

4-57. Results- Errors are decodes as follows:

Hex	Binary	Error Condition
x =	0000	None
	00-1	Cannot disable Range as trigger
	001-	Cannot enable Range as trigger

4-58. Signature Analysis Path. Use Loop A signatures and check:

U108, 113, 77, 107, 98, 100, 72, 71, 87, 121, 104, 103.

4-59. SYSTEM INTERRUPT AT MEASUREMENT COMPLETE.

4-60. Indicates a problem in propagating H/MC measurement complete signal out to LIR-1.

4-61. How. A host CPU interrupt vector is set up and the analyzer is reset. The Memory Index Counter (MIC) is loaded with 255 so that Measurement Complete occurs at Trace Point. The control word is set for interrupt at Measurement Complete. A host CPU interrupt line, L/IR-1 is enabled and the analyzer is put into 'run' mode. A PV strobe is sent to clock the Trace Point and Measurement Complete flip-flops, which should cause an interrupt.

4-62. The control word is then set for no interrupt on Measurement Complete and the analyzer is reset to release the interrupt line. The interrupt routine flag is then checked for an interrupt. If no interrupt occurred, but the Measurement Complete Flag is set, then a failure is indicated.

4-63. Signature Analysis Path. Use Loop A signatures and check:

U108, 113, 77, 98, 100, 72, 71, 107, 87, 94, 95, 88, 6, 115, 121, 104, 103.

4-64. STORAGE RAM TEST DISPLAY.

4-65. Purpose. This display indicates the ability of the board to latch emulator bus signals. Use it to review test results in detail or to execute tests.

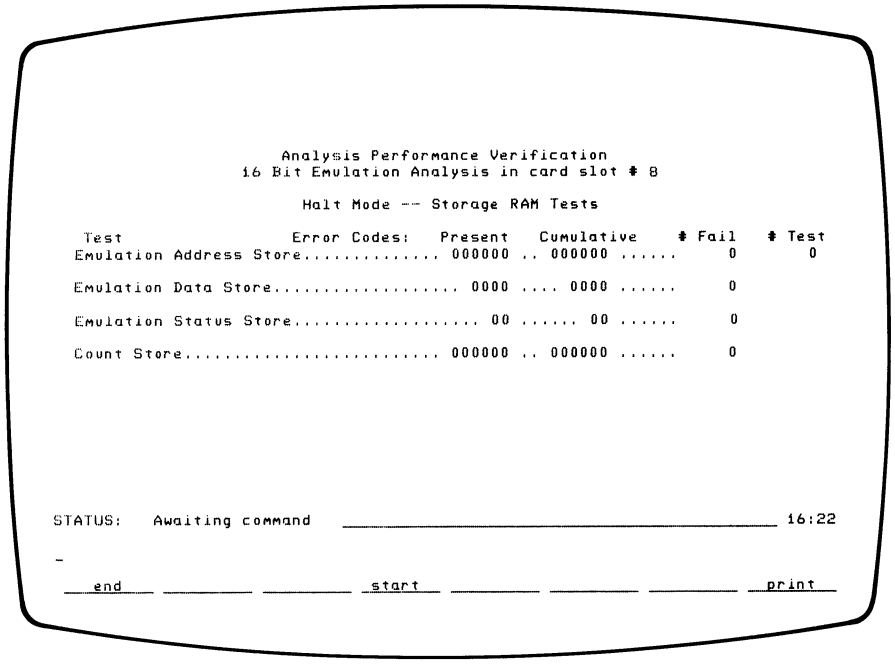


Figure 4-9. Storage RAM Display

4-66. Running the Storage RAM Tests. Press the <Start> softkey to begin execution. The tests continue to run until the <Start> softkey is pressed again. Each iteration takes less than one second.

4-67. Using the Storage RAM Results. The total number of errors detected during the tests is shown in the # Fail column. Each error code in the Present column represents a single failure encountered during the last iteration. Each error code in the Cumulative column represents the sum of all errors detected during the test. Cumulative error codes that differ from Present error codes indicate multiple, or intermittent errors. When the error codes are the same the errors are systematic.

4-68. EMULATOR ADDRESS STORE.

4-69. How. Decreasing numbers are stored in the emulation address storage RAMs. That is, FFFFFFH is stored in location 00H; FEFEFEH is stored in location 01H; and so on. To store, the desired RAM location is loaded in the Memory Address Counter (MAC), and then a PV strobe is sent to write the data from the host CPU into the selected RAMs. After all 255 locations have been accessed, they are read back to verify that they contain what was written to them. Any discrepency is indicated as a failure in the appropriate bit position of the error display.

4-70. Results. Errors are decoded as follows:

Hex	Binary	Signal in error	Sources	
xxxxx=	0000 0000 0000 0000 0000 0000	None		
	---- ---- ---- ---- ---- ---1	LL/EA0	U13-3	U14-2
	---- ---- ---- ---- ---- --1-	LL/EA1	U13-5	U14-5
	---- ---- ---- ---- ---- -1--	LL/EA2	U13-7	U14-6
	---- ---- ---- ---- ---- 1---	LL/EA3	U13-9	U14-9
	---- ---- ---- ---- ---1 ----	LL/EA4	U13-12	U14-12
	---- ---- ---- ---- --1- ----	LL/EA5	U13-14	U14-15
	---- ---- ---- ---- -1-- ----	LL/EA6	U13-16	U14-16
	---- ---- ---- ---- 1--- ----	LL/EA7	U13-18	U14-19
	---- ---- ---- ---1 ---- ----	LL/EA8	U15-3	U16-2
	---- ---- ---- --1- ---- ----	LL/EA9	U15-5	U16-5
	---- ---- ---- -1-- ---- ----	LL/EA10	U15-7	U16-6
	---- ---- ---- 1--- ---- ----	LL/EA11	U15-9	U16-9
	---- ---- ---1 ---- ---- ----	LL/EA12	U15-12	U16-12
	---- ---- --1- ---- ---- ----	LL/EA13	U15-14	U16-15
	---- ---- -1-- ---- ---- ----	LL/EA14	U15-16	U16-16
	---- ---- 1--- ---- ---- ----	LL/EA15	U15-18	U16-19
	---- ---1 ---- ---- ---- ----	LL/EA16	U17-3	U18-2
	---- --1- ---- ---- ---- ----	LL/EA17	U17-5	U18-5
	---- -1-- ---- ---- ---- ----	LL/EA18	U17-7	U18-6
	---- 1--- ---- ---- ---- ----	LL/EA19	U17-9	U18-9
	---1 ---- ---- ---- ---- ----	LL/EA20	U17-12	U18-12
	--1- ---- ---- ---- ---- ----	LL/EA21	U17-14	U18-15
	-1-- ---- ---- ---- ---- ----	LL/EA22	U17-16	U18-16
	1--- ---- ---- ---- ---- ----	LL/EA23	U17-18	U18-19

LL/EA = Low, Latched Emulator Address

24 bits of address storing RAM.

U50 --- U49 --- U48 --- U47 --- U46 --- U45
MSB <---------- LSB

4-71. Signature Analysis Path. Use Loop B signatures and check:

U108, 109, 112, 114, 93, 76, 110, 50, 49, 48, 47, 46, 45, 13, 15, 17, 93, 76, 71, 107, 106, 55, 116, 41.

4-72. EMULATOR DATA STORE.

4-73. How. Decreasing numbers are stored in the emulation data storage RAMs. That is, FFFFH is stored in location 00H; FEFEH is stored in location 01H; and so on. To store, the desired RAM location is loaded in the Memory Address Counter (MAC), and then a PV strobe is sent to write the data from the host CPU into the selected RAMs. After all 255 locations have been accessed, they are read back to verify that they contain what was written to them. Any discrepency is indicated as a failure in the appropriate bit position of the error display.

4-74. Results. Errors are decodes as follows:

Hex	Binary	Signal in error	Sources	
xxxx=	0000 0000 0000 0000	None		
	---- ---- ---- ---1	LL/ED0	U7-3	U8-2
	---- ---- ---- --1-	LL/ED1	U7-5	U8-5
	---- ---- ---- -1--	LL/ED2	U7-7	U8-6
	---- ---- ---- 1---	LL/ED3	U7-9	U8-9
	---- ---- ---1 ----	LL/ED4	U7-12	U8-12
	---- ---- --1- ----	LL/ED5	U7-14	U8-15
	---- ---- -1-- ----	LL/ED6	U7-16	U8-16
	---- ---- 1--- ----	LL/ED7	U7-18	U8-19
	---- ---1 ---- ----	LL/ED8	U9-3	U10-2
	---- --1- ---- ----	LL/ED9	U9-5	U10-5
	---- -1-- ---- ----	LL/ED10	U9-7	U10-6
	---- 1--- ---- ----	LL/ED11	U9-9	U10-9
	---1 ---- ---- ----	LL/ED12	U9-12	U10-12
	--1- ---- ---- ----	LL/ED13	U9-14	U10-15
	-1-- ---- ---- ----	LL/ED14	U9-16	U10-16
	1--- ---- ---- ----	LL/ED15	U9-18	U10-19

LL/ED = Low, Latched Emulator Data

16 bits of data storing RAM.

U43 --- U63 --- U42 --- U62
MSB <---------- LSB

4-75. Signature Analysis Path. Use Loop B signatures and check:

U108, 109, 112, 114, 93, 76, 110, 43, 63, 42, 62, 9, 7, 93, 76, 71, 107, 106, 55, 116, 41.

4-76. EMULATOR STATUS STORE.

4-77. How. Decreasing numbers are stored in the emulation status storage RAMs. That is, FFH is stored in location 00H; FEH is stored in location 01H; and so on. To store, the desired RAM location is loaded in the Memory Address Counter (MAC), and then a PV strobe is sent to write the data from the host CPU into the selected RAMs. After all 255 locations have been accessed, they are read back to verify that they contain what was written to them. Any discrepency is indicated as a failure in the appropriate bit position of the error display.

4-78. Results. Errors are decoded as follows:

Hex	Binary	Signal in error	Sources	
xx =	0000 0000	None		
	---- ---1	LL/ES0	U11-3	U12-2
	---- --1-	LL/ES1	U11-5	U12-5
	---- -1--	LL/ES2	U11-7	U12-6
	---- 1---	LL/ES3	U11-9	U12-9
	---1 ----	LL/ES4	U11-12	U12-12
	--1- ----	LL/ES5	U11-14	U12-15
	-1-- ----	LL/ES6	U11-16	U12-16
	1--- ----	LL/ES7	U11-18	U12-19

LL/ES = Low, Latched Emulator Status

8 bits of status storing RAM.

U44 --- U64
MSB <-- LSB

4-79. Signature Analysis Path. Use Loop B signatures and check:

U108, 109, 112, 114, 93, 76, 110, 44, 64, 11, 93, 76, 71, 107, 106, 55, 116, 41.

4-80. COUNT STORE.

4-81. How. The State Recognition RAMs are loaded with a 'never count' qualification so that the Time/State Counter stays at zero, and The Time/State Counter is reset. The Memory Address Counter (MAC) is loaded with 00H through FFH to address all of the locations of the Count Storage RAMs. For each location a PV strobe is sent to write 000000H into that location. After all 256 locations have been accessed they are read back to verify they all contain 000000H. Any discrepencies are indicated as a failure in the appropriate bit of the error display.

4-82. Results. Errors are decoded as follows:

Hex xxxxx=	Binary	Signal in error	Source
	0000 0000 0000 0000 0000 0000	None	
	---- ---- ---- ---- ---- ---1	CNT0	U81-14
	---- ---- ---- ---- ---- --1-	CNT1	U81-13
	---- ---- ---- ---- ---- -1--	CNT2	U81-12
	---- ---- ---- ---- ---- 1---	CNT3	U81-11
	---- ---- ---- ---- ---1 ----	CNT4	U82-14
	---- ---- ---- ---- --1- ----	CNT5	U82-13
	---- ---- ---- ---- ---- ----	CNT6	U82-12
	---- ---- ---- ---- 1--- ----	CNT7	U82-11
	---- ---- ---- ---1 ---- ----	CNT8	U83-14
	---- ---- ---- --1- ---- ----	CNT9	U83-13
	---- ---- ---- -1-- ---- ----	CNT10	U83-12
	---- ---- ---- 1--- ---- ----	CNT11	U83-11
	---- ---- ---1 ---- ---- ----	CNT12	U84-14
	---- ---- --1- ---- ---- ----	CNT13	U84-13
	---- ---- -1-- ---- ---- ----	CNT14	U84-12
	---- ---- 1--- ---- ---- ----	CNT15	U84-11
	---- ---1 ---- ---- ---- ----	CNT16	U85-14
	---- --1- ---- ---- ---- ----	CNT17	U85-13
	---- -1-- ---- ---- --- ----	CNT18	U85-12
	---- 1--- ---- ---- ---- ----	CNT19	U85-11
	---1 ---- ---- ---- ---- ----	CNT20	U86-14
	--1- ---- ---- ---- ---- ----	CNT21	U86-13
	-1-- ---- ---- ---- ---- ----	CNT22	U86-12
	1--- ---- ---- ---- ---- ----	CNT23	U86-11

24 bits of count storing RAM.

U70 --- U69 --- U68 --- U67 --- U66 --- U65
MSB <---------- LSB

4-83. Signature Analysis Path. Use Loop B signatures and check:

U108, 109, 112, 114, 71, 107, 106, 110, 93, 76, 80, 86, 85, 84, 83, 82, 81, 65, 66, 67, 68, 69, 70, 98, 97, 99.

4-84. INDEX RAM DATA TEST DISPLAY.

4-85. Purpose. This display shows the board's ability to store data at a single address and successfuly decode it with the State Recognition logic. Use the display to execute the test or review detailed results.

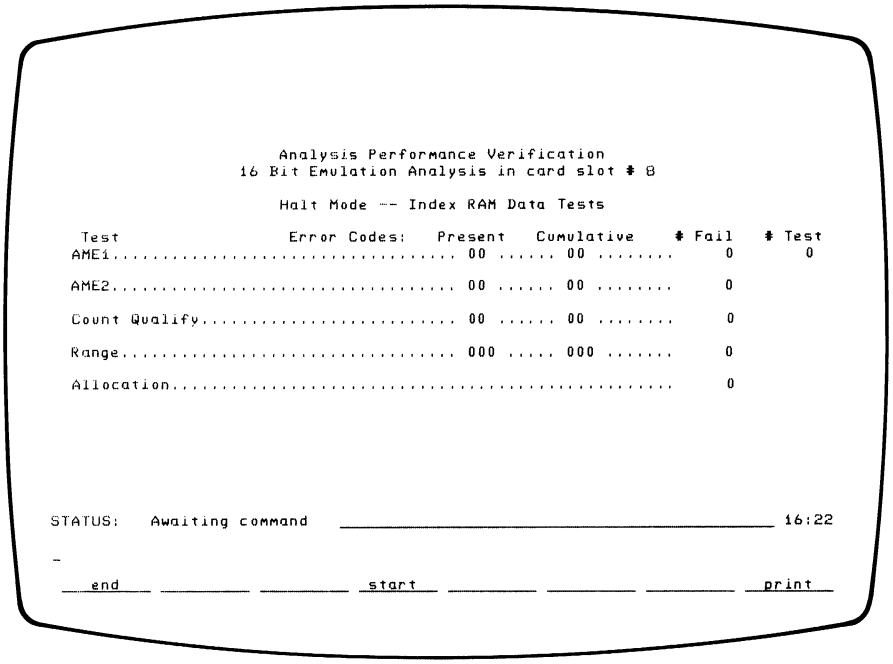


Figure 4-10. Index RAM Data Display

4-86. Running the Index RAM Tests. Press the <Start> softkey to begin; the tests continue until the <Start> softkey is pressed again. Each iteration takes less than one second.

4-87. Using the Index RAM Data Results. The total number of errors detected during the tests is shown in the # Fail column. Each error code in the Present column represents a single failure encountered during the last iteration. Each error code in the Cumulative column represents the sum of all errors detected during the test. Cumulative error codes that differ from Present error codes indicate multiple, or intermittent errors. When the error codes are the same the errors are systematic.

4-88. How. These tests are table driven; a certain bit pattern is loaded into the State Recognition RAMs and a resulting trigger or no trigger is the result. An individual test might verify the correct operation of a specific minterm signal (data line out of a State Recognition RAM) or it might only indicate that several minterm lines are functioning properly.

4-89. Resources which are used for different triggering modes are AME1, AME2, Count Qualify, and Range. To test for shorts to ground, all minterms for a given resource are set true. Because a resource is just the AND of all of its minterms, it should be true if all of its minterms are set true. If the resource is false, then one or more of its minterms lines must be shorted to ground. It is impossible to tell which line is the culprit, so all the minterm lines are flagged as failed.

4-90. To test for shorts to power, all minterms for a given resource, except one, are set true. The remaining minterm, which is under test, is set false. If the signal under test is shorted to power or open (and floats high), then the resource is detected as true and that minterm is flagged as failed.

4-91. AME1 (Adjacent Minterm Expression 1).

4-92. How. Signals SM0, DM0, DM4, AM0, AM5, AM12 are set high. Signal AME1 should cause a trigger which sets the Trace Point Flag. If not, all six lines are flagged as failed. Each of the above minterm signals are checked one at time for a short to power. If the Trace Point Flag is found to be set, the line being tested is flagged as failed.

4-93. Results. Errors are decoded as follows:

Hex	Binary	Signal in error	Source
xx =	0000 0000	None	
	00-- ---1	SM0	U28-10
	00-- --1-	DM0	U26-10
	00-- -1--	DM4	U27-10
	00-- 1---	AM0	U29-10
	00-1 ----	AM5	U31-12
	001- ----	AM12	U33-10

4-94. Signature Analysis Path. Use Loop C signatures.

a. If not all minterms fail, depending on failure, check:

SM0...U28, 11, 110, 111, 113.
DM0...U26, 96, 7, 110, 111, 113.
DM4...U27, 96, 9, 110, 111, 113.
AM0...U29, 13, 110, 111, 113.
AM5...U31, 17, 110, 111, 113.
AM12..U33, 17, 110, 111, 113.

b. If all the minterms fail, check:

U111, 113, 110, 11, 7, 9, 13, 15, 17, 28, 26, 27, 29, 31, 33, 108 109, 77, 112, 72, 71, 107, 73, 74, 97, 99, 98.

4-95. AME2 (Adjacent Minterm Expression 2).

4-96. How. Signals SM1, DM1, DM5, AM1, AM6, AM13 are set high. Signal AME2 should cause a trigger which sets the Trace Point Flag. If not, all six lines are flagged as failed. Each of the above minterm signals are checked for a short to power. If the Trace Point Flag is found to be set, the line being tested is flagged as failed.

4-97. Results. Errors are decoded as follows:

Hex	Binary	Signal in error	Source
xx =	0000 0000	None	
	00-- ---1	SM1	U28-12
	00-- --1-	DM1	U26-12
	00-- -1--	DM5	U27-12
	00-- 1---	AM1	U29-12
	00-1 ----	AM6	U31-14
	001- ----	AM13	U33-12

4-98. Signature Analysis Path. Use Loop C signatures.

a. If not all minterms fail, depending on failure, check:

SM1....U28, 11, 110, 111, 113.
DM1....U26, 96, 7, 110, 111, 113.
DM5....U27, 96, 9, 110, 111, 113.
AM1....U29, 13, 110, 111, 113.
AM6....U31, 15, 110, 111, 113.
AM13...U33, 17, 110, 111, 113.

b. If all the minterms fail, check:

U111, 113, 110, 11, 7, 9, 13, 15, 17, 28, 26, 27, 29, 31, 33, 108, 109, 77, 112, 72, 71, 107, 73, 74, 97, 99, 98.

4-99. COUNT QUALIFY.

4-100. How. Signals SM2, DM2, DM6, AM2, AM7, AM14 are set high. Count Qualify should cause the 24-bit counter to increment. If not, all six lines are flagged as failed. Each of the above minterm signals are checked one at time for shorts to power. If the 24-bit counter increments, the line being tested is flagged as failed.

4-101. Results. Errors are decoded as follows:

Hex	Binary	Signal in error	Source
xx =	0000 0000	None	
	00-- ---1	SM2	U28-14
	00-- --1-	DM2	U26-14
	00-- -1--	DM6	U27-14
	00-- 1---	AM2	U29-14
	00-1 ----	AM7	U31-16
	001- ----	AM14	U33-14

4-102. Signature Analysis Path. Use Loop C signatures.

a. If not all minterms fail, depending on failure, check:

SM2....U28, 11, 110, 111, 113.
DM2....U26, 96, 7, 110, 111, 113.
DM6....U27, 96, 9, 110, 111, 113.
AM2....U29, 13, 110, 111, 113.
AM7....U31, 15, 110, 111, 113.
AM14...U33, 17, 110, 111, 113.

b. If all the minterms fail, check:

U111, 113, 110, 11, 7, 9, 13, 15, 17, 71, 97, 98, 99, 108, 109, 112, 114, 81, 82, 83, 65, 66, 67, 68, 69, 70.

4-103. RANGE.

4-104. How. Signals SM3, DM3, DM7, AM3-4, AM8-11 and AM15-16 are set high. Range should cause a trigger which sets the Trace Point Flag. If not, all eleven lines are flagged as failed. Each of the above minterm signals are checked for shorts to power. If the Trace Point Flag is found to be set, the line being tested is flagged as failed.

4-105. Results. Errors are decoded as follows:

Hex	Binary	Signal in error	Source
xxx=	0000 0000 0000	None	
	0--- ---- ---1	SM3	U28-16
	0--- ---- --1-	DM3	U26-16
	0--- ---- -1--	DM7	U27-16
	0--- ---- 1---	AM3	U29-16
	0--- ---1 ----	AM4	U30-6
	0--- --1- ----	AM8	U32-10
	0--- -1-- ----	AM9	U32-12
	0--- 1--- ----	AM10	U32-14
	0--1 ---- ----	AM11	U32-16
	0-1- --- ----	AM15	U33-16
	01-- ---- ----	AM16	U34-6

4-106. Signature Analysis Path. Use Loop C signatures.

a. If not all minterms fail, depending on failure, check:

SM3....U28, 11, 110, 111, 113.
DM3....U26, 96, 7, 110, 111, 113.
DM7....U27, 96, 9, 110, 111, 113.
AM3....U29, 13, 110, 111, 113.
AM4....U30, 13, 110, 111, 113.
AM8....U32, 15, 110, 111, 113.
AM9....U32, 15, 110, 111, 113.
AM10...U32, 15, 110, 111, 113.
AM11...U32, 15, 110, 111, 113.
AM15...U33, 17, 110, 111, 113.
AM16...U34, 17, 110, 111, 113.

b. If all the minterms fail, check:

U111, 113, 110, 11, 7, 9, 13, 15, 17, 28, 26, 29, 30, 32, 33, 34 108, 109, 77, 112, 72, 71, 107, 73, 74, 97, 98, 99, 100, 101, 102.

4-107. ALLOCATION.

4-108. Allocation failure indicates that AME1/AME2 and Range are not being properly allocated to Trigger and Store Qualification.

4-109. How. The State Recognition RAMs are loaded such that there is a 'never trigger' for the Range resource and a 'don't care trigger' for the AME1 and AME2 resources. The control word is then set for a Range trigger. A PV strobe is sent to clock the Trace Point flip-flop. If the Trace Point Flag is set, indicating a trigger has occurred, then an Allocation failure is indicated.

4-110. The State Recognition RAMs are then loaded such that there is a 'don't care trigger' for the Range resource and a 'never trigger' for the AME1 and AME2 resources. The control word is then set for an AME1 and AME2 trigger. A PV strobe is sent to clock the Trace Point flip-flop. If the Trace Point Flag is set then an Allocation failure is indicated.

4-111. Signature Analysis Path. Use Loop C signatures and check:

U111, 113, 110, 11, 7, 9, 13, 15, 28, 26, 27, 29, 31, 33, 30, 32, 34, 98, 108, 109, 77, 112, 72, 71, 107, 73, 74, 97, 98, 99, 100, 101, 102, 55.

4-112. INDEX RAM ADDRESS TEST DISPLAY.

4-113. Purpose. The nine tests shown in this display test RAM address indexing capabilities. Use the display to review test results in detail or to run the tests.

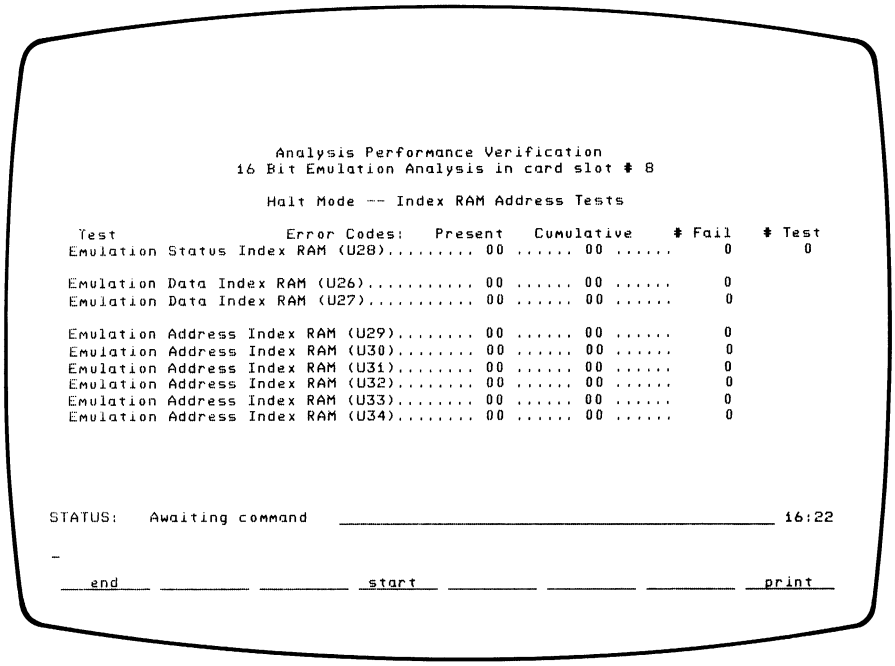


Figure 4-11. Index RAM Address Display

4-114. Running the Index RAM Address Tests. Press the <Start> softkey to begin the tests. The tests continue to execute until the <Start> softkey is pressed again. Each iteration takes less than one second.

4-115. Using the Index RAM Address Results. The total number of errors detected during the tests is shown in the # Fail column. Each error code in the Present column represents a single failure encountered during the last iteration. Each error code in the Cumulative column represents the sum of all errors detected during the test. Cumulative error codes that differ from Present error codes indicate multiple, or intermittent errors. When the error codes are the same the errors are systematic.

4-116. How. Each of the State Recognition RAM's address lines are tested one at a time. To do this, minterm lines for a particular resource are set true, except for one minterm which is set false. This one minterm is produced by the particular RAM under test.

4-117. Location 0 and 255 of all the RAMs are loaded with the above bit configuration. These locations now contain 'never trigger' bit patterns for the allocated resource, either AME1 or Range. Then, using a walking one/zero configuration on the RAM address lines, locations other than 0 or 255 are accessed and loaded with a 'don't care trigger' bit pattern.

4-118. In between each of these loads, address 0 and then address 255 are sent as trace data to the RAMs. If the Trace Point Flag is set as a result, then the last address bit which was changed during the walking one/zero has failed. The Trace Point Flag could have only been set if either location 0 or 255 of the RAM under test was overwritten with a 'don't care trigger' pattern.

4-119. EMULATION STATUS INDEX RAM U28.

4-120. Results. Errors are decoded as follows:

Hex	Binary	Signal in error	Source
xx =	0000 0000	None	
	---- ---1	HB/A0	U11-3
	---- --1-	HB/A1	U11-5
	---- -1--	HB/A2	U11-7
	---- 1---	HB/A3	U11-9
	---1 ----	HB/A4	U11-12
	--1- ----	HB/A5	U11-14
	-1-- ----	HB/A6	U11-16
	1--- ----	HB/A7	U11-18

4-121. EMULATION DATA INDEX RAM U26.

4-122. Results. Errors are decoded as follows:

Hex	Binary	Signal in error	Source
xx =	0000 0000	None	
	---- ---1	HB/A0	U7-3
	---- --1-	HB/A1	U7-5
	---- -1--	HB/A2	U7-7
	---- 1---	HB/A3	U7-9
	---1 ----	HB/A4	U7-12
	--1- ----	HB/A5	U7-14
	-1-- ----	HB/A6	U7-16
	1--- ----	HB/A7	U7-18

4-123. EMULATION DATA INDEX RAM U27.

4-124. Results. Errors are decoded as follows:

Hex	Binary	Signal in error	Source
xx =	0000 0000	None	
	---- ---1	HB/A8	U9-3
	---- --1-	HB/A9	U9-5
	---- -1--	HB/A10	U9-7
	---- 1---	HB/A11	U9-9
	---1 ----	HB/A12	U9-12
	--1- ----	HB/A13	U9-14
	-1-- ----	HB/A14	U9-16
	1--- ----	HB/A15	U9-18

4-125. EMULATION ADDRESS INDEX RAM U29.

4-126. Results. Errors are decoded as follows:

Hex	Binary	Signal in error	Source
xx =	0000 0000	None	
	---- ---1	HB/A0	U13-3
	---- --1-	HB/A1	U13-5
	---- -1--	HB/A2	U13-7
	---- 1---	HB/A3	U13-9
	---1 ----	HB/A4	U13-12
	--1- ----	HB/A5	U13-14
	-1-- ----	HB/A6	U13-16
	1--- ----	HB/A7	U13-18

4-127. EMULATION ADDRESS INDEX RAM U30.

4-128. Results. Errors are decoded as follows:

Hex	Binary	Signal in error	Source
xx =	0000 0000	None	
	---- ---1	HB/A0	U13-3
	---- --1-	HB/A1	U13-5
	---- -1--	HB/A2	U13-7
	---- 1---	HB/A3	U13-9
	---1 ----	HB/A4	U13-12
	--1- ----	HB/A5	U13-14
	-1-- ----	HB/A6	U13-16
	1--- ----	HB/A7	U13-18

4-129. EMULATION ADDRESS INDEX U31.

4-130. Results. Errors are decoded as follows:

Hex	Binary	Signal in error	Source
xx =	0000 0000	None	
	---- ---1	HB/A8	U15-3
	---- --1-	HB/A9	U15-5
	---- -1--	HB/A10	U15-7
	---- 1---	HB/A11	U15-9
	---1 ----	HB/A12	U15-12
	--1- ----	HB/A13	U15-14
	-1-- ----	HB/A14	U15-16
	1--- ----	HB/A15	U15-18

4-131. EMULATION ADDRESS INDEX RAM 32.

4-132. Results. Errors are decoded as follows:

Hex	Binary	Signal in error	Source
xx =	0000 0000	None	
	---- ---1	HB/A8	U15-3
	---- --1-	HB/A9	U15-5
	---- -1--	HB/A10	U15-7
	---- 1---	HB/A11	U15-9
	---1 ----	HB/A12	U15-12
	--1- ----	HB/A13	U15-14
	-1-- ----	HB/A14	U15-16
	1--- ----	HB/A15	U15-18

4-133. EMULATION ADDRESS INDEX RAM U33.

4-134. Results. Errors are decoded as follows:

Hex	Binary	Signal in error	Source
xx =	0000 0000	None	
	---- ---1	HB/A16	U13-3
	---- --1-	HB/A17	U13-5
	---- -1--	HB/A18	U13-7
	---- 1---	HB/A19	U13-9
	---1 ----	HB/A20	U13-12
	--1- ----	HB/A21	U13-14
	-1-- ----	HB/A22	U13-16
	1--- ----	HB/A23	U13-18

4-135. EMULATION ADDRESS INDEX RAM U34.

4-136. Results. Errors are decoded as follows.

Hex	Binary	Signal in error	Source
xx =	0000 0000	None	
	---- ---1	HB/A16	U17-3
	---- --1-	HB/A17	U17-5
	---- -1--	HB/A18	U17-7
	---- 1---	HB/A19	U17-9
	---1 ----	HB/A20	U17-12
	--1- ----	HB/A21	U17-14
	-1-- ----	HB/A22	U17-16
	1--- ----	HB/A23	U17-18

4-137. Signature Analysis Path. Use Loop D signatures.

a. If only U30, 32, and 34 have address lines which fail, check: U100, 101, 102.

b. If only U30, 32 and 34 pass, while the rest have address lines which fail, check: U97, 98, 99.

c. If all the address lines do not fail and the failures are not grouped as above, depending on failure, check:

U28...U28, 11, 110.
U26...U26, 7, 110.
U27...U27, 9, 110.
U29...U29, 13, 110.
U30...U30, 13, 110.
U31...U31, 15, 110.
U32...U32, 15, 110.
U33...U33, 17, 110.
U34...U33, 17, 110.

d. If all of the RAM address lines fail, check:
U98, 100, 74, 108, 109, 111, 113, 110, 77, 112, 71, 72, 55, 41.

4-138. RUN MODE TEST DISPLAY.

4-139. Purpose. This display presents nine tests that check the board's ability to evaluate counter and control conditions. Use it to review test results in detail or to execute the tests.

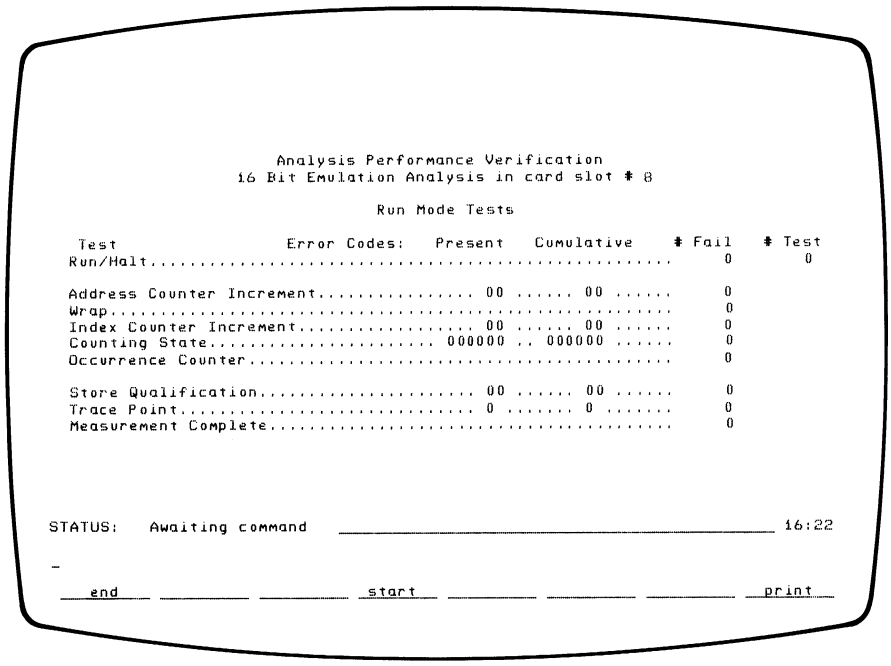


Figure 4-12. Run Mode Display

4-140. Running the Run Mode Tests. Press the <Start> softkey to begin; the tests continue until the <Start> softkey is pressed again. One iteration takes less than one second.

4-141. Using the Run Mode Results. The total number of errors detected during the tests is shown in the # Fail column. Each error code in the Present column represents a single failure encountered during the last iteration. Each error code in the Cumulative column represents the sum of all errors detected during the test. Cumulative error codes that differ from Present error codes indicate multiple, or intermittent errors. When the error codes are the same the errors are systematic.

4-142. RUN/HALT.

4-143. This failure indicates the Run/halt latch is not properly switching the mode of the analyzer.

4-144. How. The analyzer is reset and the State Recognition RAMs are loaded with a 'never trigger' specification so that Measurement Complete never occurs. The analyzer is sent a 'run' command and then the Run Flag is checked to make sure it is set. The analyzer is then sent a 'halt' command and again the Run Flag is checked to make sure it is reset. The State Recognition RAMs and the Memory Index Counter are set so that a trigger causes the Measurement Complete Flag to become set. This should reset the Run Flag. If the Run Flag is not at the proper state for any of the above tests, then a failure is indicated.

4-145. Signature Analysis Path. Use Loop E signatures and check:

U108, 109, 111, 113, 77, 112, 41, 5, 88, 71, 61, 107, 115, 6, 88, 94, 95, 98, 74.

4-146. ADDRESS COUNTER INCREMENT.

4-147. How. The Memory Index Counter (MIC) is loaded with 0 so that the Memory Address Counter (MAC) can be incremeted through its full range without the Measurement Complete Flag (H/MC) becoming set. The Memory Address Counter is then reset and incremented with a verify of count between each increment. Any discrepency is indicated as a failure in the appropriate bit.

4-148. Results. Errors are decoded as follows:

Hex	Binary	Signal in error	Source
xx =	0000 0000	None	
	---- ---1	H/MAC0	U76-14
	---- --1-	H/MAC1	U76-13
	---- -1--	H/MAC2	U76-12
	---- 1---	H/MAC3	U76-11
	---1 ----	H/MAC4	U93-14
	--1- ----	H/MAC5	U93-13
	-1-- ----	H/MAC6	U93-12
	1--- ----	H/MAC7	U93-11

4-149. Signature Analysis Path. Use Loop E signatures.

a. If not all of the MAC's output signals fail, depending on failure, check:

H/MAC0-3...U80, 114, 76, 110.
H/MAC4-7...U80, 114, 93, 110.

b. If all of the bits fail, check:

U108, 109, 111, 113, 77, 112, 114, 55, 74, 98, 88, 61, 80, 114, 110, 76, 93, 89, 41.

4-150. WRAP.

4-151. A failure indicates an overflow from the Memory Address Counter was not detected/stored by the Wrap flip-flop.

4-152. How. The State Recognition RAMs are loaded with a 'don't care' specification so that the Memory Address Counter (MAC) can increment, and the Memory Index Counter (MIC) is loaded with 0 so that the Measurement Complete Flag (H/MC) does not become set. The MAC is loaded with 254 so that two clocks should cause a memory wrap. The first clock is sent followed by a check of the Memory Wrap Flag (H/WP) to make sure that it was not set. Then the second clock is sent followed by another check of the H/WP, which should now be set. If the wrong state is encountered in either case a failure is indicated.

4-153. Signature Analysis Path. Use Loop E signatures and check:

U108, 109, 111, 113, 77, 112, 89, 77, 107, 76, 93, 55, 74, 98.

4-154. INDEX COUNTER INCREMENT.

4-155. How. The Memory Index Counter (MIC) is loaded with 0 and the State Recognition RAMs are loaded with a 'don't care' for the resources allocated to storage qualification and a 'never' for the resources allocated to trigger. The analyzer is put into 'run' mode and the MIC is clocked. The MIC should not have incremented, but should still contain 0. The MIC is again loaded with 0 and the State Recognition RAMs are loaded with a 'don't care trigger' and store qualification so that the MIC can increment. The MIC is clocked 256 times with a verify of increment in between each clock. Any discrepencies are indiated as a failure in the appropriate bit.

4-156. Results. Errors are decoded as follows:

Hex	Binary	Signal in error	Source
xx =	0000 0000	None	
	---- ---1	H/MIC0	U94-14
	---- --1-	H/MIC1	U94-13
	---- -1--	H/MIC2	U94-12
	---- 1---	H/MIC3	U94-11
	---1 ----	H/MIC4	U95-14
	--1- ----	H/MIC5	U95-13
	-1-- ----	H/MIC6	U95-12
	1--- ----	H/MIC7	U95-11

4-157. Signature Analysis Path. Use Loop E signatures.

a. If not all of the MIC's output signals fail, depending on failure, check:

H/MIC0-3...U78, 112, 111, 94.
H/MIC4-7...U78, 112, 111, 95.

b. If all of the bits fail, check:

U108, 109, 111, 113, 77, 112, 114, 55, 74, 98, 88, 61, 80, 110, 94, 95, 89, 41.

4-158. COUNTING STATE.

4-159. How. This test checks the incrementing of the Time/State Counter when counting states. Only the lower 8 bits of this 24 bit counter are tested for incrementing; the upper 16 bits are only checked for zero. The Time/State Counter tests perform more exhaustive checking.

4-160. The Time/State Counter is reset and the State Recognition RAMs are loaded with a 'never count' specification. The Counter is clocked twice; once in an attempt to increment it and the second to store the Counter output data into the Time/State Storage RAM. The Time/State Storage RAM is then checked to make sure that the Counter did not increment.

4-161. The State Recognition RAMs are then loaded with a 'don't care' count specification and the Memory Index Counter is loaded with 0 so that the Measurement Complete Flag (H/MC) will not become set until after 256 clocks. The Time/State Counter is then clocked with a verification of increment in between each clock. Any discrepencies are indicated as a failure in the appropriate bit.

4-162. Results. Errors are decoded as follows:

Hex	Binary	Signal in error	Source
xxxxx=	0000 0000 0000 0000 0000 0000	None	
	---- ---- ---- ---- ---- ---1	CNT0	U81-14
	---- ---- ---- ---- ---- --1-	CNT1	U81-13
	---- ---- ---- ---- ---- -1--	CNT2	U81-12
	---- ---- ---- ---- ---- 1---	CNT3	U81-11
	---- ---- ---- ---- ---1 ----	CNT4	U82-14
	---- ---- ---- ---- --1- ----	CNT5	U82-13
	---- ---- ---- ---- -1-- ----	CNT6	U82-12
	---- ---- ---- ---- 1--- ----	CNT7	U82-11
	---- ---- ---- ---1 ---- ----	CNT8	U83-14
	---- ---- ---- --1- ---- ----	CNT9	U83-13
	---- ---- ---- -1-- ---- ----	CNT10	U83-12
	---- ---- ---- 1--- ---- ----	CNT11	U83-11
	---- ---- ---1 ---- ---- ----	CNT12	U84-14
	---- ---- --1- ---- ---- ----	CNT13	U84-13
	---- ---- -1-- ---- ---- ----	CNT14	U84-12
	---- ---- 1--- ---- ---- ----	CNT15	U84-11
	---- ---1 ---- ---- ---- ----	CNT16	U85-14
	---- --1- ---- ---- ---- ----	CNT17	U85-13
	---- -1-- ---- ---- ---- ----	CNT18	U85-12
	---- 1--- ---- ---- ---- ----	CNT19	U85-11
	---1 ---- ---- ---- ---- ----	CNT20	U86-14
	--1- ---- ---- ---- ---- ----	CNT21	U86-13
	-1-- ---- ---- ---- ---- ----	CNT22	U86-12
	1--- ---- ---- ---- ---- ----	CNT23	U86-11

Time/State Counter - 24 bit

U86 --- U85 --- U84 --- U83 --- U82 --- U81
MSB <---------- LSB

Time/State Storage RAMs - 24 bit

U70 --- U69 --- U68 --- U67 --- U66 --- U65
MSB <---------- LSB

4-163. Signature Analysis Path. Use Loop E Signatures.

a. If not all of the Counter output signals fail, depending on failure, check:

CNT0-3.....U112, 114, 106, 65, 81.
CNT4-7.....U112, 114, 106, 65, 82.
CNT8-11....U112, 114, 106, 67, 83.
CNT12-15...U112, 114, 106, 68, 84.
CNT16-19...U112, 114, 106, 69, 85.
CNT20-23...U112, 114, 106, 70, 86.

b. If all of the bits fail, check:

U111, 113, 108, 109, 112, 14, 55, 76, 93, 94, 95, 88, 110, 106, 107, 98, 74, 65, 66, 67, 68, 69, 70, 81, 82, 83, 84, 85, 86.

4-164. OCCURRENCE COUNTER.

4-165. A failure indicates an error in counting occurrences of a trigger in the occurrence counter or lockout circuit.

4-166. How. The control word is set so that AME1 and AME2 are configured as the trigger resource, and the Occurrence Counter is loaded with zero. The State Recognition RAMs are loaded with a 'don't care trigger' for resource AME2 so that the Occurrence Counter increments each time it is clocked. The analyzer is put into the 'run' mode and the Occurrence Counter is clocked 65,535 times. At this time, the Occurrence Counter should be set at FFFFH, and the carry flag (H/OCC) of this counter should be reset. The flags are read to make sure that a Trace Point has not occurred.

4-167. After this check, the Occurrence Counter is clocked again, which should cause H/OCC to become set, and produce a Trace Point. The Occurrence Counter is then loaded with 65,534 and the State Recognition RAMS are loaded with a 'never trigger' specification for AME1 and AME2, and a 'don't care' specification for Range. Because Range was not configured as the trigger resource, it should not cause an increment of the Occurrence Counter.

4-168. To verify this, the Occurrence Counter is clocked twice and then checked to make sure it did not increment. The control word is then set so that Range is the trigger resource. The Occurrence Counter is clocked twice which should cause a carry and resulting setting of the Trace Point Flag. Any discrepency in any of the above tests is indicated as a failure.

Occurrence Counter - 16 bit

U87 --- U121 --- U104 --- U103
MSB <---------- LSB

4-169. Signature Analysis Path. Use Loop E signatures and check:

U111, 113, 108, 109, 77, 112, 72, 98, 74, 55, 107, 87, 121, 104, 103, 41.

4-170. STORE QUALIFICATION.

4-171. How. The store qualification logic is tested by verifying that a false signal keeps a nontrigger state (everything but Trace Point) from being stored and that a true signal causes these states to be stored. All combinations of sources for store qualify and trigger are tested.

4-172. The State Recognition RAMs are loaded with a 'never trigger' and a 'never store' specification. First, Range and then AME1 and AME2 are configured by the control word as the storage qualification resource. Because the Memory Address Counter (MAC) is used to indicate the number of stored states, it is also used to verify storage qualification. With the above configuration, the MAC is clocked and then checked to see if it incremented. If it did, a failure is indicated at the bit 0 position of the error display.

4-173. The control word is then configured so that first AME1 and AME2 is the trigger resource and then Range is the trigger resource. The State Recognition RAMs are loaded with a 'don't care' specification, first for AME1 and then Range. For each case the MAC is clocked in conjunction with a trigger state and a nontrigger state. The MAC should have incremented only once, indicating a storage of the trigger state. If the MAC is not set at 1, then a failure is indicated in the bit 1 position of the error display.

4-174. The control word is then set such that AME1 and AME2 are the storage qualification resource and Range is the trigger resource. The State Recognition RAMs are loaded with 'don't care' for AME1 and 'never' for AME2 and Range. The MAC is then locked and should have incremented; if not, a failure is indicated in the bit 2 position of the error display. The State Recognition RAMs are then loaded with 'don't care' for AME2 and 'never' for AME1 and Range. The MAC is clocked and should increment; if not, a failure is indicated in the bit 3 position of the error display.

4-175. The control word is then set so that Range is the storage qualification resource and AME1 and AME2 are the trigger resource. The State Recognition RAMs are loaded with 'don't care' for Range and 'never' for AME1 and AME2. The MAC is clocked and should increment; if not, a failure is indicated in the bit 4 position of the error display.

4-176. Results. Errors are decoded as follows:

Hex	Binary	Error condition
xx =	0000 0000	None
	000- ---1	Store Qualification is ON when it should be OFF
	000- --1-	Only Trigger Stored check fails
	000- -1--	AME1 Store Qualify check fails
	000- 1---	AME2 Store Qualify check fails
	0001 ----	Range Store Qualify check fails

4-177. Signature Analysis Path. Use Loop E Signatures and check:

U111, 113, 108, 109, 77, 112, 74, 75, 98, 100, 110 80, 107, 61, 41, 55, 88, 94, 95.

4-178. TRACE POINT.

4-179. How. The State Recognition RAMs are loaded with 'never trigger' and 'never store' specification. The analyzer is put into 'run' mode and is sent trace states. The analyzer is then halted and both the Trigger Enable Point Flag (H/TEP) and the Trace Point Flag (H/TP) are checked to make sure they were not set. If either were then a failure is indicated.

4-180. The State Recognition RAMS are then loaded with 'don't care trigger' and 'never store' specification. The analyzer is then put into 'run' mode and is sent trigger states. The analyzer is then halted and the flags H/TEP and H/TP are checked again. They both should now be set, otherwise a failure is indicated.

4-181. The State Recognition RAMs are then loaded with a 'never trigger', and a 'don't care store' specification and the flags are reset. The analyzer is then put into 'run' mode and is sent trace states. The analyzer is then halted and the flags H/TEP and H/TP are again checked. Both should be reset, otherwise a failure is indicated.

4-182. Results. Errors are decoded as follows:

Hex	Binary	Error condition
x =	0000	None
	00-1	H/TP, Trace Point flip-flop error
	001-	H/TEP, Trigger Enable Point flip-flop error

4-183. Signature Analysis Path. Use Loop E Signatures and check:

U111, 113, 108, 109, 77, 112, 72, 74, 75, 98, 100, 41, 55.

4-184. MEASUREMENT COMPLETE.

4-185. Failure indicates the Measurement Complete flip-flop did not detect/store the Memory Index Counter overflow.

4-186. How. The State Recognition RAMs are loaded with a 'don't care trigger' and a 'store-qualify' specification so that Measurement Complete occurs. The analyzer is reset and the Memory Index Counter (MIC) is loaded with 255 so Measurement Complete occurs at Trace Point. The analyzer is then put into 'run' mode followed by a check of the Measurement Complete Flag (H/MC). If it is not reset, then a failure is indicated. The analyzer is then clocked, followed by another check of H/MC. If it is not set at this point, then a failure is indicated.

4-187. Signature Analysis Path. Use Loop E signatures and check:

U111, 113, 108, 109, 77, 112, 88, 74, 75, 98, 100, 110, 80, 107, 61, 41, 55, 94, 95.

4-188. IMB TEST DISPLAY.

4-189. Purpose. This display shows the two IMB test categories available and their test results. Use the display to review test conditions or to select an individual test for more detailed review or further execution. The External Stimulus test only appears when another wide logic analyzer is in the card cage and has been selected for external stimulus.

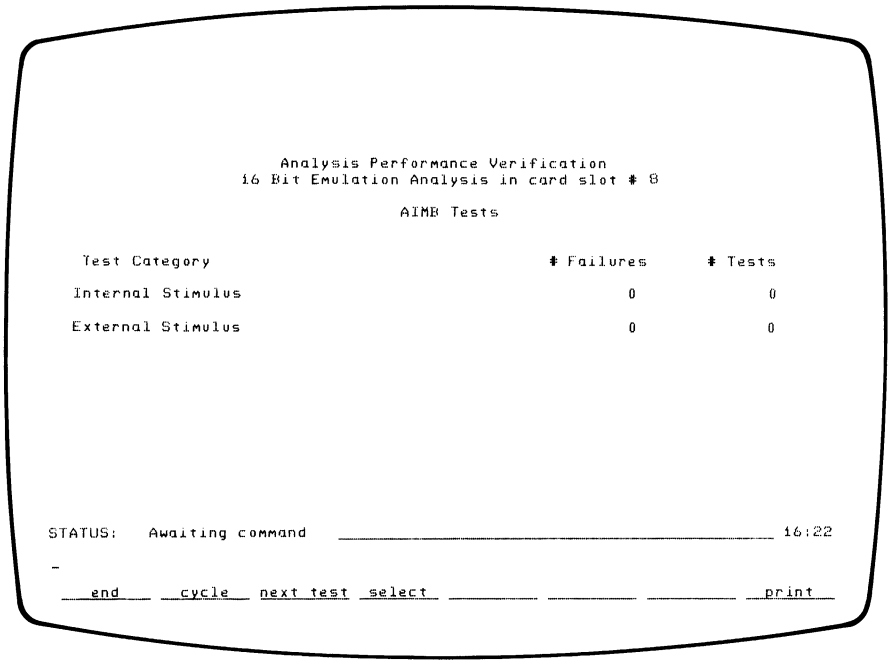


Figure 4-13. IMB Display

4-190. Running the IMB Tests. Press the <Cycle> softkey to run both the test categories shown; execution time is less than on second per iteration. To stop the iterations press the <Cycle> softkey again.

4-191. Using the IMB Results. The # Failures column shows the total number of errors detected during the tests. Determine the specific cause of the error by reviewing the failed test category in detail; it is reached by moving the highlight line to the test category and pressing the <Select> softkey.

4-192. IMB INTERNAL STIMULUS TEST DISPLAY.

4-193. Purpose. The six tests shown indicate the board's ability to drive and receive IMB signals. Use the display to review test results in detail or to execute the tests.

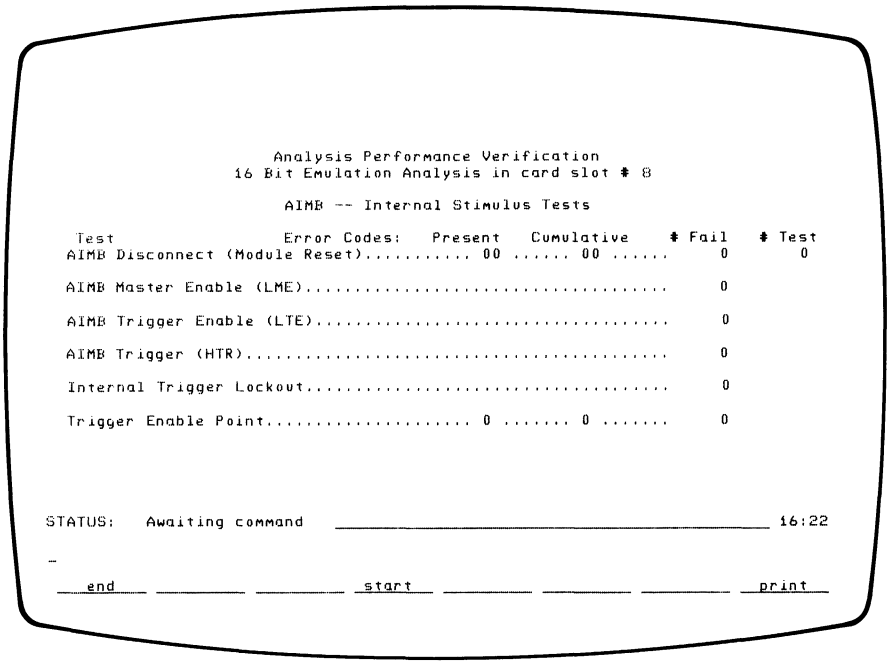


Figure 4-14. IMB Internal Stimulus Display

4-194. Running the IMB Internal Stimulus Tests. Press the <Start> softkey to begin. The tests continue until the <Start> softkey is pressed again. Execution time is less than one second per iteration.

4-195. Using the IMB Internal Stimulus Results. The total number of errors detected during the tests is shown in the # Fail column. Each error code in the Present column represents a single failure encountered during the last iteration. Each error code in the Cumulative column represents the sum of all errors detected during the test. Cumulative error codes that differ from Present error codes indicate multiple, or intermittent errors. When the error codes are the same the errors are systematic.

4-196. IMB DISCONNECT.

4-197. How. The analyzer is put into 'halt' mode and the control word is set so that all IMB functions are off. The State Recognition RAMS are then loaded with a 'never trigger' specification and the analyzer is reset and then put into 'run' mode. The Trace Point (H/TP), IMB Trigger Enable (H/TEF), IMB Trigger (H/XTR), Trigger Enable Point (H/TEP), and Run/Halt (H/RUN) flags are checked. Any discrepency against the expected state of these flags are indicated as a failure. The analyzer is then put into the 'halt' mode and then Run/Halt flag is checked to make sure it is reset.

4-198. Results. Errors are decoded as follows:

Hex	Binary	Signal in Error	Source
xx =	0000 0000	None	
	000- ---1	H/TP	U72-7
	000- --1-	H/TEF	U39-3
	000- -1--	H/TR	U24-4
	000- 1---	H/TEP	U72-9
	0001 ----	H/RUN	U41-3

4-199. Signature Analysis Path. Use Loop F Signatures.

a. If H/TP (Trace Point Flag), check:
U108, 109, 111, 113, 77, 98, 72, 71.

b. If H/TR (AIMB Trigger Flag), check:
U108, 109, 111, 113, 77 98, 24, 72, 1, 19, 3.

c. If H/TEP (Trigger Enable Point Flag), check:
U108, 109, 111, 113, 77, 98, 74, 72, 71.

d. If H/RUN (Run/Halt Flag), check:
U108, 109, 111, 113, 77, 112, 41, 5, 88, 71, 61, 107, 115, 6.

4-200. IMB MASTER ENABLE.

4-201. Failure indicates a stuck EL/ME line or problem with the ECL/TTL translators or associated selection ciruitry.

4-202. How. The control word is set so that EL/ME is both driven and received, and the State Recognition RAMs are loaded with a 'never trigger' specification. The analyzer is reset and then put into the 'run' mode, followed by a check of the Run/Halt Flag. If it is not set then a failure is indicated. The analyzer is then put into the 'halt' mode and the Run/Halt Flag is checked again. If it is not reset then a failure is indicted.

4-203. Signature Analysis Path. Use Loop F signatures and check:

U108, 109, 111, 113, 77, 112, 41, 19, 24, 59, 5, 88, 71, 61, 107, 115, 6, 98, 74.

4-204. IMB TRIGGER ENABLE.

4-205. Failure indicates a stuck EL/TE line or problem with the ECL-TTL translators, the ECL flip-flop that stores the EL/TE levels, or associated selection circuitry.

4-206. How. The control word is set so EL/TE is received and the State Recognition RAMs are loaded with a 'never trigger' specification. Note that undriven IMB signals are pulled low. The analyzer is then reset followed by a check of the IMB Trigger Enable Flag (H/TEF). If H/TEF is not reset, a failure is indicated. A PV strobe is then sent which should set H/TEF. If it is not, a failure is indicated. The analyzer is then reset followed by another check of H/TEF, which should now be reset. If it is not, a failure is indicated.

4-207. Signature Analysis Path. Use Loop F signatures and check:

U108, 109, 111, 113, 77, 98, 39, 72, 1, 19, 3, 74, 55.

4-208. IMB TRIGGER.

4-209. Failure indicates a stuck EH/TR line or a problem with the ECL/TTL translators, the ECL flip-flop that stores EH/TR levels, the EH/TR lockout circuit, or associted circuitry.

4-210. How. The control word is set so that the IMB trigger is received and the State Recognition RAMs are loaded with a 'don't care trigger' specification. The analyzer is reset followed by a check of the EH/TR flag which should be reset. If not, a failure is indicated. A PV strobe is sent followed by another check of the EH/TR flag which should still be reset. If not, a failure is indicated.

4-211. The control word is then set so that EH/TR is driven. The analyzer is reset and then two PV strobes are sent; the first to set Trace Point and drive the EH/TR line high and the second to latch the state on the EH/TR line into the EH/TR flag. The control word is then changed so that EH/TR is received. If it is not set, then a failure is indicated. Two more PV strobes are sent to check out the EH/TR flag lockout feed-back. If it does not stay set, then a failure is indicated. Finally, the analyzer is reset followed by another check of the EH/TR flag which should be reset. If not, a failure is indicated. The EH/TR flag is checked by checking the status of the IMB External Trigger Flag (H/XTR).

4-212. Signature Analysis Path. Use Loop F Signatures and check:

U108, 109, 111, 113, 77, 98, 24, 72, 1, 19, 3, 74, 55.

4-213. INTERNAL TRIGGER LOCKOUT.

4-214. Failure indicates the EL/TE is failing to inhibit triggering; for example, not setting Trace Point or decrementing the Occurrence Counter.

4-215. How. The control word is set so that EL/TE is both driven and received and AME1 or AME2 is the trigger resource. The State Recognition RAMs are loaded with a 'don't care trigger' specification. The Memory Index Counter is loaded with 0 so that Measurement Complete does not occur during the test and the Occurrence Counter is loaded with 65,535 so that a single trigger will cause a Trace Point.

4-216. The analyzer is reset and then two PV strobes are sent, the first to latch the state of the EL/TE line into the EL/TE latch and the second to make sure that a trigger is locked out from setting the Trace Point Flag. The Trace Point Flag is checked and should be reset. If not, a failure is indicated. The control word is then changed to make Range the trigger resource and the sequence of events explained in the last paragraph are executed again.

4-217. Signature Analysis Path. Use Loop F signatures and check:

U108, 109, 111, 113, 77, 112, 41, 19, 24, 59, 5, 88, 72, 71, 61, 107, 115, 6, 98, 74, 94, 95.

4-218. TRIGGER ENABLE POINT.

4-219. How. The control word is set for a separate Trigger Enable Point and the State Recognition RAMs are loaded with a 'don't care trigger' specification. The Memory Index Counter is loaded with 0 so that Measurement Complete does not occur during the test, and the Occurrence Counter is loaded with 65,535 so that a single trigger can cause a Trace Point.

4-220. The analyzer is reset and a PV strobe is sent, which should set Trigger Enable Point Flag but not the Trace Point Flag. These flags are then checked and any discrepency is indicated in the appropriate bit position of the error display. Two more PV strobes are sent followed by another check of these two flags. Any change of their state is shown in the appropriate bit position of the error display.

4-221. Results. Errors are decoded as follows:

Hex	Binary	Error condition
x =	0000	None
	00-1	Trace Point flip-flop error
	001-	Trigger Enable Point flip-flop error

4-222. Signature Analysis Path. Use Loop F signatures and check:

U108, 109, 111, 113, 77, 112, 41, 19, 24, 59, 5, 88, 72, 71, 61, 107, 6, 98, 74, 94, 95.

4-223. IMB EXTERNAL STIMULUS TEST DISPLAY.

4-224. Purpose. The four tests on this display show the board's ability to receive IMB signals from another board. This screen only appears when another board which uses IMB functions is installed in the card cage. Another wide logic analyzer can be used. The analyzer being tested is referred to as the test module and the stimulus board is referred to as the stimulus module.

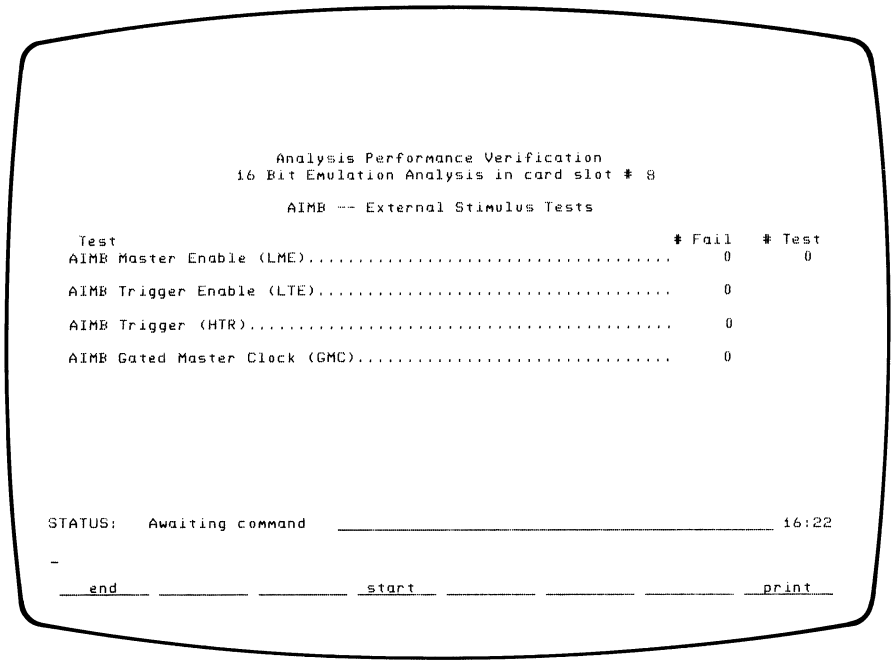


Figure 4-15. IMB External Stimulus Display

4-225. Running the IMB External Stimulus Test. Press the <Start> softkey to begin; the tests continue until the <Start> softkey is pressed again. Each iteration takes less than one second.

4-226. Using the IMB External Stimulus Results. The total number of errors detected during the tests is shown in the # Fail column. Each error code in the Present column represents a single failure encountered during the last iteration. Each error code in the Cumulative column represents the sum of all errors detected during the test. Cumulative error codes that differ from Present error codes indicate multiple, or intermittent errors. When the error codes are the same the errors are systematic.

4-227. IMB MASTER ENABLE.

4-228. Failure indicates a problem communicating with an external module over the IMB EL/ME line.

4-229. How. This set of tests checks communication over the EL/ME line. First, EL/ME is driven by the analyzer under test with EL/ME being monitored by the stimulus module. Then, EL/ME is received by the analyzer under test while the stimulus module drives EL/ME to the requested state.

4-230. The control word is set so the test module drives EL/ME and the State Recognition RAMs are loaded with a 'don't care trigger' specification. The analyzer is reset and the state of EL/ME is checked from the stimulus module, which should be high. If not, an EL/ME failure is indicated. The test module is then put into the 'run' mode and again the state of EL/ME is checked from the stimulus module, which now should be low. If not, a EL/ME failure is indicated.

4-231. The analyzer is then put into the 'halt' mode. The type of stimulus module is checked to make sure it has the capability to receive EL/ME. If it doesn't, then all failure information is discarded for this test. The type of stimulus module is checked to make sure that it has the capability to drive EL/ME. If it doesn't then the rest of this test is skipped. If it does then the control word is set so that EL/ME is received by the test module and the State Recognition RAMs are loaded with a 'never trigger' specification.

4-232. The analyzer is reset and the stimulus module is set to drive EL/ME low. The analyzer is put into the 'run' mode and the Run/Halt Flag is checked to make sure that it is set. If not a EL/ME failure is indicated. The stimulus module is then set to drive EL/ME high. The Run/Halt Flag is checked again which should now be reset. If not a EL/ME failure is indicated. The control word on the test module is then set so that EL/ME is no longer received; it does nothing. The Run/Halt Flag is checked and should be now set. If not a EL/ME failure is indicated.

4-233. IMB TRIGGER ENABLE.

4-234. Failure indicates a problem communicating with an external module over the IMB EL/TE line.

4-235. How. This set of tests checks communication over the EL/TE line. First, EL/TE is driven by the analyzer under test with EL/TE being monitored by the stimulus module. Then, EL/TE is received by the analyzer under test while the stimulus module drives EL/TE to the requested state.

4-236. The Occurrence Counter is loaded with 65,535 so that one trigger causes a Trace Point. The control word is set so that the test module drives EL/TE and the State Recognition RAMs are loaded with a 'don't care trigger' specification. The analyzer is reset and the

state of EL/TE is checked from the stimulus module, which should be high. If not, an EL/TE failure is indicated.

4-237. A PV strobe is then sent which should cause a Trace Point and drive EL/TE low. The state of EL/TE is checked from the stimulus module. If EL/TE is not low, a failure is indicated. The stimulus module is then checked to make sure it has the capability to receive EL/TE. If not any failure infromation gathered thus far is discarded.

4-238. The stimulus module is checked to make sure it has the capability to drive EL/TE. If it doesn't, then the rest of this test is not executed. If it does, the control word on the test module is set so EL/TE is received, and the State Recognition RAM are loaded with a 'never trigger' specification.

4-239. The analyzer is reset and the stimulus module is set to drive EL/TE low. A PV strobe is sent to clock the state of EL/TE into the EL/TE flip-flop. The Trigger Enable Flag is read and should be set. If not, a EL/TE failure is indicated. The stimulus module is then set to drive EL/TE high. A PV strobe is sent to clock the state of EL/TE into the EL/TE flip-flop. The Trigger Enable Flag is checked and should be reset. If not a EL/TE failure is indicated.

4-240. IMB TRIGGER.

4-241. Failure indicates a problem communicating with an external module over the IMB EH/TR line.

4-242. How. This set of tests checks communication over the EH/TR line. First, EH/TR is driven by the analyzer under test with EH/TR monitored by the stimulus module. Then, EH/TR is received by the analyzer under test while the stimulus module drives EH/TR to the requested state.

4-243. The Occurrence Counter is loaded with 65,535 so only one trigger is needed for Trace Point. The control word is set so that the test module is driving EH/TR, and the State Recognition RAMs are loaded with a 'don't care trigger' specification. The analyzer is reset and then a PV strobe is sent which should set the Trace Point Flag. This is checked through the stimulus module. If EH/TR is not high, then an EH/TR failure is indciated.

4-244. The analyzer is reset and again the state of the EH/TR is line is checked through the stimulus module. If it is not low, then an EH/TR failure is indicated. The type of stimulus module is then checked to make sure it has the capability to receive EH/TR. If not then the failures gathered are discarded.

4-245. The type of stimulus module is also checked to make sure it can drive EH/TR. If it cannot, then the rest of this test is not performed. If it does, the control word on the test module is set to recieve EH/TR, and the State Recognition RAMs are loaded with a 'never trigger' specification. The analyzer is reset and the stimulus module is set to drive EH/TR line high. A PV stobe is sent to the test

module to clock the EH/TR flip-flop. The IMB External Trigger Flag (H/XTR) is read and should be set. If not, an EH/TR failure is indicated. Another PV strobe is sent to clock the state of a trigger into the Trace Point Flag. The Trace Point Flag is checked and should be high. If not a EH/TR failure is indicated.

4-246. The control word on the test module is changed so that EH/TR is no longer received; it does nothing. The IMB External Trigger Flag is checked and should be reset. If not, an EH/TR failure is indicated. The control word on the test module is changed so that EH/TR is again received. The stimulus module is set to drive EH/TR low. The analyzer is reset and then a PV strobe is sent to clock the IMB External Trigger Flag. This flag is checked to make sure that it iis low. If not, an EH/TR failure is indicated.

4-247. IMB GATED MASTER CLOCK.

4-248. Failure indicates a problem sending L/ANAL clock signals to an external module over the IMB GMC line.

4-249. How. The following test verifies that analysis clocks can be sent out over the GMC line. Note that this test is not performed when another analyzer is selected as the IMB stimulus module. A stimulus module that can receive GMC and can count pulses is required for this test, otherwise this test is skipped.

4-250. The control word is set so that the test module is driving the GMC line. The stimulus module is set to expect 255 clock pulses. The 255 PV strobes are then sent via the test module over the GMC line. The stimulus module is checked to make sure it received the expected 255 clock pulses. If more or less, a GMC failure is indicated.

```
********************  NOTE  ********************
*                                               *
*  All four of the above failures can be caused *
*  by the analyzer under test, the connecting   *
*  cables, or the external module.              *
*                                               *
*************************************************
```

4-251. TIME/STATE COUNTER TEST DISPLAY.

4-252. Purpose. This display shows the two counter test categories available and their test results. Use the display to review test conditions or to select an individual test for more detailed review or futher execution.

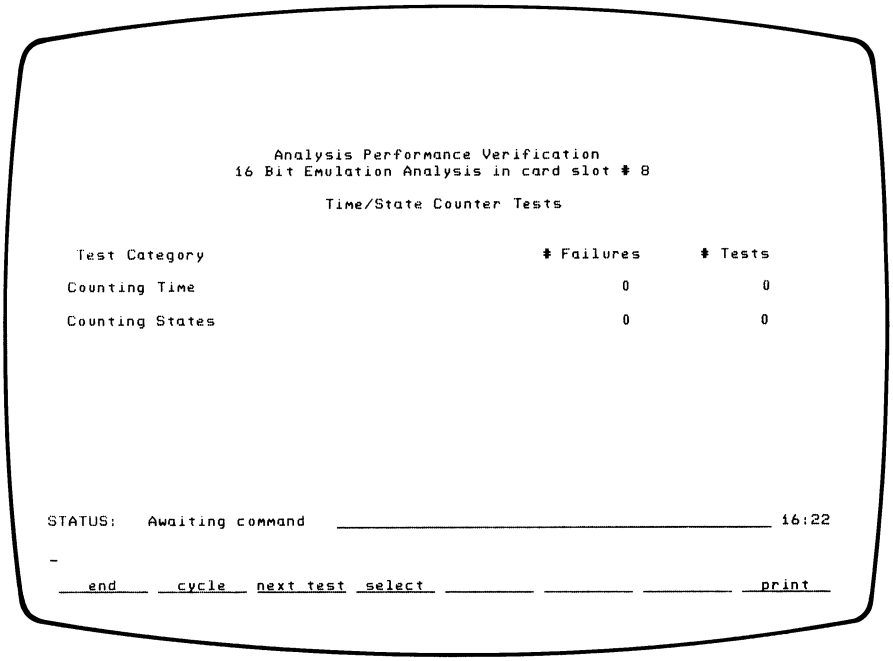


Figure 4-16. Time/State Counter Display

4-253. Running the Time/State Counter Tests. Press the <Cycle> softkey to run both the test categories. The tests continue until the <Cycle> softkey is pressed again. Each iteration takes less than one second.

4-254. Using the Time/State Counter Results. The # Failures column shows the total number of errors detected during the tests. Determine the specific cause of the error by reviewing the failed test category in detail; it is reached by moving the highlight line to the test category and pressing the <Select> softkey.

4-255. COUNTING TIME TEST DISPLAY.

4-256. Purpose. Shown on the display are two tests that indicate the board's ability to correctly count time increments during analysis. Use the display to execute the tests or to review test results in detail.

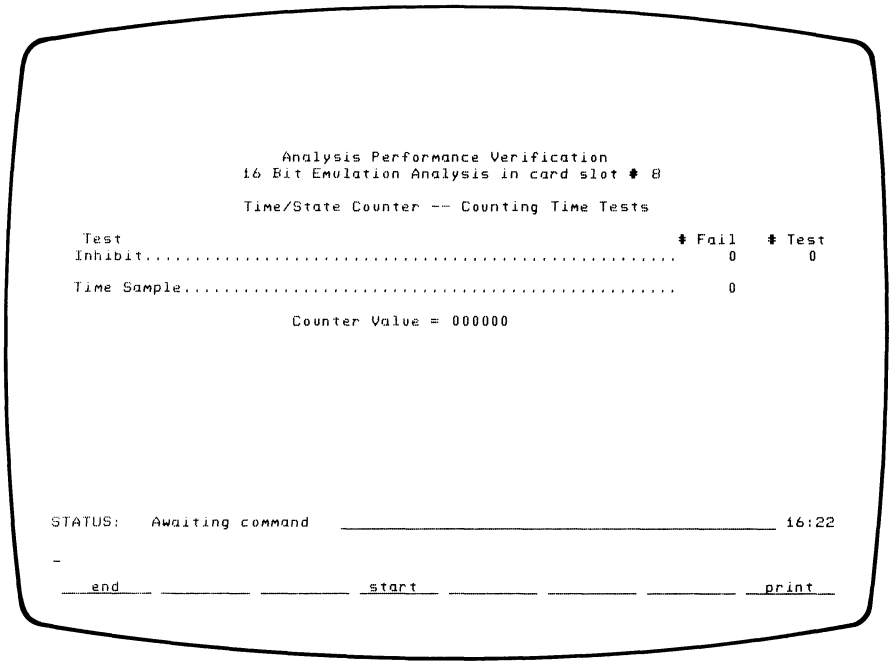


Figure 4-17. Counting Time Display

4-257. Running the Counting Time Tests. Press the <Start> softkey to begin; the tests continue until the <Start> softkey is pressed again. Time for each iteration is less than one second.

4-258. Using the Counting Time Results. The total number of errors detected during the tests is shown in the # Fail column.

4-259. INHIBIT.

4-260. Failure indicates the divide-by-16 counter is not being disabled via H/TCE when the analyzer is in the halt mode.

4-261. How. This test is performed immediately after the Time Sample test. The time value read there is saved and the analyzer is halted.

The background line (L/BKG) should be high so that the Run/Halt Flag has full control over the time count inhibit function. A time of at least 640 ns is waited by the host CPU so that at least one time tick can occur if the inhibit function was not working. A PV strobe is sent to write the data from the Time/State Counters into the Time/State RAMs. This value is read from the Time/State RAMs and compared to the value saved earlier. If the two values are not the same then an inhibit failure is indicated.

4-262. TIME SAMPLE.

4-263. Failure indicates an error in the count time synchronizer, divide-by-16, or associated circuitry (if Count States tests pass). The Time Sample test fails when the counter value, after a specified time, is not between 100000H and 1FFFFFH (1,048,576 and 2,097,151) inclusive. When a failure occurs, the screen displays below the Time Sample test, 'Counter Value = xxxxxx'.

4-264. How. If an emulator is connected to the analyzer (via emulation bus cables) then the type of emulator is checked to see if it is an 8080, 8085, Z80, or 6800 and that emulation memory is present. If one of these emulators is present then an appropriate program is loaded into emulation memory and the emulator is released to run that program. This ensures that the background line L/BKG, is high, allowing the Time/State Counter to count. If none of these emulators are present then this section of the test is skipped.

4-265. The Memory Index Counter (MIC) is loaded with 0 so that the Measurement Complete Flag is not set during the test. The control word is set for time counting and the State Recognition RAMs are loaded with a 'never trigger', 'never store' specification. All option slot interrupts are disabled and the analyzer is reset.

4-266. The analyzer is put into the 'run' mode and then the host CPU waits for 1 second. After that time the Memory Address Counter (MAC) is set to 0 and a PV strobe is sent to write the data from the Time/State Counter into the the Time/State RAMs , location 0. The value stored in these RAMs is read to make sure it lies between 100000 and 1FFFFFH (1,048,576 and 2,097,151). If it does not, a time sample failure is indicated and the value that was read is displayed. Both the anlayzer and emulator are then reset.

4-267. EIGHT BIT EMULATORS.

4-268. The Time Sample test fails when an 8 bit emulator is connected to the analyzer but without emulator memory. When this is the only test that fails, remove the emulator bus cables and rerun the test.

4-269. This is because 8 bit emulators use a background memory format for executing emulator commands, while 16 bit emulators use a monitor which is located in foreground memory. Eight bit emulators, while in background memory, inhibit Time/State Counting.

4-270. COUNTING STATES TEST DISPLAY.

4-271. Purpose. The five tests on this display show the analyzer's capabilities to count emulator states. Use the display to run the tests or to review test results in detail.

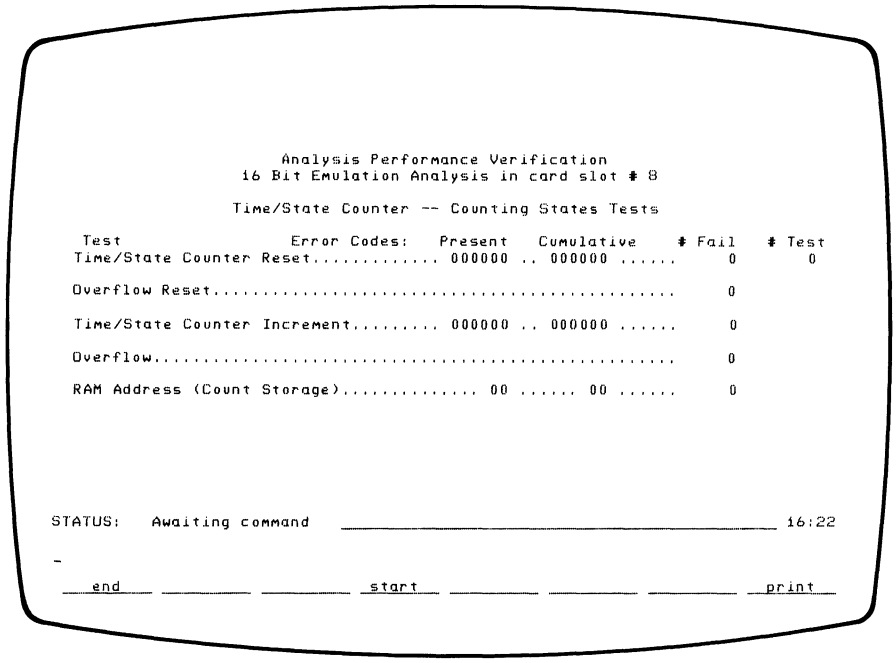


Figure 4-18. Counting States Display

4-272. Running the Counting States Tests. Press the <Start> softkey to begin; the tests continue until the <Start> softkey is pressed again. Each iteration takes about one minute.

4-273. Using the Counting State Results. The total number of errors detected during the tests is shown in the # Fail column. Each error code in the Present column represents a single failure encountered during the last iteration. Each error code in the Cumulative column represents the sum of all errors detected during the test. Cumulative error codes that differ from Present error codes indicate multiple, or intermittent errors. When the error codes are the same the errors are systematic.

4-274. TIME/STATE COUNTER RESET.

4-275. How. The analyzer is put into the 'halt' mode and reset so that the Time/State Counter is cleared. A PV strobe is sent to write this zero count in the Time/State Counter into the Time/State RAMs. This 24 bit value is read from the RAMs and checked to make sure it is zero. If not, a failure is indicated in the appropriate bit of the error display.

4-276. Results. Errors are decoded as follows:

Hex	Binary	Signal in error	Source
xxxxx=	0000 0000 0000 0000 0000 0000	None	
	---- ---- ---- ---- ---- ---1	CNT0	U81-14
	---- ---- ---- ---- ---- --1-	CNT1	U81-13
	---- ---- ---- ---- ---- -1--	CNT2	U81-12
	---- ---- ---- ---- ---- 1---	CNT3	U81-11
	---- ---- ---- ---- ---1 ----	CNT4	U82-14
	---- ---- ---- ---- --1- ----	CNT5	U82-13
	---- ---- ---- ---- ---- ----	CNT6	U82-12
	---- ---- ---- ---- 1--- ----	CNT7	U82-11
	---- ---- ---- ---1 ---- ----	CNT8	U83-14
	---- ---- ---- --1- ---- ----	CNT9	U83-13
	---- ---- ---- -1-- ---- ----	CNT10	U83-12
	---- ---- ---- 1--- ---- ----	CNT11	U83-11
	---- ---- ---1 ---- ---- ----	CNT12	U84-14
	---- ---- --1- ---- ---- ----	CNT13	U84-13
	---- ---- -1-- ---- ---- ----	CNT14	U84-12
	---- ---- 1--- ---- ---- ----	CNT15	U84-11
	---- ---1 ---- ---- ---- ----	CNT16	U85-14
	---- --1- ---- ---- ---- ----	CNT17	U85-13
	---- -1-- ---- ---- ---- ----	CNT18	U85-12
	---- 1--- ---- ---- ---- ----	CNT19	U85-11
	---1 ---- ---- ---- ---- ----	CNT20	U86-14
	--1- ---- ---- ---- ---- ----	CNT21	U86-13
	-1-- ---- ---- ---- ---- ----	CNT22	U86-12
	1--- ---- ---- ---- ---- ----	CNT23	U86-11

Time/State Counter - 24 bit

U86 --- U85 --- U84 --- U83 --- U82 --- U81
MSB <---------- LSB

Time/State Storage RAMs - 24 bit

U70 --- U69 --- U68 --- U67 --- U66 --- U65
MSB <---------- LSB

4-277. OVERFLOW RESET.

4-278. Failure indicates the Overflow flip-flop did not reset when a module reset command was given.

4-279. How. The analyzer is reset to clear the counter overflow flag, H/OV, and then the status of this flag is checked. If it is not reset, then on Overflow Reset failure is indicated.

4-280. TIME/STATE COUNTER INCREMENT.

4-281. This test determines if the Time/State Counter can properly increment through its entire range. This test supplements the Count State test which is contained in the Run Mode tests.

4-282. How. The control word is set for counting states and the State Recognition RAMs arer loaded with a 'don't care' for count qualification. This allows the Time/State Counter to increment. The analyzer is reset to make sure the Time/State and Memory Address Counters are zero.

4-283. PV strobes are then sent to increment the Time/State Counter to F80001H (16,252,930). After every 8000H (32,768) strobes, the most significant bits of Time/State Counter (which have been written in the Time/State RAMs) are checked. Any discrepencies are indicated as failures in the appropriate bit of the error display.

4-284. Then, 70000H (458,752) more PV strobes are sent to increment the counter to FF0001H (16,711,682). After every 10000H (65,536) strobes the lower three bits of the most significant bit of the Time/-State Counter are checked. Any discrepencies are indicated as failures in the appropriate bits of the error display. Then, FF00H (65,280) more PV strobes are sent to increment the counter to FFFF01H (16,776,962). After every 255 strobes the middle byte of the Time/State Counter is checked. Any discrepencies are indicated as failures in the appropriate bits of the error display.

4-285. Results. Errors are decoded as follows:

Hex xxxxx=	Binary	Signal in error	Source
	0000 0000 0000 0000 0000 0000	None	
	---- ---- ---- ---- ---- ---1	CNT0	U81-14
	---- ---- ---- ---- ---- --1-	CNT1	U81-13
	---- ---- ---- ---- ---- -1--	CNT2	U81-12
	---- ---- ---- ---- ---- 1---	CNT3	U81-11
	---- ---- ---- ---- ---1 ----	CNT4	U82-14
	---- ---- ---- ---- --1- ----	CNT5	U82-13
	---- ---- ---- ---- -1-- ----	CNT6	U82-12
	---- ---- ---- ---- 1--- ----	CNT7	U82-11
	---- ---- ---- ---1 ---- ----	CNT8	U83-14
	---- ---- ---- --1- ---- ----	CNT9	U83-13
	---- ---- ---- -1-- ---- ----	CNT10	U83-12
	---- ---- ---- 1--- ---- ----	CNT11	U83-11
	---- ---- ---1 ---- ---- ----	CNT12	U84-14
	---- ---- --1- ---- ---- ----	CNT13	U84-13
	---- ---- -1-- ---- ---- ----	CNT14	U84-12
	---- ---- 1--- ---- ---- ----	CNT15	U84-11
	---- ---1 ---- ---- ---- ----	CNT16	U85-14
	---- --1- ---- ---- ---- ----	CNT17	U85-13
	---- -1-- ---- ---- ---- ----	CNT18	U85-12
	---- 1--- ---- ---- ---- ----	CNT19	U85-11
	---1 ---- ---- ---- ---- ----	CNT20	U86-14
	--1- ---- ---- ---- ---- ----	CNT21	U86-13
	-1-- ---- ---- ---- ---- ----	CNT22	U86-12
	1--- ---- ---- ---- ---- ----	CNT23	U86-11

Time/State Counter - 24 bit

U86 --- U85 --- U84 --- U83 --- U82 --- U81
MSB <---------- LSB

Time/State Storage RAMs - 24 bit

U70 --- U69 --- U68 --- U67 --- U66 --- U65
MSB <---------- LSB

4-286. OVERFLOW.

4-287. Failure indicates the Overflow flip-flop did not detect/store an overflow by the Time/State Counter while counting states.

4-288. How. From the Time/State Counter Increment test the present count value should be at FFFF01H (16,776,692). Then, 254 more PV strobes are sent to increment the counter to FFFFFFH (16,777,216). The overflow flag (H/OV) is checked to make sure it is reset. If it is not then an Overflow failure is indicated. One more PV strobe is then sent followed by another check of the overflow flag. If it is not now set, then an Overflow failure is indicated.

4-289. RAM ADDRESS (Count Storage).

4-290. How. Incorrect addressing by a Time/State RAM might not be detected by previous tests. During the Overflow test the Memory Address Counter (MAC) is loaded with successive values from 01H thru FFH (255) followed by a PV strobe which strores FFFFH (65,535) into the upper 16 bits of Time/Count RAM. Thus, by the end of the Overflow test, all 256 RAM locations contain FFFFH in the upper word and the lower byte contains 00H through FFH.

4-291. The analyzer is reset to clear the Time/State Counter and the Memory Address Counter. A PV strobe is sent to write the value 0000H into the upper word of the Time/Count RAMs at location 00H. The MAC is then loaded with FFH and another PV strobe is sent to write 0000H into the upper word of the Time/ State RAMs at location FFH. All other RAM locations should contain FFFFH in the upper word. All Time/State RAM locations, other than 00H and FFH, are read to make sure that they contain FFFFH in the upper word. Any discrepency, is indicated as an error in the appropriate bit of the error display.

4-292. The analyzer is reset to clear the Time/State Counter and the Memory Address Counter. Then, PV strobes are sent increment the Time/State Counter to 0000FFH (255). This value is stored into all locations of the Time/State RAMs. 000000H is then stored into locations 00H and FFH of the Time/State RAMs. All locations other than 00H and FFH are then checked to make sure they contain 0000FFH. Any discrepency is indicated as a failure in the appropriate bit of the error display.

4-293. Results. Errors are decoded as follows:

Hex	Binary	Signal in error	Source
xx =	0000 0000	None	
	---- ---1	H/MAC0	U76-14
	---- --1-	H/MAC1	U76-13
	---- -1--	H/MAC2	U76-12
	---- 1---	H/MAC3	U76-11
	---1 ----	H/MAC4	U93-14
	--1- ----	H/MAC5	U93-13
	-1-- ----	H/MAC6	U93-12
	1--- ----	H/MAC7	U93-11

4-294. EMULATOR STIMULUS TEST DISPLAY.

4-295. Purpose. The seven tests on this display indicate the board's capability to receive signals from an attached emulator. Use the display to review test results in detail or to execute tests.

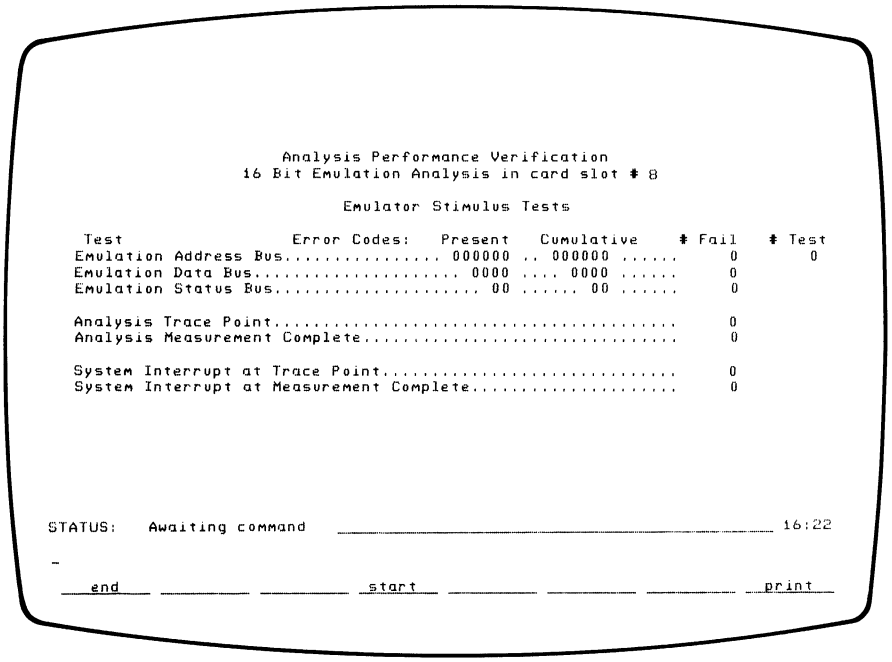


Figure 4-19. Emulator Stimulus Display

4-296. Running the Emulator Stimulus Tests. Press the <Start> softkey to begin. The tests continue until the <Start> softkey is pressed again. Each iteration takes less than one second.

4-297. Using the Emulator Stimulus Results. The total number of errors detected during the tests is shown in the # Fail column. Each error code in the Present column represents a single failure encountered during the last iteration. Each error code in the Cumulative column represents the sum of all errors detected during the test. Cumulative error codes that differ from Present error codes indicate multiple, or intermittent errors. When the error codes are the same, the errors are systematic.

```
********************  NOTE  ********************
*                                                *
*  This display only appears when there is  an   *
*  8080, 8085, Z80, 6800, or  6802 emulator in   *
*  the card cage.  However, it  only runs with   *
*  the 8080, 8085,  or  a  Z80 emulator in the   *
*  card cage.                                    *
*                                                *
**************************************************
```

4-298. EMULATOR ADDRESS BUS.

4-299. Results. Errors are decoded as follows:

Hex	Binary	Signal in error	Source
xxxxx=	0000 0000 0000 0000 0000 0000	None	
	0000 0000 ---- ---- ---- ---1	L/EA0	U14-3
	0000 0000 ---- ---- ---- --1-	L/EA1	U14-4
	0000 0000 ---- ---- ---- -1--	L/EA2	U14-7
	0000 0000 ---- ---- ---- 1---	L/EA3	U14-8
	0000 0000 ---- ---- ---1 ----	L/EA4	U14-13
	0000 0000 ---- ---- --1- ----	L/EA5	U14-14
	0000 0000 ---- ---- -1-- ----	L/EA6	U14-17
	0000 0000 ---- ---- 1--- ----	L/EA7	U14-18
	0000 0000 ---- ---1 ---- ----	L/EA8	U16-3
	0000 0000 ---- --1- ---- ----	L/EA9	U16-4
	0000 0000 ---- -1-- ---- ----	L/EA10	U16-7
	0000 0000 ---- 1--- ---- ----	L/EA11	U16-8
	0000 0000 ---1 ---- ---- ----	L/EA12	U16-13
	0000 0000 --1- ---- ---- ----	L/EA13	U16-14
	0000 0000 -1-- ---- ---- ----	L/EA14	U16-17
	0000 0000 1--- ---- ---- ----	L/EA15	U16-18

4-300. EMULATOR DATA BUS.

4-301. Results. Errors are decoded as follows:

Hex	Binary	Signal in error	Source
xxxx=	0000 0000 0000 0000	None	
	---- ---- ---- ---1	L/ED0	U8-3
	---- ---- ---- --1-	L/ED1	U8-4
	---- ---- ---- -1--	L/ED2	U8-7
	---- ---- ---- 1---	L/ED3	U8-8
	---- ---- ---1 ----	L/ED4	U8-13
	---- ---- --1- ----	L/ED5	U8-14
	---- ---- -1-- ----	L/ED6	U8-17
	---- ---- 1--- ----	L/ED7	U8-18
	---- ---1 ---- ----	L/ED8	U10-3
	---- --1- ---- ----	L/ED9	U10-4
	---- -1-- ---- ----	L/ED10	U10-7
	---- 1--- ---- ----	L/ED11	U10-8
	---1 ---- ---- ----	L/ED12	U10-13
	--1- ---- ---- ----	L/ED13	U10-14
	-1-- ---- ---- ----	L/ED14	U10-17
	1--- ---- ---- ----	L/ED15	U10-18

4-302. EMULATOR STATUS BUS.

4-303. Results. Errors are decoded as follows:

Hex	Binary	Signal in error	Source
xx =	0000 0000	None	
	---- ---1	L/ES0	U12-3
	---- --1-	L/ES1	U12-4
	---- -1--	L/ES2	U12-7
	---- 1---	L/ES3	U12-8
	---1 ----	L/ES4	U12-13
	--1- ----	L/ES5	U12-14
	-1-- ----	L/ES6	U12-17
	1--- ----	L/ES7	U12-18

4-304. ANALYSIS TRACE POINT.

4-305. Failure indicates Trace Point was not set on the analysis board. Complete loss of the L/ANAL clock from the emulator is detected by this test.

4-306. ANALYSIS MEASUREMENT COMPLETE.

4-307. Failure indicates the L/ANAL clock signal from the emulator is too slow and fails to send the required 256 cycles within 15 milliseconds.

4-308. SYSTEM INTERRUPT AT TRACE POINT.

4-309. Failure occurs when the emulator does not respond to a break on Trace Point by sending an interrupt to the system processor.

4-310. SYSTEM INTERRUPT AT MEASUREMENT COMPLETE.

4-311. Failure occurs when the emulator does not respond to a break on measurement complete by sending an interrupt to the system processor.

4-312. EMULATOR PV.

4-313. Only the lower 16 bits of the emulator address are tested. The upper 8 bits can be tested by running a 16 bit emulator performance verification with the analyzer.

4-314. ANALYSIS STIMULUS TEST DISPLAY.

4-315. This test is contained within the emulator performance verification Tests. Tables 4-1 and 4-2 indicate which emulators have PV which contain an Analysis Stimulus Test for the wide logic analyzer.

4-316. Purpose. These tests do almost the same checking of circuitry as the Emulator Stimulus Tests. For example, Figure 4-20 displays the Analysis Stimulus Subtest which is contained in the 8086 emulator PV. These subtests indicate the 64302A board's capability to receive signals from an attached emulator.

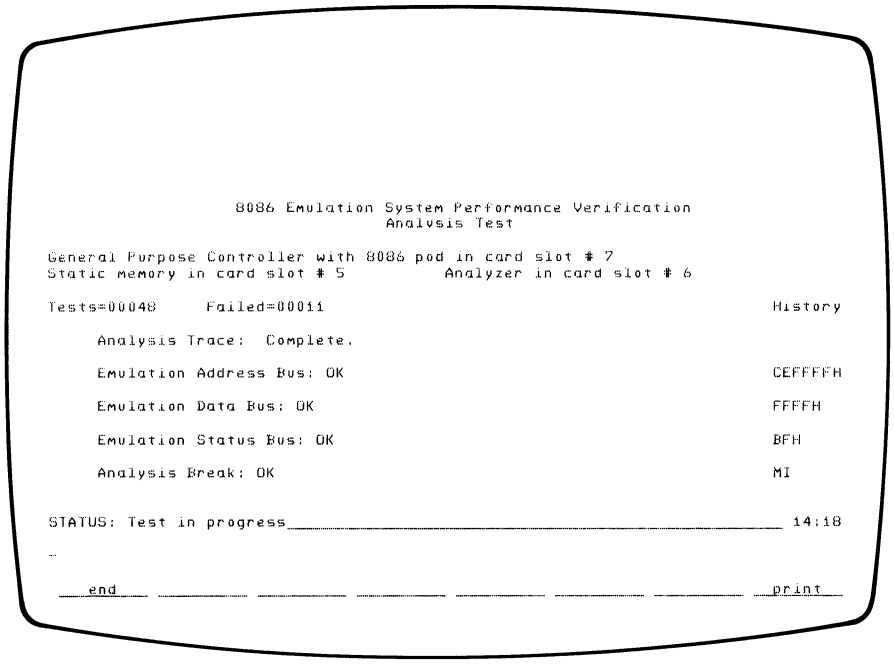


Figure 4-20. Analysis Stimulus Display (8086 Emulator)

4-317. Running the Analysis Stimulus Tests. Enter the emulation PV of an emulator which contains this test for the 64302A. (Refer to tables 4-1 and 4-2 for this information). Use the <Next Test> softkey to highlight the Analysis Stimulus Test. Press the <Start> softkey to begin. The tests will continue until the <Start> softkey is pressed again.

4-318. Using the Analysis Stimulus Results. The total number of errors detected during the tests is shown next to the Failed= entry. If the test passes, OK is indicated. Errors are indicated by a code shown to the immediate right of the test names. These codes represent

a single failure during the last iteration. Each error code in the History column represents the sum of all errors detected during the test. History error codes that differ from the present error code indicate multiple, or intermittent errors. When the error codes are the same, the errors are systematic.

4-319. ANALYSIS TRACE.
(Not present in all emulator Analysis Stimulus tests.)

4-320. A complete result here indicates that the analyzer has filled the number of memory locations for which it was configured.

4-321. An incomplete result can mean many things. The analysis clock signal L/ANAL from the emulator, may not be reaching the analyzer, or the timing circuitry may not be responding to L/ANAL correctly. Other components which could contribute to an incomplete Analysis Trace Test are checked in earlier analyzer PV.

4-322. The following three tests check the analyzers capabilty to store and unload states which are produced by the emulator. The emulator is set up to run a program which places known data onto the emulation bus. Simultaneously, the analyzer is set up for a 'don't care trigger' specification and then released to collect data. After a certain amount of time, depending upon the emulation program, the data contained in the analyzer RAMs is unloaded and checked against a table to verify that the data collected was the data sourced. Any discrepency is indicated as a failure in the appropriate bit position of the error display.

4-323. Hence, massive errors indicate that data is not being stored into the RAMs, or is being stored at the wrong address. This could be caused by a missing clock, emulation bus buffers which are not being properly enabled, or faults in the State Recognition circuitry. Be aware that the word/byte select circuitry and U96 of the State Recognition circuitry are checked in this test but nowhere else.

4-324. If not all of the bits are failing this could be an indication that the appropriate emulation bus latch are not operating correctly. Be aware that if there is a fault on the analyzer, each type of emulator (which has an Analysis Stimulus test for the 64302A) will probably indicate a different error code. This is because the data produced by the emulator and the accompaning comparison table is different for each emulator.

4-325. EMULATION ADDRESS BUS.

4-326. Results. Errors are decoded as follows:

Hex	Binary	Signal in error	Source
xxxxx=	0000 0000 0000 0000 0000 0000	None	
	---- ---- ---- ---- ---- ---1	L/EA0	U14-3
	---- ---- ---- ---- ---- --1-	L/EA1	U14-4
	---- ---- ---- ---- ---- -1--	L/EA2	U14-7
	---- ---- ---- ---- ---- 1---	L/EA3	U14-8
	---- ---- ---- ---- ---1 ----	L/EA4	U14-13
	---- ---- ---- ---- --1- ----	L/EA5	U14-14
	---- ---- ---- ---- -1-- ----	L/EA6	U14-17
	---- ---- ---- ---- 1--- ----	L/EA7	U14-18
	---- ---- ---- ---1 ---- ----	L/EA8	U16-3
	---- ---- ---- --1- ---- ----	L/EA9	U16-4
	---- ---- ---- -1-- ---- ----	L/EA10	U16-7
	---- ---- ---- 1--- ---- ----	L/EA11	U16-8
	---- ---- ---1 ---- ---- ----	L/EA12	U16-13
	---- ---- --1- ---- ---- ----	L/EA13	U16-14
	---- ---- -1-- ---- ---- ----	L/EA14	U16-17
	---- ---- 1--- ---- ---- ----	L/EA15	U16-18
	---- ---1 ---- ---- ---- ----	L/EA16	U18-3
	---- --1- ---- ---- ---- ----	L/EA17	U18-4
	---- -1-- ---- ---- ---- ----	L/EA18	U18-7
	---- 1--- ---- ---- ---- ----	L/EA19	U18-8
	---1 ---- ---- ---- ---- ----	L/EA20	U18-13
	--1- ---- ---- ---- ---- ----	L/EA21	U18-14
	-1-- ---- ---- ---- ---- ----	L/EA22	U18-17
	1--- ---- ---- ---- ---- ----	L/EA23	U18-18

4-327. EMULATION DATA BUS.

4-328. Results. Errors are decoded as follows:

Hex	Binary	Signal in error	Source
xxxx=	0000 0000 0000 0000	None	
	---- ---- ---- ---1	L/ED0	U8-3
	---- ---- ---- --1-	L/ED1	U8-4
	---- ---- ---- -1--	L/ED2	U8-7
	---- ---- ---- 1---	L/ED3	U8-8
	---- ---- ---1 ----	L/ED4	U8-13
	---- ---- --1- ----	L/ED5	U8-14
	---- ---- -1-- ----	L/ED6	U8-17
	---- ---- 1--- ----	L/ED7	U8-18
	---- ---1 ---- ----	L/ED8	U10-3
	---- --1- ---- ----	L/ED9	U10-4
	---- -1-- ---- ----	L/ED10	U10-7
	---- 1--- ---- ----	L/ED11	U10-8
	---1 ---- ---- ----	L/ED12	U10-13
	--1- ---- ---- ----	L/ED13	U10-14
	-1-- ---- ---- ----	L/ED14	U10-17
	1--- ---- ---- ----	L/ED15	U10-18

4-329. EMULATION STATUS BUS.

4-330. Results. Errors are decoded as follows:

Hex	Binary	Signal in error	Source
xx =	0000 0000	None	
	---- ---1	L/ES0	U12-3
	---- --1-	L/ES1	U12-4
	---- -1--	L/ES2	U12-7
	---- 1---	L/ES3	U12-8
	---1 ----	L/ES4	U12-13
	--1- ----	L/ES5	U12-14
	-1-- ----	L/ES6	U12-17
	1--- ----	L/ES7	U12-18

4-331. ANALYSIS BREAK.

4-332. Failure occurs when the emulator does not respond to a break on measurement complete by sending an interrupt to the system processor.

SECTION V

ADJUSTMENTS

5-1. INTRODUCTION.

5-2. This section describes adjustments and checks required to return the instrument to peak operating capability after repairs have been made.

5-3. SAFETY REQUIREMENTS.

5-4. Although this instrument has been designed in accordance with international safety standards, general safety precautions must be observed during all phases of operation, service, and repair of the instrument. Failure to comply with precautions listed in the Safety Summary at the front of this manual or with specific warnings given throughout the manual could result in damage to the equipment or serious injury or death. Service adjustments should be performed only by qualified service personnel.

5-5. EQUIPMENT REQUIRED.

a. Logic Development System mainframe with most recent PV software.

b. Extender board.

c. Hewlett-Packard Model 1743A oscilloscope or equivalent.

5-6. ADJUSTMENTS.

5-7. This procedure assumes that the 64100A mainframe has been calibrated, and all voltages and signals external to the 64302A Wide Logic analyzer are within specification.

5-8. The calibration for the wide logic analyzer is part of the performance verification stored on the system disc. The stimulus for the wide logic analyzer comes from CPU.

5-9. PROCEDURE.

a. Turn off power to mainframe.

b. Remove card cage cover and place the analyzer on an extender board with the extender cables for the emulator connected.

c. Apply power to the mainframe. Enter option_test and press [RETURN].

d. Type the number of the card slot the wide logic analyzer is located in and press [RETURN].

e. The wide logic analyzer PV will come up. Press the <Calib> softkey to enter the calibrate mode.

f. Set oscilloscope for:
   Alternate sweep, 10 ns per division
   Positive (+) trigger on channel A
   Vertical sensitivity at 1 volt per division for both channels (including probe division)
   Waveform reference voltage at 1.3 volts

g. Connect oscilloscope channel A to U5 pin 2 and channel B to U55 pin 4.

h. Locate R1 and adjust for 75 ns, channel A rising to channel B falling.

i. Set oscilloscope sweep for 20 ns per division.

j. Locate R2 and adjust for 140 ns, channel A rising to channel B rising.

k. Disconnect oscilloscope channel B from U55 pin 4 and reconnect to U5 pin 11.

l. Locate R3 and adjust for 150 ns, channel A rising to channel B rising.

m. Disconnect oscilloscope.

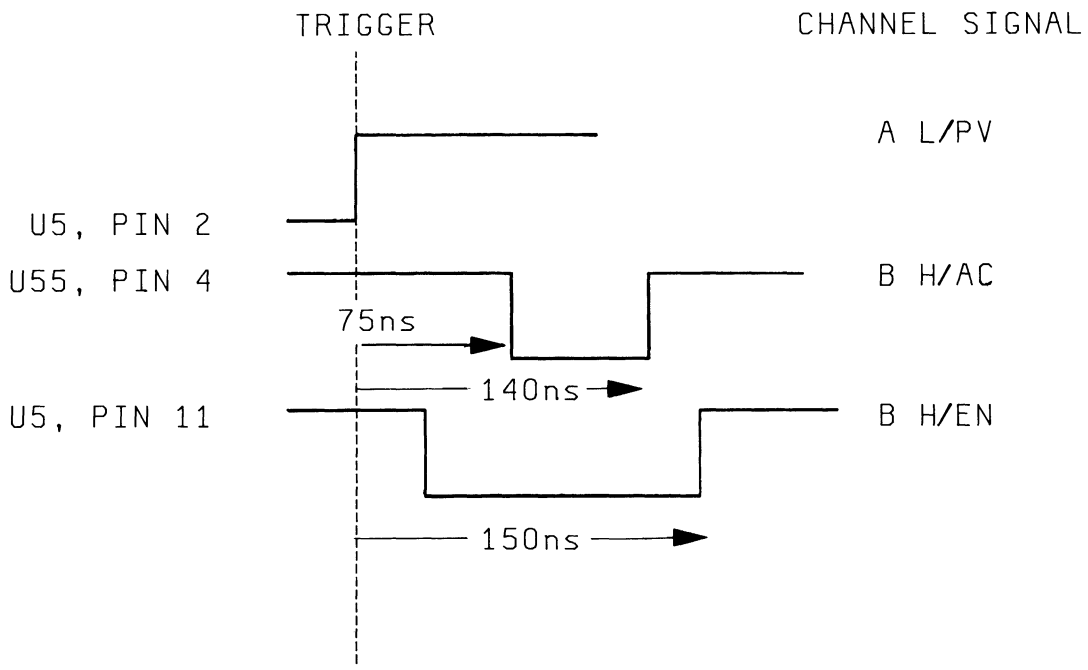


Figure 5-1. Wide Logic Analyzer Timing

n. Press <Calib.> softkey to leave calibration mode. Perform steps steps o and p only when BNC outputs require testing.

o. Press <Next Test> softkey until the Halt Mode test is reached, then press the <Select> softkey to enter the Halt Mode. Press the <Select> softkey to enter the Control Logic test, then begin the test by pressing the <Start> softkey.

p. Connect the oscilloscope to the Port 1 BNC connector on the back panel of the mainframe. The output should be the TTL level signal shown in figure 5-3. Now connect the oscilloscope to the Port 2 BNC connector. The output should be the TTL level signal shown. Note that the signals can be inverted from those shown.

q. Press the <End> softkey until system level returns.

r. Disconnect oscilloscope and turn off power to mainframe. Replace analyzer and card cage cover.

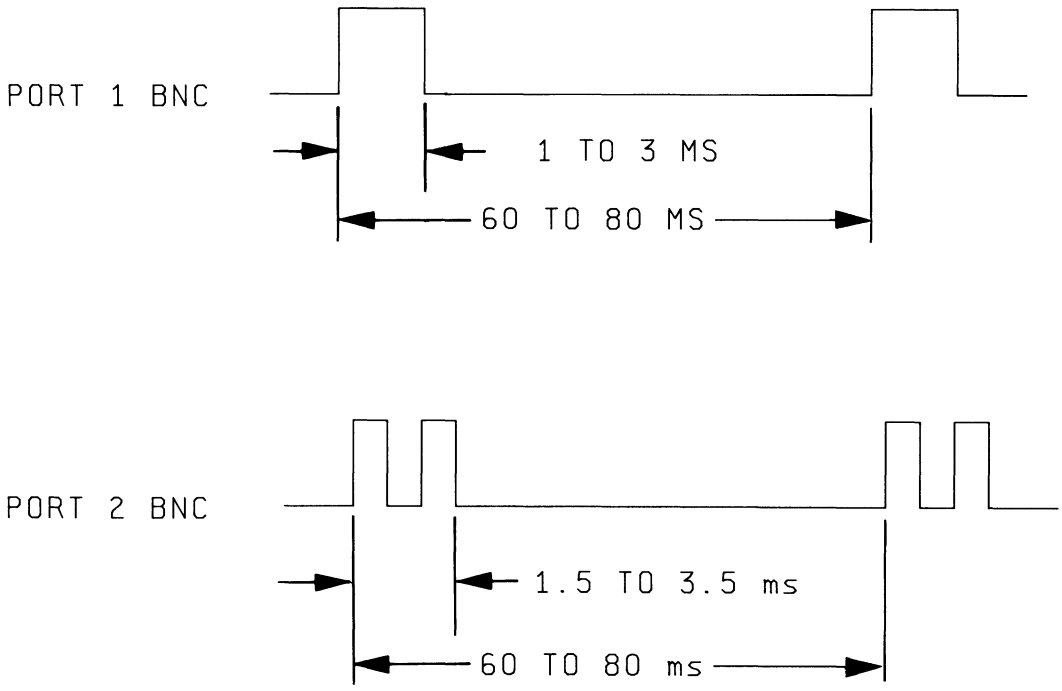


Figure 5-2. External Port Signals

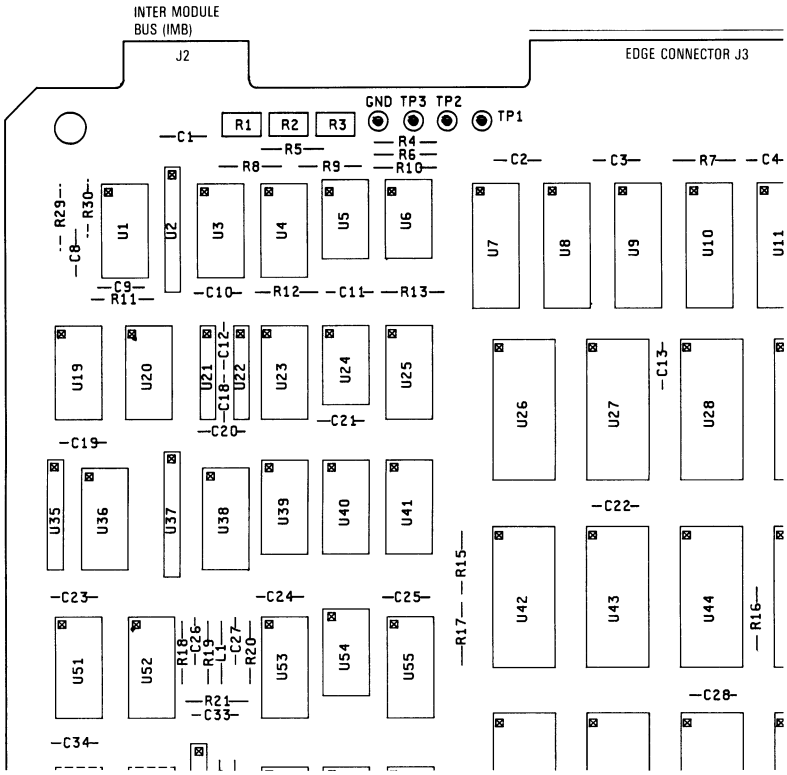


Figure 5-3. Adjustment Locations

SECTION VI

REPLACEABLE PARTS

6-1. INTRODUCTION.

6-2. This section contains information for ordering parts. Table 6-1 lists abbreviations used in the parts list and throughout the manual. Table 6-2 lists all replaceable parts in reference designator order. Table 6-3 contains the names and addresses that correspond to the manufacturers' five-digit code numbers.

6-3. ABBREVIATIONS.

6-4. Table 6-1 lists abbreviations used in the parts list, the schematics and throughout the manual. In some cases, two forms of the abbreviation are used: one all in capital letters, and one partial or no capitals. This occurs because the abbreviations in the parts list are always capitals. However, in the schematics and other parts of the manual, other abbreviation forms are used with both lowercase and uppercase letters.

6-5. REPLACEABLE PARTS LIST.

6-6. Table 6-2, the replaceable parts list, is organized as follows:

a. Chassis-mounted parts in alphanumerical order by reference designation.

b. Electrical assemblies and their components in alphanumerical order by reference designation.

c. Miscellaneous parts.

6-7. The total quantity for each part is given only once, at the first appearance of the part number in the list. The information given for each part consists of the following:

a. The Hewlett-Packard part number and the check digit.

b. The total quantity (Qty) in the instrument.

c. The description of the part.

d. A five-digit code that indicates the manufacturer.

e. The manufacturer's part number.

6-8. ORDERING INFORMATION.

6-9. To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number and check digit, indicate the quantity required, and address the order to the nearest Hewlett-Packard office.

6-10. To order a part that is not listed in the replaceable parts table, include the instrument model number, instrument repair number, the description and function of the part, and the number of parts required. Address the order to the nearest Hewlett-Packard office.

6-11. DIRECT MAIL ORDER SYSTEM.

6-12. Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using the system are as follows:

a. Direct ordering and shipment from the HP Parts Center in Mountain View, California.

b. No maximum or minimum on any mail order (there is a minimum order amount, for parts ordered through a local HP office when the orders require billing and invoicing).

c. Prepaid transportation (there is a small handling charge for each order).

d. No invoices - to provide these advantages, a check or money order must accompany each order.

6-13. Mail-order forms and specific ordering information are available through your local HP office. Addresses and phone numbers are located at the back of this manual.

Table 6-1. Reference Designators and Abbreviations

REFERENCE DESIGNATORS

A	= assembly	**F**	= fuse	**MP**	= mechanical part	**U**	= integrated circuit
B	= motor	**FL**	= filter	**P**	= plug	**V**	= vacuum, tube, neon bulb, photocell, etc
BT	= battery	**IC**	= integrated circuit	**Q**	= transistor		
C	= capacitor	**J**	= jack	**R**	= resistor	**VR**	= voltage regulator
CP	= coupler	**K**	= relay	**RT**	= thermistor	**W**	= cable
CR	= diode	**L**	= inductor	**S**	= switch	**X**	= socket
DL	= delay line	**LS**	= loud speaker	**T**	= transformer	**Y**	= crystal
DS	= device signaling (lamp)	**M**	= meter	**TB**	= terminal board	**Z**	= tuned cavity network
E	= misc electronic part	**MK**	= microphone	**TP**	= test point		

ABBREVIATIONS

A	= amperes	**H**	= henries	**N/O**	= normally open	**RMO**	= rack mount only
AFC	= automatic frequency control	**HDW**	= hardware	**NOM**	= nominal	**RMS**	= root-mean square
AMPL	= amplifier	**HEX**	= hexagonal	**NPO**	= negative positive zero (zero temperature coefficient)	**RWV**	= reverse working voltage
		HG	= mercury				
BFO	= beat frequency oscillator	**HR**	= hour(s)				
BE CU	= beryllium copper	**HZ**	= hertz	**NPN**	= negative-positive-negative	**S-B**	= slow-blow
BH	= binder head					**SCR**	= screw
BP	= bandpass			**NRFR**	= not recommended for field replacement	**SE**	= selenium
BRS	= brass	**IF**	= intermediate freq			**SECT**	= section(s)
BWO	= backward wave oscillator	**IMPG**	= impregnated	**NSR**	= not separately replaceable	**SEMICON**	= semiconductor
		INCD	= incandescent			**SI**	= silicon
CCW	= counter-clockwise	**INCL**	= include(s)			**SIL**	= silver
CER	= ceramic	**INS**	= insulation(ed)	**OBD**	= order by description	**SL**	= slide
CMO	= cabinet mount only	**INT**	= internal	**OH**	= oval head	**SPG**	= spring
COEF	= coeficient			**OX**	= oxide	**SPL**	= special
COM	= common	**K**	= kilo=1000			**SST**	= stainless steel
COMP	= composition					**SR**	= split ring
COMPL	= complete	**LH**	= left hand	**P**	= peak	**STL**	= steel
CONN	= connector	**LIN**	= linear taper	**PC**	= printed circuit		
CP	= cadmium plate	**LK WASH**	= lock washer	**PF**	= picofarads= 10^{-12} farads	**TA**	= tantalum
CRT	= cathode-ray tube	**LOG**	= logarithmic taper			**TD**	= time delay
CW	= clockwise	**LPF**	= low pass filter	**PH BRZ**	= phosphor bronze	**TGL**	= toggle
				PHL	= phillips	**THD**	= thread
DEPC	= deposited carbon	**M**	= milli=10^{-3}	**PIV**	= peak inverse voltage	**TI**	= titanium
DR	= drive	**MEG**	= meg=10^{6}	**PNP**	= positive-negative-positive	**TOL**	= tolerance
		MET FLM	= metal film			**TRIM**	= trimmer
ELECT	= electrolytic	**MET OX**	= metallic oxide	**P/O**	= part of	**TWT**	= traveling wave tube
ENCAP	= encapsulated	**MFR**	= manufacturer	**POLY**	= polystyrene		
EXT	= external	**MHZ**	= mega hertz	**PORC**	= porcelain	**U**	= micro=10^{-6}
		MINAT	= miniature	**POS**	= position(s)		
F	= farads	**MOM**	= momentary	**POT**	= potentiometer	**VAR**	= variable
FH	= flat head	**MOS**	= metal oxide substrate	**PP**	= peak-to-peak	**VDCW**	= dc working volts
FIL H	= fillister head	**MTG**	= mounting	**PT**	= point		
FXD	= fixed	**MY**	= "mylar"	**PWV**	= peak working voltage	**W/**	= with
						W	= watts
G	= giga (10^{9})	**N**	= nano (10^{-9})	**RECT**	= rectifier	**WIV**	= working inverse voltage
GE	= germanium	**N/C**	= normally closed	**RF**	= radio frequency		
GL	= glass	**NE**	= neon	**RH**	= round head or right hand	**WW**	= wirewound
GRD	= ground(ed)	**NI PL**	= nickel plate			**W/O**	= without

Table 6-2. Replaceable Parts List, Sheet 1 of 4

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
					28480	64302A
	64302-66501	9	1	BOARD ASSEMBLY-INTERNAL ANALYZER	28480	64302-66501
C1	0160-2055	9	56	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C2	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C3	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C4	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C5	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C6	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C7	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C8	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C9	0140-0151	0	1	CAPACITOR-FXD 820PF +-2% 300VDC MICA	72136	DM15F821G0300WV1CR
C10	0140-0208	8	2	CAPACITOR-FXD 680PF +-5% 300VDC MICA	72136	DM15F681J0300WV1CR
C11	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C12	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C13	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C14	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C15	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C16	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C17	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C18	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C19	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C20	0140-0208	8		CAPACITOR-FXD 680PF +-5% 300VDC MICA	72136	DM15F681J0300WV1CR
C21	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C22	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C23	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C24	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C25	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C26	0140-0197	4	1	CAPACITOR-FXD 180PF +-5% 300VDC MICA	72136	DM15F181J0300WV1CR
C27	0160-2197	0	1	CAPACITOR-FXD 10PF +-5% 300VDC MICA	28480	0160-2197
C28	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C29	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C30	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C31	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C32	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C33	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C34	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C35	0160-4789	0	2	CAPACITOR-FXD 15PF +-5% 100VDC CER 0+-30	28480	0160-4789
C36	0160-4789	0		CAPACITOR-FXD 15PF +-5% 100VDC CER 0+-30	28480	0160-4789
C37	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C38	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C39	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C40	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C41	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C42	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C43	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C44	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C45	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C46	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C47	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C48	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C49	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C50	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C51	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C52	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C53	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C54	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C55	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C56	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C57	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C58	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C59	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C60	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C61	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C62	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C63	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C64	0180-0229	7	2	CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C65	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
L1	9100-2257	6	1	INDUCTOR RF-CH-MLD 820NH 10% .105DX.26LG	28480	9100-2257
MP1	64302-85001	4	1	EXTRACTOR-PC BOARD	28480	64302-85001
MP2	64302-85002	5	1	EXTRACTOR-PC BOARD	28480	64302-85002
MP3	1480-0116	8	8	PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116
MP4	1480-0116	8		PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116

See introduction to this section for ordering information

Table 6-2. Replaceable Parts List, Sheet 2 of 4

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
R1	2100-3351	6	3	RESISTOR-TRMR 500 10% C SIDE-ADJ 1-TRN	28480	2100-3351
R2	2100-3351	6		RESISTOR-TRMR 500 10% C SIDE-ADJ 1-TRN	28480	2100-3351
R3	2100-3351	6		RESISTOR-TRMR 500 10% C SIDE-ADJ 1-TRN	28480	2100-3351
R4	0757-0442	9	2	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R5	0698-3443	0	1	RESISTOR 287 1% .125W F TC=0+-100	24546	C4-1/8-T0-287R-F
R6	0757-0438	3	3	RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
R7	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R8	0698-3441	8	2	RESISTOR 215 1% .125W F TC=0+-100	24546	C4-1/8-T0-215R-F
R9	0757-0411	2	1	RESISTOR 332 1% .125W F TC=0+-100	24546	C4-1/8-T0-332R-F
R10	0698-0082	7	1	RESISTOR 464 1% .125W F TC=0+-100	24546	C4-1/8-T0-4640-F
R11	0757-0346	2	1	RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R12	0757-0280	3	10	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R13	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R14	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R15	0698-3429	2	1	RESISTOR 19.6 1% .125W F TC=0+-100	03888	PME55-1/8-T0-19R6-F
R16	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R17	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R18	0757-0408	7	1	RESISTOR 243 1% .125W F TC=0+-100	24546	C4-1/8-T0-243R-F
R19	0757-0399	5	1	RESISTOR 82.5 1% .125W F TC=0+-100	24546	C4-1/8-T0-82R5-F
R20	0698-3441	8		RESISTOR 215 1% .125W F TC=0+-100	24546	C4-1/8-T0-215R-F
R21	0757-0407	6	1	RESISTOR 200 1% .125W F TC=0+-100	24546	C4-1/8-T0-201-F
R22	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R23	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
R24	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
R25	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R26	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R27	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R28	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
				NOT ASSIGNED		
				NOT ASSIGNED		
TP1	0360-0535	0	7	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
TP2	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
TP3	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
TP4	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
				NOT ASSIGNED		
TP6	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
TP7	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
TP8	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
U1	1820-1225	4	3	IC FF ECL D-M/S DUAL	04713	MC10231P
U2	1810-0275	1	2	NETWORK-RES 10-SIP1.0K OHM X 9	01121	210A102
U3	1820-2359	7	1	IC MISC ECL 14-INP	07263	F10014PC
U4	1820-1173	1	2	IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L
U5	1820-2687	4	4		28480	1820-2687
U6	1820-0682	5	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S03N
U7	1820-1917	1	10	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U8	1820-1997	7	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U9	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U10	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U11	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U12	1820-1677	0	4	IC FF TTL S D-TYPE OCTL	01295	SN74S374N
U13	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U14	1820-1677	0		IC FF TTL S D-TYPE OCTL	01295	SN74S374N
U15	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U16	1820-1677	0		IC FF TTL S D-TYPE OCTL	01295	SN74S374N
U17	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U18	1820-1677	0		IC FF TTL S D-TYPE OCTL	01295	SN74S374N
U19	1820-1052	5	2	IC XLTR ECL ECL-TO-TTL QUAD 2-INP	04713	MC10125L
U20	1820-1225	4		IC FF ECL D-M/S DUAL	04713	MC10231P
U21	1810-0219	3	2	NETWORK-RES 8-SIP220.0 OHM X 4	01121	208B221
U22	1810-0219	3		NETWORK-RES 8-SIP220.0 OHM X 4	01121	208B221
U23	1820-0809	8	1	IC RCVR ECL LINE RCVR QUAD 2-INP	04713	MC10115P
U24	1820-1144	6	2	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
U25	1820-1282	3	2	IC FF TTL LS J-K BAR POS-EDGE-TRIG	01295	SN74LS109AN
U26	1816-1334	7	2	IC-93422 RAM	07263	93422DC
U27	1816-1334	7		IC-93422 RAM	07263	93422DC
U28	1816-1308	5	23	IC-93L422 P.C.	07263	93L422PC
U29	1816-1308	5		IC-93L422 P.C.	07263	93L422PC
U30	1816-1092	4	2	IC TTL LS 256-BIT RAM STAT 35-NS 3-S	28480	1816-1092
U31	1816-1308	5		IC-93L422 P.C.	07263	93L422PC
U32	1816-1308	5		IC-93L422 P.C.	07263	93L422PC
U33	1816-1308	5		IC-93L422 P.C.	07263	93L422PC
U34	1816-1092	4		IC TTL LS 256-BIT RAM STAT 35-NS 3-S	28480	1816-1092
U35	1810-0273	9	2	NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471
U36	1820-1225	4		IC FF ECL D-M/S DUAL	04713	MC10231P
U37	1810-0273	9		NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471
U38	1820-1944	4	1	IC LCH ECL D-TYPE POS-EDGE-TRIG DUAL	04713	MC10130L
U39	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U40	1820-2684	1	3	IC-74F00	28480	1820-2684

See introduction to this section for ordering information

Table 6-2. Replaceable Parts List, Sheet 3 of 4

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U41	1820-2684	1		IC-74F00	28480	1820-2684
U42	1816-1308	5		IC-93L422 P.C.	07263	93L422PC
U43	1816-1308	5		IC-93L422 P.C.	07263	93L422PC
U44	1816-1308	5		IC-93L422 P.C.	07263	93L422PC
U45	1816-1308	5		IC-93L422 P.C.	07263	93L422PC
U46	1816-1308	5		IC-93L422 P.C.	07263	93L422PC
U47	1816-1308	5		IC-93L422 P.C.	07263	93L422PC
U48	1816-1308	5		IC-93L422 P.C.	07263	93L422PC
U49	1816-1308	5		IC-93L422 P.C.	07263	93L422PC
U50	1816-1308	5		IC-93L422 P.C.	07263	93L422PC
U51	1820-1173	1		IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L
U52	1820-1052	5		IC XLTR ECL ECL-TO-TTL QUAD 2-INP	04713	MC10125L
U53	1820-1782	8	1	IC MV TTL S MONOSTBL RETRIG/RESET DUAL	34335	AM26S02PC
U54	1820-2685	2	3	IC-74F02	28480	1820-2685
U55	1820-2695	4	1	IC-74F158	28480	1820-2695
				NOT ASSIGNED		
				NOT ASSIGNED		
U58	1810-0275	1		NETWORK-RES 10-SIP1.0K OHM X 9	01121	210A102
U59	1820-2693	2	3	IC-74F106	28480	1820-2693
U60	1820-1475	6	1	IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	07263	93S16DC
U61	1820-2684	1		IC-74F00	28480	1820-2684
U62	1816-1308	5		IC-93L422 P.C.	07263	93L422PC
U63	1816-1308	5		IC-93L422 P.C.	07263	93L422PC
U64	1816-1308	5		IC-93L422 P.C.	07263	93L422PC
U65	1816-1308	5		IC-93L422 P.C.	07263	93L422PC
U66	1816-1308	5		IC-93L422 P.C.	07263	93L422PC
U67	1816-1308	5		IC-93L422 P.C.	07263	93L422PC
U68	1816-1308	5		IC-93L422 P.C.	07263	93L422PC
U69	1816-1308	5		IC-93L422 P.C.	07263	93L422PC
U70	1816-1308	5		IC-93L422 P.C.	07263	93L422PC
U71	1820-2690	9	1	IC-74F32	28480	1820-2690
U72	1820-2693	2		IC-74F109	28480	1820-2693
U73	1820-1158	2	1	IC GATE TTL S AND-OR-INV DUAL 2-INP	01295	SN74S51N
U74	1820-0691	6	4	IC GATE TTL S AND-OR-INV	01295	SN74S64N
U75	1820-0691	6		IC GATE TTL S AND-OR-INV	01295	SN74S64N
U76	1820-1430	3	14	IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
U77	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U78	1820-2024	3	4	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
				NOT ASSIGNED		
U80	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U81	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
U82	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
U83	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
U84	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
U85	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
U86	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
U87	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
U88	1820-2693	2		IC-74F109	28480	1820-2693
U89	1820-1282	3		IC FF TTL LS J-K BAR POS-EDGE-TRIG	01295	SN74LS109AN
				NOT ASSIGNED		
U91	1820-2685	2		IC-74F02	28480	1820-2685
U92	1820-0683	6	1	IC INV TTL S HEX 1-INP	01295	SN74S04N
U93	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
U94	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
U95	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
U96	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U97	1820-2687	4		IC-74F10	28480	1820-2687
U98	1820-2685	2		IC-74F02	28480	1820-2685
U99	1820-2687	4		IC-7410	28480	1820-2687
U100	1820-2687	4		IC-7410	28480	1820-2687
U101	1820-0691	6		IC GATE TTL S AND-OR-INV	01295	SN74S64N
U102	1820-0691	6		IC GATE TTL S AND-OR-INV	01295	SN74S64N
U103	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
U104	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
				NOT ASSIGNED		
U106	1820-1216	3	2	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
U107	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
U108	1820-1730	6	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U109	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U110	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U111	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U112	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U113	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U115	1820-0269	4	1	IC GATE TTL NAND QUAD 2-INP	01295	SN7403N
U116	1820-1199	1	1	IC INV TTL LS HEX 1-INP	01295	SN74LS04N

See introduction to this section for ordering information

Table 6-2. Replaceable Parts List, Sheet 4 of 4

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U117	1820-1144	6		IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
U118	1820-0780	4	1	IC DRVR TTL LINE DRVR QUAD	27014	DS8831N
U119	1820-1202	7	1	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
				NOT ASSIGNED		
U121	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
XU4	1200-0607	0	4	SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU23	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU26	1200-0612	7	25	SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
XU27	1200-0612	7		SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
XU28	1200-0612	7		SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
XU29	1200-0612	7		SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
XU31	1200-0612	7		SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
XU32	1200-0612	7		SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
XU33	1200-0612	7		SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
XU42	1200-0612	7		SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
XU43	1200-0612	7		SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
XU44	1200-0612	7		SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
XU45	1200-0612	7		SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
XU46	1200-0612	7		SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
XU47	1200-0612	7		SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
XU48	1200-0612	7		SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
XU49	1200-0612	7		SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
XU50	1200-0612	7		SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
XU53	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU62	1200-0612	7		SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
XU63	1200-0612	7		SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
XU64	1200-0612	7		SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
XU65	1200-0612	7		SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
XU66	1200-0612	7		SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
XU67	1200-0612	7		SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
XU68	1200-0612	7		SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
XU69	1200-0612	7		SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
XU70	1200-0612	7		SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
XU118	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607

Table 6-3. List of Manufacturers' Codes

Mfr No.	Manufacturer Name	Address		Zip Code
00000	ANY SATISFACTORY SUPPLIER			
01121	ALLEN-BRADLEY CO	MILWAUKEE	WI	53204
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS	TX	75222
03888	KDI PYROFILM CORP	WHIPPANY	NJ	07981
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX	AZ	85062
07263	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW	CA	94042
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD	PA	16701
27014	NATIONAL SEMICONDUCTOR CORP	SANTA CLARA	CA	95051
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304
34335	ADVANCED MICRO DEVICES INC	SUNNYVALE	CA	94086
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS	MA	01247
72136	ELECTRO MOTIVE CORP SUB IEC	WILLIMANTIC	CT	06226

SECTION VII

MANUAL CHANGES

7-1. INTRODUCTION.

7-2. This section contains information for adapting this manual to instruments for which the content does not directly apply.

7-3. MANUAL CHANGES.

7-4. To adapt this manual to your instrument, refer to table 7-1 and make all of the changes listed opposite the serial prefix of your instrument.

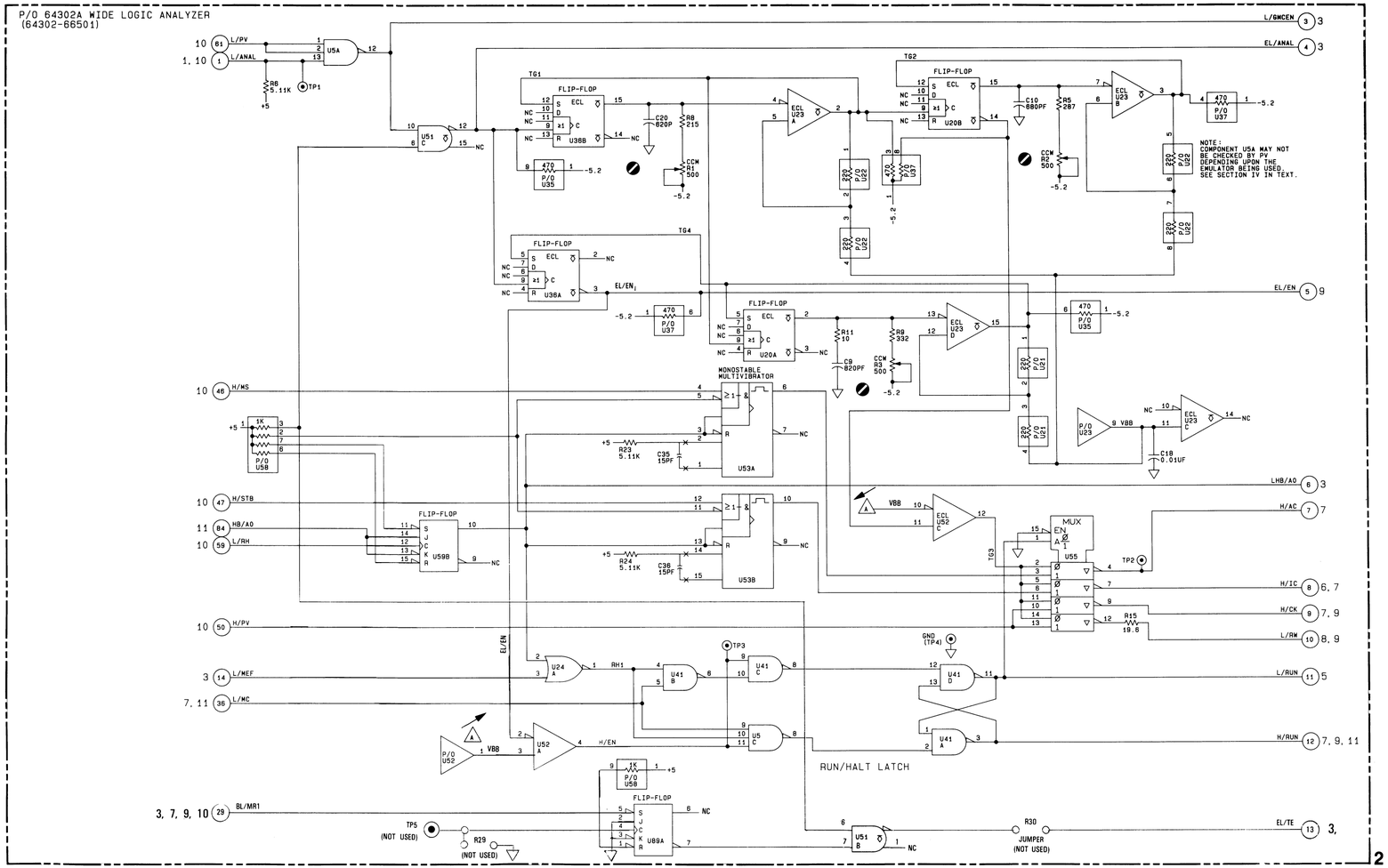
Table 7-1. Manual Changes

Serial Prefix	Manual Changes
2133A	Change 1

7-5. MANUAL CHANGE INSTRUCTIONS.

CHANGE 1.

Replace figure 8-3 with figure 7-1.
Replace figure 8-4 with figure 7-2.



ICs ON THIS SCHEMATIC

REF. DES.	HP PART NO.	MFG. PART NO.
U5	1820-2687	1820-2687
U20,36	1820-1225	MC10231P
U23	1820-0809	MC10115P
U24	1820-1144	SN74LS02N
U41	1820-2684	1820-2684
U51	1820-1173	MC10124L
U52	1820-1052	MC10125L
U53	1820-1782	AM26S02PC
U55	1820-2695	1820-2695
U59	1820-2693	1820-2693
U89	1820-1282	SN74LS109AN

PARTS ON THIS SCHEMATIC

C9,10,18,20,35,36
R1,2,3,5,6,8,9,11,23,24
TP1,TP2,TP4
U21,22,35,37,58 resistor packs

IC POWER SUPPLY PIN CONFIGURATION

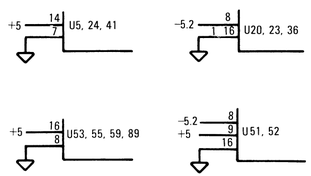
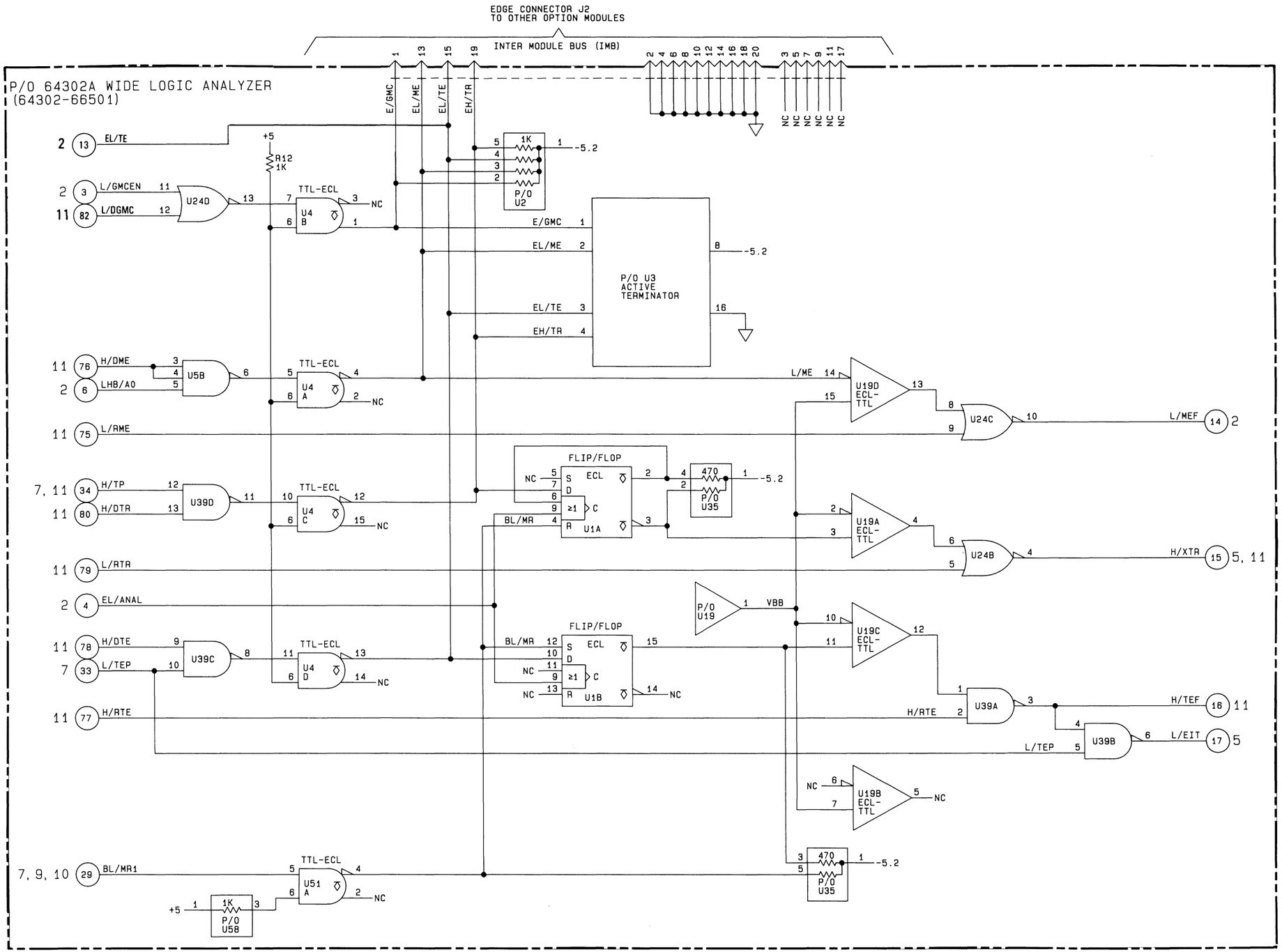


Figure 7-1.
Service Sheet 2, Timing
7-3/(7-4 blank)



ICs ON THIS SCHEMATIC

REF. DES.	HP PART NO.	MFG. PART NO.
U1	1820-1225	MC10231P
U3	1820-2359	F10014PC
U4,51	1820-1173	MC10124L
U5	1820-2687	1820-2687
U19	1820-1052	MC10125L
U24	1820-1144	SN74LS02N
U39	1820-1197	SN74LS00N

PARTS ON THIS SCHEMATIC

U2,35,58 resistor packs

IC POWER SUPPLY PIN CONFIGURATION

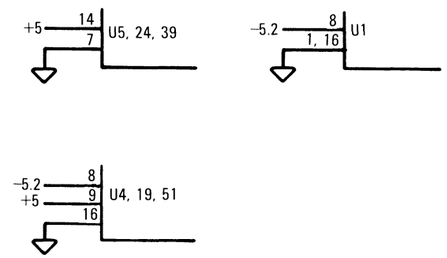


Figure 7-2.
Service Sheet 3, Inter Module Bus (IMB)
7-5/(7-6 blank)

SECTION VIII

SERVICE

8-1. INTRODUCTION.

8-2. This section contains backup information for repairing the Model 64302A Wide Logic Analyzer. For convenience, the schematics, component location figure, and other service information are provided on fold-out service sheets.

8-3. Because the wide logic analyzer is very software dependent, it is not practical to discuss the theory of operation at the bit level. Therefore, the following discussion is at the functional block level.

8-4. The purpose of the analyzer is to capture emulator state data so that the mainframe can display the states to the user. To do this the analyzer must operate in conjunction with the mainframe CPU, the emulator and, possibly, another analyzer. Thus, the board's operations are divided into two principal modes, one, the halt mode which coordinates the CPU and analyzer, and two, the run mode which performs emulator state capture, storage and decoding. The following functional blocks implement the operational modes.

Emulator Bus Latch.....Service Sheet 1.
Timing/Control and IMB.....Service Sheets 2, 3.
State Recognition Storage and Decoding...Service Sheets 4, 5.
Occurrence Counter.....Service Sheet 6.
State Storage Control.....Service Sheet 7.
State Storage .....Service Sheet 8.
Time/State Counter and Storage.....Service Sheet 9.
Read/Write Control.....Service Sheet 10.
CPU Bus Buffer and Control Latch.....Service Sheet 11.

8-5. GENERAL THEORY.

8-6. The halt mode is used to perform CPU initiated activities such as loading state recognition terms and the control word before the analysis is performed and to unload the stored states after the trace is complete.

8-7. In the halt mode, before a measurement is made, state recognition RAMs are loaded via the CPU bus, with state recognition terms. These are terms for address, data, status and address range. Also loaded is the number of trigger occurrences desired and how the recognition decoders are to be allocated. The timing and control functions are informed by state recognition when a state on the emulator bus is recognized for trigger, state counting, or storage.

8-8. The run mode begins when the real time analysis is started and ends when the trace is completed. During the run mode the analyzer captures emulator states from the emulator bus, qualifies the state

for storage in the analyzer RAMs and determines when the trace is complete. The run mode operations are controlled by the analyzer timing signals and cannot be interferred with by a CPU read or write. In this mode only control flags can be accessed by the CPU.

8-9. In the run mode, through state control, the state storage accumulates 256 states; each state consisting of 48 bits of address, data, and status from the emulator bus and 24 bits of count. The count is either a cumulative time value or a cumulative count of qualified states. State storage contains the trigger state plus all qualified states. When the trace is complete the timing/control function sets the measurement complete flag true and terminates the run mode. The CPU then unloads the state storage RAMs and displays the states to the user.

8-10. EMULATOR BUS LATCH, SERVICE SHEET 1.

8-11. The emulator bus latch temporarily stores the 48 bits comprising the address, data, and status. The rising edge of L/ANAL, the analysis clock signal from the emulator, clocks the six D type flip-flops. The latch is needed because the emulator state is present on the bus for less time than is required to set up the RAMs and store the state. The six buffers prevent signals on the latched emulator bus from appearing on the CPU address bus.

8-12. TIMING/CONTROL AND IMB, SERVICE SHEETS 2, 3.

8-13. Signal L/ANAL, the analysis clock from the emulator, is the basic frame of reference for signals generated by the timing generator. The timing generator produces several clocks and timing strobes for incrementing counters and writing into the state storage RAMs. It also sends sychronization signals to the run/halt control logic.

8-14. The run/halt control logic handles synchronization of run and halt commands from the CPU. It also places the analyzer in halt mode during a measurement disable or at the completion of a measurement. The run/halt control logic originates the Master Enable signal when the analyzer is configured to drive/receive IMB Master Enable.

8-15. The IMB circuitry receives eight control bits from the control word latch. These control bits determine which, if any, IMB signals are to be driven and/or received. The IMB interface converts signal levels (TTL/ECL) for all driven or received IMB signals. The IMB signals allow the analyzer to enable another option card with IMB to find a trigger or to receive an enable to find a trigger.

8-16. STATE RECOGNITION STORAGE AND DECODING, SERVICE SHEETS 4, 5.

8-17. Recognition terms are loaded into the nine state recognition RAMs by routing the CPU address onto the latched emulator bus and the CPU data to the data inputs of the RAMs. While in the 'halt-load' mode the emulator bus latch output is disabled (high impedance).

8-18. During the run mode, the 48 bit stored emulator state is applied to the state recognition RAMs address lines in conjunction with a read enable to output 29 recognition signals to the resource decoders. In all, four independent resources are decoded; AME1, AME2, Range, and Count Qualify. Each resource is represented by at least one 4 bit recognition term from a recognition RAM. The signals from state recognition RAMs are AND'd creating the four resources.

8-19. The four resources are combined to enable the occurence counter and the memory address counter when the desired state is identified. When a state is not a trigger or store qualified state, the resources prevent the counters from incrementing and the next state appearing on the emulator bus is written into the same state storage address.

8-20. OCCURRENCE COUNTER, SERVICE SHEET 6.

8-21. The occurrence counter gives the analyzer the capability to trigger on the Nth occurrence of a trigger specification. During the halt mode the counter is loaded with the complement of N. When the desired number of states occur, the counter overflows and the end of the count is signaled.

8-22. STATE STORAGE CONTROL, SERVICE SHEET 7.

8-23. An 8 bit memory address counter keeps the current memory address for the storage RAMs. Along with the memory address counter is a Wrap flip-flop to flag a memory full condition. Count and state data is always stored in the current memory position, but the data is overwritten by the next analysis cycle when the state was not store qualified. To effectively store a state the memory address counter is incremented just after the store operation. The next analysis cycle does not overwrite that information.

8-24. To unload the storage RAMs, the CPU sets the address in the memory address counter and the RAM data lines are connected to the CPU data bus. Before the memory is unloaded, the the memory address counter is read so that the current address is not destroyed by the unloading cycle.

8-25. The 8 bit memory index counter determines how many states are allowed to be stored following a trigger. During the halt mode the counter is loaded with the complement of the desired value. During run mode, each store qualified state increments the counter until the carry output indicates the end of the trace storage.

8-26. STATE STORAGE, SERVICE SHEET 8.

8-27. Parameters of a trace include how the captured states relate with respect to trigger. With 'Trace After', 255 states after the trigger are stored with the trigger. With 'Trace Before', 255 states (or as many as were encountered, if less than 255) are stored along with the trigger. In 'Trace About', the trigger is centered within the

256 deep memory. The poststore value, which is loaded into the memory index counter, determines how many states are captured after trigger is found, before the measurement is terminated. The memory index counter decrements for every state stored after trigger. When the counter has reached zero, it sets the measurement complete flag and terminates the trace.

8-28. TIME/STATE COUNTER AND STORAGE, SERVICE SHEET 9.

8-29. To keep track of absolute time or number of states, a 24 bit counter is employed. A flag is set when this 24 bit counter overflows to warn the user of this condition. The 24 bit time/state counter is incremented, in count time mode, by the time reference clock. In count state mode it is incremented when a count qualified state is seen on the emulator bus. The value in the counter is stored, however, only when a store qualified or trigger is encountered.

8-30. The 24 bits of count are stored in parallel with the emulator bus state. The state storage, plus count storage, is organized as a total of 72 bits, by 256 word memory to accomodate the emulator bus state and count.

8-31. The time reference is produced by the divide-by-16 circuit. This circuit divides the 25 MHz signal by 16 providing a 640 ns square wave only during analysis. When the analyzer is in the halt mode, or counting states, counting is suspended.

8-32. READ/WRITE CONTROL, SERVICE SHEET 10.

8-33. Three CPU address lines are connected to the read and write decoders to control access operations. Outputs from these decoders drive the run/halt logic, master reset of flip-flops and counters, and simulate the L/ANAL signal during PV. Other output signals control CPU read or write from the control word latch, loading the occurrence counter and loading the state recognition RAMs. Word/byte select logic determines when a word or byte is on the emulator bus and controls the assertion of the dummy recognition RAM when only a lower byte is on the bus.

8-34. CPU BUS BUFFER AND CONTROL LATCH, SERVICE SHEET 11.

8-35. Several functions of the analyzer are specified by the 16 bit control word latch. The eight most significant bits are used to define IMB operations. Three of the eight least significant bits specify BNC drive polarity and another three bits specify drive signals for emulation break and CPU interrupt. The remaining two bits specify counting of time or states. At power-up the latch is initialized to a 'neutral' condition.

8-36. The buffers on the CPU data bus prevent signals from appearing on the analyzer's internal L/DOUT data bus.

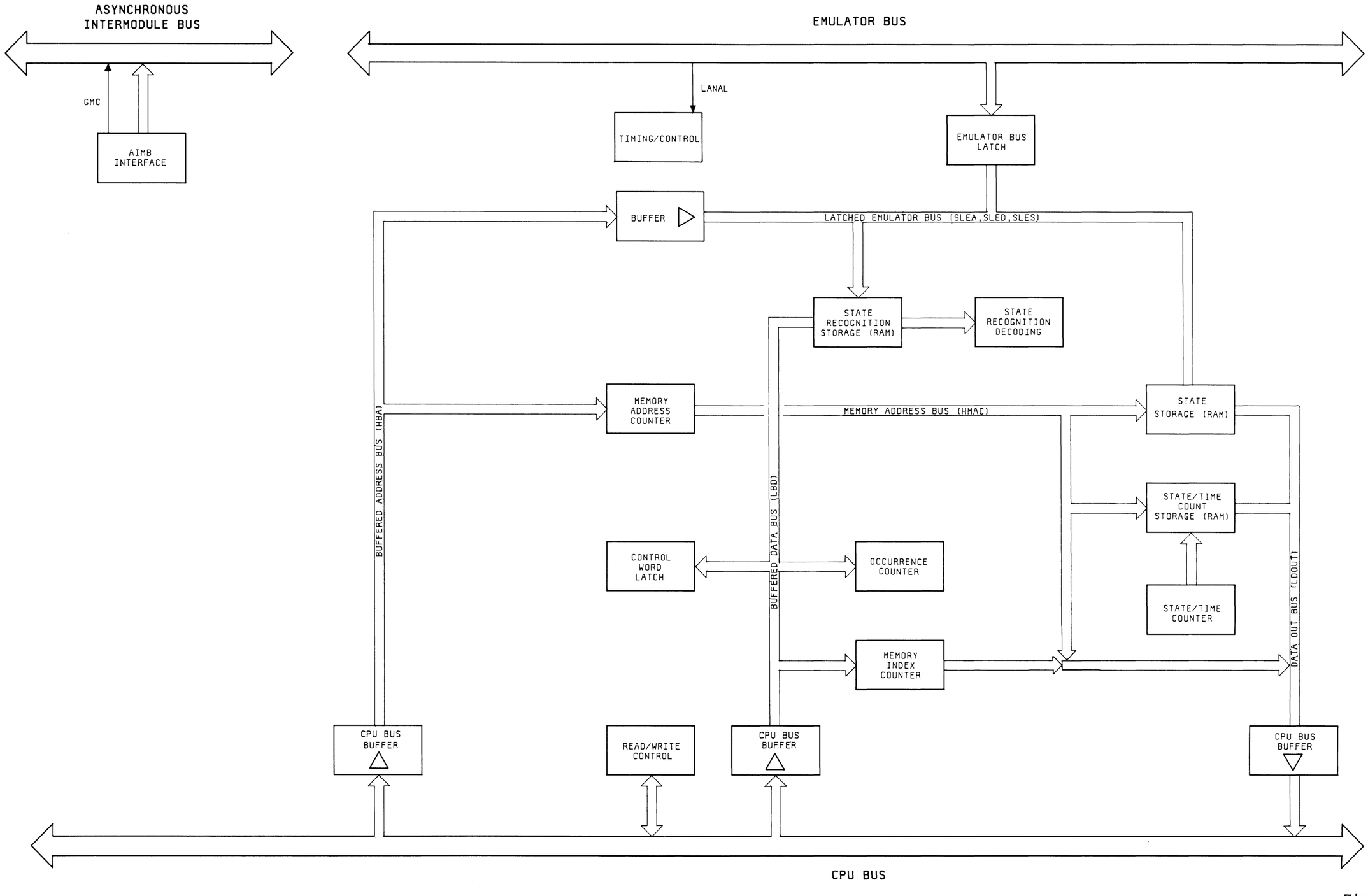


Figure 8-1.
Wide Logic Analyzer Block Diagram

8-37. MNEMONICS.

8-38. Some signals on the schematics have mnemonics that indicate their function. Table 8-1 lists the mnemonics in alphabetical order. Schematic references marked with an * indicate signal source.

Table 8-1. Mnemonics, sheet 1 of 12

Mnemonic	Description
25MHZ	25 MHz Clock. A crystal controlled clock originating in the the display controller circuitry of the mainframe; it drives B/25MHZ on the analyzer. Schematic 9.
AM0-16	Emulation Address Minterm Bus 0-16. Data output bus from State Recognition Storage RAMs that indicates whether trace specifications for emulation address have been detected. Uses positive logic: high = 1, low = 0. Schematics 4*, 5.
AME1	Adjacent Minterm Expression 1. Indicates whether the emulator bus state should, or should not, be part of the trace. Schematic 5.
AME2	Adjacent Minterm Expression 2. Indicates whether the emulator bus state is one that must occur N times to satisfy the trace specification. Schematic 5.
B/25MHZ	Buffered 25 MHz Clock. Input to Count Time circuit, used to produce L/TCK. Schematic 9.
BL/MR1	Buffered Low Measurement Reset One. Resets the Memory Address Counters, Time/State Counters and Word/Byte Select latches. Schematics 3, 7*, 9, 10.
BL/MR2	Buffered Low Measurement Reset Two. Sets the Time/State Overflow latch. Schematic 7.
BNC1	BNC1. Indicates Trace Point has occurred. Analyzer driven signal that appears on the rear panel connector labeled BNC1. Schematic 11.
BNC2	BNC2. Indicates Measurement Complete has occurred. Analyzer driven signal that appears on the rear panel connector labeled BNC2. Schematic 11.

Table 8-1. Mnemonics, sheet 2 of 12

Mnemonic	Description
CNT0-23	Time/State Counter Bits 0-23. Binary weighted count bits. Schematic 9.
COV	Counter Overflow. Indicates to the CPU that all of the the 640 ns counters have reached their terminal counts. Schematic 7.
DM0-7	Emulation Data Minterm Bus 0-7. Data output bus from State Recognition RAMs that indicates whether trace specifications for emulation data have been detected. Uses positive logic: high = 1, low = 0. Schematics 4*, 5.
E/GMC	ECL Gated Master Clock. Inter Module Bus (IMB) clocking signal driven by the analyzer that can be used by other modules as an external clock. Schematic 3.
EH/TR	ECL High Trigger. Inter Module Bus (IMB) signal that is both driven and received by the analyzer. When driven, comfirms to another module that the analyzer has found its trigger. When received, it indicates to the analyzer that the other module has found its trigger. Schematic 3.
EL/ANAL	ECL Low Analysis. Signals board to begin the analysis cycle; derived from L/ANAL. Schematics 2*, 3.
EL/EN	ECL Low Enable. Enables the Count-Time Synchronizer and drives H/EN. Schematics 2*, 9.
EL/ME	ECL Low Master Enable. Inter Module Bus (IMB) signal that can be received or driven by the analyzer. When received, the analyzer is enabled to run. When driven, another module is enabled to run. Schematic 3.
EL/TE	ECL Low Trigger Enable. Inter Module Bus (IMB) signal, when driven by the analyzer, it enables another module to look for its trigger. When received by the analyzer, it allows the analyzer to look for its trigger. Schematic 3.
H/AC	High Address Clock. Clocks the Memory Address Counters. It is derived from the Timing Generators. Schematics 2*, 7.

Table 8-1. Mnemonics, sheet 3 of 12

Mnemonic	Description
H/CCK	High Counter Clock. Clocks the Time/State Counters; developed by the 640 ns clock generator. Schematics 9*, 7.
H/CK	High Clock. Clocks Memory Address Counter Wrap latch, Trigger Enable Point latch, Measurement Complete latch, and 640 ns clock. Schematics 2*, 7, 9.
H/CQ	High Count Qualify. Allows the Time/State Counters to begin counting. Schematic 5.
H/CT	High Count Time. Allows the Time/State Counters to count at a 640 ns rate; driven by mainframe CPU. Schematics 5, 9, 11*.
H/CY	High Carry. Time/State Counter carry bit to overflow flag latch. Schematics 7, 9*.
H/DISCONB	High Disconnect Cable B. Indicates whether the emulator cable to edge connector J3 is attached. Schematic 1.
H/DISCONC	High Disconnect Cable C. Indicates whether the emulator cable to edge connector J4 is attached. Schematic 1.
H/DME	High Drive Master Enable. Drives Inter Module Bus (IMB) signal EL/ME. Schematics 3, 11*.
H/DTE	High Drive Trigger Enable. Drives Inter Module Bus (IMB) signal H/TE. Schematics 3, 11*.
H/DTR	High Drive Trigger. Drives Inter Module Bus (IMB) signal H/TR. Schematics 3, 11*.
H/EBMC	High Enable Break On Measurement Complete. Enables emulation break when the trace is complete. Schematics 7, 11*.
H/EBTP	High Enable Break On Trace Point. Enables emulation break when the trace point is found. Schematics 7, 11*.

Table 8-1. Mnemonics, sheet 4 of 12

Mnemonic	Description
H/EIMC	High Enable Interrupt On Measurement Complete. Enables interrupt of analyzer by mainframe CPU when the trace is complete. Schematics 7, 11*.
H/ELB	High Enable Lower Byte. Enables dummy byte to place all highs on the data minterm bus lower four bits, indicating a don't care condition for the emulation data bus lower byte. Schematics 4, 10*.
H/EN	High Enable. Enables analyzer to begin run mode. Schematic 2.
H/ETSC	High Enable Time/State Counter. Enables first 4 bits of the Time/State Counter to increment. Schematics 5*, 9.
H/ETSCC	High Enable Time/State Counter Carry. Carry output pulse of first four bits of the counter. Enables succeeding 4 bit counters to increment only during a carry pulse. Schematics 7, 9*.
H/EUB	High Enable Upper Byte. Enables dummy byte to place all highs on the data minterm bus upper four bits, indicating a don't care condition for the emulation data bus upper byte. Schematics 4, 10*.
H/IC	High Index Clock. Clocks the Memory Index and Occurrence Counters; also used when loading the Index Counters. It is derived from the Timing Generator. Schematics 2*, 6, 7.
H/MAC0-7	High Memory Address Counter Bus 0-7. Addresses the State Storage and Count Storage RAMs. During an analysis trace, the addresses are incremented by the analyzer. During unloading of the RAMs and PV, the addresses are incremented under control of the mainframe CPU. Uses positive logic: high = 1, low = 0. Schematics 7*, 8, 9, 11.
H/MACC	High Memory Address Counter Carry. Indicates the Memory Address Counter has counted all 256 addresses. Schematic 7.
H/MC	High Measurement Complete. Indicates to the mainframe CPU that the trace is complete. Schematics 7*, 11.

Table 8-1. Mnemonics, sheet 5 of 12

Mnemonic	Description
H/MCD	High Drive BNC2 At Measurement Complete. Drives BNC2 on rear panel when the analysis measurement is complete. Schematic 11.
H/MICC	High Memory Index Counter Carry. Indicates that Memory Index Counter has reached its terminal count. Schematic 7.
H/MICE	High Memory Index Counter Enable. Enables Memory Index Counter to increment. Schematic 7.
H/MS	High Memory Start. Indiates to the analyzer that its memory is going to be accessed by the mainframe CPU. It is driven by the CPU. Schematics 2, 10*.
H/OCC	High Occurrence Counter Carry. Indicates that the Occurrence Counter has reached its terminal count. Schematics 5, 6*.
H/OV	High Counter Overflow Flag. Indicates the Time/State Counter has overflowed. Schematics 7*, 11.
H/PV	High Performance Verification. Indicates performance verification is being run; prevents the logic analyzer from running in the analysis mode. Schematics 2, 10*.
H/QUAL	High Qualify. Indicates that the requirements for L/QUAL or L/TRIG have been meet. Schematic 7.
H/RTE	High Receive Trigger Enable. Enables analyzer to receive a trigger enable over the Inter Module Bus (IMB). Schematics 3, 11*.
H/RUN	High Run. Starts and stops the logic analyzer's functions. Derived from either the Timing Generator or the mainframe CPU. Schematics 2*, 7, 9, 11.
H/STB	High Strobe. Indicates to the analyzer that the mainframe CPU is performing a read or write from the analyzer memory. Schematics 2, 10*.

Table 8-1. Mnemonics, sheet 6 of 12

Mnemonic	Description
H/TA	High Trigger On AME (Store on Range). Directs valid patterns flagged by AME1 and AME2 to cause a trigger; and patterns flagged by Range1 and Range2 to be stored. Schematics 5, 11*.
H/TCE	High Time Count Enable. Enables 640 ns time counter. Schematic 9.
H/TEF	High Trigger Enable Flag. Indicates to the mainframe CPU the status of the Inter Module Bus (IMB) Trigger Enable line. Schematics 3*, 11.
H/TEP	High Trigger Enable Point. Confirms that the analyzer has found its trigger enable point. Schematics 7*, 11.
H/TP	High Trace Point. Confirms that the logic analyzer has found the trace point. Also, stops the Occurrence Counters. Schematics 3, 7*, 11.
H/TPD	High Drive BNC1 At Trace Point. Drives BNC1 on rear panel when the analysis measurement is is at trace point. Schematic 11.
H/WP	High Wrap. Shows the mainframe CPU that the State Storage and Count Storage RAMs have been filled and then written over again. Schematic 7*, 11.
H/XTR	High External Trigger. Indicates to the mainframe CPU that the analyzer has received a trigger from another module. Schematics 3*,11,5.
HB/A0-7	High Buffered Address Bus 0-7. Addresses the State Storage RAMs and State Recognition RAMs. Also, used as data input for Memory Address Counters. It is inverted version of mainframe CPU address bus lines L/A0-7. Uses positive logic: High = 1, low = 0. Schematics 1, 7, 11*; HB/A0 on 2, 11*.
L/A0-10	Low Address Bus 0-10. Address bus from the mainframe CPU. Uses negative logic: high = 0, low = 1. Schematics 10*, 11*.
L/ANAL	Low Analysis. Signals the analysis board to begin its cycle; driven by the emulator. Schematics 1*, 2, 10.

Table 8-1. Mnemonics, sheet 7 of 12

Mnemonic	Description
L/BKG	Low Background. Indicates to the analyzer that the emulator is in background memory (ie. non-real time). It is driven by the emulator. Schematic 9.
L/BRK	Low Break. Stops emulation, and indicates High Trace Complete or High Trace Point has occurred. Schematic 7.
L/BS	Low Bus Strobe. Gates data out of the analyzer onto the bi-directional data bus to the mainframe CPU. Schematics 10*, 11.
L/CB	Low Write Control Bits. Clocks Control Bits latch and Emulator Bus Control latch. Schematics 1, 10*, 11.
L/D0-15	Low Data Bus 0-15. Bi-directional data bus from mainframe CPU. Uses negative logic: high = 0, low = 1. Schematic 11.
L/DGMC	Low Drive Gated Master Clock. Drives Gated Master Clock Inter Module Bus (IMB) signal. Schematics 2, 11*.
L/DGMCEN	Low Drive Gated Master Clock Enable. Enables drive GMC drive. Schematics 2*, 3.
L/DOUT0-15	Low Data Output Bus 0-15. Data output bus from the Memory Index Counter, State Storage, and Time/State Counter Storage. It is gated onto the bi-directional data bus to the mainframe CPU. Uses negative logic: high = 0, low = 1. Schematics 7*, 8*, 9*, 11.
L/EA0-23	Low Emulator Address Bus 0-23. Emulator address bus that is monitored by the analysis board. Uses negative logic: high = 0, low = 1. Schematic 1.
L/EBUP	Low Enable Byte Upper. Indicates to the Word/Byte latches that the emulator is using only bits L/ED8-15 (upper byte) of the emulator data bus. It is sent by the emulator over the emulator bus. Schematic 10.
L/EBYT	Low Emulation Byte Mode. Indicates to the Word/Byte latches that the emulator is using only bits L/ED0-7 (lower byte) of the emulator data bus. It is sent by the emulator over the emulator bus. Schematic 10.

Table 8-1. Mnemonics, sheet 8 of 12

Mnemonic	Description
L/ED0-15	Low Emulator Data Bus 0-15. Emulator data bus that is monitored by the analysis board. Uses negative logic: high = 0, low = 1. Schematic 1.
L/EIT	Low Enable Internal Trigger. Indicates that another module has enabled the analyzer to begin its trace. Schematics 3*, 5.
L/ES0-7	Low Emulator Status Bus 0-7. Emulator status bus that is monitored by the analysis board. Uses negative logic: high = 0, low = 1. Schematic 1.
L/GMCEN	Low Gated Master Clock Enable. Enables GMC drive circuit. Schematics 2*, 3.
L/ID	Low Identification. Requests the analysis board identification be sent to the mainframe CPU over the bi-directional bus lines L/D1 and L/D8. The signal originates in the I/O circuitry of the mainframe. Schematic 10.
L/IR-1	Low Interrupt Request 1. Interrupt line to mainframe CPU, driven by the analyzer. Schematic 7.
L/MACSEL	Low Memory Address Counter Select. Allows data to be loaded from the mainframe CPU address bus into the Memory Address Counters. Schematic 7, 10*.
L/MC	Low Measurement Complete. Indicates the analyzer has finished the trace. Schematics 2, 7*, 11.
L/MCE	Low Measurement Complete Enable. Clocks the Measurement Complete latch. Schematic 7.
L/MEF	Low Master Enable Flag. Indicates condition of Master Enable line. Schematics 2, 3*.
L/MIC0-7	High Memory Index Counter Bus 0-7. Data output bus from Memory Index Counter. Uses negative logic: high = 0, low = 1. Schematic 7.
L/MICSEL	Low Memory Index Counter Select. Allow data to be loaded from the mainframe CPU bi-directional data bus (bits L/D0-7) into Memory Index Counters. Schematics 7, 10*.

Table 8-1. Mnemonics, sheet 9 of 12

Mnemonic	Description
L/MR	Low Master Reset. Resets or clears various flip flops, and counters, preparing the analyzer for the next run. It comes from the mainframe CPU. Schematics 7, 10*.
L/OCCSEL	Low Occurrence Counter Select. Allows the Occurrence Counters to be loaded with data from the mainframe CPU bi-directional data bus. Schematics 6, 10*.
L/OCEN	Low Occurrence Counter Enable. Enables Occurrence Counters to count. Schematics 5, 6*.
L/POP	Low Power-On-Pulse. Indicates to the analyzer that power has been applied to the system; driven by mainframe power supply. Schematic 11.
L/PV	Low Performance Verification. Indicates that PV is being run and prevents the analyzer from running in the analysis mode. Schematics 2, 10*.
L/QUAL	Low Qualify. Indicates that the information on the emulator bus satisfies the requirements of the trace specifications. Schematics 5*, 7.
L/RCH	Low Read Count, High. Enables read of highest 8 bits in the Time/State Counter Storage. Schematics 9, 10*.
L/RCL	Low Read Count, Low. Enables read of lowest 16 bits in the Time/State Counter Storage. Schematics 9, 10*.
L/REAH	Low Read Emulator Address, High Byte. Enables read of highest 8 bits of emulator address in the State Storage RAMs. Schematics 8, 10*.
L/REAL	Low Read Emulator Address, Low Word. Enables read of lowest 16 bits of emulator address in the State Storage RAMs. Schematics 8, 10*.
L/RED	Low Read Emulator Data. Enables read of 16 bit emulator data bus in the State Storage RAMs. Schematics 8, 10*.
L/RES	Low Read Emulator Status. Enables read of 8 bit emulator status bus in the State Storage RAMs. Schematics 8, 10*.

Table 8-1. Mnemonics, sheet 10 of 12

Mnemonic	Description
L/RF	Low Read Flags. Gates analyzer status flags onto the Low Data Output bus. Schematics 10*, 11.
L/RH	Low Run/Halt. Indicates whether the analyzer is in the run or halt mode. Low = run. Schematics 2, 10*.
L/RME	Low Receive Master Enable. Allows Inter Module Bus (IMB) Master Enable signal to be received from another module by the analyzer. Schematics 3, 11*.
L/RP	Low Read Pointers. Gates the 8 bit Memory Index Counter output onto the Low Data Output bus. Schematics 7, 10*, 11.
L/RTR	Low Receive Trigger. Allows the analyzer to receive the Inter Module Bus (IMB) Trigger signal from another module. Schematics 3, 11*.
L/RUN	Low Run. Starts and stops the logic analyzer's functions. Derived from either the Timing Generator or the mainframe CPU. Schematics 2*, 5.
L/RW	Low RAM Write. Enables write to State Storage RAMs and Time/State Counter Storage RAMs. Schematics 2*, 8, 9.
L/SEL	Low Select. Allows the analyzer's identification code to be returned over the mainframe CPU bi-directional data bus. It is also used to enable the analyzer during measurments. Schematic 10.
L/STB	Low Strobe. When the mainframe CPU is writing, indicates that there is valid data on the bi-directional data bus. When the mainframe CPU is reading, indicates that data may be placed on the bus. Schematic 10.
L/STM	Low Start Memory. Signal from mainframe processor that indicates a memory operation is beginning. Schematic 10.
L/TCK	Low Time Clock. Input to the 640 ns Count Time Synchronizer. It is derived from B/25MHZ. Schematic 9.

Table 8-1. Mnemonics, sheet 11 of 12

Mnemonic	Description
L/TEP	Low Trigger Enable Point. Indicates that the analyzer is has found its trigger enable point. Schematics 5, 7*.
L/TEPC	Low Trigger Enable Point Control. Controls setting of the Trace Point latch. Schematics 7, 11*.
L/TP	Low Trace Point. Indicates that the analyzer has found the trigger word or sequence. It is routed from the analyzer board through the motherboard to connector BNC1 on the rear panel for triggering external devices. Schematics 5, 7*, 11.
L/TPE	Low Trace Point Enable. When Trace Point is found, enables the Memory Index Counters to increment. Schematic 7.
L/TRIG	Low Trigger. Indicates that the trace specification has been satisfied. Schematic 5*, 7.
L/WADM	Low Write Address & Data Minterms. Enables write to highest 4 bits of the Address Minterm RAMs and all 8 bits of the Data Minterm RAMs. Schematics 4, 10*.
L/WASM	Low Write Address & Status Minterms. Enables write to lower 8 bits of Address Minterm and the 4 bits of Status Minterm. Schematics 4, 10*.
L/WRT	Low Write. Enables the mainframe CPU to write to the analyzer; produced by the CPU. Schematic 10.
LB/D0-15	Low Buffered Data Bus 0-15. Used to program Occurrence Counters and Control Bits Latch. Also, bits 0-7 are used to load the Memory Index Counter. It is the buffered version of the bi-directional data bus from the mainframe CPU. Uses negative logic: high = 0, low = 1. Schematics 4, 6, 7, 11*.
LHB/A0	Latched High Buffered Address 0. Latched version of HB/A0. Schematics 2*, 3.
LL/EB	Low Latched Emulator Bus. Latched emulator bus that includes Low Latched Emulator Address Bus, Low Latched Emulator Data Bus, and Low Latched Emulator Status Bus. Uses negative logic: high = 0, low = 1. Schematics 1*, 4, 8.

Table 8-1. Mnemonics, sheet 12 of 12

Mnemonic	Description
POL	Polarity. Determines polarity of L/MC and L/TP. It is controlled by software and is not operator defined. Schematic 11.
RANGE1	Data and Status Range Qualify. Indicates whether the emulator data bus and status bus are within the singly bounded range within the trace specification. Schematic 5.
RANGE2	Address Range Qualify. Indicates whether the emulator address bus is within the doubly bounded range in the trace specification. Schematic 5.
RH1	Run/halt Latch Input. Input to the Run/halt latch that indicates run or halt mode. Schematic 2.
SM0-7	Status Minterm Bus 0-7. Data output bus from State Recognition Storage RAMs that indicates whether trace specifications for emulation status have been detected. Uses positive logic: high =1, low = 0. Schematics 4*, 5.
TG1-4	Timing Generators. Various signals in the Timing Generator. Schematic 2.

Table 8-2. Logic Symbols, sheet 1 of 3

GENERAL

All signals flow from left to right, relative to the symbol's orientation with inputs on the left side of the symbol, and outputs on the right side of the symbol (the symbol may be reversed if the dependency notation is a single term.)

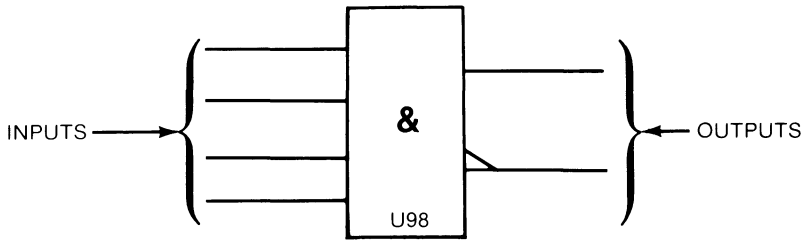
All dependency notation is read from left to right (relative to the symbol's orientation).

An external state is the state of an input or output outside the logic symbol.

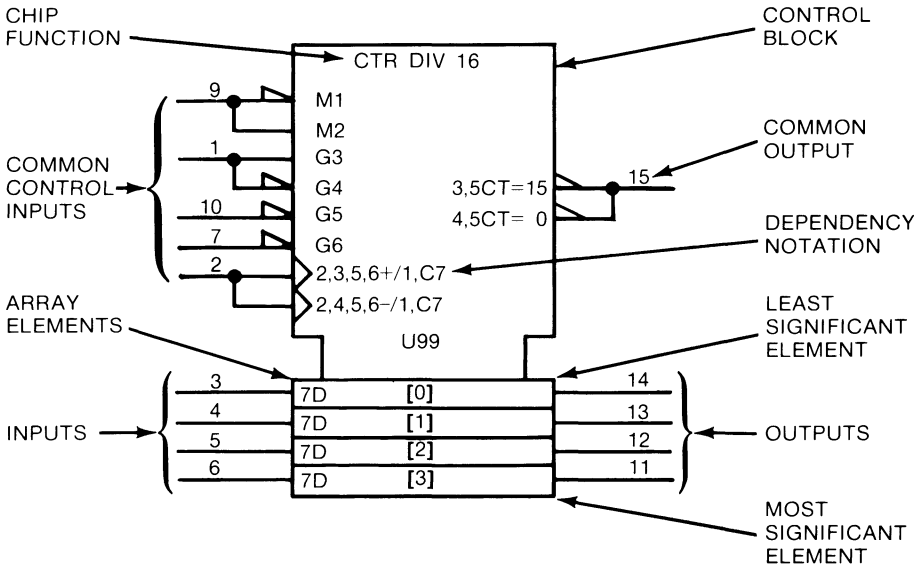
An internal state is the state of an input or output inside the logic symbol. All internal states are True = High.

SYMBOL CONSTRUCTION

Some symbols consist of an outline or combination of outlines together with one or more qualifying symbols, and the representation of input and output lines.



Some have a common Control Block with an array of elements:



CONTROL BLOCK - All inputs and dependency notation affect the array elements directly. Common outputs are located in the control block. (Control blocks may be above or below the array elements.)

ARRAY ELEMENTS -All array elements are controlled by the control block as a function of the dependency notation. Any array element is independent of all other array elements. Unless indicated, the least significant element is always closest to the control block. The array elements are arranged by binary weight. The weights are indicated by powers of 2 (shown in **[ ]**).

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Table 8-2. Logic Symbols, sheet 2 of 3

INPUTS - Inputs are located on the left side of the symbol and are affected by their dependency notation.

Common control inputs are located in the control block and control the inputs/outputs to the array elements according to the dependency notation.

Inputs to the array elements are located with the corresponding array element with the least significant element closest to the control block.

OUTPUTS - Outputs are located on the right side of the symbol and are effected by their dependency notation.

Common control outputs are located in the control block.

Outputs of array elements are located in the corresponding array element with the least significant bit closest to the control block.

CHIP FUNCTION - The labels for chip functions are defined, i.e., CTR - counter, MUX - multiplexer.

DEPENDENCY NOTATION

Dependency notation is always read from left to right relative to the symbol's orientation.

Dependency notation indicates the relationship between inputs, outputs, or inputs and outputs. Signals having a common relationship will have a common number, i.e., C7 and 7D....C7 controls D. Dependency notation 2,3,5,6+/1,C7 is read as when 2 and 3 and 5 and 6 are true, the input will cause the counter to increment by one count....or (/) the input (C7) will control the loading of the input value (7D) into the D flip-flops.

The following types of dependencies are defined:

a. AND (G), OR (V), and Negate (N) denote Boolean relationship between inputs and outputs in any combination.

b. Interconnection (Z) indicates connections inside the symbol.

c. Control (C) identifies a timing input or a clock input of a sequential element and indicates which inputs are controlled by it.

d. Set (S) and Reset (R) specify the internal logic states (outputs) of an RS bistable element when the R or S input stands at its internal 1 state.

e. Enable (EN) identifies an enable input and indicates which inputs and outputs are controlled by it (which outputs can be in their high impedance state).

f. Mode (M) identifies an input that selects the mode of operation of an element and indicates the inputs and outputs depending on that mode.

g. Address (A) identifies the address inputs.

h. Transmission (X) identifies bi-directional inputs and outputs that are connected together when the transmission input is true.

DEPENDENCY NOTATION SYMBOLS

A	Address (selects inputs/outputs) (indicates binary range)	N	Negate (compliments state)
C	Control (permits action)	R	Reset Input
EN	Enable (permits action)	S	Set Input
G	AND (permits action)	V	OR (permits action)
M	Mode (selects action)	Z	Interconnection
		X	Transmission

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Table 8-2. Logic Symbols, sheet 3 of 3

OTHER SYMBOLS

∩ Analog Signal	◺◿ Inversion	→ Shift Right (or up)
& AND	O Negation	/ Solidus (allows an input or output to have more than one function)
} { Bit Grouping	—✕— Nonlogic Input/Output	▽ Tri-State
▷ Buffer	◇ Open Circuit (external resistor)	, Causes notation and symbols to effect inputs/outputs in an AND relationship, and to occur in the order read from left to right.
! Compare	◇ Open Circuit (external resistor)	
▷ Dynamic	≥1 OR	( ) Used for factoring terms using algebraic techniques.
=1 Exclusive OR	◇ Passive Pull Down (internal resistor)	[ ] Information not defined.
⊓ Hysteresis	◇ Passive Pull Up (internal resistor)	Φ Logic symbol not defined due to complexity.
? Interrogation	⌐ Postponed	
— Internal Connection	← Shift Left (or down)	

LABELS

BG	Borrow Generate	CO	Carry Output	J	J Input
BI	Borrow Input	CP	Carry Propagate	K	K Input
BO	Borrow Output	CT	Content	P	Operand
BP	Borrow Propagate	D	Data Input	T	Transition
CG	Carry Generate	E	Extension (input or output)	+	Count Up
CI	Carry Input	F	Function	–	Count Down

MATH FUNCTIONS

Σ	Adder	>	Greater Than
ALU	Arithmetic Logic Unit	<	Less Than
COMP	Comparator	CPG	Look Ahead Carry Generator
DIV	Divide By	π	Multiplier
=	Equal To	P-Q	Subtractor

CHIP FUNCTIONS

BCD	Binary Coded Decimal	DIR	Directional	RAM	Random Access Memory
BIN	Binary	DMUX	Demultiplexer	RCVR	Line Receiver
BUF	Buffer	FF	Flip-Flop	ROM	Read Only Memory
CTR	Counter	MUX	Multiplexer	SEG	Segment
DEC	Decimal	OCT	Octal	SRG	Shift Register

DELAY and MULTIVIBRATORS

⊓⊓⊓	Astable
100 ns	Delay
1⊓	Nonretriggerable Monostable
NV	Nonvolatile
⊓⊓_	Retriggerable Monostable

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Table 8-3. Schematic Diagram Notes

ETCHED CIRCUIT BOARD

FRONT PANEL MARKING

REAR-PANEL MARKING

MANUAL CONTROL

SCREWDRIVER ADJUSTMENT

TP1 ELECTRICAL TEST POINT TP (WITH NUMBER)

NUMBERED WAVEFORM NUMBER CORRESPONDS TO ELECTRICAL TEST POINT NO.

LETTERED TEST POINT NO MEASUREMENT AID PROVIDED

COMMON CONNECTIONS. ALL LIKE-DESIGNATED POINTS ARE CONNECTED.

1 3 NUMBER ON WHITE BACKGROUND = OFF-PAGE CONNECTION. LARGE NUMBER ADJACENT = SERVICE SHEET NUMBER FOR OFF-PAGE CONNECTION.

A CIRCLED LETTER = OFF-PAGE CONNECTION BETWEEN PAGES OF SAME SERVICE SHEET.

(925) WIRE COLORS ARE GIVEN BY NUMBERS IN PARENTHESES USING THE RESISTOR COLOR CODE

[(925) IS WHT-RED-GRN]

0 - BLACK	5 - GREEN
1 - BROWN	6 - BLUE
2 - RED	7 - VIOLET
3 - ORANGE	8 - GRAY
4 - YELLOW	9 - WHITE

* OPTIMUM VALUE SELECTED AT FACTORY, TYPICAL VALUE SHOWN; PART MAY HAVE BEEN OMITTED.

UNLESS OTHERWISE INDICATED:
RESISTANCE IN OHMS
CAPACITANCE IN PICOFARADS
INDUCTANCE IN MICROHENRIES

μP	=	MICROPROCESSOR
P/O	=	PART OF
NC	=	NO CONNECTION
CW	=	CLOCKWISE END OF VARIABLE RESISTOR

INDICATES SINGLE SIGNAL LINE

NUMBER OF LINES ON A BUS

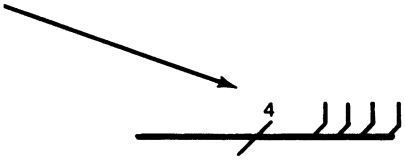

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Table 8-4. Integrated Circuit to Schematic Cross Reference

IC	Schematic Sheet	IC	Schematic Sheet
U 1	3	U 64	8
U 3	3	U 65	9
U 4	3	U 66	9
U 5	2, 3	U 67	9
U 6	7, 9	U 68	9
U 7	1	U 69	9
U 8	1	U 70	9
U 9	1	U 71	5, 7
U 10	1	U 72	7
U 11	1	U 73	5, 7
U 12	1	U 74	5
U 13	1	U 75	5
U 14	1	U 76	7
U 15	1	U 77	11
U 16	1	U 78	7
U 17	1	U 80	11
U 18	1	U 81	9
U 19	2, 3	U 82	9
U 20	2	U 83	9
U 23	2	U 84	9
U 24	2, 3	U 85	9
U 25	10	U 86	9
U 26	4	U 87	6
U 27	4	U 88	7
U 28	4	U 89	3, 7
U 29	4	U 91	5, 7
U 30	4	U 92	5, 9
U 31	4	U 93	7
U 32	4	U 94	7
U 33	4	U 95	7
U 34	4	U 96	4
U 36	2	U 97	5
U 38	9	U 98	5
U 39	3	U 99	5
U 40	9	U100	5
U 41	2	U101	5
U 42	8	U102	5
U 43	8	U103	6
U 44	8	U104	6
U 45	8	U106	10
U 46	8	U107	10
U 47	8	U108	11
U 48	8	U109	11
U 49	8	U110	11
U 50	8	U111	11
U 51	3, 9	U112	11
U 52	2, 9	U113	11
U 53	2	U114	11
U 54	9	U115	7, 10
U 55	2	U116	10, 11
U 59	1, 2	U117	10
U 60	9	U118	11
U 61	7, 10	U119	7, 10
U 62	8	U121	6
U 63	8		

ICs On This Schematic

REF. DES.	HP PART NO.	MFG. PART NO.
U7, 9,11,13, 15,17	1820-1917	SN74LS240N
U8,10	1820-1997	SN74LS374N
U12,14,16,18	1820-1677	SN74S374N
U59	1820-2693	1820-2693

PARTS ON THIS SCHEMATIC

U58 resistor pack

IC POWER SUPPLY PIN CONFIGURATION

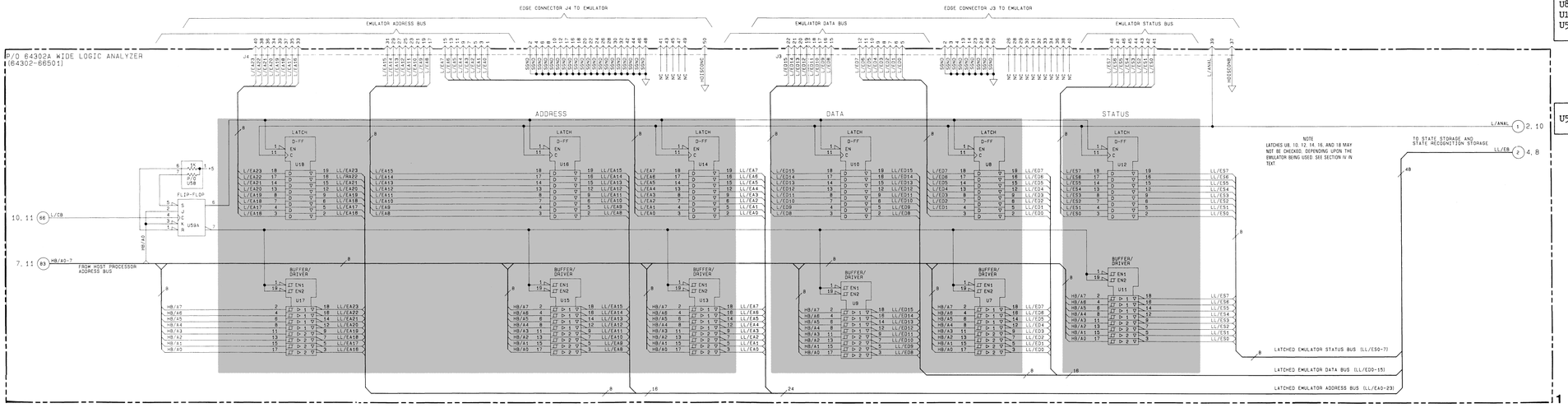
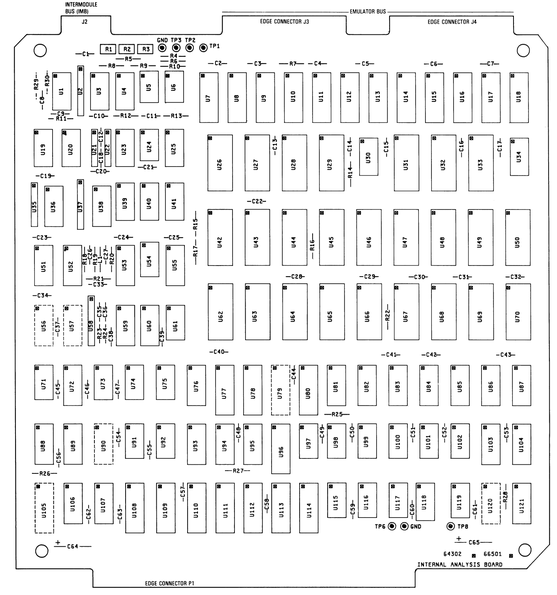
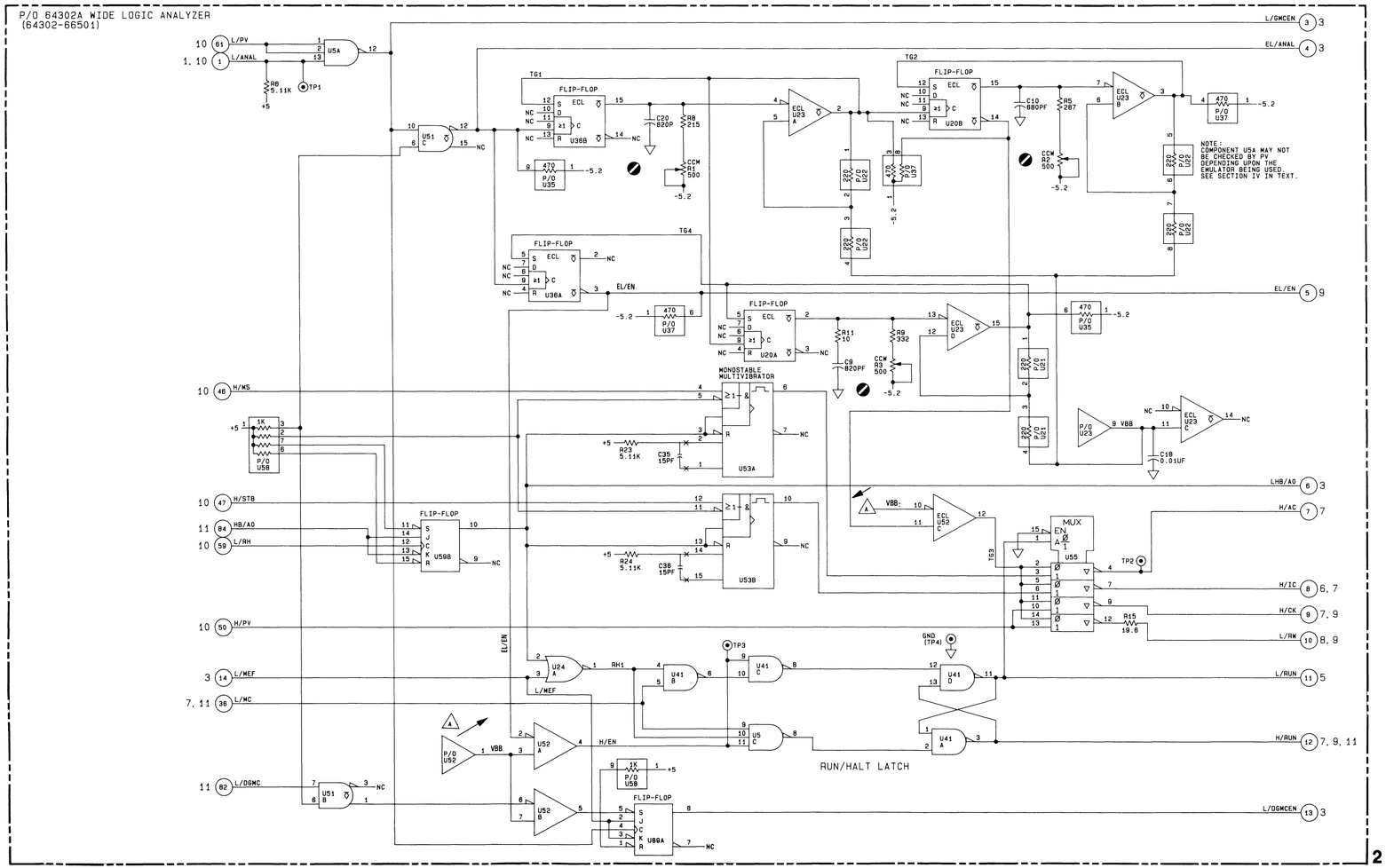


Figure 8-2.
Service Sheet 1, Emulator Bus Latch



Component Locator



ICs ON THIS SCHEMATIC

REF. DES.	HP PART NO.	MFG. PART NO.
U5	1820-2687	1820-2687
U20,36	1820-1225	MC10231P
U23	1820-0809	MC10115P
U24	1820-1144	SN74LS02N
U41	1820-2684	1820-2684
U51	1820-1173	MC10124L
U52	1820-1052	MC10125L
U53	1820-1782	AM26S02PC
U55	1820-2695	1820-2695
U59	1820-2693	1820-2693
U89	1820-1282	SN74LS109AN

PARTS ON THIS SCHEMATIC

C9,10,18,20,35,36
R1,2,3,5,6,8,9,11,23,24
TP1,TP2,TP4
U21,22,35,37,58 resistor packs

IC POWER SUPPLY PIN CONFIGURATION

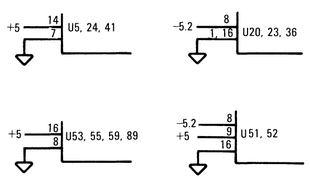
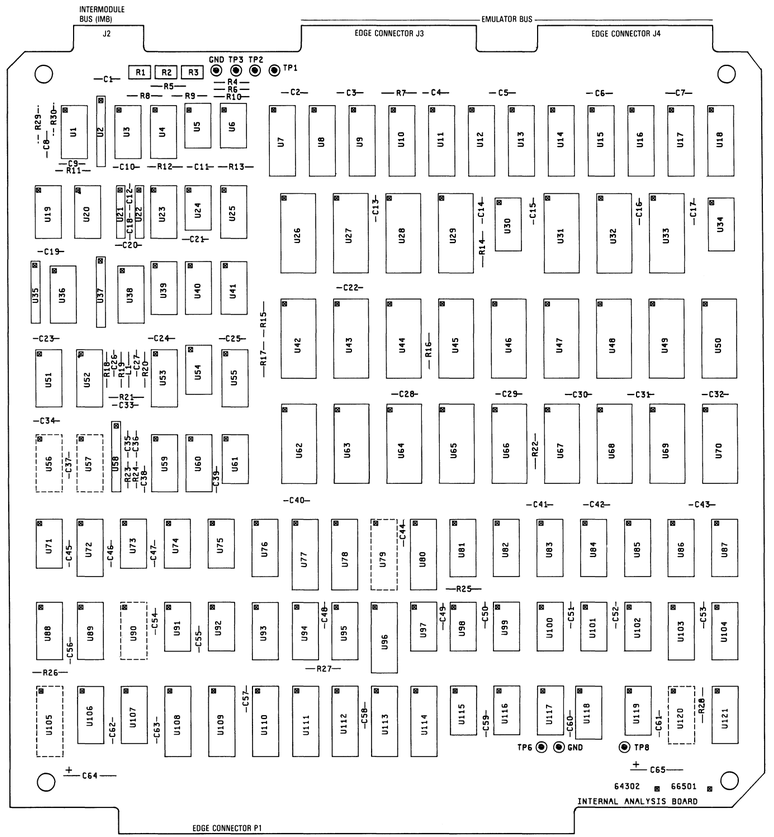
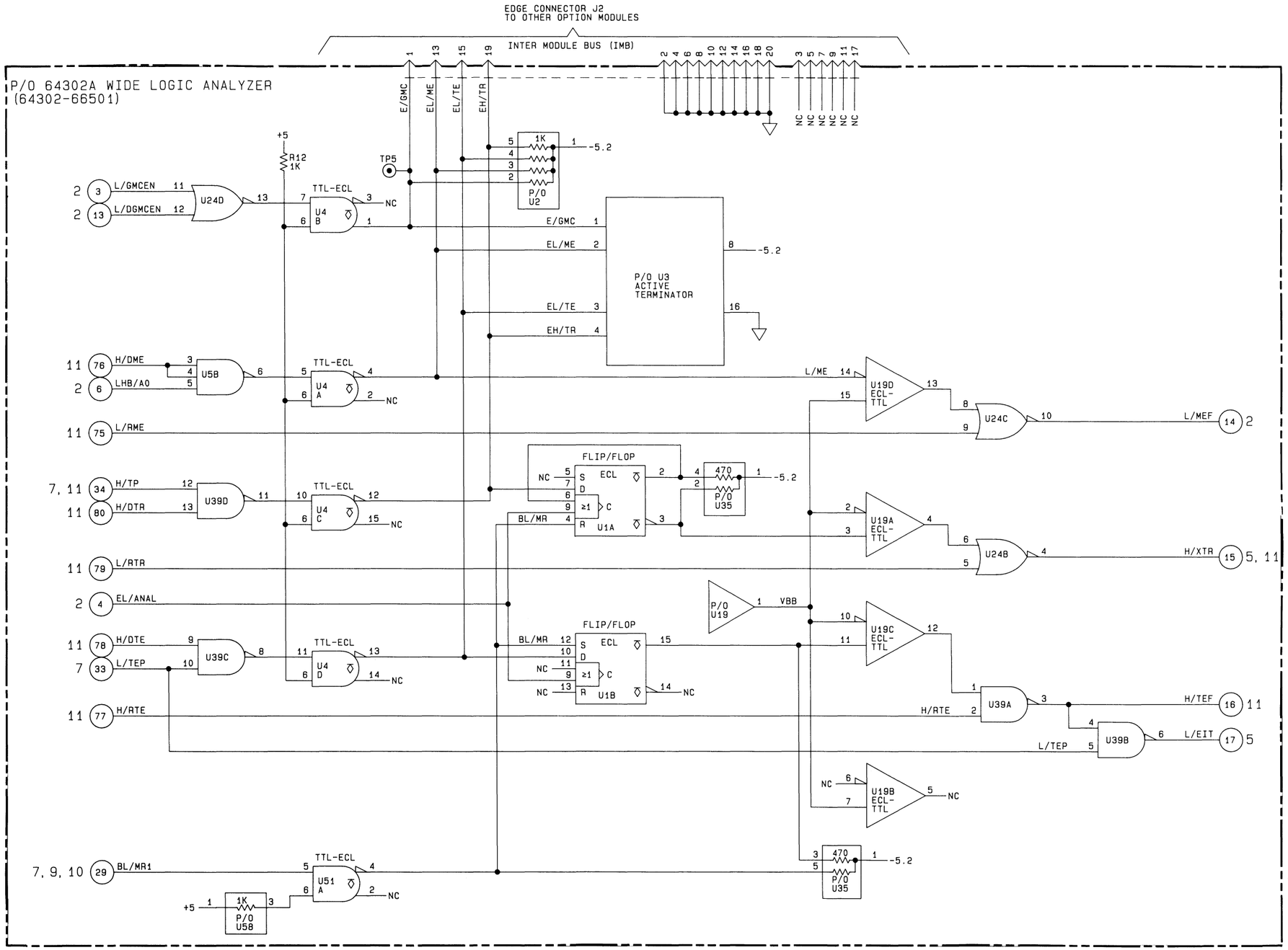


Figure 8-3.
Service Sheet 2, Timing



Component Locator



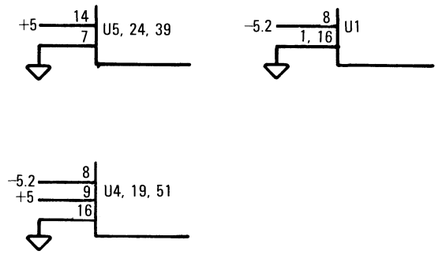
ICs ON THIS SCHEMATIC

REF. DES.	HP PART NO.	MFG. PART NO.
U1	1820-1225	MC10231P
U3	1820-2359	F10014PC
U4,51	1820-1173	MC10124L
U5	1820-2687	1820-2687
U19	1820-1052	MC10125L
U24	1820-1144	SN74LS02N
U39	1820-1197	SN74LS00N

PARTS ON THIS SCHEMATIC

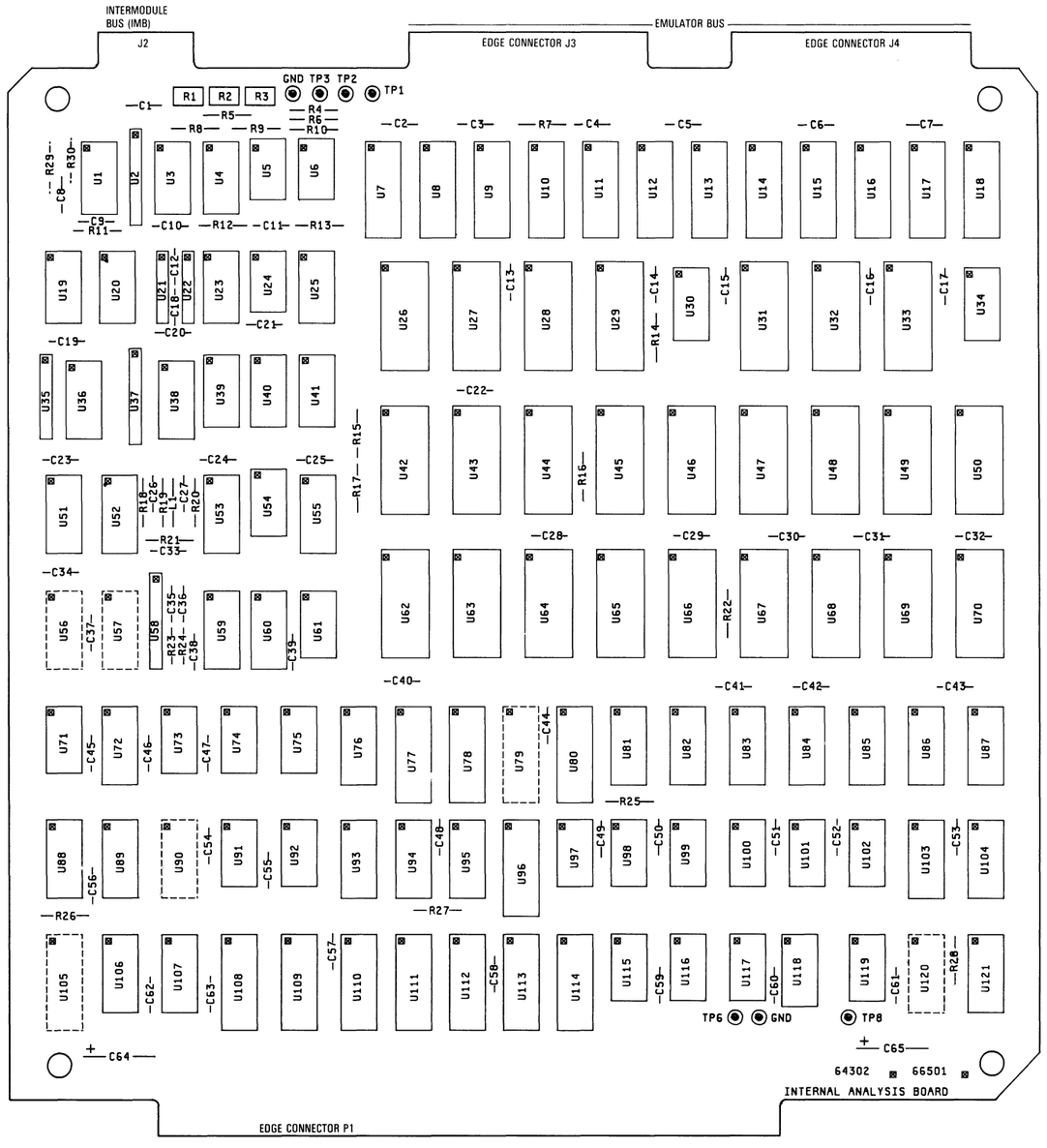
U2,35,58 resistor packs

IC POWER SUPPLY PIN CONFIGURATION

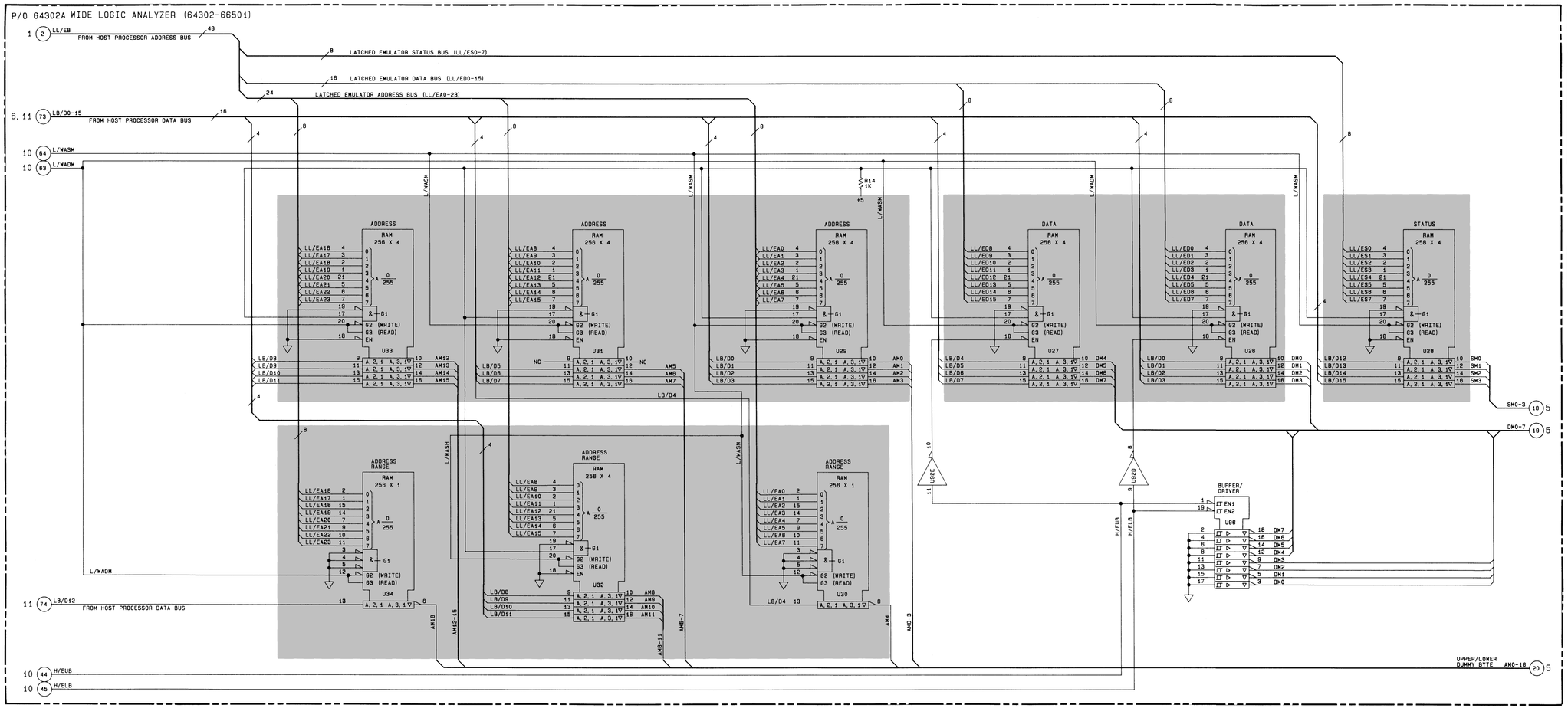


3

Figure 8-4.
Service Sheet 3, Inter Module Bus (IMB)



Component Locator



4

ICs ON THIS SCHEMATIC

REF. DES.	HP PART NO.	MFG. PART NO.
U26,27,31, 32,33,	1816-1334	93422DC
U28,29	1816-1308	93L422PC
U30	1816-1092	1816-1092
U34	1816-1092	1816-1092
U92	1820-0683	SN7404N
U96	1820-1917	SN74LS240N

PARTS ON THIS SCHEMATIC

R14

IC POWER SUPPLY PIN CONFIGURATION

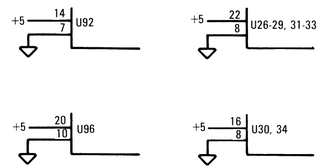
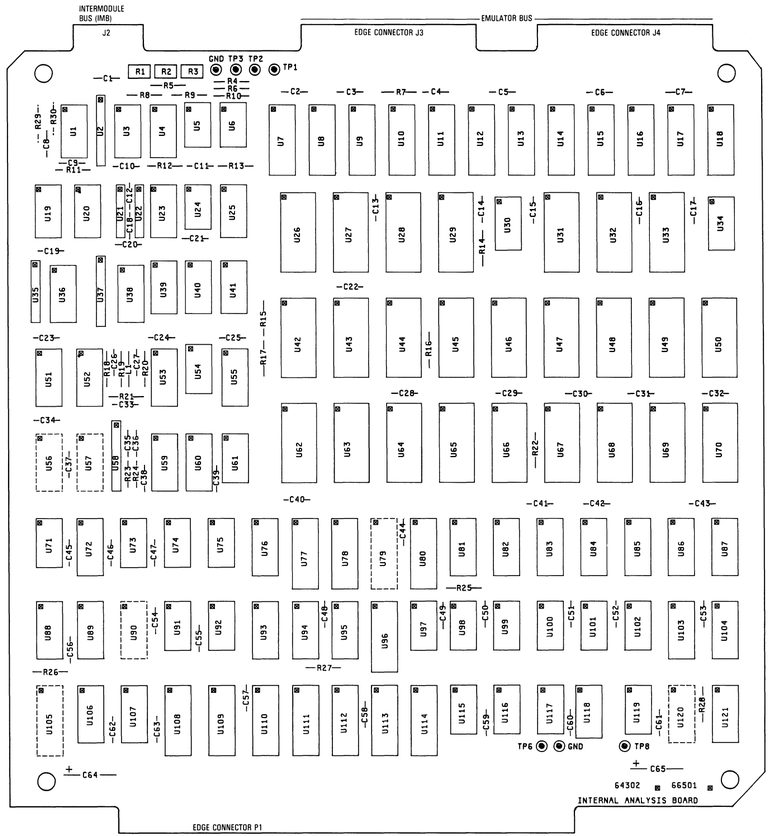


Figure 8-5.
Service Sheet 4, State Recognition Storage



Component Locator

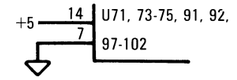
ICs ON THIS SCHEMATIC

REF. DES.	HP PART NO.	MFG. PART NO.
U71	1820-2690	1820-2690
U73	1820-1158	SN74S51N
U74,75,101, 102	1820-0691	SN74S64N
U91,98	1820-2685	1820-2685
U92	1820-0683	SN74S04N
U97,99,100	1820-2687	1820-2687

PARTS ON THIS SCHEMATIC

None

IC POWER SUPPLY PIN CONFIGURATION



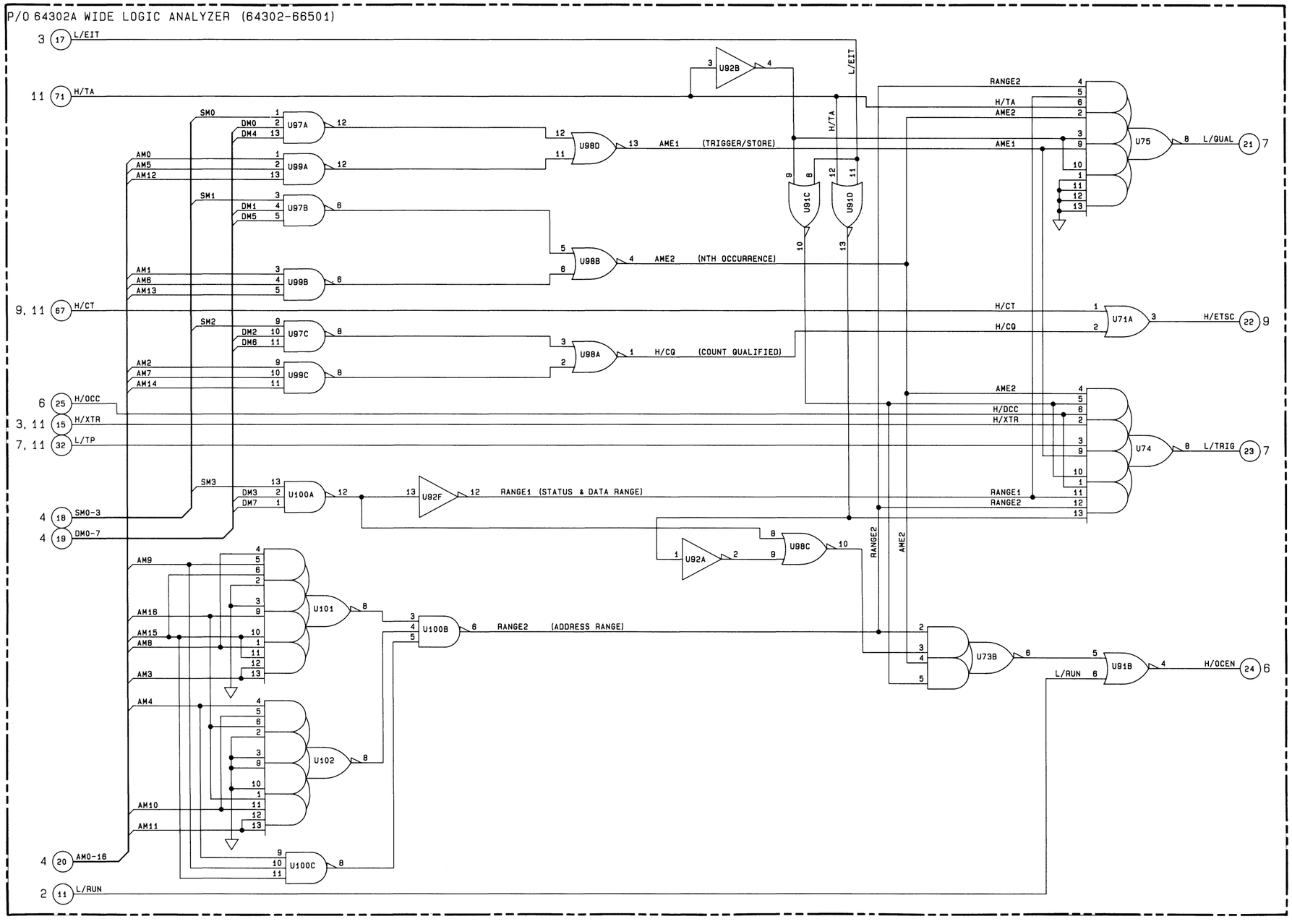
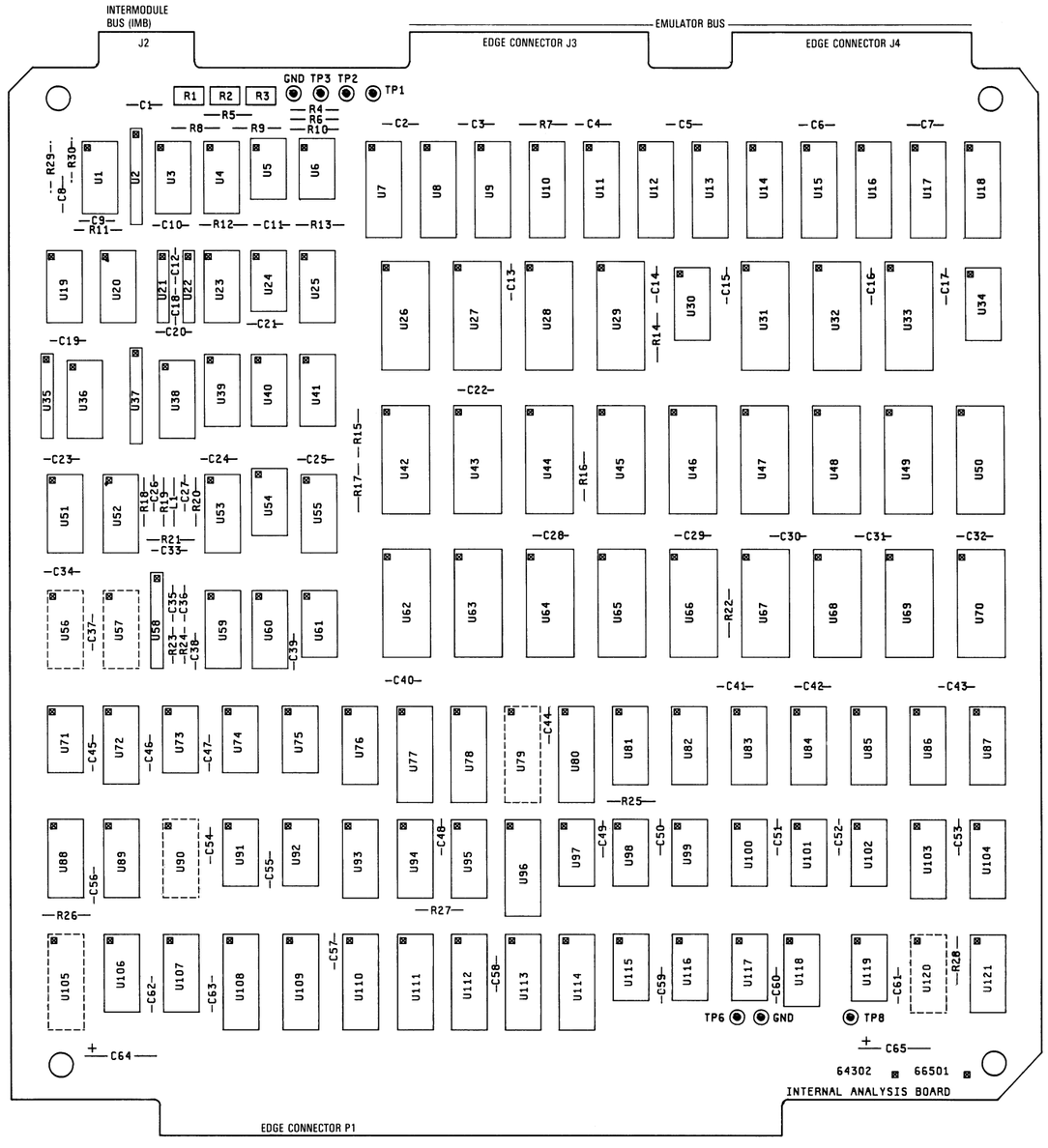
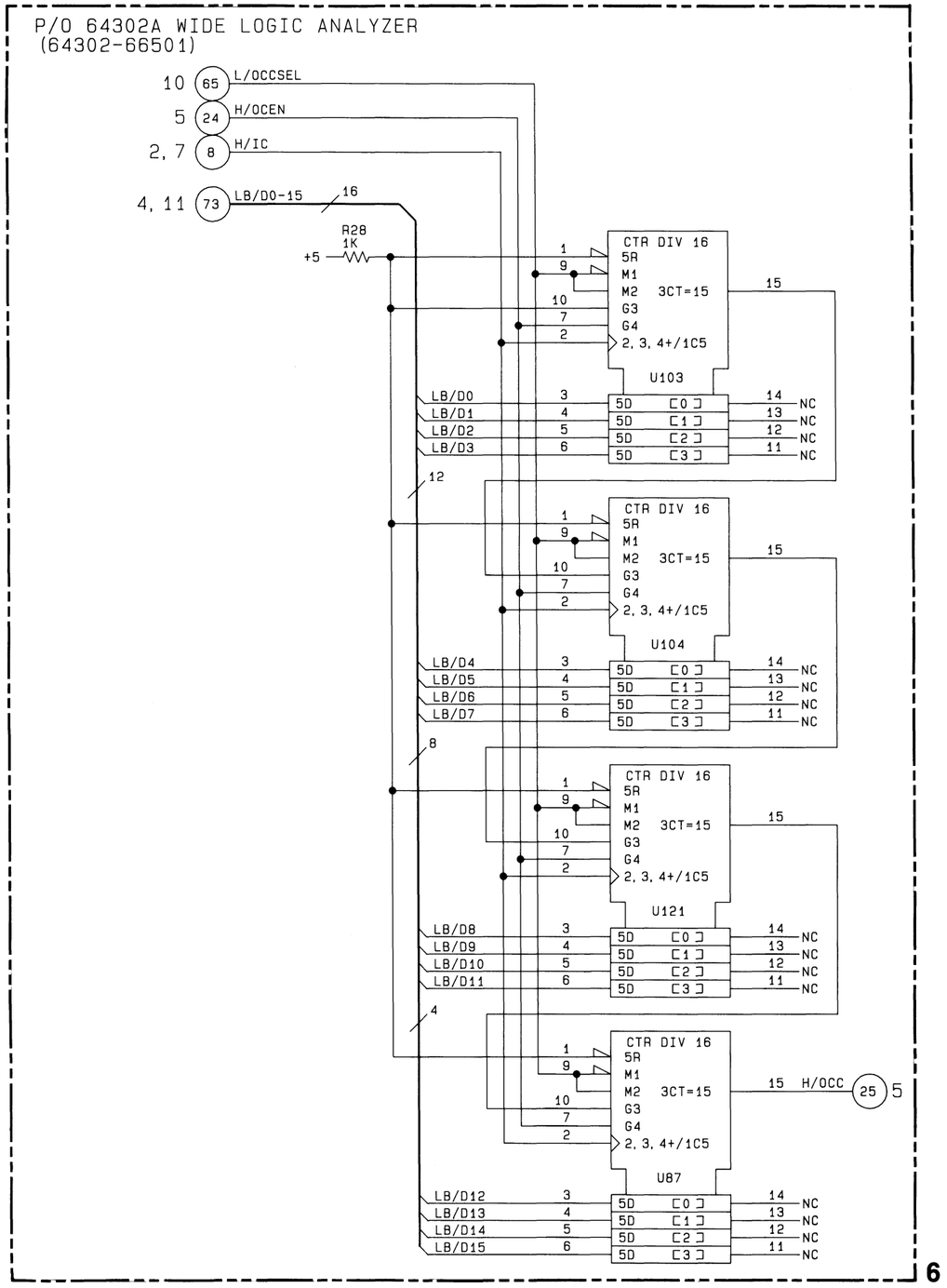


Figure 8-6.
Service Sheet 5, State Recognition Decoding



Component Locator



ICs ON THIS SCHEMATIC

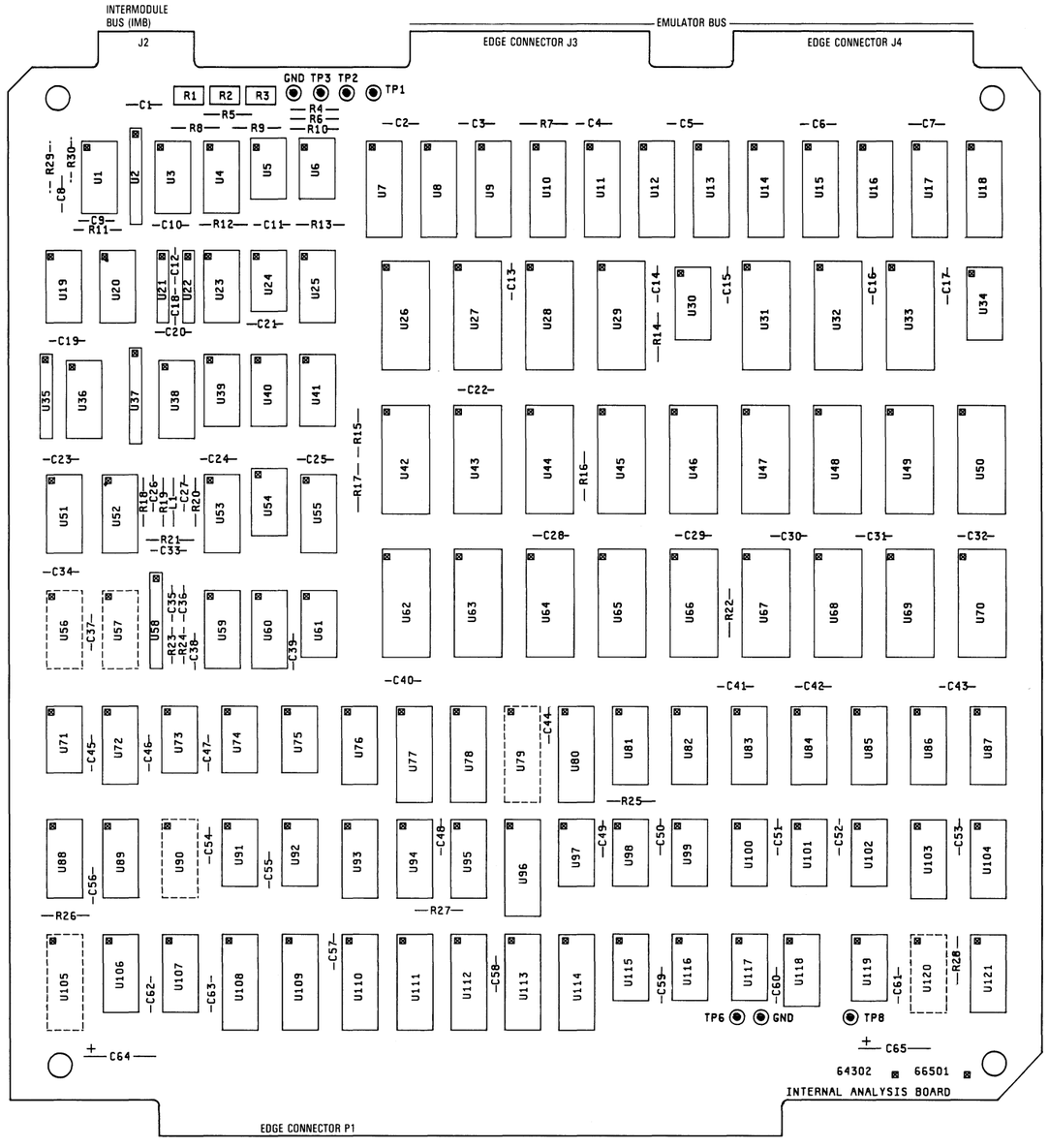
REF. DES.	HP PART NO.	MFG. PART NO.
U87,103,104, 121	1820-1430	SN74LS161AN

PARTS ON THIS SCHEMATIC

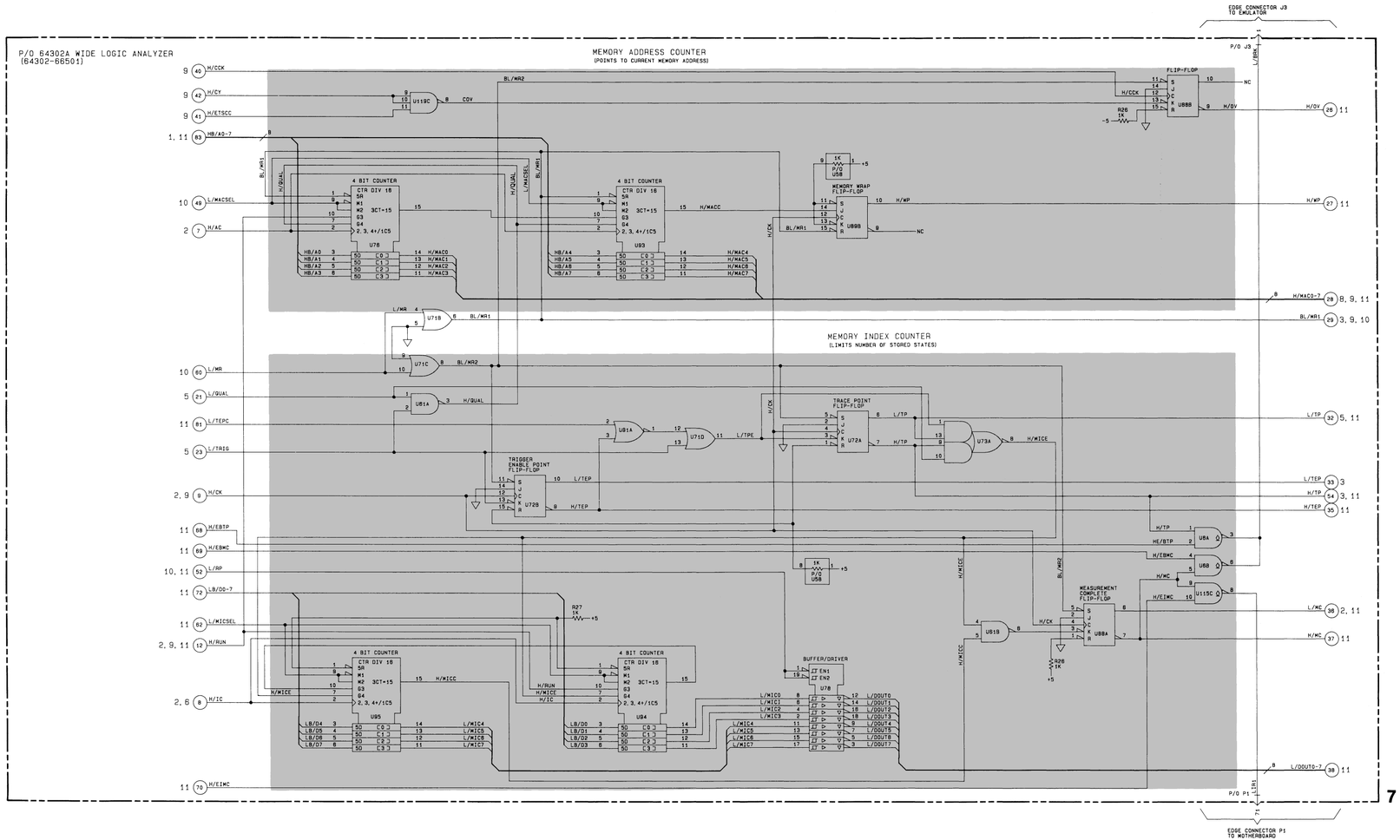
R28

IC POWER SUPPLY PIN CONFIGURATION

Figure 8-7.
Service Sheet 6, Occurrence Counter



Component Locator



ICs ON THIS SCHEMATIC

REF. DES.	HP PART NO.	MFG. PART NO.
U6	1820-0682	SN74S03N
U61	1820-2684	1820-2684
U71	1820-2690	1820-2690
U72,88	1820-2693	1820-2693
U73	1820-1158	SN74S51N
U76,93,94,95	1820-1430	SN74LS161AN
U78	1820-2024	SN74LS244N
U89	1820-1282	SN74LS109AN
U91	1820-2685	1820-2685
U115	1820-0269	SN7403N
U119	1820-1202	SN74LS10N

PARTS ON THIS SCHEMATIC

R26,27
U58 resistor pack

IC POWER SUPPLY PIN CONFIGURATION

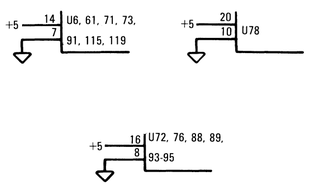
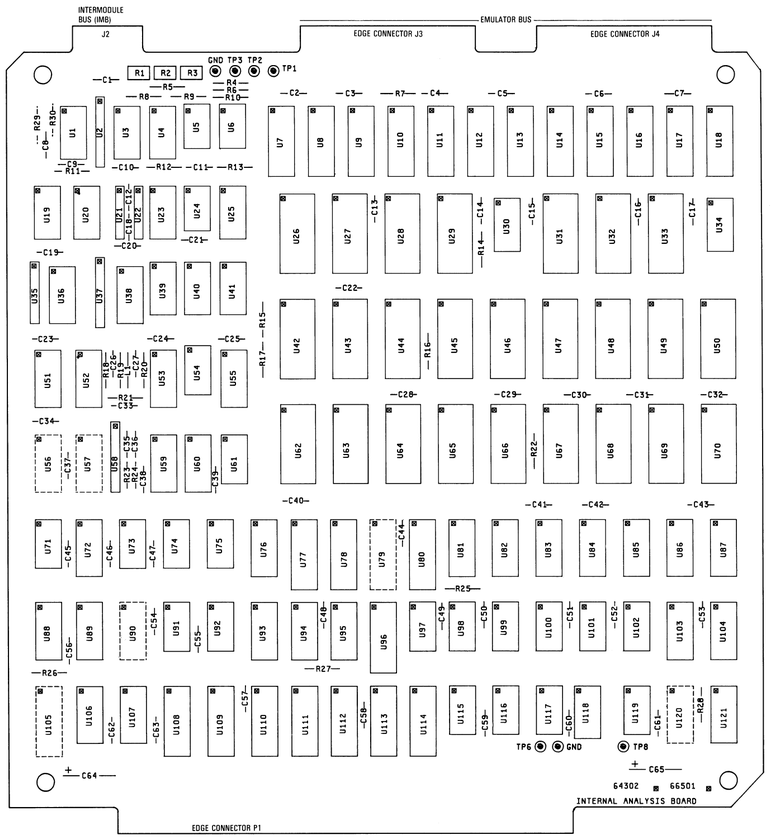


Figure 8-8.
Service Sheet 7, State Storage Control



Component Locator

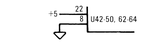
ICs ON THIS SCHEMATIC

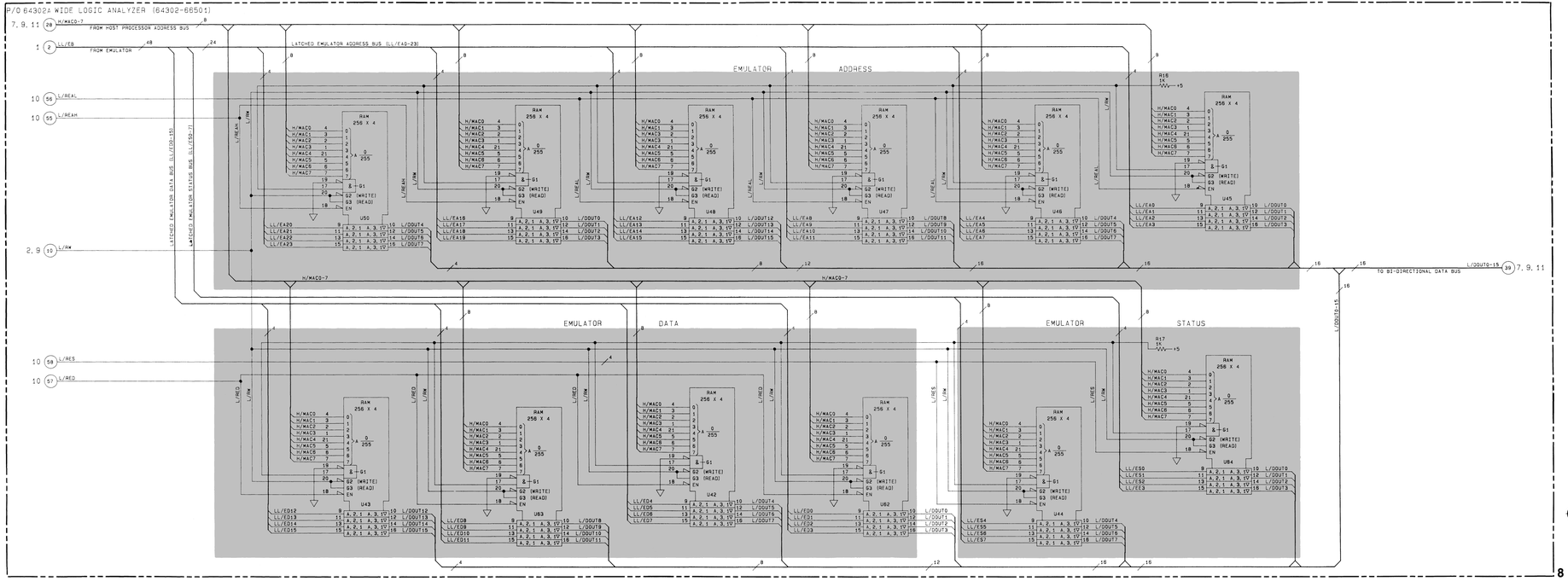
REF. DES.	HP PART NO.	MFG. PART NO.
U42,43,44, 45,46,47, 48,49,50, 62,63,64	1816-1308	93L422PC

PARTS ON THIS SCHEMATIC

R16,17

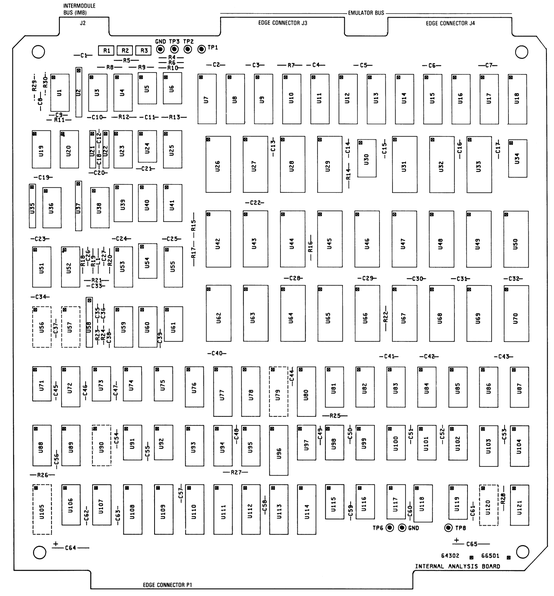
IC POWER SUPPLY PIN CONFIGURATION



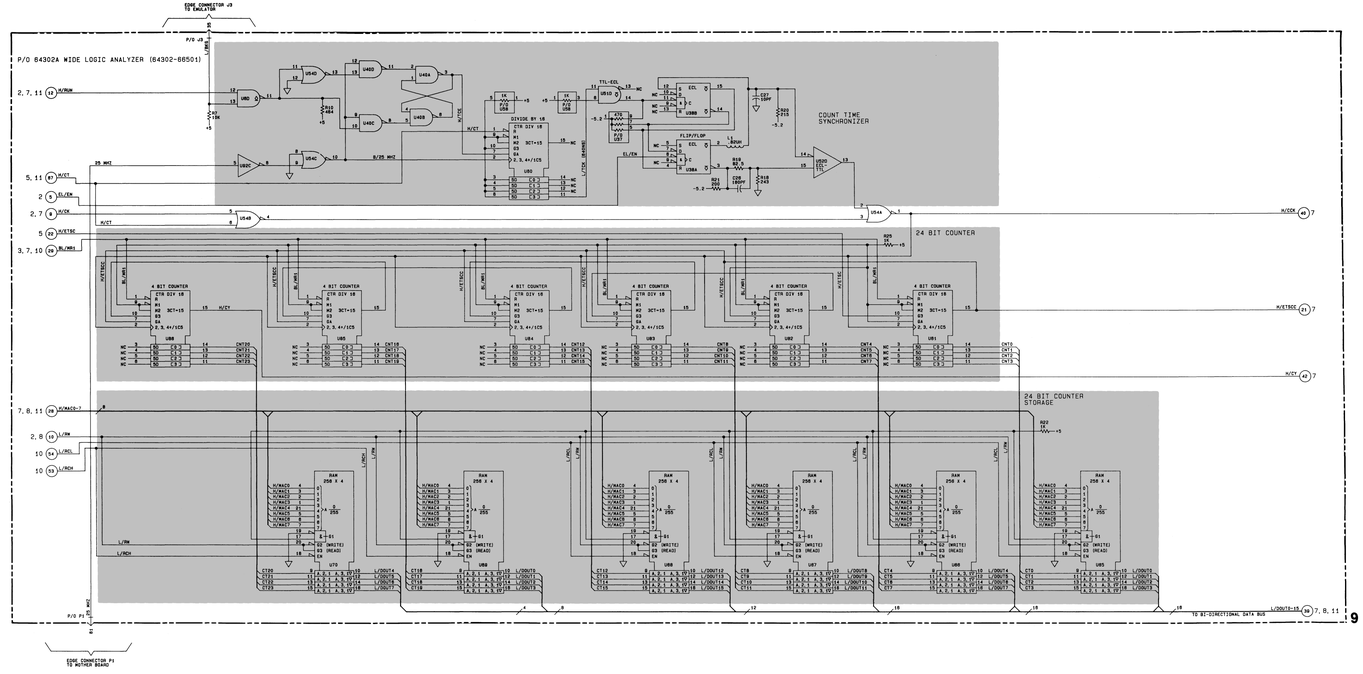


8

Figure 8-9.
Service Sheet 8, State Storage



Component Locator



9

ICs ON THIS SCHEMATIC

REF. DES.	HP PART NO.	MFG. PART NO.
U6	1820-0682	SN74S03N
U38	1820-1944	MC10130L
U40	1820-2684	1820-2684
U51	1820-1173	MC10124L
U52	1820-1052	MC10125L
U54	1820-2685	1820-2685
U60	1820-1475	93S16DC
U65,66,67, 68,69,70	1816-1308	93L422PC
U81,82,83, 84,85,86	1820-1430	SN74LS161AN
U92	1820-0683	SN74S04N

PARTS ON THIS SCHEMATIC

C26,27
L1
R7,10,18,19,20,21,22,25
U37,58 resistor packs

IC POWER SUPPLY PIN CONFIGURATION

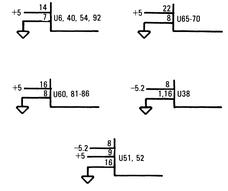
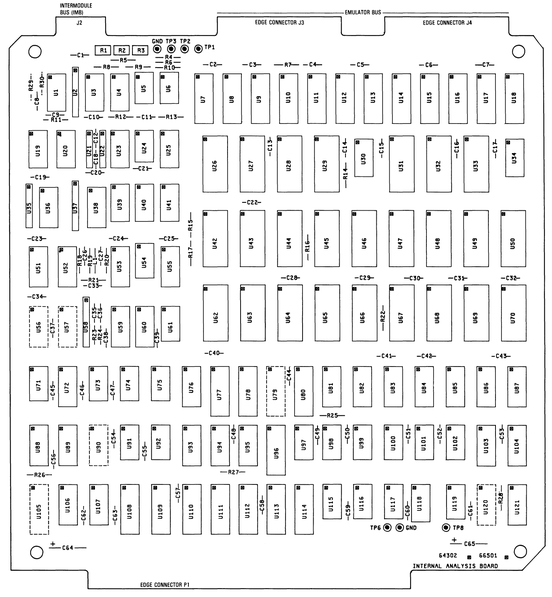
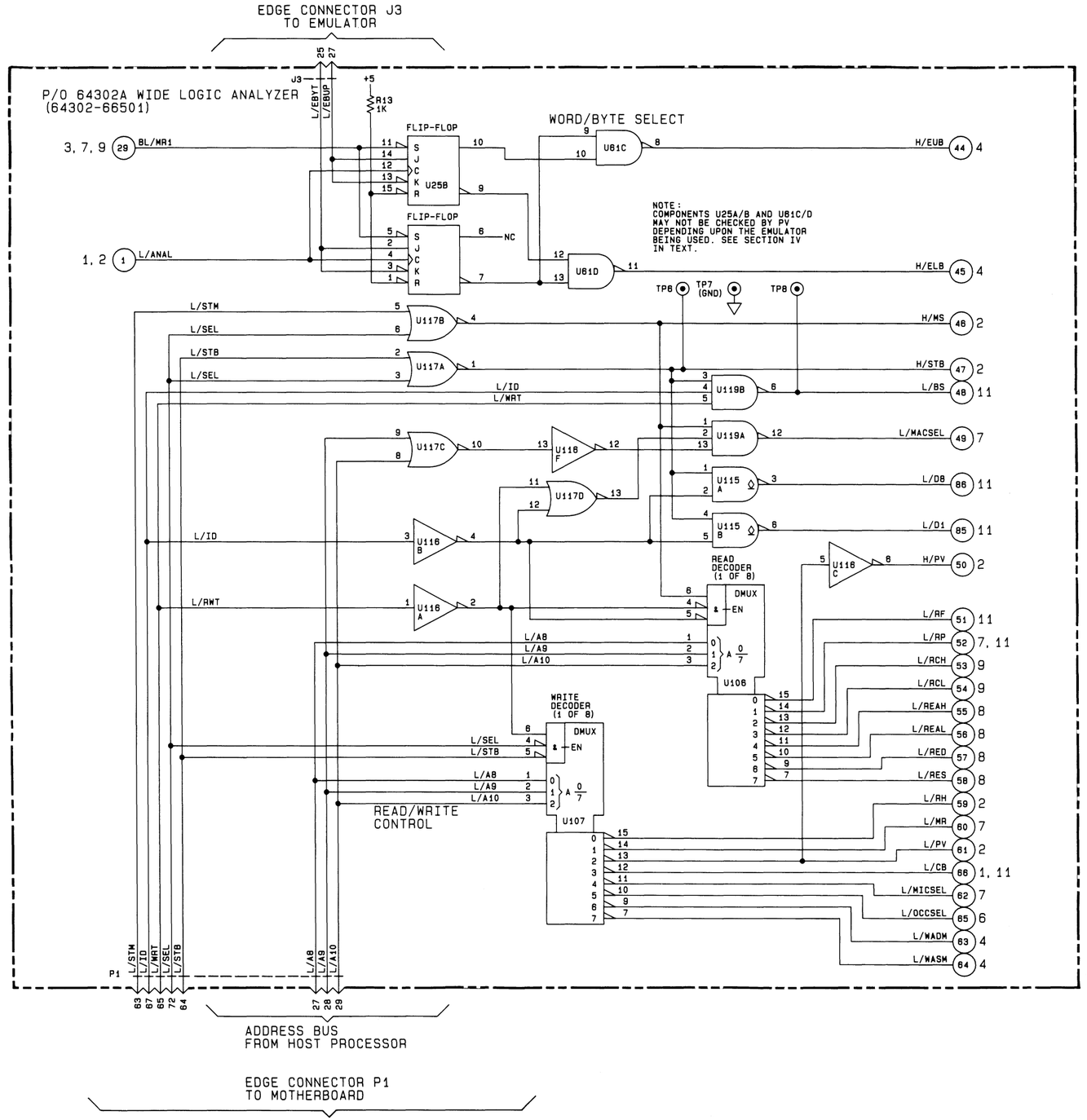


Figure 8-10.
Service Sheet 9, Time/State Counter and Storage
8-39



Component Locator



ICs ON THIS SCHEMATIC

REF. DES.	HP PART NO.	MFG. PART NO.
U25	1820-1282	SN74LS109AN
U61	1820-2684	1820-2684
U106,107	1820-1216	SN74LS138N
U115	1820-0269	SN7403N
U116	1820-1199	SN74LS04N
U117	1820-1144	SN74LS02N
U119	1820-1202	SN74LS10N

PARTS ON THIS SCHEMATIC

R13
TP6,TP7,TP8

IC POWER SUPPLY PIN CONFIGURATION

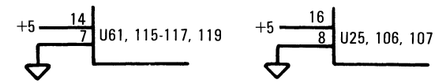
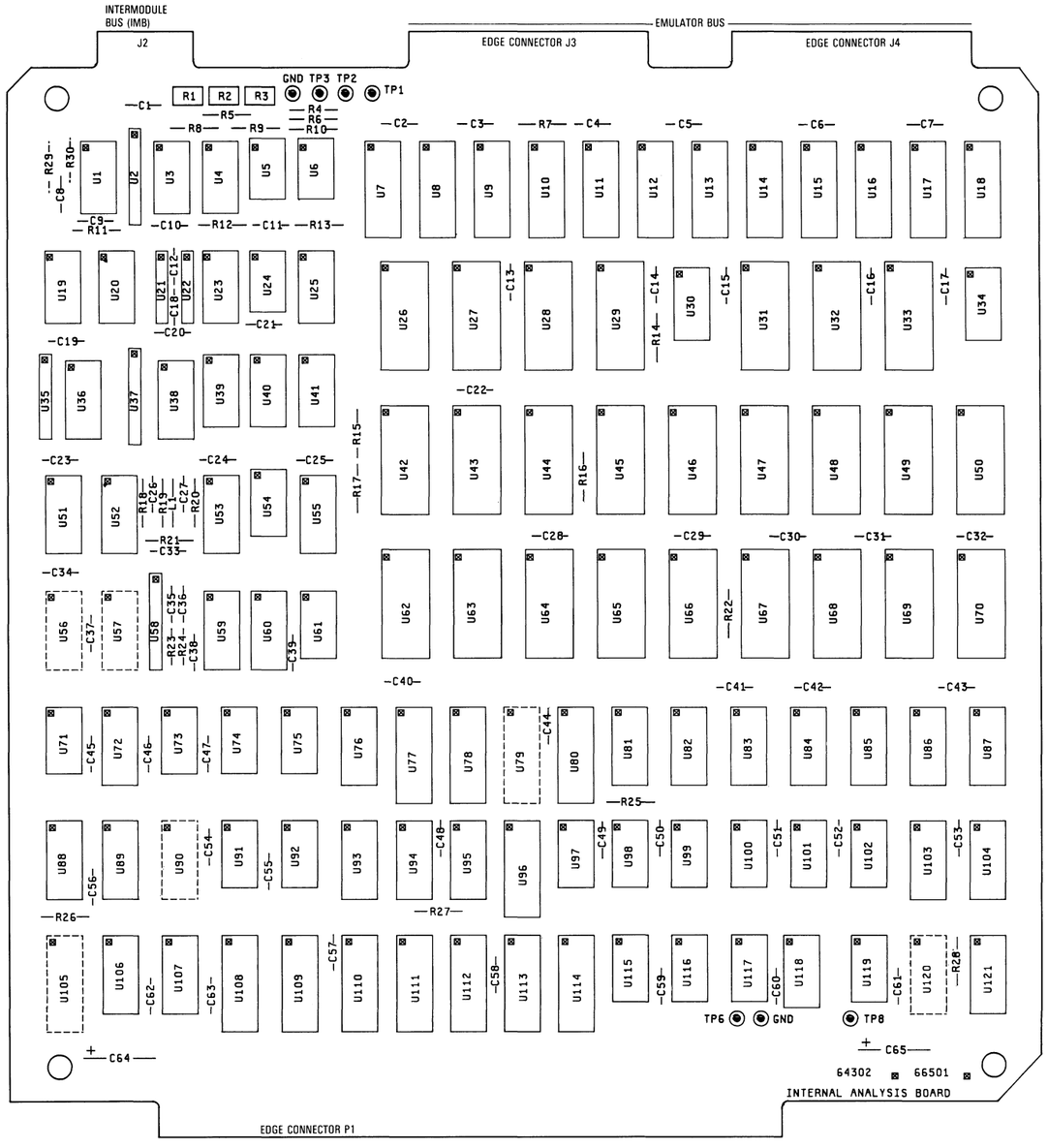
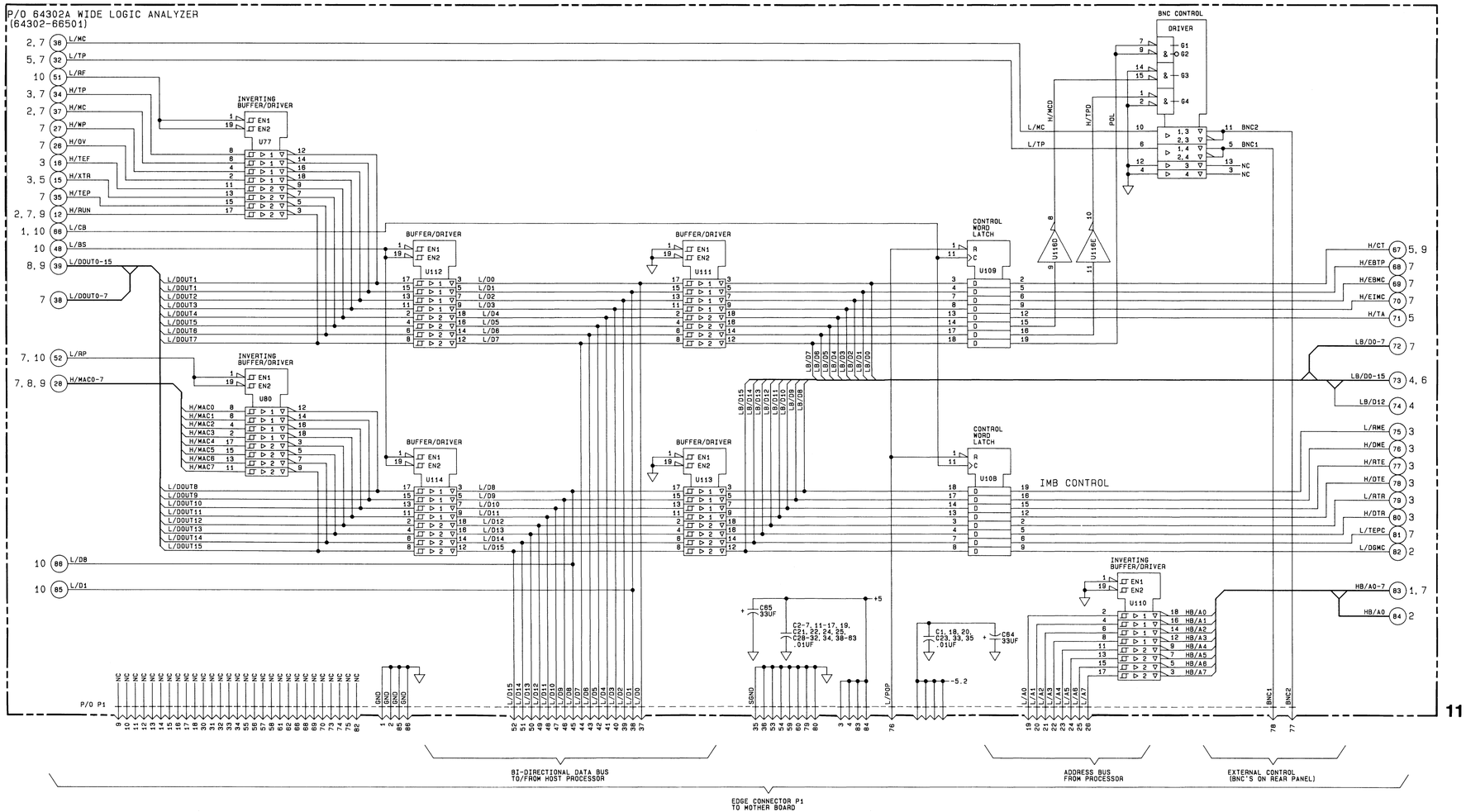


Figure 8-11.
Service Sheet 10, Read/Write Control



Component Locator



11

ICs ON THIS SCHEMATIC

REF. DES.	HP PART NO.	MFG. PART NO.
U77,80,110	1820-1917	SN74LS240N
U108,109	1820-1730	SN74LS273N
U111,112, 113,114	1820-2024	SN74LS244N
U116	1820-1199	SN74LS04N
U118	1820-0780	DS8831N

PARTS ON THIS SCHEMATIC

None

IC POWER SUPPLY PIN CONFIGURATION

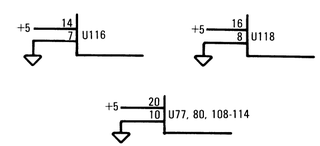


Figure 8-12.
Service Sheet 11, CPU Bus Buffer and Control Latch
8-43/(8-44 blank)

SIGNATURE TABLE: LOOP A

Loop A signatures are valid while running the Halt Mode Control Logic Tests.

Start = Positive edge of TP2 on the 64100A mainframe IO board, or TP5 on the 64110A mainframe CPU/IO board.

Stop = Negative edge of TP2 on the 64100A mainframe IO board, or TP5 on the 64110A mainframe CPU/IO board.

Clock = Negative edge of U117 pin 1 on the Wide Logic Analyzer.

Ground = Use a ground lead from probe to a ground point on the Wide Logic Analyzer.

Clock Qualifier = No qualified clocks are necessary.

ECL signatures require a 5005A Signature Analyzer:

To change from TTL to ECL --->
press the data threshold button three times.

To change from ECL to TTL --->
press the data threshold button five times.

High = indicates a solid HIGH on the node under test.
Low = indicates a solid LOW on the node under test.

All logic is positive logic.

Vh = 5099

Node	Signature		Schematic
U 1- 1	high	ECL	Sheet 3
U 1- 2	low	ECL	
U 1- 3	high	ECL	
U 1- 4	UP8U	ECL	
U 1- 5	low	ECL	
U 1- 6	low	ECL	
U 1- 7	low	ECL	
U 1- 8	low	ECL	
U 1- 9	67U8	ECL	
U 1-10	2UHP	ECL	
U 1-11	low	ECL	
U 1-12	UP8U	ECL	
U 1-13	low	ECL	
U 1-14	5099	ECL	
U 1-15	1CUF	ECL	
U 1-16	high	ECL	
U 3- 1	A749	ECL	Sheet 3
U 3- 2	366C	ECL	
U 3- 3	2UHP	ECL	
U 3- 4	low	ECL	
U 3- 8	low	ECL	
U 3-16	high	ECL	
U 4- 1	A749	ECL	Sheet 3
U 4- 2	5099	ECL	
U 4- 3	5099	ECL	
U 4- 4	366C	ECL	
U 4- 5	66U2		
U 4- 6	high		
U 4- 7	A749		
U 4- 8	low	ECL	
U 4- 9	high	ECL	
U 4-10	high		
U 4-11	7U47		
U 4-12	low	ECL	
U 4-13	2UHP	ECL	
U 4-14	5099	ECL	
U 4-15	high	ECL	
U 4-16	high	ECL	
U 5- 1	67U8		Sheet 2, 3
U 5- 2	67U8		
U 5- 3	366C		
U 5- 4	366C		
U 5- 5	5099		
U 5- 6	66U2		
U 5- 7	low		
U 5- 8	5099		
U 5- 9	5099		
U 5-10	0000		
U 5-11	5099		
U 5-12	3761		
U 5-13	high		
U 5-14	high		
U 6- 1	717U		Sheet 7, 9
U 6- 2	366C		
U 6- 4	6H23		
U 6- 5	low		
U 6- 7	low		
U 6-11	5099		
U 6-12	low		
U 6-13	high		
U 6-14	high		
U 7- 1	low		Sheet 1
U 7- 2	3F2U		
U 7- 3	F785		
U 7- 4	F85F		
U 7- 5	A291		
U 7- 6	U246		
U 7- 7	1193		
U 7- 8	7422		
U 7- 9	CA6U		
U 7-10	low		
U 7-11	PAU6		
U 7-12	24CC		
U 7-13	410A		
U 7-14	A2HU		
U 7-15	U208		
U 7-16	98F5		
U 7-17	971F		
U 7-18	6FC6		
U 7-19	low		
U 7-20	high		
U 8- 1	high		Sheet 1
U 8- 2	F785		
U 8- 5	A291		
U 8- 6	1193		
U 8- 9	CA6U		
U 8-10	low		
U 8-11	high		
U 8-12	24CC		
U 8-15	A2HU		
U 8-16	98F5		
U 8-19	6FC6		
U 8-20	high		
U 9- 1	low		Sheet 1
U 9- 2	3F2U		
U 9- 3	F785		
U 9- 4	F85F		
U 9- 5	A291		
U 9- 6	U246		
U 9- 7	1193		
U 9- 8	7422		
U 9- 9	CA6U		
U 9-10	low		
U 9-11	PAU6		
U 9-12	24CC		
U 9-13	410A		
U 9-14	A2HU		
U 9-15	U208		
U 9-16	98F5		
U 9-17	971F		
U 9-18	6FC6		
U 9-19	low		
U 9-20	high		
U 10- 1	high		Sheet 1
U 10- 2	F785		
U 10- 5	A291		
U 10- 6	1193		
U 10- 9	CA6U		
U 10-10	low		
U 10-11	high		
U 10-12	24CC		
U 10-15	A2HU		
U 10-16	98F5		
U 10-19	6FC6		
U 10-20	high		
U 11- 1	low		Sheet 1
U 11- 2	3F2U		
U 11- 3	F785		

Signature Analysis Loop A

U 11- 4	F85F		
U 11- 5	A291		
U 11- 6	U246		
U 11- 7	1193		
U 11- 8	7422		
U 11- 9	CA6U		
U 11-10	low		
U 11-11	PAU6		
U 11-12	24CC		
U 11-13	410A		
U 11-14	A2HU		
U 11-15	U208		
U 11-16	98F5		
U 11-17	971F		
U 11-18	6FC6		
U 11-19	low		
U 11-20	high		
U 12- 1	high	Sheet 1	
U 12- 2	F785		
U 12- 5	A291		
U 12- 6	1193		
U 12- 9	CA6U		
U 12-10	low		
U 12-11	high		
U 12-12	24CC		
U 12-15	A2HU		
U 12-16	98F5		
U 12-19	6FC6		
U 12-20	high		
U 13- 1	low	Sheet 1	
U 13- 2	3F2U		
U 13- 3	F785		
U 13- 4	F85F		
U 13- 5	A291		
U 13- 6	U246		
U 13- 7	1193		
U 13- 8	7422		
U 13- 9	CA6U		
U 13-10	low		
U 13-11	PAU6		
U 13-12	24CC		
U 13-13	410A		
U 13-14	A2HU		
U 13-15	U208		
U 13-16	98F5		
U 13-17	971F		
U 13-18	6FC6		
U 13-19	low		
U 13-20	high		
U 14- 1	high	Sheet 1	
U 14- 2	F785		
U 14- 5	A291		
U 14- 6	1193		
U 14- 9	CA6U		
U 14-10	low		
U 14-11	high		
U 14-12	24CC		
U 14-15	A2HU		
U 14-16	98F5		
U 14-19	6FC6		
U 14-20	high		
U 15- 1	low	Sheet 1	
U 15- 2	3F2U		
U 15- 3	F785		
U 15- 4	F85F		
U 15- 5	A291		
U 15- 6	U246		
U 15- 7	1193		
U 15- 8	7422		
U 15- 9	CA6U		
U 15-10	low		
U 15-11	PAU6		
U 15-12	24CC		
U 15-13	410A		
U 15-14	A2HU		
U 15-15	U208		
U 15-16	98F5		
U 15-17	971F		
U 15-18	6FC6		
U 15-19	low		
U 15-20	high		
U 16- 1	high	Sheet 1	
U 16- 2	F785		
U 16- 5	A291		
U 16- 6	1193		
U 16- 9	CA6U		
U 16-10	low		
U 16-11	high		
U 16-12	24CC		
U 16-15	A2HU		
U 16-16	98F5		
U 16-19	6FC6		
U 16-20	high		
U 17- 1	low	Sheet 1	
U 17- 2	3F2U		
U 17- 3	F785		
U 17- 4	F85F		
U 17- 5	A291		
U 17- 6	U246		
U 17- 7	1193		
U 17- 8	7422		
U 17- 9	CA6U		
U 17-10	low		
U 17-11	PAU6		
U 17-12	24CC		
U 17-13	410A		
U 17-14	A2HU		
U 17-15	U208		
U 17-16	98F5		
U 17-17	971F		
U 17-18	6FC6		
U 17-19	low		
U 17-20	high		
U 18- 1	high	Sheet 1	
U 18- 2	F785		
U 18- 5	A291		
U 18- 6	1193		
U 18- 9	CA6U		
U 18-10	low		
U 18-11	high		
U 18-12	24CC		
U 18-15	A2HU		
U 18-16	98F5		
U 18-19	6FC6		
U 18-20	high		
U 19- 1	5099	ECL	Sheet 2, 3
U 19- 2	5099	ECL	
U 19- 3	high	ECL	
U 19- 4	high		
U 19- 5	high		
U 19- 7	5099	ECL	
U 19- 8	low	ECL	
U 19- 9	high	ECL	
U 19-10	5099	ECL	
U 19-11	1CUF	ECL	
U 19-12	1CUF		
U 19-13	66U2		
U 19-14	366C	ECL	
U 19-15	5099	ECL	
U 19-16	high	ECL	
U 20- 1	high	ECL	Sheet 2
U 20- 2	5099	ECL	
U 20- 3	5099	ECL	
U 20- 4	low	ECL	
U 20- 5	0000	ECL	
U 20- 6	low	ECL	
U 20- 7	low	ECL	
U 20- 8	low	ECL	
U 20- 9	0000	ECL	
U 20-10	low	ECL	
U 20-11	low	ECL	
U 20-12	0000	ECL	
U 20-13	low	ECL	
U 20-14	0000	ECL	
U 20-15	5C99	ECL	
U 20-16	high	ECL	
U 23- 1	high	ECL	Sheet 2
U 23- 2	0000	ECL	
U 23- 4	5099	ECL	
U 23- 5	0000	ECL	
U 23- 6	0000	ECL	
U 23- 7	5099	ECL	
U 23- 8	low	ECL	
U 23-12	low	ECL	
U 23-13	5099	ECL	
U 23-14	high	ECL	
U 23-15	0000	ECL	
U 23-16	high	ECL	
U 24- 1	0000		Sheet 2, 3
U 24- 2	5099		
U 24- 3	PHH9		
U 24- 4	low		
U 24- 5	9588		
U 24- 6	high		
U 24- 7	low		
U 24- 8	66U2		
U 24- 9	0636		
U 24-10	PHH9		
U 24-11	3761		
U 24-12	U7H0		
U 24-13	A749		
U 24-14	high		
U 25- 1	high		Sheet 10
U 25- 2	high		
U 25- 3	high		
U 25- 4	high		
U 25- 5	AP16		
U 25- 7	low		
U 25- 8	low		
U 25- 9	low		
U 25-10	high		
U 25-11	AP16		
U 25-12	high		
U 25-15	high		
U 25-16	high		

Signature Analysis Loop A

U 26- 1	CA6U	Sheet 4
U 26- 2	1193	
U 26- 3	A291	
U 26- 4	F785	
U 26- 5	A2HU	
U 26- 6	98F5	
U 26- 7	6FC6	
U 26- 8	low	
U 26-17	high	
U 26-18	low	
U 26-19	low	
U 26-20	UF30	
U 26-21	24CC	
U 26-22	high	
U 27- 1	CA6U	Sheet 4
U 27- 2	AA2H	
U 27- 3	A291	
U 27- 4	F785	
U 27- 5	A2HU	
U 27- 6	98F5	
U 27- 7	6FC6	
U 27- 8	low	
U 27-17	high	
U 27-18	low	
U 27-19	low	
U 27-20	UF30	
U 27-21	24CC	
U 27-22	high	
U 28- 1	CA6U	Sheet 4
U 28- 2	1193	
U 28- 3	A291	
U 28- 4	F785	
U 28- 5	A2HU	
U 28- 6	98F5	
U 28- 7	6FC6	
U 28- 8	low	
U 28- 9	59A3	
U 28-10	5099	
U 28-11	UPPF	
U 28-12	5099	
U 28-13	5U20	
U 28-14	5099	
U 28-15	F93C	
U 28-16	5099	
U 28-17	high	
U 28-18	low	
U 28-19	low	
U 28-20	405F	
U 28-21	24CC	
U 28-22	high	
U 29- 1	CA6U	Sheet 4
U 29- 2	1193	
U 29- 3	A291	
U 29- 4	F785	
U 29- 5	A2HU	
U 29- 6	98F5	
U 29- 7	6FC6	
U 29- 8	low	
U 29-17	high	
U 29-18	low	
U 29-19	low	
U 29-20	405F	
U 29-21	24CC	
U 29-22	high	
U 30- 1	A291	Sheet 4
U 30- 2	F785	
U 30- 3	low	
U 30- 4	low	
U 30- 5	low	
U 30- 7	24CC	
U 30- 8	low	
U 30- 9	A2HU	
U 30-10	98F5	
U 30-11	6FC6	
U 30-12	405F	
U 30-14	CA6U	
U 30-15	1193	
U 30-16	high	
U 31- 1	CA6U	Sheet 4
U 31- 2	1193	
U 31- 3	A291	
U 31- 4	F785	
U 31- 5	A2HU	
U 31- 6	98F5	
U 31- 7	6FC6	
U 31- 8	low	
U 31-17	high	
U 31-18	low	
U 31-19	low	
U 31-20	405F	
U 31-21	24CC	
U 31-22	high	
U 32- 1	CA6U	Sheet 4
U 32- 2	1193	
U 32- 3	A291	
U 32- 4	F785	
U 32- 5	A2HU	
U 32- 6	98F5	
U 32- 7	6FC6	
U 32- 8	low	
U 32- 9	45P0	
U 32-10	5099	
U 32-11	184U	
U 32-12	5099	
U 32-13	7845	
U 32-14	5099	
U 32-15	764H	
U 32-16	5099	
U 32-17	high	
U 32-18	low	
U 32-19	low	
U 32-20	405F	
U 32-21	24CC	
U 32-22	high	
U 33- 1	CA6U	Sheet 4
U 33- 2	1193	
U 33- 3	A291	
U 33- 4	F785	
U 33- 5	A2HU	
U 33- 6	98F5	
U 33- 7	6FC6	
U 33- 8	low	
U 33- 9	45P0	
U 33-10	5099	
U 33-11	184U	
U 33-12	5099	
U 33-13	7845	
U 33-14	5099	
U 33-15	764H	
U 33-16	5099	
U 33-17	high	
U 33-18	low	
U 33-19	low	
U 33-20	UF30	
U 33-21	24CC	
U 33-22	high	
U 34- 1	A291	Sheet 4
U 34- 2	F785	
U 34- 3	low	
U 34- 4	low	
U 34- 5	low	
U 34- 6	5099	
U 34- 7	24CC	
U 34- 8	low	
U 34- 9	A2HU	
U 34-10	98F5	
U 34-11	6FC6	
U 34-12	UF30	
U 34-13	59A3	
U 34-14	CA6U	
U 34-15	1193	
U 34-16	high	
U 36- 1	high	ECL Sheet 2
U 36- 2	high	ECL
U 36- 3	0000	ECL
U 36- 4	low	ECL
U 36- 5	0000	ECL
U 36- 6	low	ECL
U 36- 7	low	ECL
U 36- 8	low	ECL
U 36- 9	67U8	ECL
U 36-10	low	ECL
U 36-11	low	ECL
U 36-12	0000	ECL
U 36-13	low	ECL
U 36-14	0000	ECL
U 36-15	5099	ECL
U 36-16	high	ECL
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U 93-12	AA2P	
U 93-13	6293	
U 93-14	PA46	
U 93-15	low	
U 93-16	high	
U 94- 1	high	Sheet 7
U 94- 2	5099	
U 94- 7	8HC8	
U 94- 8	low	
U 94- 9	P064	

Signature Analysis Loop A

U 94-10	0000	
U 94-11	93F9	
U 94-12	2081	
U 94-13	0060	
U 94-14	4370	
U 94-15	0000	
U 94-16	high	
U 95- 1	high	Sheet 7
U 95- 2	5099	
U 95- 7	8HC8	
U 95- 8	low	
U 95- 9	P064	
U 95-10	low	
U 95-11	4H93	
U 95-12	26UH	
U 95-13	C787	
U 95-14	A62F	
U 95-15	low	
U 95-16	high	
U 96- 1	high	Sheet 4
U 96- 2	low	
U 96- 3	5099	
U 96- 4	low	
U 96- 5	5099	
U 96- 6	low	
U 96- 7	5099	
U 96- 8	low	
U 96- 9	5099	
U 96-10	low	
U 96-11	low	
U 96-12	5099	
U 96-13	low	
U 96-14	5099	
U 96-15	low	
U 96-16	5099	
U 96-17	low	
U 96-18	5099	
U 96-19	high	
U 96-20	high	
U 97- 1	5099	Sheet 5
U 97- 2	5099	
U 97- 3	5099	
U 97- 4	5099	
U 97- 5	5099	
U 97- 6	0000	
U 97- 7	low	
U 97- 8	0000	
U 97- 9	5099	
U 97-10	5099	
U 97-11	5099	
U 97-12	0000	
U 97-13	5099	
U 97-14	high	
U 98- 1	5099	Sheet 5
U 98- 2	0000	
U 98- 3	0000	
U 98- 4	5099	
U 98- 5	0000	
U 98- 6	0000	
U 98- 7	low	
U 98- 8	0000	
U 98- 9	U161	
U 98-10	A1U8	
U 98-11	0000	
U 98-12	0000	
U 98-13	5099	
U 98-14	high	
U 99- 1	5099	Sheet 5
U 99- 2	5099	
U 99- 3	5099	
U 99- 4	5099	
U 99- 5	5099	
U 99- 6	0000	
U 99- 7	low	
U 99- 8	0000	
U 99- 9	5099	
U 99-10	5099	
U 99-11	5099	
U 99-12	0000	
U 99-13	5099	
U 99-14	high	
U100- 1	5099	Sheet 5
U100- 2	5099	
U100- 3	0000	
U100- 4	0000	
U100- 5	0000	
U100- 6	5099	
U100- 7	low	
U100- 8	0000	
U100- 9	high	
U100-10	5099	
U100-11	5099	
U100-12	0000	
U100-13	5099	
U100-14	high	
U101- 1	5099	Sheet 5
U101- 2	low	
U101- 3	low	
U101- 4	5099	
U101- 5	5099	
U101- 6	5099	
U101- 7	low	
U101- 8	0000	
U101- 9	5099	
U101-10	5099	
U101-11	5099	
U101-12	5099	
U101-13	5099	
U101-14	high	
U102- 1	5099	Sheet 5
U102- 2	low	
U102- 3	low	
U102- 4	5099	
U102- 5	5099	
U102- 6	5099	
U102- 7	low	
U102- 8	0000	
U102- 9	low	
U102-10	low	
U102-11	5099	
U102-12	5099	
U102-13	5099	
U102-14	high	
U103- 1	high	Sheet 6
U103- 2	5099	
U103- 7	0000	
U103- 8	low	
U103- 9	503P	
U103-10	high	
U103-15	52P1	
U103-16	high	
U104- 1	high	Sheet 6
U104- 2	5099	
U104- 7	low	
U104- 8	low	
U104- 9	503P	
U104-10	52P1	
U104-15	5HU8	
U104-16	high	
U106- 1	UHHU	Sheet 10
U106- 2	41F2	
U106- 3	U718	
U106- 4	4853	
U106- 5	low	
U106- 6	5099	
U106- 7	ACC7	
U106- 8	low	
U106- 9	high	
U106-10	high	
U106-11	high	
U106-12	high	
U106-13	high	
U106-14	8964	
U106-15	6A80	
U106-16	high	
U107- 1	UHHU	Sheet 10
U107- 2	41F2	
U107- 3	U718	
U107- 4	0000	
U107- 5	5099	
U107- 6	4853	
U107- 7	405F	
U107- 8	low	
U107- 9	UF30	
U107-10	503P	
U107-11	P064	
U107-12	6178	
U107-13	67U8	
U107-14	AP16	
U107-15	PFU3	
U107-16	high	
U108- 1	high	Sheet 11
U108- 2	9588	
U108- 3	59A3	
U108- 4	UPPF	
U108- 5	003P	
U108- 6	3656	
U108- 7	5U20	
U108- 8	F93C	
U108- 9	U7H0	
U108-10	low	
U108-11	6178	
U108-12	2UHP	
U108-13	764H	
U108-14	7845	
U108-15	6H23	
U108-16	366C	
U108-17	184U	
U108-18	45P0	
U108-19	0636	
U108-20	high	
U110- 1	low	Sheet 11
U110- 2	F785	
U110- 3	3F2U	

Signature Analysis Loop A

U110- 4	A291	
U110- 5	F85F	
U110- 6	1193	
U110- 7	U246	
U110- 8	CA6U	
U110- 9	7422	
U110-10	low	
U110-11	24CC	
U110-12	PAU6	
U110-13	A2HU	
U110-14	410A	
U110-15	98F5	
U110-16	U208	
U110-17	6FC6	
U110-18	971F	
U110-19	low	
U110-20	high	
U116- 1	18FA	Sheet 10, 11
U116- 2	4853	
U116- 3	high	
U116- 4	low	
U116- 5	67U8	
U116- 6	3761	
U116- 7	low	
U116- 8	50A7	
U116- 9	003P	
U116-10	FHA7	
U116-11	9H3P	
U116-12	U198	
U116-13	A101	
U116-14	high	
U117- 1	5099	Sheet 10
U117- 2	5099	
U117- 3	0000	
U117- 4	5099	
U117- 5	5099	
U117- 6	0000	
U117- 7	low	
U117- 8	U718	
U117- 9	41F2	
U117-10	A101	
U117-11	4853	
U117-12	low	
U117-13	18FA	
U117-14	high	
U118- 1	FHA7	Sheet 11
U118- 2	low	
U118- 4	low	
U118- 5	0F21	
U118- 6	21P6	
U118- 7	U7H0	
U118- 8	low	
U118- 9	U7H0	
U118-10	5099	
U118-11	0F21	
U118-12	low	
U118-14	low	
U118-15	50A7	
U118-16	high	
U113- 1	low	Sheet 11
U113- 2	59A3	
U113- 3	45P0	
U113- 4	UPPF	
U113- 5	184U	
U113- 6	5U20	
U113- 7	7845	
U113- 8	F93C	
U113- 9	764H	
U113-10	low	
U113-11	764H	
U113-12	F93C	
U113-13	7845	
U113-14	5U20	
U113-15	184U	
U113-16	UPPF	
U113-17	45P0	
U113-18	59A3	
U113-19	low	
U113-20	high	
U114- 1	4853	Sheet 11
U114- 2	C0U7	
U114- 3	45P0	
U114- 4	U49H	
U114- 5	184U	
U114- 6	90F3	
U114- 7	7845	
U114- 8	4A18	
U114- 9	764H	
U114-10	low	
U114-11	7H8P	
U114-12	F93C	
U114-13	515F	
U114-14	5U20	
U114-15	H964	
U114-16	UPPF	
U114-17	09A0	
U114-18	59A3	
U114-19	4853	
U114-20	high	
U115- 1	5099	Sheet 7, 10
U115- 2	low	
U115- 3	45P0	
U115- 4	5099	
U115- 5	low	
U115- 7	low	
U115- 8	5099	
U115- 9	0000	
U115-10	0000	
U115-14	high	
U119- 1	5099	Sheet 7, 10
U119- 2	18FA	
U119- 3	5099	
U119- 4	high	
U119- 5	18FA	
U119- 6	4853	
U119- 7	low	
U119- 8	high	
U119- 9	low	
U119-10	low	
U119-11	low	
U119-12	ACC7	
U119-13	U198	
U119-14	high	
U121- 1	high	Sheet 6
U121- 2	5099	
U121- 3	45P0	
U121- 4	184U	
U121- 5	7845	
U121- 6	764H	
U121- 7	0000	
U121- 8	low	
U121- 9	503P	
U121-10	5HU8	
U121-15	5H09	
U121-16	high	

SIGNATURE TABLE: LOOP B

Loop B signatures are valid while running the Halt Mode Storage RAM Tests.

Start = Positive edge of TP2 on the 64100A mainframe IO board, or TP5 on the 64110A mainframe CPU/IO board.

Stop = Negative edge of TP2 on the 64100A mainframe IO board, or TP5 on the 64110A mainframe CPU/IO board.

Clock = Negative edge of U117 pin 1 on the Wide Logic Analyzer.

Ground = Use a ground lead from probe to a ground point on the Wide Logic Analyzer.

Clock Qualifier = No qualified clocks are necessary.

ECL signatures require a 5005A Signature Analyzer:

To change from TTL to ECL --->
press the data threshold button three times.

To change from ECL to TTL --->
press the data threshold button five times.

High = indicates a solid HIGH on the node under test.
Low = indicates a solid LOW on the node under test.

All logic is positive logic.

Vh = 87UU

Node	Signature		Schematic
U 1- 1	high	ECL	Sheet 3
U 1- 2	low	ECL	
U 1- 3	high	ECL	
U 1- 4	5P33	ECL	
U 1- 5	low	ECL	
U 1- 6	low	ECL	
U 1- 7	low	ECL	
U 1- 8	low	ECL	
U 1- 9	38F6	ECL	
U 1-10	low	ECL	
U 1-11	low	ECL	
U 1-12	5P33	ECL	
U 1-13	low	ECL	
U 1-14	87UU	ECL	
U 1-15	C064	ECL	
U 1-16	high	ECL	
U 3- 1	low	ECL	Sheet 3
U 3- 2	low	ECL	
U 3- 3	low	ECL	
U 3- 4	low	ECL	
U 3- 8	low	ECL	
U 3-16	high	ECL	
U 4- 1	low	ECL	Sheet 3
U 4- 2	high	ECL	
U 4- 3	high	ECL	
U 4- 4	low	ECL	
U 4- 5	high		
U 4- 6	high		
U 4- 7	low		
U 4- 8	low	ECL	
U 4- 9	high	ECL	
U 4-10	high		
U 4-11	high		
U 4-12	low	ECL	
U 4-13	low	ECL	
U 4-14	high	ECL	
U 4-15	high	ECL	
U 4-16	high	ECL	
U 5- 1	38F6		Sheet 2, 3
U 5- 2	38F6		
U 5- 3	low		
U 5- 4	low		
U 5- 5	high		
U 5- 6	high		
U 5- 7	low		
U 5- 8	high		
U 5- 9	high		
U 5-10	low		
U 5-11	87UU		
U 5-12	CU39		
U 5-13	high		
U 5-14	high		
U 6- 1	low		Sheet 7, 9
U 6- 2	low		
U 6- 4	low		
U 6- 5	low		
U 6- 7	low		
U 6-11	high		
U 6-12	low		
U 6-13	high		
U 6-14	high		
U 7- 1	low		Sheet 1
U 7- 2	4865		
U 7- 3	C25U		
U 7- 4	4CF0		
U 7- 5	83C9		
U 7- 6	U42U		
U 7- 7	P1A0		
U 7- 8	91P9		
U 7- 9	3CAU		
U 7-10	low		
U 7-11	CF50		
U 7-12	1616		
U 7-13	665U		
U 7-14	73H0		
U 7-15	0446		
U 7-16	FF3U		
U 7-17	35A0		
U 7-18	FU9A		
U 7-19	low		
U 7-20	high		
U 8- 1	high		Sheet 1
U 8- 2	C25U		
U 8- 5	83C9		
U 8- 6	P1A0		
U 8- 9	3CAU		
U 8-10	low		
U 8-11	high		
U 8-12	1616		
U 8-15	73H0		
U 8-16	FF3U		
U 8-19	FU9A		
U 8-20	high		
U 9- 1	low		Sheet 1
U 9- 2	4865		
U 9- 3	C25U		
U 9- 4	4CF0		
U 9- 5	83C9		
U 9- 6	U42U		
U 9- 7	P1A0		
U 9- 8	91P9		
U 9- 9	3CAU		
U 9-10	low		
U 9-11	CF50		
U 9-12	1616		
U 9-13	665U		
U 9-14	73H0		
U 9-15	0446		
U 9-16	FF3U		
U 9-17	35A0		
U 9-18	FU9A		
U 9-19	low		
U 9-20	high		
U 10- 1	high		Sheet 1
U 10- 2	C25U		
U 10- 5	83C9		
U 10- 6	P1A0		
U 10- 9	3CAU		
U 10-10	low		
U 10-11	high		
U 10-12	1616		
U 10-15	73H0		
U 10-16	FF3U		
U 10-19	FU9A		
U 10-20	high		

U 11- 1	low		Sheet 1
U 11- 2	4865		
U 11- 3	C25U		
U 11- 4	4CF0		
U 11- 5	83C9		
U 11- 6	U42U		
U 11- 7	P1A0		
U 11- 8	91P9		
U 11- 9	3CAU		
U 11-10	low		
U 11-11	CF50		
U 11-12	1616		
U 11-13	665U		
U 11-14	73H0		
U 11-15	0446		
U 11-16	FF3U		
U 11-17	35A0		
U 11-18	FU9A		
U 11-19	low		
U 11-20	high		
U 12- 1	high		Sheet 1
U 12- 2	C25U		
U 12- 5	83C9		
U 12- 6	P1A0		
U 12- 9	3CAU		
U 12-10	low		
U 12-11	high		
U 12-12	1616		
U 12-15	73H0		
U 12-16	FF3U		
U 12-19	FU9A		
U 12-20	high		
U 13- 1	low		Sheet 1
U 13- 2	4865		
U 13- 3	C25U		
U 13- 4	4CF0		
U 13- 5	83C9		
U 13- 6	U42U		
U 13- 7	P1A0		
U 13- 8	91P9		
U 13- 9	3CAU		
U 13-10	low		
U 13-11	CF50		
U 13-12	1616		
U 13-13	665U		
U 13-14	73H0		
U 13-15	0446		
U 13-16	FF3U		
U 13-17	35A0		
U 13-18	FU9A		
U 13-19	low		
U 13-20	high		
U 14- 1	high		Sheet 1
U 14- 2	C25U		
U 14- 5	83C9		
U 14- 6	P1A0		
U 14- 9	3CAU		
U 14-10	low		
U 14-11	high		
U 14-12	1616		
U 14-15	73H0		
U 14-16	FF3U		
U 14-19	FU9A		
U 14-20	high		
U 15- 1	low		Sheet 1
U 15- 2	4865		
U 15- 3	C25U		
U 15- 4	4CF0		
U 15- 5	83C9		
U 15- 6	U42U		
U 15- 7	P1A0		
U 15- 8	91P9		
U 15- 9	3CAU		
U 15-10	low		
U 15-11	CF50		
U 15-12	1616		
U 15-13	665U		
U 15-14	73H0		
U 15-15	0446		
U 15-16	FF3U		
U 15-17	35A0		
U 15-18	FU9A		
U 15-19	low		
U 15-20	high		
U 16- 1	high		Sheet 1
U 16- 2	C25U		
U 16- 5	83C9		
U 16- 6	P1A0		
U 16- 9	3CAU		
U 16-10	low		
U 16-11	high		
U 16-12	1616		
U 16-15	73H0		
U 16-16	FF3U		
U 16-19	FU9A		
U 16-20	high		
U 17- 1	low		Sheet 1
U 17- 2	4865		
U 17- 3	C25U		
U 17- 4	4CF0		
U 17- 5	83C9		
U 17- 6	U42U		
U 17- 7	P1A0		
U 17- 8	91P9		
U 17- 9	3CAU		
U 17-10	low		
U 17-11	CF50		
U 17-12	1616		
U 17-13	665U		
U 17-14	73H0		
U 17-15	0446		
U 17-16	FF3U		
U 17-17	35A0		
U 17-18	FU9A		
U 17-19	low		
U 17-20	high		
U 18- 1	high		Sheet 1
U 18- 2	C25U		
U 18- 5	83C9		
U 18- 6	P1A0		
U 18- 9	3CAU		
U 18-10	low		
U 18-11	high		
U 18-12	1616		
U 18-15	73H0		
U 18-16	FF3U		
U 18-19	FU9A		
U 18-20	high		
U 19- 1	0000	ECL	Sheet 2, 3
U 19- 2	0000	ECL	
U 19- 3	high	ECL	
U 19- 4	high		
U 19- 5	high		
U 19- 7	0000	ECL	
U 19- 8	low	ECL	
U 19- 9	high	ECL	
U 19-10	0000	ECL	
U 19-11	C064	ECL	
U 19-12	C064		
U 19-13	high		
U 19-14	low	ECL	
U 19-15	0000	ECL	
U 19-16	high	ECL	
U 20- 1	high	ECL	Sheet 2
U 20- 2	87UU	ECL	
U 20- 3	0000	ECL	
U 20- 4	low	ECL	
U 20- 5	0000	ECL	
U 20- 6	low	ECL	
U 20- 7	low	ECL	
U 20- 8	low	ECL	
U 20- 9	0000	ECL	
U 20-10	low	ECL	
U 20-11	low	ECL	
U 20-12	0000	ECL	
U 20-13	low	ECL	
U 20-14	0000	ECL	
U 20-15	87UU	ECL	
U 20-16	high	ECL	
U 23- 1	high	ECL	Sheet 2
U 23- 2	0000	ECL	
U 23- 4	87UU	ECL	
U 23- 5	0000	ECL	
U 23- 6	0000	ECL	
U 23- 7	87UU	ECL	
U 23- 8	low	ECL	
U 23-12	low	ECL	
U 23-13	87UU	ECL	
U 23-14	high	ECL	
U 23-15	0000	ECL	
U 23-16	high	ECL	
U 24- 1	low		Sheet 2, 3
U 24- 2	high		
U 24- 3	low		
U 24- 4	low		
U 24- 5	high		
U 24- 6	high		
U 24- 7	low		
U 24- 8	high		
U 24- 9	high		
U 24-10	low		
U 24-11	CU39		
U 24-12	high		
U 24-13	low		
U 24-14	high		
U 25- 1	high		Sheet 10
U 25- 2	high		
U 25- 3	high		
U 25- 4	high		

Signature Analysis Loop B

U 25- 5	H9FF	
U 25- 7	low	
U 25- 8	low	
U 25- 9	low	
U 25-10	high	
U 25-11	H9FF	
U 25-12	high	
U 25-15	high	
U 25-16	high	
U 26- 1	3CAU	Sheet 4
U 26- 2	P1A0	
U 26- 3	83C9	
U 26- 4	C25U	
U 26- 5	73H0	
U 26- 6	FF3U	
U 26- 7	FU9A	
U 26- 8	low	
U 26- 9	F904	
U 26-10	0000	
U 26-11	425U	
U 26-12	0000	
U 26-13	729A	
U 26-14	0000	
U 26-15	38H6	
U 26-16	0000	
U 26-17	high	
U 26-18	low	
U 26-19	low	
U 26-20	FC20	
U 26-21	1616	
U 26-22	high	
U 27- 1	3CAU	Sheet 4
U 27- 2	P1A0	
U 27- 3	83C9	
U 27- 4	C25U	
U 27- 5	73H0	
U 27- 6	FF3U	
U 27- 7	FU9A	
U 27- 8	low	
U 27- 9	8HHP	
U 27-10	0000	
U 27-11	C669	
U 27-12	0000	
U 27-13	98HH	
U 27-14	0000	
U 27-15	P9CF	
U 27-16	0000	
U 27-17	high	
U 27-18	low	
U 27-19	low	
U 27-20	FC20	
U 27-21	1616	
U 27-22	high	
U 28- 1	3CAU	Sheet 4
U 28- 2	P1A0	
U 28- 3	83C9	
U 28- 4	C25U	
U 28- 5	73H0	
U 28- 6	FF3U	
U 28- 7	FU9A	
U 28- 8	low	
U 28-10	0000	
U 28-11	3FU8	
U 28-12	0000	
U 28-13	1839	
U 28-14	0000	
U 28-15	767C	
U 28-16	0000	
U 28-17	high	
U 28-18	low	
U 28-19	low	
U 28-20	HHP2	
U 28-21	1616	
U 28-22	high	
U 29- 1	3CAU	Sheet 4
U 29- 2	P1A0	
U 29- 3	83C9	
U 29- 4	C25U	
U 29- 5	73H0	
U 29- 6	FF3U	
U 29- 7	FU9A	
U 29- 8	low	
U 29- 9	F904	
U 29-10	0000	
U 29-11	425U	
U 29-12	0000	
U 29-13	729A	
U 29-14	0000	
U 29-15	38H6	
U 29-16	0000	
U 29-17	high	
U 29-18	low	
U 29-19	low	
U 29-20	HHP2	
U 29-21	1616	
U 29-22	high	
U 30- 1	83C9	Sheet 4
U 30- 2	C25U	
U 30- 3	low	
U 30- 4	low	
U 30- 5	low	
U 30- 6	low	
U 30- 7	1616	
U 30- 8	low	
U 30- 9	73H0	
U 30-10	FF3U	
U 30-11	FU9A	
U 30-12	HHP2	
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U 30-14	3CAU	
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U 78-14	26U7	
U 78-15	high	
U 78-16	118F	
U 78-17	high	
U 78-18	P404	
U 78-19	high	
U 78-20	high	
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U 80- 3	F77H	
U 80- 4	3H1P	
U 80- 5	P7P6	
U 80- 6	9625	
U 80- 7	3478	
U 80- 8	8217	
U 80- 9	3725	
U 80-10	low	
U 80-11	8F7C	
U 80-12	F032	
U 80-13	5993	
U 80-14	3A11	
U 80-15	2ACU	
U 80-16	H816	
U 80-17	7U8A	
U 80-18	59C2	
U 80-19	high	
U 80-20	high	
U 81- 1	H9FF	Sheet 9
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U 81- 7	high	
U 81- 8	low	
U 81- 9	high	
U 81-10	0000	
U 81-11	low	
U 81-12	low	
U 81-13	low	
U 81-14	low	
U 81-15	low	
U 81-16	high	
U 82- 1	H9FF	Sheet 9
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U 82- 7	low	
U 82- 8	low	
U 82- 9	high	
U 82-10	high	
U 82-11	low	
U 82-12	low	
U 82-13	low	
U 82-14	low	
U 82-15	low	
U 82-16	high	
U 83- 1	H9FF	Sheet 9
U 83- 2	38F6	
U 83- 7	low	
U 83- 8	low	

U 83- 9	high	
U 83-10	low	
U 83-11	low	
U 83-12	low	
U 83-13	low	
U 83-14	low	
U 83-15	low	
U 83-16	high	
U 84- 1	H9FF	Sheet 9
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U 84- 7	low	
U 84- 8	low	
U 84- 9	high	
U 84-10	low	
U 84-11	low	
U 84-12	low	
U 84-13	low	
U 84-14	low	
U 84-15	low	
U 84-16	high	
U 85- 1	H9FF	Sheet 9
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U 85- 7	low	
U 85- 8	low	
U 85- 9	high	
U 85-10	low	
U 85-11	low	
U 85-12	low	
U 85-13	low	
U 85-14	low	
U 85-15	low	
U 85-16	high	
U 86- 1	H9FF	Sheet 9
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U 86- 7	low	
U 86- 8	low	
U 86- 9	high	
U 86-10	low	
U 86-11	low	
U 86-12	low	
U 86-13	low	
U 86-14	low	
U 86-15	low	
U 86-16	high	
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U 87- 5	1839	
U 87- 6	767C	
U 87- 7	low	
U 87- 8	low	
U 87- 9	C1HU	
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U 87-15	high	
U 87-16	high	
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U 88- 5	H9FF	
U 88- 6	high	
U 88- 7	low	
U 88- 8	low	
U 88- 9	low	
U 88-11	H9FF	
U 88-12	38F6	
U 88-13	high	
U 88-14	low	
U 88-15	high	
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U 89- 7	low	
U 89- 8	low	
U 89-10	low	
U 89-11	high	
U 89-12	38F6	
U 89-13	high	
U 89-14	low	
U 89-15	H9FF	
U 89-16	high	
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U 91- 3	low	
U 91- 4	low	
U 91- 5	87UU	
U 91- 6	high	
U 91- 7	low	
U 91- 8	low	
U 91- 9	high	
U 91-10	low	
U 91-11	low	
U 91-12	low	
U 91-13	high	
U 91-14	high	
U 92- 1	high	Sheet 5, 9
U 92- 2	low	
U 92- 3	low	
U 92- 4	high	
U 92- 5	87UU	
U 92- 6	0000	
U 92- 7	low	
U 92- 8	low	
U 92- 9	high	
U 92-10	low	
U 92-11	high	
U 92-12	0000	
U 92-13	87UU	
U 92-14	high	
U 93- 1	H9FF	Sheet 7
U 93- 2	87UU	
U 93- 3	91P9	
U 93- 4	U42U	
U 93- 5	4CF0	
U 93- 6	4865	
U 93- 7	0000	
U 93- 8	low	
U 93- 9	CAA8	
U 93-10	low	
U 93-11	8F7C	
U 93-12	5993	
U 93-13	2ACU	
U 93-14	7U8A	
U 93-15	low	
U 93-16	high	
U 94- 1	high	Sheet 7
U 94- 2	87UU	
U 94- 3	F904	
U 94- 4	425U	
U 94- 5	729A	
U 94- 6	38H6	
U 94- 7	0000	
U 94- 8	low	
U 94- 9	PCCU	
U 94-10	low	
U 94-11	high	
U 94-12	high	
U 94-13	high	
U 94-14	high	
U 94-15	low	
U 94-16	high	
U 95- 1	high	Sheet 7
U 95- 2	87UU	
U 95- 3	8HHP	
U 95- 4	C669	
U 95- 5	98HH	
U 95- 6	P9CF	
U 95- 7	0000	
U 95- 8	low	
U 95- 9	PCCU	
U 95-10	low	
U 95-11	high	
U 95-12	high	
U 95-13	high	
U 95-14	high	
U 95-15	low	
U 95-16	high	
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U 96- 3	0000	
U 96- 4	low	
U 96- 5	0000	
U 96- 6	low	
U 96- 7	0000	
U 96- 8	low	
U 96- 9	0000	
U 96-10	low	
U 96-11	low	
U 96-12	0000	
U 96-13	low	
U 96-14	0000	
U 96-15	low	
U 96-16	0000	
U 96-17	low	
U 96-18	0000	
U 96-19	high	
U 96-20	high	
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U 97- 3	0000	
U 97- 4	0000	
U 97- 5	0000	
U 97- 6	87UU	
U 97- 7	low	
U 97- 8	87UU	
U 97- 9	0000	
U 97-10	0000	

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U 97-12	87UU	
U 97-13	0000	
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U 98- 1	0000	Sheet 5
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U 98- 4	0000	
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U 98- 8	87UU	
U 98- 9	low	
U 98-10	0000	
U 98-11	87UU	
U 98-12	87UU	
U 98-13	0000	
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U 99- 7	low	
U 99- 8	87UU	
U 99- 9	0000	
U 99-10	0000	
U 99-11	0000	
U 99-12	87UU	
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U100- 6	4FHU	
U100- 7	low	
U100- 8	high	
U100- 9	low	
U100-10	0000	
U100-11	0000	
U100-12	87UU	
U100-13	0000	
U100-14	high	

U101- 1	0000	Sheet 5
U101- 2	low	
U101- 3	low	
U101- 4	0000	
U101- 5	0000	
U101- 6	0000	
U101- 7	low	
U101- 8	FC20	
U101- 9	low	
U101-10	0000	
U101-11	0000	
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U101-13	0000	
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U102- 4	low	
U102- 5	0000	
U102- 6	low	
U102- 7	low	
U102- 8	high	
U102- 9	low	
U102-10	low	
U102-11	0000	
U102-12	0000	
U102-13	0000	
U102-14	high	
U103- 1	high	Sheet 6
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U103- 3	F904	
U103- 4	425U	
U103- 5	729A	
U103- 6	38H6	
U103- 7	low	
U103- 8	low	
U103- 9	C1HU	
U103-10	high	
U103-15	high	
U103-16	high	
U104- 1	high	Sheet 6
U104- 2	87UU	
U104- 3	8HHP	
U104- 4	C669	
U104- 5	98HH	
U104- 6	P9CF	

U104- 7	low	
U104- 8	low	
U104- 9	C1HU	
U104-10	high	
U104-15	high	
U104-16	high	
U106- 1	F78U	Sheet 10
U106- 2	4A2C	
U106- 3	2A14	
U106- 4	7PA8	
U106- 5	low	
U106- 6	87UU	
U106- 7	1C3A	
U106- 8	low	
U106- 9	120C	
U106-10	FH05	
U106-11	A282	
U106-12	1541	
U106-13	4PA0	
U106-14	high	
U106-15	43UU	
U106-16	high	
U107- 1	F78U	Sheet 10
U107- 2	4A2C	
U107- 3	2A14	
U107- 4	0000	
U107- 5	87UU	
U107- 6	7PA8	
U107- 7	HHP2	
U107- 8	low	
U107- 9	FC20	
U107-10	C1HU	
U107-11	PCCU	
U107-12	36UU	
U107-13	38F6	
U107-14	H9FF	
U107-15	P5UU	
U107-16	high	
U108- 1	high	Sheet 11
U108- 2	high	
U108- 4	3FU8	
U108- 5	low	
U108- 6	high	
U108- 7	1839	
U108- 8	767C	
U108- 9	high	
U108-10	low	

U108-11	36UU	
U108-12	low	
U108-13	2AC4	
U108-14	9H9F	
U108-15	low	
U108-16	low	
U108-17	842F	
U108-18	3102	
U108-19	high	
U108-20	high	
U109- 1	high	Sheet 11
U109- 2	low	
U109- 3	F904	
U109- 4	425U	
U109- 5	low	
U109- 6	low	
U109- 7	729A	
U109- 8	38H6	
U109- 9	low	
U109-10	low	
U109-11	36UU	
U109-12	low	
U109-13	8HHP	
U109-14	C669	
U109-15	low	
U109-16	low	
U109-17	98HH	
U109-18	P9CF	
U109-19	high	
U109-20	high	
U110- 1	low	Sheet 11
U110- 2	C25U	
U110- 3	4865	
U110- 4	83C9	
U110- 5	4CF0	
U110- 6	P1A0	
U110- 7	U42U	
U110- 8	3CAU	
U110- 9	91P9	
U110-10	low	
U110-11	1616	
U110-12	CF50	
U110-13	73H0	
U110-14	665U	
U110-15	FF3U	
U110-16	0446	
U110-17	FU9A	
U110-18	35A0	

U110-19	low	
U110-20	high	
U111- 1	low	Sheet 11
U111- 2	8HHP	
U111- 3	F904	
U111- 4	C669	
U111- 5	425U	
U111- 6	98HH	
U111- 7	729A	
U111- 8	P9CF	
U111- 9	38H6	
U111-10	low	
U111-11	38H6	
U111-12	P9CF	
U111-13	729A	
U111-14	98HH	
U111-15	425U	
U111-16	C669	
U111-17	F904	
U111-18	8HHP	
U111-19	low	
U111-20	high	
U112- 1	7PA8	Sheet 11
U112- 2	3564	
U112- 3	F904	
U112- 4	61H3	
U112- 5	425U	
U112- 6	A88F	
U112- 7	729A	
U112- 8	3H0U	
U112- 9	38H6	
U112-10	low	
U112-11	P404	
U112-12	P9CF	
U112-13	118F	
U112-14	98HH	
U112-15	26U7	
U112-16	C669	
U112-17	8H81	
U112-18	8HHP	
U112-19	7PA8	
U112-20	high	
U113- 1	low	Sheet 11
U113- 3	3102	
U113- 4	3FU8	
U113- 5	842F	
U113- 6	1839	
U113- 7	9H9F	
U113- 8	767C	
U113- 9	2AC4	
U113-10	low	
U113-11	2AC4	
U113-12	767C	
U113-13	9H9F	
U113-14	1839	
U113-15	842F	
U113-16	3FU8	
U113-17	3102	
U113-19	low	
U113-20	high	
U114- 1	7PA8	Sheet 11
U114- 2	F77H	
U114- 3	3102	
U114- 4	P7P6	
U114- 5	842F	
U114- 6	3478	
U114- 7	9H9F	
U114- 8	3725	
U114- 9	2AC4	
U114-10	low	
U114-11	59C2	
U114-12	767C	
U114-13	H816	
U114-14	1839	
U114-15	3A11	
U114-16	3FU8	
U114-17	F032	
U114-19	7PA8	
U114-20	high	
U115- 1	87UU	Sheet 7, 10
U115- 2	low	
U115- 3	3102	
U115- 4	87UU	
U115- 5	low	
U115- 6	425U	
U115- 7	low	
U115- 8	87UU	
U115- 9	low	
U115-10	low	
U115-14	high	
U116- 1	U957	Sheet 10, 11
U116- 2	7PA8	
U116- 3	high	
U116- 4	low	
U116- 5	38F6	
U116- 6	CU39	
U116- 7	low	
U116- 8	high	
U116- 9	low	
U116-10	high	
U116-11	low	
U116-12	7UFF	
U116-13	U833	
U116-14	high	
U117- 1	87UU	Sheet 10
U117- 2	87UU	
U117- 3	0000	
U117- 4	87UU	
U117- 5	87UU	
U117- 6	0000	
U117- 7	low	
U117- 8	2A14	
U117- 9	4A2C	
U117-10	U833	
U117-11	7PA8	
U117-12	low	
U117-13	U957	
U117-14	high	
U118- 1	high	Sheet 11
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U118- 4	low	
U118- 5	0000	
U118- 6	high	
U118- 7	high	
U118- 8	low	
U118- 9	high	
U118-10	high	
U118-11	0000	
U118-12	low	
U118-14	low	
U118-15	high	
U118-16	high	
U119- 1	87UU	Sheet 7, 10
U119- 2	U957	
U119- 3	87UU	
U119- 4	high	
U119- 5	U957	
U119- 6	7PA8	
U119- 7	low	
U119- 8	high	
U119- 9	low	
U119-10	low	
U119-11	low	
U119-12	CAA8	
U119-13	7UFF	
U119-14	high	
U121- 1	high	Sheet 6
U121- 2	87UU	
U121- 3	3102	
U121- 4	842F	
U121- 5	9H9F	
U121- 6	2AC4	
U121- 7	low	
U121- 8	low	
U121- 9	C1HU	
U121-10	high	
U121-15	high	
U121-16	high	

SIGNATURE TABLE: LOOP C

Loop C signatures are valid while running the Halt Mode Index RAM Data Tests.

Start = Positive edge of TP2 on the 64100A mainframe IO board, or TP5 on the 64110A mainframe CPU/IO board.

Stop = Negative edge of TP2 on the 64100A mainframe IO board, or TP5 on the 64110A mainframe CPU/IO board.

Clock = Negative edge of U117 pin 1 on the Wide Logic Analyzer.

Ground = Use a ground lead from probe to a ground point on the Wide Logic Analyzer.

Clock Qualifier = No qualified clocks are necessary.

ECL signatures require a 5005A Signature Analyzer:

To change from TTL to ECL --->
press the data threshold button three times.

To change from ECL to TTL --->
press the data threshold button five times.

High = indicates a solid HIGH on the node under test.
Low = indicates a solid LOW on the node under test.

All logic is positive logic.

Vh = 9CC1

Node	Signature		Schematic
U 1- 1	high	ECL	Sheet 3
U 1- 2	low	ECL	
U 1- 3	high	ECL	
U 1- 4	CFP9	ECL	
U 1- 5	low	ECL	
U 1- 6	low	ECL	
U 1- 7	low	ECL	
U 1- 8	low	ECL	
U 1- 9	6H6F	ECL	
U 1-10	low	ECL	
U 1-11	low	ECL	
U 1-12	CFP9	ECL	
U 1-13	low	ECL	
U 1-14	9CC1	ECL	
U 1-15	4FC0	ECL	
U 1-16	high	ECL	
U 3- 1	low	ECL	Sheet 3
U 3- 2	low	ECL	
U 3- 3	low	ECL	
U 3- 4	low	ECL	
U 3- 8	low	ECL	
U 3-16	high	ECL	
U 4- 1	low	ECL	Sheet 3
U 4- 2	high	ECL	
U 4- 3	high	ECL	
U 4- 4	low	ECL	
U 4- 5	high		
U 4- 6	high		
U 4- 7	low		
U 4- 8	low	ECL	
U 4- 9	high	ECL	
U 4-10	high		
U 4-11	high		
U 4-12	low	ECL	
U 4-13	low	ECL	
U 4-14	high	ECL	
U 4-15	high	ECL	
U 4-16	high	ECL	
U 5- 1	6H6F		Sheet 2, 3
U 5- 2	6H6F		
U 5- 3	low		
U 5- 4	low		
U 5- 5	high		
U 5- 6	high		
U 5- 7	low		
U 5- 8	high		
U 5- 9	high		
U 5-10	low		
U 5-11	9CC1		
U 5-12	U6HH		
U 5-13	high		
U 5-14	high		
U 6- 1	8P07		Sheet 7, 9
U 6- 2	low		
U 6- 4	low		
U 6- 5	low		
U 6- 7	low		
U 6-11	high		
U 6-12	low		
U 6-13	high		
U 6-14	high		
U 7- 1	low		Sheet 1
U 7- 2	901F		
U 7- 3	82AC		
U 7- 4	9300		
U 7- 5	PU4H		
U 7- 6	26F7		
U 7- 7	2C65		
U 7- 8	73C5		
U 7- 9	U135		
U 7-10	low		
U 7-11	6A84		
U 7-12	P804		
U 7-13	C0H4		
U 7-14	CH76		
U 7-15	74UF		
U 7-16	08C1		
U 7-17	191A		
U 7-18	0CAH		
U 7-19	low		
U 7-20	high		
U 8- 1	high		Sheet 1
U 8- 2	82AC		
U 8- 5	PU4H		
U 8- 6	2C65		
U 8- 9	U135		
U 8-10	low		
U 8-11	high		
U 8-12	P804		
U 8-15	CH76		
U 8-16	08C1		
U 8-19	0CAH		
U 8-20	high		
U 9- 1	low		Sheet 1
U 9- 2	901F		
U 9- 3	82AC		
U 9- 4	9300		
U 9- 5	PU4H		
U 9- 6	26F7		
U 9- 7	2C65		
U 9- 8	73C5		
U 9- 9	U135		
U 9-10	low		
U 9-11	6A84		
U 9-12	P804		
U 9-13	C0H4		
U 9-14	CH76		
U 9-15	74UF		
U 9-16	08C1		
U 9-17	191A		
U 9-18	0CAH		
U 9-19	low		
U 9-20	high		
U 10- 1	high		Sheet 1
U 10- 2	82AC		
U 10- 5	PU4H		
U 10- 6	2C65		
U 10- 9	U135		
U 10-10	low		
U 10-11	high		
U 10-12	P804		
U 10-15	CH76		
U 10-16	08C1		
U 10-19	0CAH		
U 10-20	high		

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U 11- 1	low		Sheet 1
U 11- 2	901F		
U 11- 3	82AC		
U 11- 4	9300		
U 11- 5	PU4H		
U 11- 6	26F7		
U 11- 7	2C65		
U 11- 8	73C5		
U 11- 9	U135		
U 11-10	low		
U 11-11	6A84		
U 11-12	P804		
U 11-13	C0H4		
U 11-14	CH76		
U 11-15	74UF		
U 11-16	08C1		
U 11-17	191A		
U 11-18	0CAH		
U 11-19	low		
U 11-20	high		
U 12- 1	high		Sheet 1
U 12- 2	82AC		
U 12- 5	PU4H		
U 12- 6	2C65		
U 12- 9	U135		
U 12-10	low		
U 12-11	high		
U 12-12	P804		
U 12-15	CH76		
U 12-16	08C1		
U 12-19	0CAH		
U 12-20	high		
U 13- 1	low		Sheet 1
U 13- 2	901F		
U 13- 3	82AC		
U 13- 4	9300		
U 13- 5	PU4H		
U 13- 6	26F7		
U 13- 7	2C65		
U 13- 8	73C5		
U 13- 9	U135		
U 13-10	low		
U 13-11	6A84		
U 13-12	P804		
U 13-13	C0H4		
U 13-14	CH76		
U 13-15	74UF		
U 13-16	08C1		
U 13-17	191A		
U 13-18	0CAH		
U 13-19	low		
U 13-20	high		
U 14- 1	high		Sheet 1
U 14- 2	82AC		
U 14- 5	PU4H		
U 14- 6	2C65		
U 14- 9	U135		
U 14-10	low		
U 14-11	high		
U 14-12	P804		
U 14-15	CH76		
U 14-16	08C1		
U 14-19	0CAH		
U 14-20	high		
U 15- 1	low		Sheet 1
U 15- 2	901F		
U 15- 3	82AC		
U 15- 4	9300		
U 15- 5	PU4H		
U 15- 6	26F7		
U 15- 7	2C65		
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U 51- 7	low	
U 51- 8	low	ECL
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U 51-11	low	
U 51-12	6H6F	ECL
U 51-13	high	ECL
U 51-14	low	ECL
U 51-15	9CC1	ECL
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U 52- 3	0000	ECL
U 52- 4	9CC1	
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U 52- 6	0000	ECL
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U 52- 9	high	ECL
U 52-10	0000	ECL
U 52-11	0000	ECL
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U 52-13	low	
U 52-14	high	ECL
U 52-15	0000	ECL
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U 53- 3	high	
U 53- 4	9CC1	
U 53- 5	high	
U 53- 6	0000	
U 53- 8	low	
U 53-10	0000	
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U 61-10	high	
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U 61-12	low	

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U 66-10	0000	
U 66-11	low	
U 66-12	7H71	
U 66-13	low	
U 66-14	3A26	
U 66-15	low	
U 66-16	7H71	
U 66-17	high	
U 66-18	9567	
U 66-19	low	
U 66-20	6H6F	
U 66-21	low	
U 66-22	high	
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U 67- 3	low	
U 67- 4	low	
U 67- 5	low	
U 67- 6	low	
U 67- 7	low	
U 67- 8	low	
U 67- 9	low	
U 67-10	0000	
U 67-11	low	
U 67-12	0000	
U 67-13	low	
U 67-14	0000	
U 67-15	low	
U 67-16	0000	
U 67-17	high	
U 67-18	9567	
U 67-19	low	
U 67-20	6H6F	
U 67-21	low	
U 67-22	high	
U 68- 1	low	Sheet 9
U 68- 2	low	
U 68- 3	low	
U 68- 4	low	
U 68- 5	low	
U 68- 6	low	
U 68- 7	low	
U 68- 8	low	
U 68- 9	low	
U 68-10	0000	
U 68-11	low	
U 68-12	0000	
U 68-13	low	
U 68-14	0000	
U 68-15	low	
U 68-16	0000	
U 68-17	high	
U 68-18	9567	
U 68-19	low	
U 68-20	6H6F	
U 68-21	low	
U 68-22	high	
U 69- 1	low	Sheet 9
U 69- 2	low	
U 69- 3	low	
U 69- 4	low	
U 69- 5	low	
U 69- 6	low	
U 69- 7	low	
U 69- 8	low	
U 69- 9	low	
U 69-10	5PFU	
U 69-11	low	
U 69-12	7H71	
U 69-13	low	
U 69-14	7H71	
U 69-15	low	
U 69-16	7H71	
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U 69-18	high	
U 69-19	low	
U 69-20	6H6F	
U 69-21	low	
U 69-22	high	
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U 70- 3	low	
U 70- 4	low	
U 70- 5	low	
U 70- 6	low	
U 70- 7	low	
U 70- 8	low	
U 70- 9	low	
U 70-10	0000	
U 70-11	low	
U 70-12	7H71	
U 70-13	low	
U 70-14	3A26	
U 70-15	low	
U 70-16	7H71	
U 70-17	high	

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U 70-19	low	
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U 70-21	low	
U 70-22	high	
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U 71- 3	379C	
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U 71- 7	low	
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U 71- 9	low	
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U 71-11	4A84	
U 71-12	low	
U 71-13	4A84	
U 71-14	high	
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U 72- 5	2758	
U 72- 6	15C6	
U 72- 7	8P07	
U 72- 8	low	
U 72- 9	8P07	
U 72-10	15C6	
U 72-11	2758	
U 72-12	6H6F	
U 72-13	4A84	
U 72-14	low	
U 72-15	high	
U 72-16	high	
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U 73- 2	0FH4	
U 73- 3	AF33	
U 73- 4	H4HH	
U 73- 5	PA6C	
U 73- 6	3UU2	
U 73- 7	low	
U 73- 8	A6C0	
U 73- 9	8P07	
U 73-10	P6PF	
U 73-13	15C6	
U 73-14	high	

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U 74- 3	15C6	
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U 74- 5	PA6C	
U 74- 6	high	
U 74- 7	low	
U 74- 8	4A84	
U 74- 9	AU37	
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U 75- 4	0FH4	
U 75- 5	9U8F	
U 75- 6	A0HU	
U 75- 7	low	
U 75- 8	P6PF	
U 75- 9	AU37	
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U 75-11	low	
U 75-12	low	
U 75-13	low	
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U 76- 9	9567	
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U 76-12	low	
U 76-13	low	
U 76-14	low	
U 76-15	low	
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U 77- 9	0000	
U 77-10	low	
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U 78- 4	high	
U 78- 5	3A26	
U 78- 6	high	
U 78- 7	7H71	
U 78- 8	high	
U 78- 9	0000	
U 78-10	low	
U 78-11	high	
U 78-12	5PFU	
U 78-13	high	
U 78-14	7H71	
U 78-15	high	
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U 80- 4	low	
U 80- 5	0000	
U 80- 6	low	
U 80- 7	0000	
U 80- 8	low	
U 80- 9	0000	
U 80-10	low	
U 80-11	low	
U 80-12	0000	

U 80-13	low	
U 80-14	0000	
U 80-15	low	
U 80-16	0000	
U 80-17	low	
U 80-18	0000	
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U 80-20	high	
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U 81- 8	low	
U 81- 9	high	
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U 81-14	PH77	
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U 81-16	high	
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U 82- 8	low	
U 82- 9	high	
U 82-10	high	
U 82-11	low	
U 82-12	low	
U 82-13	low	
U 82-14	low	
U 82-15	low	
U 82-16	high	
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U 83- 8	low	
U 83- 9	high	
U 83-10	low	
U 83-11	low	
U 83-12	low	
U 83-13	low	
U 83-14	low	
U 83-15	low	
U 83-16	high	
U 84- 1	2758	Sheet 9
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U 84- 7	low	

U 84- 8	low	
U 84- 9	high	
U 84-10	low	
U 84-11	low	
U 84-12	low	
U 84-13	low	
U 84-14	low	
U 84-15	low	
U 84-16	high	
U 85- 1	2758	Sheet 9
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U 85- 7	low	
U 85- 8	low	
U 85- 9	high	
U 85-10	low	
U 85-11	low	
U 85-12	low	
U 85-13	low	
U 85-14	low	
U 85-15	low	
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U 86- 9	high	
U 86-10	low	
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U 87- 9	2A10	
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U 88- 6	high	
U 88- 7	low	
U 88- 8	low	
U 88- 9	low	
U 88-11	2758	
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U 91- 1	low	Sheet 5, 7
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U 91- 4	low	
U 91- 5	3UU2	
U 91- 6	high	
U 91- 7	low	
U 91- 8	8P07	
U 91- 9	3C6P	
U 91-10	PA6C	
U 91-11	8P07	
U 91-12	A0HU	
U 91-13	UUHH	
U 91-14	high	
U 92- 1	UUHH	Sheet 5, 9
U 92- 2	646F	
U 92- 3	A0HU	
U 92- 4	3C6P	
U 92- 5	9CC1	
U 92- 6	0000	
U 92- 7	low	
U 92- 8	low	

U 92- 9	high	
U 92-10	low	
U 92-11	high	
U 92-12	9U8F	
U 92-13	043H	
U 92-14	high	
U 93- 1	2758	Sheet 7
U 93- 2	9CC1	
U 93- 3	73C5	
U 93- 4	26F7	
U 93- 5	9300	
U 93- 6	901F	
U 93- 7	6177	
U 93- 8	low	
U 93- 9	9567	
U 93-10	low	
U 93-11	low	
U 93-12	low	
U 93-13	low	
U 93-14	low	
U 93-15	low	
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U 94- 3	UP29	
U 94- 4	510C	
U 94- 5	0F42	
U 94- 6	8833	
U 94- 7	A6C0	
U 94- 8	low	
U 94- 9	2PH7	
U 94-10	low	
U 94-11	high	
U 94-12	high	
U 94-13	high	
U 94-14	high	
U 94-15	low	
U 94-16	high	
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U 95- 3	1P06	
U 95- 4	1HHU	
U 95- 5	526C	
U 95- 6	9H69	
U 95- 7	A6C0	
U 95- 8	low	
U 95- 9	2PH7	
U 95-10	low	

U 95-11	high	
U 95-12	high	
U 95-13	high	
U 95-14	high	
U 95-15	low	
U 95-16	high	
U 96- 1	high	Sheet 4
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U 96- 4	low	
U 96- 5	9A96	
U 96- 6	low	
U 96- 7	85A2	
U 96- 8	low	
U 96- 9	9721	
U 96-10	low	
U 96-11	low	
U 96-12	4CH2	
U 96-13	low	
U 96-14	2251	
U 96-15	low	
U 96-16	4F77	
U 96-17	low	
U 96-18	PHF5	
U 96-19	high	
U 96-20	high	
U 97- 1	016C	Sheet 5
U 97- 2	P7AA	
U 97- 3	770P	
U 97- 4	9A96	
U 97- 5	2251	
U 97- 6	H685	
U 97- 7	low	
U 97- 8	183U	
U 97- 9	2F40	
U 97-10	85A2	
U 97-11	4F77	
U 97-12	U1A4	
U 97-13	4CH2	
U 97-14	high	
U 98- 1	379C	Sheet 5
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U 98- 3	183U	
U 98- 4	H4HH	
U 98- 5	H685	
U 98- 6	7A3A	
U 98- 7	low	
U 98- 8	043H	

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U 98-12	U1A4	
U 98-13	AU37	
U 98-14	high	
U 99- 1	7796	Sheet 5
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U 99- 3	7H06	
U 99- 4	C9A9	
U 99- 5	78U0	
U 99- 6	7A3A	
U 99- 7	low	
U 99- 8	P617	
U 99- 9	153U	
U 99-10	0PFP	
U 99-11	463C	
U 99-12	1287	
U 99-13	7385	
U 99-14	high	
U100- 1	PHF5	Sheet 5
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U100- 3	717P	
U100- 4	U391	
U100- 5	1523	
U100- 6	0FH4	
U100- 7	low	
U100- 8	1523	
U100- 9	895F	
U100-11	670U	
U100-12	043H	
U100-13	C986	
U100-14	high	
U101- 1	F73P	Sheet 5
U101- 2	low	
U101- 3	low	
U101- 4	F73P	
U101- 6	670U	
U101- 7	low	
U101- 8	717P	
U101- 9	P9CP	
U101-10	670U	
U101-11	670U	
U101-12	643A	
U101-13	643A	
U101-14	high	
U102- 1	P9CP	Sheet 5
U102- 2	low	
U102- 3	low	
U102- 4	895F	
U102- 5	CUC5	
U102- 6	P9CP	
U102- 7	low	
U102- 8	U391	
U102- 9	low	
U102-10	low	
U102-11	CUC5	
U102-12	CF4P	
U102-13	CF4P	
U102-14	high	
U103- 1	high	Sheet 6
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U103- 6	8833	
U103- 7	low	
U103- 8	low	
U103- 9	2A10	
U103-10	high	
U103-15	high	
U103-16	high	
U104- 1	high	Sheet 6
U104- 2	9CC1	
U104- 3	1P06	
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U104- 5	526C	
U104- 6	9H69	
U104- 7	low	
U104- 8	low	
U104- 9	2A10	
U104-10	high	
U104-15	high	
U104-16	high	
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U106- 5	low	
U106- 6	9CC1	
U106- 7	high	
U106- 8	low	
U106- 9	high	
U106-10	high	
U106-11	high	
U106-12	9567	
U106-13	high	
U106-14	high	
U106-15	H074	
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U107- 3	075A	
U107- 4	0000	
U107- 5	9CC1	
U107- 6	HPA2	
U107- 7	66A7	
U107- 8	low	
U107- 9	653A	
U107-10	2A10	
U107-11	2PH7	
U107-12	A349	
U107-13	6H6F	
U107-14	2758	
U107-15	3085	
U107-16	high	
U108- 1	high	Sheet 11
U108- 2	high	
U108- 3	4759	
U108- 4	077P	
U108- 5	low	
U108- 6	high	
U108- 7	7UC4	
U108- 8	U7F1	
U108- 9	high	
U108-10	low	
U108-11	A349	
U108-12	low	
U108-13	C942	
U108-14	A713	
U108-15	low	
U108-16	low	
U108-17	FH72	
U108-18	4004	
U108-19	high	
U108-20	high	
U109- 1	high	Sheet 11
U109- 2	low	
U109- 3	UP29	
U109- 4	510C	
U109- 5	low	
U109- 6	low	
U109- 7	0F42	
U109- 8	8833	
U109- 9	low	
U109-10	low	
U109-11	A349	
U109-12	A0HU	
U109-13	1P06	
U109-14	1HHU	
U109-15	low	
U109-16	low	
U109-17	526C	
U109-18	9H69	
U109-19	high	
U109-20	high	
U110- 1	low	Sheet 11
U110- 2	82AC	
U110- 3	901F	
U110- 4	PU4H	
U110- 5	9300	
U110- 6	2C65	
U110- 7	26F7	
U110- 8	U135	
U110- 9	73C5	
U110-10	low	
U110-11	P804	
U110-12	6A84	
U110-13	CH76	
U110-14	C0H4	
U110-15	08C1	
U110-16	74UF	
U110-17	0CAH	
U110-18	191A	
U110-19	low	
U110-20	high	
U111- 1	low	Sheet 11
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U111- 3	UP29	
U111- 4	1HHU	
U111- 5	510C	
U111- 6	526C	
U111- 7	0F42	
U111- 8	9H69	
U111- 9	8833	
U111-10	low	
U111-11	8833	
U111-12	9H69	
U111-13	0F42	
U111-14	526C	
U111-15	510C	
U111-16	1HHU	

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U111-17	UP29	
U111-18	1P06	
U111-19	low	
U111-20	high	
U112- 1	HPA2	Sheet 11
U112- 2	0000	
U112- 3	UP29	
U112- 4	7H71	
U112- 5	510C	
U112- 6	3A26	
U112- 7	0F42	
U112- 8	7H71	
U112- 9	8833	
U112-10	low	
U112-11	7H71	
U112-12	9H69	
U112-13	7H71	
U112-14	526C	
U112-15	7H71	
U112-16	1HHU	
U112-17	5PFU	
U112-18	1P06	
U112-19	HPA2	
U112-20	high	
U113- 1	low	Sheet 11
U113- 2	4759	
U113- 3	4004	
U113- 4	077P	
U113- 5	FH72	
U113- 6	7UC4	
U113- 7	A713	
U113- 8	U7F1	
U113- 9	C942	
U113-10	low	
U113-11	C942	
U113-12	U7F1	
U113-13	A713	
U113-14	7UC4	
U113-15	FH72	
U113-16	077P	
U113-17	4004	
U113-18	4759	
U113-19	low	
U113-20	high	
U114- 1	HPA2	Sheet 11
U114- 2	0000	
U114- 3	4004	
U114- 4	0000	
U114- 5	FH72	
U114- 6	0000	
U114- 7	A713	
U114- 8	0000	
U114- 9	C942	
U114-10	low	
U114-11	0000	
U114-12	U7F1	
U114-13	0000	
U114-14	7UC4	
U114-15	0000	
U114-16	077P	
U114-17	0000	
U114-18	4759	
U114-19	HPA2	
U114-20	high	
U115- 1	9CC1	Sheet 7, 10
U115- 2	low	
U115- 3	4004	
U115- 4	9CC1	
U115- 5	low	
U115- 6	510C	
U115- 7	low	
U115- 8	high	
U115- 9	low	
U115-10	low	
U115-14	high	
U116- 1	4513	Sheet 10, 11
U116- 2	HPA2	
U116- 3	high	
U116- 4	low	
U116- 5	6H6F	
U116- 6	U6HH	
U116- 7	low	
U116- 8	high	
U116- 9	low	
U116-10	high	
U116-11	low	
U116-12	F7A9	
U116-13	5F18	
U116-14	high	
U117- 1	9CC1	Sheet 10
U117- 2	9CC1	
U117- 3	0000	
U117- 4	9CC1	
U117- 5	9CC1	
U117- 6	0000	
U117- 7	low	
U117- 8	075A	
U117- 9	F36P	
U117-10	5F18	
U117-11	HPA2	
U117-12	low	
U117-13	4513	
U117-14	high	
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U118- 2	low	
U118- 4	low	
U118- 5	high	
U118- 6	15C6	
U118- 7	high	
U118- 8	low	
U118- 9	high	
U118-10	high	
U118-11	0000	
U118-12	low	
U118-14	low	
U118-15	high	
U118-16	high	
U119- 1	9CC1	Sheet 7, 10
U119- 2	4513	
U119- 3	9CC1	
U119- 4	high	
U119- 5	4513	
U119- 6	HPA2	
U119- 7	low	
U119- 8	high	
U119- 9	low	
U119-10	low	
U119-11	low	
U119-12	9567	
U119-13	F7A9	
U119-14	high	
U121- 1	high	Sheet 6
U121- 2	9CC1	
U121- 3	4004	
U121- 4	FH72	
U121- 5	A713	
U121- 6	C942	
U121- 7	low	
U121- 8	low	
U121- 9	2A10	
U121-10	high	
U121-15	high	
U121-16	high	

SIGNATURE TABLE: LOOP D

Loop D signatures are valid while running the Halt Mode Index RAM Address Tests.

Start = Positive edge of TP2 on the 64100A mainframe IO board, or TP5 on the 64110A mainframe CPU/IO board.

Stop = Negative edge of TP2 on the 64100A mainframe IO board, or TP5 on the 64110A mainframe CPU/IO board.

Clock = Negative edge of U117 pin 1 on the Wide Logic Analyzer.

Ground = Use a ground lead from probe to a ground point on the Wide Logic Analyzer.

Clock Qualifier = No qualified clocks are necessary.

ECL signatures require a 5005A Signature Analyzer:

To change from TTL to ECL --->
press the data threshold button three times.

To change from ECL to TTL --->
press the data threshold button five times.

High = indicates a solid HIGH on the node under test.
Low = indicates a solid LOW on the node under test.

All logic is positive logic.

Vh = FP9P

Node	Signature		Schematic
U 1- 1	high	ECL	Sheet 3
U 1- 2	low	ECL	
U 1- 3	high	ECL	
U 1- 4	9U9H	ECL	
U 1- 5	low	ECL	
U 1- 6	low	ECL	
U 1- 7	low	ECL	
U 1- 8	low	ECL	
U 1- 9	F3FH	ECL	
U 1-10	low	ECL	
U 1-11	low	ECL	
U 1-12	9U9H	ECL	
U 1-13	low	ECL	
U 1-14	FP9P	ECL	
U 1-15	87FC	ECL	
U 1-16	high	ECL	
U 3- 1	low	ECL	Sheet 3
U 3- 2	low	ECL	
U 3- 3	low	ECL	
U 3- 4	low	ECL	
U 3- 8	low	ECL	
U 3-16	high	ECL	
U 4- 1	low	ECL	Sheet 3
U 4- 2	high	ECL	
U 4- 3	high	ECL	
U 4- 4	low	ECL	
U 4- 5	high		
U 4- 6	high		
U 4- 7	low		
U 4- 8	low	ECL	
U 4- 9	high	ECL	
U 4-10	high		
U 4-11	high		
U 4-12	low	ECL	
U 4-13	low	ECL	
U 4-14	high	ECL	
U 4-15	high	ECL	
U 4-16	high	ECL	
U 5- 1	F3FH		Sheet 2, 3
U 5- 2	F3FH		
U 5- 3	low		
U 5- 4	low		
U 5- 5	high		
U 5- 6	high		
U 5- 7	low		
U 5- 8	high		
U 5- 9	high		
U 5-10	low		
U 5-11	FP9P		
U 5-12	0H53		
U 5-13	high		
U 5-14	high		
U 6- 1	low		Sheet 7, 9
U 6- 2	low		
U 6- 4	low		
U 6- 5	low		
U 6- 7	low		
U 6-11	high		
U 6-12	low		
U 6-13	high		
U 6-14	high		
U 7- 1	low		Sheet 1
U 7- 2	FAC7		
U 7- 3	9843		
U 7- 4	P4HU		
U 7- 5	AC4C		
U 7- 6	26F2		
U 7- 7	365P		
U 7- 8	979C		
U 7- 9	473U		
U 7-10	low		
U 7-11	89A1		
U 7-12	5905		
U 7-13	U8F0		
U 7-14	P85F		
U 7-15	65H5		
U 7-16	2A41		
U 7-17	56HH		
U 7-18	0429		
U 7-19	low		
U 7-20	high		
U 8- 1	high		Sheet 1
U 8- 2	9843		
U 8- 5	AC4C		
U 8- 6	365P		
U 8- 9	473U		
U 8-10	low		
U 8-11	high		
U 8-12	5905		
U 8-15	P85F		
U 8-16	2A41		
U 8-19	0429		
U 8-20	high		
U 9- 1	low		Sheet 1
U 9- 2	FAC7		
U 9- 3	9843		
U 9- 4	P4HU		
U 9- 5	AC4C		
U 9- 6	26F2		
U 9- 7	365P		
U 9- 8	979C		
U 9- 9	473U		
U 9-10	low		
U 9-11	89A1		
U 9-12	5905		
U 9-13	U8F0		
U 9-14	P85F		
U 9-15	65H5		
U 9-16	2A41		
U 9-17	56HH		
U 9-18	0429		
U 9-19	low		
U 9-20	high		
U 10- 1	high		Sheet 1
U 10- 2	9843		
U 10- 5	AC4C		
U 10- 6	365P		
U 10- 9	473U		
U 10-10	low		
U 10-11	high		
U 10-12	5905		
U 10-15	P85F		
U 10-16	2A41		
U 10-19	0429		
U 10-20	high		
U 11- 1	low		Sheet 1
U 11- 2	FAC7		

Signature Analysis Loop D

U 11- 3	9843		
U 11- 4	P4HU		
U 11- 5	AC4C		
U 11- 6	26F2		
U 11- 7	365P		
U 11- 8	979C		
U 11- 9	473U		
U 11-10	low		
U 11-11	89A1		
U 11-12	5905		
U 11-13	U8F0		
U 11-14	P85F		
U 11-15	65H5		
U 11-16	2A41		
U 11-17	56HH		
U 11-18	0429		
U 11-19	low		
U 11-20	high		
U 12- 1	high	Sheet 1	
U 12- 2	9843		
U 12- 5	AC4C		
U 12- 6	365P		
U 12- 9	473U		
U 12-10	low		
U 12-11	high		
U 12-12	5905		
U 12-15	P85F		
U 12-16	2A41		
U 12-19	0429		
U 12-20	high		
U 13- 1	low	Sheet 1	
U 13- 2	FAC7		
U 13- 3	9843		
U 13- 4	P4HU		
U 13- 5	AC4C		
U 13- 6	26F2		
U 13- 7	365P		
U 13- 8	979C		
U 13- 9	473U		
U 13-10	low		
U 13-11	89A1		
U 13-12	5905		
U 13-13	U8F0		
U 13-14	P85F		
U 13-15	65H5		
U 13-16	2A41		
U 13-17	56HH		
U 13-18	0429		
U 13-19	low		
U 13-20	high		

U 14- 1	high	Sheet 1	
U 14- 2	9843		
U 14- 5	AC4C		
U 14- 6	365P		
U 14- 9	473U		
U 14-10	low		
U 14-11	high		
U 14-12	5905		
U 14-15	P85F		
U 14-16	2A41		
U 14-19	0429		
U 14-20	high		
U 15- 1	low	Sheet 1	
U 15- 2	FAC7		
U 15- 3	9843		
U 15- 4	P4HU		
U 15- 5	AC4C		
U 15- 6	26F2		
U 15- 7	365P		
U 15- 8	979C		
U 15- 9	473U		
U 15-10	low		
U 15-11	89A1		
U 15-12	5905		
U 15-13	U8F0		
U 15-14	P85F		
U 15-15	65H5		
U 15-16	2A41		
U 15-17	56HH		
U 15-18	0429		
U 15-19	low		
U 15-20	high		
U 16- 1	high	Sheet 1	
U 16- 2	9843		
U 16- 5	AC4C		
U 16- 6	365P		
U 16- 9	473U		
U 16-10	low		
U 16-11	high		
U 16-12	5905		
U 16-15	P85F		
U 16-16	2A41		
U 16-19	0429		
U 16-20	high		
U 17- 1	low	Sheet 1	
U 17- 2	FAC7		
U 17- 3	9843		
U 17- 4	P4HU		
U 17- 5	AC4C		

U 17- 6	26F2		
U 17- 7	365P		
U 17- 8	979C		
U 17- 9	473U		
U 17-10	low		
U 17-11	89A1		
U 17-12	5905		
U 17-13	U8F0		
U 17-14	P85F		
U 17-15	65H5		
U 17-16	2A41		
U 17-17	56HH		
U 17-18	0429		
U 17-19	low		
U 17-20	high		
U 18- 1	high	Sheet 1	
U 18- 2	9843		
U 18- 5	AC4C		
U 18- 6	365P		
U 18- 9	473U		
U 18-10	low		
U 18-11	high		
U 18-12	5905		
U 18-15	P85F		
U 18-16	2A41		
U 18-19	0429		
U 18-20	high		
U 19- 1	0000	ECL	Sheet 2, 3
U 19- 2	0000	ECL	
U 19- 3	high	ECL	
U 19- 4	high		
U 19- 5	high		
U 19- 7	0000	ECL	
U 19- 8	low	ECL	
U 19- 9	high	ECL	
U 19-10	0000	ECL	
U 19-11	87FC	ECL	
U 19-12	87FC		
U 19-13	high		
U 19-14	low	ECL	
U 19-15	0000	ECL	
U 19-16	high	ECL	
U 20- 1	high	ECL	Sheet 2
U 20- 2	FP9P	ECL	
U 20- 3	0000	ECL	
U 20- 4	low	ECL	
U 20- 5	0000	ECL	
U 20- 6	low	ECL	
U 20- 7	low	ECL	

U 20- 8	low	ECL	
U 20- 9	0000	ECL	
U 20-10	low	ECL	
U 20-11	low	ECL	
U 20-12	0000	ECL	
U 20-13	low	ECL	
U 20-14	0000	ECL	
U 20-15	FP9P	ECL	
U 20-16	high	ECL	
U 23- 1	high	ECL	Sheet 2
U 23- 2	0000	ECL	
U 23- 4	FP9P	ECL	
U 23- 5	0000	ECL	
U 23- 6	0000	ECL	
U 23- 7	FP9P	ECL	
U 23- 8	low	ECL	
U 23-12	low	ECL	
U 23-13	FP9P	ECL	
U 23-14	high	ECL	
U 23-15	0000	ECL	
U 23-16	high	ECL	
U 24- 1	low		Sheet 2, 3
U 24- 2	high		
U 24- 3	low		
U 24- 4	low		
U 24- 5	high		
U 24- 6	high		
U 24- 7	low		
U 24- 8	high		
U 24- 9	high		
U 24-10	low		
U 24-11	0H53		
U 24-12	high		
U 24-13	low		
U 24-14	high		
U 25- 1	high		Sheet 10
U 25- 2	high		
U 25- 3	high		
U 25- 4	high		
U 25- 5	5103		
U 25- 7	low		
U 25- 8	low		
U 25- 9	low		
U 25-10	high		
U 25-11	5103		
U 25-12	high		
U 25-15	high		
U 25-16	high		

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U 26- 1	473U	Sheet 4
U 26- 2	365P	
U 26- 3	AC4C	
U 26- 4	9843	
U 26- 5	P85F	
U 26- 6	2A41	
U 26- 7	0429	
U 26- 8	low	
U 26- 9	UH27	
U 26-10	7034	
U 26-11	FA8H	
U 26-12	0000	
U 26-13	FA8H	
U 26-14	0000	
U 26-15	1PH1	
U 26-16	0HUF	
U 26-17	high	
U 26-18	low	
U 26-19	low	
U 26-20	87UF	
U 26-21	5905	
U 26-22	high	

U 27- 1	473U	Sheet 4
U 27- 2	365P	
U 27- 3	AC4C	
U 27- 4	9843	
U 27- 5	P85F	
U 27- 6	2A41	
U 27- 7	0429	
U 27- 8	low	
U 27- 9	C10U	
U 27-10	79F6	
U 27-11	770H	
U 27-12	0000	
U 27-13	FA8H	
U 27-14	0000	
U 27-15	AP8F	
U 27-16	0HUF	
U 27-17	high	
U 27-18	low	
U 27-19	low	
U 27-20	87UF	
U 27-21	5905	
U 27-22	high	

U 28- 1	473U	Sheet 4
U 28- 2	365P	
U 28- 3	AC4C	
U 28- 4	9843	
U 28- 5	P85F	
U 28- 6	2A41	
U 28- 7	0429	
U 28- 8	low	
U 28- 9	2P30	
U 28-10	8F1F	
U 28-11	83PU	
U 28-12	0000	
U 28-13	33C2	
U 28-14	0000	
U 28-15	62F2	
U 28-16	P741	
U 28-17	high	
U 28-18	low	
U 28-19	low	
U 28-20	33C2	
U 28-21	5905	
U 28-22	high	

U 29- 1	473U	Sheet 4
U 29- 2	365P	
U 29- 3	AC4C	
U 29- 4	9843	
U 29- 5	P85F	
U 29- 6	2A41	
U 29- 7	0429	
U 29- 8	low	
U 29- 9	UH27	
U 29-10	U4P3	
U 29-11	FA8H	
U 29-12	0000	
U 29-13	FA8H	
U 29-14	0000	
U 29-15	1PH1	
U 29-16	0000	
U 29-17	high	
U 29-18	low	
U 29-19	low	
U 29-20	33C2	
U 29-21	5905	
U 29-22	high	

U 30- 1	AC4C	Sheet 4
U 30- 2	9843	
U 30- 3	low	
U 30- 4	low	
U 30- 5	low	
U 30- 6	9UA2	
U 30- 7	5905	
U 30- 8	low	
U 30- 9	P85F	
U 30-10	2A41	
U 30-11	0429	
U 30-12	33C2	
U 30-13	C10U	
U 30-14	473U	
U 30-15	365P	
U 30-16	high	

U 31- 1	473U	Sheet 4
U 31- 2	365P	
U 31- 3	AC4C	
U 31- 4	9843	
U 31- 5	P85F	
U 31- 6	2A41	
U 31- 7	0429	
U 31- 8	low	
U 31- 9	high	
U 31-10	FP9P	
U 31-11	770H	
U 31-12	F80F	
U 31-13	FA8H	
U 31-14	0000	
U 31-15	AP8F	
U 31-16	0000	
U 31-17	high	
U 31-18	low	
U 31-19	low	
U 31-20	33C2	
U 31-21	5905	
U 31-22	high	

U 32- 1	473U	Sheet 4
U 32- 2	365P	
U 32- 3	AC4C	
U 32- 4	9843	
U 32- 5	P85F	
U 32- 6	2A41	
U 32- 7	0429	
U 32- 8	low	
U 32- 9	C745	
U 32-10	0000	
U 32-11	FA8H	
U 32-12	0000	
U 32-13	869A	
U 32-14	8A68	
U 32-15	FA8H	
U 32-16	0000	
U 32-17	high	
U 32-18	low	
U 32-19	low	
U 32-20	33C2	
U 32-21	5905	
U 32-22	high	

U 33- 1	473U	Sheet 4
U 33- 2	365P	
U 33- 3	AC4C	
U 33- 4	9843	
U 33- 5	P85F	
U 33- 6	2A41	
U 33- 7	0429	
U 33- 8	low	
U 33- 9	C745	
U 33-10	773F	
U 33-11	FA8H	
U 33-12	0000	
U 33-13	869A	
U 33-14	0000	
U 33-15	FA8H	
U 33-16	0000	
U 33-17	high	
U 33-18	low	
U 33-19	low	
U 33-20	87UF	
U 33-21	5905	
U 33-22	high	

U 34- 1	AC4C	Sheet 4
U 34- 2	9843	
U 34- 3	low	
U 34- 4	low	
U 34- 5	low	
U 34- 6	740C	
U 34- 7	5905	
U 34- 8	low	
U 34- 9	P85F	
U 34-10	2A41	
U 34-11	0429	
U 34-12	87UF	
U 34-13	2P30	
U 34-14	473U	
U 34-15	365P	
U 34-16	high	

U 36- 1	high	ECL	Sheet 2
U 36- 2	high	ECL	
U 36- 3	0000	ECL	
U 36- 4	low	ECL	
U 36- 5	0000	ECL	
U 36- 6	low	ECL	
U 36- 7	low	ECL	
U 36- 8	low	ECL	
U 36- 9	F3FH	ECL	
U 36-10	low	ECL	
U 36-11	low	ECL	
U 36-12	0000	ECL	

U 36-13	low	ECL	
U 36-14	0000	ECL	
U 36-15	FP9P	ECL	
U 36-16	high	ECL	
U 38- 1	high	ECL	Sheet 9
U 38- 2	high	ECL	
U 38- 3	low	ECL	
U 38- 4	low	ECL	
U 38- 5	low	ECL	
U 38- 6	0000	ECL	
U 38- 7	high	ECL	
U 38- 8	low	ECL	
U 38- 9	low	ECL	
U 38-10	low	ECL	
U 38-11	low	ECL	
U 38-12	high	ECL	
U 38-13	low	ECL	
U 38-14	high	ECL	
U 38-15	low	ECL	
U 38-16	high	ECL	
U 39- 1	87FC		Sheet 3
U 39- 2	low		
U 39- 3	high		
U 39- 4	high		
U 39- 5	high		
U 39- 6	low		
U 39- 7	low		
U 39- 8	high		
U 39- 9	low		
U 39-10	high		
U 39-11	high		
U 39-12	low		
U 39-13	low		
U 39-14	high		
U 40- 1	high		Sheet 9
U 40- 2	high		
U 40- 3	low		
U 40- 4	low		
U 40- 5	0000		
U 40- 6	high		
U 40- 7	low		
U 40- 8	0000		
U 40- 9	FP9P		
U 40-10	high		
U 40-11	high		
U 40-12	FP9P		
U 40-13	low		
U 40-14	high		

U 41- 1	high	Sheet 2
U 41- 2	high	
U 41- 3	low	
U 41- 4	low	
U 41- 5	high	
U 41- 6	high	
U 41- 7	low	
U 41- 8	0000	
U 41- 9	FP9P	
U 41-10	high	
U 41-11	high	
U 41-12	0000	
U 41-13	low	
U 41-14	high	
U 42- 1	low	Sheet 8
U 42- 2	low	
U 42- 3	low	
U 42- 4	low	
U 42- 5	low	
U 42- 6	low	
U 42- 7	low	
U 42- 8	low	
U 42- 9	5905	
U 42-10	0000	
U 42-11	P85F	
U 42-12	FP9P	
U 42-13	2A41	
U 42-14	FP9P	
U 42-15	0429	
U 42-16	FP9P	
U 42-17	high	
U 42-18	high	
U 42-19	low	
U 42-20	F3FH	
U 42-21	low	
U 42-22	high	
U 43- 1	low	Sheet 8
U 43- 2	low	
U 43- 3	low	
U 43- 4	low	
U 43- 5	low	
U 43- 6	low	
U 43- 7	low	
U 43- 8	low	
U 43- 9	5905	
U 43-10	0000	
U 43-11	P85F	
U 43-12	0000	
U 43-13	2A41	
U 43-14	0000	

U 43-15	0429	
U 43-16	0000	
U 43-17	high	
U 43-18	high	
U 43-19	low	
U 43-20	F3FH	
U 43-21	low	
U 43-22	high	
U 44- 1	low	Sheet 8
U 44- 2	low	
U 44- 3	low	
U 44- 4	low	
U 44- 5	low	
U 44- 6	low	
U 44- 7	low	
U 44- 8	low	
U 44- 9	5905	
U 44-10	0000	
U 44-11	P85F	
U 44-12	FP9P	
U 44-13	2A41	
U 44-14	FP9P	
U 44-15	0429	
U 44-16	FP9P	
U 44-17	high	
U 44-18	high	
U 44-19	low	
U 44-20	F3FH	
U 44-21	low	
U 44-22	high	
U 45- 1	low	Sheet 8
U 45- 2	low	
U 45- 3	low	
U 45- 4	low	
U 45- 5	low	
U 45- 6	low	
U 45- 7	low	
U 45- 8	low	
U 45- 9	9843	
U 45-10	FP9P	
U 45-11	AC4C	
U 45-12	FP9P	
U 45-13	365P	
U 45-14	FP9P	
U 45-15	473U	
U 45-16	FP9P	
U 45-17	high	
U 45-18	high	
U 45-19	low	
U 45-20	F3FH	

U 45-21	low	
U 45-22	high	
U 46- 1	low	Sheet 8
U 46- 2	low	
U 46- 3	low	
U 46- 4	low	
U 46- 5	low	
U 46- 6	low	
U 46- 7	low	
U 46- 8	low	
U 46- 9	5905	
U 46-10	0000	
U 46-11	P85F	
U 46-12	FP9P	
U 46-13	2A41	
U 46-14	FP9P	
U 46-15	0429	
U 46-16	FP9P	
U 46-17	high	
U 46-18	high	
U 46-19	low	
U 46-20	F3FH	
U 46-21	low	
U 46-22	high	
U 47- 1	low	Sheet 8
U 47- 2	low	
U 47- 3	low	
U 47- 4	low	
U 47- 5	low	
U 47- 6	low	
U 47- 7	low	
U 47- 8	low	
U 47- 9	9843	
U 47-10	0000	
U 47-11	AC4C	
U 47-12	0000	
U 47-13	365P	
U 47-14	0000	
U 47-15	473U	
U 47-16	0000	
U 47-17	high	
U 47-18	high	
U 47-19	low	
U 47-20	F3FH	
U 47-21	low	
U 47-22	high	
U 48- 1	low	Sheet 8
U 48- 2	low	
U 48- 3	low	

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U 48- 4	low	
U 48- 5	low	
U 48- 6	low	
U 48- 7	low	
U 48- 8	low	
U 48- 9	5905	
U 48-10	0000	
U 48-11	P85F	
U 48-12	0000	
U 48-13	2A41	
U 48-14	0000	
U 48-15	0429	
U 48-16	0000	
U 48-17	high	
U 48-18	high	
U 48-19	low	
U 48-20	F3FH	
U 48-21	low	
U 48-22	high	
U 49- 1	low	Sheet 8
U 49- 2	low	
U 49- 3	low	
U 49- 4	low	
U 49- 5	low	
U 49- 6	low	
U 49- 7	low	
U 49- 8	low	
U 49- 9	9843	
U 49-10	FP9P	
U 49-11	AC4C	
U 49-12	FP9P	
U 49-13	365P	
U 49-14	FP9P	
U 49-15	473U	
U 49-16	FP9P	
U 49-17	high	
U 49-18	high	
U 49-19	low	
U 49-20	F3FH	
U 49-21	low	
U 49-22	high	
U 50- 1	low	Sheet 8
U 50- 2	low	
U 50- 3	low	
U 50- 4	low	
U 50- 5	low	
U 50- 6	low	
U 50- 7	low	
U 50- 8	low	
U 50- 9	5905	
U 50-10	0000	
U 50-11	P85F	
U 50-12	FP9P	
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U 51- 4	9U9H	ECL
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U 51- 6	high	
U 51- 7	low	
U 51- 8	low	ECL
U 51- 9	high	ECL
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U 51-11	low	
U 51-12	F3FH	ECL
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U 52- 3	FP9P	ECL
U 52- 4	FP9P	
U 52- 5	high	
U 52- 7	FP9P	ECL
U 52- 8	low	ECL
U 52- 9	high	ECL
U 52-10	FP9P	ECL
U 52-11	0000	ECL
U 52-12	0000	
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U 54- 8	low	
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U 54-13	low	
U 54-14	high	
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U 55-11	0000	
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U 61- 8	high	
U 61- 9	low	
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U 61-13	low	
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U 62-14	FP9P	
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U 63- 7	low	
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U 63-11	AC4C	
U 63-12	0000	
U 63-13	365P	
U 63-14	0000	
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U 65-12	FP9P	
U 65-13	low	
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U 67-16	0000	
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U 81-10	0000	
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U 82-10	high	
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U 82-12	low	
U 82-13	low	
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U 83- 8	low	
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U 83-11	low	
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U 92- 8	low	
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U 94- 9	8F03	
U 94-10	low	
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U 96- 7	0000	
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U 96-15	low	
U 96-16	0000	
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U 97- 7	low	
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U102- 6	740C	
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U102- 8	08UA	
U102- 9	low	
U102-10	low	
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U103- 5	FA8H	
U103- 6	1PH1	
U103- 7	low	
U103- 8	low	
U103- 9	6UH0	
U103-10	high	
U103-15	high	
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U104-16	high	
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U106- 5	low	
U106- 6	FP9P	
U106- 7	high	
U106- 8	low	
U106- 9	high	
U106-10	high	
U106-11	high	
U106-12	high	
U106-13	high	
U106-14	high	
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U107- 3	579H	
U107- 4	0000	
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U107- 7	33C2	
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U108- 4	83PU	
U108- 5	low	
U108- 6	high	
U108- 7	33C2	
U108- 8	62F2	
U108- 9	high	
U108-10	low	
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U108-12	low	
U108-13	FA8H	
U108-14	869A	
U108-15	low	
U108-16	low	
U108-17	FA8H	
U108-18	C745	
U108-19	high	
U108-20	high	
U109- 1	high	Sheet 11
U109- 2	low	
U109- 3	UH27	
U109- 4	FA8H	
U109- 5	low	
U109- 6	low	
U109- 7	FA8H	
U109- 8	1PH1	
U109- 9	low	
U109-10	low	
U109-11	7PF3	
U109-12	82HA	
U109-13	C10U	
U109-14	770H	
U109-15	low	
U109-16	low	
U109-17	FA8H	
U109-18	AP8F	
U109-19	high	
U109-20	high	
U110- 1	low	Sheet 11
U110- 2	9843	
U110- 3	FAC7	
U110- 4	AC4C	
U110- 5	P4HU	
U110- 6	365P	
U110- 7	26F2	
U110- 8	473U	
U110- 9	979C	
U110-10	low	
U110-11	5905	
U110-12	89A1	
U110-13	P85F	
U110-14	U8F0	
U110-15	2A41	
U110-16	65H5	
U110-17	0429	
U110-18	56HH	
U110-19	low	
U110-20	high	
U111- 1	low	Sheet 11
U111- 2	C10U	
U111- 3	UH27	
U111- 4	770H	
U111- 5	FA8H	
U111- 6	FA8H	
U111- 7	FA8H	
U111- 8	AP8F	
U111- 9	1PH1	
U111-10	low	
U111-11	1PH1	
U111-12	AP8F	
U111-13	FA8H	
U111-14	FA8H	
U111-15	FA8H	
U111-16	770H	
U111-17	UH27	
U111-18	C10U	
U111-19	low	
U111-20	high	
U112- 1	61P6	Sheet 11
U112- 2	0000	
U112- 3	UH27	
U112- 4	FP9P	
U112- 5	FA8H	
U112- 6	FP9P	
U112- 7	FA8H	
U112- 8	FP9P	
U112- 9	1PH1	
U112-10	low	
U112-11	FP9P	
U112-12	AP8F	
U112-13	FP9P	
U112-14	FA8H	
U112-15	FP9P	
U112-16	770H	
U112-17	FP9P	
U112-18	C10U	
U112-19	61P6	
U112-20	high	
U113- 1	low	Sheet 11
U113- 2	2P30	
U113- 3	C745	
U113- 4	83PU	
U113- 5	FA8H	
U113- 6	33C2	
U113- 7	869A	
U113- 8	62F2	
U113- 9	FA8H	
U113-10	low	

U113-11	FA8H	
U113-12	62F2	
U113-13	869A	
U113-14	33C2	
U113-15	FA8H	
U113-16	83PU	
U113-17	C745	
U113-18	2P30	
U113-19	low	
U113-20	high	
U114- 1	61P6	Sheet 11
U114- 2	0000	
U114- 3	C745	
U114- 4	0000	
U114- 5	FA8H	
U114- 6	0000	
U114- 7	869A	
U114- 8	0000	
U114- 9	FA8H	
U114-10	low	
U114-12	62F2	
U114-13	0000	
U114-14	33C2	
U114-15	0000	
U114-16	83PU	
U114-17	0000	
U114-18	2P30	
U114-19	61P6	
U114-20	high	
U115- 1	FP9P	Sheet 7, 10
U115- 2	low	
U115- 3	C745	
U115- 4	FP9P	
U115- 5	low	
U115- 6	FA8H	
U115- 7	low	
U115- 8	high	
U115- 9	low	
U115-10	low	
U115-14	high	
U116- 1	AU78	Sheet 10, 11
U116- 2	61P6	
U116- 3	high	
U116- 4	low	
U116- 5	F3FH	
U116- 6	0H53	
U116- 7	low	
U116- 8	high	
U116- 9	low	
U116-10	high	
U116-11	low	
U116-12	PA93	
U116-13	240H	
U116-14	high	
U117- 1	FP9P	Sheet 10
U117- 2	FP9P	
U117- 3	0000	
U117- 4	FP9P	
U117- 5	FP9P	
U117- 6	0000	
U117- 7	low	
U117- 8	579H	
U117- 9	0940	
U117-10	240H	
U117-11	61P6	
U117-12	low	
U117-13	AU78	
U117-14	high	
U118- 1	high	Sheet 11
U118- 2	low	
U118- 4	low	
U118- 6	high	
U118- 7	high	
U118- 8	low	
U118- 9	high	
U118-10	high	
U118-11	0000	
U118-12	low	
U118-14	low	
U118-15	high	
U118-16	high	
U119- 1	FP9P	Sheet 7, 10
U119- 2	AU78	
U119- 3	FP9P	
U119- 4	high	
U119- 5	AU78	
U119- 6	61P6	
U119- 7	low	
U119- 8	high	
U119- 9	low	
U119-10	low	
U119-11	low	
U119-12	high	
U119-13	PA93	
U119-14	high	
U121- 1	high	Sheet 6
U121- 2	FP9P	
U121- 3	C745	
U121- 4	FA8H	
U121- 5	869A	
U121- 6	FA8H	
U121- 7	low	
U121- 8	low	
U121- 9	6UH0	
U121-10	high	
U121-15	high	
U121-16	high	

* end of table *

Signature Analysis Loop E

SIGNATURE TABLE: LOOP E

Loop E signatures are valid while running the Run Mode Tests.

Start = Positive edge of TP2 on the 64100A mainframe IO board, or TP5 on the 64110A mainframe CPU/IO board.

Stop = Negative edge of TP2 on the 64100A mainframe IO board, or TP5 on the 64110A mainframe CPU/IO board.

Clock = Negative edge of U117 pin 1 on the Wide Logic Analyzer.

Ground = Use a ground lead from probe to a ground point on the Wide Logic Analyzer.

Clock Qualifier = No qualified clocks are necessary.

ECL signatures require a 5005A Signature Analyzer:

To change from TTL to ECL --->
press the data threshold button three times.

To change from ECL to TTL --->
press the data threshold button five times.

High = indicates a solid HIGH on the node under test.
Low = indicates a solid LOW on the node under test.

All logic is positive logic.

Vh = A709

Node	Signature		Schematic
U 1- 1	high	ECL	Sheet 3
U 1- 2	low	ECL	
U 1- 3	high	ECL	
U 1- 4	952P	ECL	
U 1- 5	low	ECL	
U 1- 6	low	ECL	
U 1- 7	low	ECL	
U 1- 8	low	ECL	
U 1- 9	7581	ECL	
U 1-10	low	ECL	
U 1-11	low	ECL	
U 1-12	952P	ECL	
U 1-13	low	ECL	
U 1-14	A709	ECL	
U 1-15	F0F6	ECL	
U 1-16	high	ECL	
U 3- 1	low	ECL	Sheet 3
U 3- 2	low	ECL	
U 3- 3	low	ECL	
U 3- 4	low	ECL	
U 3- 8	low	ECL	
U 3-16	high	ECL	
U 4- 1	low	ECL	Sheet 3
U 4- 2	high	ECL	
U 4- 3	high	ECL	
U 4- 4	low	ECL	
U 4- 5	high		
U 4- 6	high		
U 4- 7	low		
U 4- 8	low	ECL	
U 4- 9	high	ECL	
U 4-10	high		
U 4-11	high		
U 4-12	low	ECL	
U 4-13	low	ECL	
U 4-14	high	ECL	
U 4-15	high	ECL	
U 4-16	high	ECL	
U 5- 1	7581		Sheet 2, 3
U 5- 2	7581		
U 5- 3	low		
U 5- 4	low		
U 5- 5	FAP1		
U 5- 6	high		
U 5- 7	low		
U 5- 8	F03U		
U 5- 9	9760		
U 5-10	6HP8		
U 5-11	A709		
U 5-12	H288		
U 5-13	high		
U 5-14	high		
U 6- 1	A3F3		Sheet 7, 9
U 6- 2	low		
U 6- 4	low		
U 6- 5	3069		
U 6- 7	low		
U 6-11	F03U		
U 6-12	6736		
U 6-13	high		
U 6-14	high		
U 7- 1	low		Sheet 1
U 7- 2	CU5C		
U 7- 3	PP65		
U 7- 4	CUU5		
U 7- 5	2947		
U 7- 6	U86H		
U 7- 7	PF2A		
U 7- 8	P156		
U 7- 9	87AP		
U 7-10	low		
U 7-11	20A7		
U 7-12	465U		
U 7-13	4C23		
U 7-14	5U64		
U 7-15	8P4P		
U 7-16	18UF		
U 7-17	496F		
U 7-18	1852		
U 7-19	low		
U 7-20	high		
U 8- 1	high		Sheet 1
U 8- 2	PP65		
U 8- 5	2947		
U 8- 6	PF2A		
U 8- 9	87AP		
U 8-10	low		
U 8-11	high		
U 8-12	465U		
U 8-15	5U64		
U 8-16	18UF		
U 8-19	1852		
U 8-20	high		
U 9- 1	low		Sheet 1
U 9- 2	CU5C		
U 9- 3	PP65		
U 9- 4	CUU5		
U 9- 5	2947		
U 9- 6	U86H		
U 9- 7	PF2A		
U 9- 8	P156		
U 9- 9	87AP		
U 9-10	low		
U 9-11	20A7		
U 9-12	465U		
U 9-13	4C23		
U 9-14	5U64		
U 9-15	8P4P		
U 9-16	18UF		
U 9-17	496F		
U 9-18	1852		
U 9-19	low		
U 9-20	high		
U 10- 1	high		Sheet 1
U 10- 2	PP65		
U 10- 5	2947		
U 10- 6	PF2A		
U 10- 9	87AP		
U 10-10	low		
U 10-11	high		
U 10-12	465U		
U 10-15	5U64		
U 10-16	18UF		
U 10-19	1852		
U 10-20	high		
U 11- 1	low		Sheet 1
U 11- 2	CU5C		
U 11- 3	PP65		
U 11- 4	CUU5		
U 11- 5	2947		
U 11- 6	U86H		
U 11- 7	PF2A		
U 11- 8	P156		
U 11- 9	87AP		
U 11-10	low		
U 11-11	20A7		

Signature Analysis Loop E

U 11-12	465U		
U 11-13	4C23		
U 11-14	5U64		
U 11-15	8P4P		
U 11-16	18UF		
U 11-17	496F		
U 11-18	1852		
U 11-19	low		
U 11-20	high		
U 12- 1	high		Sheet 1
U 12- 2	PP65		
U 12- 5	2947		
U 12- 6	PF2A		
U 12- 9	87AP		
U 12-10	low		
U 12-11	high		
U 12-12	465U		
U 12-15	5U64		
U 12-16	18UF		
U 12-19	1852		
U 12-20	high		
U 13- 1	low		Sheet 1
U 13- 2	CU5C		
U 13- 3	PP65		
U 13- 4	CUU5		
U 13- 5	2947		
U 13- 6	U86H		
U 13- 7	PF2A		
U 13- 8	P156		
U 13- 9	87AP		
U 13-10	low		
U 13-11	20A7		
U 13-12	465U		
U 13-13	4C23		
U 13-14	5U64		
U 13-15	8P4P		
U 13-16	18UF		
U 13-17	496F		
U 13-18	1852		
U 13-19	low		
U 13-20	high		
U 14- 1	high		Sheet 1
U 14- 2	PP65		
U 14- 5	2947		
U 14- 6	PF2A		
U 14- 9	87AP		
U 14-10	low		
U 14-11	high		
U 14-12	465U		
U 14-15	5U64		
U 14-16	18UF		
U 14-19	1852		
U 14-20	high		
U 15- 1	low		Sheet 1
U 15- 2	CU5C		
U 15- 3	PP65		
U 15- 4	CUU5		
U 15- 5	2947		
U 15- 6	U86H		
U 15- 7	PF2A		
U 15- 8	P156		
U 15- 9	87AP		
U 15-10	low		
U 15-11	20A7		
U 15-12	465U		
U 15-13	4C23		
U 15-14	5U64		
U 15-15	8P4P		
U 15-16	18UF		
U 15-17	496F		
U 15-18	1852		
U 15-19	low		
U 15-20	high		
U 16- 1	high		Sheet 1
U 16- 2	PP65		
U 16- 5	2947		
U 16- 6	PF2A		
U 16- 9	87AP		
U 16-10	low		
U 16-11	high		
U 16-12	465U		
U 16-15	5U64		
U 16-16	18UF		
U 16-19	1852		
U 16-20	high		
U 17- 1	low		Sheet 1
U 17- 2	CU5C		
U 17- 3	PP65		
U 17- 4	CUU5		
U 17- 5	2947		
U 17- 6	U86H		
U 17- 7	PF2A		
U 17- 8	P156		
U 17- 9	87AP		
U 17-10	low		
U 17-11	20A7		
U 17-12	465U		
U 17-13	4C23		
U 17-14	5U64		
U 17-15	8P4P		
U 17-16	18UF		
U 17-17	496F		
U 17-18	1852		
U 17-19	low		
U 17-20	high		
U 18- 1	high		Sheet 1
U 18- 2	PP65		
U 18- 5	2947		
U 18- 6	PF2A		
U 18- 9	87AP		
U 18-10	low		
U 18-11	high		
U 18-12	465U		
U 18-15	5U64		
U 18-16	18UF		
U 18-19	1852		
U 18-20	high		
U 19- 1	0000	ECL	Sheet 2, 3
U 19- 2	0000	ECL	
U 19- 3	high	ECL	
U 19- 4	high		
U 19- 5	high		
U 19- 7	0000	ECL	
U 19- 8	low	ECL	
U 19- 9	high	ECL	
U 19-10	0000	ECL	
U 19-11	F0F6	ECL	
U 19-12	F0F6		
U 19-13	high		
U 19-14	low	ECL	
U 19-15	A709	ECL	
U 19-16	high	ECL	
U 20- 1	high	ECL	Sheet 2
U 20- 2	A709	ECL	
U 20- 3	0000	ECL	
U 20- 4	low	ECL	
U 20- 5	0000	ECL	
U 20- 6	low	ECL	
U 20- 7	low	ECL	
U 20- 8	low	ECL	
U 20- 9	0000	ECL	
U 20-10	low	ECL	
U 20-11	low	ECL	
U 20-12	0000	ECL	
U 20-13	low	ECL	
U 20-14	0000	ECL	
U 20-15	A709	ECL	
U 20-16	high	ECL	
U 23- 1	high	ECL	Sheet 2
U 23- 2	0000	ECL	
U 23- 4	A709	ECL	
U 23- 5	0000	ECL	
U 23- 6	0000	ECL	
U 23- 7	A709	ECL	
U 23- 8	low	ECL	
U 23-12	0000	ECL	
U 23-13	A709	ECL	
U 23-14	high	ECL	
U 23-15	0000	ECL	
U 23-16	high	ECL	
U 24- 1	6HP8		Sheet 2, 3
U 24- 2	FAP1		
U 24- 3	low		
U 24- 4	low		
U 24- 5	high		
U 24- 6	high		
U 24- 7	low		
U 24- 8	high		
U 24- 9	high		
U 24-10	low		
U 24-11	H288		
U 24-12	high		
U 24-13	low		
U 24-14	high		
U 25- 1	high		Sheet 10
U 25- 2	high		
U 25- 3	high		
U 25- 4	high		
U 25- 5	3227		
U 25- 7	low		
U 25- 8	low		
U 25- 9	low		
U 25-10	high		
U 25-11	3227		
U 25-12	high		
U 25-15	high		
U 25-16	high		
U 26- 1	87AP		Sheet 4
U 26- 2	PF2A		
U 26- 3	2947		
U 26- 4	PP65		
U 26- 5	5U64		
U 26- 6	18UF		
U 26- 7	1852		

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U 26- 8	low	
U 26- 9	05HH	
U 26-10	1144	
U 26-11	2HP9	
U 26-12	A440	
U 26-13	P994	
U 26-14	5982	
U 26-15	A9P9	
U 26-16	2402	
U 26-17	high	
U 26-18	low	
U 26-19	low	
U 26-20	4H33	
U 26-21	465U	
U 26-22	high	
U 27- 1	87AP	Sheet 4
U 27- 2	PF2A	
U 27- 3	2947	
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U 27- 5	5U64	
U 27- 6	18UF	
U 27- 7	1852	
U 27- 8	low	
U 27- 9	021P	
U 27-10	1144	
U 27-11	P5H7	
U 27-12	A440	
U 27-13	176C	
U 27-14	5982	
U 27-15	H07A	
U 27-16	2402	
U 27-17	high	
U 27-18	low	
U 27-19	low	
U 27-20	4H33	
U 27-21	465U	
U 27-22	high	
U 28- 1	87AP	Sheet 4
U 28- 2	PF2A	
U 28- 3	2947	
U 28- 4	PP65	
U 28- 5	5U64	
U 28- 6	18UF	
U 28- 7	1852	
U 28- 8	low	
U 28- 9	HC46	
U 28-10	6810	
U 28-11	H4F8	
U 28-12	2864	
U 28-13	AUU3	
U 28-14	F013	
U 28-15	C9CH	
U 28-16	7A24	
U 28-17	high	
U 28-18	low	
U 28-19	low	
U 28-20	A5C7	
U 28-21	465U	
U 28-22	high	
U 29- 1	87AP	Sheet 4
U 29- 2	PF2A	
U 29- 3	2947	
U 29- 4	PP65	
U 29- 5	5U64	
U 29- 6	18UF	
U 29- 7	1852	
U 29- 8	low	
U 29- 9	05HH	
U 29-10	6810	
U 29-11	2HP9	
U 29-12	2864	
U 29-13	P994	
U 29-14	F013	
U 29-15	A9P9	
U 29-16	7A24	
U 29-17	high	
U 29-18	low	
U 29-19	low	
U 29-20	A5C7	
U 29-21	465U	
U 29-22	high	
U 30- 1	2947	Sheet 4
U 30- 2	PP65	
U 30- 3	low	
U 30- 4	low	
U 30- 5	low	
U 30- 6	7A24	
U 30- 7	465U	
U 30- 8	low	
U 30- 9	5U64	
U 30-10	18UF	
U 30-11	1852	
U 30-12	A5C7	
U 30-13	021P	
U 30-14	87AP	
U 30-15	PF2A	
U 30-16	high	
U 31- 1	87AP	Sheet 4
U 31- 2	PF2A	
U 31- 3	2947	
U 31- 4	PP65	
U 31- 5	5U64	
U 31- 6	18UF	
U 31- 7	1852	
U 31- 8	low	
U 31- 9	high	
U 31-10	A709	
U 31-11	P5H7	
U 31-12	6810	
U 31-13	176C	
U 31-14	2864	
U 31-15	H07A	
U 31-16	F013	
U 31-17	high	
U 31-18	low	
U 31-19	low	
U 31-20	A5C7	
U 31-21	465U	
U 31-22	high	
U 32- 1	87AP	Sheet 4
U 32- 2	PF2A	
U 32- 3	2947	
U 32- 4	PP65	
U 32- 5	5U64	
U 32- 6	18UF	
U 32- 7	1852	
U 32- 8	low	
U 32- 9	U311	
U 32-10	7A24	
U 32-11	25P8	
U 32-12	7A24	
U 32-13	CFAC	
U 32-14	7A24	
U 32-15	A9C8	
U 32-16	7A24	
U 32-17	high	
U 32-18	low	
U 32-19	low	
U 32-20	A5C7	
U 32-21	465U	
U 32-22	high	
U 33- 1	87AP	Sheet 4
U 33- 2	PF2A	
U 33- 3	2947	
U 33- 4	PP65	
U 33- 5	5U64	
U 33- 6	18UF	
U 33- 7	1852	
U 33- 8	low	
U 33- 9	U311	
U 33-10	1144	
U 33-11	25P8	
U 33-12	A440	
U 33-13	CFAC	
U 33-14	5982	
U 33-15	A9C8	
U 33-16	2402	
U 33-17	high	
U 33-18	low	
U 33-19	low	
U 33-20	4H33	
U 33-21	465U	
U 33-22	high	
U 34- 1	2947	Sheet 4
U 34- 2	PP65	
U 34- 3	low	
U 34- 4	low	
U 34- 5	low	
U 34- 6	2402	
U 34- 7	465U	
U 34- 8	low	
U 34- 9	5U64	
U 34-10	18UF	
U 34-11	1852	
U 34-12	4H33	
U 34-13	HC46	
U 34-14	87AP	
U 34-15	PF2A	
U 34-16	high	
U 36- 1	high	ECL Sheet 2
U 36- 2	high	ECL
U 36- 3	0000	ECL
U 36- 4	low	ECL
U 36- 5	0000	ECL
U 36- 6	low	ECL
U 36- 7	low	ECL
U 36- 8	low	ECL
U 36- 9	7581	ECL
U 36-10	low	ECL
U 36-11	low	ECL
U 36-12	0000	ECL
U 36-13	low	ECL
U 36-14	0000	ECL
U 36-15	A709	ECL
U 36-16	high	ECL
U 38- 1	high	ECL Sheet 9
U 38- 2	high	ECL
U 38- 3	low	ECL

Signature Analysis Loop E

U 38- 4	low	ECL	
U 38- 5	low	ECL	
U 38- 6	0000	ECL	
U 38- 7	high	ECL	
U 38- 8	low	ECL	
U 38- 9	low	ECL	
U 38-10	low	ECL	
U 38-11	low	ECL	
U 38-12	high	ECL	
U 38-13	low	ECL	
U 38-14	high	ECL	
U 38-15	low	ECL	
U 38-16	high	ECL	
U 39- 1	F0F6		Sheet 3
U 39- 2	low		
U 39- 3	high		
U 39- 4	high		
U 39- 5	04FA		
U 39- 6	A3F3		
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U 89- 7	low	
U 89- 8	low	
U 89-10	H6FU	
U 89-11	high	
U 89-12	A50F	
U 89-13	high	
U 89-14	590C	
U 89-15	3227	
U 89-16	high	
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U 91- 3	A3F3	
U 91- 4	2H78	
U 91- 5	1HF3	
U 91- 6	F03U	
U 91- 7	low	
U 91- 8	A3F3	
U 91- 9	2A3F	
U 91-10	1PF1	
U 91-11	A3F3	
U 91-12	8H35	
U 91-13	1A0C	
U 91-14	high	
U 92- 1	1A0C	Sheet 5, 9
U 92- 2	CH02	
U 92- 3	8H35	
U 92- 4	2A3F	
U 92- 6	0000	
U 92- 7	low	
U 92- 8	low	
U 92- 9	high	
U 92-10	low	
U 92-11	high	
U 92-12	7A24	
U 92-13	HH2H	
U 92-14	high	
U 93- 1	3227	Sheet 7
U 93- 2	A709	
U 93- 3	P156	
U 93- 4	U86H	
U 93- 5	CUU5	
U 93- 6	CU5C	
U 93- 7	3U5A	
U 93- 8	low	
U 93- 9	HH1U	
U 93-10	26AU	
U 93-11	F397	
U 93-12	6955	
U 93-13	C704	
U 93-14	6P05	
U 93-15	590C	
U 93-16	high	
U 94- 1	high	Sheet 7
U 94- 2	A709	
U 94- 3	05HH	
U 94- 4	2HP9	
U 94- 5	P994	
U 94- 6	A9P9	
U 94- 7	1HAA	
U 94- 8	low	
U 94- 9	6H9P	
U 94-10	6736	
U 94-11	H87U	
U 94-12	3F85	
U 94-13	9AU9	
U 94-14	F507	
U 94-15	54HH	
U 94-16	high	
U 95- 1	high	Sheet 7
U 95- 2	A709	
U 95- 3	021P	
U 95- 4	P5H7	
U 95- 5	176C	
U 95- 6	H07A	
U 95- 7	1HAA	
U 95- 8	low	
U 95- 9	6H9P	
U 95-10	54HH	
U 95-11	6C9H	
U 95-12	0FC2	
U 95-13	869U	
U 95-14	36HU	
U 95-15	2C79	
U 95-16	high	
U 96- 1	high	Sheet 4
U 96- 2	low	
U 96- 3	1144	
U 96- 4	low	
U 96- 5	A440	
U 96- 6	low	
U 96- 7	5982	
U 96- 8	low	
U 96- 9	2402	
U 96-10	low	
U 96-11	low	
U 96-12	1144	
U 96-13	low	
U 96-14	A440	
U 96-15	low	
U 96-16	5982	
U 96-17	low	
U 96-18	2402	
U 96-19	high	
U 96-20	high	
U 97- 1	6810	Sheet 5
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U 97- 3	2864	
U 97- 4	A440	
U 97- 5	A440	
U 97- 6	8U6H	
U 97- 7	low	
U 97- 8	671A	
U 97- 9	F013	
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U 97-14	high	
U 98- 1	F013	Sheet 5
U 98- 2	671A	
U 98- 3	671A	
U 98- 4	2864	
U 98- 5	8U6H	
U 98- 6	8U6H	
U 98- 7	low	
U 98- 8	HH2H	
U 98- 9	CH02	
U 98-10	5071	
U 98-11	FU19	
U 98-12	FU19	
U 98-13	6810	
U 98-14	high	
U 99- 1	6810	Sheet 5
U 99- 2	6810	
U 99- 3	2864	
U 99- 4	2864	
U 99- 5	A440	
U 99- 6	8U6H	
U 99- 7	low	
U 99- 8	671A	
U 99- 9	F013	
U 99-10	F013	
U 99-11	5982	
U 99-12	FU19	
U 99-13	1144	
U 99-14	high	
U100- 1	2402	Sheet 5
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U100- 3	5CH5	
U100- 4	HH2H	
U100- 5	HH2H	
U100- 6	UFHF	
U100- 7	low	
U100- 8	HH2H	
U100- 9	7A24	
U100-10	7A24	
U100-11	2402	
U100-12	HH2H	
U100-13	7A24	
U100-14	high	
U101- 1	7A24	Sheet 5
U101- 2	low	
U101- 3	low	
U101- 4	7A24	

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U101- 6	2402	
U101- 7	low	
U101- 8	5CH5	
U101- 9	2402	
U101-10	2402	
U101-11	2402	
U101-12	7A24	
U101-13	7A24	
U101-14	high	
U102- 1	2402	Sheet 5
U102- 2	low	
U102- 3	low	
U102- 4	7A24	
U102- 5	7A24	
U102- 6	2402	
U102- 7	low	
U102- 8	HH2H	
U102- 9	low	
U102-10	low	
U102-11	7A24	
U102-12	7A24	
U102-13	7A24	
U103- 1	high	Sheet 6
U103- 2	A709	
U103- 3	05HH	
U103- 4	2HP9	
U103- 5	P994	
U103- 6	A9P9	
U103- 7	2H78	
U103- 8	low	
U103- 9	4242	
U103-10	high	
U103-15	7P07	
U103-16	high	
U104- 1	high	Sheet 6
U104- 2	A709	
U104- 3	021P	
U104- 4	P5H7	
U104- 5	176C	
U104- 6	H07A	
U104- 7	2H78	
U104- 8	low	
U104- 9	4242	
U104-10	7P07	
U104-15	2FF5	
U104-16	high	
U106- 1	0HC8	Sheet 10
U106- 2	0CA4	
U106- 3	F758	
U106- 4	P2PH	
U106- 5	low	
U106- 6	A709	
U106- 7	high	
U106- 8	low	
U106- 9	high	
U106-10	high	
U106-11	high	
U106-12	6204	
U106-13	1812	
U106-14	56H9	
U106-15	692C	
U106-16	high	
U107- 1	0HC8	Sheet 10
U107- 2	0CA4	
U107- 3	F758	
U107- 4	0000	
U107- 5	A709	
U107- 6	P2PH	
U107- 7	A5C7	
U107- 8	low	
U107- 9	4H33	
U107-10	4242	
U107-11	6H9P	
U107-12	PFC7	
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U107-14	3227	
U107-15	8PA4	
U107-16	high	
U108- 1	high	Sheet 11
U108- 2	high	
U108- 3	HC46	
U108- 4	H4F8	
U108- 5	low	
U108- 6	high	
U108- 7	AUU3	
U108- 8	C9CH	
U108- 9	high	
U108-10	low	
U108-11	PFC7	
U108-12	low	
U108-13	A9C8	
U108-14	CFAC	
U108-15	low	
U108-16	low	
U108-17	25P8	
U108-18	U311	
U108-19	high	
U108-20	high	
U109- 1	high	Sheet 11
U109- 2	low	
U109- 3	05HH	
U109- 4	2HP9	
U109- 5	low	
U109- 6	low	
U109- 7	P994	
U109- 8	A9P9	
U109- 9	low	
U109-10	low	
U109-11	PFC7	
U109-12	8H35	
U109-13	021P	
U109-14	P5H7	
U109-15	low	
U109-16	low	
U109-17	176C	
U109-18	H07A	
U109-19	high	
U109-20	high	
U110- 1	low	Sheet 11
U110- 2	PP65	
U110- 3	CU5C	
U110- 4	2947	
U110- 5	CUU5	
U110- 7	U86H	
U110- 8	87AP	
U110- 9	P156	
U110-10	low	
U110-11	465U	
U110-12	20A7	
U110-13	5U64	
U110-14	4C23	
U110-15	18UF	
U110-16	8P4P	
U110-17	1852	
U110-18	496F	
U110-19	low	
U110-20	high	
U111- 1	low	Sheet 11
U111- 2	021P	
U111- 3	05HH	
U111- 4	P5H7	
U111- 5	2HP9	
U111- 6	176C	
U111- 7	P994	
U111- 8	H07A	
U111- 9	A9P9	
U111-10	low	
U111-11	A9P9	
U111-12	H07A	
U111-13	P994	
U111-14	176C	
U111-15	2HP9	
U111-16	P5H7	
U111-17	05HH	
U111-18	021P	
U111-19	low	
U111-20	high	
U112- 1	P2PH	Sheet 11
U112- 2	4110	
U112- 3	05HH	
U112- 4	97CA	
U112- 5	2HP9	
U112- 6	23P9	
U112- 7	P994	
U112- 8	50HF	
U112- 9	A9P9	
U112-10	low	
U112-11	5470	
U112-12	H07A	
U112-13	2AA9	
U112-14	176C	
U112-15	CH1C	
U112-16	P5H7	
U112-17	H39P	
U112-18	021P	
U112-19	P2PH	
U112-20	high	
U113- 1	low	Sheet 11
U113- 2	HC46	
U113- 3	U311	
U113- 4	H4F8	
U113- 5	25P8	
U113- 6	AUU3	
U113- 7	CFAC	
U113- 8	C9CH	
U113- 9	A9C8	
U113-10	low	
U113-11	A9C8	
U113-12	C9CH	
U113-13	CFAC	
U113-14	AUU3	
U113-15	25P8	
U113-16	H4F8	
U113-17	U311	
U113-18	HC46	

U113-19	low	
U113-20	high	
U114- 1	P2PH	Sheet 11
U114- 2	550A	
U114- 3	U311	
U114- 4	P54A	
U114- 5	25P8	
U114- 6	6U67	
U114- 7	CFAC	
U114- 8	0848	
U114- 9	A9C8	
U114-10	low	
U114-11	CCAA	
U114-12	C9CH	
U114-13	5U50	
U114-14	AUU3	
U114-15	PPCH	
U114-16	H4F8	
U114-17	80F7	
U114-18	HC46	
U114-19	P2PH	
U114-20	high	
U115- 1	A709	Sheet 7, 10
U115- 2	low	
U115- 3	U311	
U115- 4	A709	
U115- 5	low	
U115- 6	2HP9	
U115- 7	low	
U115- 8	A709	
U115- 9	3069	
U115-10	low	
U115-14	high	
U116- 1	45P4	Sheet 10, 11
U116- 2	P2PH	
U116- 3	high	
U116- 4	low	
U116- 5	7581	
U116- 6	H288	
U116- 7	low	
U116- 8	high	
U116- 9	low	
U116-10	high	
U116-11	low	
U116-12	2478	
U116-13	8371	
U116-14	high	

U117- 1	A709	Sheet 10
U117- 2	A709	
U117- 3	0000	
U117- 4	A709	
U117- 5	A709	
U117- 6	0000	
U117- 7	low	
U117- 8	F758	
U117- 9	0CA4	
U117-10	8371	
U117-11	P2PH	
U117-12	low	
U117-13	45P4	
U117-14	high	
U118- 1	high	Sheet 11
U118- 2	low	
U118- 4	low	
U118- 5	0000	
U118- 6	04FA	
U118- 7	high	
U118- 8	low	
U118- 9	high	
U118-10	9760	
U118-11	0000	
U118-12	low	
U118-14	low	
U118-15	high	
U118-16	high	
U119- 1	A709	Sheet 7, 10
U119- 2	45P4	
U119- 3	A709	
U119- 4	high	
U119- 5	45P4	
U119- 6	P2PH	
U119- 7	low	
U119- 8	high	
U119- 9	low	
U119-10	low	
U119-11	9457	
U119-12	HH1U	
U119-13	2478	
U119-14	high	
U121- 1	high	Sheet 6
U121- 2	A709	
U121- 3	U311	
U121- 4	25P8	
U121- 5	CFAC	

U121- 6	A9C8
U121- 7	2H78
U121- 8	low
U121- 9	4242
U121-10	2FF5
U121-15	H150
U121-16	high

* end of table *

Signature Analysis Loop F

Loop F signatures are valid while running IMB Internal Stimulus Tests.

Start = Positive edge of TP2 on the 64100A mainframe IO board, or TP5 on the 64110A mainframe CPU/IO board.

Stop = Negative edge of TP2 on the 64110A mainframe IO board, or TP5 on the 64110A mainframe CPU/IO board.

Clock = Negative edge of U117 pin 1 on the Wide Logic Analyzer.

Ground = Use a ground lead from probe to a ground point on the Wide Logic Analyzer.

Clock Qualifier = No qualified clocks are necessary.

ECL signatures require a 5005A Signature Analyzer:

To change from TTL to ECL --->
press the data threshold button three times.

To change from ECL to TTL --->
press the data threshold button five times.

High = indicates a solid HIGH on the node under test.
Low = indicates a solid LOW on the node under test.

All logic is positive logic.

Vh = 806F

Node	Signature		Schematic
U 1- 1	high	ECL	Sheet 3
U 1- 2	6982	ECL	
U 1- 3	P9PP	ECL	
U 1- 4	U394	ECL	
U 1- 5	low	ECL	
U 1- 6	6982	ECL	
U 1- 7	9C1H	ECL	
U 1- 8	low	ECL	
U 1- 9	9AH1	ECL	
U 1-10	U77P	ECL	
U 1-11	low	ECL	
U 1-12	U394	ECL	
U 1-13	low	ECL	
U 1-14	806F	ECL	
U 1-15	A018	ECL	
U 1-16	high	ECL	
U 3- 1	0001	ECL	Sheet 3
U 3- 2	UPC9	ECL	
U 3- 3	U77P	ECL	
U 3- 4	9C1H	ECL	
U 3- 8	low	ECL	
U 3-16	high	ECL	
U 4- 1	0001	ECL	Sheet 3
U 4- 2	806F	ECL	
U 4- 3	806F	ECL	
U 4- 4	UPC9	ECL	
U 4- 5	7PH5		
U 4- 6	high		
U 4- 7	0001		
U 4- 8	low	ECL	
U 4- 9	high	ECL	
U 4-10	1C71		
U 4-11	7712		
U 4-12	9C1H	ECL	
U 4-13	U77P	ECL	
U 4-14	806F	ECL	
U 4-15	806F	ECL	
U 4-16	high	ECL	
U 5- 1	9AH1		Sheets 2, 3
U 5- 2	9AH1		
U 5- 3	4A59		
U 5- 4	4A59		
U 5- 5	0F9P		
U 5- 6	7PH5		
U 5- 7	low		
U 5- 8	0F9P		
U 5- 9	high		
U 5-10	8FU2		
U 5-11	806F		
U 5-12	1ACH		
U 5-13	high		
U 5-14	high		
U 6- 1	5AUA		Sheets 7, 9
U 6- 2	low		
U 6- 4	low		
U 6- 5	low		
U 6- 7	low		
U 6-11	0F9P		
U 6-12	8FU2		
U 6-13	high		
U 6-14	high		
U 19- 1	0000	ECL	Sheets 2, 3
U 19- 2	0000	ECL	
U 19- 3	P9PP	ECL	
U 19- 4	P9PP		
U 19- 5	high		
U 19- 7	0000	ECL	
U 19- 8	low	ECL	
U 19- 9	high	ECL	
U 19-10	0000	ECL	
U 19-11	A018	ECL	
U 19-12	A018		
U 19-13	7PH5		
U 19-14	UPC9	ECL	
U 19-15	0000	ECL	
U 19-16	high	ECL	
U 20- 1	high	ECL	Sheet 2
U 20- 2	806F	ECL	
U 20- 3	0000	ECL	
U 20- 4	low	ECL	
U 20- 5	0000	ECL	
U 20- 6	low	ECL	
U 20- 7	low	ECL	
U 20- 8	low	ECL	
U 20- 9	0000	ECL	
U 20-10	low	ECL	
U 20-11	low	ECL	
U 20-12	0000	ECL	
U 20-13	low	ECL	
U 20-14	0000	ECL	
U 20-15	806F	ECL	
U 20-16	high	ECL	
U 23- 1	high	ECL	Sheet 2
U 23- 2	0000	ECL	
U 23- 4	806F	ECL	
U 23- 5	0000	ECL	
U 23- 6	0000	ECL	
U 23- 7	806F	ECL	
U 23- 8	low	ECL	
U 23-12	low	ECL	
U 23-13	806F	ECL	
U 23-14	high	ECL	
U 23-15	0000	ECL	
U 23-16	high	ECL	
U 24- 1	8FU2		Sheets 2, 3
U 24- 2	0F9P		
U 24- 3	UPC9		
U 24- 4	1U76		
U 24- 5	FC7H		
U 24- 6	P9PP		
U 24- 7	low		
U 24- 8	7PH5		
U 24- 9	FA35		
U 24-10	UPC9		
U 24-11	1ACH		
U 24-12	7F8A		
U 24-13	0001		
U 24-14	high		
U 39- 1	A018		Sheet 3
U 39- 2	507A		
U 39- 3	F637		
U 39- 4	F637		
U 39- 5	C639		
U 39- 6	700P		
U 39- 7	low		
U 39- 8	7712		
U 39- 9	U77P		
U 39-10	C639		

U 39-11	1C71	
U 39-12	5AUA	
U 39-13	40FU	
U 39-14	high	
U 41- 1	0F9P	Sheet 2
U 41- 2	0F9P	
U 41- 3	8FU2	
U 41- 4	8FU2	
U 41- 5	high	
U 41- 6	0F9P	
U 41- 7	low	
U 41- 8	8FU2	
U 41- 9	806F	
U 41-10	0F9P	
U 41-11	0F9P	
U 41-12	8FU2	
U 41-13	8FU2	
U 41-14	high	
U 55- 1	0F9P	Sheet 2
U 55- 2	0000	
U 55- 3	0000	
U 55- 4	806F	
U 55- 5	0000	
U 55- 6	0000	
U 55- 7	806F	
U 55- 8	low	
U 55- 9	9AH1	
U 55-10	1ACH	
U 55-11	0000	
U 55-12	9AH1	
U 55-13	1ACH	
U 55-14	0000	
U 55-15	low	
U 55-16	high	
U 59- 1	high	Sheets 1, 2
U 59- 2	8081	
U 59- 3	8081	
U 59- 4	5FC9	
U 59- 5	high	
U 59- 6	high	
U 59- 7	low	
U 59- 8	low	
U 59-10	0F9P	
U 59-11	high	
U 59-12	P53A	
U 59-13	8081	
U 59-14	8081	
U 59-15	high	
U 59-16	high	

U 61- 1	UP27	Sheets 7, 10
U 61- 2	A845	
U 61- 3	7P4C	
U 61- 4	22U8	
U 61- 5	low	
U 61- 6	high	
U 61- 7	low	
U 61- 8	high	
U 61- 9	low	
U 61-10	high	
U 61-11	high	
U 61-12	low	
U 61-13	low	
U 61-14	high	
U 71- 1	low	Sheets 5, 7
U 71- 2	7P4C	
U 71- 3	7P4C	
U 71- 4	73U8	
U 71- 5	low	
U 71- 6	73U8	
U 71- 7	low	
U 71- 8	73U8	
U 71- 9	low	
U 71-10	73U8	
U 71-11	U86P	
U 71-12	502C	
U 71-13	A845	
U 71-14	high	
U 72- 1	high	Sheet 7
U 72- 2	low	
U 72- 3	U86P	
U 72- 4	9AH1	
U 72- 5	73U8	
U 72- 6	HA96	
U 72- 7	5AUA	
U 72- 8	low	
U 72- 9	3655	
U 72-10	C639	
U 72-11	73U8	
U 72-12	9AH1	
U 72-13	A845	
U 72-14	low	
U 72-15	high	
U 72-16	high	
U 74- 1	14CF	Sheet 5
U 74- 2	1U76	
U 74- 3	HA96	
U 74- 4	7P4C	
U 74- 5	5CAH	

U 74- 6	14CF	
U 74- 7	low	
U 74- 8	A845	
U 74- 9	7P4C	
U 74-10	5CAH	
U 74-11	7P4C	
U 74-12	8535	
U 74-13	ACFU	
U 74-14	high	
U 77- 1	P457	Sheet 11
U 77- 2	low	
U 77- 3	0F9P	
U 77- 4	low	
U 77- 5	U155	
U 77- 6	low	
U 77- 7	34AH	
U 77- 8	5AUA	
U 77- 9	54UC	
U 77-10	low	
U 77-11	F637	
U 77-12	721U	
U 77-13	1U76	
U 77-14	806F	
U 77-15	3655	
U 77-16	806F	
U 77-17	8FU2	
U 77-18	806F	
U 77-19	P457	
U 77-20	high	
U 88- 1	high	Sheet 7
U 88- 2	low	
U 88- 3	high	
U 88- 4	9AH1	
U 88- 5	73U8	
U 88- 6	high	
U 88- 7	low	
U 88- 8	low	
U 88- 9	low	
U 88-11	73U8	
U 88-12	9AH1	
U 88-13	high	
U 88-14	low	
U 88-15	high	
U 88-16	high	
U 94- 1	high	Sheet 7
U 94- 2	806F	
U 94- 3	2683	
U 94- 4	4549	
U 94- 5	4549	

U 94- 6	4549	
U 94- 7	22U8	
U 94- 8	low	
U 94- 9	084F	
U 94-10	8FU2	
U 94-11	low	
U 94-12	low	
U 94-13	low	
U 94-14	low	
U 94-15	low	
U 94-16	high	
U 95- 1	high	Sheet 7
U 95- 2	806F	
U 95- 3	U71P	
U 95- 4	A95F	
U 95- 5	6U6C	
U 95- 6	6PF0	
U 95- 7	22U8	
U 95- 8	low	
U 95- 9	084F	
U 95-10	low	
U 95-11	low	
U 95-12	low	
U 95-13	low	
U 95-14	low	
U 95-15	low	
U 95-16	high	
U 98- 1	7P4C	Sheet 5
U 98- 2	UP27	
U 98- 3	UP27	
U 98- 4	7P4C	
U 98- 5	UP27	
U 98- 6	UP27	
U 98- 7	low	
U 98- 8	UP27	
U 98- 9	2CA3	
U 98-10	ACFU	
U 98-11	UP27	
U 98-12	UP27	
U 98-13	7P4C	
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U107- 1	9F73	Sheet 10
U107- 2	CPA5	
U107- 3	C4UH	
U107- 4	0000	
U107- 5	806F	
U107- 6	P457	
U107- 7	774P	
U107- 8	low	

Signature Analysis Loop F

U107- 9	0U83	
U107-10	F47F	
U107-11	084F	
U107-12	5FC9	
U107-13	9AH1	
U107-14	73U8	
U107-15	P53A	
U107-16	high	
U108- 1	high	Sheet 11
U108- 2	FC7H	
U108- 3	01C2	
U108- 4	81C3	
U108- 5	40FU	
U108- 6	C06U	
U108- 7	CUPH	
U108- 8	PUP8	
U108- 9	7F8A	
U108-10	low	
U108-11	5FC9	
U108-12	U77P	
U108-13	F611	
U108-14	22U9	
U108-15	507A	
U108-16	4A59	
U108-17	U76A	
U108-18	2CCU	
U108-19	FA35	
U108-20	high	
U109- 1	high	Sheet 11
U109- 2	low	
U109- 3	2683	
U109- 4	4549	
U109- 5	low	
U109- 6	low	
U109- 7	4549	
U109- 8	4549	
U109- 9	low	
U109-10	low	
U109-11	5FC9	
U109-12	1HH0	
U109-13	U71P	
U109-14	A95F	
U109-15	low	
U109-16	low	
U109-17	6U6C	
U109-18	6PF0	
U109-19	high	
U109-20	high	
U111- 1	low	Sheet 11
U111- 2	U71P	
U111- 3	2683	
U111- 4	A95F	
U111- 5	4549	
U111- 6	6U6C	
U111- 7	4549	
U111- 8	6PF0	
U111- 9	4549	
U111-10	low	
U111-11	4549	
U111-12	6PF0	
U111-13	4549	
U111-14	6U6C	
U111-15	4549	
U111-16	A95F	
U111-17	2683	
U111-18	U71P	
U111-19	low	
U111-20	high	
U112- 1	P457	Sheet 11
U112- 2	54UC	
U112- 3	2683	
U112- 4	34AH	
U112- 5	4549	
U112- 6	U155	
U112- 7	4549	
U112- 8	0F9P	
U112- 9	4549	
U112-10	low	
U112-11	806F	
U112-12	6PF0	
U112-13	806F	
U112-14	6U6C	
U112-15	806F	
U112-16	A95F	
U112-17	721U	
U112-18	U71P	
U112-19	P457	
U112-20	high	
U113- 1	low	Sheet 11
U113- 2	01C2	
U113- 3	2CCU	
U113- 4	81C3	
U113- 5	U76A	
U113- 6	CUPH	
U113- 7	22U9	
U113- 8	PUP8	
U113- 9	F611	
U113-10	low	
U113-11	F611	
U113-12	PUP8	
U113-13	22U9	
U113-14	CUPH	
U113-15	U76A	
U113-16	81C3	
U113-17	2CCU	
U113-18	01C2	
U113-19	low	
U113-20	high	
U115- 1	806F	Sheet 7,8
U115- 2	low	
U115- 3	2CCU	
U115- 4	806F	
U115- 5	low	
U115- 6	4549	
U115- 7	low	
U115- 8	high	
U115- 9	low	
U115-10	low	
U115-14	high	
U117- 1	806F	Sheet 10
U117- 2	806F	
U117- 3	0000	
U117- 4	806F	
U117- 5	806F	
U117- 6	0000	
U117- 7	low	
U117- 8	C4UH	
U117- 9	CPA5	
U117-10	U2U9	
U117-11	P457	
U117-12	low	
U117-13	643C	
U117-14	high	

* end of table *

SALES & SUPPORT OFFICES

Arranged alphabetically by country

Product Line Sales/Support Key

Key	Product Line
A	Analytical
CM	Components
C	Computer Systems Sales only
CH	Computer Systems Hardware Sales and Services
CS	Computer Systems Software Sales and Services
E	Electronic Instruments & Measurement Systems
M	Medical Products
MP	Medical Products Primary SRO
MS	Medical Products Secondary SRO
P	Personal Computation Products
*	Sales only for specific product line
**	Support only for specific product line

IMPORTANT: These symbols designate general product line capability. They do not insure sales or support availability for all products within a line, at all locations. Contact your local sales office for information regarding locations where HP support is available for specific products.

HP distributors are printed in italics.

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R. Barbosa Rodrigues, 41-I DT.
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LUANDA
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E,M,P

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Avenida Santa Fe 2035
Martinez 1640 **BUENOS AIRES**
Tel: 798-5735, 792-1293
Telex: 17595 BIONAR
Cable: HEWPACKARG
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Biotron S.A.C.I.M. e I.
Av Paseo Colon 221, Piso 9
1399 BUENOS AIRES
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M

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Hewlett-Packard Australia Ltd.
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PARKSIDE, S.A. 5063
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Hewlett-Packard Australia Ltd.
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Telex: 42133
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121 Wollongong Street
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CLAREMONT, W.A. 6010
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NORTH RYDE, N.S.W. 2113
Tel: 887-1611
Telex: 21561
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Verkaufsburo Graz
A-8052 **GRAZ**
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Telex: 32375
CH,E*

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P.O. Box 72
A-1222 **VIENNA**
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Telex: 134425 HEPA A
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Green Salon
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BAHRAIN
Tel: 255503-255950
Telex: 84419
P

Wael Pharmacy
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Tel: 256123
Telex: 8550 WAEL BN
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Hewlett-Packard do Brasil I.e.C. Ltda.
Avenida Epitacio Pessoa, 4664
22471 **RIO DE JANEIRO-RJ**
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Arturo Buhrle 065
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CHINA, People's Republic of

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Telex: 22601 CTSHP CN
Cable: 1920
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Cable: AARIS Bogota
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San Pedro de Montes de Oca
Apartado 10159
SAN JOSÉ
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Arroyo Hondo
SANTO DOMINGO
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Telex: 2548 CYEDE ED
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Robles 625
Casilla 3590
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Kasr-el-Aini
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Informatic For Systems
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Telex: 93337 EGPOR
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SAN SALVADOR
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2

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Arranged alphabetically by country

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Herrenberger Strasse 110
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A,CH,CM,CS,E,M,P

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Tel: 36-11-160
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GUATEMALA

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A,CH,CM,CS,E,M,P

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E,CH,CS,P

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Telex: 85148 CET HX
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Schmidt & Co. (Hong Kong) Ltd.
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Connaught Road, C.
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Elding Trading Company Inc.
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IS-REYKJAVIK
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M

INDIA

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***BOMBAY** 400 025*
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***CALCUTTA** 700 001*
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Telex: 021-7655
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A,M

Blue Star Ltd.
133 Kodambakkam High Road
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Telex: 041-379
Cable: BLUESTAR
A,M

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Bhandari House, 7th/8th Floors
91 Nehru Place
***NEW DELHI** 110 024*
Tel: 682547
Telex: 031-2463
Cable: BLUESTAR
A,CH,CM,CS*,E,M*

Blue Star Ltd.
15/16:C Wellesley Rd.
***PUNE** 411 011*
Tel: 22775
Cable: BLUE STAR
A

Blue Star Ltd.
2-2-47/1108 Bolarum Rd.
***SECUNDERABAD** 500 003*
Tel: 72057
Telex: 0155-459
Cable: BLUEFROST
A,E

Blue Star Ltd.
T.C. 7/603 Poornima
Maruthankuzhi
***TRIVANDRUM** 695 013*
Tel: 65799
Telex: 0884-259
Cable: BLUESTAR
E

Computer Maintenance Corporation Ltd.
115, Sarojini Devi Road
***SECUNDERABAD** 500 003*
Tel: 310-184, 345-774
Telex: 031-2960
*CH***

INDONESIA

BERCA Indonesia P.T.
P.O.Box 496/JKT.
Jl. Abdul Muis 62
JAKARTA
Tel: 373009
Telex: 46748 BERSAL IA
Cable: BERSAL JAKARTA
P

BERCA Indonesia P.T.
P.O.Box 2497/Jkt Antara Bldg.,
17th Floor
Jl. Medan Merdeka Selatan 17
JAKARTA-PUSAT
Tel: 21-344-181
Telex: BERSAL IA
A,CS,E,M

BERCA Indonesia P.T.
P.O. Box 174/SBY.
Jl. Kutei No. 11
SURABAYA
Tel: 68172
Telex: 31146 BERSAL SB
Cable: BERSAL-SURABAYA
A,E,M,P*

IRAQ

Hewlett-Packard Trading S.A.
Service Operation
Al Mansoor City 9B/3/7
BAGHDAD
Tel: 551-49-73
Telex: 212-455 HEPAIRAQ IK
CH,CS

SALES & SUPPORT OFFICES

Arranged alphabetically by country

IRELAND

Hewlett-Packard Ireland Ltd.
82/83 Lower Leeson Street
DUBLIN 2
Tel: (1) 60 88 00
Telex: 30439
A,CH,CM,CS,E,M,P

Cardiac Services Ltd.
Kilmore Road
Artane
DUBLIN 5
Tel: (01) 351820
Telex: 30439
M

ISRAEL

Eldan Electronic Instrument Ltd.
P.O.Box 1270
***JERUSALEM** 91000*
16, Ohaliav St.
***JERUSALEM** 94467*
Tel: 533 221, 553 242
Telex: 25231 AB/PAKRD IL
A

Electronics Engineering Division
Motorola Israel Ltd.
16 Kremenetski Street
P.O. Box 25016
TEL-AVIV 67899
Tel: 3-338973
Telex: 33569 Motil IL
Cable: BASTEL Tel-Aviv
CH,CM,CS,E,M,P

ITALY

Hewlett-Packard Italiana S.p.A
Traversa 99C
Via Giulio Petroni, 19
I-70124 **BARI**
Tel: (080) 41-07-44
M

Hewlett-Packard Italiana S.p.A.
Via Martin Luther King, 38/111
I-40132 **BOLOGNA**
Tel: (051) 402394
Telex: 511630
CH,E,MS

Hewlett-Packard Italiana S.p.A.
Via Principe Nicola 43G/C
I-95126 **CATANIA**
Tel: (095) 37-10-87
Telex: 970291
C,P

Hewlett-Packard Italiana S.p.A.
Via G. Di Vittorio 9
I-20063 **CERNUSCO SUL NAVIGLIO**
Tel: (2) 903691
Telex: 334632
A,CH,CM,CS,E,MP,P

Hewlett-Packard Italiana S.p.A.
Via Nuova San Rocco a
Capodimonte, 62/A
I-80131 **NAPLES**
Tel: (081) 7413544
Telex: 710698
A,CH,E

Hewlett-Packard Italiana S.p.A.
Viale G. Modugno 33
I-16156 **GENOVA PEGLI**
Tel: (010) 68-37-07
Telex: 215238
E,C

Hewlett-Packard Italiana S.p.A.
Via Turazza 14
I-35100 **PADOVA**
Tel: (049) 664888
Telex: 430315
A,CH,E,MS

Hewlett-Packard Italiana S.p.A.
Viale C. Pavese 340
I-00144 **ROMA**
Tel: (06) 54831
Telex: 610514
A,CH,CM,CS,E,MS,P*

Hewlett-Packard Italiana S.p.A.
Corso Svizzera, 184
I-10149 **TORINO**
Tel: (011) 74 4044
Telex: 221079
CH,E

JAPAN

Yokogawa-Hewlett-Packard Ltd.
152-1, Onna
000 **ATSUGI,** Kanagawa, 243
Tel: (0462) 28-0451
CM,C*,E

Yokogawa-Hewlett-Packard Ltd.
Towa Building
2-3, Kaigan-dori, 2 Chome Chuo-ku
KOBE, 650
Tel: (078) 392-4791
C,E

Yokogawa-Hewlett-Packard Ltd.
Kumagaya Asahi 82 Bldg
3-4 Tsukuba
KUMAGAYA, Saitama 360
Tel: (0485) 24-6563
CH,CM,E

Yokogawa-Hewlett-Packard Ltd.
Asahi Shinbun Daiichi Seimei Bldg.
4-7, Hanabata-cho
KUMAMOTO,860
Tel: (0963) 54-7311
CH,E

Yokogawa-Hewlett-Packard Ltd.
Shin-Kyoto Center Bldg.
614, Higashi-Shiokoji-cho
Karasuma-Nishiiru
Shiokoji-dori, Shimogyo-ku
KYOTO, 600
Tel: 075-343-0921
CH,E

Yokogawa-Hewlett-Packard Ltd.
Mito Mitsui Bldg
4-73, Sannomaru, 1 Chome
MITO, Ibaragi 310
Tel: (0292) 25-7470
CH,CM,E

Yokogawa-Hewlett-Packard Ltd.
Sumitomo Seimei 14-9 Bldg.
Meieki-Minami, 2 Chome
Nakamura-ku
NAGOYA, 450
Tel: (052) 571-5171
CH,CM,CS,E,MS

Yokogawa-Hewlett-Packard Ltd.
Chuo Bldg.,
4-20 Nishinakajima, 5 Chome
Yodogawa-ku
OSAKA, 532
Tel: (06) 304-6021
Telex: YHPOSA 523-3624
A,CH,CM,CS,E,MP,P*

Yokogawa-Hewlett-Packard Ltd.
27-15, Yabe, 1 Chome
SAGAMIHARA Kanagawa, 229
Tel: 0427 59-1311

Yokogawa-Hewlett-Packard Ltd.
Daiichi Seimei Bldg.
7-1, Nishi Shinjuku, 2 Chome
Shinjuku-ku,**TOKYO** 160
Tel: 03-348-4611-5
CH,E

Yokogawa-Hewlett-Packard Ltd.
29-21 Takaido-Higashi, 3 Chome
Suginami-ku **TOKYO** 168
Tel: (03) 331-6111
Telex: 232-2024 YHPTOK
A,CH,CM,CS,E,MP,P*

Yokogawa-Hewlett-Packard Ltd.
Daiichi Asano Building
2-8, Odori, 5 Chome
UTSUNOMIYA, Tochigi 320
Tel: (0286) 25-7155
CH,CS,E

Yokogawa-Hewlett-Packard Ltd.
Yasuda Seimei Nishiguchi Bldg.
30-4 Tsuruya-cho, 3 Chome
YOKOHAMA221
Tel: (045) 312-1252
CH,CM,E

JORDAN

Mouasher Cousins Company
P.O. Box 1387
AMMAN
Tel: 24907, 39907
Telex: 21456 SABCO JO
CH,E,M,P

KENYA

ADCOM Ltd., Inc., Kenya
P.O.Box 30070
NAIROBI
Tel: 331955
Telex: 22639
E,M

KOREA

Samsung Electronics Computer Division
76-561 Yeoksam-Dong
Kwangnam-Ku
C.P.O. Box 2775
SEOUL
Tel: 555-7555, 555-5447
Telex: K27364 SAMSAN
A,CH,CM,CS,E,M,P

KUWAIT

Al-Khaldiya Trading & Contracting
P.O. Box 830 Safat
KUWAIT
Tel: 42-4910, 41-1726
Telex: 22481 Areeg kt
CH,E,M

Photo & Cine Equipment
P.O. Box 270 Safat
KUWAIT
Tel: 42-2846, 42-3801
Telex: 22247 Matin kt
P

LEBANON

G.M. Dolmadjian
Achrafieh
P.O. Box 165.167
BEIRUT
Tel: 290293
*MP**

LUXEMBOURG

Hewlett-Packard Belgium S.A./N.V.
Blvd de la Woluwe, 100
Woluwedal
B-1200 **BRUSSELS**
Tel: (02) 762-32-00
Telex: 23-494 paloben bru
A,CH,CM,CS,E,MP,P

MALAYSIA

Hewlett-Packard Sales (Malaysia)
Sdn. Bhd.
1st Floor, Bangunan British
American
Jalan Semantan, Damansara Heights
KUALA LUMPUR 23-03
Tel: 943022
Telex: MA31011
A,CH,E,M,P*

Protel Engineering
P.O.Box 1917
Lot 6624, Section 64
23/4 Pending Road
Kuching, SARAWAK
Tel: 36299
Telex: MA 70904 PROTEL
Cable: PROTELENG
A,E,M

MALTA

Philip Toledo Ltd.
Notabile Rd.
MRIEHEL
Tel: 447 47, 455 66
Telex: Media MW 649
P

MEXICO

Hewlett-Packard Mexicana, S.A.
de C.V.
Av. Periferico Sur No. 6501
Tepepan, Xochimilco
MEXICO D.F. 16020
Tel: 676-4600
Telex: 17-74-507 HEWPACK MEX
A,CH,CS,E,MS,P

Hewlett-Packard Mexicana, S.A.
de C.V.
Ave. Colonia del Valle #409
Col. del Valle
Municipio de Garza Garcia
MONTERREY, N.L.
Tel: 78 42 41
Telex: 038 410
CH

ECISA
José Vasconcelos No. 218
Col. Condesa Deleg. Cuauhtémoc
***MEXICO** D.F. 06140*
Tel: 553-1206
Telex: 17-72755 ECE ME
M

MOROCCO

Dolbeau
81 rue Karatchi
CASABLANCA
Tel: 3041-82, 3068-38
Telex: 23051, 22822
E

Gerep
2 rue d'Agadir
Boite Postale 156
CASABLANCA
Tel: 272093, 272095
Telex: 23 739
P

NETHERLANDS

Hewlett-Packard Nederland B.V.
Van Heuven Goedhartlaan 121
NL 1181KK **AMSTELVEEN**
P.O. Box 667
NL1180 AR **AMSTELVEEN**
Tel: (020) 47-20-21
Telex: 13 216 HEPA NL
A,CH,CM,CS,E,MP,P

Hewlett-Packard Nederland B.V.
Bongerd 2
NL 2906VK **CAPELLE, A/D IJSSEL**
P.O. Box 41
NL 2900AA **CAPELLE, A/D IJSSEL**
Tel: (10) 51-64-44
Telex: 21261 HEPAC NL
A,CH,CS,E

NEW ZEALAND

Hewlett-Packard (N.Z.) Ltd.
169 Manukau Road
P.O. Box 26-189
Epsom, **AUCKLAND**
Tel: 687-159
Cable: HEWPACK Auckland
CH,CM,E,P*

Hewlett-Packard (N.Z.) Ltd.
4-12 Cruickshank Street
Kilbirnie, **WELLINGTON 3**
P.O. Box 9443
Courtenay Place, **WELLINGTON 3**
Tel: 877-199
Cable: HEWPACK Wellington
CH,CM,E,P

Northrop Instruments & Systems Ltd.
369 Khyber Pass Road
P.O. Box 8602
AUCKLAND
Tel: 794-091
Telex: 60605
A,M

Northrop Instruments & Systems Ltd.
110 Mandeville St.
P.O. Box 8388
CHRISTCHURCH
Tel: 486-928
Telex: 4203
A,M

Northrop Instruments & Systems Ltd.
Sturdee House
85-87 Ghuznee Street
P.O. Box 2406
WELLINGTON
Tel: 850-091
Telex: NZ 3380
A,M

NORTHERN IRELAND

See United Kingdom

NORWAY

Hewlett-Packard Norge A/S
Folke Bernadottes vei 50
P.O. Box 3558
N-5033 **FYLLINGSDALEN** (Bergen)
Tel: (05) 16-55-40
Telex: 16621 hpnas n
CH,CS,E,MS

Hewlett-Packard Norge A/S
Österndalen 18
P.O. Box 34
N-1345 **ÖSTERÅS**
Tel: (02) 17-11-80
Telex: 16621 hpnas n
A,CH,CM,CS,E,M,P

OMAN

Khimjil Ramdas
P.O. Box 19
MUSCAT
Tel: 722225, 745601
Telex: 3289 BROKER MB MUSCAT
P

Suhail & Saud Bahwan
P.O.Box 169
MUSCAT
Tel: 734 201-3
Telex: 3274 BAHWAN MB

PAKISTAN

Mushko & Company Ltd.
1-B, Street 43
Sector F-8/1
ISLAMABAD
Tel: 26875
Cable: FEMUS Rawalpindi
A,E,M

Mushko & Company Ltd.
Oosman Chambers
Abdullah Haroon Road
***KARACHI** 0302*
Tel: 524131, 524132
Telex: 2894 MUSKO PK
Cable: COOPERATOR Karachi
*A,E,M,P**

PANAMA

Electrónico Balboa, S.A.
Calle Samuel Lewis, Ed. Alfa
Apartado 4929
PANAMA 5
Tel: 64-2700
Telex: 3483 ELECTRON PG
A,CM,E,M,P

4 SALES & SUPPORT OFFICES

Arranged alphabetically by country

PERU
Cía Electro Médica S.A.
Los Flamencos 145, San Isidro
Casilla 1030
***LIMA** 1*
Tel: 41-4325, 41-3703
Telex: Pub. Booth 25306
CM,E,M,P

PHILIPPINES
The Online Advanced Systems Corporation
Rico House, Amorsolo Cor. Herrera Street
Legaspi Village, Makati
P.O. Box 1510
*Metro **MANILA***
Tel: 85-35-81, 85-34-91, 85-32-21
Telex: 3274 ONLINE
A,CH,CS,E,M

Electronic Specialists and Proponents Inc.
690-B Epifanio de los Santos Avenue
*Cubao, **QUEZON CITY***
P.O. Box 2649 Manila
Tel: 98-96-81, 98-96-82, 98-96-83
Telex: 40018, 42000 ITT GLOBE MACKAY BOOTH
P

PORTUGAL
Mundinter
Intercambio Mundial de Comércio S.A.R.L.
P.O. Box 2761
Avenida Antonio Augusto de Aguiar 138
P-LISBON
Tel: (19) 53-21-31, 53-21-37
Telex: 16691 munter p
M

Soquimica
Av. da Liberdade, 220-2
*1298 **LISBOA** Codex*
Tel: 56 21 81/2/3
Telex: 13316 SABASA
P

Telectra-Empresa Técnica de Equipmentos Eléctricos S.A.R.L.
Rua Rodrigo da Fonseca 103
P.O. Box 2531
***P-LISBON** 1*
Tel: (19) 68-60-72
Telex: 12598
CH,CS,E,P

PUERTO RICO
Hewlett-Packard Puerto Rico
P.O. Box 4407
CAROLINA, Puerto Rico 00628
Calle 272 Edificio 203
Urb. Country Club
RIO PIEDRAS, Puerto Rico
Tel: (809) 762-7255
A,CH,CS

QATAR
Computearbia
P.O. Box 2750
DOHA
Tel: 883555
Telex: 4806 CHPARB
P

Eastern Technical Services
P.O.Box 4747
DOHA
Tel: 329 993
Telex: 4156 EASTEC DH

Nasser Trading & Contracting
P.O.Box 1563
DOHA
Tel: 22170, 23539
Telex: 4439 NASSER DH
M

SAUDI ARABIA
Modern Electronic Establishment
Hewlett-Packard Division
P.O. Box 281
Thuobah
AL-KHOBAR
Tel: 864-46 78
Telex: 671 106 HPMEEK SJ
Cable: ELECTA AL-KHOBAR
CH,CS,E,M,P

Modern Electronic Establishment
Hewlett-Packard Division
P.O. Box 1228
Redec Plaza, 6th Floor
JEDDAH
Tel: 644 38 48
Telex: 4027 12 FARNAS SJ
Cable: ELECTA JEDDAH
CH,CS,E,M,P

Modern Electronic Establishment
Hewlett-Packard Division
P.O.Box 2728
RIYADH
Tel: 491-97 15, 491-63 87
Telex: 202049 MEERYD SJ
CH,CS,E,M,P

SCOTLAND
See United Kingdom

SINGAPORE
Hewlett-Packard Singapore (Sales) Pte. Ltd.
P.O. Box 58 Alexandra Post Office
SINGAPORE, 9115
6th Floor, Inchcape House
450-452 Alexandra Road
SINGAPORE 0511
Tel: 631788
Telex: HPSGSO RS 34209
Cable: HEWPACK, Singapore
A,CH,CS,E,MS,P

Dynamar International Ltd.
Unit 05-11 Block 6
Kolam Ayer Industrial Estate
***SINGAPORE** 1334*
Tel: 747-6188
Telex: RS 26283
CM

SOUTH AFRICA
Hewlett-Packard So Africa (Pty.) Ltd.
P.O. Box 120
Howard Place **CAPE PROVINCE** 7450
Pine Park Center, Forest Drive, Pinelands
CAPE PROVINCE 7405
Tel: 53-7954
Telex: 57-20006
A,CH,CM,E,MS,P

Hewlett-Packard So Africa (Pty.) Ltd.
P.O. Box 37099
92 Overport Drive
DURBAN 4067
Tel: 28-4178, 28-4179, 28-4110
Telex: 6-22954
CH,CM

Hewlett-Packard So Africa (Pty.) Ltd.
6 Linton Arcade
511 Cape Road
Linton Grange
PORT ELIZABETH 6001
Tel: 041-302148
CH

Hewlett-Packard So Africa (Pty.) Ltd. P.O.Box 33345
Glenstantia 0010 **TRANSVAAL**
1st Floor East
Constantia Park Ridge Shopping Centre
Constantia Park
PRETORIA
Tel: 982043
Telex: 32163
CH,E

Hewlett-Packard So Africa (Pty.) Ltd.
Private Bag Wendywood
SANDTON 2144
Tel: 802-5111, 802-5125
Telex: 4-20877
Cable: HEWPACK Johannesburg
A,CH,CM,CS,E,MS,P

SPAIN
Hewlett-Packard Española S.A.
Calle Entenza, 321
E-BARCELONA 29
Tel: 322.24.51, 321.73.54
Telex: 52603 hpbee
A,CH,CS,E,MS,P

Hewlett-Packard Española S.A.
Calle San Vicente S/No
Edificio Albia II
E-BILBAO 1
Tel: 423.83.06
A,CH,E,MS

Hewlett-Packard Española S.A.
Crta. de la Coruña, Km. 16, 400
Las Rozas
E-MADRID
Tel: (1) 637.00.11

CH,CS,M

Hewlett-Packard Española S.A.
Avda. S. Francisco Javier, S/no
Planta 10. Edificio Sevilla 2,
E-SEVILLA 5
Tel: 64.44.54
Telex: 72933
A,CS,MS,P

Hewlett-Packard Española S.A.
Calle Ramon Gordillo, 1 (Entlo.3)
E-VALENCIA 10
Tel: 361-1354
CH,P

SWEDEN
Hewlett-Packard Sverige AB
Sunnanvagen 14K
S-22226 **LUND**
Tel: (046) 13-69-79
Telex: (854) 17886 (via Spånga office)
CH

Hewlett-Packard Sverige AB
Vastra Vintergatan 9
S-70344 **OREBRO**
Tel: (19) 10-48-80
Telex: (854) 17886 (via Spånga office)
CH

Hewlett-Packard Sverige AB
Skalholtsgatan 9, Kista
Box 19
S-16393 **SPÅNGA**
Tel: (08) 750-2000
Telex: (854) 17886
A,CH,CM,CS,E,MS,P

Hewlett-Packard Sverige AB
Frötallisgatan 30
S-42132 **VÄSTRA-FRÖLUNDA**
Tel: (031) 49-09-50
Telex: (854) 17886 (via Spånga office)
CH,E,P

SWITZERLAND
Hewlett-Packard (Schweiz) AG
Clarastrasse 12
CH-4058 **BASLE**
Tel: (61) 33-59-20
A

Hewlett-Packard (Schweiz) AG
7, rue du Bois-du-Lan
Case Postale 365
CH-1217 **MEYRIN** 1
Tel: (0041) 22-83-11-11
Telex:27333 HPAG CH
CH,CM,CS

Hewlett-Packard (Schweiz) AG
Allmend 2
CH-8967 **WIDEN**
Tel: (0041) 57 31 21 11
Telex: 53933 hpag ch
Cable: HPAG CH
A,CH,CM,CS,E,MS,P

SYRIA
General Electronic Inc.
Nuri Basha P.O. Box 5781
DAMASCUS
Tel: 33-24-87
Telex: 11216 ITIKAL SY
Cable: ELECTROBOR DAMASCUS
E

Middle East Electronics
Place Azmé
P.O.Box 2308
DAMASCUS
Tel: 334592
Telex: 11304 SATACO SY
M,P

TAIWAN
Hewlett-Packard Far East Ltd.
Kaohsiung Office
2/F 68-2, Chung Cheng 3rd Road
KAOHSIUNG
Tel: 241-2318, 261-3253
CH,CS,E

Hewlett-Packard Far East Ltd.
Taiwan Branch
5th Floor
205 Tun Hwa North Road
TAIPEI
Tel: (02) 712-0404
Cable:HEWPACK Taipei
A,CH,CM,CS,E,M,P

Ing Lih Trading Co.
3rd Floor, 7 Jen-Ai Road, Sec. 2
TAIPEI 100
Tel: (02) 3948191
Cable: INGLIH TAIPEI
A

THAILAND
Unimesa
30 Patpong Ave., Suriwong
***BANGKOK** 5*
Tel: 235-5727
Telex: 84439 Simonco TH
Cable: UNIMESA Bangkok
A,CH,CS,E,M

Bangkok Business Equipment Ltd.
5/5-6 Dejo Road
BANGKOK
Tel: 234-8670, 234-8671
Telex: 87669-BEQUIPT TH
Cable: BUSIQUIPT Bangkok
P

TRINIDAD & TOBAGO
Caribbean Telecoms Ltd.
50/A Jerningham Avenue
P.O. Box 732
PORT-OF-SPAIN
Tel: 62-44213, 62-44214
Telex: 235,272 HUGCO WG
CM,E,M,P

TUNISIA
Tunisie Electronique
31 Avenue de la Liberte
TUNIS
Tel: 280-144
E,P

Corema
1 ter. Av. de Carthage
TUNIS
Tel: 253-821
Telex: 12319 CABAM TN
M

TURKEY
Teknim Company Ltd.
Iran Caddesi No. 7
*Kavaklidere, **ANKARA***
Tel: 275800
Telex: 42155 TKNM TR
E

E.M.A.
Medina Eldem Sokak No.41/6
Yuksel Caddesi
ANKARA
Tel: 175 622
M

UNITED ARAB EMIRATES
Emitac Ltd.
P.O. Box 1641
SHARJAH
Tel: 354121, 354123
Telex: 68136 Emitac Sh
CH,CS,E,M,P

UNITED KINGDOM

GREAT BRITAIN
Hewlett-Packard Ltd.
Trafalgar House
Navigation Road
ALTRINCHAM
Chesire WA14 1NU
Tel: (061) 928-6422
Telex: 668068
A,CH,CS,E,M

Hewlett-Packard Ltd.
Oakfield House, Oakfield Grove
Clifton
BRISTOL BS8 2BN, Avon
Tel: (027) 38606
Telex: 444302
CH,M,P

SALES & SUPPORT OFFICES

Arranged alphabetically by country

GREAT BRITAIN (Cont'd)

Hewlett-Packard Ltd.
Fourier House
257-263 High Street
LONDON COLNEY
Herts., AL2 1HA, St. Albans
Tel: (0727) 24400
Telex: 1-8952716
CH,CS,E

Hewlett-Packard Ltd.
Quadrangle
106-118 Station Road
REDHILL, Surrey
Tel: (0737) 68655
Telex: 947234
CH,CS,E

Hewlett-Packard Ltd.
Avon House
435 Stratford Road
SHIRLEY, Solihull
West Midlands B90 4BL
Tel: (021) 745 8800
Telex: 339105
CH

Hewlett-Packard Ltd.
West End House 41
High Street, West End
SOUTHAMPTON
Hampshire S03 3DQ
Tel: (703) 886767
Telex: 477138
CH

Hewlett-Packard Ltd.
King Street Lane
WINNERSH, Wokingham
Berkshire RG11 5AR
Tel: (0734) 784774
Telex: 847178
A,CH,E,M

Hewlett-Packard Ltd.
Nine Mile Ride
WOKINGHAM
Berkshire, 3RG11 3LL
Tel: 3446 3100
Telex: 84-88-05
CH,CS,E

NORTHERN IRELAND

Cardiac Services Company
95A Finaghy Road South
***BELFAST** BT 10 OBY*
Tel: (0232) 625-566
Telex: 747626
M

SCOTLAND

Hewlett-Packard Ltd.
SOUTH QUEENSFERRY
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