HP 9000 Series 500 and Series 800 Computer Systems

HP 27110B

CIO HP-IB Interface Card

Installation and Reference Manual

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Warning: This equipment generates and uses radio frequency energy and, if not installed and used properly, that is, in strict accordance with the manufacturer's instructions, may cause interference to radio and television reception. It has been type tested and found to comply with the limits for a Class A computing device in accordance with the specifications in Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

If this equipment does cause interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures: re-orient the receiving antenna; relocate the equipment with respect to the receiver; move the equipment away from the receiver; plug the equipment into a different branch circuit. If necessary, the user should consult the dealer or authorized field service representative for additional suggestions. The user may find the following booklet prepared by the Federal Communications Commission helpful: "How to Identify and Resolve Radio-TV Interference Problems". This booklet is available from the U.S. Government Printing Office, Washington, DC 20402. Stock No. 004-000-00345-4.

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Safety Considerations

General

This product and related documentation must be reviewed for familiarization with safety markings before operation.

Safety Symbols

Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect the product against damage.

Indicates hazardous voltages.

Indicates earth (ground) terminal. This symbol is sometimes used in the manual to indicate circuit common connected to a grounded chassis.

Warning

The warning sign denotes a hazard. It calls attention to a procedure, practice,or the like, which, if not correctly performed or adhered to, could result in injury. Do not proceed beyond a warning sign until the indicated conditions are fully understood and met.

Caution

The caution sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a caution sign until the indicated conditions are fully understood and met.

Servicing

Any servicing, adjustment, maintenance, or repair of this product must be performed only by service-trained personnel.

Grounding

Warning

SAFETY EARTH GROUND – The computer on which this product is installed is a safety class I product and is provided with a protective earthing terminal. An uninterruptible safety earth ground must be provided from the main power source to the product input wiring terminals, power cord, or supplied power cord set. Whenever it is likely that the protection has been impaired, the product must be made inoperative and be secured against any unintended operation.

BEFORE APPLYING POWER – Verify that the computer system is configured to match the available main power. Consult your system installation manuals.

Handling

Caution

STATIC SENSITIVE DEVICES - When any two materials make contact, their surfaces are crushed on the atomic level and electrons pass back and forth between the objects. On separation, one surface comes away with excess electrons (negatively charged) while the other surface is electron deficient (positively charged). The level of charge that is developed depends on the type of material. Insulators can easily build up charges in excess of 20,000 volts. A person working at a bench or walking across a floor can build up a charge of many thousands of volts. The amount of static voltage developed depends on the rate of generation of the charge and the capacitance of the body holding the charge. If the discharge happens to go through a semiconductor device and the transient current pulse is not effectively diverted by protection circuitry, the resulting current flow through the device can raise the temperature of internal junctions to their melting points. MOS structures are also susceptible to dielectric damage due to high fields.

The resulting damage can range from complete destruction to latent degradation. Small geometry semiconductor devices are especially susceptible to damage by static discharge.

This product contains static devices. Transport or store the printed circuit board assembly in an antistatic container. When installing or removing the printed circuit board assembly, do not touch any components. Hold the board by its edges. Component replacement operations must be performed at a static-free workstation using proper anti-static procedures.

Preface

This is the second edition of the HP 27110B CIO/HP-IB Interface Card Reference Manual. The manual contains information needed to install and check out the operation of the interface card. There are twelve chapters in the manual:

Chapter 1 **General Information** – introductory and should be read first.

Chapter 2 **Site Preparation** – not applicable to the product covered by this manual.

Chapter 3 **Installation and Configuration** – should be read before installing the product.

Chapter 4 **Preventive Maintenance** – read this before attempting any repairs or maintenance of the product.

Chapter 5 **Functional Description** – read when it is necessary to understand the technical operation of the product.

Chapter 6 **Removal and Replacement** – refer to this chapter when it is necessary to remove or replace this product in the host computer.

Chapter 7 **Adjustments** – refer to this chapter if it is considered necesary to tune the product.

Chapter 8 **Troubleshooting** – refer to this chapter when it is necessary to diagnose a problem in the product.

Chapter 9 **Component Parts** – refer to this chapter when it is necessary to identify a component in the product that must be removed and a new component installed.

Chapter 10 **Reference** – lists information source for the product.

Chapter 11 **Product History** – compares previous versions of this product.

Chapter 12 **Diagrams** – contains functional block and schematic drawings for the product.

Contents

1 General Information

The HP 27110B Hewlett-Packard Interface Bus (HP-IB) Interface Card is Hewlett-Packard's implementation of the IEEE Standard 488-1978 and Supplement 488-1978A-1980. The HP 27110B is an input/output (I/O) card and is used with the Hewlett-Packard HP 9000, Series 500 and Series 800, computers.

The HP 27110B can connect up to 14 slow-speed to medium-speed peripheral devices (such as instruments), or up to eight high-speed peripheral devices (such as disc drives). (Standard-speed and high-speed devices can NOT be mixed on the high-speed bus.)

The HP 27110B supports Command Set 80 protocol for HP CS/80-based discs and tape drives.

For error detection, the HP 27110B has parity check and cyclic redundancy check (CRC) as included features, and a firmware-based self-test is in read-only-memory (ROM). Parallel-poll mode can be programmatically enabled or disabled. A no-listener-detection circuit can be enabled or disabled with a switch on the HP 27110B.

Standard Product

The standard HP 27110B HP-IB Interface Card consists of the following parts:

Item	Part Number
HP-IB printed circuit card assembly	27110-60301
HP 27110B to HP-IB cable	27110-63001
HP 27110B manual (this manual)	27110-90005
HP-IB connector backing plate	30070-00043

The descriptors that identify the card are product number, card assembly number, and date code. The card assembly number and date code are printed on a sticker attached to the card.

Specifications

Maximum Transfer Rates

Medium/Slow-Speed:	500 kilobytes/second
High-Speed:	980 kilobytes/second

(Note: transfer rates are host-computer and software dependent)

Data Settling Time

Medium/Slow-Speed Operation:	May exceed 500 ns (i.e., 2 μs)
High-Speed Operation:	350 ns maximum

HP-IB Address

Switch-selectable (set to 30 decimal when acting as the HP-IB System Controller).

HP-IB Signal Line Terminations

Without the optional load resistor pack installed (the card configured for medium/slow-speed operation), each of the 16 HP-IB signal lines is terminated with a 2.3K-ohm resistor to Vcc and a 4.7K-ohm resistor to common. With the installation of the load resistor pack for high-speed operation, signal line termination values are changed except for the REN line, which is not affected.

HP-IB Signal Line Drivers

Each of the 16 HP-IB signal lines is driven with a circuit having the following typical characteristics:

Type:	Tri-state, open collector
Output Voltage, Low State:	0.5 V, 48 mA
Output Voltage, High State:	2.5 V, -5.2 mA

HP-IB Line Receivers

Each of the 16 HP-IB signal lines is received with a circuit having the following characteristics:

Type:	Schmitt Trigger
Threshold, Positive Transition:	1.6 V
Threshold, Negative Transition:	0.9 V for data lines, 1.0 V for control lines
Input Current, Low State:	-1.3 mA minimum to -3.2 mA maximum @ 0.5V
Input Current, High State:	0.7 mA minimum to 2.5 mA maximum, between 5V and 5.5V

Maximum Cable Length

Medium/Slow-Speed Operation: 2 metres per device connected, or 20 metres total, whichever is less

High-Speed Operation:

Number of Devices	*Maximum Total Cable Length (metres)*
1	8
2	9
3	10
4	11
5	12
6	13
7	14
8 (maximum)	15

Environmental Limits

Operating Temperatures: 0° to 55° Celsius

Operating Humidity: 5% to 95% relative humidity at 40° Celsius

Operating Altitude: 4600 metres (15,000 feet) maximum

(Before operating this unit in any extreme environment, consult your HP Customer Engineer or your nearest HP Sales and Support Office.)

Physical Characteristics

Size: 172.7 mm (6.80 inches) long, 172.0 mm (7.75 inches) wide

Weight: 265 grams

I/O Channel Connector: 80-pin connector, J1

Device Connector: 26-pin connector, J2

Power Requirements

Voltage	Current	Power Usage
+5 V	1.68 A	8.4 Watts

HP-IB Supported Functions

The HP 27110B card is designed to support the following HP-IB Interface Functions as defined by the IEEE Standard 488-1978. These functions are fully supported by the HP 27110B unless noted otherwise.

Mnemonic	Controller Functions
C1	System Controller
C2	Send Interface Clear and Take Charge
C3	Send Remote Enable
C4	Respond to Service Request
C5	Send Interface Messages, Receive Control, Pass Control, Pass Control to Self, Parallel Poll, Take Control Synchronously

Mnemonic	Controlled Device Functions
SR1	Service Request
RL2	Remote Local
PP1	Parallel Poll
DC1	Device Clear
DT1	Device Trigger

The following utility functions are provided to support the above listed functions:

Mnemonic	Utility Functions
SH1	Source Handshake
AH1	Acceptor Handshake
T1	Basic Talker, Serial Poll, Talk Only
TE1	Basic Extended Talker, Serial Poll, Talk Only, Unaddress if My Listener Address and My Secondary Address (requires host software support)
L1	Basic Listener, Listen Only Mode
LE1	Basic Extended Listener, Listener Only Mode, Unaddress if My Secondary Address and Talker Primary Addressed State (requires host software support)

2 Site Preparation

Note There are no site preparation requirements specific to the HP 27110B HP-IB interface card. Refer to your computer system manuals for general site preparation procedures.

3 Installation

This chapter provides information for you to install, configure, and verify correct operation of the HP 27110B HP-IB Interface card. You will also need your computer system installation manual for reference.

Unpacking and Examining the HP-IB Card

Caution

Many of the components of the HP 27110B are susceptible to destruction or degradation by electrostatic discharge. See the safety considerations in the front of this manual. To handle this card, use only the edges and extractor levers to avoid damage to components.

Remove the HP-IB card from its protective envelope and place it on *anti-static material* in a clean workspace. Inspect the card itself for damage or missing parts, and verify the part number. Also, check the other sub-assemblies (cables, etc.) for damage.

Storage

If you store the card for any reason, place it in an electrically and mechanically safe container. The safest place for the card is in the computer card cage. If you must store the card outside of the computer, use the original packaging material or have the card packed by a commercial packaging firm. You must protect the card from static electricity and impact. Place the package containing the card upright (like a book on a shelf) to avoid crushing.

General Guidelines for HP-IB Configuration

The following general guidelines should be observed when configuring an HP-IB system:

1. Devices or cable segments should not be added to an HP-IB system that is active.

   If a device is to be added to an active HP-IB system, the possibility of errors will be minimized if the following procedure is used:

   a. Attach all new cables to the new device to be added. Do not attach any unterminated cables to the existing bus.

   b. Power on the new device.

   c. Attach the new device (with power on) and its cable to the existing bus as a unit.

2. On an active HP-IB system, all devices attached should be powered-on to avoid excessive loads caused by powered-down devices.

3. The HP 27110B HP-IB Interface Card is shipped from Hewlett-Packard properly configured as system controller and set for high-speed operation. [Switch S1(6) is in the up, or open, position.] The 18-pin Dual In-Line Package (DIP) resistor pack (1810-0081) is also pre-installed in the socket (U123) to support this configuration.

   Depending on both the number and performance characteristics of the attached devices, the HP-IB card may be reconfigured for slow and medium operating speeds. Devices that talk at a slower rate may be configured as high-speed devices in the same system, provided all of the requirements for high-speed operation are med. (See "High-Speed Configuration" below.)

Caution

Adding termination resistors to more than one interface card on an HP-IB bus may result in permanent damage to any or all cards on the bus.

Note

A System Controller that is powered off will not allow the HP-IB bus to be used (as long as the System Controller is connected) because HP-IB bus drivers cannot drive the powered-down termination resistors.

4. Bus configuration guidelines in the following paragraphs should be observed.

Slow-Speed and Medium-Speed Configurations

For proper operation of the HP-IB bus at slow and medium operating speeds, observe the following guidelines:

1. Counting the HP-IB interface card as a device, up to 15 HP-IB devices may be connected to the bus.

2. The maximum length of cable permitted is two metres per connected device, or 20 metres total, whichever is less. For example, when connecting an HP-IB card to one peripheral device, a cable of up to 4 metres is allowed (2 devices X 2 metres/device). The length between adjacent devices is not normally critical as long as the overall limit is not exceeded.

3. At least four out of every five devices should be powered on.

4. The 18-pin Dual In-Line Package (DIP) resistor pack (1810-0081) must be removed from socket U123 behind connector J2 and placed in socket U106, labeled "NRML-SPD STORAGE". (See parts location diagram, figure 9-1, in Chapter 9.)

High-Speed Configuration

To achieve the maximum possible data transfer rate within a system, the following guidelines must be followed:

1. Switch S1(7) (see figure 9-1), marked "SLOW", should be set to the high speed position (down, or closed). Switch S1(7) determines the delay between data assertion and DAV (data valid) during an HP-IB write from the computer to the device. With the switch in SLOW position (up, or open), a delay of approximately 500 ns is realized. In the high-speed (down) position, the delay is reduced to approximately 350 ns.

2. All devices expected to talk at high speed must use a settling time of 350 nanoseconds or less.

3. All devices expected to talk at the higher rates should use 48 mA, three-state drivers.

4. The device capacitance on each HP-IB line, except REN (Remote Enable) and IFC (Interface Clear), should be less than 50 pF per device. In a system configuration, the total device capacitance should be no more than 50 pF for each equivalent resistive load in the system.

5. When the HP-IB interface card is the HP-IB System Controller [switch S1(6), marked "SCTL", is in the up, or open, position], the 18-pin Dual In-Line Package (DIP) load resistor pack (1810-0081) must also be installed. Verify that the resistor pack is installed in the socket U123, labeled "HI-SPD", located directly behind connector J2 (peripheral device cable connector), with pins 1 and 18 on the package oriented toward the half-circle notch on the socket. See figure 3-1.

6. Interconnecting cable links should be as short as possible, with a maximum of 15 metres total length per system (see table 3-1). There should be AT LEAST one equivalent resistive load per metre of cable. With the HP-IB interface card as the System Controller, each peripheral device provides a resistive load, and the high-speed resistor pack adds seven equivalent resistive loads.

   Thus a maximum system would be composed of the HP-IB card as the System Controller (with its high-speed resistor pack installed) and eight HP-IB peripherals.

7. All devices on the cable should be powered-on to avoid excessive loads caused by powered-down devices.

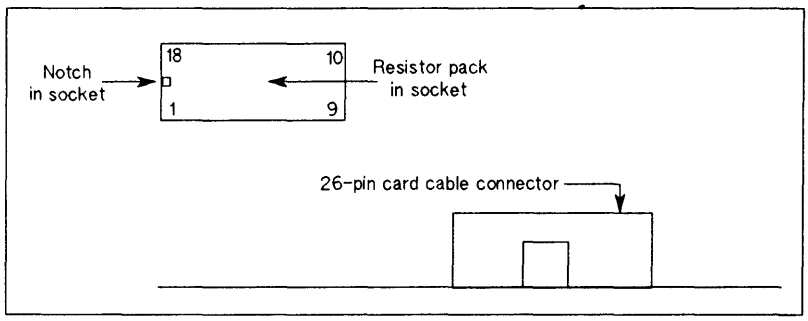


Figure 3-1. Top View of U123 Socket

Table 3-1. Maximum HP-IB Cable Lengths

Number of Peripheral Devices	Maximum Total Cable Length (metres)
1	8
2	9
3	10
4	11
5	12
6	13
7	14
8 (maximum)	15

Installation and Checkout

Install and check the operation of the HP-IB card as follows:

Warning

Before attempting to install this (or any) card, follow the computer "shut down" procedure and TURN OFF the computer power supply. Failure to disconnect the power could result in an electrical shock; and it may damage both the computer and the card. Any resultant damage will not be covered by the warranty.

1. All I/O cards draw their power from the host computer system. Determine if your computer system can supply the power needed for the HP-IB card. Refer to Chapter 1 for power requirements of the HP-IB card.

2. Set the card switches. Table 3-2 provides a summary of switch positions. Note that UP (open) is logic one, and DOWN (closed) is logic zero.

   a. Set switch S1(7), marked "SLOW", either up (for medium/slow-speed operation) or down (for high-speed operation). Check that the optional load resistor pack (see the "HIGH-SPEED OPERATION" paragraph) is installed if high-speed devices are going to be connected to the card AND the card is the HP-IB System Controller.

   b. Set switch S1(6), marked "SCTL", either up (System Controller ON) or down (System Controller OFF) depending on whether the card is going to operate as the System Controller.

   c. Set switches S1(1) through S1(5) to the card HP-IB address. If the card is to be the System Controller [switch S1(6) up], set the address to 30 decimal [S1(1) down, S1(2) through S1(5) up].

   d. Ensure that switch S1(8) is in the down/disabled position.

3. Turn off your computer power following system shutdown procedures compatible with your computer operating system. All HP-IB devices should also be powered-down. Insert the HP-IB card into the desired slot in the I/O channel. Make sure that the components on the card are on the same side as other installed cards. When installing the card, use care not to damage the components or traces on the card or on adjacent cards. Press the card firmly into place.

4. Connect the interface cable supplied to the 26-pin connector (J2) on the card. Table 3-3 shows the pin signal definitions for connector J2. Connect the other end to the HP-IB device(s).

Note

A "grounding grommet" on the interface cable allows the cable shield to be electrically grounded, which helps to reduce electromagnetic interference generated by some systems. Refer to your computer installation manual for additional information.

5. The HP-IB interface has a self-test in ROM. Depending on the power on sequence and logic of the host computer system, card self-test may be initiated at power on or system reset, or it may have to be invoked by you through software. Refer to the appropriate manual for your system for a description of self-test initiation.

6. Power-up the computer following procedures compatible with your operating system. To provide an indication that the HP-IB card is working properly:

   a. Some systems have a Computer Service Panel that has LEDs (light emitting diodes) for each I/O slot. These LEDs indicate that the interface card in the specified slot failed to pass self-test. Consult your computer system installation manual for additional information.

   b. For systems that do not have a Computer Service Panel, system software will provide console messages relating I/O slot status. Consult your system manuals.

Table 3-2. Configuration Switch Functions

Switch	Function	Settings
S1(8)	No Listener Detection	Should be down/disabled
S1(7)	Data Settling Time Selection	Up = Medium/Slow speed, Down = High speed
S1(6)	System Controller Selection	Up = System Controller, Down = Not System Controller
S1(1)–S1(5)	HP-IB Address Selection when not Controller-In-Charge	S5 = MSB (Most Significant Bit); S1 = LSB (Least Significant Bit); Up = Logic 1 = Open; Down = Logic 0 = Closed

The original factory switch settings are as follows:

S1(1) = DOWN
S1(2) = UP
S1(3) = UP
S1(4) = UP
S1(5) = UP
S1(6) = UP
S1(7) = DOWN
S1(8) = DOWN

Which set these conditions:

Speed – HIGH
System Controller – ON
Address – 30 Decimal
No-Listener Detect – Disabled

Table 3-3. Device Connector J2

Pin Number	Signal Mnemonic	Signal Definition
A1	SAFETY	Cable outer shield (chassis ground)
A2	SAFETY	Cable outer shield (chassis ground)
A3	ATN	Attention
A4	SRQ	Service Request
A5	IFC	Interface Clear
A6	NDAC	Not Data Accepted
A7	NRFD	Not Ready For Data
A8	DAV	Data Valid
A9	EOI	End Or Identify
A10	DIO4	Data Input/Output, Bit 4
A11	DIO3	Data Input/Output, Bit 3
A12	DIO2	Data Input/Output, Bit 2
A13	DIO1	Data Input/Output, Bit 1
B1	GND	Ground
B2	GND	Ground
B3	GND	Ground
B4	GND	Ground
B5	GND	Ground
B6	GND	Ground
B7	GND	Ground
B8	GND	Ground
B9	REN	Remote Enable
B10	DIO8	Data Input/Output, Bit 8
B11	DIO7	Data Input/Output, Bit 7
B12	DIO6	Data Input/Output, Bit 6
B13	DIO5	Data Input/Output, Bit 5

Reshipment

If the HP-IB card is to be shipped to Hewlett-Packard for any reason, attach a tag identifying the owner and indicating the reason for shipment.

Pack the HP-IB card in the original factory packing material, if available. If the original material is not available, good commercial packing material should be used. Reliable commercial packing and shipping companies have the facilities and materials to repack the item. BE SURE TO OBSERVE ANTI-STATIC PRECAUTIONS.

4 Preventive Maintenance

Caution

There are no operator adjustments on the HP 27110B card. *Do not adjust potentiometer R10.* This control was set permanently at the factory. Service, troubleshooting, or other maintenance of the HP 27110B should only be done by qualified electronic maintenance personnel.

Warning

Removal and replacement of the HP 27110B card should only be done with all power removed from the host computer. Power connected to the host computer in normal operation is dangerous and can cause serious injury or death if not switched off during service operations.

Caution

Static electricity can cause permanent damage to, or catastrophic failure of, the HP 27110B card. All work performed on electronic assemblies such as the HP 27110B must be at static-safe work stations that have correct static grounding for the card and the service person. Keep the card in a static protection bag whenever it is possible. Use the two plastic ejector levers to handle the card when it is not in a static protection bag or in the computer.

Preventive Maintenance and Cleaning Instructions

No regularly scheduled preventive maintenance is recommended for the HP 27110B card except the preventive maintenance recommended in the manual for the host computer.

Refer to the cleaning instructions in the host computer manual, and use the same procedures to clean the HP 27110B card.

5 Functional Description

The HP 27110B HP-IB card provides an interface between a Hewlett-Packard computer system and an HP-IB bus of up to 14 additional devices. Several such HP-IB devices, each connected to an HP-IB interface card, can be connected to one host computer.

Overview

Block and schematic diagrams for the HP-IB card are in Chapter 12.

Eight devices are connected to the Z8 address/data bus as shown below:

Device	Access Direction
HP-IB Controller	Buffered Read/Write
Address Latch	Write
Z8 Microcomputer	Read/Write
External ROM	Buffered Read
External RAM	Buffered Read/Write
Switch Register	Read
Backplane Interface Circuit (BIC)	Buffered Read/Write
Hardware Revision Code Register	Read

The devices are controlled by the Z8 and/or the DMA controller.

Interface between the HP-IB card and the I/O channel is accomplished via the Backplane Interface Circuit (BIC), U31, gate array and transceivers. Interface between the card and the HP-IB bus is through the HP-IB circuit: U103, U102, and U223.

Direct memory access (DMA) is used on HP-IB data transfers, and is done with a DMA state machine controller in a programmable logic array, and controlled by the Z8 microcomputer. The Z8 does not allow other devices (including itself) to use the data bus while DMA is in progress.

The Address Latch latches the lower eight address bits (A0–A7) from the multiplexed Address/Data bus. Only the memory components (ROM, RAM) require these address bits—all other devices are addressed via A8–A15.

The Switch Register buffers the HP-IB address of the card to the Z8.

The Hardware Revision Code Register has the hardware revision level.

The BIC, HP-IB circuit, RAM and ROM are buffered from the Z8 data bus to prevent timing problems caused by the Z8 interfacing requirements.

Backplane Interface

The Backplane Interface Circuit (BIC), which is a CMOS gate array integrated circuit or "chip", provides a standard method of interfacing to the I/O channel (backplane).

From a hardware standpoint, the BIC performs as a simple microprocessor peripheral. As used in the HP-IB card, the BIC has the following standard signal lines:

- Eight-bit bi-directional tri-state data bus
- Three-bit address bus
- Chip Select line to enable the chip for addressed data transfers
- Data Strobe line to strobe incoming data
- Read/Write line to specify data transfer direction
- Interrupt line to alert the Z8 of important events occurring on the I/O channel

Table 5-1 lists pin connections and describes signals to the BIC.

Table 5-1. BIC Chip Pin Connections

Pin No.	Signal Mnemonic	BIC Mnemonic	Description
1	D0	D0	Data Bus, Bit 0
2	D2	D2	Data Bus, Bit 2
3	D4	D4	Data Bus, Bit 4
4	D6	D6	Data Bus, Bit 6
5	END-	END-	Indicates end of data read or write
6	A8	A0	Register Address, Bit 0
7	A10	A2	Register Address, Bit 2
8	Z8RD	DS0-	Z8 Read (Read Data Strobe)
9	RDY-		Asserted by BIC when ready for data transfer
10	---		Not used
11	---		Not used
12	BIC:INT-	INT-	BIC Interrupt
13	NMI	NMI	Non-Maskable Interrupt
14	IFC (RST)	IFC	Interface Clear (Reset)
15	POLL	POLL	Poll
16		SYNC_MYAD-	In conjunction with DE, determines data bus drivers mode of operation
17	DOUT	DOUT	Data Out, specifies data bus direction
18	BP0	BP0	Bus Primitive, Bit 0 – with BP1, specifies bus primitive operation
19	UAD		Unary Address, latches BIC channel address after a PPON or IFC
20	AD0	AD0	Address Bus, Bit 0
21	AD2	AD2	Address Bus, Bit 2
22	CEND	CEND	Channel End
23	DB0	BIOD0-	Backplane I/O Data, Bit 0
24	DB1	BIOD1-	Backplane I/O Data, Bit 1
25	DB3	BIOD3-	Backplane I/O Data, Bit 3
26	DB5	BIOD5-	Backplane I/O Data, Bit 5
27	DB7	BIOD7-	Backplane I/O Data, Bit 7
28	DB9	BIOD9-	Backplane I/O Data, Bit 9
29	DB10	BIOD10	Backplane I/O Data, Bit 10
30	DB11	BIOD11-	Backplane I/O Data, Bit 11
31	DB13	BIOD13-	Backplane I/O Data, Bit 13
32	DB15	BIOD15-	Backplane I/O Data, Bit 15
33	BR	BR	Burst Request – at least one more transfer after current one
34	DBYT	DBYT	Device Byte, indicates current transfer is a byte
35	IOSB	IOSB	I/O Strobe

Table 5-1. BIC Chip Pin Connections (continued)

Pin No.	Signal Mnemonic	BIC Mnemonic	Description
36	D1	D1	Data Bus, Bit 1
37	D3	D3	Data Bus, Bit 3
38	D5	D5	Data Bus, Bit 5
39	D7	D7	Data Bus, Bit 7
40	GND	GND	Ground
41	A9	A1	Register Address, Bit 1
42	BIC:SEL-	CHSEL-	BIC Select, enables the BIC to read or write
43	DS-	DS1-	Data Strobe (Write Data Strobe)
44	DTR-	DTR-	Data Transfer Request
45	RESET-	RST-	Reset
46	ARQ	ARQ	Attention Request
47	+5		+5V
48	SYNC	SYNC	Synchronize, signals that an addressed bus operation will occur
49	MYAD	MYAD	My Address
50	BP1	BP1	Bus Primitive, Bit 1—with BPO, specifies bus primitive operation
51	AD1	AD1	Address Bus, Bit 1
52	AD3	AD3	Address Bus, Bit 3
53	CBYT	CBYT	Channel Byte, indicates that current transfer is a byte
54	GND	GND	Ground
55	DB2	BIOD2-	Backplane I/O Data, Bit 2
56	DB4	BIOD4-	Backplane I/O Data, Bit 4
57	DB7	BIOD7-	Backplane I/O Data, Bit 7
58	DB8	BIOD8-	Backplane I/O Data, Bit 8
59	DB12	BIOD12-	Backplane I/O Data, Bit 12
60	DB14	BIOD14-	Backplane I/O Data, Bit 14
61	---		Not used
62	DEND	DEND	Device End, indicates end of transfer
63	DE	DE	Direction Enable
64	PPON	PPON-	Primary Power On

A set of eight BIC registers, addressed by the 3-bit address bus, perform the following functions:

Register Number	Write Direction		Read Direction
0	<----------	DATA	---------->
1	COMMAND		SRQ ADDRESS
2	ORDER		BIC STATUS
3	BACKPLANE STATUS		BACKPLANE CONTROL
4	<----------	CONFIGURATION	---------->
5	<----------	INTERRUPT	---------->
6	<----------	INTERRUPT MASK	---------->
7	<----------	RESERVED	---------->

In addition to the eight resistors, the BIC provides:

A "ninth" data bit called END-. This open collector line is bi-directional. When the HP-IB card is performing a host write, this data bit is set true (LOW) to indicate the associated data byte is the last of that transfer. When reading from the host, the BIC drives END- true when the data byte on the 8-bit bus is the last of the transfer. Timing for END- is identical to data bus timing, thus the term "ninth data bit".

DMA lines DTR- (Data Transfer Request) and RDY- (Ready) are for unaddressed data transfers. These lines allow the BIC to transfer data in or out quickly without the necessity of repeatedly addressing the FIFO (First In First Out) data register in the HP-IB circuit. The DTR- and RDY- lines provide a two-wire handshake for performing unaddressed FIFO data transfers (DMA). DTR- is driven by the DMA controller when the controller is ready to begin a DMA transfer. RDY- is driven by the BIC when it is ready to begin a data transfer (when the FIFO data register has room on a host read or the FIFO is not empty on a host write). DTR- is not allowed to be driven true unless RDY- is true.

A reset line (RESET-), initializes the Z8. RESET- informs the Z8 that one or more of the following events has occurred:

- Primary power has been turned on
- A CHANNEL I/O Reset has been issued (global reset)
- A CHANNEL I/O Device Clear has been issued (addressed reset)

RESET- connects directly to the Z8 reset input. By polling the BIC registers after a reset, the Z8 can determine which of the three types of reset occurred, and take the appropriate action.

A timing diagram for a BIC DMA–host read is shown in figure 5-1. A BIC DMA–host write timing diagram is shown in figure 5-2.

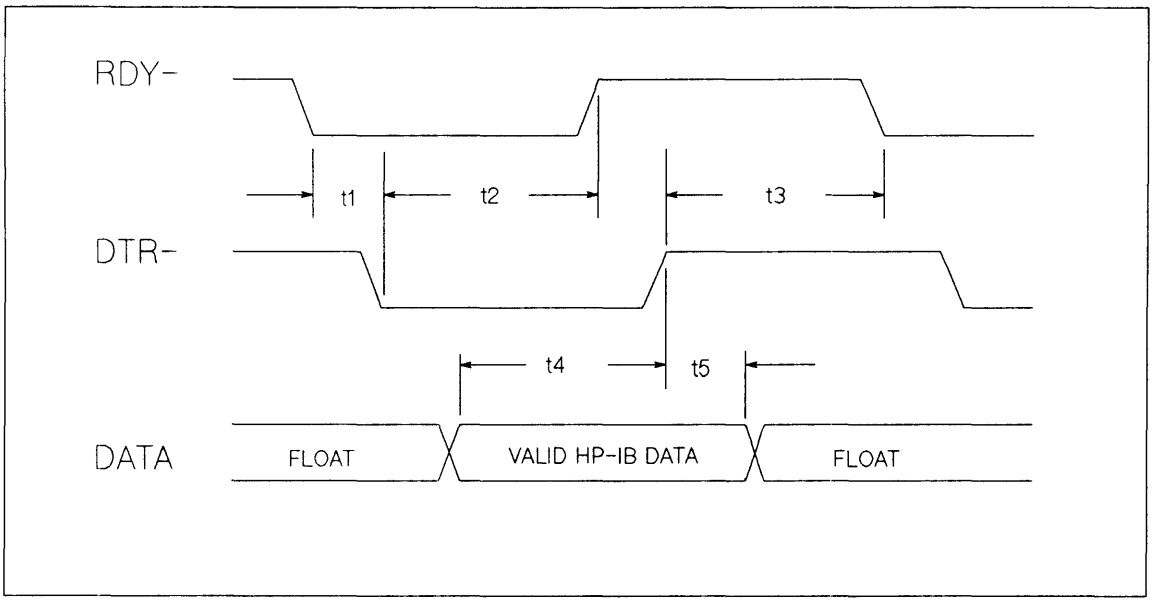


Figure 5-1. BIC DMA–Host Read Timing Diagram

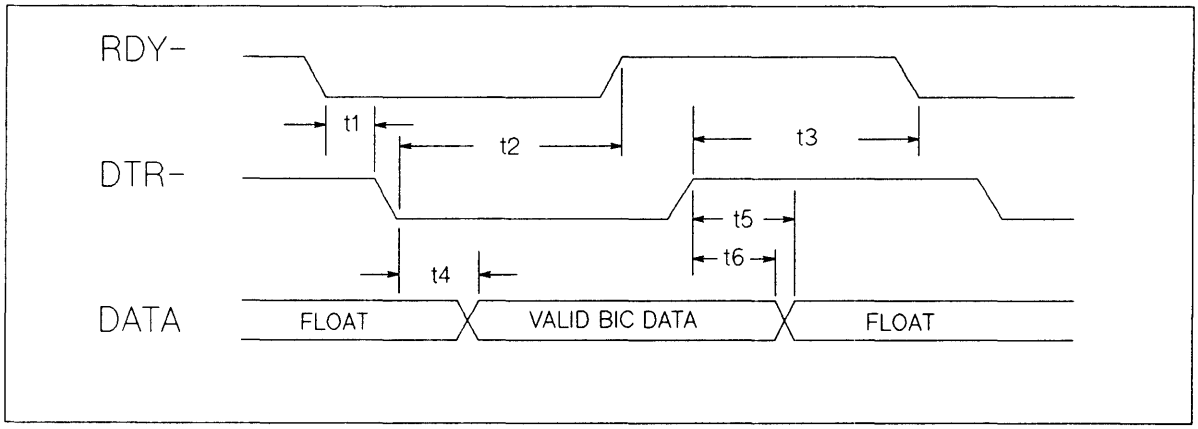


Figure 5-2. BIC DMA–Host Write Timing Diagram

HP-IB Interface

The HP-IB controller (a CMOS chip) provides a high-speed interface between the Z8 and the HP-IB bus. As with the BIC chip, the HP-IB chip appears to the Z8 as a simple microprocessor peripheral. The chip is buffered from the Z8 data bus to allow the HP-IB chip to meet Z8 timing restrictions.

The HP-IB chip contains the following lines:

- A 10-bit wide data bus
- Three register-select lines for selecting among the eight registers of HP-IB controller chip. Table 5-2 shows the HP-IB chip registers selected by the Z8 addressing.
- Chip select
- Read/write line
- Data strobe line (IOGO-)

Table 5-2. HP-IB Controller Register Selection

Z8 Address, A10	A9	A8	Register Number	Register Name
0	1	0	0	FIFO
0	1	1	1	HP-IB Chip Status
0	0	0	2	Interrupt
0	0	1	3	Interrupt Mask
1	1	0	4	Parallel Poll Mask
1	1	1	5	Parallel Poll Sense
1	0	0	6	HP-IB Control
1	0	1	7	HP-IB Address

The ninth and tenth bits of the 10-bit data bus are used by the HP-IB chip registers to provide a special meaning to the 8-bit register value. For example, in the inbound FIFO direction, these two bits indicate whether or not a secondary has been addressed, if the last byte or a record has occurred, if the last byte of a subgroup has occurred, or if a counted transfer has ended. In the outbound FIFO direction, the two bits are used to specify ATN and EOI true.

HP-IB chip pin connections are listed in table 5-3.

Table 5-3. HP-IB Chip Pin Connections

Pin No.	Chip Mnemonic	Type*	Description
		HP-IB Data Lines – Low True	
44	DIO71	B	Data Input/Output, Bit 1 – low true
45	DIO2-	B	Data Input/Output, Bit 2 – low true
46	DIO3-	B	Data Input/Output, Bit 3 – low true
47	DIO4-	B	Data Input/Output, Bit 4 – low true
48	DIO5-	B	Data Input/Output, Bit 5 – low true
2	DIO6-	B	Data Input/Output, Bit 6 – low true
3	DIO7-	B	Data Input/Output, Bit 7 – low true
4	DIO9-	B	Data Input/Output, Bit 8 – low true
		HP-IB Handshake Lines	
18	ATN-	B	Attention
16	RFD	B	Ready for Data
15	DAC	B	Data Accepted
		HP-IB Bus Management Lines – Low True	
6	DAV-	B	Data Available
5	EOI-	B	End or Identify
14	REN-	B	Remote Enable
13	IFC-	B	Interface Clear
17	SRQ-	B	Service Request
		Internal Data Lines	
30	D0	B	These two bits indicate the following bus conditions when read from register 2: **D0 D1** 0 0 Normal Data 0 1 Secondary Address 1 0 Last byte of subgroup 1 1 Last byte of record
29	D1	B	
28	D8	B	Z8 Data Bus, Bit 7
27	D9	B	Z8 Data Bus, Bit 6
26	D10	B	Z8 Data Bus, Bit 5
25	D11	B	Z8 Data Bus, Bit 4
24	D12	B	Z8 Data Bus, Bit 3
23	D13	B	Z8 Data Bus, Bit 2
22	D14	B	Z8 Data Bus, Bit 1
21	D15	B	Z8 Data Bus, Bit 0

*Line Types:
B = Bidirectional
I = Input
O = Output
P = Power
T = Timing

Table 5-3. HP-IB Chip Pin Connections (continued)

Pin No.	Chip Mnemonic	Type*	Description
33	A13	I	Register address lines used by Z8 to access HP-IB chip registers, along with IB:WRT and IB:SEL-
34	A14	I	
35	A15	I	
7	SCTRL	I	Makes HP-IB card System Controller
40	PON	I	When low, initializes the HP-IB chip for > 500 nanoseconds
39	W	I	Write enable, read disable (IB:WRT)
36	IOGO-	I	Initiates a register read/write
32	CHSEL-	I	Enables IOGO-
41	DMARQ-	O	DMA request, indicating that the HP-IB chip FIFO register is ready
38	INT-	O	Requests interrupt from Z8 (ABI:INT-)
37	IOEND-	O	Handshake complete
19	TRIG	O	Pulse generated when HP-IB card gets Group Execute Trigger (GET)
12	CIC	O	Enables ATN driver when true and SRQ driver when false
11	HSE	O	Transceivers use active pullups (vs. open collector)
10	DEE	O	DAV/EOI enable (send DAV and EOI, vs. receive)
9	DIOE	O	DIO enable (send data, vs. receive)
43	GND	P	Ground
1	GND	P	Ground
8	VCC	P	+5V
31	VDC	P	+5V
42	RS	T	Delay stabilizing resistor
20	RTL	I	Return to local (tied permanently false)

*Line Types:
- B = Bidirectional
- I = Input
- O = Output
- P = Power
- T = Timing

DMA Requirements

The signals IOEND- and DMARQ- are used for DMA purposes only (no handshaking occurs on an addressed HP-IB chip access). IOEND- false (high) and DMARQ- true (low) indicate that the HP-IB chip is ready to transfer a byte via DMA in the direction specified by its read/write line. This condition (IOEND- false and DMARQ- true) is AND'ed with the BIC RDY- signal to generate Interface Ready (IF:RDY-). When the DMA controller detects IF:RDY- true, it is ready to begin DMA upon command from the Z8.

The IOGO- signal is asserted by the DMA controller to handshake DMA data through the HP-IB chip, and also for normal HP-IB chip register accesses. Note that IOGO- is a combination of the Z8 data strobe, and the DMA controller strobe. The DMA controller ensures that the timing relationships between data and IOGO- are maintained.

Because the HP-IB chip generates its IEEE-488 timing constants, a tuning network is provided to extract the maximum possible data rate. A potentiometer is used, with a firmware routine, to adjust the pulse widths of a continuous stream of pulses. The potentiometer is set at the factory and requires no further adjustment.

The HP-IB chip TRIG signal goes high when a Group Execute Trigger (GET signal) occurs on the HP-IB card. The GET signal is a means of triggering a number of devices, such as voltmeters, to take readings simultaneously. ABI:INT- becomes true if any of its nine interrupting conditions exists. The HP-IB chip Interrupt register defines these conditions, as follows:

Parity Error
Status Change
Processor Handshake Abort
Parallel Poll Response
Service Request
FIFO Room Available
FIFO Bytes Available
FIFO Idle
Device Clear

The ABI:INT- signal is deasserted when the interrupting condition no longer exists.

The HP-IB bus transceivers have two types of control inputs: One input determines the direction of the transceiver (send or receive), and is labeled "TE" for Talk Enable; the other input determines whether the outputs facing the HP-IB are open collector or active TTL (when Talk Enable is true). Each transceiver has a pullup to +5 and a pulldown to ground.

All signals and data on the HP-IB card are low true, except NRFD and NDAC. When NRFD is high, all devices on the bus are ready for data. When NDAC is high, all devices that were to receive data have received the data. In a powered-down system, all lines are true, except that all devices are not ready and have not accepted data.

HP-IB Chip DMA Read Timing

The following steps describe the sequence of events during a host read from the HP-IB chip. A timing diagram is shown in figure 5-3.

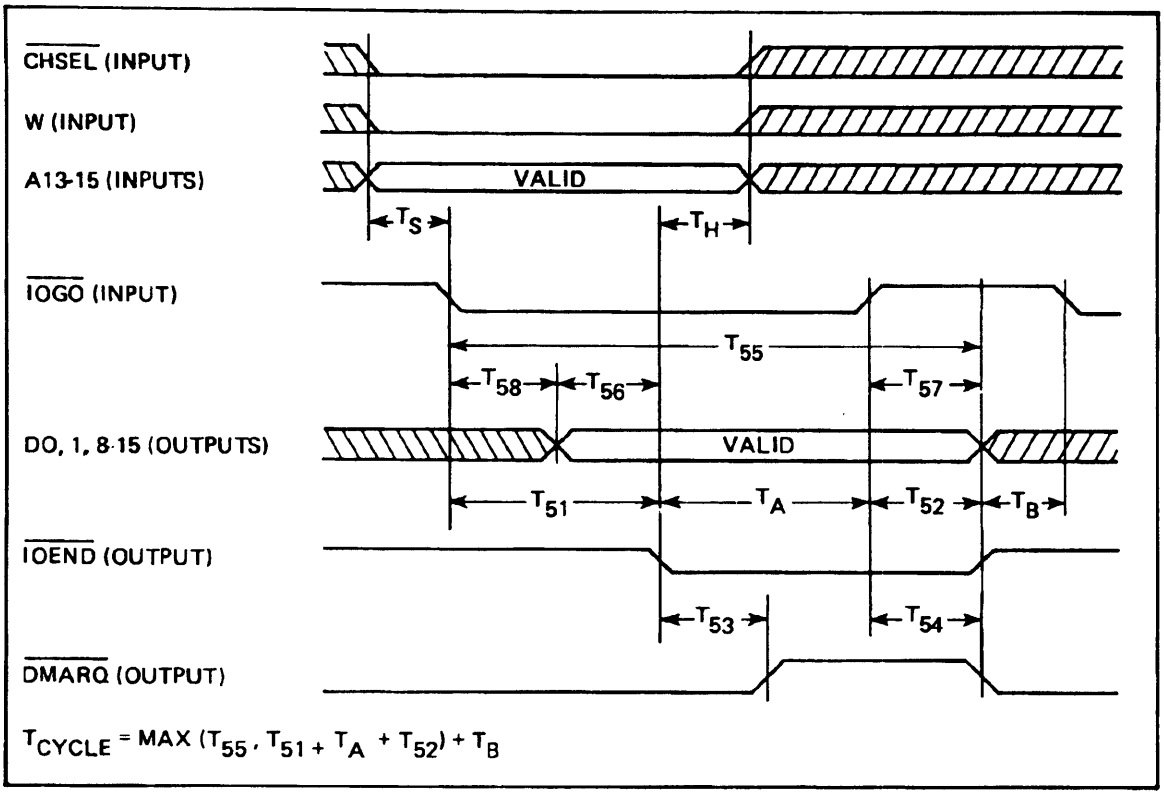
1. The first step in a host read from the HP-IB chip is to wait until DMARQ- goes true (indicating that the HP-IB chip FIFO is ready to move another byte), and IOEND- goes false (indicating that the previous handshake has completed).

2. IOGO- may not be asserted. On a host read, IOGO- indicates to the HP-IB chip that the HP-IB card is prepared to accept inbound data. Once asserted, data from the HP-IB chip will become valid 25-140 nanoseconds later.

3. Up to 25 nanoseconds after IOGO- is asserted, IOEND- will become true, indicating that the HP-IB chip has completed the inbound data transfer. DMARQ- momentarily goes false 100 nanoseconds (maximum) after IOEND- goes true.

4. IOEND- is acknowledged by deasserting IOGO-.

5. IOEND- will go false in response to IOGO- deassertion. If the inbound FIFO has more data in it, DMARQ- goes true within 150 nanoseconds after IOGO- is deasserted. If no data is left in FIFO, then DMARQ- remains false until the FIFO receives another data byte from the HP-IB bus. To continue a host read, the process is repeated beginning at step 1.



SWITCHING CHARACTERISTICS, V_{DD} = 12V±5%, V_{DC}= 12V±5% OR 5V±5% OR 0°C ≤ T ≤ 70°C

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
T_{51} IOGO ⌊ TO IOEND ⌊				250	NS
T_{52} IOGO ⌈ TO IOEND ⌈				150	NS
T_{53} IOEND ⌊ TO DMARQ ⌈	A13-A15 = 010, REG 4 (14) = 0	FIFO NOT EMPTY		125	NS
T_{54} IOGO ⌈ TO DMARQ ⌊		1 BYTE IN FIFO		150	NS
T_{55} IOGO ⌊ TO IOEND ⌈	T_A = ONS			450	NS
T_{56} DATA TO IOEND ⌊	A13-A15 = 010, FIFO NOT EMPTY		25		NS
	ALL REGISTERS EXCEPT ABOVE		−30*		NS
T_{57} IOGO ⌈ TO DATA OFF			25	140	NS
T_{58} IOGO ⌊ TO DATA ON	A13-A15 = 010, FIFO NOT EMPTY		25	140	NS

RECOMMENDED SAMPLE AND HOLD TIMES: $T_S \geq$ ONS, $T_H \geq$ ONS

*NEGATIVE SIGN INDICATES IOEND MAY RESPOND BEFORE DATA

Figure 5-3. HP-IB Chip DMA Read Timing

HP-IB Chip DMA Write Timing

The steps listed below describe the sequence of events during a host write to the HP-IB chip. A "write" timing diagram is shown in figure 5-4.

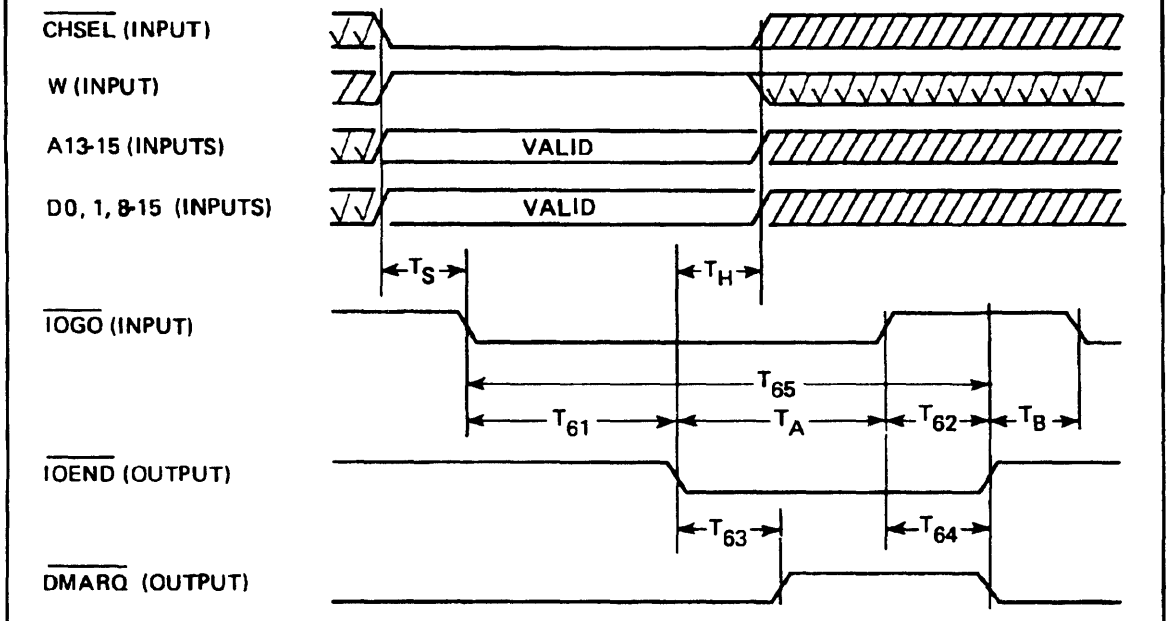
1. Assuming the data source (BIC) has data ready to send, the first step in a host write operation is to wait for IOEND- false and DMARQ- is true, as in a host read.

2. IOGO- is asserted to initiate the transfer.

3. A maximum of 150 nanoseconds later, IOEND- is asserted, indicating that the HP-IB chip has accepted the data. Then, 100 nanoseconds (maximum) after IOEND- goes true, DMARQ- goes false.

4. IOEND- is recognized and IOGO- is deasserted.

5. IOEND- goes false in response to IOGO- deassertion. If the outbound FIFO is not full, DMARQ- goes true; if the outbound FIFO is full, DMARQ- goes false until the FIFO is not full. To continue the host write, the steps are repeated beginning at step 1.



SWITCHING CHARACTERISTICS, V_{DD} = 12V±5%, V_{DC} = 12V±5% OR 5V±5%, 0 °C ≤ T_A ≤ 70°C

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
T_{61} IOGO ↓ TO IOEND ↓				150	NS
T_{62} IOGO ↑ TO IOEND ↑				150	NS
T_{63} IOEND ↓ TO DMARQ ↑	A13-A15 =010, REG 4 (14) =1	FIFO NOT FULL		100	NS
T_{64} IOGO ↑ TO DMARQ ↓		< 7 BYTES IN FIFO		150	NS
T_{65} IOGO ↓ TO IOEND ↑	T_A = 0NS			350	NS

RECOMMENDED SAMPLE AND HOLD TIMES: $T_S \geq$ 0NS, $T_H \geq$ 0NS

Figure 5-4. HP-IB Chip DMA Write Timing

Z8 Interface

The Z8 integrated circuit (U53) is a one-chip microcomputer that, under software control, can assume different memory and I/O configurations. Thirty-two lines are dedicated to I/O. These lines are grouped into four ports of eight lines each, and are configurable as input, output, or bidirectional. Under software control, the ports can provide timing, status signals, address outputs, and serial or parallel I/O with or without handshake. In the HP-IB card, all device communication is done via memory-mapped I/O. That is, the BIC and HP-IB chip registers and the DMA/PPOL control lines are all addressed as external memory.

Table 5-4 shows the Z8 pin connections grouped according to the four ports; the Z8 pin connections are listed again in table 5-5 with the signals described in greater detail.

Table 5-4. Z8 Pinouts Grouped by Port

Port 0	Port 1	Port 2	Port 3
P00: A8	P10: D0	P20: BUCKET	P30: IB:IFC-
P01: A9	P11: D1	P21: SEND:ATN	P31: BIC:INT-
P02: A10	P12: D2	P22: SEND:EOI-/EOC	P32: IB:INT-
P03: A11	P13: D3	P23: R:SENSE	P33: DMA:INT-
P04: A12	P14: D4	P24: EN:END-	P34: LED:ON
P05: A13	P15: D5	P25: LAST:EOI-	P35: DMA:PAUSE
P06: A14	P16: D6	P26: SLOW:SPEED	P36: DMA:RST
P07: A15	P17: D7	P27: ODD	P37: DMA:READ

The Z8 control signals are:

XTAL1	Clock Input
AS-	Address Strobe
DS-	Data Strobe
RESET-	Z8 Reset
Z8RD	Read/Write Line

Port 0 outputs the upper address byte, valid on the rising edge of AS-.

Port 1 multiplexes the lower address byte and the data byte. A0 through A7 are valid on the rising edge of AS-, D0 through D7 are valid on the rising edge of DS-.

Port 2 provides general-purpose outputs (see table 5-4).

Port 3 provides interrupt inputs and DMA control lines (see table 5-4).

Table 5-5. Z8 Pin Connections

Z8 Mnemonic	Pin No.	Description
	21–28	**Port 1.** Used for bidirectional internal data bus. Addresses are multiplexed with the data, and latched on the rising edge AS- (pin 9). On power-on these lines are configured as inputs. After power-on the port is always configured for external memory reference.
	31–38	**Port 2.** Used for DMA control, Group Execute Trigger Clear, and to send ATN and EOI data. On power-on these lines are configured as inputs, and float high because of external pullups.
P20	31	BUCKET, used to discard data without causing the DMA transfer to end
P21	32	SEND:ATN, used to send ATN data
P22	33	SEND:EOI-/EOC, used to send EOI data; EOC (End On Count) is used to enable device end on counted reads.
P23	34	RSENSE, driven by circuit to sense presence of load resistor pack in U123 socket.
P24	35	EN:END, enables END bit generation
P25	36	LAST:EOI-, represents the status of EOI- on the most recent byte transferred across HP-IB.
P26	37	SLOW_SPEED, used to detect position of SLOW switch. Logic HIGH indicates switch is set for standard data rate.
P27	38	ODD, driven by the ODD flip-flop, set on every odd byte
P00–P07	13–20	**Port 0.** Used to provide additional address bits/chip selects for external memory (A8-A15). A13-A15 is used as a "chip" select for I/O, which includes all HP-IB chip and BIC chip registers, the switch (read-only), and the external RAM and ROM.
	6	RESET-. The Z8 will be initialized if PPON is held low for 50 msec or more after power is applied and if the voltage is between 4.75 and 5.25 volts.
	7	Z8RD. When high, the Z8 addresses both the ABI and the BIC to be read from, according to the appropriate chip selects. When low, the Z8 is writing to external memory/IO.
	8	Z8DS-, Z8 data strobe. Used to generate the BIC strobe, to latch switch data, and to generate IOGO- from C:IOGO-.
	9	AS-, address strobe. Used to latch the lower 8 bits of address from the multiplexed data/address bus (port 1). AS- is also used as the enable input to the address decoder for chip select.

Table 5-5. Z8 Pin Connections (continued)

Z8 Mnemonic	Pin No.	Description
	2, 3	Clock inputs (12.00 MHz frequency, 0.0833 μsec period)
	1, 11	+5 and GND, respectively
P30 - P37		**Port 3.** Configured as serial I/O, interrupts, and DMA control lines. P30-33 are always inputs, P34-37 are always output.
P30	5	IB:IFC, interface bus IFC line
P31	39	BIC:INT-, BIC interrupt
P32	12	ABI:INT-, ABI interrupt
P33	30	DMA:INT-, DMA controller interrupt
P37	4	DMA:READ, asserted when the Z8 wants to initialize a DMA read operation. Deasserted when the Z8 wants to terminate a DMA read without data loss.
P35	10	DMA:PAUSE, asserted when the Z8 wants to pause DMA without data loss.
P36	40	DMA:RST, aborts DMA and acknowledges DMA interrupt.
P34	29	LED:ON when asserted switches LED on.

Addressing

Devices are selected using the upper three bits (A13, A14, A15) of the 16-bit address bus. This divides the I/O address range into eight 8K segments as shown in table 5-6.

For example, if the firmware references an external memory address between 8000 and 9FFF, the HP-IB chip will be accessed, with address bits A8–A10 specifying a particular HP-IB chip register.

Table 5-6. Addressing Codes

A13–A15	Device Selected	Address Range (HEX)
0	Unassigned	0000–1FFF
1	GET_CLR-Rev*	2000–3FFF
2	BIC	4x00–5xFF
3	Switch	6000–7FFF
4	HP-IB chip	8x00–9xFF
5	RAM	A000–BFFF
6	ROM	C000–DFFF
7	ROM	E000–FFFF
x = 3-bit register address for the seven BIC or HP-IB chip registers *Card Revision Code		

The device select decoder, U74, using AS- from the Z8 as the enable for the decoder, implements the decoding shown in table 5-6 to select the appropriate device. The ROM is selected by ANDing the outputs 6 and 7 from the decoder (U74).

Switch Register Interface

The Switch register (U114) buffers the address switch (S1) settings onto the Z8 data bus. When the Z8 reads from the Switch register, the output enable lines from the Switch register become true, and the status of the switch is driven onto the Z8 data bus. In addition to the address switch status, NDAC (Not Data Accepted), GET (Group Execute Trigger) and TUNING_MODE are read via the Switch register.

The NDAC signal comes directly from the HP-IB bus (no transceivers in line), and is used by the Z8 to determine if outbound data has been accepted. Data has been accepted when the signal is high.

The Group Execute Trigger (GET) signal is sent to all devices in the system. If a device (such as some voltmeters) understands GET, that device will perform a function when it receives the trigger. In this manner, several devices can be triggered simultaneously on the bus. The HP-IB chip detects the trigger signal, and outputs a 60 nsec (minimum) pulse on TRIG, which is sent to the edge input of a D flip-flop (U105). The output of this flip-flop is buffered through the Switch register and is used by the Z8 to determine if a GET signal has been received from the HP-IB chip. The GET:CLR signal clears the flip-flop after it has been read. The

GET_CLR signal is generated whenever the Z8 addresses the memory space 2000H–3FFFH.

The TUNING MODE signal indicates to the Z8 whether R13 has been connected to ground which signals the Z8 to enter the HP-IB chip tuning mode. This mode is for factory adjustment of R10 to set the HP-IB controller chip R/C time constant. This time constant adjusts the HP-IB controller chips to agree with IEEE-488 timing specifications.

Revision Code Register

A hardware revision number that can be reported to the host is set on the card.

A 74LS125 buffer (U104) with inputs tied through a resistor to +5 V or ground and with outputs on the address/data bus is used to gate the revision code into the Z8. There are three bits available with the first code being set to zero, with all resistors tied to ground. The bit significance is:

Most significant bit:	3
	7
Least significant bit:	4

The revision number buffer is enabled by any access to address location 2000H. The revision code uses the same line off the address decoder as the GET_CLEAR- line. There is no conflict when both functions are enabled at the same time.

The revision number is reported to the host computer in response to a Level 2 IDY order as part of the card identification message. The Z8 firmware handles this order by performing a memory read from the revision code register.

Revision 2.0 of the HP-CIO Standard allows only three bits to be reported to the host computer.

Z8 Control Signals

The Z8 is driven to its maximum clock frequency with an external crystal (Y1) running at 12 MHz. The Z8 is reset by only one signal: the BIC RESET- line. This line goes true if power is cycled to the host computer, an IFC signal is issued, or an addressed device clear is issued to the HP-IB card. When the Z8 is reset, it begins executing code at location 0C (hex), and the following conditions exist:

- Port 2 lines are defined as inputs (floating)
- Port 3 lower four bits are inputs, upper four bits are outputs
- Ports 0 and 1 are defined as inputs (floating)
- Memory cycle timing is normal (instead of slow)
- Stack is internal

Note

All Z8 inputs are high impedance (maximum +/- 10μA, 0V to +5.25V, which is essentially floating).

To initialize the Z8 on the HP-IB card, RESET- must be held low for 50 milliseconds after power is applied and is within the supply tolerance, **OR** five microseconds after power and clock have stabilized.

This means that the RESET- due to Primary Power On (PPON) must be 50 milliseconds, and other RESETs due to Interface Clear (IFC) or Device Clear (DCL) can be five microseconds long (assuming they occur after power-up). While RESET- is held low, the Z8 should be driving a low on Data Strobe (DS-), and a square wave (6 MHz, or half the Z8 input frequency) on Address Strobe (AS-).

Address Strobe (AS-) and Data Strobe (DS-) clock address and data information, respectively. Addresses on port 1 (lower byte) and port 0 (upper byte) are valid on the rising edge of AS-. Outbound data is valid on the rising edge of Z8DS-. Incoming data is latched on the rising edge of Z8DS-. An HP 1630D Logic Analyzer can monitor all Z8 activity using the rising edge of AS- to clock the 16-bit address, and the rising edge of DS- to clock the eight-bit data.

The Z8 RD signal specifies whether the Z8 is reading from or writing to the eight-bit internal data bus.

SEND:ATN, SEND:EOI, LAST:EOI, and LED:ON

The SEND:ATN and SEND:EOI signals are used by the HP-IB chip on host writes. The SEND:ATN signal is asserted by the Z8 before writing command sequences to HP-IB peripherals, as a means of selecting devices to talk or listen. In addition, the signal is used to send special commands which inform peripherals to go into local or remote mode, take control of the bus, clear themselves, etc.

The SEND:EOI signal enables the END- line to generate an EOI signal on the HP-IB bus. The EOI and ATN control signals go into the ninth and tenth data bits of the HP-IB chip FIFO register. The HP-IB chip outbound FIFO reserves these bits to specify ATN or EOI on the HP-IB bus.

The LAST:EOI- signal is derived from NDAC and EOI- and allows the Z8 to distinguish between an inbound "Line Feed" character and a "Line Feed" character with EOI true.

When reading data, the HP-IB chip sets IB:D0 and IB:D1 true when a "Line Feed" occurs, or when any character with EOI true occurs. Both of these conditions are considered "end-of-record" terminating condition and the HP-IB chip treats them identically.

The DMA controller has been programmed to sense when IB:D0 and IB:D1 are simultaneously true. When this occurs, DMA is halted and the

Z8 is interrupted. The Z8 polls IB:D0 and IB:D1 and recognizes that one of the two possible "end-of-record" conditions has occurred.

The LAST:EOI- signal allows the Z8 to distinguish between the two types of "end-of-record" terminations by polling LAST:EOI- when it polls IB:D0 and IB:D1. LAST:EOI- low means the last byte transferred across HP-IB had an EOI attached to it.

This distinction is required when reading data from instruments that use LF and LF with/EOI as two different levels of termination. The majority of HP-IB applications do not require this distinction.

The LED:ON signal lights the LED on the HP-IB card. When the Z8 is reset, pin P34 (LED:ON) is made an input to the Z8, and the external pullup forces the LED on. When the reset line is released, the Z8 begins initialization (and self-test, if invoked) which will eventually turn the LED off. If the HP 27110B fails the self-test, the LED will remain on.

Interrupts

The Z8 microcomputer has eight sources of interrupts, four of which are implemented on the HP-IB card. Each interrupt input is negative edge-triggered, with the minimum pulse width of the interrupt equal to 100 nanoseconds.

The four interrupts on the HP-IB card are:

- HP-IB Interface Clear (IB:IFC- signal). When the HP-IB is not the System Controller, an interrupt occurs when the System Controller asserts IFC.
- BIC Interrupt (BIC:INT- signal).
- HP-IB Chip Interrupt (ABI:INT- signal).
- DMA Interrupt (DMA:INT- signal). This interrupt informs the Z8 of an END condition on a host read.

Interrupts 2 (BIC:INT-) and 3 (ABI:INT-) are continuous-edge interrupts. That is, as long as the device is interrupting, a clock (3.6864 MHz) will generate negative-going interrupt edges to the Z8. With this technique, the Z8 can detect any interrupts that may have occurred when interrupts are disabled. When the Z8 re-enables interrupts, the edges will continue to occur until the specific interrupting condition is acknowledged. The interrupt clock is the system clock (14.7456 MHz) divided by four. This provides a period of 271 nanoseconds (ns), or a half-period of 135 ns, which is 35 ns more than the interrupt inputs require.

Interrupt 4 is the DMA interrupt, informing the Z8 of an END condition on a host read. By interrogating the HP-IB chip, the Z8 can determine why the DMA interrupt occurred (end-of-record, end-of-subgroup, secondary address, or end-of-count).

Direct Memory Access Interface (DMA)

The DMA controller (U45) is a synchronous logic array with eight inputs and eight outputs. The DMA controller allows the HP-IB chip and BIC chip to converse over the internal data bus at high speed. The Z8 microcomputer controls the DMA controller via five signals: DMA:PAUSE, DMA:RST, DMA:READ, BUCKET, and EOC. An algorithmic state diagram of the DMA controller operation is shown in Chapter 12. Refer to this diagram, as well as the schematic diagram when reading the following paragraphs.

The DMA:RST signal resets all DMA controller flip-flops when latched through U44 on the rising edge of CCLK-. This is the way the Z8 initializes the DMA controller.

The READ signal controls the DMA direction (host read or host write) of the DMA controller. (READ true = host read, READ false = host write.)

The PAUSE signal provides a means of terminating DMA without losing data. The DMA controller completes transfers before monitoring PAUSE. If PAUSE is true, a new DMA cycle is not started until PAUSE goes false. This means that several hundred nanoseconds may pass after PAUSE is asserted before the DMA controller actually pauses (if PAUSE is asserted just after the Z8 has begun a new DMA cycle). Because each Z8 instruction takes approximately 13 microseconds to execute, the DMA controller will have paused by the time the Z8 executes its next instruction.

The BUCKET signal causes the DMA controller to perform a DM read out of the HP-IB chip, but the data is not passed to the BIC. This allows the Z8 to monitor END conditions on device-to-device transfers.

The SEND:EOI-/EOC signal performs two functions:

- When writing, the signal is SEND:EOI for End Or Identify,
- When reading, the signal is SEND:EOC for End On Count.

The signal can be used for EOI and EOC because the DMA does not monitor the signal during a write (thus EOC is meaningless), and the IB:D0 signal is disabled during a read (thus EOI is meaningless).

If the HP-IB card is performing a counted transfer of 256 bytes or less, EOC should be true, indicating to the DMA controller that a device end (END-) is needed when the DMA controller detects an end-of-count from the HP-IB chip. The Z8 is interrupted when an enabled end-on-count condition occurs. For counted transfers of more than 256, the Z8 still needs to be interrupted on end-on-count condition, but the DMA controller will NOT generate END- because the Z8 will be ready to start another 256-byte counted transfer. Therefore, in this case, EOC is set false, disabling the end-on-count device end. When the last 256 (or less) bytes of an extended counted transfer are ready to be transferred, the Z8 re-enables EOC before starting another DMA cycle.

Of the DMA controller's eight outputs, two (ODD, via the Odd/Even flip-flop; and DMA:INT-) go to the Z8. The ODD signal is a 1-bit counter that keeps track of whether an odd or even number of bytes has been DMA transferred. The Q- output of the Odd/Even flip-flop is connected to the D input, forming a toggle flip-flop that changes state on each rising edge of DTR-. The ODD signal is only used by the Z8 on host reads. The Odd/Even flip-flop is reset by the DMA:RST command from the Z8. If the host is reading data in word mode, it needs to know if the last word read contains one or two bytes. If ODD is true, the host is informed that the last word is only half full, or one byte.

See the paragraph "Interrupts" for a description of the DMA:INT signal. Briefly, this interrupt is a means of calling attention to certain end conditions that may be generated by a peripheral on a host read.

The C:END- bit from the DMA controller is enabled by the EN:END- signal from the Z8. When the DMA controller senses an end condition during a host read, it interrupts the Z8 and drives C:END true. This line is connected to the enable line of a 3-state driver. The input to the driver is EN:END-. This effectively performs an inverting NAND function (END- true only if EN:END- true and C:END- true). The EN:END- signal is set up before DMA begins, and the 3-state enable line going true (low) controls the state of END-. If EN:END- is true, it takes 25 nanoseconds to pull END- low from the leading edge of C:END-.

In addition to the control inputs from the Z8, described in the preceding paragraphs, three other inputs (IB:D0, IB:D1, and READY) are provided for the DMA controller.

The IB:D0 and IB:D1 signals are the two extra HP-IB chip bi-directional data bits (bits 9 and 10). In the host write direction, these signals specify ATN and EOI data. In the read direction, the DMA controller uses them to detect the following END conditions:

IB:D0	IB:D1	Condition
0	0	No end condition (normal data)
1	1	Last byte of record
1	0	Last byte of subgroup
0	1	Secondary address

If one of the end conditions occurs, the DMA controller will halt and assert DMA:INT-, which informs the Z8 of the end condition. The Z8 can interrogate the HP-IB chip to determine the cause of the DMA interrupt.

READY is a composite signal which indicates that both the HP-IB and BIC chips are ready to transfer a data byte (= IOEND- * DMARQ * RDY). The READY, DMA:PAUSE, DMA:RST, and DMA:READ signals are double buffered, because they are asynchronous inputs that are monitored by the DMA controller at any given moment. The other inputs

to the DMA controller are also asynchronous, but are guaranteed not to change once the DMA cycle begins.

Regardless of the current state, a RESET input will force state 04 hex (all states are pin 12 = LSB, pin 19 = MSB). State 04 asserts RST:ACK (Reset Acknowledge), which resets the Odd/Even flip-flop. Once RESET is released, the card idles, waiting for PAUSE to be de-asserted and for READY to become true. When both of these conditions exist, the DMA controller will begin a DMA cycle in the direction specified by READ. Note that READ must be stable before PAUSE and RESET are made false.

The DMA controller will now perform a DMA read or write, and is in "free run" mode. The DMA cycle is running independent of the HP-IB chip, BIC, or Z8 (except for the RESET input) until the byte has been transferred. The READY signal has guaranteed that there is room in the appropriate HP-IB chip and BIC FIFO registers, so the transfer should never "hang up". The read and write cycles are tailored to meet the worst-case timing of the BIC and HP-IB chip. Refer to figures 5-1, 5-2, 5-3, and 5-4.

DMA Write

A DMA write timing diagram for the DMA controller is shown in figure 5-5. In the host write direction, the DMA controller must first extract data from the BIC. It does this by asserting DTR- in state 20. BIC timing dictates that data from the BIC can be delayed as much as 200 nanoseconds following the assertion of DTR-, thus DTR- must be held true for three states (68 nanoseconds x 3 = 204). Q0 and Q1 are used in states 21 and 22 as wait qualifiers, thus the DMA controller can leave DTR- asserted and still distinguish between states. After the 200 nanosecond wait, IOGO- is asserted to inform the HP-IB chip that there is valid BIC data on the bus. The HP-IB chip timing needs 150 nanosecond to accept the data, so IOGO- is held asserted for three states. During the last of these three states, DTR- is released, because the BIC can only remove data within 20 nanoseconds maximum. This allows the BIC FIFO register one extra state to recover and become ready for the next DMA transfer. This completes a DMA write cycle, and the DMA controller returns to the IDLE loop and waits for the READY signal.

Refer to the BIC DMA write timing diagram (figure 5-2). The timing values are defined as shown below (recall that RDY- is asserted by the BIC and DTR- is asserted by the DMA controller. DATA is supplied by the BIC).

t1: RDY- assertion to DTR- assertion

The BIC requires that this time be no less than zero. Because RDY- is combined with HP-IB chip signals, synchronized with CCLK, and then input to the DMA controller which again samples it at CCLK-, a non-zero time can be guaranteed (RDY- is gated and double-buffered).

t2: DTR- assertion to RDY- removal

t3: DTR- removal to RDY- assertion

The BIC can become ready as quickly as 40 nanoseconds after removal of DTR-. Because the first six bytes into an empty FIFO will have about 150 nanoseconds each (900 nanoseconds total), time t3 is not critical to DMA operation.

t4: DTR- assertion to DATA

The BIC provides data to the internal data bus within 0 to 200 nanoseconds after DTR- is asserted.

t5: DTR- removal to data float

The BIC releases the data bus within 130 nanoseconds of DTR- removal.

t6: Data hold time from DTR- removal

The BIC keeps valid data on the data bus for at least 20 nanoseconds after the removal of DTR-. The t5 timing allows 130 nanoseconds maximum for t6.

DMA Read

A DMA read timing diagram for the DMA controller is shown in figure 5-6.

A DMA read shares the same idle loop as a DMA write. The DMA controller must first extract data from the HP-IB chip on a read. It does this by asserting IOGO-. When data is being written to the BIC, as in a DMA read, the BIC latches the data on the trailing edge of DTR-; thus, DTR- can be asserted now, and removed (de-asserted) once the data is on the internal data bus. State A8 in figure 5-6 demonstrates this.

The IOGO- signal must be held true for 140 nanoseconds (three states) to allow the HP-IB chip time to drive data. IOGO- is asserted and an internal 2-bit counter is started to count off two wait states. (Asserting COUNT starts the counter.) States A8 through AA show DTR- and IOGO- asserted and the counter running.

After state AA, the HP-IB chip data is on the bus, and DTR- can be removed, allowing the BIC to latch the data. The BIC has a data setup time of 20 nanoseconds. Because data is guaranteed 140 nanoseconds after IOGO-, a delay of three states (3 x 68 = 204) is implemented, thus giving the BIC at least 60 seconds of setup time. State 80 shows the DMA controller removing DTR- while continuing to drive the data bus. Because the BIC needs the data to remain on the bus for 45 nanoseconds after removal of DTR-, state 80 guarantees that 68 nanoseconds (one state) of hold time will be provided.

After state 80, the DMA controller returns to its idle loop. Beginning at state 00, the HP-IB chip needs 140 nanosceconds to "float" the data bus (return it to neutral with no data passing in either direction). Because it takes several microseconds to initiate a write cycle, BIC data cannot collide with HP-IB chip data.

Refer to the BIC DMA read timing diagram in figure 5-1. The timing values are defined as follows: (Recall that RDY- is asserted by the BIC and DTR- is asserted by the DMA controller, and that DATA is provided by the HP-IB chip.):

t1: RDY- assertion to DTR- assertion

The BIC requires this time be no less than zero. Because RDY- is combined with HP-IB signals, synchronized with CCLK-, and then input to the DMA controller which again samples it at CCLK-, a non-zero time is guaranteed (RDY- is gated and double-buffered).

t2: DTR- assertion of RDY- removal

t3: DTR- removal to RDY- assertion

The BIC can become ready as quickly as 40 nanoseconds after removal of DTR-. Because the first six bytes into an empty FIFO will have about 150 nanoseconds each (900 nanoseconds total), time t3 is not critical to DMA operation.

t4: DATA setup time (before DTR- is removed)

The BIC requires that the data from the HP-IB chip is present on the data bus at least 20 nanoseconds before DTR- is de-asserted. Because the HP-IB guarantees that it can drive the data bus within 150 nanoseconds of the time when IOGO- is set true (asserted), IOGO- needs to be asserted for 170 nanoseconds before DTR- can be removed.

t5: DTR- removal to data float

The BIC has a hold time on data of 45 nanoseconds, and the fastest that the HP-IB chip can remove data from the bus following the de-assertion of IOGO- is 25 nanoseconds. Therefore, IOGO- (and DATA) need to remain asserted for 20 nanoseconds following the removal of DTR-. This is accomplished via state 80.

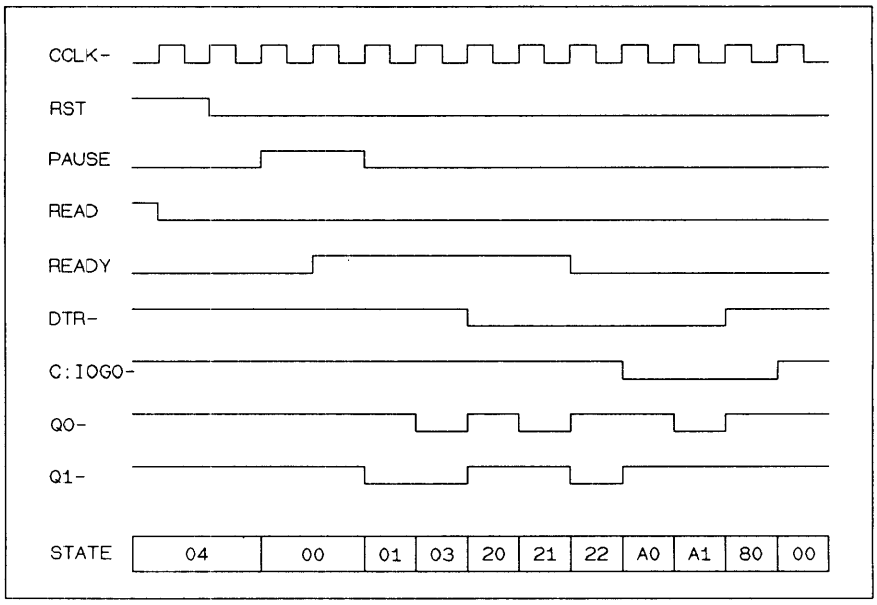


Figure 5-5. DMA Controller Host Write Timing

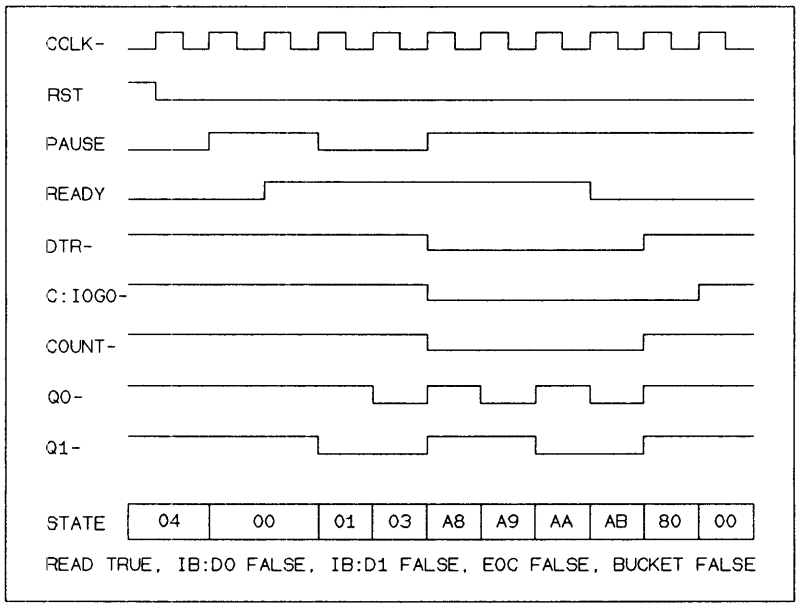


Figure 5-6. DMA Controller Host Read Timing

6 Removal and Replacement

Caution

There are no operator adjustments or controls on the HP 27110B card. Service, troubleshooting, or other maintenance of the HP 27110B should only be done by qualified electronic maintenance personnel.

Warning

Removal and replacement of the HP 27110B card should only be done with all power removed from the host computer. Power connected to the host computer in normal operation is dangerous and can cause serious injury or death if not switched off during service operations.

Caution

Static electricity can cause permanent damage to, or catastrophic failure of the HP 27110B card. All work performed on electronic assemblies such as the HP 27110B must be at static-safe work stations that have correct static grounding for the card and the service person. Keep the card in a static protection bag whenever it is possible. Use the two plastic ejector levers to handle the card when it is not in a static protection bag or in the computer.

Required Tools

No special tools are required for removal and replacement of the HP 27110B card.

Repair Environment

The HP 27110B should be removed from the host computer in a clean and dry repair facility.

Removal and Replacement Procedures

Refer to the manual for the host computer for specific instructions for removal and replacement of the HP 27110B. The HP 27110B should be removed from the host computer by lifting up the two plastic levers on each end of the edge of the HP 27110B card. Tilting these two levers up gently should remove the HP 27110B out of the host computer card slot. To replace the card, put the card in the original slot for the HP 27110B and press it securely into the slot connector.

Note

The resistor network described in the following paragraph is part of the configuration of the HP 27110B. Refer to Chapter 3 for instructions on positioning the resistor network.

One part on the HP 27110B is designed to be moved. A resistor network in an 18-pin dual in-line package may be installed in the socket marked U123 or in the socket marked RESISTOR STORAGE. This part can be removed by pulling up carefully. Be very careful when you move this part. The resistor network must be installed in a socket very carefully to avoid bending the pins.

7 Adjustments

There are no field-adjustable parts on the HP 27110B. The one adjustable control on the card is set at the factory, and it should not be adjusted except at the factory. Adjustable resistor, R10, is adjusted and sealed at the factory.

8 Troubleshooting

Caution Service, troubleshooting, or other maintenance of the HP 27110B should only be done by qualified electronic maintenance personnel.

Warning **Removal and replacement of the HP 27110B card should only be done with all power removed from the host computer. Power connected to the host computer in normal operation is dangerous and can cause serious injury or death if not switched off during service operations.**

Caution Static electricity can cause permanent damage to, or catastrophic failure of the HP 27110B card. All work performed on electronic assemblies such as the HP 27110B must be at static-safe work stations that have correct static grounding for the card and the service person. Keep the card in a static protection bag whenever possible. Use the two plastic extractor levers to handle the card when it is not in a static protection bag or in the computer.

Card Self-Test

The HP 27110B card contains on-board intelligence for conducting a card self-test. I/O card self-tests are generally initiated upon system power-up or reset; consult your system manuals for specific details.

Although the circuitry across card connectors is not tested, the HP 27110B card self-test includes the following:

- A CRC algorithm that confirms the contents and accuracy of ROM contents.
- A procedure that verifies that reads and writes can be performed on all RAM locations.
- Functional tests on all VLSI chips.
- Data transfer tests between appropriate VLSI chips.
- The onboard Z8 processor is exercised.

The HP 27110B card contains a Light Emitting Diode (LED) that indicates self-test status. Access to and observation of this LED is limited to qualified service personnel.

LED Interpretation

When the card self-test is started, the card LED should light for approximately one second, indicating that self-test is in progress, and then go out. This sequence indicates that the card passed self-test.

If the LED does not light at all, or lights and stays lit, the card is defective and should be replaced.

9 Replaceable Parts

This chapter has information for ordering replaceable parts for the HP 27110B card. Table 9-1 has a list of replaceable parts, table 9-2 has the names and addresses of the manufacturers indexed by the code numbers used in table 9-1, and figure 9-1 shows the locations of the parts on the HP 27110B card.

Replaceable Parts

Table 9-1 has a list of replaceable parts in reference designation order. The following information is listed for each part:

1. Reference designation of the part.
2. The Hewlett-Packard part number.
3. Part number check digit (CD).
4. Total quantity (QTY).
5. Description of the part.
6. A five-digit manufacturer's code number of a typical manufacturer of the part. Refer to table 9-2 for a cross-reference of the manufacturers.
7. The manufacturer's part number.

Ordering Parts

To order replacement parts or to obtain information on parts, address the order or inquiry to the nearest Hewlett-Packard Sales and Support Office (Sales and Support Offices are listed at the back of this manual).

To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number (with the check digit), and indicate the quantity required. The check digit will insure accurate and timely processing of your order.

To order a part that is not listed in the replaceable parts table, specify the following information:

1. Identification of the unit with the part (refer to the product identification information supplied in Chapter 1).

2. Description and function of the part.

3. Quantity required.

Table 9-1. HP 27110B Replaceable Parts List

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	27110-60301	5	1	PCA-HP-IB	28480	27110-60301
C1	0160-4835	7	28	CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C2	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C3	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C4	0180-0228	6	1	CAPACITOR-FXD 22UF+-10% 15VDC TA	56289	150D226X9015B2
C6	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C7	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C8	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C9	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C10	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C11	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C12	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C13	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C14	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C15	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C16	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C17	0160-4795	8	2	CAPACITOR-FXD 4.7PF +-.5PF 100VDC CER	28480	0160-4795
C18	0160-4795	8		CAPACITOR-FXD 4.7PF +-.5PF 100VDC CER	28480	0160-4795
C19	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C20	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C21	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C22	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C23	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C24	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C25	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C26	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C28	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C29	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C30	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C31	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C32	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C33	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
CR1	1990-0968	9	1	LED-LAMP LUM-INT=1.5MCD IF=15MA-MAX	28480	HLMP-5060
EXRIGHT	0403-0527	2	1	CIO EXT HNDL BLK	28480	0403-0527
EXLEFT	0403-0545	4	1	EXTR-PC BD ORN NYL 1.6-MM-BD-THKNS	28480	0403-0545
EXRIGHT	1480-0116	8	2	PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116
EXLEFT	1480-0116	8		PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116
J1	1251-7276	0	1	CONN-POST TYPE .100-PIN-SPCG 80-COUNT	28480	1251-7276
J2	1252-1740	3	1	CONN-POST TYPE .100-PIN-SPCG 80-COUNT	22526	78228-001
R1	0698-3445	2	2	RESISTOR 348 1% .125W F TC=0+-100	24546	CT4-1/8-T0-348R-F
R2	0698-0084	9	1	RESISTOR 2.15K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-2151-F
R3	0698-3445	2		RESISTOR 348 1% .125W F TC=0+-100	24546	CT4-1/8-T0-348R-F
R5	0811-3716	2	5	RESISTOR ZERO OHM 22 AWG LEAD DIAG	28480	0811-3716
R6	0811-3716	2		RESISTOR ZERO OHM 22 AWG LEAD DIAG	28480	0811-3716
R7	0811-3716	2		RESISTOR ZERO OHM 22 AWG LEAD DIAG	28480	0811-3716
R8	0757-0199	3	2	RESISTOR 21.5K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-2152-F
R9	0757-0199	3		RESISTOR 21.5K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-2152-F
R10	2100-3869	1	1	RESISTOR-TRMR 100K 10% C SIDE-ADJ 17-TRN	28480	2100-3869
R11	0811-3716	2		RESISTOR ZERO OHM 22 AWG LEAD DIAG	28480	0811-3716
R12	0811-3716	2		RESISTOR ZERO OHM 22 AWG LEAD DIAG	28480	0811-3716
S1	3101-2243	6	1	SWITCH-RKR DIP-RKR-ASSY 8-1A .05A 30VDC	28480	3101-2243

Table 9-1. HP 27110B Replaceable Parts List (continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U11	1820-2862	7	2	IC RCVR TTL S BUS OCTL	27014	DS3667N
U12	1820-2862	7		IC RCVR TTL S BUS OCTL	27014	DS3667N
U13	1820-1633	8	3	IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U14	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U15	1820-2739	7	1	IC GATE TTL ALS NOR QUAD 2-INP	01295	SN74ALS02N
U23	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U24	1820-2634	1	2	IC INV TTL ALS HEX	01295	SN74ALS04BN
U31	1820-2975	3	1	IC GATE-ARY CMOS	S0166	C-2000
U33	1820-0684	7	1	IC INV TTL S HEX 1-INP	01295	SN74S05N
U34	1820-2775	1	1	IC GATE TTL ALS NAND TPL 3-INP	01295	SN74ALS10N
U35	1820-2657	8	1	IC GATE TTL ALS OR QUAD 2-INP	01295	SN74ALS32N
U43	1820-2557	7	1	IC DRVR TTL AS LINE DRVR HEX 2-INP	01295	SN74AS804BN
U44	1820-3465	8	1	IC FF TTL ALS D-TYPE POS-EDGE-TRIG COM	01295	SN74ALS174N
U45	1820-4875	6	1	ICFGM PAL16R8-2	28480	1820-4875
U51	1820-2724	0	2	IC LCH TTL ALS TRANSPARENT OCTL	01295	SN74ALS573BN
U53	1820-4222	7	1	IC-Z8 12MHZ 8BIT MCU W/4K MASKED ROM	07653	Z8611-12PS MASKED
U55	1820-3443	2	1	IC DRVR TTL ALS AND HEX 2-INP	01295	SN74AS808AN
U61	1820-3707	1	2	IC DRVR TTL ALS LINE OCTL	01295	SN74ALS541N
U71	1820-3905	1	1	IC TRANSCEIVER TTL ALS BUS OCTL	01295	SN74ALS623AN
U74	1820-3258	7	1	IC DCDR TTL ALS BIN 3-TO-8-LINE 3-INP	01295	SN74ALS137N
U75	1820-1568	8	2	IC BFR TTL LS BUS QUAD	01295	SN74LS125AN
U81	1820-2724	0		IC LCH TTL ALS TRANSPARENT OCTL	01295	SN74ALS573BN
U83	1TL1-0006	6	1	IC-MEDUSA	28480	1TL1-0006
U85	1820-2488	3	3	IC FF TTL ALS D-TYPE POS-EDGE-TRIG	01295	SN74ALS74AN
U91	1818-3198	9	1	IC CMOS 65536 (64K) STAT RAM 150-NS 3-S	S4013	HM6264P-15
U93	1820-2634	1		IC INV TTL ALS HEX	01295	SN74ALS04BN
U95	1820-2488	3		IC FF TTL ALS D-TYPE POS-EDGE-TRIG	01295	SN74ALS74AN
U101	27110-81014	1	1	BURNIN 1818-3604	28480	27110-81014
U102	1820-2058	3	2	IC TRANSCEIVER TTL S INSTR-BUS IEEE-488	04713	MC3448AL
U103	1820-2058	3		IC TRANSCEIVER TTL S INSTR-BUS IEEE-488	04713	MC3448AL
U104	1820-1568	8		IC BFR TTL LS BUS QUAD	01295	SN74LS125AN
U105	1820-2488	3		IC FF TTL ALS D-TYPE POS-EDGE-TRIG	01295	SN74ALS74AN
U114	1820-3707	1		IC DRVR TTL ALS LINE OCTL	01295	SN74ALS541N
U123	1810-0081	7	1	NETWORK-RES 18-DIP MULTI-VALUE	28480	1810-0081
U124	1810-0235	3	1	NETWORK-RES 16-DIP 2.2K OHM X 15	73138	898-1-R2.2K
U223	1820-2485	0	1	IC TRANSCEIVER TTL LS INSTR-BUS IEEE-488	01295	SN75 160AN
XU101	1200-0567	1	1	SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
XU106	1200-0539	7	2	SOCKET-IC 18-CONT DIP DIP-SLDR	28480	1200-0539
XU123	1200-0539	7		SOCKET-IC 18-CONT DIP DIP-SLDR	28480	1200-0539
Y1	0410-1565	5	1	CRYSTAL-QUARTZ 12.000 MHZ HC-18/U-HLDR	28480	0410-1565
	5180-7266	1	1	PC BOARD	28480	5180-7266

Table 9-2. Code List of Manufacturers

Code	Manufacturer	Location	
S0166	Fuji Kohki Ltd	Japan	
S4013	Hitachi America Ltd.	Sunnyvale, CA	94086
01295	Texas Instruments Inc.	Dallas, TX	75265
04713	Motorola Semiconductor Products	Phoenix, AZ	85008
07653	Fidelity Chemical Products Co	Newark, NJ	07114
22526	DuPont Connector Systems	Camp Hill, PA	17011
24546	Corning Electronics	Santa Clara, CA	95050
27014	National Semiconductor Corp	Santa Clara, CA	95052
28480	Hewlett-Packard Co., Corporate Hq	Palo Alto, CA	94304
56289	Sprague Electric Co	Palo Alto, CA	94304
73138	Beckman Industrial Corp	Fullerton,CA	92632
80509	Avery Label Co	Monrovia, CA	91016

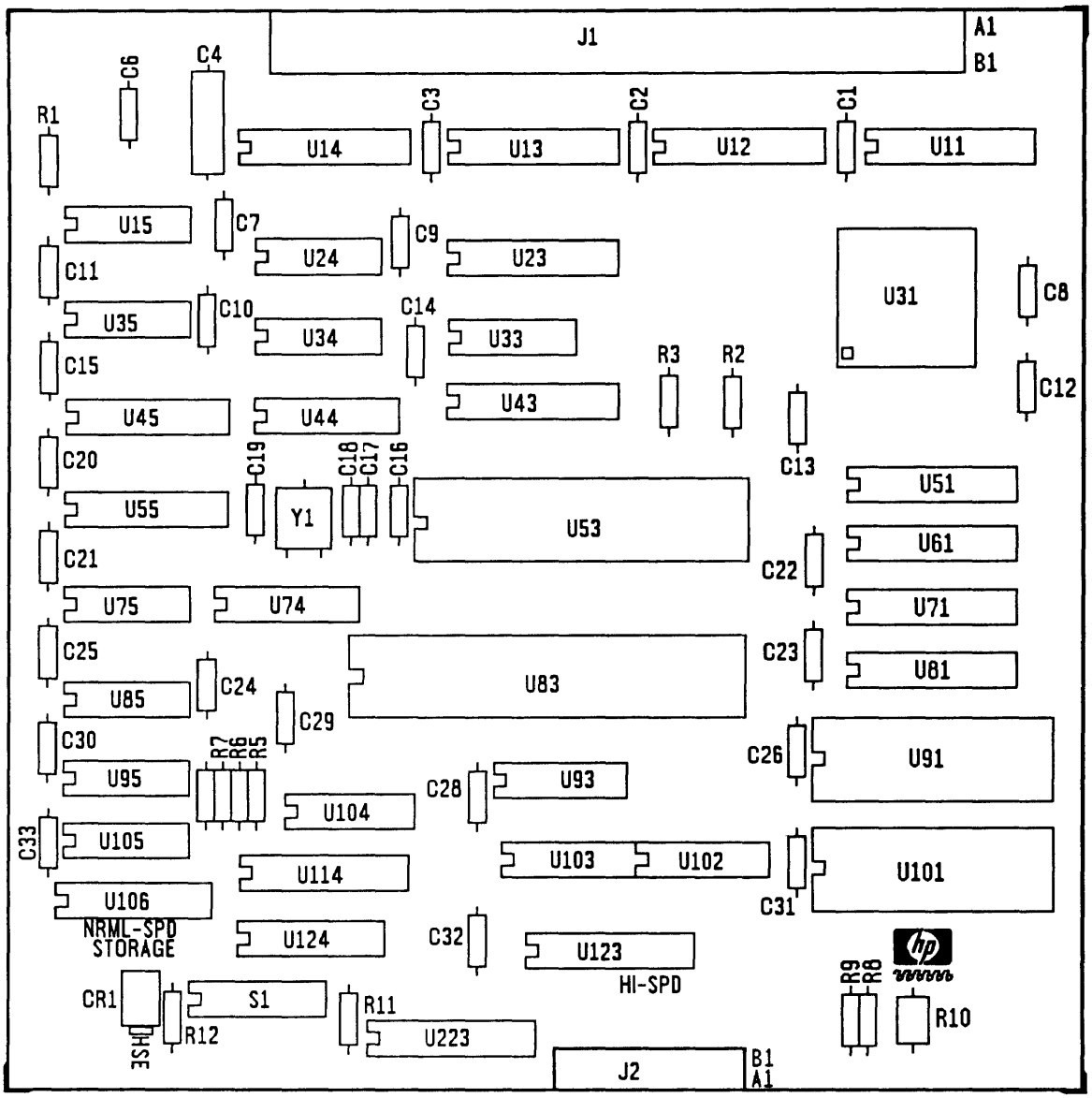


Figure 9-1. HP 27110B Parts Location Diagram

10 Reference

This chapter contains reference information that may help you to use and maintain the HP 27110B HP-IB Interface card.

HP Computer Users Documentation Index

Hewlett-Packard publishes a Computer Users Documentation Index that lists all HP computer printed matter. This index is available free. Ask your Hewlett-Packard representative. The index is available from the Hewlett-Packard Direct Marketing Division, P.O. Box 60008, Sunnyvale, California 94088; Telephone: 800-538-8787 (California: 408-738-4133).

Note

The HP Direct Marketing Division mentioned above will send you a copy of its Computer Users Catalog free on request. This catalog lists computer books and learning aids.

HP-IB Tutorial Description

Hewlett-Packard has published a comprehensive book about the HP-IB with the title *Tutorial Description of the Hewlett-Packard Interface Bus*. The HP part number is: 5952-0156. Ask your HP representative to help you get a copy.

11 Product History

The HP 27110B HP-IB Interface card is similar to the 27110A HP-IB Interface card. However, the differences are extensive enough to prevent using the manual for one card as a reference for the other card.

The HP 27110B card has all of the capability of the 27110A card. But the 27110A card does NOT have all the capability of the 27110B. Differences between the two cards are shown in the respective specifications tables.

The HP 27110B card part number 27110-60301 does NOT have the option of allowing the "No-listener-detect" capability to be selected. The HP 27110B card part number 27110-60201 DOES have the option of allowing the "No-listener-detect" capability to be selected.

12 Diagrams

This chapter contains HP 27110B functional block and schematic logic diagrams, and an algorithmic state diagram on the DMA controller.

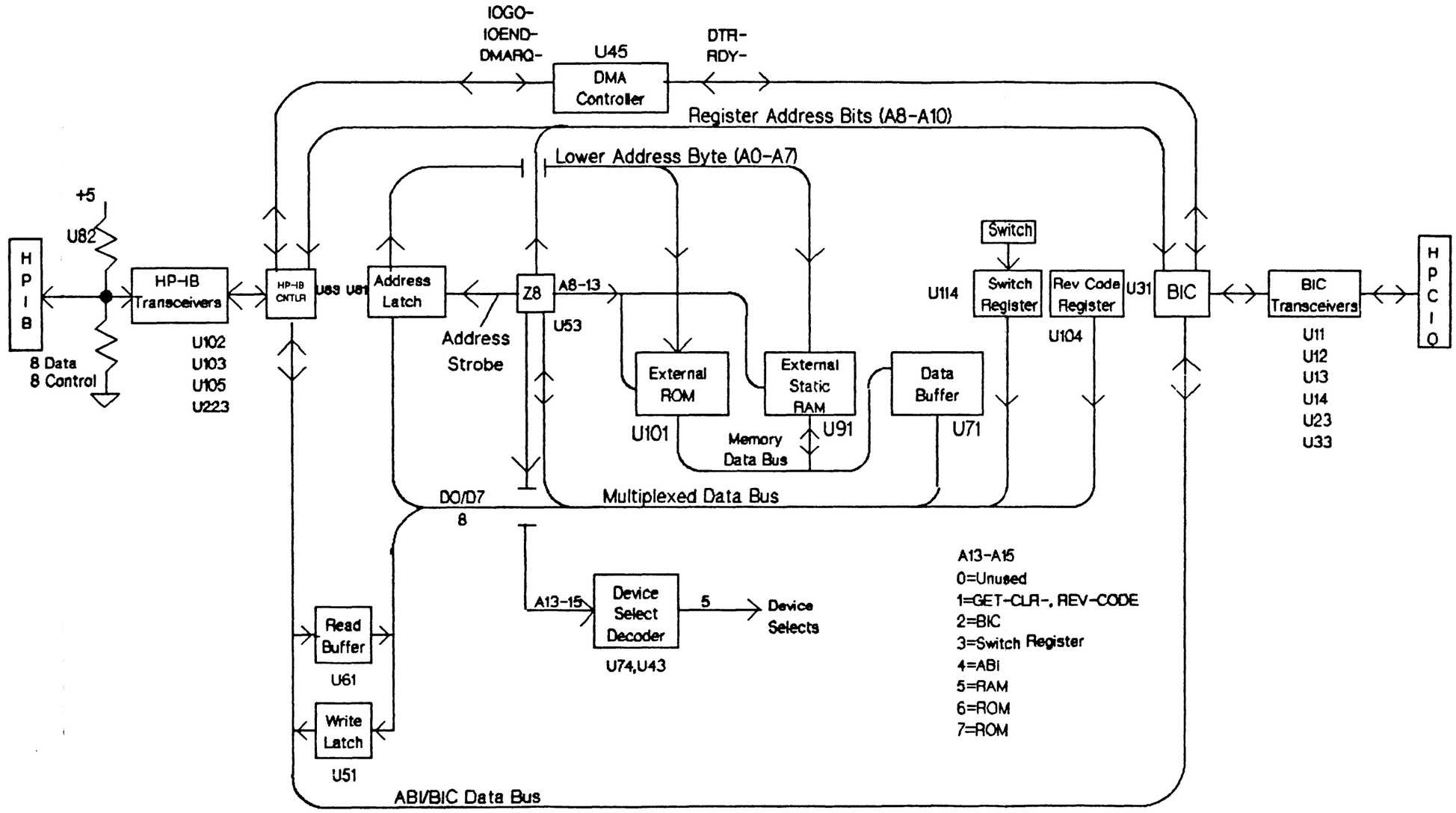


Figure 12-1. Functional Block Diagram

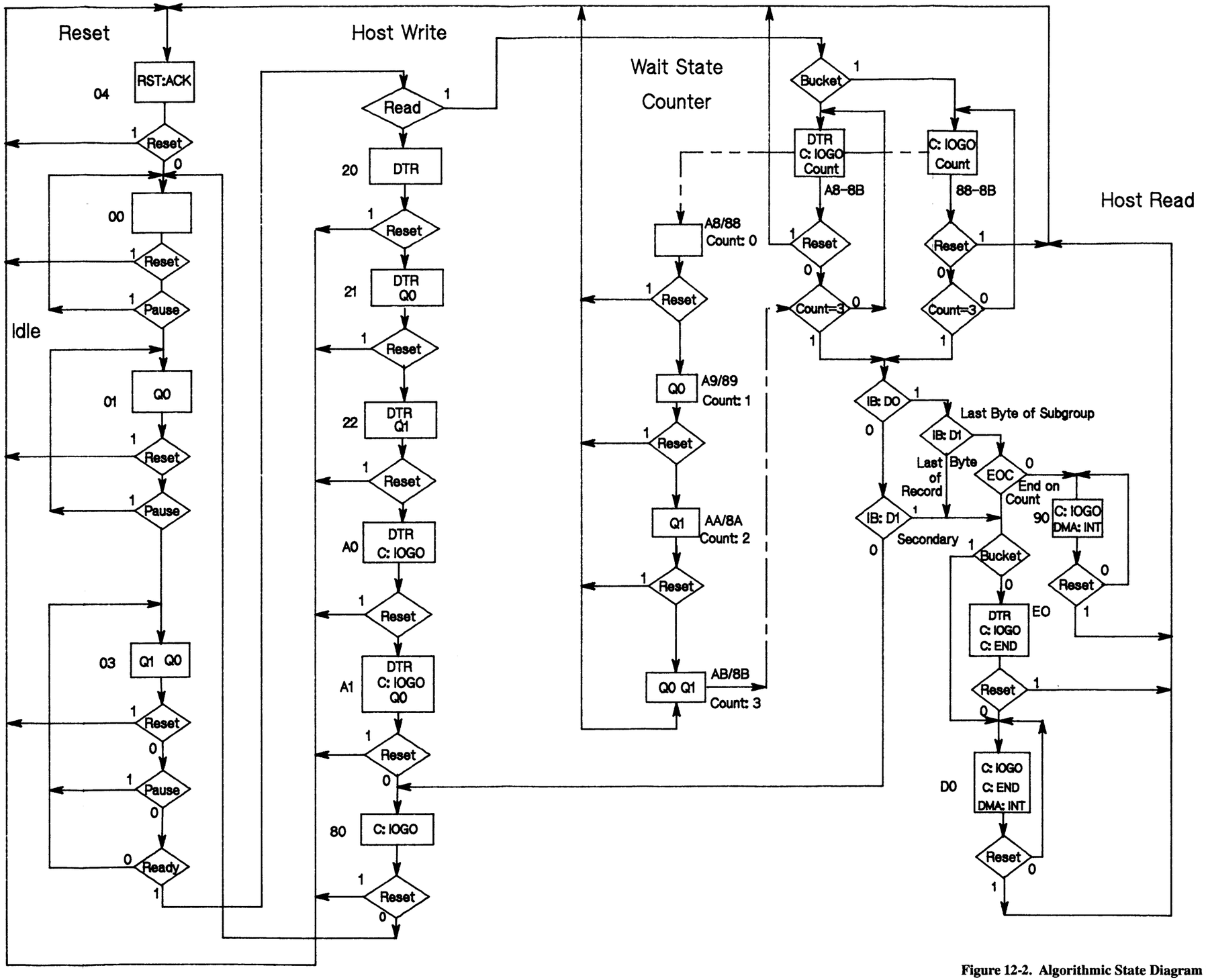


Figure 12-2. Algorithmic State Diagram for DMA Controller

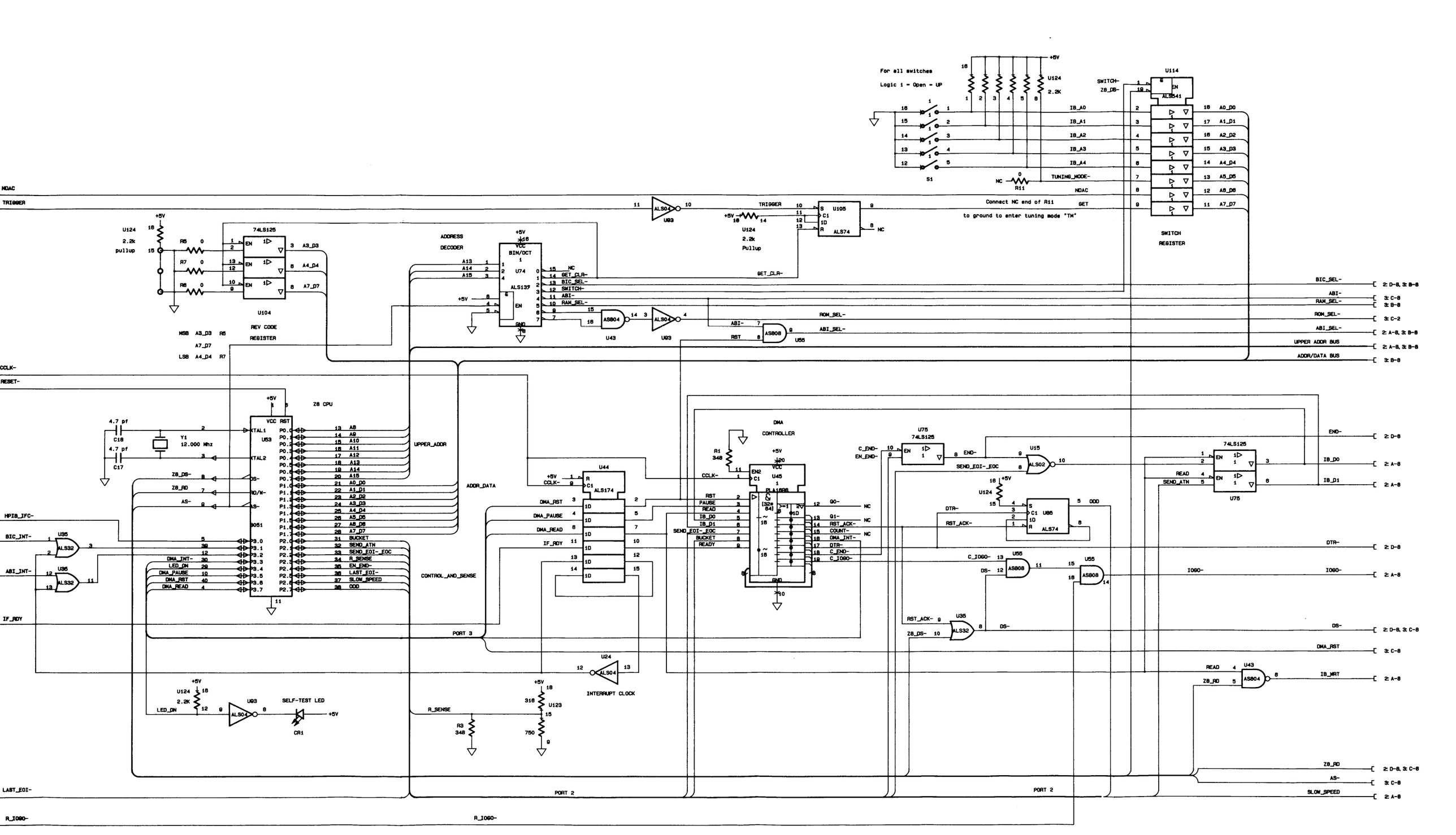


Figure 12-3. Schematic Diagram (sheet 1 of 3)

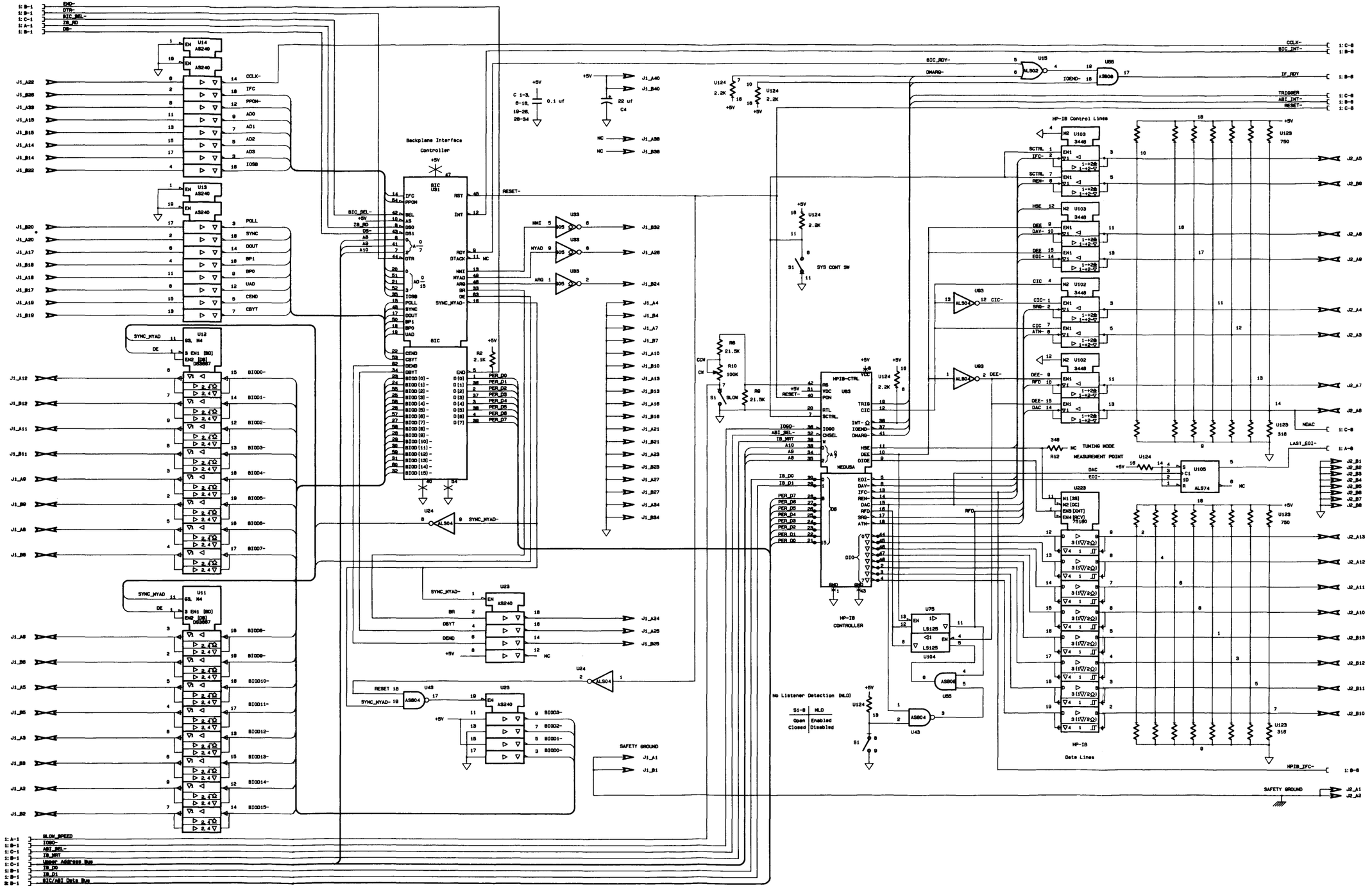


Figure 12-3. Schematic Diagram (sheet 2 of 3)

Figure 12-3. Schematic Diagram (sheet 3 of 3)

Index

Reader Comment Sheet

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