HEWLETT PACKARD

Valid Logic Systems vs HP EE DesignCenter

Competitive Report June, 1989

Electronic Design Division
Fort Collins, Colorado
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For Internal Use Only

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Introduction

This report provides competitive information on Valid Logic Systems in comparison to HP's EE DesignCenter products. The information contains both a business analysis and technical (product) analysis. The report is a reference tool for EDD's sales organization and is intended for HP internal use only.

The business analysis section contains both statistical information and background material on Valid. Business information was obtained through company press releases, company brochures, reports to the shareholders, outside research consultants and industry analysts, and customer contacts. The report is HP's interpretation of information in the public domain and information obtained through outside consultants. HP does not guarantee the information's completeness, timeliness, or accuracy.

The document also contains technical information on products offered by Valid as compared to EDD's product offerings. Product comparisons are based on technology comparisons, as opposed to product feature comparisons. Product strengths and weaknesses are also included. The technical information was obtained through field-based systems engineers and factory-based support engineers research.

Executive Summary

Valid Logic Systems, a pioneer in the electronic design automation industry, has benefited in recent years from new management and policies designed to strengthen and expand its current product lines. The major thrust of which was a series of acquisitions and third-party agreements. With four major acquisitions in the last two years, Valid has created a full EDA product offering including, CAE, PCB CAD, and IC CAD tools.

One of Valid's key advantage's is offering products on two standard platforms, DEC and Sun. Valid's products also support widely used operating and networking systems as well as computer languages, such as the UNIX and VMS operating systems, Ethernet local area network, and C and Pascal languages, respectively.

Since Valid's acquisition of Telesis, and the appointment of Douglas Hajjar as CEO, Valid's revenue has increased by 66% making it one of the fastest growing CAE/CAD company's in the marketplace. One of Hajjar's goals is to surpass Mentor Graphics in the next 2 years. Valid still faces an uphill battle competing with companies that have greater resources, both in terms of financial strengths and field presence.

Valid Strengths

- Aggressive business management team
- DEC/Sun platforms
- IC CAD/CAE products
- Hierarchical design
- Front to back end integration

HP Strengths

- Product-line integration
- Open links to other vendors' CAD systems
- Service and support
- On-line rule checking
- Superior provider of links to test
- Physical design graphic performance & acceleration

Company Background

History

Valid Logic Systems, formed in 1981, is one of the three pioneers in the electronic computer-aided engineering (CAE) market, along with Mentor and Daisy. The company was founded by Dr. Jared Anderson, Dr. Curtis Widdoes, Dr. Thomas McWilliams, Jeffrey Rubin, and Ray King. Valid's original intent was designing and marketing tools focused at the integrated circuit (IC) design engineer. In the late 1970's, two of Valid's founders developed a methodology called Structured Computer-Aided Logic Design (SCALD), allowing designers to represent groups of components and their interconnections as unique symbols. Valid developed a proprietary 68000-based UNIX workstation to implement this technology. The SCALDsystem and SCALDstar were based on industry standards: UNIX for the operating system, Ethernet for network communication, and C and Pascal languages for software development.

Valid's revenues grew explosively in the early years, but in 1985 Valid experienced difficulties including being tied to proprietary workstations, management turnover, and very little marketing and sales support for its products.

In 1987 Valid completed a port to DEC and Sun workstations and in May 1987, Valid merged with Telesis Systems Corporation, a maker of PCB tools. With the merger, Valid appointed as president and CEO, W. Douglas Hajjar, formerly Telesis's president and CEO. As part of the reorganization, hardware modeling development was made into a separate company called Logic Modeling Systems.

In 1988, Valid acquired several new companies to broaden their product line. Valid acquired GE's Calma division, a pioneer product in IC design software, consisting primarily of Calma's GDS-II (Graphics Design System) and EDS-II (Electronics Design System). Valid also acquired Integrated Measurement Systems Inc. (IMS), a manufacturer of application-specific integrated circuit (ASIC) device verification systems. Valid's last acquisition of 1988, was Analog Design Tools Inc. (ADT), a manufacturer of computer-aided engineering (CAE) systems for analog circuit design.

Industry analysts are split in their opinions on Valid's acquisitions. Some believe that Valid moved too quickly and should have concentrated first on making its core business more competitive. But most analysts approve of Valid's buying binge.

General Information

Headquarters: Valid Logic Systems, Inc.
2820 Orchard Parkway
San Jose, CA 95134
(408) 432-9400

President and CEO: W. Douglas Hajjar

Number of Employees

Valid: approximately 510 prior to Calma, IMS, and ADT acquisitions

R & D:	104
Administration:	73
Sales & Marketing:	291
Manufacturing:	42

Valid Calma acquisition: approximately 100

R & D:	40
Sales & Marketing:	50
Manufacturing & Administration:	10

Valid IMS acquisition: approximately 125

Valid ADT acquisition: approximately 140

Prior to the Calma acquisition, Valid had an installed base of approximately 8,300 seats. Valid expects to acquire approximately 2,700 GDS-II installed seats from the Calma acquisition and approximately 450 installed seats from the IMS acquisition.

Table 1 shows the regional segmentation of Valid's installed base, prior to the acquisitions of Calma, IMS, and ADT, in units shipped. The total shipped to date figures are cumulative, while the other figures represent the number shipped in that year. The table also lists figures for systems shipped each year. The last column presents Valid's compounded annual growth rate (CAGR) in regional segmentations of its market. N/A represents not applicable.

Table 1: Regional Segmentation of Valid Installed Base

	1983	1984	1985	1986	1987	CAGR 83-87
World-wide Workstations	325	1020	990	1260	688	21%
North America	260	774	696	585	346	7%
Europe	49	197	248	438	216	45%
Far East	16	49	47	225	120	65%
Rest of World	0	0	0	13	6	n/a
Total Shipped to date	325	1345	2089	3349	3709	84%
CAE Systems	325	933	888	1176	589	16%
PCB Systems	n/a	n/a	n/a	11	76	n/a
IC Systems	n/a	87	102	74	23	n/a

Source: Dataquest, July 1988

Target Markets

Valid's largest customers are computer companies because Valid's software architecture permits porting to the systems manufactured by those customers. The largest examples are DEC, Sun and Compaq. Valid is also strong in the aerospace industry and is expected to grow in the semiconductor market as a result of the Calma acquisition. Valid's acquisition of IMS will enable them to become a leading supplier of complete design-to-test solutions for design engineers.

- **CAE** - computer-aided engineering
- **CAD** - computer-aided design
- **PCB** - printed circuit board layout
- **CAT** - computer-aided test

Technology Partners

Valid hopes to strengthen and expand its current product lines with its new acquisitions and third-party agreements into the full spectrum of EDA products

- **Teradyne** — agreement to port Teradyne Lasar-6 simulation system onto Valid's SCALDsystems. Also, made Valid's RealCHIP hardware modeling products available to the Lasar-6 simulator.
- **Siemens** -- technology exchange agreement in which Siemens installed Valid's SCALD Graphics Editor on Siemens' computers, and relabeled it for sale as Siemens' product.
- **Logic Modeling Systems Inc.** — exclusive, perpetual license covering Valid's hardware modeling technology in exchange for specified fees and royalties. Valid holds equity interest in the company.
- **Denies Resources** — licensing and marketing agreement for ValidBLOCKS, ECAD/SDA systems (design rule checker), Logic Automation, and Quadtree and EPIC Technologies (TIMEMILL).
- **DEC** — cooperative marketing program
- **Sun Microsystems** — cooperative marketing program allowing Valid to be promoted by Sun including space on Sun's exhibition stands.
- **Structural Dynamics Research Corporation (SDRC)** — joint reference for sales aimed at electro-mechanical manufacturers. Agreement includes development of interfaces between Valid's Allegro PCB CAD product and SDRC's I-DEAS mechanical CAD product.
- **Gateway Design Automation Corporation** — joint marketing agreement aimed at design engineers using Gateway's Verilog and Verilog-XL logic simulators with Valid's RealCHIP and RealCHIP II hardware modeling products.
- **Test Systems Strategies Inc. (TSSI)** — joint marketing agreement linking Valid's EDA products with TSSI's TestBridge test development series.
- **Interleaf** — cooperative marketing agreement for Valid to interface Interleaf's Workstation Publishing Software and Technical Publishing Software to the ValidGED graphics editor.

Financial and Market Share Information

Financials

Since the acquisition of Telesis in 1987, Valid's revenue has increased by 66%. Valid currently is the fastest-growing, broad-based player in its industry. Sales in 1988 soared 63% exceeding $108 million, and Valid expects to pass the $200 Million mark this year. Before long, Valid intends to replace Mentor Graphics as No. 1.

Table 2 shows regional segmentation of revenue for Valid from 1983 to 1987. The figures in the tables represent millions of dollars per year.

Table 3: Regional Segmentations of Valid's Revenue

Valid	1983	1984	1985	1986	1987	CAGR 83-87
Total Revenues	16.1	48.2	56.8	60.9	67.3	43%
North America	13.1	36.2	26.4	28.0	37.1	30%
Europe	2.0	10.1	20.3	21.3	22.1	82%
Far East	1.0	2.0	10.1	11.1	7.5	65%
Rest of World	0	0	0	.6	.7	n/a

Source: Dataquest, July 1988

Market Share

After 3 years of declining market share and significant losses, Valid began turning around its business in 1987 with a new CEO and a business plan for increasing market share through aggressive acquisitions. Valid's 1987 Telesis acquisition gave them an entry into the PCB market which industry forecasts are expecting to grow at a rate of 18% world-wide over 1989. Valid still faces an uphill battle competing with companies that have greater resources, both in terms of financial strengths and field presence.

Figure 1 compares the total revenues of the combined markets of Technical Workstation Platforms of CAE, PCB, and IC. The figures reflect Valid's position prior to the Calma, IMS, and ADT acquisitions. As of 1988, Valid was barely leading HP with a 6.0% share as compared to HP's 5.3% market share. Valid has a greater lead over HP in the CAE market with a 10.3% share compared to HP's 4.3% share (**figure 2**). In the IC market HP and Valid are equal with 1.9% shares of the market, (**figure 3**), but Valid's recent acquisition of IMS should increase their share in this market. In the PCB market, even with the 1987 acquisition of Telesis, Valid only has a 2.4% share of the market compared to HP's 8.6% share (**figure 4**).

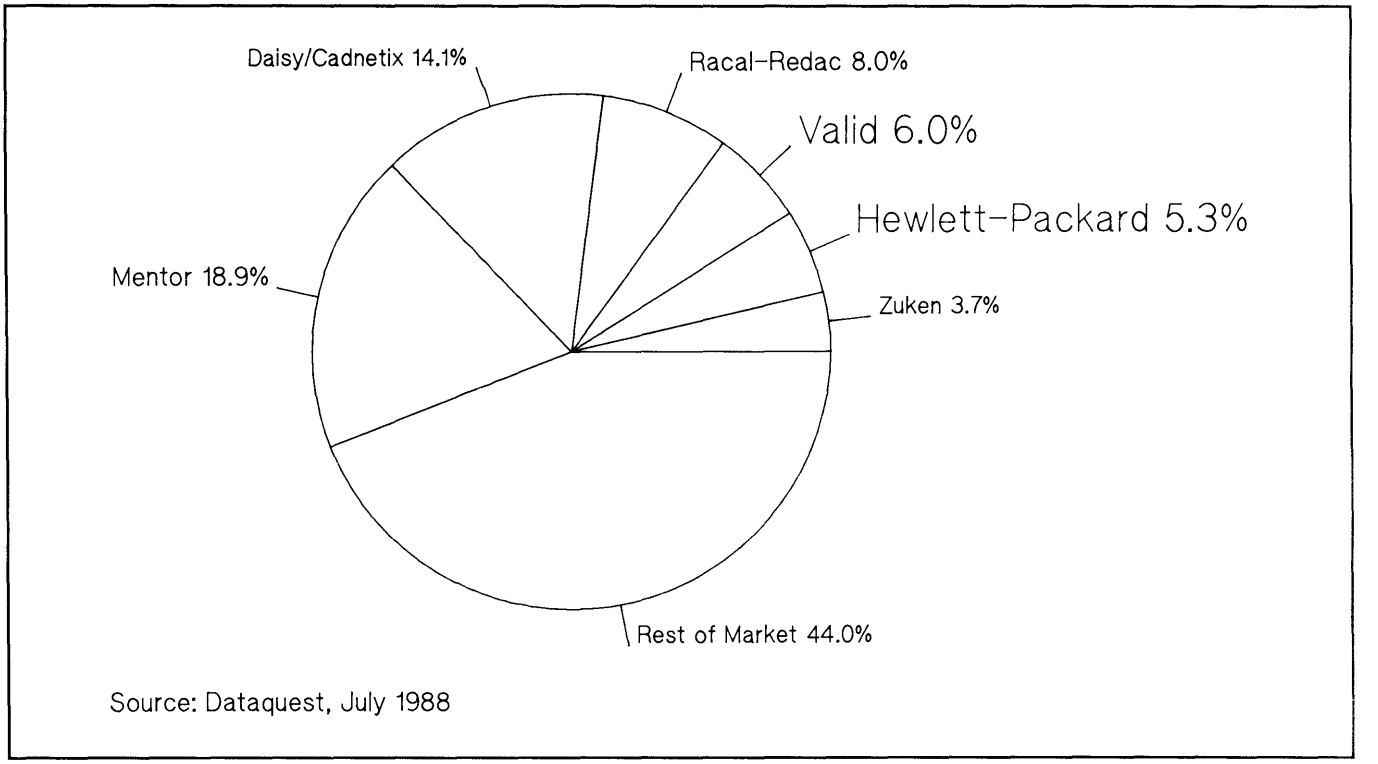

Figure 1: Market Share 1988, Total CAE, PCB, IC Markets

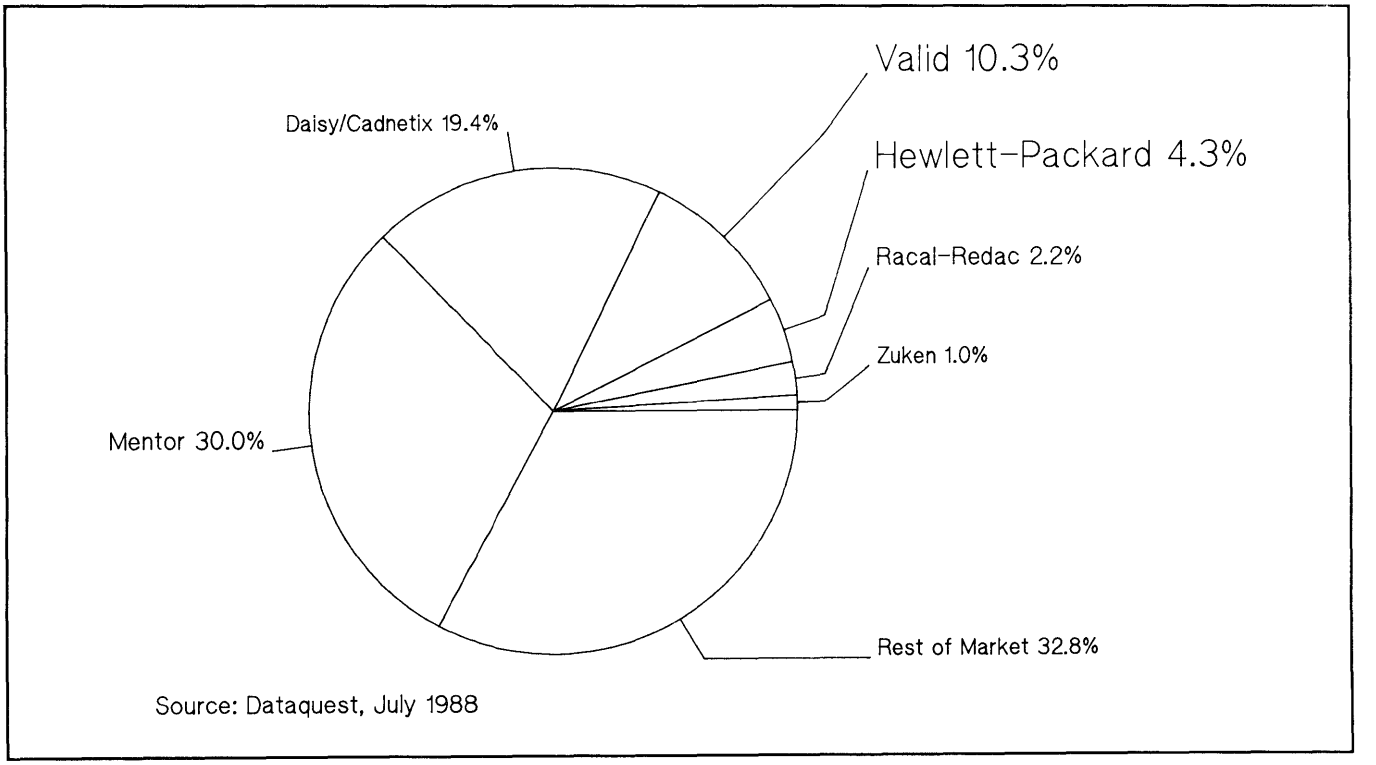

Figure 2: Market Share 1988, CAE Market

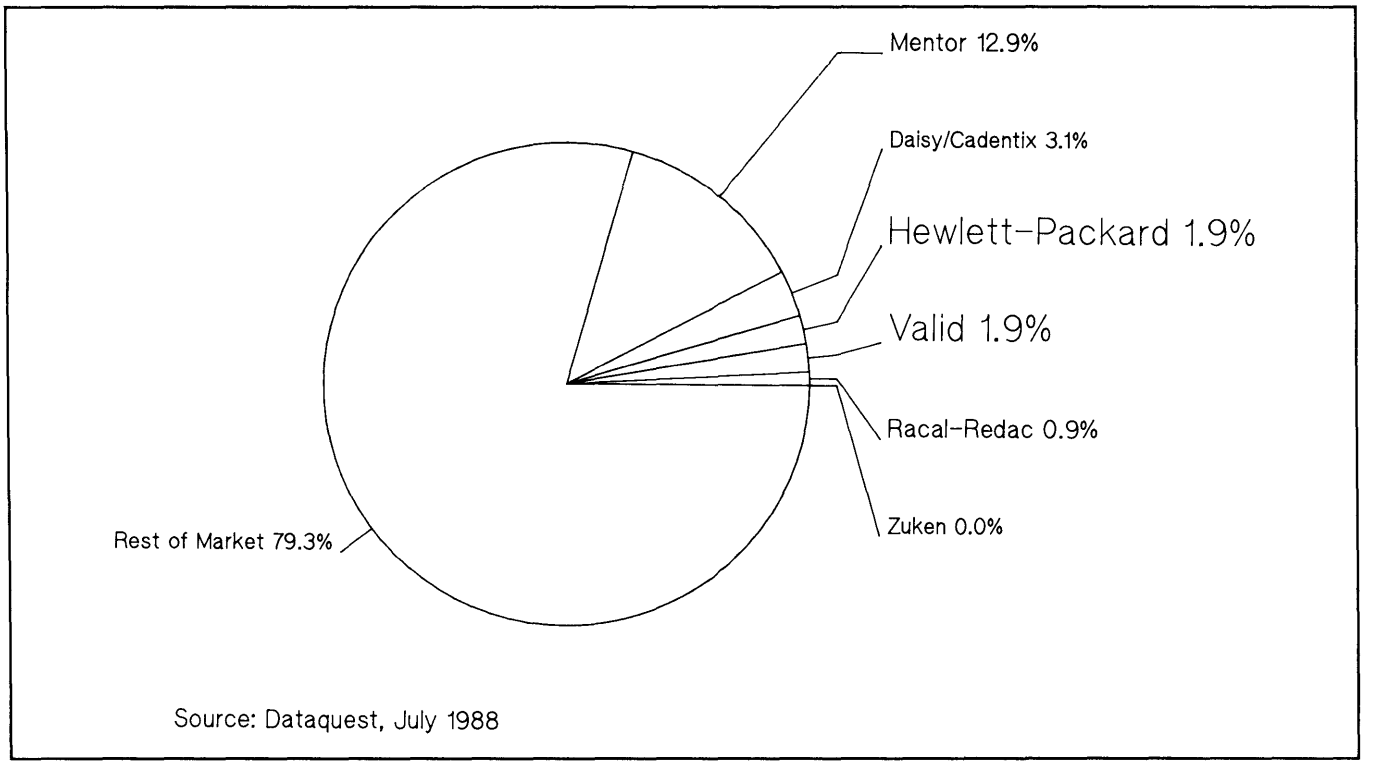

Figure 3: Market Share 1988, IC Market

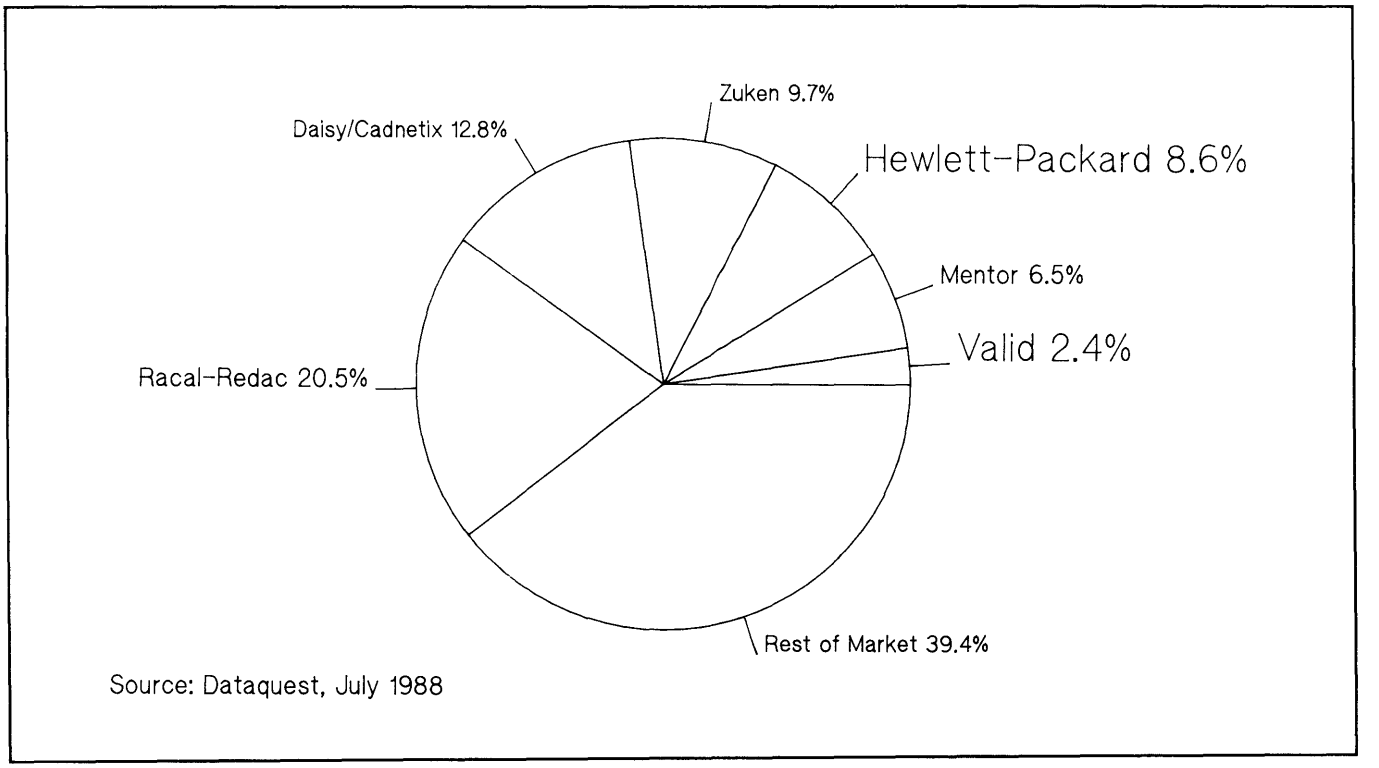

Figure 4: Market Share 1988, PCB Market

Product Family

Platforms

Valid introduced its products on DEC's VAXstation II under the VMS operating system in October 1986 and on the Sun 3 under the UNIX operating system in June 1987. In early 1987, Valid stopped manufacturing its proprietary SCALD series of computer systems. In July 1988, Valid committed to porting its CAE tools onto the Compaq 386 for Compaq's own use. It is expected that a Compaq 386 port will be made generally available in the future. Valid's core CAE tools are also available on the IBM PC/AT and compatible systems via a UNIX co-processor.

DEC Platforms running under the VMS operating system:

- VAXstation II
- VAXstation 2000
- VAXstation 3000
- VAX-11*
- VAX 8000 series*

*Valid offers analysis tools on these models only.

Sun Platforms running under UNIX operating system:

- Sun-3 family of workstation and servers
- Sun-4 family, based on SPARC architecture

- IBM PC/AT and compatibles — Valid's core CAE tools

Software:

Valid's products can be divided into four main categories: CAE, PCB CAD, IC CAD, and application-specific hardware. Valid's software is designed to support the C and Pascal languages, and the Ethernet local area networking system. For a comparison of Valid's and HP's products, see Appendix A.

CAE:

- **ValidGED** — design capture (Sun/VAX/IBM PC AT)
- **ValidSIM** — logic and timing simulator (Sun/VAX)
- **ValidTIME** — timing verifier (Sun/VAX)
- **ValidPACKAGER** — logical to physical design packager and design rule checker (Sun/VAX/IBM PC AT)
- **ValidFLAT** — automatic schematic generator (Sun/VAX)
- **ADvantage** — analog design (Sun/VAX)
- **TIMEMILL** — transistor level simulator and critical path analyzer (Sun/VAX)
- **RealChip** — hardware modeler (VAX)
- **RealFast** — hardware modeler and simulator accelerator (Sun/VAX)
- **RealModel** — hardware modeler and simulator accelerator (Sun/VAX)
- **R1Chip II** — second generation hardware modeler (Sun/VAX)

Software, cont'd

PCB CAD :

- **Allegro** — PCB layout
  (Sun/VAX)
- **Allegro-Review** — initiating board layout by floor planning, placing components, routing critical traces, and verifying circuit functionality before passing to PCB layout designer.
  (Sun/VAX)
- **Allegro-Prep** — generating component symbols, creating netlists and preparing mechanical documentation for PCB design.
  (Sun/VAX)
- **ThermoSTATS** — PCB thermal/noise/reliability analysis
  (Sun/VAX)
- **Multiwire** — I/face between PCB and multiwire router
  (Sun/VAX)
- **Insight** — high speed router
  (Sun/VAX)

IC CAD:

- **ValidLED** — IC layout editor for custom cell
  (Sun/VAX)
- **ValidDRC/EXTRACT** — hierarchical IC design rule checker and netlist extract
  (Sun/VAX)
- **ValidCOMPARE** — IC comparison for logic and layout
  (Sun/VAX)
- **Compose** — chip assembly tool for automatic/interactive placement routing and compaction
  (Sun)
- **GDS II** — IC graphics editor
  (Data General)
- **EDS II** — 3rd generation IC graphics editor
  (Sun)
- **FMS** — fast mask design
  (Sun)

Service and Support

Valid markets its products world-wide, primarily through a direct sales force. The sales and marketing operation is divided up into four divisions; three sales and support divisions, namely North America, International (Europe) and the Far East, and a marketing division located at San Jose. Each division is headed up by a vice-president reporting directly to Douglas Hajjar.

Valid employs technically experienced sales personnel, systems engineers, and field engineers at its sales and customer support offices. Valid also employees application engineers at its headquarters for technical support. Valid's training staff consists of technically qualified instructors who conduct customer training at Valid's facilities and at customer locations.

Valid warrants each system from 90 days to one year after installation, with the one-year warranty relating primarily to systems installed in Europe and Japan. After the warranty period, Valid offers renewable maintenance contracts providing hardware maintenance and software updates. A majority of Valid's systems are covered by maintenance contracts after expiration of the warranty.

Valid Future Products and Markets

With Douglas Hajjar's appointment as CEO in 1987, Valid began an aggressive acquisition policy aimed at broadening Valid's product line into the full spectrum of EDA products. Since the Telesis merger in 1987, Valid's research and development spending has remained constant. Valid's research and development is now almost exclusively concerned with software; hardware development is minimal. The development platform is Sun, and an estimated 30% to 40% of research and development is spent porting Valid's products to other platforms.

With the acquisition of Calma's IC CAD business, Valid can address the needs of layout technicians and design engineers. The Calma product integration involves picking the best features from Valid's Compose and Calma's EDS II, and developing a tightly coupled, well integrated IC CAD tool that will be available in the third quarter of 1989.

Valid's IMS acquisition gives Valid the foothold in the ASIC design verification business it needs to compete head-on with Mentor Graphics, HP and other diversified CAE houses. The IMS Logic Master series of products provides Valid with the hardware verification tools needed to link ASIC design to test.

The acquisition of ADT allows Valid to develop advanced mixed-signal products for the future. Valid wants to offer engineers a full spectrum of design, validation, layout, manufacturing, and test set-up solutions for analog and mixed-signal designs. In addition to supporting the Analog Workbench, Valid will incorporate ADT's state-of-the-art analog products, including libraries, analysis tools and simulators, into Valid's comprehensive environment. Valid will also maintain all of ADT's third-party relationships and honor all of ADT's outstanding licensing and OEM agreements, including a software marketing deal between ADT and HP. This acquisition positions Mentor, Daisy, and Valid with their own captive analog suppliers, leaving the rest of the industry to joust over what is left.

Douglas Hajjar also confirms reports that Valid is considering acquiring a major ATE company, such as LTX Corporation or GenRad Corporation. This will be the final piece in Valid's expansion plan.

Valid announced in January 1989 its complete line of EDA tools will be available on the DECstation 3100 and VAXstation 3100. The DECstation 3100 is a RISC architecture running full UNIX and requires a complete port of Valid's software; based on previous port timescales its first availability will be mid 1989.

Valid Future Products and Markets, cont'd

Valid expects to integrate Allegro with its CAE software tools, in terms of both products sharing a common user interface, by mid 1989, and Valid is also preparing an ATE link to its Allegro PC-board design package, called the Design For Accessibility (DFA) Toolkit. The DFA package looks for vias on the board to use as test points, or inserts vias and test pads to use as test points. Again, the package will be ported to Sun-3s, Sun-4s and Digital VAXstations.

Valid Sales Pitches

Currently, 75% of Valid's business is achieved from its installed customer base. A fundamental sales strategy is to leverage sales with their expanded product line from customers of each of the merged companies. They are seeking to sell PCB CAD to their CAE base, IC CAD to their Calma base, and open up design-to-test to all customers. Their success with this strategy very much hinges on whether they can achieve a meaningful integration of their product streams in 1989.

In very few instances does Valid have complete control of its major accounts. Valid generally shares these accounts with other EDA vendors. Siemens is a typical example where Valid supplies IC CAD and CAE, but Racal-Redac supply the PCB CAD. Valid is therefore always under threat of losing its major accounts to the other resident EDA vendors, particularly while its product integration remains a weakness.

One particular creative sales strategy announced by Valid in 1988 was its "White Knight" campaign aimed at Tektronix CAE customers. This came about as a result of Mentor's acquisition of the Tektronix EDA business. Valid stepped in with a transition plan for Tektronix CAE customers. This was of particular interest to those customers with DEC equipment who did not wish to be coerced onto the Apollo platform by Mentor.

Currently Valid's major sales pitch is they are the leading supplier of EDA systems based on industry standards: Digital, Sun, and personal computer platforms; VMS and UNIX operating systems; and Ethernet, TCP/IP, DECnet and NFS networking. One disadvantage to this is the poor delivery dates by DEC and Sun.

Another sales pitch is Valid's statement that it intends to replace Mentor as number one within the next two years. Valid's method for expansion and gaining market share is through an aggressive acquisition policy that will provide it with a greater depth in its product line.

With the proliferation of acquisitions, industry analysts are concerned whether Valid can maintain the Telesis, Calma, IMS, and ADT customer bases as well as its own. This will be particularly acute in the outlying branch offices' who will not have the skills to deal with these customers. The problem is compounded by the range of platforms including Data General (Calma), PDP11 (Telesis), and Valid's SCALD systems. There are also some customers still using such diverse platforms as IBM mainframes and DEC minis. CEO Douglas Hajjar admits acquiring so many companies so quickly is risky. So far, though, the Valid acquisitions seem to be going smoothly. Hajjar states the integration of the product lines will be relatively smooth since Valid is on multiple standard platforms and operating systems.

Technical Analysis

Introduction

This section contains technical comparisons of Valid and HP/EDD applications for standard logic design, design verification, documentation, and PCB layout. It is also a presentation of the strengths and weaknesses of both Valid and HP/EDD products.

Spider diagrams are used for comparing the technical applications. Each application is divided by product component or parameters. The parameters establish the axis of the spider diagrams. In some cases, such as standard logic design entry design verification, and board layout, there are several subcategories or attributes for each axis.

For each axis a whole number between 1 and 10 is used by HP field and factory support engineers. The larger the number, the "better" the performance of the application for that measurement axis. A value of 10 indicates the best, or state of the art, for current products on the market. A value of 1 indicates no capability, while a 5 is considered average. Unknown information is left blank and not included in the calculations. The subcategories are averaged and rounded to the nearest integer for plotting on the axis.

Design capture and design verification were studied on a Sun 3/260 workstation with 8 MB Ram, a 19" color monitor, and 500 MBytes diskspace with 16 MBytes swap memory. The software used was Valid GED (Schematic editor) version 8.5 and ValidSIM, version 2.2.

PCB layout was studied at a PCB service bureau in the U.S. on a Valid Allegro system, (version 2.1). The system was running on a Sun 3/60 workstation with 24 meg internal memory, two discs piggybacked, 147 meg and 327. Swap memory was approximately 120-130 meg..

Standard Logic Design Entry

Figure 5 is a spider diagram comparing the standard logic design entry systems of Valid and HP. The parameters and their attributes chosen are:

- **User Interface**
  - —flexible command entry
  - —operating system access
  - —windowing
  - —customizability
  - —commonality
- **Libraries**
  - —coverage
  - —completeness
  - —creation
  - —standards
- **Editor**
  - —graphics performance
  - —speed of design entry
  - —part selection
  - —design rule checking
  - —flat design
  - —hierarchical design
- **Capacity**
  - —IC design
  - —PCB design
- **Data Access**
  - —industry standard database
  - —access language
  - —design file access
- **Technology**
  - —PCB
  - —IC
- **Links**
  - —EDIF
  - —IGES
  - —test
  - —simulation
  - —layout
  - —documentation
- **General**
  - —learning tools
  - —revision control
  - —quality
  - —engineering changes

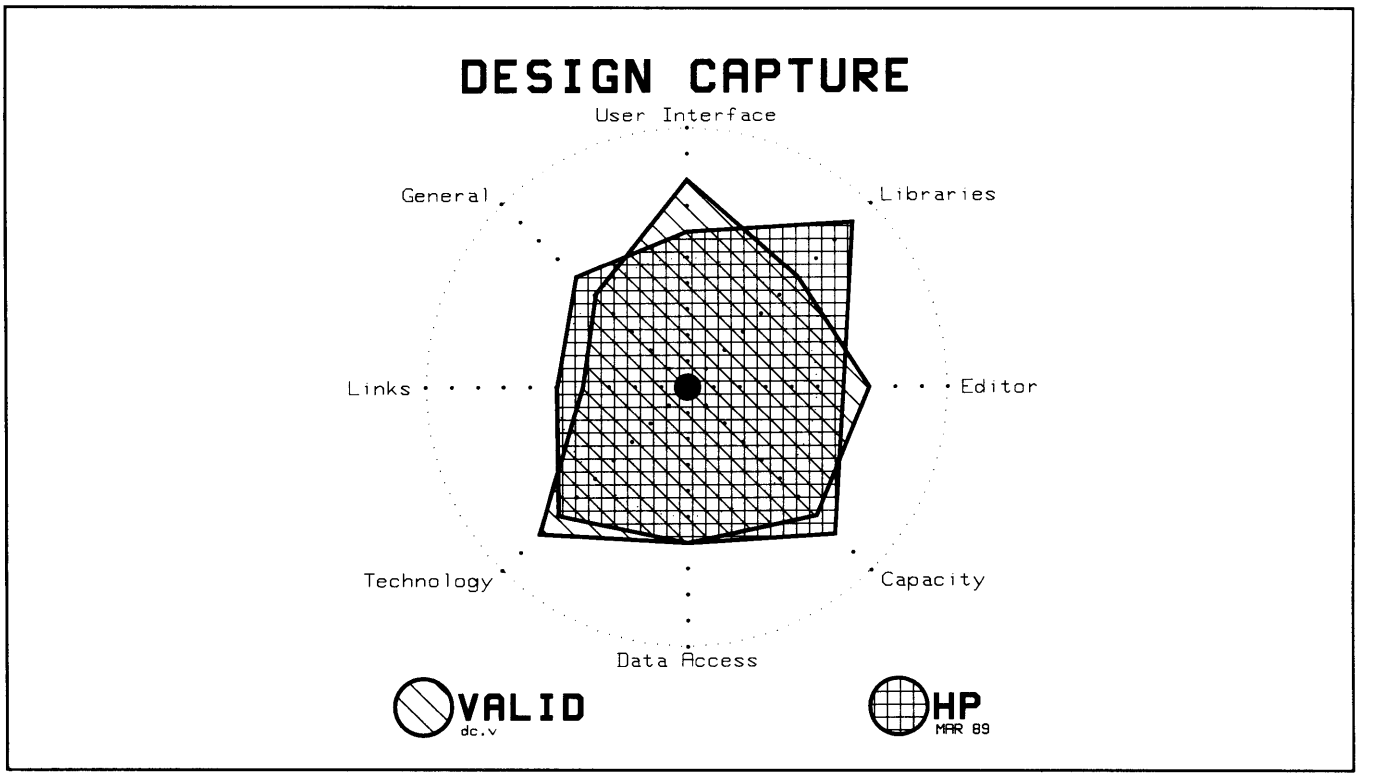

Figure 5: Standard Logic Design Entry

Valid Design Capture Strengths

- **Graphical Performance** — Valid's system response for basic graphical functions (drawing schematics) is superior to HP DCS on equivalent hardware.
- **Platform Environment** — Valid's CAE tools run under Suntools which provide good access to the operating system. This also allows the user to take advantage of multiprocessing for schematic entry and simulation. Users can have multiple schematic entry processes running simultaneously.
- **Database Access** — Valid supports a complete database access tool called DIAL. Dial is a procedural interface tool which uses the high level control constructs in Pascal to provide users with a powerful medium for database access.
- **Hierarchical Design** — Valid's Design Capture system provides hierarchical design without having to enter each element individually. For example, if it is desired to buffer each signal in a 16 bit bus, the designer merely connects the bus to a single buffer and then sets the SIZE parameter to 16. To create a flattened schematic, Valid offers ValidFlat which automatically breaks out all hierarchy in a design to create the leaf level schematics.
- **Schematic/PCB Integration** — Valid supports the specification of maximum trace length, trace width, and preferred placement in the schematic editor.

HP EDS Design Capture Strengths

- **DCS Database** — HP EDS does not require users to compile their designs for simulation and layout. While Valid users must perform separate compilations for timing verification, simulation, and PC layout. The HP EDS simulator also uses the last compiled design for analysis. While Valid users must make sure that the design they wish to simulate was the last design compiled for simulation.
- **Scions** — HP DCS uses Scions to take advantage of functionally similar parts. This reduces the time and work for each component even if they only differ in electrical characteristics but are functionally identical.
- **On-Line Rule Checking** — On-line rule checking minimizes the time spent debugging the design before it can be expanded for layout (assigning references) or simulation (opening the simulation page). Valid supports only a rudimentary check of a schematic by identifying name inconsistencies for a single sheet. HP DCS is also superior to Valid in its ability to check symbol pin/connector mapping automatically.
- **DDL** — HP DDL provides more complete access to the database than Valid. For example, Valid cannot back annotate to hierarchical schematics.

Design Verification

Figure 6 is a diagram of Valid's and HP's process for transferring information from capture to simulation and layout. HP benefits from an object-oriented database structure which eliminates the need to do separate compilations on the design. Valid depends upon a large number of files and three separate compilation steps that are required to verify timing, simulate, and transfer the design information to the Allegro layout package. Design errors are eliminated early in HP's design cycle because of HP's on-line design rule checking whereas in Valid's design cycle they are not uncovered until the compilation step.

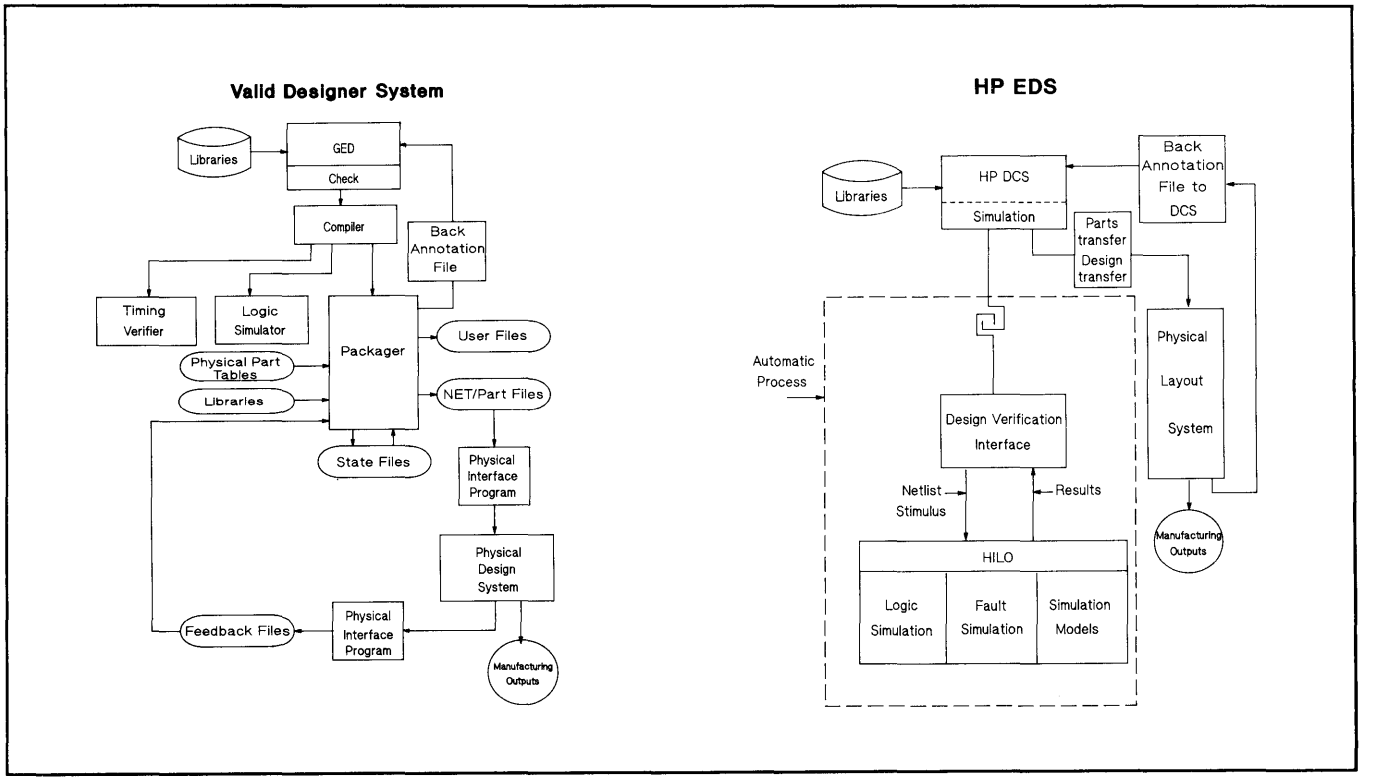

Figure 6: Valid Design Verification System vs HP EDS Design Verification

Figure 7 is a spider diagram comparing Valid and HP design verification systems. The parameters and attributes chosen for this comparison are:

- **Simulator Performance**
  - —state initialization
  - —acceleration support
  - —simulator speed
  - —simulator capacity
  - —mixed mode capability
- **Timing Analysis**
  - —back annotation of timing info
  - —physical modeling support
  - —diagnostics
  - —static and dynamic analysis
- **Links**
  - —software interfaces
  - —netlist generation
  - —to analog/mixed mode
  - —to ASIC/PLD tools
  - —to test
- **Model Language**
  - —ease of creating models
  - —debug capabilities
  - —physical shell creation
  - —HDL's supported
- **Stimulus Creation**
  - —graphical
  - —algorithmic
  - —tester compatibility
- **Results Analysis**
  - —interactive waveform
  - —what-if analysis
  - —simulator interactivity
  - —results analysis tools
  - —circuit debug capabilities
- **Usability**
  - —design cycle complexity
  - —simulator interactivity
  - —remote/distributed simulate
  - —ease of use
  - —run-time status reports
- **Libraries**
  - —coverage
  - —physical modeling supported
  - —ASIC/PLD coverage
  - —standards supported
- **Fault Analysis**
  - —testability assessment
  - —physical modeling support
  - —simulator speed
  - —fault lists and types
  - —selective fault analysis

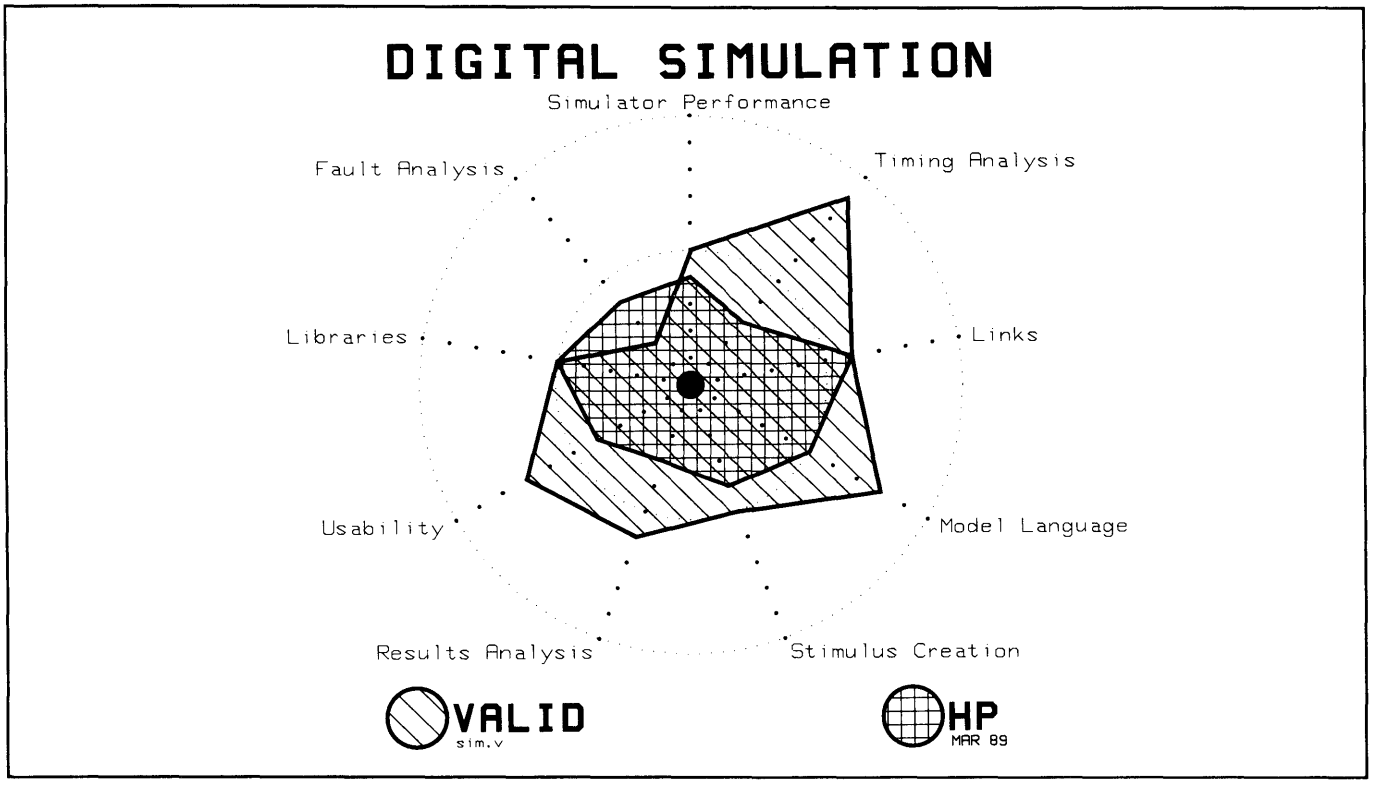

Figure 7: Design Verification, Valid vs HP EDS

Valid Design Verification Strengths

- **Timing Analysis** — Valid provides a "good" tool for static timing analysis called ValidTIME. This tool does not require an input stimulus.
- **Schematic/Simulator Integration** — Valid users can view the schematic while running the simulator, and can pick nodes in the design, and automatically insert corresponding traces in the simulator window.
- **Stimulus/Tester Compatibility** — The stimulus used in the simulator can easily be converted into a compatible form for Teradyne, HP, GenRad, Zehnetel, and TSSI tester equipment.

HP EDD Design Verification Strengths

- **Dual Delay Analysis*** — Logic simulation can be run in single or dual delay mode. Dual delay timing analysis can verify whether the circuit still performs within regions of uncertainty and whether the circuit has the necessary timing margin to operate over the range of devices that may be used when manufacturing the actual product.
- **Hazard Monitoring/Path Trace-Back***
- **High-Level Waveform Language**
- **Waveform Comparisons** — The input stimulus on the Simulation page can be specified in both waveform and textual format.
- **Links to Prototyping Test** — HP EDD Vulcan link has no equivalent in Valid's Design Verification System.

*** System Hilo Release**

Documentation

In July 1988, Valid announced a cooperative marketing agreement with Interleaf for interfacing Interleaf's Workstation Publishing Software and Technical Publishing Software to the ValidGED graphics editor. This will provide engineers with a documentation capability.

Valid Interleaf Strengths

- **Sophisticated composition functions**
- **Optical scanner capabilities for image input**
- **Interface to CAD systems**
- **Output to Monotype Lasercomps or other typesetters**

HP offers FrameMaker, a professional document publishing software designed for the engineer, scientist or technical professional.

HP FrameMaker Strengths

- **Complete word processor** — full-featured text processor including mathematical equation composition and scientific notations
- **User Interface** — WYSIWYG
- **Graphics program** — allows importing, formatting, and creating graphics
- **Hypertext capabilities**
- **Interactive page and document layout**
- **HP FrameViewer** — provides view-only access to FrameMaker documents
- **International FrameMaker** — provides localization in 5 languages

PCB CAD (Board Layout)

Figure 8 is a spider diagram comparing Valid and HP board layout systems. The parameters and attributes chosen for this comparison are:

- **Manufacturing Outputs**
  - —panelization
  - —photoplotters
  - —drill
  - —pick and place
  - —assembly drawings
  - —reports
- **Library**
  - —creation
  - —maintenance
  - —vendor supplied quantity
- **Editing**
  - —interactive placement
  - —interactive routing
  - —design rule checking
  - —logic information access
- **Place & Route**
  - —automatic placer
  - —automatic router
- **Technology**
  - —surface mount
  - —through hole
  - —hybrid thick film
  - —hybrid thin film
  - —multi layer
  - —metal core
  - —ECL
- **Links**
  - —front end
  - —mechanical engineering
  - —documentation
  - —thermal
  - —test
  - —EDIF
  - —IGES
  - —open system
- **General**
  - —user interface
  - —customizability
  - —quality
  - —reliability
  - —engineering changes

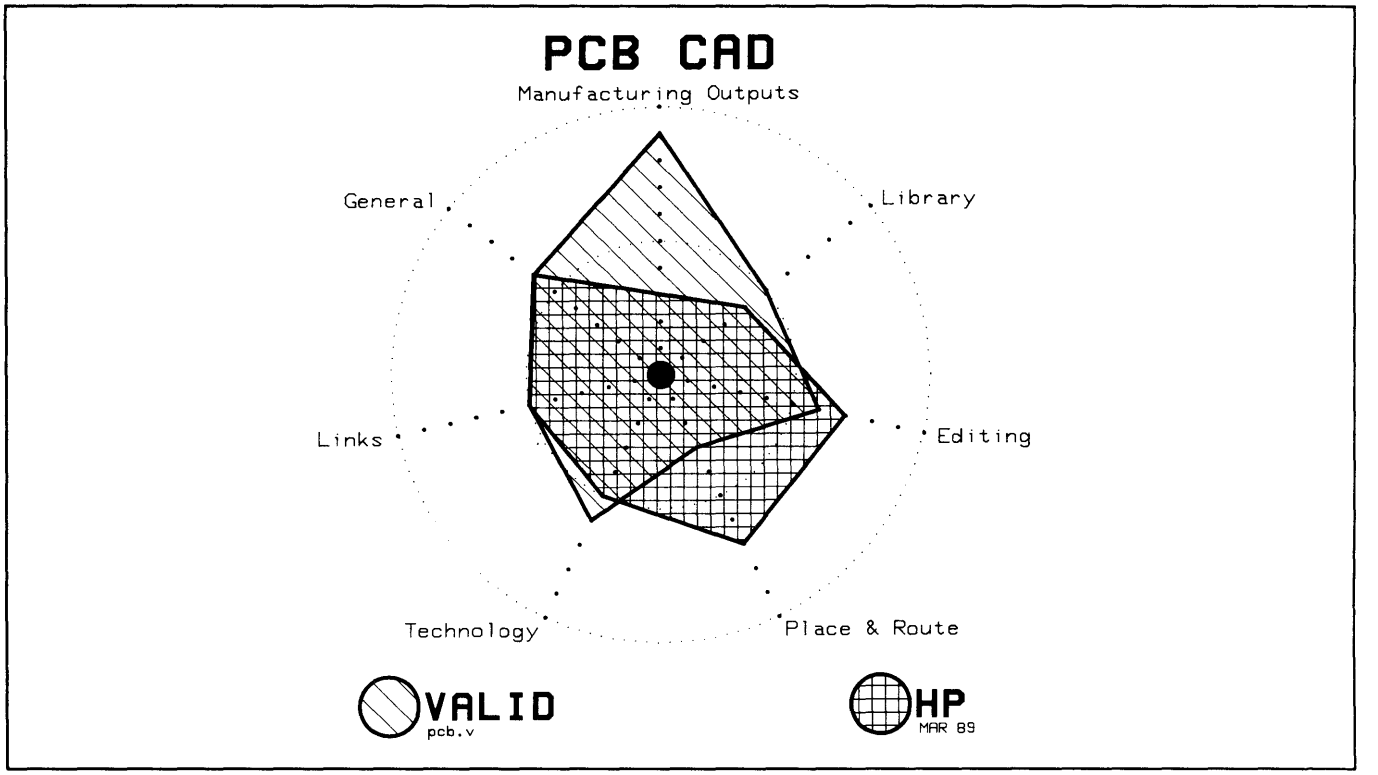

Figure 8: PCB CAD (Board Layout), Valid Allegro vs HP PCDS

Valid Allegro Strengths

- **One Vendor Contact** — Valid is a hardware OEM for Sun with its own contract maintainence. A Valid user need only contact Valid for any problem they may encounter, hardware and software. Valid has been known to push for the more expensive solution to hardware problems, causing some of their customers to contact Sun directly.
- **Windowing Capabilities** — Allegro operates under SunWindows (similar to HP Windows), and has a nice looking user interface. Valid uses both pop-up menus and static cascading menus to enter commands. Macros are supported by Allegro.
- **Interactive Routing** — The multiple menus make interactive routing very easy to learn and to use, but as one gains experience the multiple menus become a greater obstacle to increases in productivity.
- **Front to Back End Integration** — Superior to HP PCDS because it provides the capability to do preferred placement and to specify maximum trace length.

HP PCDS Strengths

- **Performance** — HP PCDS graphics performance and acceleration is superior to Allegro, though Valid is working on supporting a graphical accelerator which should make the system faster graphically and add additional color.
- **Placement** — HP PCDS placement tools are superior both in scope and execution when compared to Valid's Allegro placement tools which are still in their infancy.
- **Resolution** — HP PCDS has finer resolution capabilities than Allegro which has a resolution of 1 mil.
- **Color Adjustment** — HP PCDS uses a hue, saturation, and intensity approach for adjusting color. Allegro incorporates an RGB schema for adjusting color which human factors research has shown to be difficult to grasp.

Valid Buzz-Word List

ADvantage
Analog design environment includes tools for the design and analysis of analog circuitry in the time, frequency, noise, and direct current (DC) domains.

Allegro
A rules-driven system for PCB layout that addresses the needs of high-speed and double-sided board surface mount technologies.

Allegro-Review
New Allegro module aimed at engineers initiating board layout by floor planning, placing components, routing critical traces, and verifying circuit functionality before passing to PCB layout designer.

Allegro-Prep
New Allegro module used for generating component symbols, creating netlists and preparing mechanical documentation for PCB design.

Compose
Chip assembly tool for automatic/ interactive placement routing and compaction

EDS III
A Calma product that supersedes GDS II.

FMS
Fast mask design

GDS II
A Calma product acquired by Valid. Used for the design of cell layouts.

Insight
High speed router

Multiwire
I/face between PCB and multiwire router

RealChip Hardware Modelling System
Application-specific hardware product using actual ICs as functional models of themselves when simulating board designs containing complex very large integrated (VLSI) devices. RealChip can be used to simulate off-the-shelf components such as microprocessors and their peripheral chips, or application-specific integrated circuit (ASIC) devices.

RealFast Simulation Accelerator
Addresses two simulation problems inherent in complex system designs -- speed and capacity. RealFast provides interactive simulations at a rate of up to 500,000 events per second for designs containing up to a million primitives.

RealModel System Simulator
A tightly coupled hardware modeler and simulation accelerator.

R1Chip II
Second generation hardware modeler

ThermoSTATS
Analyzes board designs for component temperature and calculates a board's reliability and susceptibility to noise interference.

TIMEMILL
Provides timing simulation of ICs at the functional, logic or transistor levels from the design's layout. Designer can simulate entire chips to perform timing, critical path and functional analysis.

ValidCOMPARE
Performs logic-to-layout comparisons to verify that circuits in the layout are implemented as defined in the schematic, and to check that the layout is design rule and electrically correct.

Valid Buzz-Words, cont'd

ValidDRC/EXTRACT

A tool allowing designers to verify IC layout. ValidDRC determines whether design rules have been observed and whether the chip layout is correct. ValidEXTRACT can extract circuits for circuit-level simulation.

ValidFLAT

Hierarchical Schematic Flattener converts hierar chical schematics into flat schematics for use in manufacturing and design documentation.

ValidGED Graphics Editor

A easy to use, menu-driven tool used to accelerate design capture.

ValidLED

A manual editor specifically tailored to create fully custom IC layouts, cells and blocks.

ValidPACKAGER

A physical design and analysis tool that converts logic desins into a net list suitable for use with other tools. It automatically assigns reference designators and identification numbers, performs design rule checking and prepares data for back annotation with the schematic.

ValidSIM

Interactive Logic Simulator is a functional simulation and analysis tool for design verification.

ValidTIME

Analyzes designs for digital circuit timing characteristics, such as set up and hold times and pulse widths. It also generates a list of timing violations, as well as a timing diagram of all the signals in the circuitry.

Appendix A: Product Coverage Comparison

	Conventional PCB		PLD	
Design Step	Valid	HP	Valid	HP
Architecture Design				
Structured Des.				
HW/SW Partition				
Implm. Indep.				PLDDS
Library Parts				
Sch. Parts Creat	ValidGED, Valid Extract	DCS/PCDS	Valid PLD	
PCB Parts Creat	Allegro	DCS/PCDS		
Hardware Models	RealModel	yes		
Mil Std Parts		no		
Design Capture	ValidGED	DCS		
Behavioral	UCP	HILO HDL		
Wave/STD/Boa				PLDDS
Schematic Capt	ValidGED	DCS	ValidGED	PLDDS/DCS
Digital Simulation	Valid SIM	HILO-3/ System HILO	Valid SIM	HILO-3/ System HILO
Logic Sim.	Valid SIM	System-HILO	Valid SIM	System-HILO
HW Sim.	Realchip	HiChip	Realchip	HiChip
Fault Analysis	Rapid Test	HILO FAULT	RapidTest	HILOFAULT
Timing Analysis	ValidTime	System-HILO	ValidSIM	System-HILO
	TIMEMILL (EPIC)	HiTime	TIMEMILL (EPIC)	HiTime
Analog Simulation	ValidSPICE/AWB	AWB/Saber		
SW Analog				
Mixed Mode		no		
Stress/reliabil	AWB	AWB/Saber		
RF/microwave		MDS		
Physical Layout	Allegro	PCDS		
Edit	Allegro	PCDS		
Forced Router	yes	yes		
Rip-Up Router	yes	yes		
Random Route	no	no		
Other Router	no	no		
DRC	on-line	on-line		
Manuf. Outputs	Allegro	Mfg links		
Prototype Testing				
Waveform Cap/Com		HP16500A		HP16500A
Digital HW Test		HP16500A		HP16500A
Analog Waveform				
Analog HW Test				
System Integr Test				

Appendix A: Product Coverage Comparison, cont'd

	Conventional PCB		PLD	
Design Step	Valid	HP	Valid	HP
Design Compilation Schematic PCB Schematic SIM	 Compile/ ValidPACKAGE Compile	(None Necessary)		
Simulation Acceleration	RealFast	No	RealFast	No
Mfg. Test Prep. Fault Analysis Test Generation Tester Links	 Rapid Test Teradyne, HP, GenRad, Zehntet, TSSI	 3065/TSSI		
Mechanical Design 2D 3D Thermal Analysis	 included	 ME-30 ME-30		
Documentation Text & Graph Integrated Tech. Pub.		 FRAME FRAME FRAME		
SW Firmware		HP64000		
Engineering Parts				
Project Mgmt.				
Design Mgmt.	SCCS	DSM		
File Management	SCCS	DDC		
Misc Database Access	 DIAL	 DDL		
Silicon Compilers				
System Level Sim				
MSPICE PLUS				

Appendix A: Product Coverage Comparison, con'td

	Standard Cell ASIC		Gate Array ASIC	
Design Step	Valid	HP	Valid	HP
Architecture Design Structured Des. HW/SW Partition Implm. Indep.				
Library Parts Sch. Parts Creat PCB Parts Creat Harware Models Mil Std Parts	Vendor Kits	DCS	Vendor Kits	DCS
Design Capture Behavioral Wave/STD/Boa Schematic Capt		DCS		DCS
Digital Simulation Logic Sim. HW Sim. Fault Analysis Timing Analysis	ValidSIM ValidSIM RealChip RapidTest ValidTIME TIMEMILL (EAC)	HILO-3/ System HILO System-HILO HiChip HILO FAULT System HILO/ HiTime	ValidSIM ValidSIM RealChip RapidTest ValidTIME TIMEMILL (EAC)	HILO-3/ System HILO System-HILO HiChip HILO FAULT System HILO/ HiTime
Analog Simulation SW Analog Mixed Mode Stress/reliabil RF/microwave				
Physical Layout Edit Forced Router Rip-Up Router Random Router Other Router DRC Manuf. Outputs				
Prototype Testing Waveform Cap/Com Digital HW Test Analog HW Test		HP16500A HP16500A		HP16500A HP16500A
System Integr Test				

Appendix A: Product Coverage Comparison, con'td

	Standard Cell ASIC		Gate Array ASIC	
Design Step	Valid	HP	Valid	HP
Mfg. Test Prep. Fault Analysis Test Generation Tester Links		DICE		DICE
Mechanical Design 2D 3D Thermal Analysis				
Documentation Text & Graph Integrated Tech. Pub.				
SW/Firmware				
Engineering Parts				
Project Mgmt.				
Design Mgmt.				
File Management				
Misc				
Silicon Compilers	Concorde		Concorde	
System Level Sim				

Appendix B: Valid List Prices

ValidGED	Design capture	$8,800
ValidSIM	Logic & timing simulator	12.500
ValidTIME	Timing verifier	6,250
ValidPACKAGER	Logical to physical design packager and rule checker	4,500
ValidFLAT	Automatic schematic generator	10,000
ADvantage	Analog design	33,000
Allegro	PCB layout	50,000
ThermoSTATS	PCB thermal/noise/ reliability analysis	15,000
Multiwire	I/face between PCB and multiwire router	10,000
Insight	High speed router	30,000
ValidLED	IC layout editor for custom cell	20,000
ValidDRC/EXTRACT	Hierarchical IC design rule checker and netlist extract	20,000
ValidCOMPARE	IC comparison for logic & layout	10,000
Compose	Chip assembly tool for automatic interactive placement routing and compaction	39,900
TIMEMILL	Transistor level simulator & critical path analyzer	20,000
GDS II	IC graphics editor	85,000*
EDS III	3rd generation IC graphics editor	25,000
FMS	Fast mask design	15K-22K
RealChip	Hardware modeler	30,000
RealFast	Hardware simulator	40,000
RealModel	Hardware modeler & simulator accelerator	84,500
R1Chip II	2nd generation hardware modeler	65,000


HEWLETT
PACKARD