

**OPERATING AND SERVICE MANUAL**

**PART 4**

**7970B/7970C**

**DIGITAL MAGNETIC TAPE UNIT**

**WRITE MODULES**

Printed-Circuit Assemblies:

07970-60230, Series 1015  
07970-60240, Series 1134  
07970-60300, Series 1218  
07970-60800, Series 1025  
07970-60810, Series 1025  
07970-60820, Series 1025  
07970-60880, Series 1025

## SECTION I

### DESCRIPTION

#### 1-1. INTRODUCTION.

1-2. This section describes the write modules of the 7970B/7970C Digital Magnetic Tape Units. A functional description and circuit description is also included to aid in servicing the write modules.

#### 1-3. PHYSICAL DESCRIPTION.

1-4. The write modules consist of a write enable assembly, a write interconnect PC assembly, and a write magnetic head assembly. The write enable assembly senses the presence of a write enable ring on the supply reel and provides write current for the write data circuits. The control switch assembly of write equipped units contains an indicator that displays the write enabled condition.

1-5. The magnetic head assembly is a seven or nine track, read while write, NRZI head with an erase head. Channel scrambling is accomplished in the head assembly wiring. From the reference edge of the tape (edge nearest the operator) the nine-track channel designations are 5, 7, 3, P, 2, 1, 0, 6, and 4. The seven-track channel designations are 7, 6, 5, 4, 3, 2, and P.

1-6. The write assembly is a card cage assembly (motherboard) that contains a write control PC assembly, a single-channel write data PC assembly and three or four dual channel PC assemblies. Seven-track units will have three dual-channel write data PC assemblies and nine-track units will have four dual-channel PC assemblies. Seven-track units do not use channels 0 and 1. The channels are numbered left-to-right starting with P.

1-7. The write interconnect PC assembly contains load resistors for all write drivers and interconnects the head assembly with the write assembly. The write interconnect PC assembly is located near the head assembly.

#### 1-8. FUNCTIONAL DESCRIPTION.

1-9. Information to be written is generated by the on-line interface and processed by the tape unit write data circuits. The information to be written is recorded in NRZI (non-return-to-zero-ones inverted) form. A "one" data bit is represented by a tape flux reversal and a "zero" data bit is represented by the absence of a flux reversal.

1-10. When the tape unit is loaded with a reel of tape equipped with a write enable ring, the write enable assembly provides +12 volts (+12 WE) to the write data circuits. The +12 WE provides write current for the write head drivers and the erase head driver. Tape unit motion status signals and

interface commands are processed by the write control circuits to control the write data circuits. The write control circuits also provide a Write Latch status signal which is used to switch the read threshold level.

1-11. When unit write condition is first established, the write control circuits ensure that the write head drivers are in a reset state (inter-record gap flux) and tape is saturated in the same polarity as the erase head. A write "one" data bit from the interface is processed by the write control circuits and the write head drivers change state to generate a flux reversal.

1-12. Each successive "one" data bit causes the write head drivers to alternately conduct. After all characters of a data block have been written,  $\overline{WRS}$  from the interface causes an additional flux reversal to be generated if an odd number of bits was written in the channel. All write head drivers are therefore left in a reset state. The LRC character is written on the tape as a result of returning all of the seven or nine write head drivers to the reset state.

#### 1-13. CIRCUIT DESCRIPTION.

1-14. Data bits of the character byte including the CRCC character from the interface are on individual lines to seven or nine individual write data channels. The interface generated Write Clock ( $\overline{WC}$ ) and Write Reset ( $\overline{WRS}$ ) are routed to the write control circuits. The following paragraphs describe the operation of the write control circuits and a typical write data channel. Block diagrams and timing diagrams are included to aid in understanding the operation of the circuits.

#### 1-15. WRITE CONTROL CIRCUITS.

1-16. The write control circuits are on the write control PC assembly located in the write assembly (motherboard). Figure 1-1 is a block diagram of the write control circuits.

1-17. A tape reel equipped with a write enable ring will cause the write enable solenoid to energize. With the solenoid energized, +12 volts (+12 WE) is provided for the write circuits. The driver enable circuit detects the presence of both +5 volts and +12 WE and generates a write bias voltage for the write head drivers and the erase head driver.

1-18. Tape unit status signals are gated to provide a direct clear to the Write Latch flip-flop. If any of the following conditions change, the gate causes a direct clear of the Write Latch flip-flop.

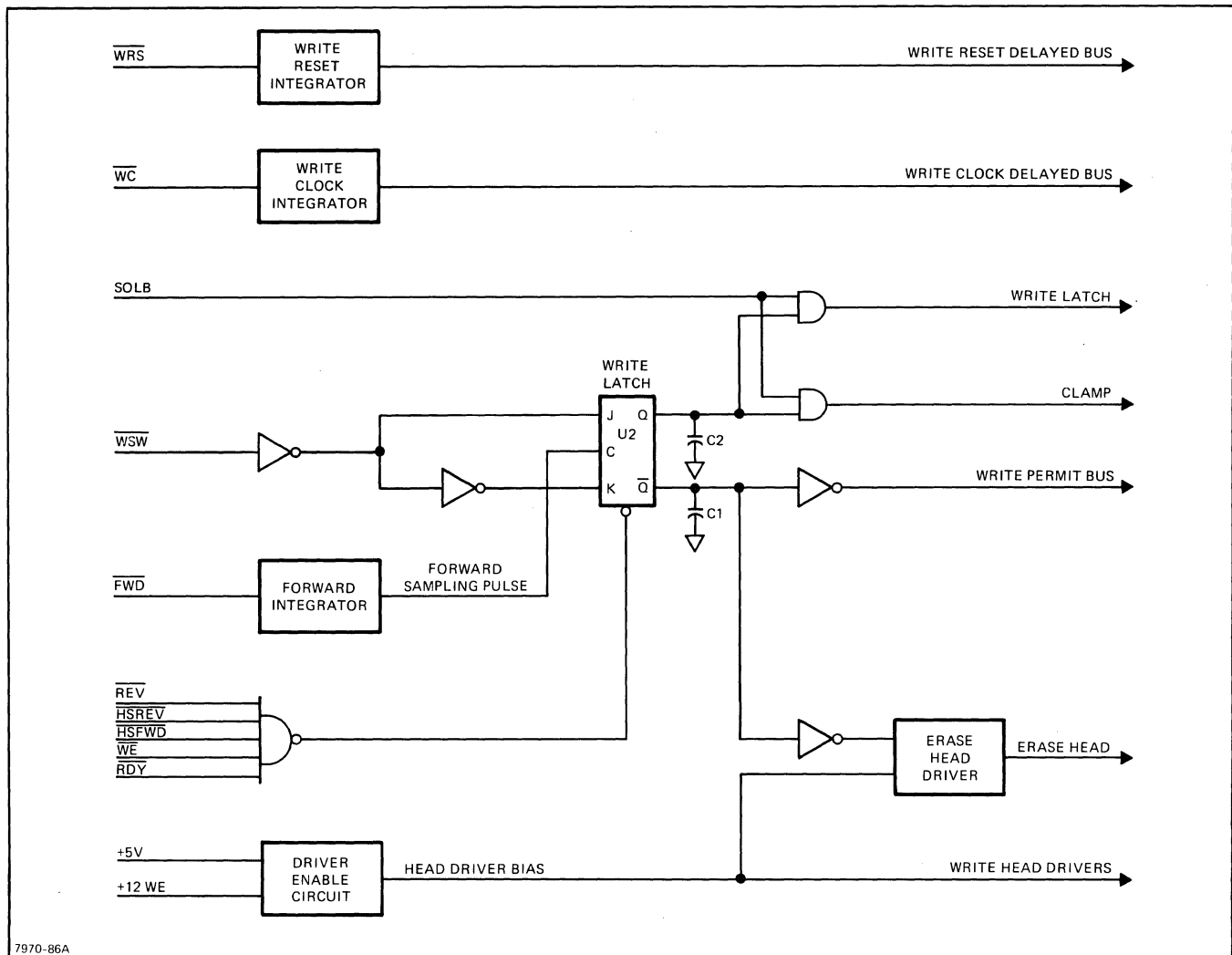


Figure 1-1. Write Control Circuits Block Diagram

- a. Tape unit must be ready ( $\overline{RDY}$ ).
- b. Supply reel must be equipped with a write enable ring ( $\overline{WE}$ ).
- c. Tape unit must not be in a reverse mode ( $\overline{REV}$ ).
- d. Tape unit must not be in a high-speed reverse mode ( $\overline{HSREV}$ ).
- e. Tape unit must not be in a high-speed forward mode ( $\overline{HSFWD}$ ).

1-19. The  $\overline{Forward}$  ( $\overline{FWD}$ ) status from the control and status circuits is integrated to provide a sampling pulse. The pulse is delayed approximately 10  $\mu$ s. The leading edge (negative-going) of the Forward ( $\overline{FWD}$ ) status opens gate U5A (open collector circuit) and capacitor C6 charges towards +12 volts. When the base voltage exceed +5.6 volts, transistor Q1 conducts and the collector of Q1 drops to +5.6 volts. The negative-going transition asserts U4C. The time between the leading edge of  $\overline{Forward}$  ( $\overline{FWD}$ ) status and the assertion of U4C is the 10  $\mu$ s delay. The pulse width

of the sampling pulse from U4C is determined by the time required for capacitor C5 to recharge toward +5V through R10. When the charge exceeds the threshold level of U4C, the gate changes state and the resulting pulse is applied as a clock input to the Write Latch (U2). Figure 1-2 is a timing diagram showing the generation of the sampling pulse.

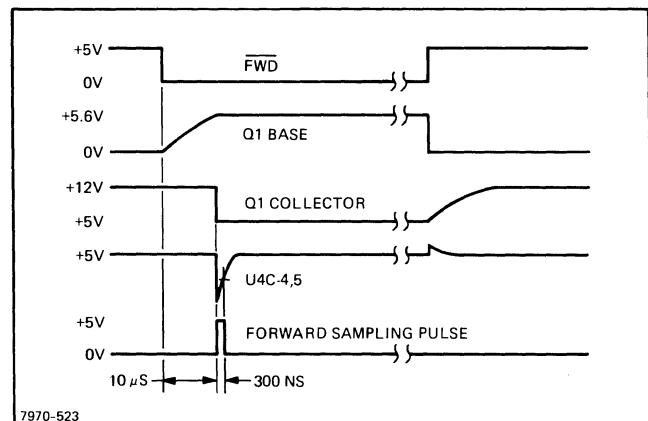


Figure 1-2. Forward Sampling Pulse Generation

1-20. The Set Write ( $\overline{WSW}$ ) command from the interface (through the control and status PC assembly) is inverted by line receiver U1C and applied to the J input of the Write Latch. The output of the U1C is again inverted and applied to the K input of the Write Latch. The delayed and integrated forward sampling pulse at the clock input therefore samples the Set Write ( $\overline{WSW}$ ) command. If Set Write ( $\overline{WSW}$ ) is true (low) when the Write Latch is clocked, the Write Latch is set.

1-21. When the Write Latch is set, capacitor C2 charges toward +5 volts. When the charge on C2 exceeds the threshold of U1A, delayed SOLB (selected and on-line) is gated with the delayed Write Latch Q output to provide clamp. The leading edge of clamp is delayed 100 nanosecond from the start of Write Latch set. The Q output is also gated with SOLB to provide the Write Latch status for the read circuits.

1-22. When the Write Latch is set, the  $\overline{Q}$  output goes Low and U3D is negated placing the write permit bus at approximately +5 volts. The leading (positive-going) edge of Write Permit is coincident with the negative going edge of the Write Latch  $\overline{Q}$  output. Capacitor C1 has no effect.

1-23. When the write latch changes state, the negative going transition of the  $\overline{Q}$  output is not affected by C2 and the trailing (negative-going) edge of clamp is coincident with the transition. The positive going transition of the  $\overline{Q}$  output however has to charge C1 and the trailing edge of Write Permit is therefore delayed approximately 100 nanoseconds. Figure 1-3 is a timing diagram showing the generation of write permit and clamp.

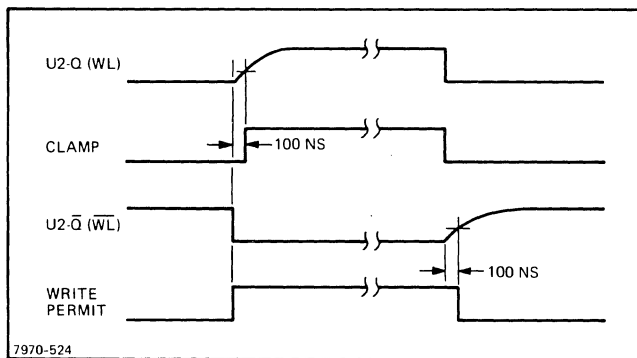


Figure 1-3. Write Permit and Clamp Timing Diagram

1-24. The Write Clock ( $\overline{WC}$ ) and Write Reset ( $\overline{WRS}$ ) commands from the interface are delayed and integrated in the same manner as Forward ( $\overline{FWD}$ ). The commands are delayed 1.1  $\mu$ s and the pulse width of the integrated pulses is approximately 200 nanoseconds.

#### 1-25. WRITE DATA CIRCUITS.

1-26. The write data circuits are on the single- and dual-channel write data PC assemblies located in the write assembly (motherboard). The single-channel assembly is adjacent to the write control PC assembly and is designated as the P (parity) channel. The dual-channel assemblies are designated as 0, 1, 2, 3, 4, 5, 6, and 7 for nine-track units and 2, 3, 4, 5, 6, and 7 for seven-track units. The dual-channel assembly (0 and 1) adjacent to the single-channel assembly is not used in seven-track units. Figure 1-4 is a block diagram of a typical write data channel.

1-27. Initially the Write Permit and Clamp buses are low. Therefore, the Write Toggle Q and  $\overline{Q}$  outputs are both false (high). Inverters U1D and U1E prevent the write drivers from conducting. The Write Permit bus leads the Clamp bus by approximately 100 nanoseconds, therefore when the Write Permit bus goes true (low), the Write Toggle is set. The Write Toggle Q output remains false (high) and the  $\overline{Q}$  output is true (low). The inverter is negated, and the set write driver conducts. This allows current to flow through one-half of the center tapped head. Tape is therefore saturated in the same polarity as the erase head.

1-28. A write "one" data bit from the interface is gated with the delayed Write Clock pulse and applied to the skew delay one-shot. The trailing edge of the one-shot output clocks the Write Toggle flip-flop. The Write Toggle flip-flop changes state, the Set Write Driver is turned off and the Reset Write Driver conducts, reversing the direction of tape saturation.

1-29. Each successive "one" bit changes the state of the Write Toggle flip-flop causing the set and reset write drivers to alternately conduct. After all characters have been written, "not" Delayed Write Reset ( $\overline{WRSD}$ ) from the write control circuits is gated with the Q output of the Write Toggle flip-flop to generate one more flux reversal if an odd number of bits was written in the channel. All Write Toggle flip-flops are therefore left in the clear state.

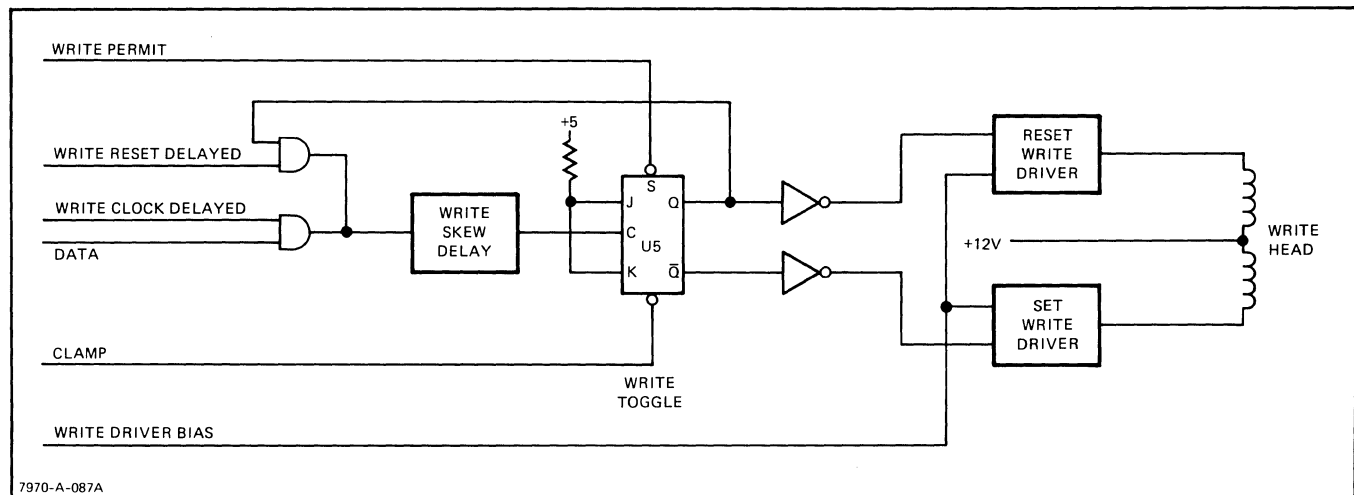


Figure 1-4. Typical Write Data Channel, Block Diagram

## SECTION II

### MAINTENANCE

#### 2-1. INTRODUCTION.

2-2. This section provides maintenance information for the write modules of the HP 7970B/7970C Digital Magnetic Tape Units. Maintenance information consists of performance test procedures and adjustment procedures. Prior to performing any maintenance to the write modules, ensure that the transport is functioning properly (refer to part 2) and that the read module circuits are operating within specifications. (Refer to part 3.)

#### 2-3. TEST EQUIPMENT REQUIRED.

2-4. In addition to the equipment required for transport maintenance (refer to part 2), the following tapes and test items are required to perform maintenance procedures described in this section.

- a. A means of generating a variety of write data patterns specified.
- b. A means of reading and detecting parity errors.
- c. Write Test Tape, part number 9162-0025.

#### Note

The HP 13192A Write Test Board is available as an accessory to provide all required write data patterns. When used in conjunction with the HP 13191A Control and Status Test Board and the HP 13193A Read Test Board, maintenance procedures can be performed without the aid of an interfaced computer.

#### 2-5. PERFORMANCE TEST PROCEDURES.

2-6. The following test procedures verify that the write module circuits conform to published specifications. The test procedures described assume the use of an on-line computer or the use of off-line test accessories.

#### 2-7. STATUS AND FUNCTION COMMAND TESTS.

2-8. The status and function command tests verify that the write circuits respond to input commands and that status circuits are operating properly.

2-9. SET WRITE ( $\overline{WSW}$ ). With the set write function true (from controlling device), a Forward ( $\overline{FWD}$ ) command will cause the  $\overline{WSW}$  line to be sampled within less than 20  $\mu$ s following  $\overline{FWD}$ . If  $\overline{WSW}$  is true (Low) then the internal

write condition will be set true if the tape unit is selected and on-line. Measurement is made as follows:

a. Connect the A probe of an oscilloscope to the write permit test point on the write control printed circuit assembly. When this level goes in the positive direction, write permit is true.

b. Connect the oscilloscope external sweep to the forward drive command from the controlling device  $\overline{FWD}$ ; and arrange the controlling device to provide bidirectional commands of sufficient length to exceed the start/stop time requirements for the unit. Synchronize sweep with this command.

c. The oscilloscope display should show the Write Permit line going in the positive direction within 5 to 15 microseconds following  $\overline{FWD}$ .

d. Observe that the following conditions exist at the write permit line as tape unit is put in the following modes.

- (1) Sequential  $\overline{FWD}$  commands: Write Permit remains true (steady level).
- (2) Sequential  $\overline{REV}$  commands: Permit remains false (steady level).
- (3)  $\overline{WSW}$  command removed and applied during bidirectional: With  $\overline{WSW}$  false, Write Permit remains false and at steady level. With  $\overline{WSW}$  true, Write Permit pulses with  $\overline{FWD}$  command.

2-10. WRITE STATUS ( $\overline{SW}$ ). Check to be sure status is true when selected tape unit is write enabled and  $\overline{WSW}$  is true.

#### 2-11. WRITE TIME ASYMMETRY TEST.

2-12. Write time asymmetry is the departure (in micro-inches) of the effective magnetic location of a data bit from that location which would make all sequential data bits equal distances apart. Measurement is made as follows:

a. Place unit in the read after write mode with all ones at 800 cpi.

b. Use channel A of oscilloscope and connect to read skew test point.

c. Sync oscilloscope sweep on negative edge and adjust oscilloscope main sweep rate so that the 10 divisions are equal to two bit-to-bit distances. When this is done, there will be a negative-going trailing edge at the beginning of the

sweep and at the end of the sweep. At the center, there may or may not be double trailing edges (this is the time asymmetry). Oscilloscope is now calibrated at 250 microinches per horizontal division, or 25 microinches if the X10 magnifier is used.

d. Observe the separation that may exist between the trailing edges at the center of the oscilloscope. The maximum acceptable condition is a total separation of 75 microinches.

### 2-13. WRITE/READ SKEW TEST.

2-14. The static skew of the write head is adjusted by electronic skew delays and is set to duplicate the effective bit positions exhibited by the IBM master alignment tape used to check and adjust the read electronic skew delays. Prior to performing the write/read skew test, perform the read skew test described in part 3. Log the results of the read skew test and perform the following procedures:

#### Note

Skew measurements can become somewhat difficult if significant write time asymmetry exists. When writing tapes for check of write/read skew, it is important that all write pulses start with the same relative flux polarities on tape. This can be assured if there is a sequence of reverse/stop/forward drive commands prior to a skew measurement. The forward command assures complete write reset conditions as the WSW line is made true.

- a. Write an all "1's" tape at 800 cpi.
- b. Read this tape in the read-after-write mode, and connect the channel A probe of an oscilloscope to the skew test point of the P-track read data printed-circuit assembly. Channel A of the oscilloscope will be used as a reference.
- c. Adjust the oscilloscope sweep to synchronize near the zero axis crossover on the positive slope. Set the oscilloscope to operate in the alternate mode.
- d. With the delayed sweep operated under a sweep rate of 2 microseconds/cm adjust the delay to display the positive-going step at the start of the channel P skew delay ramp on the center of the scope. This will be the zero time reference for all other measurements. Adjust channel B gain as required to obtain good resolution.
- e. Without making any further adjustments to the oscilloscope time base, move the channel B probe to each track skew delay test point in sequence and note its relative position to the center of the oscilloscope. Signals to the left of center are early, and may be noted as "plus" with those to the right noted as "minus" as they are later than the signal from track P.

f. When all measurements have been completed in the forward direction; the same sequence can be repeated for the reverse. It will be necessary to readjust the time delay for positioning track P to center.

g. Review data taken and determine the two tracks that are the earliest (largest plus number) and latest (largest minus number). The time differential between them (sum of the two times) converted to microinches for the tape speed involved is the write skew.

h. Compare the write skew readings taken with read skew test results. Any specific differences represent a measure of the ability of the tape unit write functions to duplicate the master alignment tape. A normally adjusted unit should duplicate the tape within  $\pm 1$  percent of the bit-to-bit distance at 800 cpi. This corresponds to a time difference equivalent to 25 microinches, or less.

### 2-15. WRITE/READ PHASING AND WRITE RESET TEST.

2-16. The following checks will verify that the write and read circuitry is correctly phased and that the LRCC character will be written.

a. Arrange for a write data program that will write three characters of all "1's", three characters of all "0's", followed by a Write Reset command. This program should be repetitive and usable for continuous writing.

b. With this program input and the tape unit operated in the read after write mode, observe the preamplifier output test points on each track.

c. Correct phasing and operation of the Write Reset command will result in a series of three recognizable "1" bits, three "0" bits and a single "1" bit. If phasing is correct, the first bit following the "1's" will be caused by the Write Reset and should be a positive-going pulse. It is essential that there be an odd number of all "1's" characters prior to the Write Reset command. The number of characters of all "0's" is not critical and is only to permit positive identification of the first character to follow.

### 2-17. ERASE/WRITE PHASING TEST.

2-18. This test is made only on the P track, and verifies that the erase head is correctly phased with respect to the write head. Evaluation is accomplished as follows:

a. Starting at loadpoint, write a section of all "0's" data for 30 to 60 seconds, then rewind tape to loadpoint.

b. Remove the P track write data card to preclude any further possibility of the write head changing the tape flux on the P track.

c. Place tape unit in a cyclic forward drive mode (FWD true/FWD false/FWD true, etc). During this period of

time (again 30 to 60 seconds) alternate periods of  $\overline{\text{WSW}}$  true/WSW false by manual operation of other means. Continue all "0's" program.

d. Operation as instructed in step "c" has resulted in intervals of tape (on track P) which have been magnetized by the write head during step "a" above, and other intervals which possibly have reversed flux polarity as set by the erase head if it is incorrectly phased.

e. After completion of steps "a" through "d", connect oscilloscope channel A to the output of channel P read pre-amplifier, and read the section of tape in steady forward or reverse drive mode. If the erase head is incorrectly phased, the flux reversal generated will produce full pulse amplitudes of approximately 3 volts zero-to-peak. A correctly phased head will show minor pulse disturbances as the erase current is applied. These levels will generally be below 15 percent of the zero-to-peak signal level or in the vicinity of 0.4 volts zero-to-peak, maximum.

#### 2-19. WRITE CROSSTALK TEST.

2-20. Write crosstalk (or write-feedthru) is a measure of the degree to which write head currents induce read head output voltages due to transformer action between the write and read heads. It is expressed as a percentage of the nominal read-after-write output level. Measurement is as follows:

a. Generate a random data write pattern and place tape unit in the read after write mode.

b. Connect oscilloscope to individual read preamplifier output test points and note the composite peak-to-peak output level (use relatively slow sweep speeds). This will be in the vicinity of 6.4 volts peak-to-peak for typical data.

c. Stop the tape unit but do not drop  $\overline{\text{WSW}}$  or give a  $\overline{\text{REV}}$  command. This state will allow the write data head currents to continue, provided the write clock and data are still present.

d. Again observe the peak-to-peak composite signal level present at the output of the read preamplifier. This peak-to-peak value must not exceed 5 percent of the value measured for the same track in step "b". Typical crosstalk levels must not exceed 320 millivolts peak-to-peak.

#### 2-21. INTERNAL WRITE CLOCK DELAY AND PULSE WIDTH TEST.

2-22. Measure the internal write clock delay by the following method.

a. The tape unit may be stopped in any mode. Write clock input signals are required.

b. Connect oscilloscope channel A to the Write Clock (WC) test point on the read control card and synchronize main sweep on negative slope.

c. Connect oscilloscope channel B to the delayed Write Clock ( $\overline{\text{WCD}}$ ) test point and using the alternate triggered by A mode, observe the time delay between the negative-going edge of the write clock and the positive-going edge of Write Clock delayed. This should be between 1 and 3 microseconds.

d. Using channel B only, sync on positive slope and observe the pulse width of the delayed Write Clock. This should be between 0.3 and 1.0 microsecond.

#### 2-23. DATA TRANSFER CHARACTERISTICS TEST.

2-24. The following checks cover the general data transfer characteristics of the tape unit and the final sequence of the performance checkout.

2-25. TAPE INTERCHANGEABILITY. Tape interchangeability optional test is evaluated by reading a specially prepared (random length) block tape written by a computer on a tape unit which has been specifically misadjusted to cause the maximum allowable write character skew (150 microinches absolute). The tape unit should read this tape in its entirety without read errors.

2-26. TOTAL DYNAMIC SKEW. Total dynamic skew is the microinch equivalent of the time interval between the arrival of the first and last bit of any read character under worst case data conditions (read or write) using tapes written on the unit under test. Measurement is made as follows:

a. Write a test tape having a maximum variety of random data patterns.

b. Connect channel A of the oscilloscope to the NOR test point on the read control card. The negative-going waveform at this point represents the arrival of the first data bit. All other data bits in the character will also generate negative-going waveforms at this point.

c. Sync the sweep on negative slope and adjust time as required to observe the total time required for all bits to arrive at the NOR test point.

d. This time, converted to equivalent microinches at the tape speed involved, represents the total dynamic skew of any worst case single character.

e. Operate tape unit in read-after-write, read forward, and read reverse modes. Under any of these conditions, the maximum dynamic skew must not exceed 200 microinches.

#### Note

If total dynamic skew is measured at the read clock (read clock jitter) it will appear as plus or minus dynamic skew and the total jitter band (less read clock pulse width) will correspond to  $\pm 200$  microinches.



2-27. **READ-AFTER-WRITE DATA TRANSFER.** Read-after-write data transfer is evaluated by writing a program having odd parity characters. The tape unit must operate error-free in the read-after-write mode throughout a full 10-1/2 inch reel of tape. Errors that can be positively associated with defects in the tape need not negate a test. Such errors will be read in both forward and reverse drive over the same area of the tape.

2-28. **READ ONLY DATA TRANSFER.** The tape generated during the read-after-write test must also be read error free in both the forward and reverse directions under read only operation.

## 2-29. ADJUSTMENT PROCEDURES.

2-30. The only adjustment for write data electronics is the write skew delay adjustment. Write skew delay provides additional assurance that tapes written on the unit will not have more than 150 microinches of absolute skew in any data character. This figure applies to any data pattern condition and includes all factors that cause bits to be displaced from theoretical locations. Prior to performing the write skew delay adjustment ensure that power supply adjustment, capstan adjustments, and all read data adjustments have been completed and verified.

2-31. Load the tape transport with a reel of scratch tape equipped with a write enable ring. Set all write skew delay controls fully ccw. Place the unit in synchronous forward

write mode and write a data pattern consisting of all "ones" at 800 cpi. Adjust the write skew delays as follows:

a. Using an oscilloscope, compare each read channel skew in a read-while-write condition to determine which channel is lagging the most.

b. Adjust the channel 2 write skew delay until channel 2 is slightly lagging the channel determined in step "a." Channel 2 will be used as a reference channel.

c. Connect the oscilloscope channel A probe to tape unit channel 2 read SKEW test point, and connect the oscilloscope channel B probe to the SKEW test point corresponding to the write data channel being adjusted. Set the oscilloscope controls to algebraically sum channels A and B. Adjust oscilloscope sweep to display at least one full bit time (leading edge of one bit to the leading edge of the next).

d. Adjust the skew delay variable resistor of the channel under adjustment to obtain a maximum amplitude on the oscilloscope display.

e. Repeat step "d" for all remaining channels except the reference channel (channel 2).

### Note

Under no circumstances are any of the read skew adjustments to be changed during the write skew compensation process.

## SECTION III

### REPLACEABLE PARTS

#### 3-1. INTRODUCTION.

3-2. This section provides information for ordering replacement parts for the write modules of the HP 7970B/7970C Digital Magnetic Tape Units.

3-3. This section contains assembly parts lists, supporting illustrations, ordering information, and a part number cross reference.

#### 3-4. ASSEMBLY PARTS LISTS.

3-5. The assembly parts lists represent a breakdown of all replaceable parts of the write data package. The information contained in the lists are under the following headings:

- a. FIGURE & INDEX NO.
- b. PART NUMBER.
- c. DESCRIPTION.
- d. UNITS PER ASSY.

#### 3-6. FIGURE AND INDEX NUMBER.

3-7. The figure and index number column will identify the figure that illustrates each listed item and the index number that identifies the item on the illustration.

#### 3-8. PART NUMBER.

3-9. The part number column provides the Hewlett-Packard part number for each item listed in the assembly parts list.

#### 3-10. DESCRIPTION.

3-11. The description column describes the items within the article. An indented column arrangement is used to show the relationship between a part and the next higher

assembly. The top assembly of each listing appears in indentation 1. Primary subassemblies (of top assembly) and attaching parts appear in indentation 2. This method of indentation is continued through indentation 3, 4, etc., until all replaceable parts are listed. Attaching parts are listed immediately following the part they attach. Attaching parts are identified by the abbreviation (AP) enclosed in parentheses at the end of the description.

3-12. Reference designation and manufacture information (if applicable) is also included in the description column.

#### 3-13. UNITS PER ASSEMBLY.

3-14. The quantity shown in the units per assembly column reflects the total quantity of a part required by the next higher assembly of that part. This quantity is not necessarily the total used for the complete equipment. The abbreviation AR is used to indicate usage as required of a particular item. The abbreviation REF is used to indicate that the quantity of an item used per assembly is listed in the next higher assembly of the group assembly parts list.

#### 3-15. ORDERING INFORMATION.

3-16. To order replacement parts, address the order or inquiry to the local Hewlett-Packard Sales and Service Office (Refer to the list at the end of this manual for addresses.) Specify the following information for each part ordered.

- a. Identification of the unit, kit, or assembly containing the part.
- b. Hewlett-Packard part number for each part.
- c. Description of each part.
- d. Circuit reference designation (if applicable).

#### 3-17. PART NUMBER CROSS REFERENCE.

3-18. Table 3-1 at the end of this section provides a cross reference between Hewlett-Packard part numbers and manufacturer's part numbers.

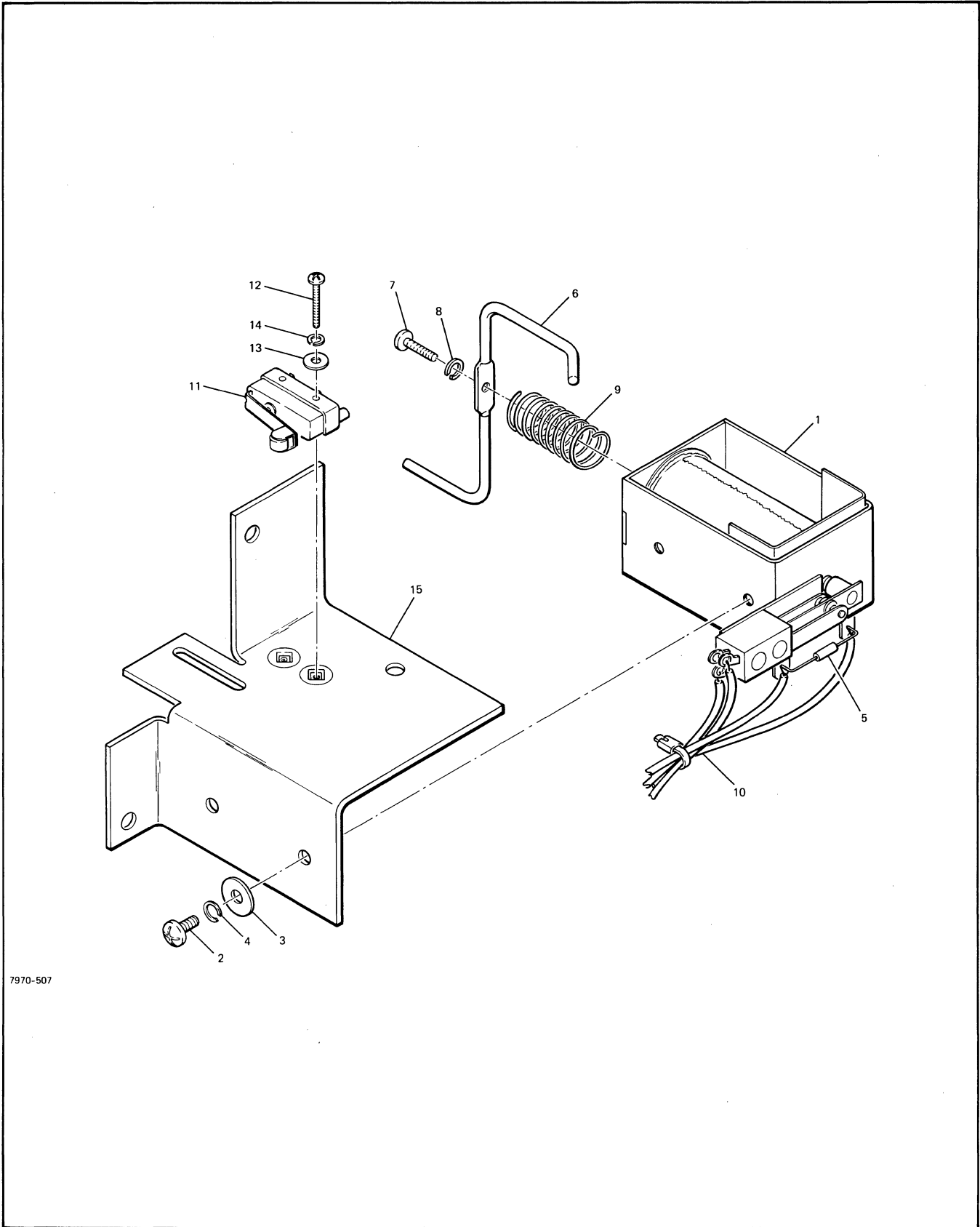
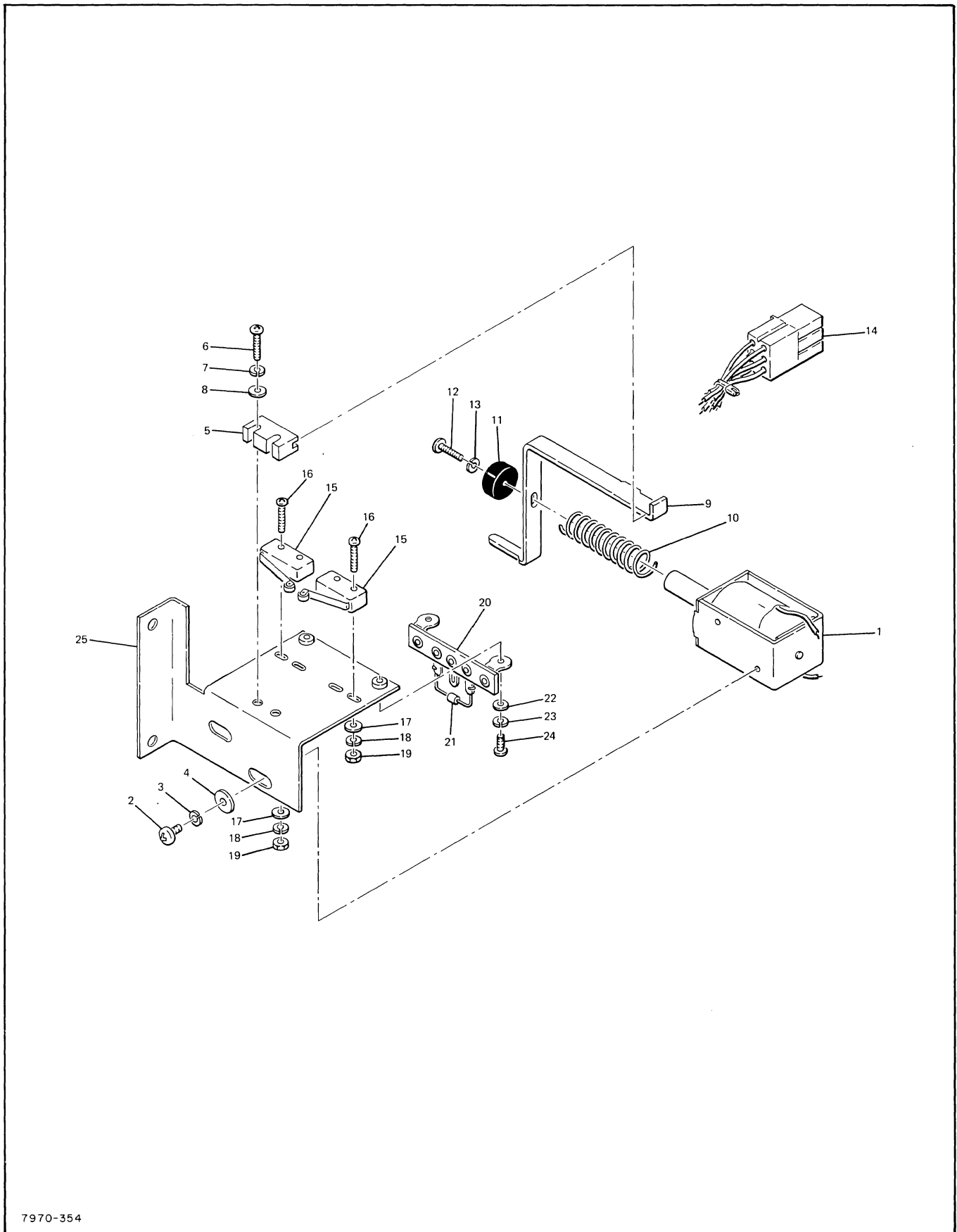


Figure 3-1. Write Enable Assembly A10



7970-354

Figure 3-1. Write Enable Assembly A10

FIGURE & INDEX NO.	PART NUMBER	DESCRIPTION					UNITS PER ASSY
		1	2	3	4	5	
3-1-	07970-62122	WRITE ENABLE ASSEMBLY A10 . . . . .					REF
-1	0491-0062	. SOLENOID, 24 Vdcw (L1) . . . . .					1
-2	2360-0193	. . SCREW, no. 6-32, 0.25-inch, pozi (AP) . . . . .					2
-3	2190-0227	. . WASHER, flat (AP) . . . . .					2
-4	2190-0085	. . WASHER, lock, helical (AP) . . . . .					2
-5	1901-0039	. DIODE, Si (CR1) . . . . .					1
-6	07970-20833	. ACTUATOR, write enable . . . . .					1
-7	2200-0145	. . SCREW, no. 4-40, 0.437-inch, pozi (AP) . . . . .					1
-8	2190-0003	. . WASHER, lock, helical (AP) . . . . .					1
-9	1460-1288	. SPRING, compression . . . . .					1
-10	07970-62123	. CABLE ASSEMBLY (W1) . . . . .					1
-11	3102-0009	. . SWITCH, sensitive (S2) . . . . .					1
-12	0520-0131	. . SCREW, no. 2-56, 0.437-inch, pozi (AP) . . . . .					2
-13	2190-0417	. . WASHER, flat (AP) . . . . .					2
-14	2190-0040	. . WASHER, lock, helical (AP) . . . . .					2
-15	07970-01187	. BRACKET, write enable . . . . .					1



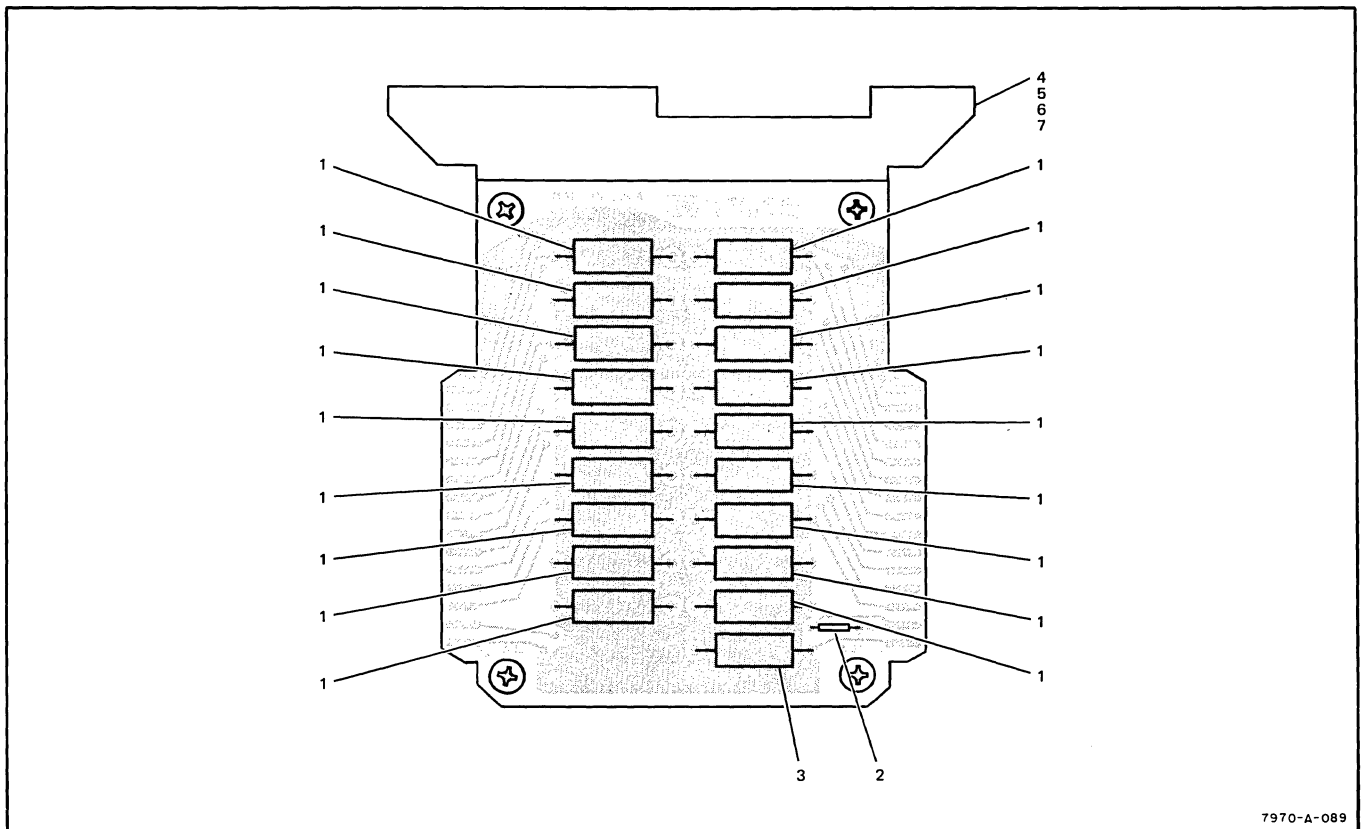


Figure 3-2. Write Interconnect PC Assembly A14

FIGURE & INDEX NO.	PART NUMBER	DESCRIPTION					UNITS PER ASSY
		1	2	3	4	5	
3-2-	07970-60300	WRITE INTERCONNECT PC ASSEMBLY A14 . . . . .					REF
-1	0698-3622	. RESISTOR, fxd, 120 ohms, 5%, 2W (R2 thru R19) . . . . .					18
-2	1901-0025	. DIODE, Si (CR1) . . . . .					1
-3	0698-3627	. RESISTOR, fxd, 200 ohms, 5%, 2W (R1) . . . . .					1
-4	07970-00440	. BRACKET, write interconnect PC assembly . . . . .					1
-5	2360-0195	. . SCREW, no. 6-32, 0.312-inch, pozi (AP) . . . . .					4
-6	2190-0085	. . WASHER, lock, helical (AP) . . . . .					4
-7	3050-0228	. . WASHER, flat (AP) . . . . .					4

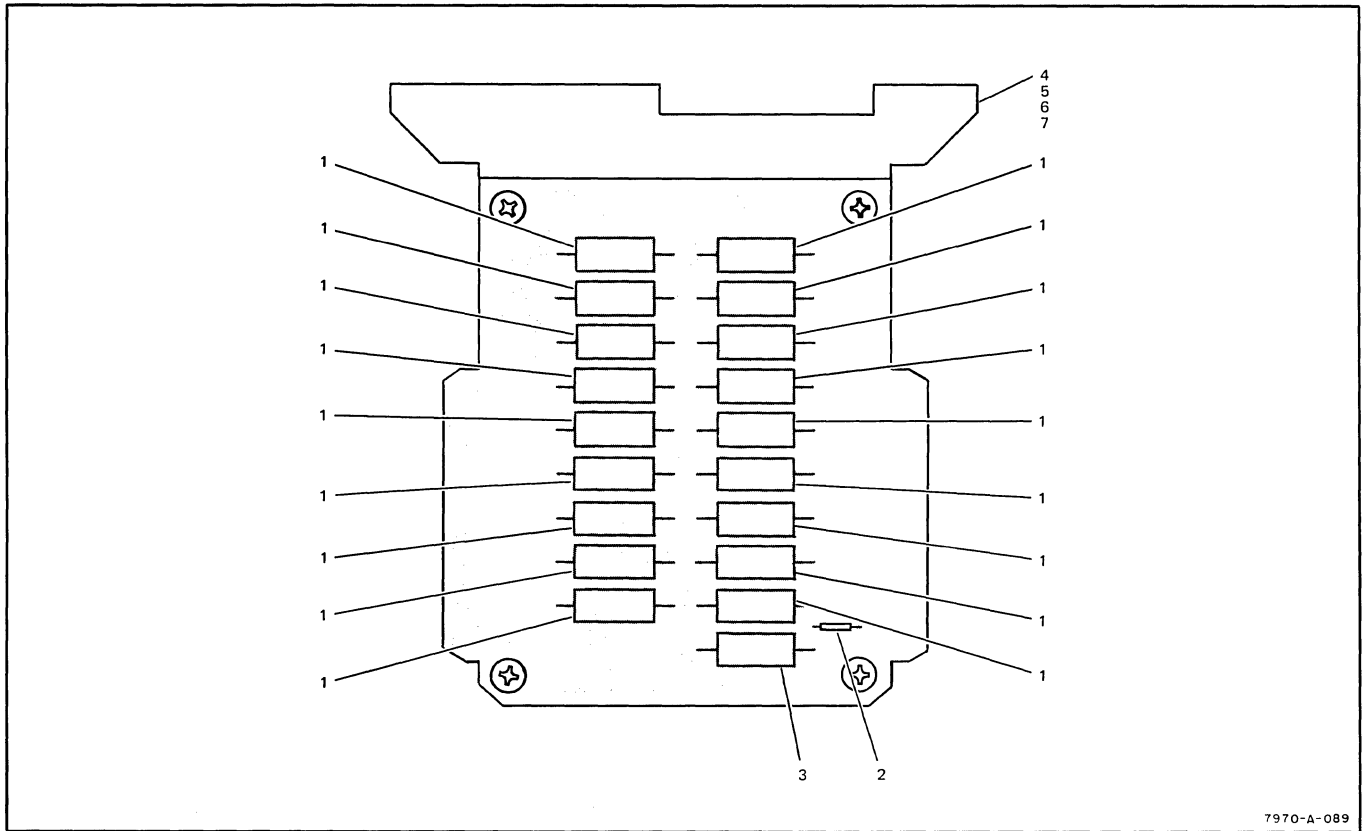
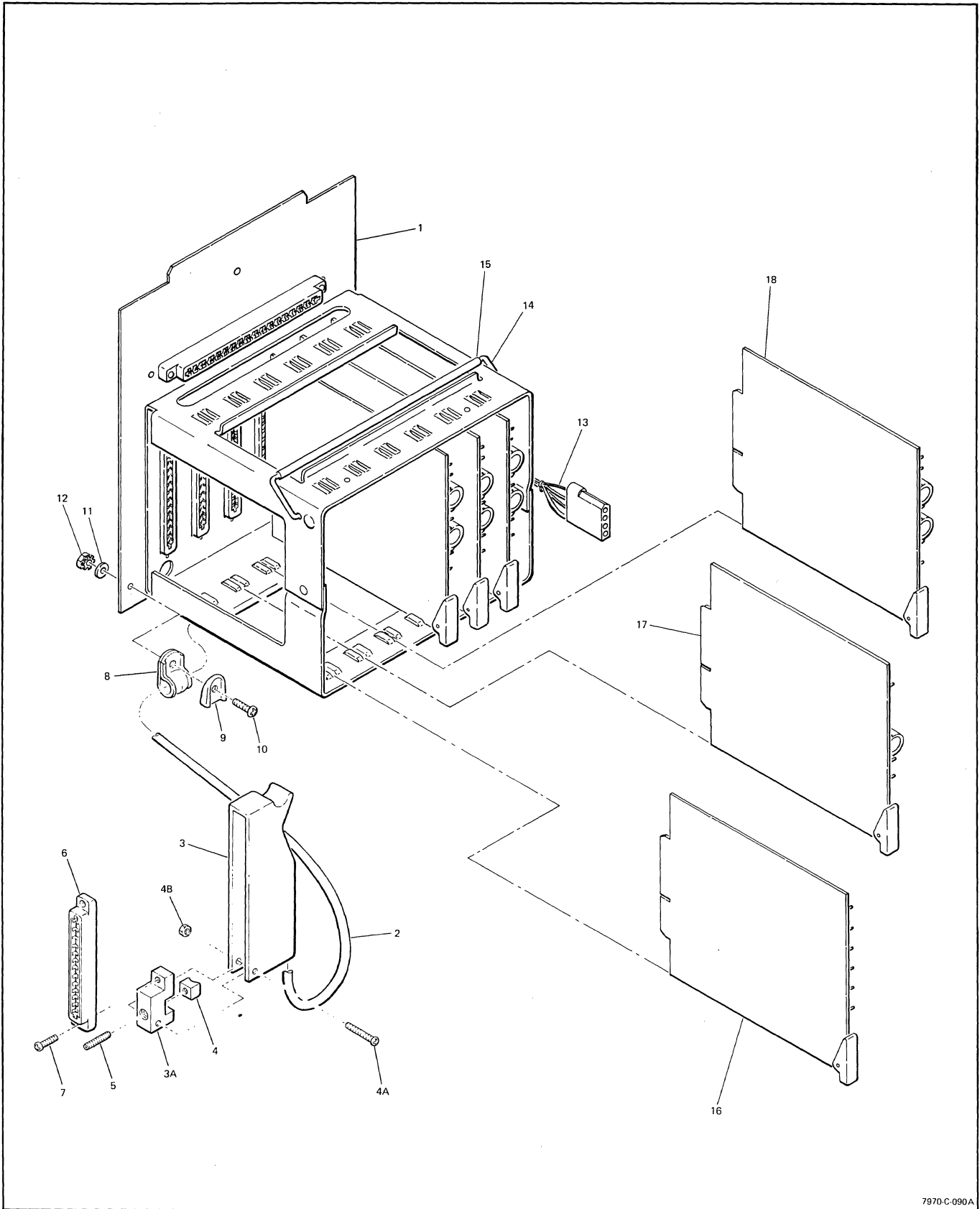


Figure 3-2. Write Interconnect PC Assembly A14

FIGURE & INDEX NO.	PART NUMBER	DESCRIPTION					UNITS PER ASSY
		1	2	3	4	5	
3-2-	07970-62165	WRITE INTERCONNECT PC ASSEMBLY A14 (10 to 20.9 ips) . . . . .					REF
3-2-	07970-60300	WRITE INTERCONNECT PC ASSEMBLY A14 (21 to 45 ips) . . . . .					REF
-1	0698-3626	. RESISTOR, fxd, 180 ohms, 5%, 2W (R2 thru R19) (10 to 20.9 ips) . . . . .					18
-1	0698-3622	. RESISTOR, fxd, 120 ohms, 5%, 2W (R2 thru R19) (21 to 45 ips) . . . . .					18
-2	1901-0025	. DIODE, Si (CR1) . . . . .					1
-3	0698-3624	. RESISTOR, fxd, 150 ohms, 5%, 2W (R1) (10 to 20.9 ips) . . . . .					1
-3	0698-3627	. RESISTOR, fxd, 200 ohms, 5%, 2W (R1) (21 to 45 ips) . . . . .					1
-4	07970-00440	. BRACKET, write interconnect PC assembly . . . . .					1
-5	2360-0195	. . . SCREW, no. 6-32, 0.312-inch, pozi (AP) . . . . .					4
-6	2190-0085	. . . WASHER, lock, helical (AP) . . . . .					4
-7	3050-0228	. . . WASHER, flat (AP) . . . . .					4





7970-C-090A

Figure 3-3. Write Assembly A17



FIGURE & INDEX NO.	PART NUMBER	DESCRIPTION					UNITS PER ASSY
		1	2	3	4	5	
3-3-	Reference Only	WRITE ASSEMBLY A17 . . . . .					REF
-1	07970-60230	. WRITE MOTHERBOARD ASSEMBLY . . . . .					1
-2	8120-1535	. . CABLE, shielded, 29 conductor . . . . .					3 ft.
-3	07970-40204	. . HOLDER, connector . . . . .					1
-3A	5040-6072	. . . BLOCK, mounting . . . . .					1
-4	5040-6003	. . CLAMP, cable, connector holder . . . . .					1
-4A	2200-0091	. . . SCREW, no. 4-40, 0.562-inch, pozi (AP) . . . . .					1
-4B	2260-0001	. . . NUT, Hex, no. 4-40 (AP) . . . . .					1
-5	3030-0143	. . . SCREW, set, no. 6-32, 0.500-inch, socket head (AP) . . . . .					1
-6	1251-0159	. . CONNECTOR, printed circuit . . . . .					1
-7	0624-0098	. . . SCREW, tapping, no. 4-40, 0.438-inch, pozi (AP) . . . . .					2
-8	1400-0440	. . CLAMP, cable, 0.250-inch (AP) . . . . .					1
-9	2190-0452	. . . WASHER, flat (AP) . . . . .					1
-10	2360-0199	. . . SCREW, no. 6-32, 0.438-inch, pozi (AP) . . . . .					1
-11	3050-0227	. . . WASHER (AP) . . . . .					1
-12	2420-0001	. . . NUT, hex, no. 6-32 (AP) . . . . .					1
-13	07970-60410	. . CABLE ASSEMBLY, write power (W1) . . . . .					1
-14	07970-00470	. . RETAINING SPRING, PC board . . . . .					1
-15	1400-0795	. . TIE, cable, spiral, 0.250-inch . . . . .					5.8 in.
-16	----	. WRITE CONTROL PC ASSEMBLY A17A1 (See figure 3-4 for details.) . . . . .					1
-17	----	. WRITE DATA PC ASSEMBLY A17A2, single-channel . . . . . (See figure 3-5 for details.)					1
-18	----	. WRITE DATA PC ASSEMBLY A17A3 thru A17A6, dual-channel . . . . . (See figure 3-6 for details.)					3 or 4*

\*A17A3 is used only in 9-track applications.



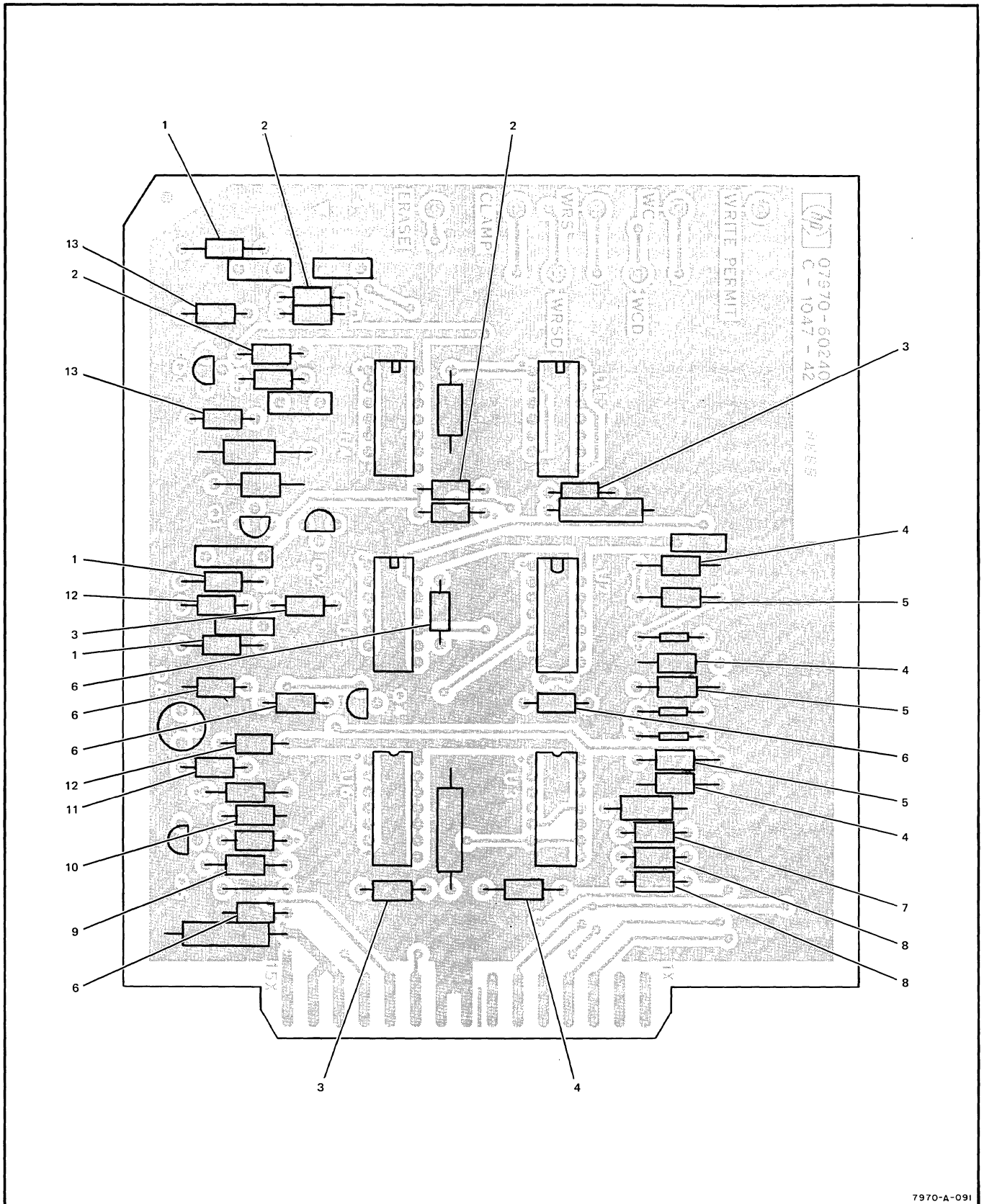


Figure 3-4. Write Control PC Assembly (Sheet 1 of 2)

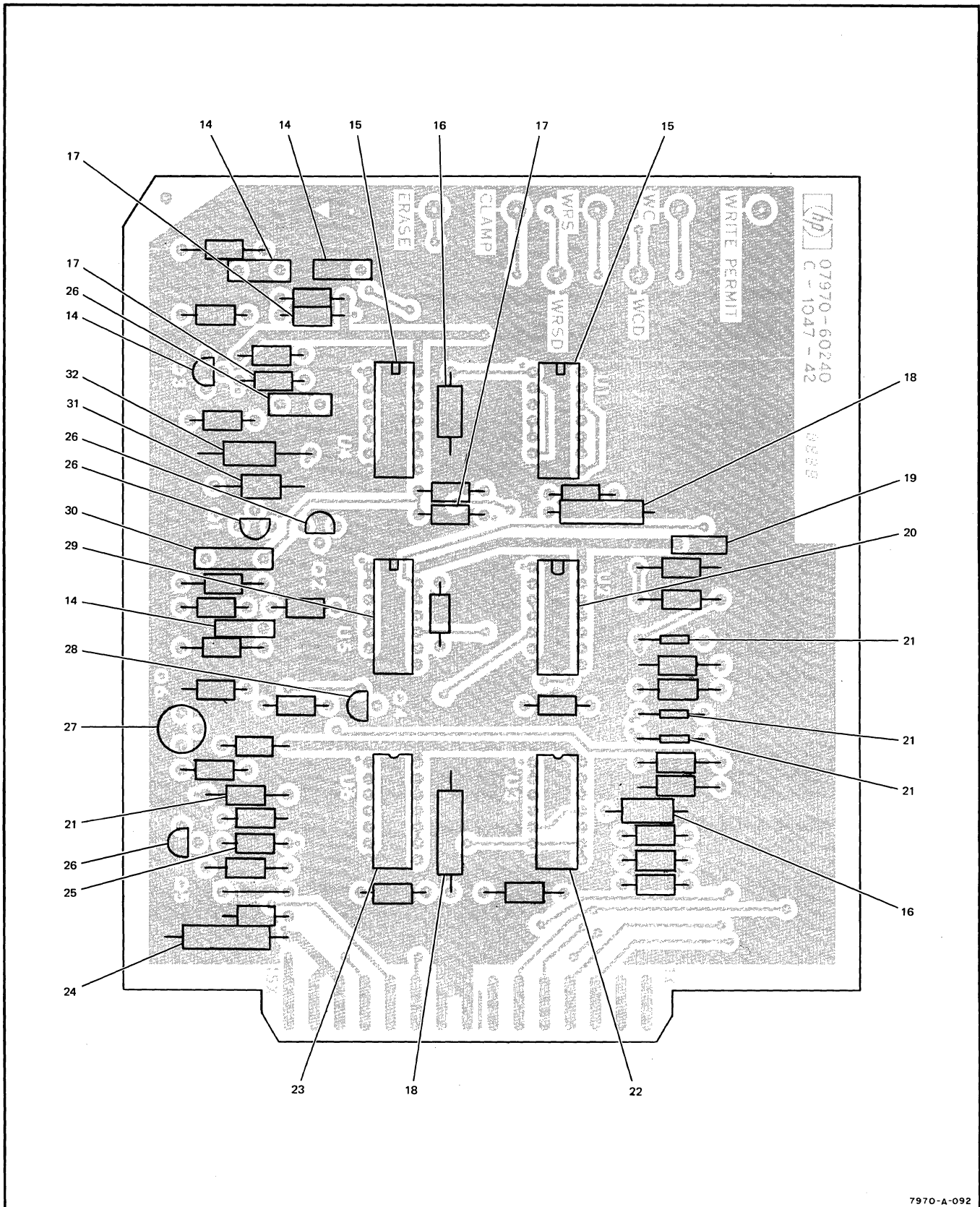


Figure 3-4. Write Control PC Assembly (Sheet 2 of 2)

FIGURE & INDEX NO.	PART NUMBER	DESCRIPTION					UNITS PER ASSY
		1	2	3	4	5	
3-4-	07970-60240	WRITE CONTROL PC ASSEMBLY A17A1 . . . . .					REF
-1	0757-0290	. RESISTOR, fxd, 6.19k, 1%, 1/8W (R8, R12, R25) . . . . .					3
-2	0683-3925	. RESISTOR, fxd, 3.9k, 5%, 1/4W (R10, R14, R27) . . . . .					3
-3	0683-8205	. RESISTOR, fxd, 82 ohms, 5%, 1/4W (R15, R28, R30) . . . . .					3
-4	0757-0428	. RESISTOR, fxd, 1.62k, 1%, 1/8W (R3, R18, R22, R24) . . . . .					4
-5	0757-0418	. RESISTOR, fxd, 619 ohms, 1%, 1/8W (R17, R21, R23) . . . . .					3
-6	0683-1025	. RESISTOR, fxd, 1k, 5%, 1/4W (R4, R5, R6, R29, R33) . . . . .					5
-7	0683-2225	. RESISTOR, fxd, 2.2k, 5%, 1/4W (R31) . . . . .					1
-8	0683-1825	. RESISTOR, fxd, 1.8k, 5%, 1/4W (R, R2) . . . . .					2
-9	0698-0084	. RESISTOR, fxd, 2.15k, 1%, 1/8W (R20) . . . . .					1
-10	0698-0085	. RESISTOR, fxd, 2.61k, 1%, 1/8W (R7) . . . . .					1
-11	0683-3015	. RESISTOR, fxd, 300 ohms, 5%, 1/4W (R11) . . . . .					1
-12	0683-1035	. RESISTOR, fxd, 10k, 5%, 1/4W (R9, R16) . . . . .					2
-13	0683-5625	. RESISTOR, fxd, 5.6k, 5%, 1/4W (R13, R26) . . . . .					2
-14	0160-2207	. CAPACITOR, fxd, 300 pF, 5%, 300 Vdcw (C8, C9, C10, C11) . . . . .					4
-15	1820-0054	. INTEGRATED CIRCUIT, type 7400N (U1, U4) . . . . .					2
-16	0160-0153	. CAPACITOR, fxd, 0.001 $\mu$ F, 10%, 200 Vdcw (C1, C2) . . . . .					2
-17	1910-0016	. DIODE, Ge (CR1, CR5, CR7) . . . . .					3
-18	0160-0161	. CAPACITOR, fxd, 0.01 $\mu$ F, 10% (C25, C26) . . . . .					2
-19	0160-2055	. CAPACITOR, fxd, 0.01 $\mu$ F, -20 +80%, 100 Vdcw (C7) . . . . .					1
-20	1820-0095	. INTEGRATED CIRCUIT, type 848 (U2) . . . . .					1
-21	1901-0040	. DIODE, Si (CR2, CR4, CR6, CR9) . . . . .					4
-22	1820-0256	. INTEGRATED CIRCUIT (U3) . . . . .					1
-23	1820-0441	. INTEGRATED CIRCUIT (U6) . . . . .					1
-24	0180-1746	. CAPACITOR, fxd, 15 $\mu$ F, 10%, 20 Vdcw (C4) . . . . .					1
-25	1902-1261	. DIODE (CR3) . . . . .					1
-26	1854-0270	. TRANSISTOR, NPN, Si, 2N4265 (Q1, Q2, Q3, Q4) . . . . .					4
-27	1853-0016	. TRANSISTOR, PNP, Si, (Q6) . . . . .					1
-28	1854-0246	. TRANSISTOR Q4) . . . . .					1
-29	1820-0269	. INTEGRATED CIRCUIT (U5) . . . . .					1
-30	0160-2210	. CAPACITOR, fxd, 470 pF, 5%, 300 Vdcw (C5) . . . . .					1
-31	0160-0300	. CAPACITOR, fxd, 0.0027 $\mu$ F, 10%, 20 Vdcw (C6) . . . . .					1
-32	0180-0106	. CAPACITOR, fxd, 60 $\mu$ F, 20%, 6 Vdcw (C3) . . . . .					1

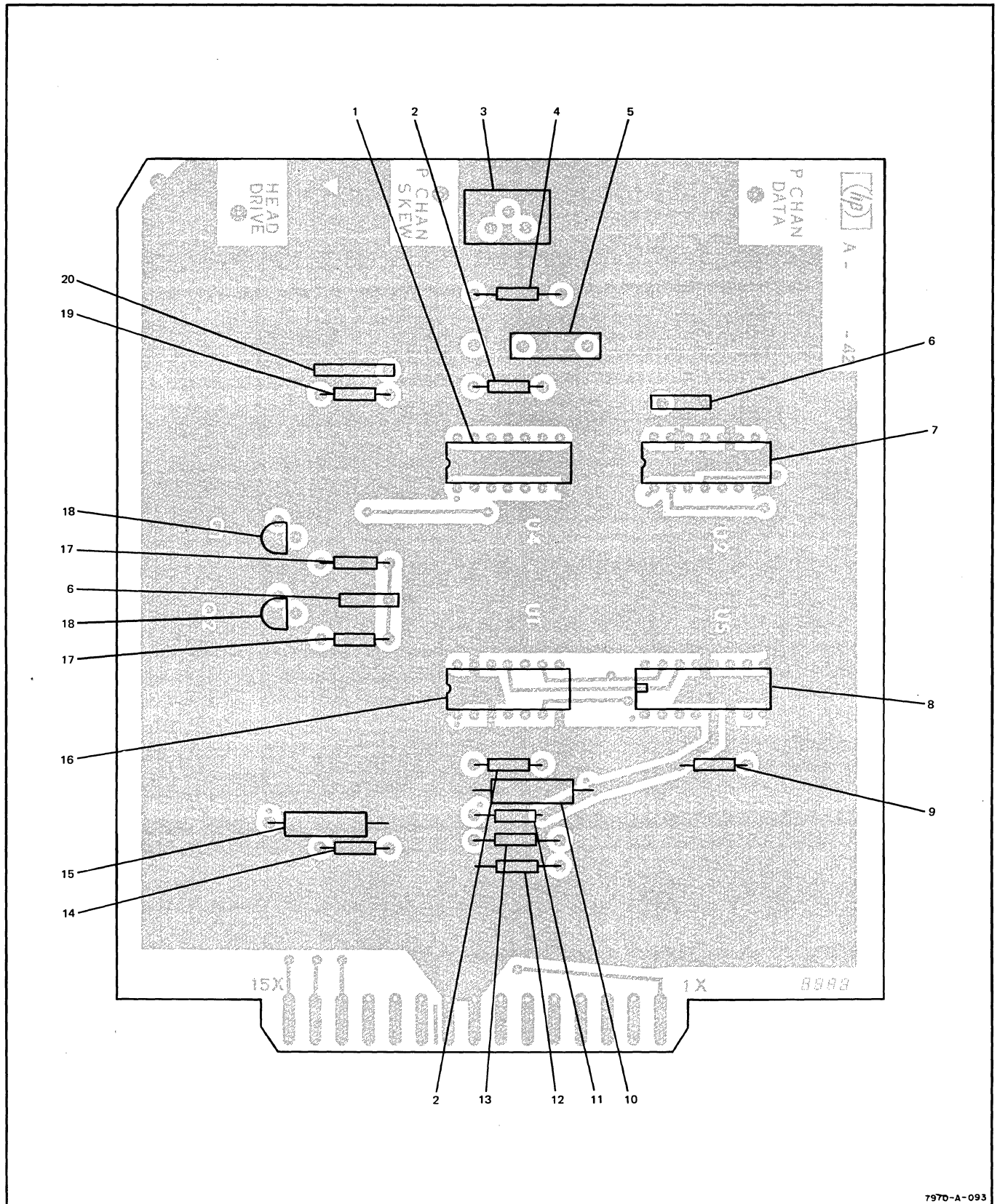


Figure 3-5. Single-Channel Write Data PC Assembly



FIGURE & INDEX NO.	PART NUMBER	DESCRIPTION					UNITS PER ASSY
		1	2	3	4	5	
3-5-	07970-60820	WRITE DATA PC ASSEMBLY A17A3, single-channel, 10-20.9 ips . . . . .					REF
3-5-	07970-60830	WRITE DATA PC ASSEMBLY A17A2, single-channel, 21-45 ips . . . . .					REF
-1	1820-0088	. INTEGRATED CIRCUIT, type 850 (U4) . . . . .					1
-2	0683-2225	. RESISTOR, fxd, 2.2k, 5%, 1/4W (R6, R27) . . . . .					2
-3	2100-1761	. RESISTOR, var, ww, 10k, 5%, 1W (R11) . . . . .					1
-4	0698-3153	. RESISTOR, fxd, 38.3k, 1%, 1/8W (R12) . . . . .					1
-5	0160-2373	. CAPACITOR, fxd, 4700 pF, 2%, 300 Vdcw (C4) . . . . . (Used on 07970-60820)					1
-5	0160-2227	. CAPACITOR, fxd, 2400 pF, 5%, 300 Vdcw (C4) . . . . . (Used on 07970-60830)					1
-6	0160-2055	. CAPACITOR, fxd, 0.01 μF, 100 Vdcw (C6, C9) . . . . .					2
-7	1820-0094	. INTEGRATED CIRCUIT, type 846 (U2) . . . . .					1
-8	1820-0076	. INTEGRATED CIRCUIT, type 7476N (U5) . . . . .					1
-9	0683-1025	. RESISTOR, fxd, 1k, 5%, 1/4W (R13) . . . . .					1
-10	0180-0106	. CAPACITOR, fxd, 60 μF, 20%, 6 Vdcw (C1) . . . . .					1
-11	1901-0040	. DIODE, Si (CR1) . . . . .					1
-12	0757-0428	. RESISTOR, fxd, 16.2k, 1%, 1/8W (R2) . . . . .					1
-13	0757-0418	. RESISTOR, fxd, 619 ohms, 1%, 1/8W (R1) . . . . .					1
-14	0683-1005	. RESISTOR, fxd, 10 ohms, 5%, 1/4W (R20) . . . . .					1
-15	0180-1746	. CAPACITOR, fxd, 15 μF, 10%, 20 Vdcw (C7) . . . . .					1
-16	1820-0479	. INTEGRATED CIRCUIT (U1) . . . . .					1
-17	0683-8215	. RESISTOR, fxd, 820 ohms, 5%, 1/4W (R16, R17) . . . . .					2
-18	1854-0246	. TRANSISTOR (Q1, Q2) . . . . .					2
-19	0683-2205	. RESISTOR, fxd, 20 ohms, 5%, 1/4W (R5) . . . . .					1
-20	0150-0121	. CAPACITOR, fxd, 0.1 μF, -20 +80%, 50 Vdcw (C2) . . . . .					1

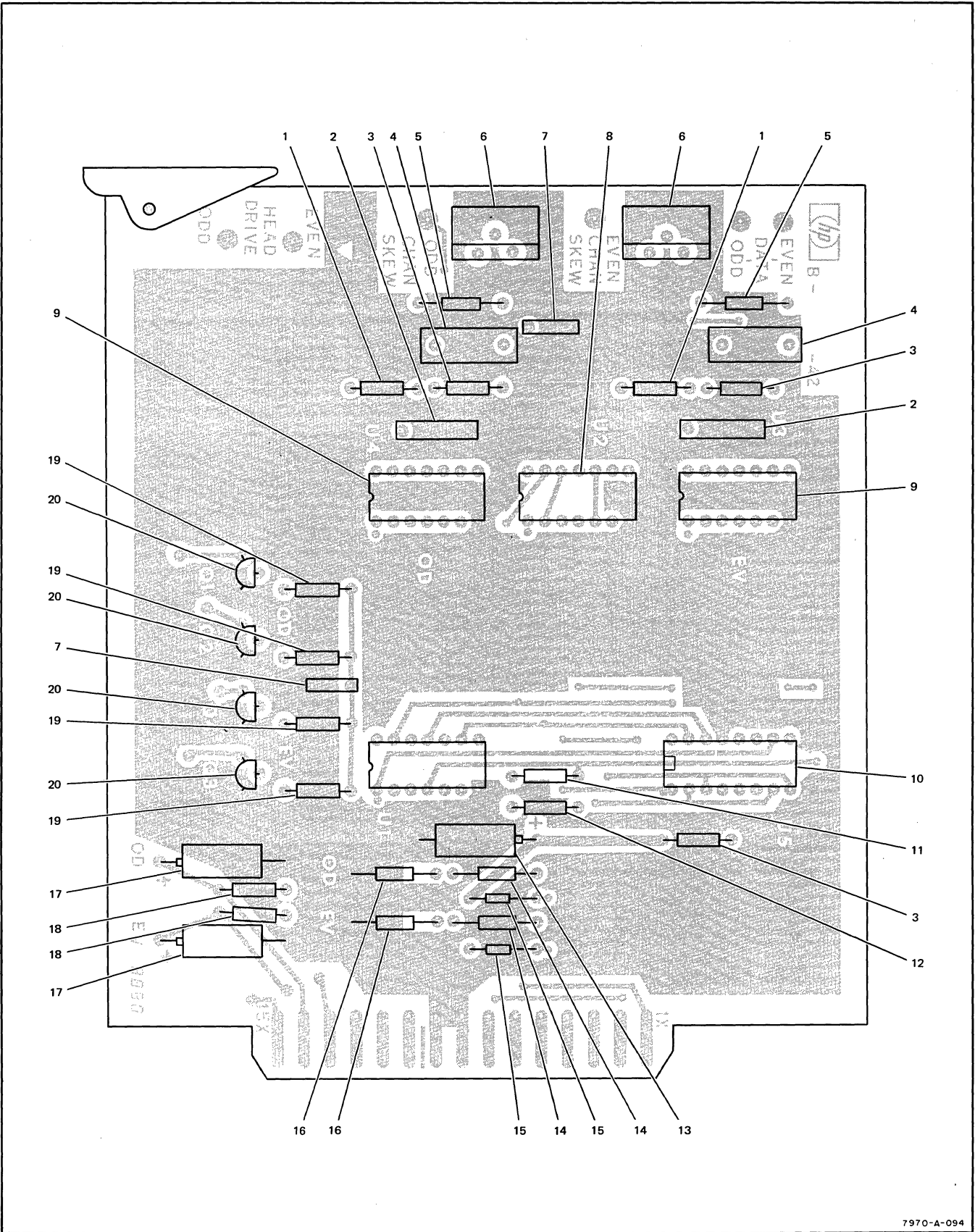


Figure 3-6. Dual-Channel Write Data PC Assembly

FIGURE & INDEX NO.	PART NUMBER	DESCRIPTION					UNITS PER ASSY
		1	2	3	4	5	
3-6-	07970-60800	WRITE DATA PC ASSEMBLY A17A3 thru A17A6, dual-channel, 10-20.9 ips . . . . .					REF
3-6-	07970-60810	WRITE DATA PC ASSEMBLY A17A3 thru A17A6, dual-channel, 21-45 ips . . . . .					REF
-1	0683-2205	. RESISTOR, fxd, 22 ohms, 5%, 1/4W (R5, R10) . . . . .					2
-2	0150-0121	. CAPACITOR, fxd, 0.1 $\mu$ F, 50 Vdcw (C2, C3) . . . . .					2
-3	0683-2225	. RESISTOR, fxd, 2.2k, 5%, 1/4W (R6, R9, R27, R28) . . . . .					4
-4	0160-2373	. CAPACITOR, fxd, 4700 pF, 2%, 300 Vcdw (C4, C5) . . . . . (Used on 07970-60800)					2
-4	0160-2227	. CAPACITOR, fxd, 2400 pF, 5%, 300 Vdcw (C4, C5) . . . . . (Used on 07970-60810)					2
-5	0698-3153	. RESISTOR, fxd, 3.83k, 1%, 1/8W (R12, R14) . . . . .					2
-6	2100-1761	. RESISTOR, var, ww, 10k, 5%, 1W (R11, R15) . . . . .					2
-7	0160-2055	. CAPACITOR, fxd, 0.01 $\mu$ F, 100 Vdcw (C6, C9) . . . . .					2
-8	1820-0094	. INTEGRATED CIRCUIT, type 846 (U2) . . . . .					1
-9	1820-0088	. INTEGRATED CIRCUIT, type 851 (U3, U4) . . . . .					2
-10	1820-0479	. INTEGRATED CIRCUIT (U1) . . . . .					1
-11	1820-0076	. INTEGRATED CIRCUIT, type 7476N (U5) . . . . .					1
-12	0683-1025	. RESISTOR, fxd, 1k, 5%, 1/4W (R13) . . . . .					1
-13	0180-0106	. CAPACITOR, fxd, 60 $\mu$ F, 20%, 6 Vdcw (C1) . . . . .					1
-14	0757-0418	. RESISTOR, fxd, 619 ohms, 1%, 1/8W (R1, R3) . . . . .					2
-15	1901-0040	. DIODE, Si (CR1, CR2) . . . . .					2
-16	0757-0428	. RESISTOR, fxd, 1.62k, 1%, 1/8W (R2, R4) . . . . .					2
-17	0180-1746	. CAPACITOR, fxd, 15 $\mu$ F, 10%, 20 Vdcw (C7, C8) . . . . .					2
-18	0683-1005	. RESISTOR, fxd, 10 ohms, 5%, 1/4W (R20, R25) . . . . .					2
-19	0683-8215	. RESISTOR, fxd, 820 ohms, 5%, 1/4W (R16, R17, R18, R19) . . . . .					4
-20	1854-0246	. TRANSISTOR (Q1, Q2, Q3, Q4) . . . . .					4

Table 3-1. Part Number Cross Reference

HP PART NUMBER	MFR CODE	MFR PART NUMBER
0150-0121	56289	5C50BIS-CML
0160-0153	56289	192P10292-PTS
0160-0161	56289	192P10392-PTS
0160-0300	56289	192P27292-PTS
0160-2055	56289	C023F101F103ZS22-CDH
0160-2207	28480	0160-2207
0160-2210	28480	0160-2210
0160-2227	28480	0160-2227
0160-2373	28480	0160-2373
0180-0106	28480	0180-0106
0180-1746	28480	0180-1746
0360-1290	83330	853
0403-0091	77969	9102A
0491-0058	28480	0491-0058
0520-0133	00000	OBD
0610-0001	00000	OBD
0624-0098	00000	OBD
0683-1005	01121	CB 1005
0683-1025	01121	CB 1025
0683-1035	01121	CB 1035
0683-1825	01121	CB 1825
0683-2205	01121	CB 2205
0683-2225	01121	CB 2225
0683-3015	01121	CB 3015
0683-3925	01121	CB 3925
0683-5625	01121	CB 5625
0683-8205	01121	CB 8205
0683-8215	01121	CB 8215
0698-0084	28480	0698-0084
0698-0085	28480	0698-0085
0698-3153	28480	0698-3153
0698-3622	28480	0698-3622
0698-3627	28480	0698-3627
0757-0290	28480	0757-0290
0757-0428	28480	0757-0428
1251-0159	71785	251-15-30-261
1400-0292	95987	1/4-6B
1400-0795	05593	SWP-1/4XXT(100')

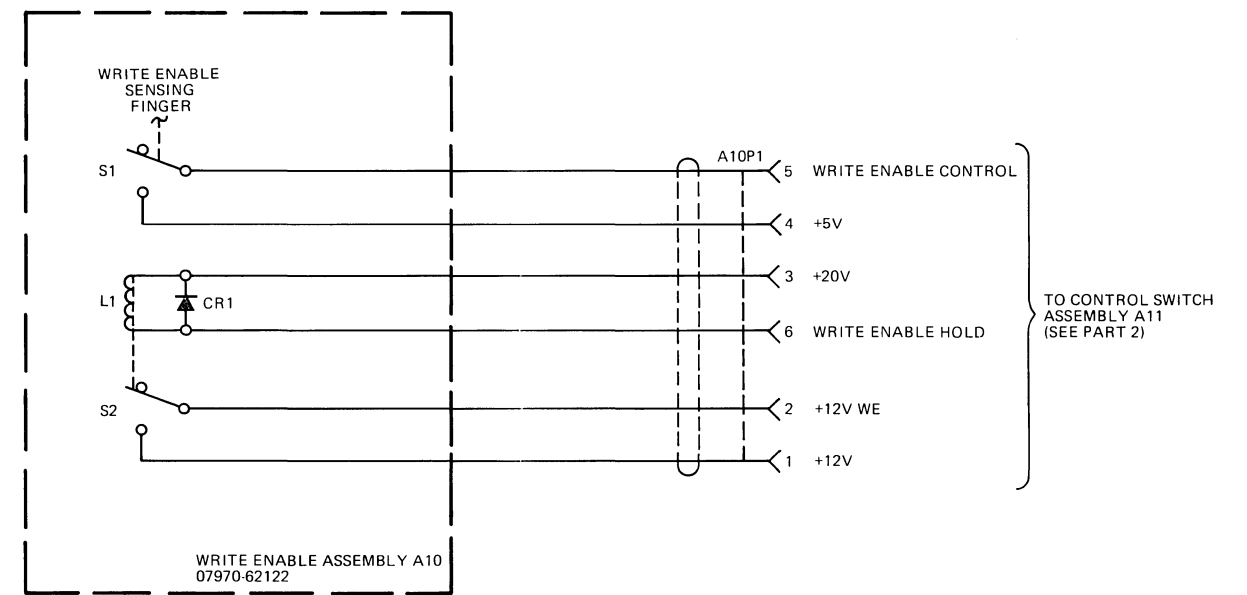
HP PART NUMBER	MFR CODE	MFR PART NUMBER
1460-1239	00000	OBD
1820-0054	01295	SN7400N
1820-0076	01295	SN7476N
1820-0088	04713	MC851P
1820-0094	28480	1820-0094
1820-0095	01295	SN15848N
1820-0256	04713	MC858P
1820-0269	01295	SN7403N
1820-0441	04713	MC1801P
1820-0479	04713	MC835P
1853-0016	80131	2N3638
1854-0246	80131	2N3643
1854-0270	80131	2N4265
1901-0025	07263	FD 2387
1901-0026	04713	SR1358-8
1901-0040	07263	FDG1088
1902-1261	28480	1902-1261
1910-0016	93332	D2361
2100-1761	28480	2100-1761
2190-0003	28480	2190-0003
2190-0085	00000	OBD
2190-0117	28480	2190-0117
2190-0128	00000	OBD
2190-0416	00000	OBD
2190-0452	95987	D6-140
2200-0139	00000	OBD
2200-0145	00000	OBD
2200-0147	00000	OBD
2360-0193	00000	OBD
2360-0195	00000	OBD
2360-0199	00000	OBD
2420-0001	78189	OBD
3030-0143	00000	OBD
3050-0066	28480	3050-0066
3050-0227	80120	AN960AC-6
3050-0228	80120	MS15795-305
3102-0009	80207	2LMW-E
8120-1535	28480	8120-1535

## **SECTION IV**

# **MAINTENANCE DIAGRAMS**

This section contains schematic and parts location diagrams for the write modules of the HP 7970B/7970C Digital Magnetic Tape Units.





7970-525

Figure 4-1. Write Enable Assembly A10, Schematic Diagram

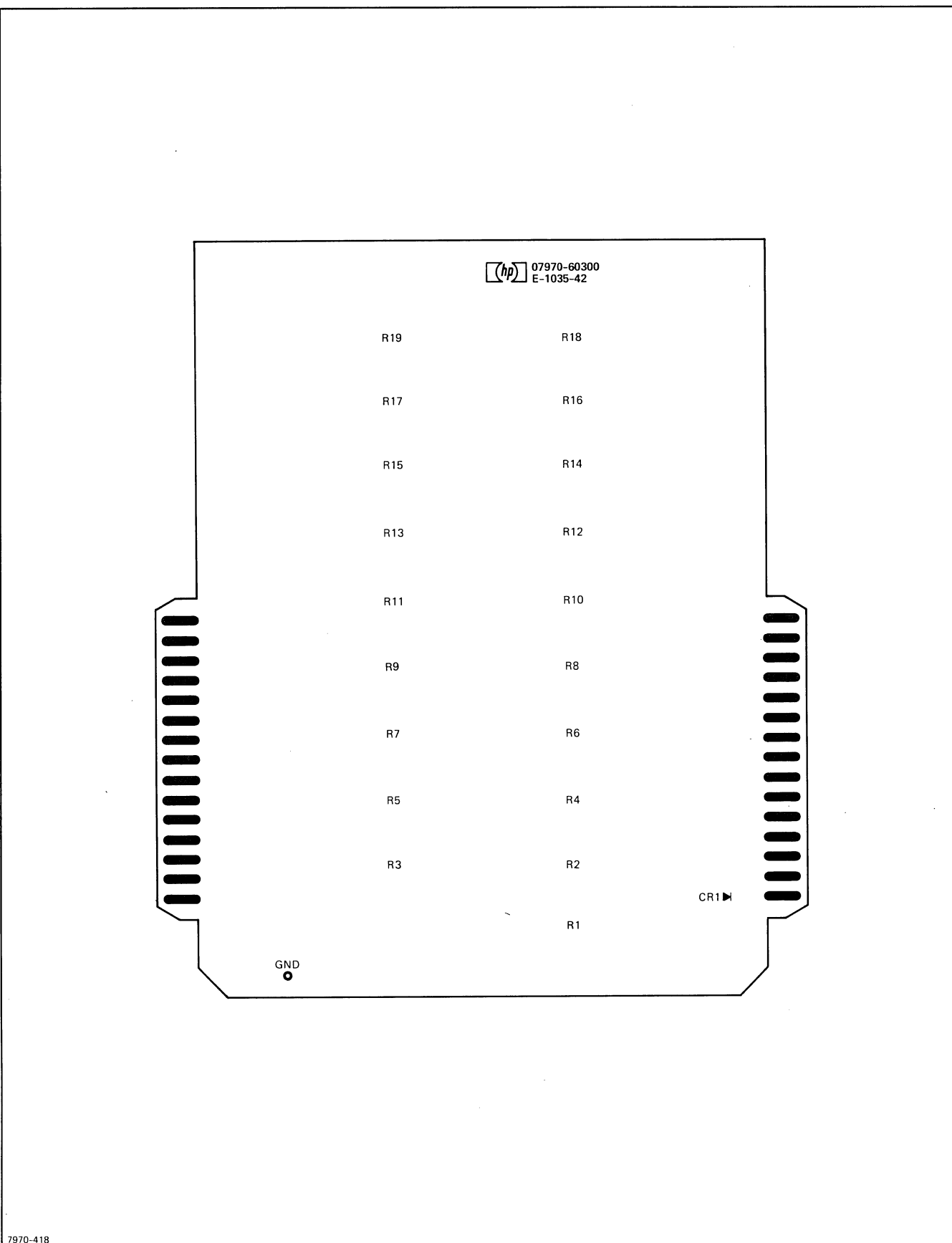


Figure 4-2. Write Interconnect PC Assembly A14, Parts Location Diagram

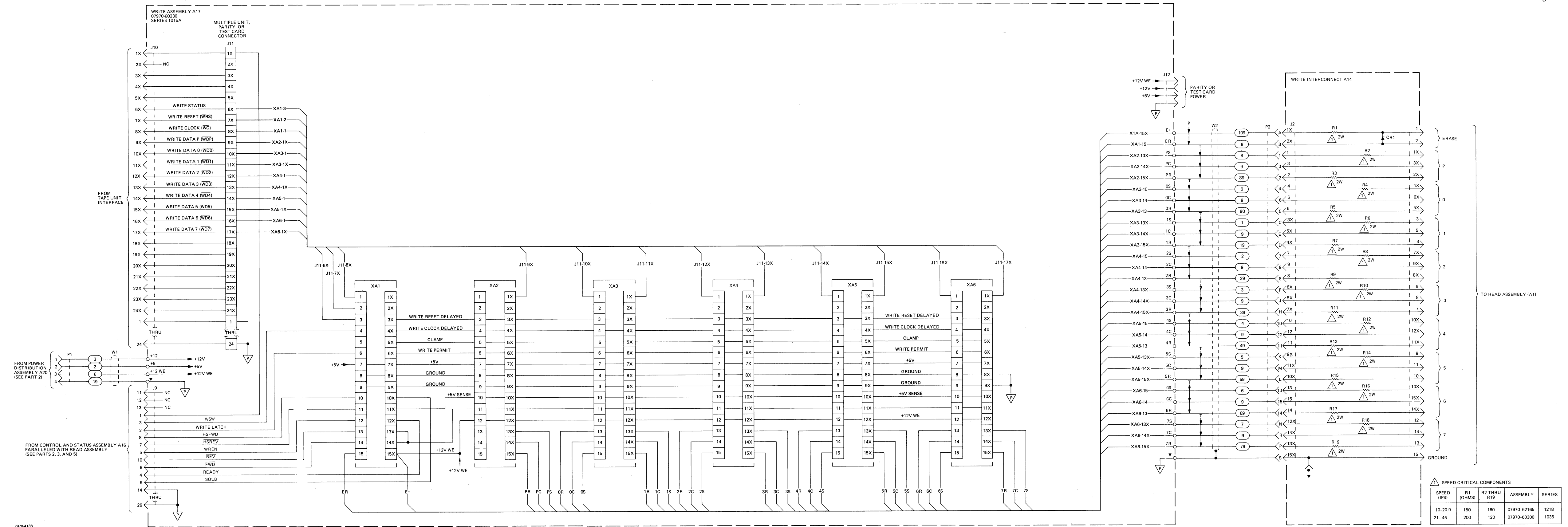


Figure 4-3. Write Assembly A17 (Motherboard) and Write Interconnect PC Assembly A14, Schematic Diagram



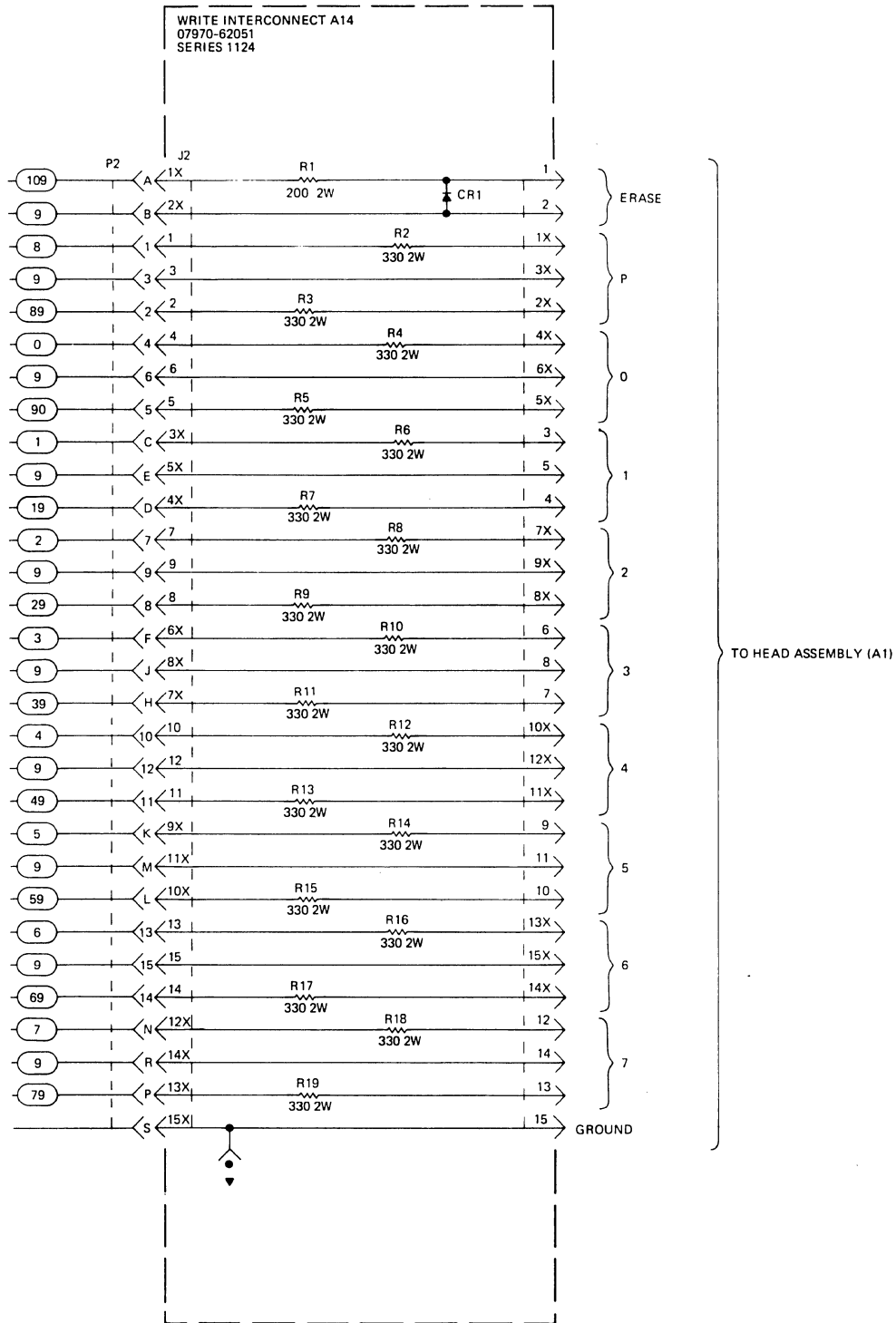


Figure 4-3. Write Assembly A17 (Motherboard) and Write Interconnect Assembly A14, Schematic Diagram



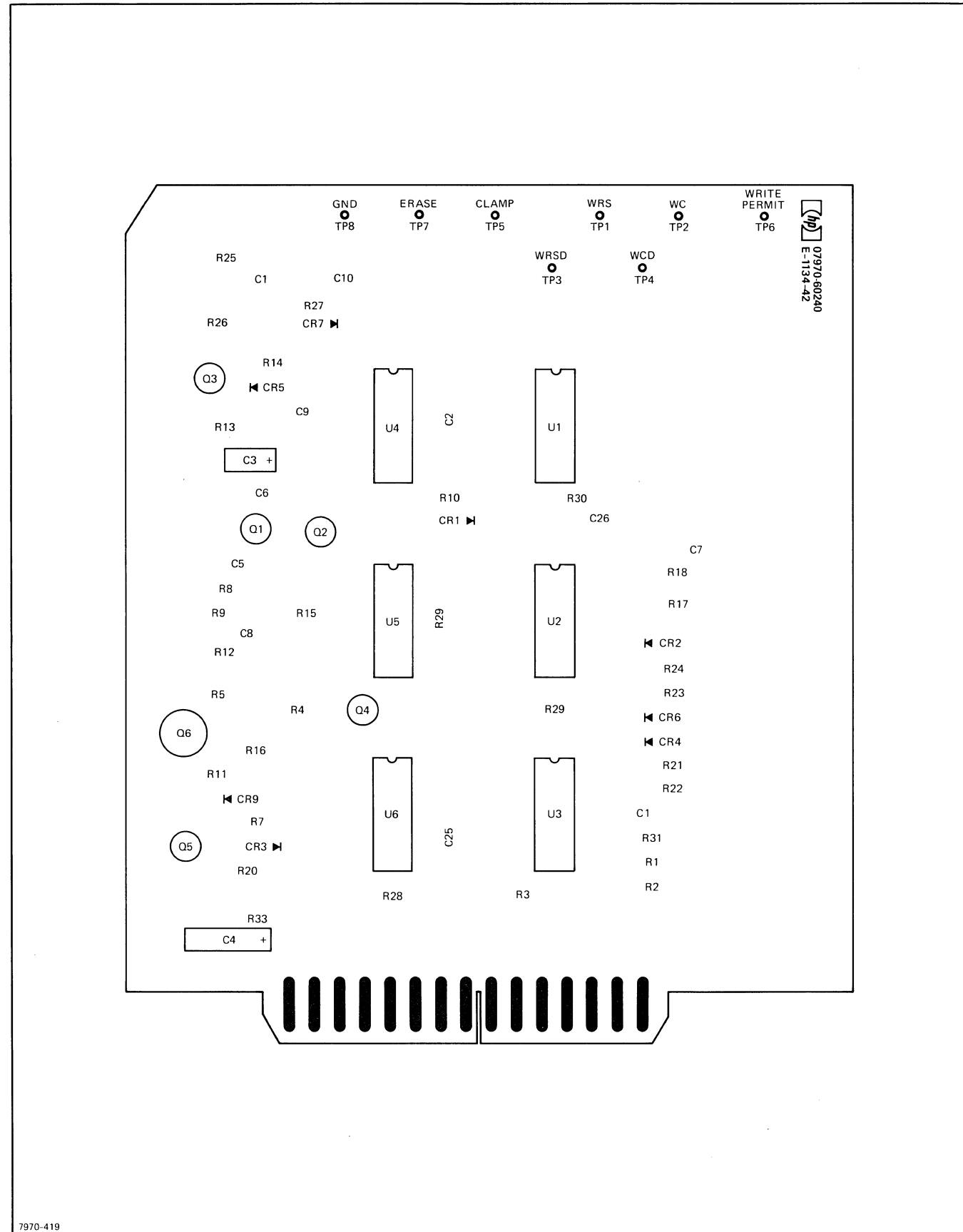


Figure 4-4. Write Control PC Assembly, Parts Location Diagram

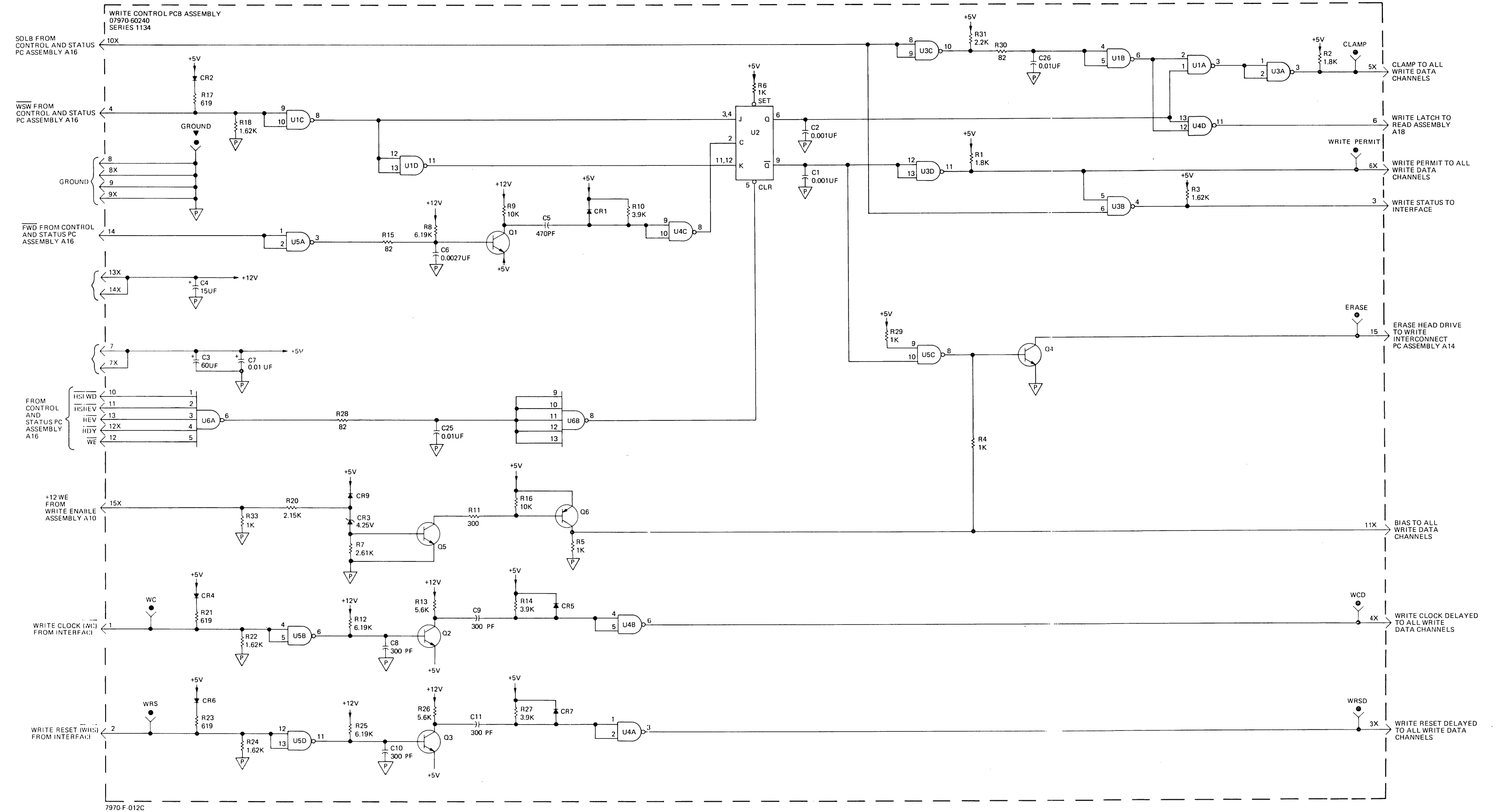


Figure 4-5. Write Control PC Assembly, Schematic Diagram

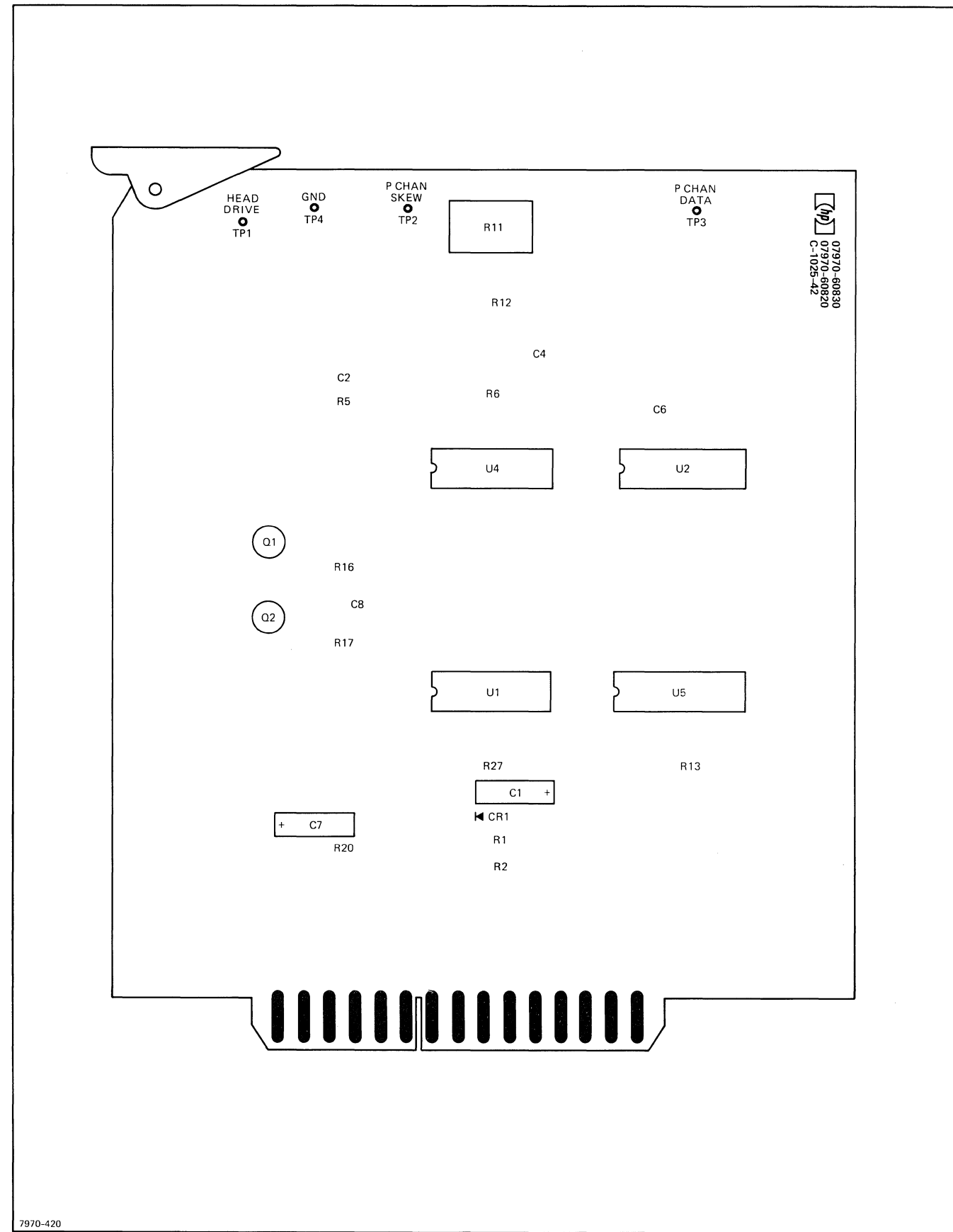


Figure 4-6. Single-Channel Write Data PC Assembly, Parts Location Diagram

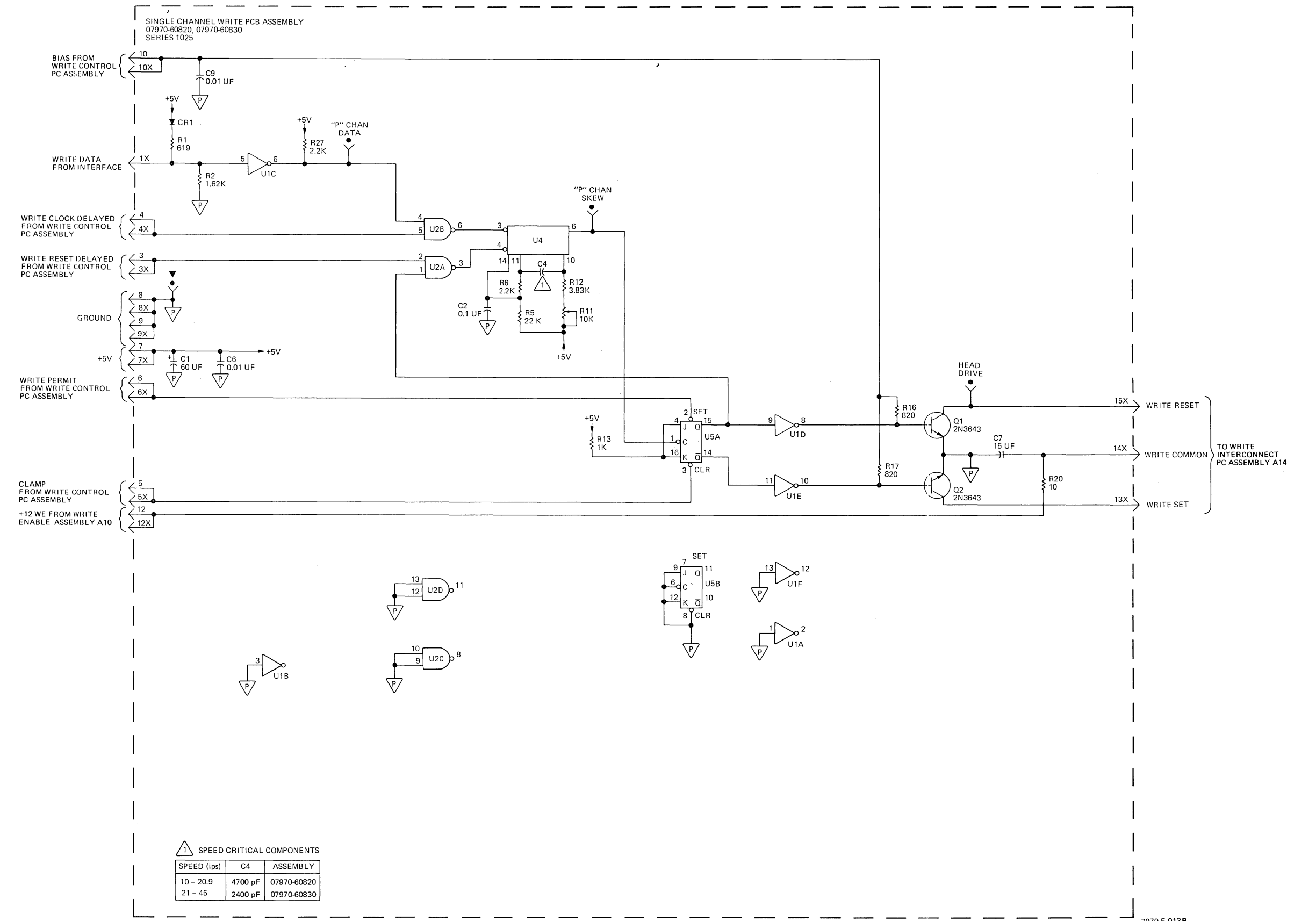


Figure 4-7. Single-Channel Write Data PC Assembly, Schematic Diagram

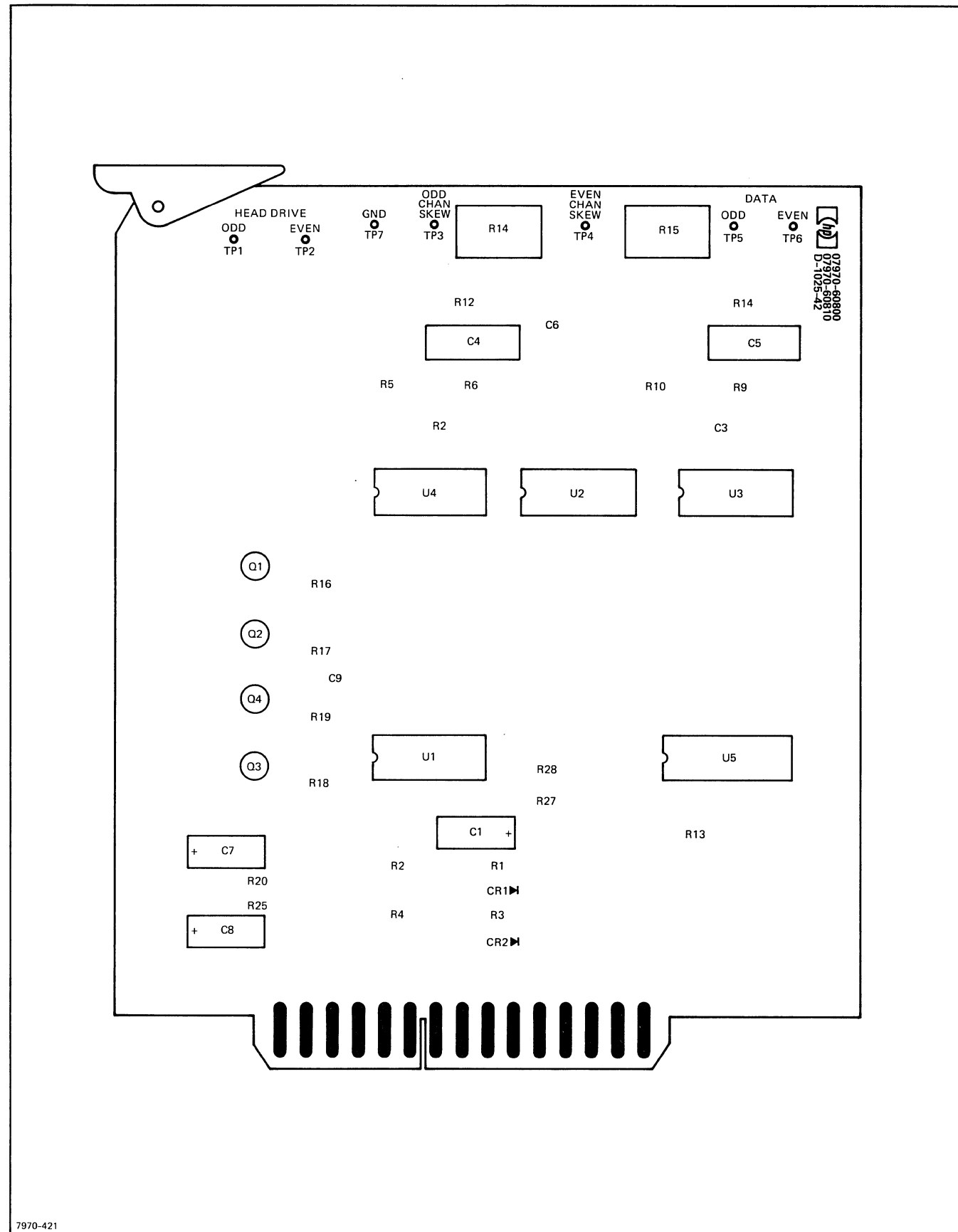


Figure 4-8. Dual-Channel Write Data PC Assembly, Parts Location Diagram

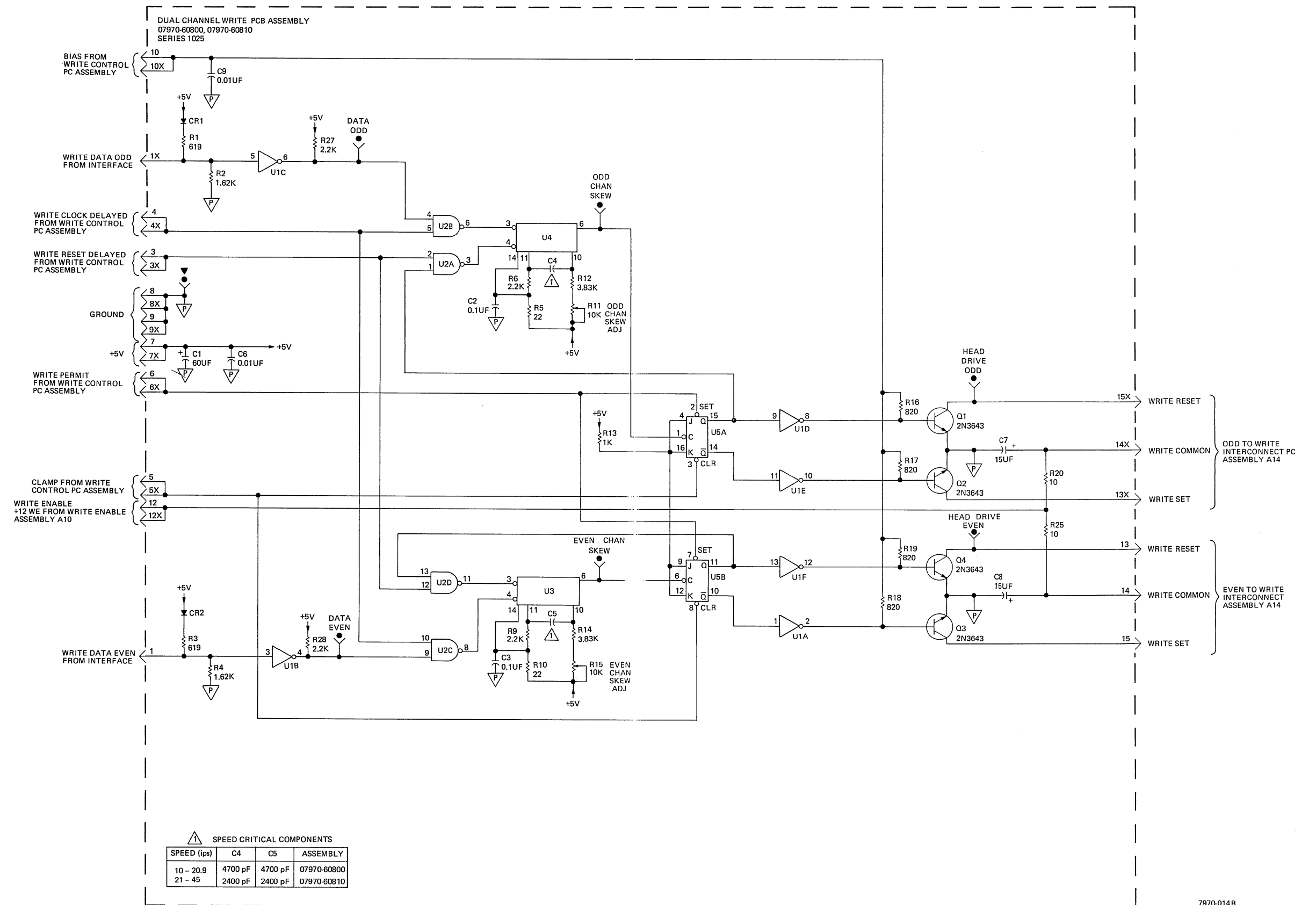


Figure 4-9. Dual-Channel Write Data PC Assembly, Schematic Diagram