HP 13255

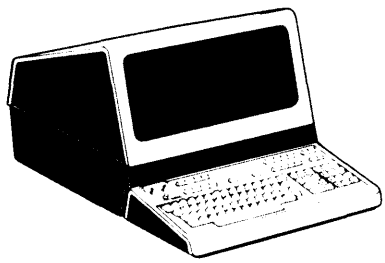
+2K MEMORY MODULE

Manual Part No. 13255-91064

PRINTED

AUG-01-76

DATA TERMINAL
TECHNICAL INFORMATION



HEWLETT hp PACKARD

Printed in U.S.A.

1.0 INTRODUCTION.

The +2K Memory Module allows expansion of 264XX Data Terminal memory capacity. The read/write memory is accessible through the terminal bus and is organized in 2,048 by 8-bit bytes. This memory module uses dynamic MOS RAM chips organized 4K by 1-bit in a 22-pin, dual-in-line package.

2.0 OPERATING PARAMETERS.

A summary of operating parameters for the +2K Memory Module is contained in tables 1.0 through 5.0.

Table 1.0 Physical Parameters

Part Number	Nomenclature	Size (L x W x D) +/-0.100 Inches	Weight (Pounds)
02640-60064	+2K Memory PCA	12.5 x 4.0 x 0.5	0.44

Number of Backplane Slots Required: 1

HP 13255

+2K MEMORY MODULE

Manual Part No. 13255-91064

PRINTED

AUG-01-76

NOTICE

The information contained in this document is subject to change without notice.

HEWLETT-PACKARD MAKES NO WARRANTY OF ANY KIND WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Hewlett-Packard shall not be liable for errors contained herein or for incidental or consequential damages in connection with the furnishing, performance, or use of this material.

NOTE: This document is part of the 264XX DATA TERMINAL product series Technical Information Package (HP 13255).

1.0 INTRODUCTION.

The +2K Memory Module allows expansion of 264XX Data Terminal memory capacity. The read/write memory is accessible through the terminal bus and is organized in 2,048 by 8-bit bytes. This memory module uses dynamic MOS RAM chips organized 4K by 1-bit in a 22-pin, dual-in-line package.

2.0 OPERATING PARAMETERS.

A summary of operating parameters for the +2K Memory Module is contained in tables 1.0 through 5.0.

Table 1.0 Physical Parameters

Part Number	Nomenclature	Size (L x W x D) +/-0.100 Inches	Weight (Pounds)
02640-60064	+2K Memory PCA	12.5 x 4.0 x 0.5	0.44

Number of Backplane Slots Required: 1

Table 2.0 Reliability and Environmental Information

Environmental: (X) HP Class B ( ) Other:
Restrictions: Type tested at product level
Failure Rate: 1.192 (percent per 1000 hours)

Table 3.0 Power Supply and Clock Requirements - Measured
(At +/-5% Unless Otherwise Specified)

+5 Volt Supply	+12 Volt Supply	-12 Volt Supply	-42 Volt Supply
@ 120 mA	@ 30 mA	@ 14 mA	@ mA
			NOT APPLICABLE

115 volts ac	220 volts ac
@ A	@ A
NOT APPLICABLE	NOT APPLICABLE

Clock Frequency: 4.915 MHz +/0.1%

Table 4.0 Jumper Definitions

PCA Designation	Function	
	In	Out
RAM START ADD		
2K	Add 0 to Start Address of Module.	Add 2K to Start Address of Module.
4K	Add 0 to Start Address of Module.	Add 4K to Start Address of Module.
8K	Add 0 to Start Address of Module.	Add 8K to Start Address of Module.
16K	Add 0 to Start Address of Module.	Add 16K to Start Address of Module.
32K	Add 0 to Start Address of Module.	Add 32K to Start Address of Module.
	(All in is Start Address of 0)	(All out is Start Address of 62K)

5.0 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P1, Pin 1	+5V	+5 Volt Power Supply
-2	GND	Ground Common Return (Power and Signal)
-3	SYS CLK	4.915 MHz System Clock
-4	-12V	-12 Volt Power Supply
-5	$\overline{\text{ADDR0}}$	Negative True, Address Bit 0
-6	$\overline{\text{ADDR1}}$	Negative True, Address Bit 1
-7	$\overline{\text{ADDR2}}$	Negative True, Address Bit 2
-8	$\overline{\text{ADDR3}}$	Negative True, Address Bit 3
-9	$\overline{\text{ADDR4}}$	Negative True, Address Bit 4
-10	$\overline{\text{ADDR5}}$	Negative True, Address Bit 5
-11	$\overline{\text{ADDR6}}$	Negative True, Address Bit 6
-12	$\overline{\text{ADDR7}}$	Negative True, Address Bit 7
-13	$\overline{\text{ADDR8}}$	Negative True, Address Bit 8
-14	$\overline{\text{ADDR9}}$	Negative True, Address Bit 9
-15	$\overline{\text{ADDR10}}$	Negative True, Address Bit 10
-16	$\overline{\text{ADDR11}}$	Negative True, Address Bit 11
-17	$\overline{\text{ADDR12}}$	Negative True, Address Bit 12
-18	$\overline{\text{ADDR13}}$	Negative True, Address Bit 13
-19	$\overline{\text{ADDR14}}$	Negative True, Address Bit 14
-20	$\overline{\text{ADDR15}}$	Negative True, Address Bit 15
-21	$\overline{\text{I/O}}$	Negative True, Input Output/Memory
-22	GND	Ground Common Return (Power and Signal)

Table 5.0 Connector Information (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
P1, Pin A	GND	Ground Common Return (Power and Signal)
-B		Not Used
-C	+12V	+12 volt Power Supply
-D	PWR ON	System Power On
-E	$\overline{\text{BUS0}}$	Negative True, Data Bus Bit 0
-F	$\overline{\text{BUS1}}$	Negative True, Data Bus Bit 1
-H	$\overline{\text{BUS2}}$	Negative True, Data Bus Bit 2
-J	$\overline{\text{BUS3}}$	Negative True, Data Bus Bit 3
-K	$\overline{\text{BUS4}}$	Negative True, Data Bus Bit 4
-L	$\overline{\text{BUS5}}$	Negative True, Data Bus Bit 5
-M	$\overline{\text{BUS6}}$	Negative True, Data Bus Bit 6
-N	$\overline{\text{BUS7}}$	Negative True, Data Bus Bit 7
-P	$\overline{\text{WRITE}}$	Negative True, Write/Read Type Cycle
-R		Not used
-S	$\overline{\text{WAIT}}$	Negative True, Wait Control Line
-T	PRTOR IN	Bus Controller Priority In
-U	PRTOR OUT	Bus Controller Priority Out
-V		Not Used
-W	$\overline{\text{BUSY}}$	Negative True, Bus Currently Busy (Not Available)
-X		Not Used
-Y	$\overline{\text{REQ}}$	Negative True, Request (Bus Data Currently Valid)
-Z		Not Used

3.0 FUNCTIONAL DESCRIPTION. Refer to the block diagram (figure 1), schematic diagram (figure 2), timing diagrams (figures 3, 4, and 5), component location diagram (figure 6), and parts list (02640-60064) located in the appendix.

The +2K Memory Module consists of 2K of RAM, an address comparator, timing and control logic, multiplexing logic, refresh logic, and bus request logic circuits.

3.1 RAM.

3.1.1 The memory portion of the PCA is comprised of four LSI RAM chips, each organized 4K by 1-bit. The chips are arranged into an array of 4K by 4. The 2K by 8-bit organization of the PCA is achieved by making two read or write cycles per memory request. The RAM chips have TTL-compatible inputs and outputs (except for CE CLOCK).

3.1.2 A read operation on the memory array requires that internal signal

R/$\overline{W}$ be high and that all address inputs be stable when CE CLOCK (Chip Enable Clock) is asserted (ground to +12 volts). Internal signal Data Out (DO), is then routed to the two read registers (U15 and U16 in the multiplexing logic), which store data from the two 4-bit read operations. (Refer to figure 3 for read timing explanations.)

A write is the same as a memory read, except that R/$\overline{W}$ is held low.

Data In ($\overline{DI}$) comes from the input multiplexer (U24) during two 4-bit write operations. (Refer to figure 4 for write timing explanations.)

3.2 ADDRESS COMPARATOR.

3.2.1 The address comparator logic is comprised of a comparator (U38 and U39) and an address configuration jumper network (W1). The jumpers are used to specify which 2K partition in the 64K memory space the +2K Memory PCA will represent.

3.2.2 The terminal bus provides 16 address inputs ($\overline{ADDR0}$ through $\overline{ADDR15}$)

and two control bits ($\overline{I/O}$ and $\overline{WRITE}$) which define module addressing.

The most significant five bits (ADDR15, ADDR14, ADDR13, ADDR12, and ADDR11) are routed to the address comparator to determine if the memory PCA is configured for the selected address. The remaining 11 address bits go to the memory chips through inverters (U31 and U32) to preserve terminal bus loading rules. Other bus control inputs determine if a memory operation is requested and distinguish whether it is a read or write operation.

3.2.2.1 The memory module uses the WRITE signal to determine read or write access and uses I/O to inhibit a memory access during input/output operations. Another control input, REQ, is used and is equivalent to an execute signal, which starts the memory access cycle.

3.2.2.2 The final address bit to the memory chips, LSB ADDRESS (U213, Pin 9), determines which half of the 8-bit character is being accessed. When the address comparator logic indicates an equal condition and I/O is high, Module Accessed (U311, Pin 6) is high as soon as REQ goes low.

3.3 TIMING AND CONTROL LOGIC.

3.3.1 The timing and control logic is an interface between the terminal bus and the memories. The control logic portion of the PCA accepts address compare (ADDR =) information and bus control inputs to determine if the module is being accessed. If it is, this block generates all timing and control signals necessary to access the memory chips and perform the multiplexing operation.

3.3.2 When the address comparator determines that the +2K Memory PCA is selected for a Module Accessed, the state counter (U211) begins a sequence which generates the timing for two memory chip read or writes and the signals to control the multiplexing. (Refer to figures 3 and 4 for typical read and write cycle timing information.) The refresh logic also uses this block to perform pseudo read cycles.

3.3.2.1 The state counter (U211) is a presetable binary counter which is in the reset condition until a memory cycle is started by $\overline{REQ}$ and Module Select being true. Two accesses to the 4K by 4 array require a count, a preset, an additional count, and a hold sequence (States 0, 1, 2, 7, 8, 9, and 10). Each count state represents about 203 nanoseconds (from SYS CLK of 4.915 MHz) and the states of the counter are decoded to derive the necessary control signals.

3.3.2.2 The timing and control logic outputs go to the chip clock driver (U23) and to the state counter to control its sequencing. The LSB Address flip-flop is controlled by the state counter; it is false during the first half of a memory module access and true on the second half. The read registers (U15 and U16) receive LSB CLK (U311, Pin 11) and MSB CLK (U17, Pin 6) signals which clock $\overline{DI}$ into them during read operations. Two other signals are generated by the timing and control logic; $R/\overline{W}$ (U27, Pin 8) tells the memory to read or write and READ (U311, Pin 8) enables the outputs of the read registers to be gated to the terminal bus during a memory read. While the memory cycle is in progress, $\overline{WAIT}$ is held true (low). When the cycle is completed, $\overline{WAIT}$ goes false (high) and the state counter is halted (State 10). When $\overline{REQ}$ goes false (high), the 2K Memory PCA is then ready for another memory request.

3.4 MULTIPLEXING LOGIC.

3.4.1 The multiplexing logic consists of an 8-to-4 multiplexer chip (U24) and two read registers (U15 and U16). The outputs of the registers are connected to the terminal bus through bus drivers, U25 and U26.

3.4.2 When a write cycle is initiated, data and address on the data bus are stable and the multiplexer gates the least significant four bits ($\overline{BUS0}$, $\overline{BUS1}$, $\overline{BUS2}$, and $\overline{BUS3}$) to $\overline{DI}$ in the memory chips. When the first memory write operation is complete, the LSB Address flip-flop changes and the most significant four bits ($\overline{BUS4}$ through $\overline{BUS7}$) are gated to the chips. This puts the least significant four bits in even locations in memory and the most significant bits in odd locations.

When a read access is performed, the data bus bits out of the memory are strobed into two 4-bit read registers (U15 and U16), with the least significant four bits ($\overline{BUS3}$, $\overline{BUS2}$, $\overline{BUS1}$, and $\overline{BUS0}$) being strobed first. During a read, the bus drivers (U25 and U26) are enabled and place the data in the read registers onto the terminal data bus.

3.5 REFRESH LOGIC.

3.5.1 The refresh logic consists of a refresh address counter with bus drivers, and portions of the timing and control logic.

Dynamic MOS memories require periodic pseudo memory read cycles so that the internal data storage mechanisms do not lose data. A memory refresh cycle is initiated every 2 milliseconds and lasts approximately 45.2 microseconds. All 64 refresh addresses are accessed in sequence, while the memory module has control of the terminal bus. (Refer to figure 5 for refresh cycle timing explanations.)

3.5.2 The refresh is accomplished by performing 32 memory cycles of two read operations. The least six significant bits are cycled by gating the refresh address counter (five) bits onto the address bus and back into the memory chips and by toggling the LSB address bit during pseudo read cycles.

3.5.2.1 The timing and control logic is used to perform the pseudo read cycles to the memory chips. At the end of each pseudo read cycle, the refresh address counter (U37) is incremented and the timing and control logic goes to State 0 and begins a new read cycle.

3.5.2.2 When the counter completes its count of 32, the Refresh Cycle Complete flip-flop at U18, Pin 9 is set; the bus request logic then releases the terminal bus, and the refresh cycle ends.

3.6 BUS REQUEST LOGIC.

3.6.1 The bus request logic consists of four J-K flip-flops, gates and an astable (U112). The astable (U112) is used as a precision timer in the free run mode. The frequency is 500 Hz, giving a 2-millisecond refresh interval (550 Hz +/-50 Hz).

3.6.2 The astable clocks the first flip-flop signal REFRESH REQUEST, (U110, Pin 6) and a bus request operation is started. The second flip-flop (U110, Pin 8) buffers the REFRESH REQUEST signal and synchronizes it with the system clock. When the bus is available ($\overline{BUSY}$ is high) and no other module is requesting the terminal bus, the 2K Memory PCA makes $\overline{BUSY}$ low and takes control of the terminal bus. An internal Bus Available (BUS AVAIL) signal at U19, Pin 8 goes true, signaling the start of the refresh cycle. The Bus Available signal gates the refresh counter (U37) outputs onto the terminal address bus.

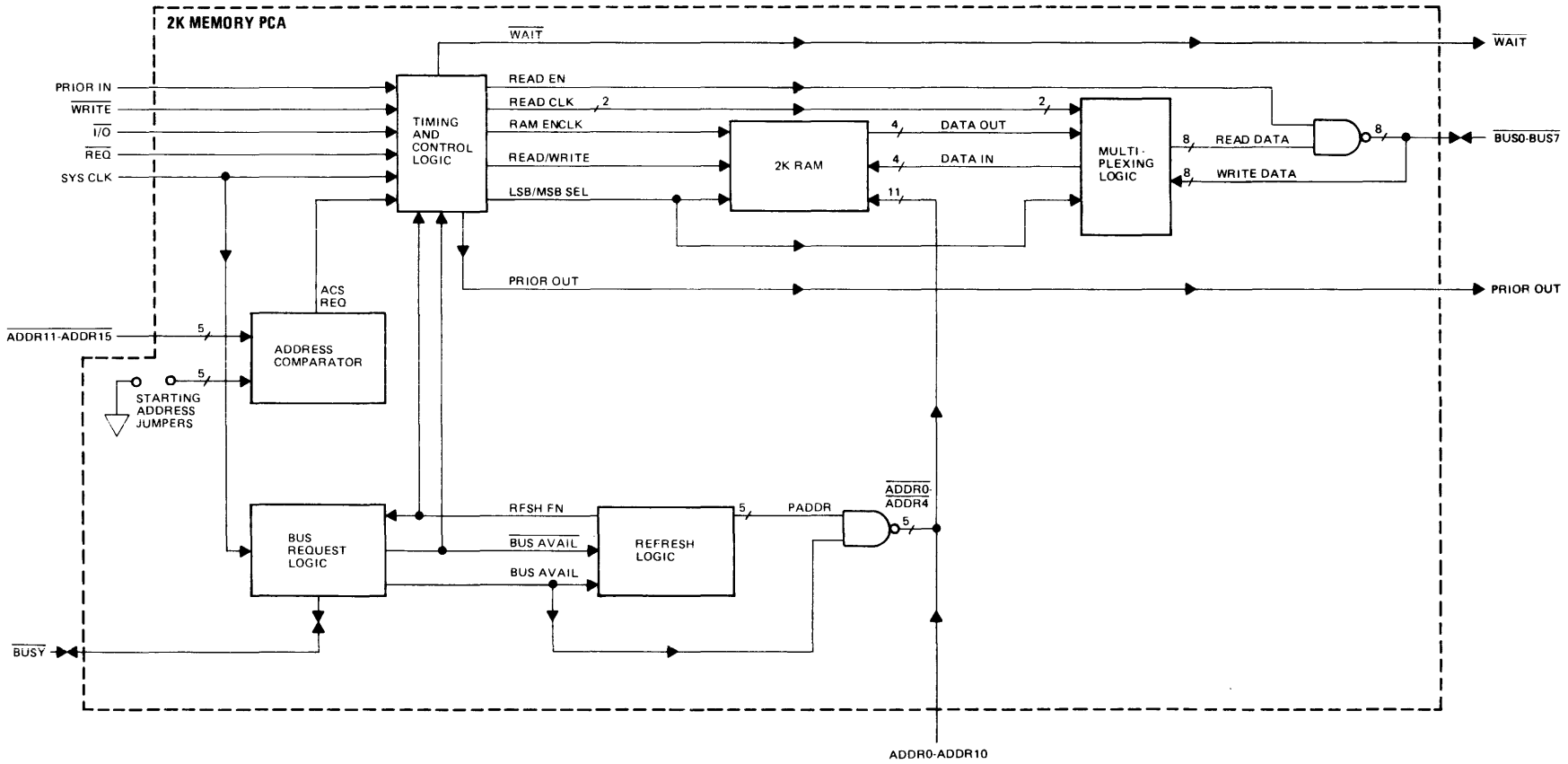


Figure 1
+2K Memory Block Diagram
AUG-01-76 13255-91064

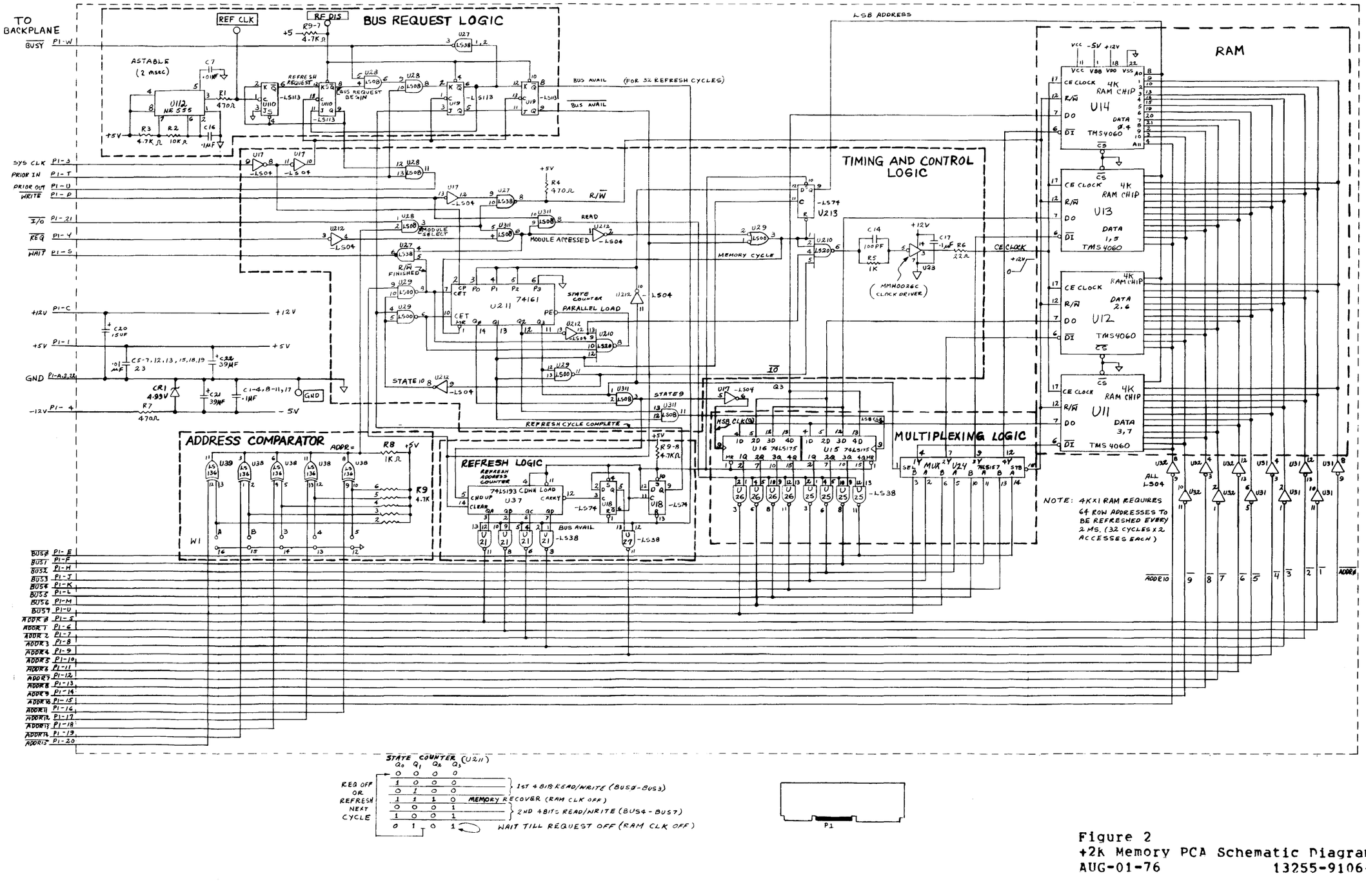


Figure 2
+2k Memory PCA Schematic Diagram
AUG-01-76 13255-91064

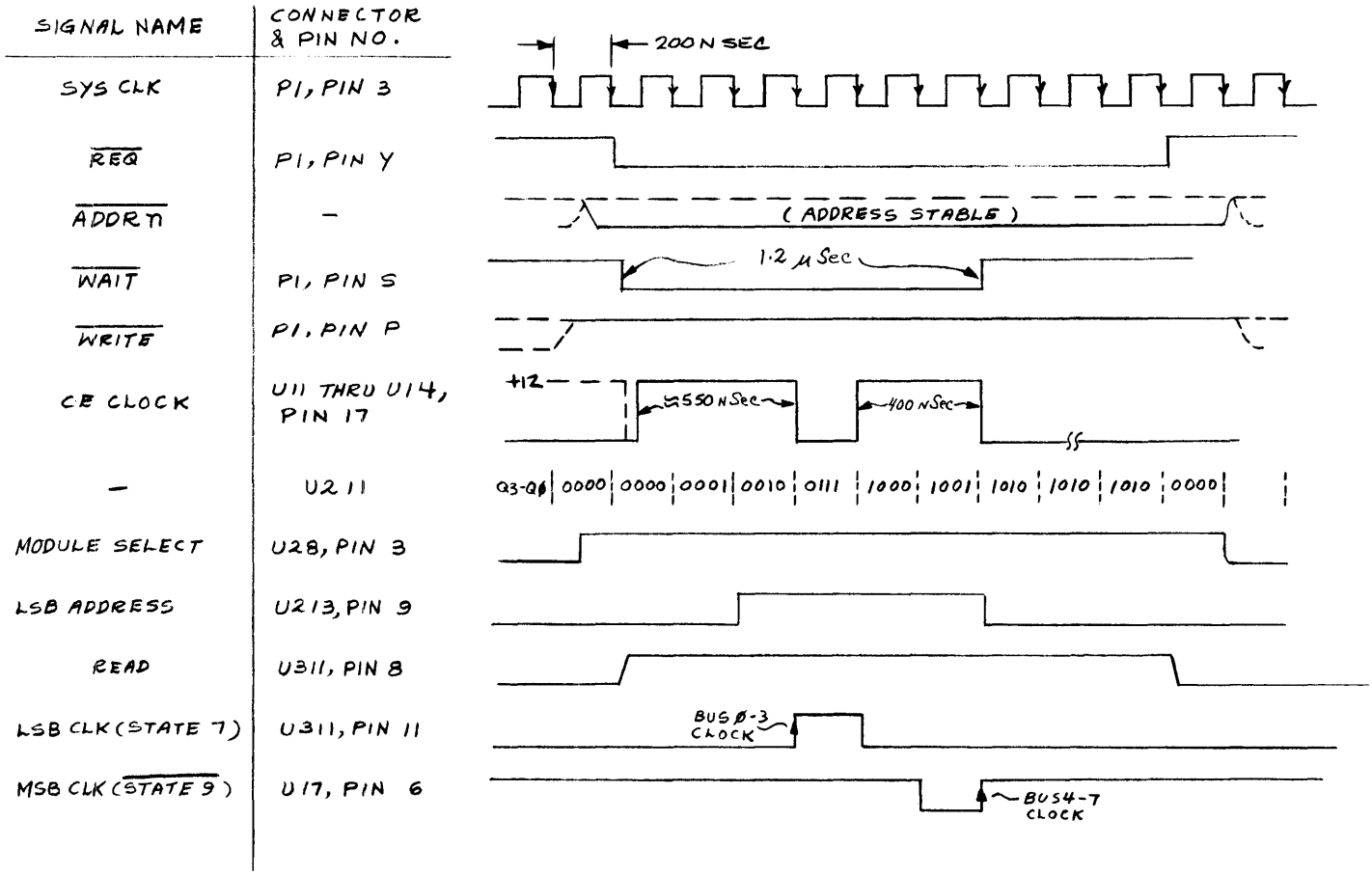


Figure 3
+2K Memory Read Timing Diagram
AUG-01-76 13255-91064

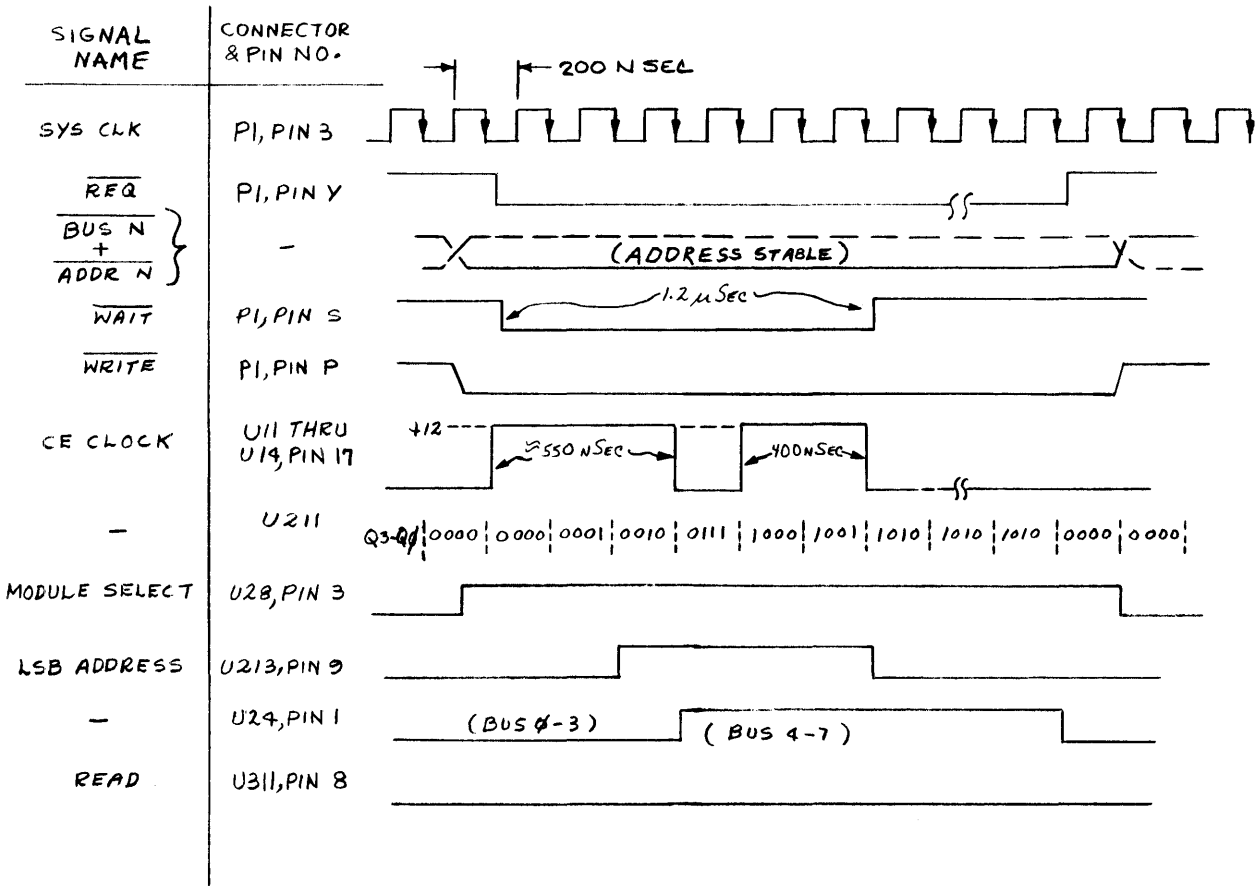


Figure 4
+2K Memory Write Timing Diagram
AUG-01-76 13255-91064

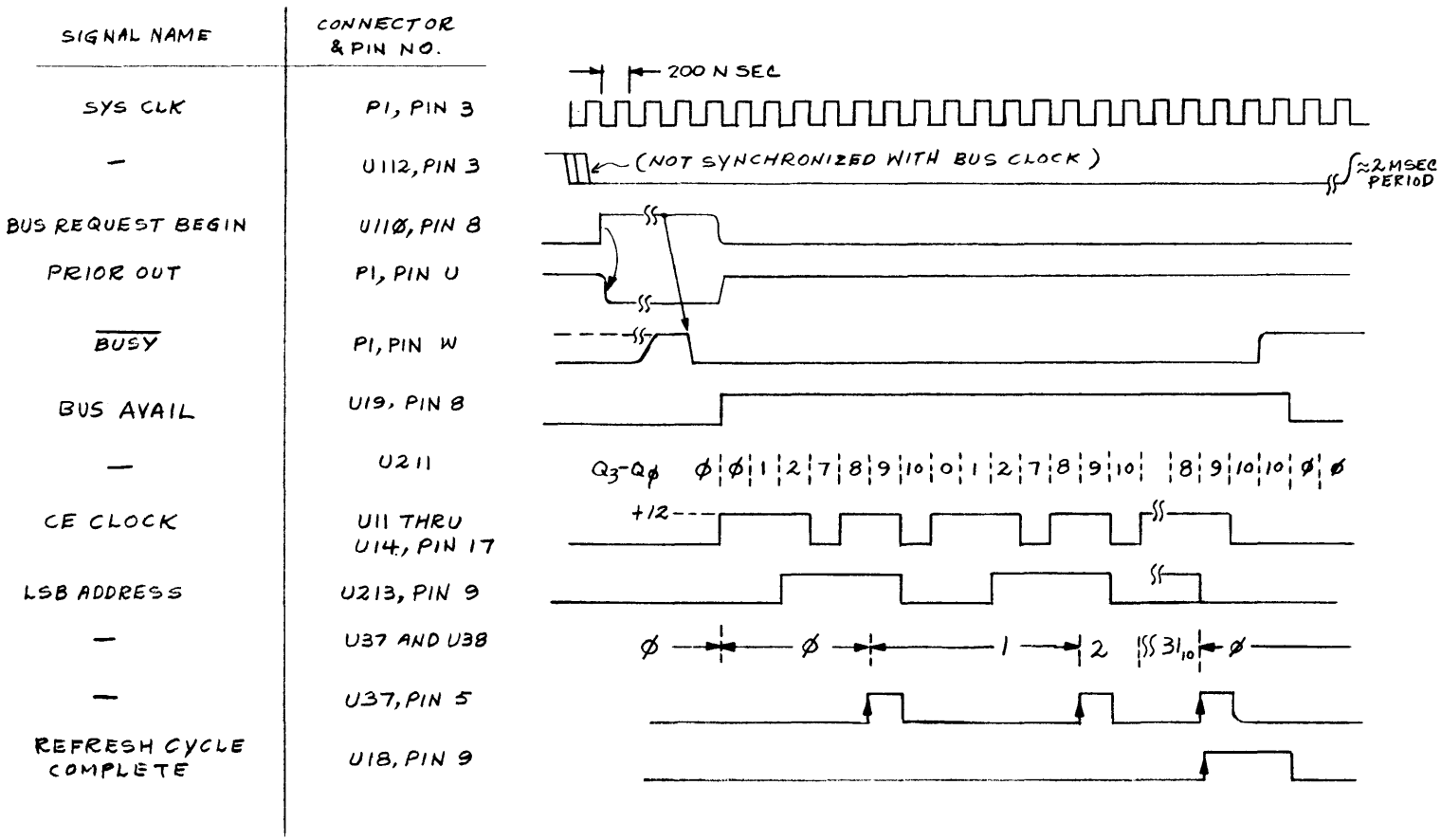


Figure 5
+2K Memory Refresh Timing Diagram
AUG-01-76 13255-91064

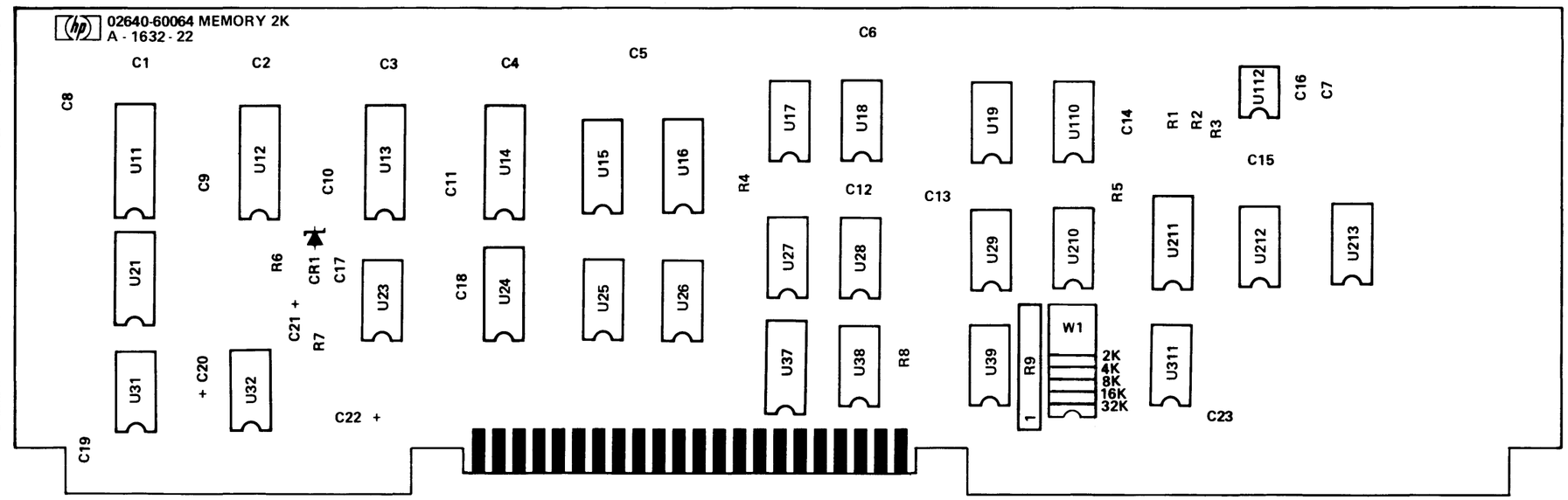


Figure 6
+2K Memory PCA Component Location Diagram
AUG-01-76 13255-91064

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
	02640-60064	1	MEMORY ASSEMBLY, 2K DATE CODE: A-1632-22 REVISION DATE: 08-04-76	28480	02640-60064
C1	0150-0121	9	CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
C2	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
C3	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
C4	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
C5	0160-2055	9	CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C6	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C7	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C8	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
C9	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
C10	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
C11	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
C12	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C13	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C14	0160-2204	1	CAPACITOR-FXD 100PF +-5% 300WVDC MICA	28480	0160-2204
C15	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C16	0180-1743	1	CAPACITOR-FXD .1UF+-10% 35VDC TA	56289	150D104X9035A2
C17	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
C18	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C19	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C20	0180-1746	1	CAPACITOR-FXD 150UF+-10% 20VDC TA	56289	150D156X9020B2
C21	0180-0393	2	CAPACITOR-FXD 39UF+-10% 10VDC TA	56289	150D396X9010B2
C22	0180-0393		CAPACITOR-FXD 39UF+-10% 10VDC TA	56289	150D396X9010B2
C23	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
CR1	1902-3092	1	DIODE-ZNR 4.99V 2% DO-7 PD=.4W TC=-.012%	04713	SZ 10939-96
E1	0360-0124	4	TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
E2	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
E3	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
E4	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
R1	0683-4715	3	RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R2	0757-0442	1	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R3	0757-0200	1	RESISTOR 5.62K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5621-F
R4	0683-4715		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R5	0683-1025	2	RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R6	0683-2205	1	RESISTOR 22 5% .25W FC TC=-400/+500	01121	CB2205
R7	0683-4715		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R8	0683-1025		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R9	1810-0125	1	NETWORK-RES 8-PIN-SIP .125-PIN-SPCG	11236	750
U11	5080-9785	4	4K RAM 22-PIN HR	28480	5080-9785
U12	5080-9785		4K RAM 22-PIN HR	28480	5080-9785
U13	5080-9785		4K RAM 22-PIN HR	28480	5080-9785
U14	5080-9785		4K RAM 22-PIN HR	28480	5080-9785
U15	1820-1195	2	IC-DIGITAL SN74LS175N TTL LS QUAD	01295	SN74LS175N
U16	1820-1195		IC-DIGITAL SN74LS175N TTL LS QUAD	01295	SN74LS175N
U17	1820-1199	4	IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
U18	1820-1112	2	IC-DIGITAL SN74LS74N TTL LS DUAL	01295	SN74LS74N
U19	1820-1213	2	IC-DIGITAL SN74LS113N TTL LS DUAL	01295	SN74LS113N
U21	1820-1209	4	IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U23	1820-1288	1	IC-DIGITAL MMH0026CL TTL/MOS 1 CLOCK	04713	MMH0026CL
U24	1820-1470	1	IC-DIGITAL SN74LS157N TTL LS QUAD 2	01295	SN74LS157N
U25	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U26	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U27	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U28	1820-1201	2	IC-DIGITAL SN74LS08N TTL LS QUAD 2 AND	01295	SN74LS08N
U29	1820-1197	1	IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
U31	1820-1199		IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
U32	1820-1199		IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
U37	1820-1194	1	IC-DIGITAL SN74LS193N TTL LS BIN	01295	SN74LS193N
U38	1820-1215	2	IC-DIGITAL SN74LS136N TTL LS QUAD 2	01295	SN74LS136N
U39	1820-1215		IC-DIGITAL SN74LS136N TTL LS QUAD 2	01295	SN74LS136N
U110	1820-1213		IC-DIGITAL SN74LS113N TTL LS DUAL	01295	SN74LS113N
U112	1826-0373	1	IC-LINEAR		
U210	1820-1204	1	IC-DIGITAL SN74LS20N TTL LS DUAL 4 NAND	01295	SN74LS20N
U211	1820-0716	1	IC-DIGITAL SN74161N TTL BIN SYNCHRO	01295	SN74161N
U212	1820-1199		IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
U213	1820-1112		IC-DIGITAL SN74LS74N TTL LS DUAL	01295	SN74LS74N
U311	1820-1201		IC-DIGITAL SN74LS08N TTL LS QUAD 2 AND	01295	SN74LS08N

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
			MEMORY ASSEMBLY, 2K CONT'D.		
A1	1200-0482	1	SOCKET-IC 16-CONT DIP-SLDR	91506	516-AG110
W1A	1258-0124	5	PIN-PROGRAMMING JUMPER;.30 CONTACT	91506	8136-475G1
W1B	1258-0124		PIN-PROGRAMMING JUMPER;.30 CONTACT	91506	8136-475G1
W1C	1258-0124		PIN-PROGRAMMING JUMPER;.30 CONTACT	91506	8136-475G1
W1D	1258-0124		PIN-PROGRAMMING JUMPER;.30 CONTACT	91506	8136-475G1
W1E	1258-0124		PIN-PROGRAMMING JUMPER;.30 CONTACT	91506	8136-475G1