HP 13255

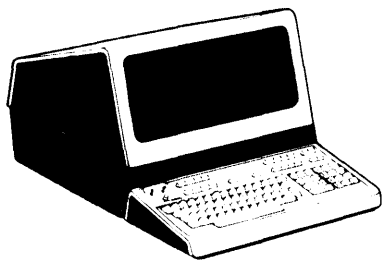
GENERAL PURPOSE ASYNCHRONOUS DATA COMM MODULE

Manual Part No. 13255-91143

REVISED

APR-20-78

DATA TERMINAL
TECHNICAL INFORMATION



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1.0 INTRODUCTION.

The General Purpose Asynchronous Data Communications Module provides a general purpose EIA RS232C or 20 mA dc current loop link from the terminal to an external device. The GP Async Data Comm PCA transmits and receives bit serial data to and from the external device through an interface cable assembly, provides parallel-to-serial and serial-to-parallel conversion, and transmits and receives bit parallel data to and from the terminal through the Backplane Assembly (data bus).

2.0 OPERATING PARAMETERS.

A summary of operating parameters for the GP Async Data Comm Module is contained in tables 1.0 through 6.5.

Table 1.0 Physical Parameters

Part Number	Nomenclature	Size (L x W x D) +/-0.100 Inches	Weight (Pounds)
02640-60143	GP Async Data Comm PCA	12.9 x 4.0 x 0.6	0.50
Number of Backplane Slots Required: 1			

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NOTE: This document is part of the 264XX DATA TERMINAL product series Technical Information Package (HP 13255).

1.0 INTRODUCTION.

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Number of Backplane Slots Required: 1			

Table 2.0 Reliability and Environmental Information

Environmental: (X) HP Class B ( ) Other:
Restrictions: Type tested at product level
Failure Rate: 1.502 (percent per 1000 hours)

Table 3.0 Power Supply and Clock Requirements - Measured
(At +/-5% Unless Otherwise Specified)

+5 Volt Supply	+12 Volt Supply	-12 Volt Supply	-42 Volt Supply
@ 300 mA	@ 40 mA	@ 20 mA	@ mA
			NOT APPLICABLE

115 volts ac	220 volts ac
@ A	@ A
NOT APPLICABLE	NOT APPLICABLE

Clock Frequency: 4.915 MHz

Table 4.0 Switch Definitions

PCA Designation	Function
A11,A10,A9,A4	Module Address Selection (see section 4.0)
FC0 thru FC7	Firmware Control Word - Function depends on firmware application
CBE	Custom Baud Rate Enable Closed - The custom baud rate generator is enabled when the baud rate switch is in the EXT position Open - The custom baud rate generator is disabled
B0 thru B11	Custom Baud Rate Selection (see section 4.1)
S0,S1,S2	Split Baud Rate Selection (see section 4.2)
134	134.5 Baud Closed - Enable 134.5 baud and 6-bit data word when baud rate switch is in 150 position Open - Disable 134.5 baud
2SB	Two Stop Bits Closed - Transmit and receive data with two stop bits at all baud rates Open - Transmit and receive data with one stop bit at all baud rates except 110 (two stop bits)

Table 4.0 Switch Definitions (Cont'd.)

PCA Designation	Function
NOSB	Inhibit Secondary Channel Carrier Detect Closed - Inhibit RS232 line SB Open - No effect
THE	Transmit Handshake Enable Closed - Enable transmit handshake circuit Open - Disable transmit handshake circuit
RHE	Receive Handshake Enable Closed - Enable receive handshake circuit Open - Disable receive handshake circuit
IAT	Inhibit $\overline{\text{ATN}}$ Closed - Disable Data Comm Interrupt from this module Open - Enable Data Comm Interrupt from this module
ATN2	Enable $\overline{\text{ATN2}}$ Closed - Direct interrupts to $\overline{\text{ATN2}}$ instead of $\overline{\text{ATN}}$ and enable interrupt poll response on $\overline{\text{BUS6}}$ Open - Direct interrupts to $\overline{\text{ATN}}$ and inhibit interrupt poll responses

Table 5.0 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P1, Pin 1	+5V	+5 Volt Power Supply
-2	GND	Ground Common Return (Power and Signal)
-3	SYS CLK	4.915 MHz System Clock
-4	-12V	-12 Volt Power Supply
-5	$\overline{\text{ADDR0}}$	Negative True, Address Bit 0
-6		Not Used
-7	$\overline{\text{ADDR2}}$	Negative True, Address Bit 2
-8	$\overline{\text{ADDR3}}$	Negative True, Address Bit 3
-9	$\overline{\text{ADDR4}}$	Negative True, Address Bit 4
-10	$\overline{\text{ADDR5}}$	Negative True, Address Bit 5
-11	$\overline{\text{ADDR6}}$	Negative True, Address Bit 6
-12		Not Used
-13		
-14	$\overline{\text{ADDR9}}$	Negative True, Address Bit 9
-15	$\overline{\text{ADDR10}}$	Negative True, Address Bit 10
-16	$\overline{\text{ADDR11}}$	Negative True, Address Bit 11
Pin -17 through Pin -20		Not Used
-21	$\overline{\text{I/O}}$	Negative True, Input Output/Memory
-22	GND	Ground Common Return (Power and Signal)

Table 5.0 Connector Information (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
P1, Pin A	GND	Ground Common Return (Power and Signal)
-B		Not Used
-C	+12V	
-D	PWR ON	System Power On
-E	$\overline{\text{BUS0}}$	Negative True, Data Bus Bit 0
-F	$\overline{\text{BUS1}}$	Negative True, Data Bus Bit 1
-H	$\overline{\text{BUS2}}$	Negative True, Data Bus Bit 2
-J	$\overline{\text{BUS3}}$	Negative True, Data Bus Bit 3
-K	$\overline{\text{BUS4}}$	Negative True, Data Bus Bit 4
-L	$\overline{\text{BUS5}}$	Negative True, Data Bus Bit 5
-M	$\overline{\text{BUS6}}$	Negative True, Data Bus Bit 6
-N	$\overline{\text{BUS7}}$	Negative True, Data Bus Bit 7
-P	$\overline{\text{WRITE}}$	Negative True, Write/Read Type Cycle
-R		}
		} Not Used
-S		}
-T	PRIOR IN	Bus Controller Priority In
-U	PRIOR OUT	Bus Controller Priority Out
-V		}
		}
-W		} Not used
		}
-X		}
-Y	$\overline{\text{REQ}}$	Negative True, Request (Bus Data Currently Valid)
-Z	$\overline{\text{ATN}}$	Negative True, Data Comm Interrupt Request

Table 5.1 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P2, Pin 1	$\overline{\text{ENCL}}$	Negative True, Current Loop Enable
- 2	$\overline{\text{INI}}$	Negative True, Invert Current Loop Received Data
- 3	CL+12	Power Source for Current Loop Active Receiver
- 4	CL+	Current Loop Receiver Positive Input
- 5	CL-	Current Loop Receiver Negative Input
- 6	CLA	Current Loop Transmitter Current Sourcing Terminal
- 7	CLP	Current Loop Transmitter Current Sinking Terminal
- 8	$\overline{\text{INO}}$	Negative True, Invert Current Loop Transmitted Data
- 9	PON	Power On Clear
-10	$\overline{\text{ISB}}$	Negative True, Invert the Sense of SB
-11	XECL	Programmable Control Signal
-12	TTYIN	Teletype Current Loop Receiver Input
-13	+5V	+5 Volt Supply
-14		Not Used
-15	TEST	9650 Test Point

Table 5.1 Connector Information (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
P2, Pin A	AA	Frame Ground
-B	BA	Transmitted Data Out
-C	BB	Received Data In
-D	CA	Request to Send
-E	CB	Clear to Send
-F	CC	Data Set Ready
-H	GND	Signal Ground (AB)
-J	CF	Carrier Received
-K	X8 OUT	Clock of 8 X the Transmit Baud Rate
-L	X16 OUT	Clock of 16 X the Transmit Baud Rate
-M	SCA	Secondary Channel Request To Send
-N	SCF	Secondary Channel Carrier Detect
-P	CD	Data Terminal Ready
-R	CH	Rate Select
-S	X16 IN	Clock of 16 X the Receive Baud Rate

Table 6.0 Module Bus Pin Assignments

Function Performed: Output Data Character for Transmission

Poll Bit: Not Applicable

Module Address: (ADDR 11,10,9,4) = (A11,A10,A9,A4)
Switch Selectable (0001) = Data Comm
(0101) = Printer

Function Specifier: ADDR 5 = 1
ADDR 6 = 1

Data Bus Bit Interpretation:

B7 Data Output Bit 7

B6 Data Output Bit 6

B5 Data Output Bit 5

B4 Data Output Bit 4

B3 Data Output Bit 3

B2 Data Output Bit 2

B1 Data Output Bit 1

B0 Data Output Bit 0

Value	Bus Signal
X	ADDR 15
X	ADDR 14
X	ADDR 13
X	ADDR 12
A11	ADDR 11
A10	ADDR 10
A9	ADDR 9
X	ADDR 8
X	ADDR 7
1	ADDR 6
1	ADDR 5
A4	ADDR 4
X	ADDR 3
X	ADDR 2
X	ADDR 1
X	ADDR 0
B7	BUS 7
B6	BUS 6
B5	BUS 5
B4	BUS 4
B3	BUS 3
B2	BUS 2
B1	BUS 1
B0	BUS 0

1=Logical 1=Bus Low
0=Logical 0=Bus High
X=Don't Care

Table 6.1 Module Bus Pin Assignments

Function Performed: Read Firmware Control Word (FC Switches)

Poll Bit: Not Applicable

Module Address: (ADDR 11,10,9,4) = (A11,A10,A9,A4)
Switch Selectable (0001) = Data Comm
(0101) = Printer

Function Specifier: ADDR 5 = 0
ADDR 6 = 1

Data Bus Bit Interpretation:

B7 Switch FC7
0 = Switch Closed
1 = Switch Open

B6 Switch FC6
0 = Switch Closed
1 = Switch Open

B5 Switch FC5
0 = Switch Closed
1 = Switch Open

B4 Switch FC4
0 = Switch Closed
1 = Switch Open

B3 Switch FC3
0 = Switch Closed
1 = Switch Open

B2 Switch FC2
0 = Switch Closed
1 = Switch Open

B1 Switch FC1
0 = Switch Closed
1 = Switch Open

B0 Switch FC0
0 = Switch Closed
1 = Switch Open

Value	Bus Signal
X	ADDR 15
X	ADDR 14
X	ADDR 13
X	ADDR 12
A11	ADDR 11
A10	ADDR 10
A9	ADDR 9
X	ADDR 8
X	ADDR 7
1	ADDR 6
0	ADDR 5
A4	ADDR 4
X	ADDR 3
X	ADDR 2
X	ADDR 1
X	ADDR 0
B7	BUS 7
B6	BUS 6
B5	BUS 5
B4	BUS 4
B3	BUS 3
B2	BUS 2
B1	BUS 1
B0	BUS 0

1=Logical 1=Bus Low
0=Logical 0=Bus High
X=Don't Care

Table 6.2 Module Bus Pin Assignments

Function Performed: Input Module Status Byte

Poll Bit: Bit 6 (When ATN2 switch is closed)

Module Address: (ADDR 11,10,9,4) = (A11,A10,A9,A4)
Switch Selectable (0001) = Data Comm
(0101) = Printer

Function Specifier: ADDR 5 = 1
ADDR 6 = 0
A0 = 0 Read Standard Status
A0 = 1 Read Alternate Status

Data Bus Bit Interpretation:
Alternate status is the same as the standard status unless noted otherwise

B7 Not Used — (Alternate) 0 = CC on, 1 = CC off

B6 0 = SB On, 1 = SB Off

B5 0 = CB On, 1 = CB Off

B4 0 = CF On, 1 = CF Off

B3 0 = No Parity Error, 1 = Parity Error

B2 0 = No Overrun Error, 1 = Overrun Error

B1 0 = Transmit Holding Register Full, 1 = Transmit Holding Register Empty — (Alternate) 0 = Transmission in Progress, 1 = Transmission Complete

B0 0 = Receiver Register Empty, 1 = Receiver Register Full

Value	Bus Signal
X	ADDR 15
X	ADDR 14
X	ADDR 13
X	ADDR 12
A11	ADDR 11
A10	ADDR 10
A9	ADDR 9
X	ADDR 8
X	ADDR 7
0	ADDR 6
1	ADDR 5
A4	ADDR 4
X	ADDR 3
X	ADDR 2
X	ADDR 1
A0	ADDR 0
B7	BUS 7
B6	BUS 6
B5	BUS 5
B4	BUS 4
B3	BUS 3
B2	BUS 2
B1	BUS 1
B0	BUS 0

1=Logical 1=Bus Low
0=Logical 0=Bus High
X=Don't Care

Table 6.3 Module Bus Pin Assignments

Function Performed: Read Received Data Character

Poll Bit: Not Applicable

Module Address: (ADDR 11,10,9,4) = (A11,A10,A9,A4)
Switch Selectable (0001) = Data Comm
(0101) = Printer

Function Specifier: ADDR 5 = 0
ADDR 6 = 0

Data Bus Bit Interpretation:

B7 Data Input Bit 7

B6 Data Input Bit 6

B5 Data Input Bit 5

B4 Data Input Bit 4

B3 Data Input Bit 3

B2 Data Input Bit 2

B1 Data Input Bit 1

B0 Data Input Bit 0

Value	Bus Signal
X	ADDR 15
X	ADDR 14
X	ADDR 13
X	ADDR 12
A11	ADDR 11
A10	ADDR 10
A9	ADDR 9
X	ADDR 8
X	ADDR 7
0	ADDR 6
0	ADDR 5
A4	ADDR 4
X	ADDR 3
X	ADDR 2
X	ADDR 1
X	ADDR 0
B7	BUS 7
B6	BUS 6
B5	BUS 5
B4	BUS 4
B3	BUS 3
B2	BUS 2
B1	BUS 1
B0	BUS 0

1=Logical 1=Bus Low
0=Logical 0=Bus High
X=Don't Care

Table 6.4 Module Bus Pin Assignments

Function Performed: Output Control Register Bits

Poll Bit: Not Applicable

Module Address: (ADDR 11,10,9,4) = (A11,A10,A9,A4)
Switch Selectable (0001) = Data Comm
(0101) = Printer

Function Specifier: ADDR 5 = 0
ADDR 6 = 1

Data Bus Bit Interpretation:

B7
0 = CH On
1 = CH Off

B6
0 = No Break
1 = Break

B5
0 = Enable Parity
1 = Inhibit Parity

B4
0 = Odd Parity
1 = Even Parity

Value	Bus Signal
X	ADDR 15
X	ADDR 14
X	ADDR 13
X	ADDR 12
A11	ADDR 11
A10	ADDR 10
A9	ADDR 9
X	ADDR 8
X	ADDR 7
1	ADDR 6
0	ADDR 5
A4	ADDR 4
X	ADDR 3
X	ADDR 2
X	ADDR 1
X	ADDR 0
B7	BUS 7
B6	BUS 6
B5	BUS 5
B4	BUS 4
B3	BUS 3
B2	BUS 2
B1	BUS 1
B0	BUS 0

1=Logical 1=Bus Low
0=Logical 0=Bus High
X=Don't Care

RECEIVE BAUD RATE

	Ext Clk	110	150	300	1200	2400	4800	9600
B3	0	0	0	0	1	1	1	1
B2	0	0	1	1	0	0	1	1
B1	0	1	0	1	0	1	0	1

B0
0 = CA on
1 = CA off

Table 6.5 Module Bus Pin Assignments

Function Performed:	Value	Bus Signal
Input instruction to Set/Reset Data Terminal Ready (CD) and Set/Reset External Control signal (XECL)	X	ADDR 15
	X	ADDR 14
Poll Bit: Not Applicable	X	ADDR 13
	X	ADDR 12
Module Address: (ADDR 11,10,9,4) = (A11,A10,A9,A4)	A11	ADDR 11
Switch Selectable (0001) = Data Comm	A10	ADDR 10
(0101) = Printer	A9	ADDR 9
	X	ADDR 8
Function Specifier: ADDR 5 = 1	X	ADDR 7
ADDR 6 = 1	1	ADDR 6
A2 = 0, XECL = Low	1	ADDR 5
A2 = 1, XECL = High	A4	ADDR 4
	A3	ADDR 3
A3 = 0, CD On	A2	ADDR 2
A3 = 1, CD Off	X	ADDR 1
	X	ADDR 0
Data Bus Bit Interpretation: Not Applicable	B7	BUS 7
	B6	BUS 6
	B5	BUS 5
	B4	BUS 4
	B3	BUS 3
	B2	BUS 2
	B1	BUS 1
	B0	BUS 0
	1=Logical 1=Bus Low	
	0=Logical 0=Bus High	
	X=Don't Care	

3.0 FUNCTIONAL DESCRIPTION. Refer to the block diagram (figure 1), schematic diagram (figure 2), component location diagram (figure 3), current loop configurations (figure 4), and parts list (02640-60143) located in the appendix.

The functional description of this module is detailed in blocks as shown on the block diagram.

3.1 UART. The UART is an MOS/LSI device used for interfacing a serial asynchronous data path to a parallel data path. The baud rate, number of stop bits, and parity configuration of the received and transmitted serial characters can be programmed. (For details of the UART, consult Western Digital's TR1602B specification sheet.)

3.1.1 Transmitted and received characters can have 6, 7, or 8 data bits (excluding parity). All characters have one start bit. Characters have one stop bit unless 110 baud is selected or the 2SB Switch is closed, in which case two stop bits are used. Six or seven-bit data words can have even or odd parity. Eight-bit data words have no parity.

3.1.2 When the 134 Switch is closed and control register bits 3, 2, and 1 are "010", then 134.5 baud, six data bits, one start bit, and one stop bit are selected.

3.2 I/O INSTRUCTION DECODER.

3.2.1 The I/O instruction decoder is a circuit which decodes terminal data bus signals into hardware control signals on the PCA. It consists of a module address decoder (U16) and a 3-to-8 decoder (U46). The module address decoder is composed of four exclusive OR gates which can be programmed with switches. When the proper module address is present on $\overline{\text{ADDR11}}$, $\overline{\text{ADDR10}}$, $\overline{\text{ADDR9}}$, and $\overline{\text{ADDR4}}$, an enable signal is provided to the 3-to-8 decoder.

3.2.2 The 3-to-8 decoder provides control signals to the other functional blocks. Address lines $\overline{ADDR0}$, $\overline{ADDR2}$, $\overline{ADDR3}$, $\overline{ADDR5}$, $\overline{ADDR6}$, and $\overline{WRITE}$ and $\overline{I/O}$ are decoded and strobed by $\overline{REQ}$ to realize control pulses. The following control signals are activated as shown whenever the proper module address is selected.

$\overline{I/O}$	$\overline{WRITE}$	$\overline{ADDR0}$	$\overline{ADDR2}$	$\overline{ADDR3}$	$\overline{ADDR5}$	$\overline{ADDR6}$	$\overline{REQ}$	
0	0	X	X	X	1	0	+	Load control register from data bus.
0	0	X	X	X	0	0	+	Load character into transmit half of UART.
0	1	X	X	X	1	0	0	Gate firmware control word onto data bus.
0	1	1	X	X	0	1	0	Gate status word onto data bus.
0	1	0	X	X	0	1	0	Gate modified status word onto data bus.
0	1	X	X	X	1	1	0	Gate received data from UART to data bus. Reset UART's Data Ready flip-flop
0	1	X	0	X	0	0	+	Set XECL high
0	1	X	1	X	0	0	+	Set XECL low
0	1	X	X	0	0	0	+	Turn CD off
0	1	X	X	1	0	0	+	Turn CD on

X = Don't Care
+ = Rising Edge

3.2.3 The instruction decoder also recognizes interrupt polls. If the ATN2 switch is closed, an interrupt is active, and the processor does a read with $\overline{POLL}$ low, and Bit 6 on the data bus will be pulled low.

3.3 CONTROL REGISTER.

3.3.1 The control register is a 6-bit latch that contains the control state of the PCA. The control bits set the parity, baud rate, and RS232C control signals.

3.3.2 The register is composed of six D-type flip-flops (U61). Data is latched in this register from the data bus. The register's output controls the RS232C control lines and programs the UART and baud rate generator. When latched in the control register, $\overline{\text{BUS1}}$, $\overline{\text{BUS2}}$, and $\overline{\text{BUS3}}$ program the baud rate generator receive multiplexer. The control register of the UART is also loaded when U61 is loaded. $\overline{\text{BUS4}}$ and $\overline{\text{BUS5}}$, in conjunction with the 134 and 2SB Switches, control the PI, SBS, WLS2, WLS1, and EPE signal inputs to the UART.

3.4 BAUD RATE GENERATOR.

3.4.1 The baud rate generator provides the timing for data reception and control. It consists of two parts--a standard baud rate generator and a custom baud rate generator.

3.4.2 The standard baud rate generator is composed of three 4-bit binary counters (U34, U35, and U36) and associated presetting logic. The standard baud rates are derived by dividing the bus System Clock to a rate of 16 times the desired baud rate. The standard baud rates are: 110 baud (1.76 kHz), 150 baud (2.4 kHz), 300 baud (4.8 kHz), 1200 baud (19.2 kHz), 2400 baud (38.4 kHz), 4800 baud (76.8 kHz), and 9600 baud (153.6 kHz). The counter preset function is only used when 110 or 134.5 baud is selected.

The select inputs of the receive baud rate multiplexer (U27) are driven by the control register. The proper X16 clock rate is selected to drive the UART receiver. The receive baud rates are selected as follows:

CONTROL REGISTER 3	2	1	RECEIVE BAUD RATE	
1	1	1	9600	
1	1	0	4800	
1	0	1	2400	
1	0	0	1200	
0	1	1	300	
0	1	0	150	(If 134 Switch Open)
			134.5	(If 134 Switch Closed)
0	0	1	110	
0	0	0	External Clock	(If CBE Switch Open)
			Custom Baud Rate	(If CBE Switch Closed)

3.4.3 The custom baud rate generator also consists of three 4-bit binary counters (U14, U24, and U25). These counters are programmed with 12 switches to produce the desired baud rate. The counters get preset when the TC (Pin 15) output of all three counters is true. The TC output of the last counter is gated with the bus System Clock to prevent glitching and routed through a D-type flip-flop to square the signal.

The transmit baud rate multiplexer (U26) is programmed with the split-rate (S0, S1, and S2) Switches and selects a frequency to clock the UART at the desired baud rate. The transmit baud rates are selected as follows:

S2	S1	S0	TRANSMIT BAUD RATE
SC	SC	SC	Custom Baud Rate
S0	S0	SC	4800
S0	SC	S0	2400
S0	SC	SC	1200
SC	S0	S0	300
SC	S0	SC	150
SC	SC	S0	9600
S0	S0	S0	Selected Receive Baud Rate

SC = Switch Closed
S0 = Switch Open

3.5 TRANSMIT HANDSHAKE.

3.5.1 The transmit handshake circuit provides the capability of handshaking transmitted data with an RS232C control line. When the transmit handshake circuit is enabled (THE Switch closed), the device receiving the transmission has the capability of signaling a "busy" condition on the CB or SB control lines and thus temporarily stopping data transmission. Transmission is halted by turning off the Transmit Clock (TRC) to the UART.

3.5.2 This circuit is a 2-state, synchronous machine that is clocked at 16 times the transmit baud rate. CB and SB must be stable at the middle of the last sixteenth of the last stop bit of a character with at least 150 nanoseconds of setup time. The Off state of CB signals a "busy" condition. The On state of SB signals a "busy" condition unless $\overline{\text{ISB}}$ (P2, Pin 10) is grounded, in which case the Off state of SB signals a "busy" condition. If a "busy" signal appears on CB, SB, or both, then the transmission will be held off.

3.6 RECEIVE HANDSHAKE.

3.6.1 The receive handshake circuit provides the capability of handshaking received data with an RS232C control line.

3.6.2 When the receive handshake circuit is enabled (RHE Switch closed), CD is driven by the DR output of the UART. When DR is active (a character is in the receiver holding register of the UART), CD is turned off. CD is turned off at the nominal center of the first stop bit of each receive character. When the character is read by the processor (DR cleared), CD is turned on. It should be noted that the mandatory disconnect feature (ESCf) cannot be used when the receive handshake circuit is enabled.

3.6.3 To use the receive handshake function, the IAT (Inhibit $\overline{\text{ATN}}$) Switch must be closed. The PCA will not generate interrupts and must be scanned for received data.

3.7 STATUS.

3.7.1 The status circuit is used to gate RS232C control signal information (CF, CB, and SB) and UART status signals (DR, THRE, OE, and PE) to the terminal data bus. When the proper address is decoded, this circuit gates seven bits of status information onto the data bus while $\overline{\text{REQ}}$ is low. (Refer to table 6.2 for detailed explanation of data bit interpretation.)

3.8 FIRMWARE CONTROL WORD. The firmware control word circuit consists of drivers that gate an 8-bit firmware control word to the terminal data bus when enabled by the I/O instruction decoder. When the proper address is decoded, Switch FC0 through FC7 information is gated onto the data bus while $\overline{\text{REQ}}$ is low. A closed switch produces a logic 0 on the data bus and an open switch generates a logic 1.

3.9 CURRENT LOOP. The current loop circuits (In and Out) provide the capability of transmitting and receiving data in a 20-mA dc current loop. (Refer to figure 4 for current loop configurations.)

3.9.1 The current loop receiver (In) is enabled when $\overline{\text{ENCL}}$ (P2, Pin 1) is low (grounded). The receiver can be configured as a floating, passive receiver or as a non-floating, active receiver.

3.9.1.1 In the floating configuration, the transmitter sources current. The current path is into the CL+ (P2, Pin 4) terminal and out the CL- (P2, Pin 5) terminal. When a teletype is the transmitter, the TTY IN (P2, Pin 12) input should be used instead of the CL+ input. In the non-floating configuration, CL+12 (P2, Pin 3) and CL+ are connected, and CL- is connected to ground. (A passive transmitter should be used with this configuration.) The current path is from +12V into CL+ and out of CL- to ground. The transmitter can then short the CL+ and CL- terminals and make the path from +12V to ground directly.

3.9.1.2 The output current of the 5082-4352 opto-isolator (U11) is converted to a voltage with a 2.2k resistor and sensed with a 74LS132 (U19). From a distortion standpoint, the ideal 0-to-20 mA or 20 mA to 0 transition sense level is 10 mA. However, noise considerations dictate that some hysteresis should be incorporated into the design. The current transfer ratio of the opto-isolator and the thresholds of the 74LS132 are the primary factors in determining the current thresholds of the receiver. The 0-to-20 mA transition is sensed between 8.2 mA and 13.4 mA. The 20 mA to 0 transition is sensed between 7.4 mA and 9.4 mA. There is always at least 0.82 mA of hysteresis in the receiver.

3.9.1.3 Current flowing in the receiver is interpreted as a mark. By grounding $\overline{\text{INI}}$ (P2, Pin 2), current flowing in the receiver can be interpreted as a space.

3.9.2 The current loop transmitter (Out) consists of a 20-mA dc current source and a 20-mA dc current sink.

3.9.2.1 The transmitter circuits are switched on and off to provide a high output impedance 20-mA dc current loop transmitter. The CLA line (P2, Pin 6) will source 20 mA when on. The current path is from the +12V supply out the CLA pin, and into the receiver. The return path is ground. The CLP line (P2, Pin 7) will sink 20 mA dc when on. The current path is from the receiver into the CLP pin, and into the -12V supply. The return path is ground. This transmitter will source current into +7.5V to -12V (referenced to ground) or sink current from +12V to -7.5V (referenced to ground).

3.9.2.2 The first stage of the transmitter consists of an NPN (2N4401) and a PNP (2N4403) transistor Q2 and Q1, respectively. This circuit shifts the data from TTL levels to the 12V levels required to turn the 20 mA current controllers on and off. The second stage controls the sourced and sunk current when on, and presents a high impedance to the line when off. The CLA and CLP output pins are protected with series diodes. The output current is controlled by impressing a constant voltage across the 0.15K and 0.10K resistors that are in series with the output. This voltage is maintained by the 1.5K, 8.2K, 1.5K voltage divider. When the transmitter is on, 24V is impressed across these resistors. The two diodes in series with these resistors are used to reduce current variations due to temperature changes.

3.9.2.3 A mark is transmitted as current in the line. By grounding $\overline{\text{IN0}}$ (P2, Pin 8), a space can be transmitted as current in the line.

3.9.3 Current Loop Specifications.

	Min	Max	Units
Passive Receiver, Floating			
Marking Current	15.0	25.00	mA
Spacing Current	0.0	5.00	mA
Voltage Drop, Marking	1.4	1.80	volts
Active Receiver, Non-floating			
Marking Current	0.0	10.00	mA
Spacing Current	20.0	25.00	mA
Open Circuit Voltage	1.4	1.80	volts
Active Transmitter			
Marking Current Sourced	17.0	25.00	mA
Marking Current Sunk	25.0	35.00	mA
Spacing Current	0.0	0.01	mA
Receiver Voltage			
(receiver sourcing)	- 7.5	12.00	volts
(receiver sinking)	-12.0	7.50	volts

4.0 MODULE ADDRESS STRAPPING.

The module address is a unique 4-bit value (2 octal digits) used to address a particular module on the terminal data bus. The GP Async Data Comm PCA can be straped to respond to any module address from 00 17. To determine the configuration of the A4, A11, A10, and A9 Switches, the following is required:

a) Convert the octal address to a binary address as shown below.

		Switch A4	A11	A10	A9
Module Address	12	1	0	1	0
	3	0	0	1	1

b) Close a switch wherever a "0" appears in the binary module address.

The data comm driver uses module address 10 and the RS232C printer driver uses module address 12.

4.1 CUSTOM BAUD RATE STRAPPING.

The custom baud rate generator provides a clock that is 16 times the desired baud rate. The range of baud rates is from 37.5 to 2400 baud (within 1.0 percent). In addition, certain rates from 2400 to 19.2K baud are also provided.

The baud rate switches are configured as follows. (The example configuration is for 110 baud selection.)

a) Divide 153600 by the desired baud rate.

153600/110 = 1396.36

b) Round the quotient to the nearest integer.

1396.36 becomes 1396

c) Subtract one from the rounded quotient.

1396-1 = 1395

d) Convert the decimal number to a 12-bit binary number.

	MSB											LSB
SWITCH	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
1395	0	1	0	1	0	1	1	1	0	0	1	1

e) Close a switch in every position that has a "1". The remaining switches are left open.

f) To calculate the actual generated baud rate, divide 153600 by the result of step b, above.

153600/1396 = 110.03

(Note: The actual rate may not be exactly equal to the desired rate.)

To clock the receive half of the UART with a custom baud rate, the CBE Switch must be closed and bits, 1, 2, and 3 of the control register must be "0" (External Clock).

4.2 SPLIT BAUD RATE STRAPPING.

Baud rate selection is controlled by bits 1, 2, and 3 of the control register and the S0-S2 Switches. Bits 1, 2, and 3 of the control register, in conjunction with the 134 and CBE switches, determine the receive baud rate. If the S0-S2 Switches are all open the transmit baud rate will always be equal to the receive baud rate. The following chart shows the available split rates and corresponding switch configurations.

TRANSMIT BAUD RATE

			EXT	CUST OM	1 1 5 0 0	1 3 4 . 5	1 2 0 0	2 4 0 0	4 8 0 0	9 6 0 0	BIT 3	BIT 2	BIT 1	
			X		X		X	X	X	X	0	0	0	
		CUSTOM		X	X		X	X	X	X	0	0	0	CBE Switch Closed
	B	110		X	X						0	0	1	
R	A	150		X			X	X	X	X	0	1	0	
E	U	300		X			X	X	X	X	0	1	1	
C	D	1200		X			X	X	X	X	1	0	0	
E		2400		X			X	X	X	X	1	0	1	
I	R	4800		X			X	X	X	X	1	1	0	
V	A	9600		X			X	X	X	X	1	1	1	
E	T	134.5		X		X					0	1	0	134 Switch Closed
	E													
		S2	S0	SC	S0	SC	SC	S0	S0	S0	SC	S0		
		S1	S0	SC	S0	S0	S0	SC	SC	S0	SC	S0		
		S0	S0	SC	S0	SC	S0	SC	S0	SC	S0	S0		

X = Available Split Rate
SC = Switch Closed
S0 = Switch Open

Note: a) If all S0-S2 Switches are open, the transmit baud rate will equal the receive baud rate.
b) The 134 Switch must be closed to get 134.5 baud.
c) The CBE Switch must be closed to get a custom baud rate.

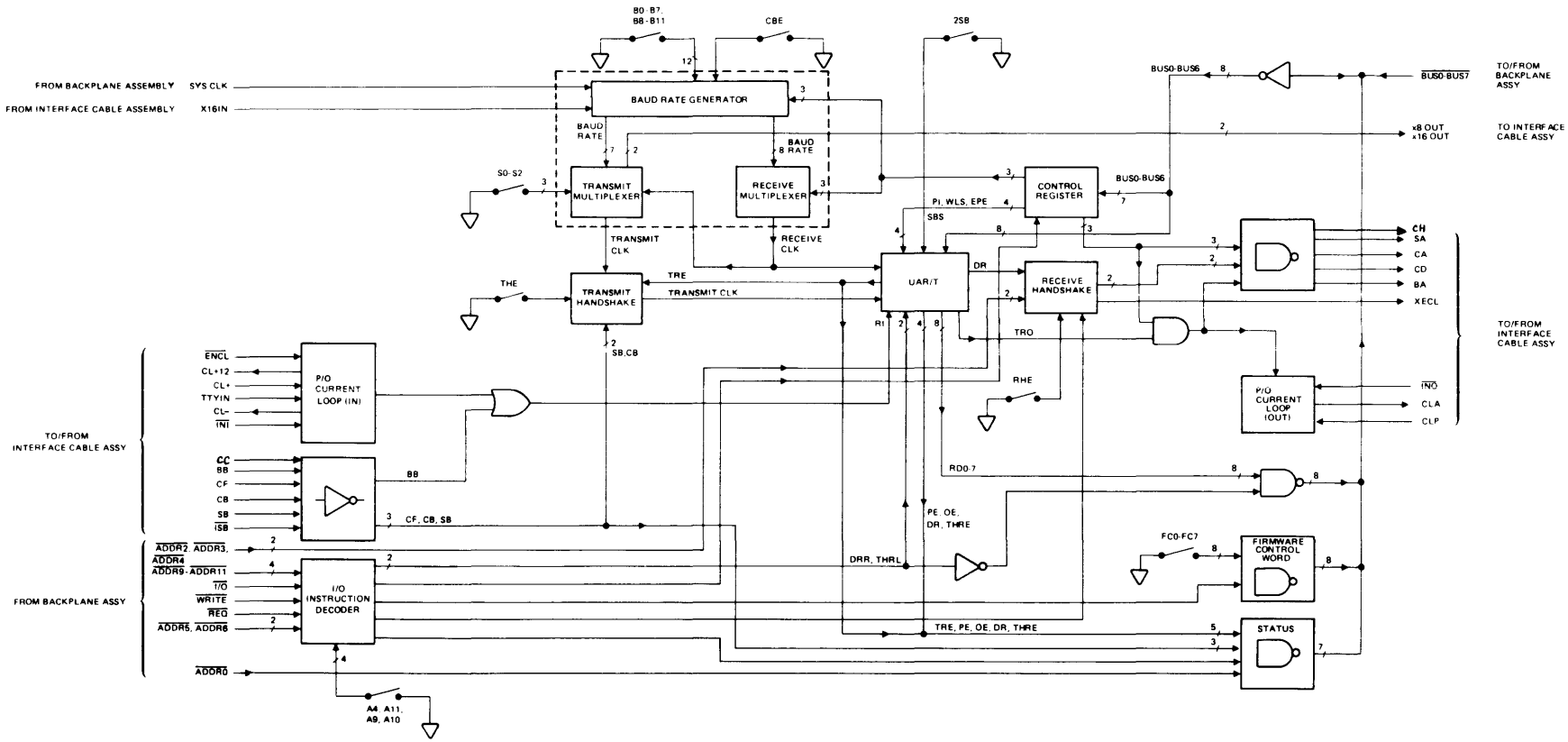

Figure 1
GP Asynchronous Data Comm Block Diagram
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SPARES
1-LS27 - U68
2-LS14 - U110
2-LS04 - U63
2-LS08 - U49
1-LS04 - U62
1-LS74 - U19

Figure 2
GP Asynchronous Data Comm PCA Schematic Diagram
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13255-91143