HP 13255

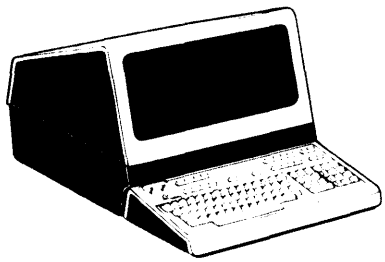
CONTROL STORE MODULE

Manual Part No. 13255-91144

PRINTED

AUG-01-76

DATA TERMINAL
TECHNICAL INFORMATION



HEWLETT hp PACKARD

Printed in U.S.A.

1.0 INTRODUCTION.

The ROM (EA) Module contains space for up to 12K of ROM for storing the operating system firmware.

2.0 OPERATING PARAMETERS.

A summary of operating parameters for the ROM (EA) Module is contained in tables 1.0 through 5.0.

Table 1.0 Physical Parameters

Part Number	Nomenclature	Size (L x W x D) +/-0.100 Inches	Weight (Pounds)
02640-60150	ROM (EA) PCA	12.5 x 4.0 x 0.5	0.44
Number of Backplane Slots Required: 1			

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NOTICE

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NOTE: This document is part of the 264XX DATA TERMINAL product series Technical Information Package (HP 13255).

1.0 INTRODUCTION.

The Control Store Module contains space for up to 8K of ROM and provides 1K byte of read/write storage.

2.0 OPERATING PARAMETERS.

A summary of operating parameters for the Control Store Module is contained in tables 1.0 through 5.0.

Table 1.0 Physical Parameters

Part Number	Nomenclature	Size (L x W x D) +/-0.100 Inches	Weight (Pounds)
02640-60144	Control Store PCA	12.5 x 4.0 x 0.5	0.44
Number of Backplane Slots Required: 1			

Table 2.0 Reliability and Environmental Information

Environmental: (X) HP Class B ( ) Other:
Restrictions: Type tested at product level
Failure Rate: 1.325 (percent per 1000 hours)

Table 3.0 Power Supply and Clock Requirements - Measured
(At +/-5% Unless Otherwise Specified)

+5 Volt Supply	+12 Volt Supply	-12 Volt Supply	-42 Volt Supply
@ 700 mA	@ mA	@ 100 mA	@ mA
	NOT APPLICABLE		NOT APPLICABLE

115 volts ac	220 volts ac
@ A	@ A
NOT APPLICABLE	NOT APPLICABLE

Clock Frequency: 4.915 MHz +/- 0.1%

Table 4.0 Jumper Definitions

PCA Designation	Function	
	In	Out
	If all RAM START ADDR Jumpers are In, then START ADDR=0	
RAM START ADDR 1K	Add 0 to START ADDR	Add 1K to START ADDR
RAM START ADDR 2K	Add 0 to START ADDR	Add 2K to START ADDR
RAM START ADDR 4K	Add 0 to START ADDR	Add 4K to START ADDR
RAM START ADDR 8K	Add 0 to START ADDR	Add 8K to START ADDR
RAM START ADDR 16K	Add 0 to START ADDR	Add 16K to START ADDR
RAM START ADDR 32K	Add 0 to START ADDR	Add 32K to START ADDR
ROM DIAG	ROM Disabled ROM Starts at 32K	ROM Enabled ROM Starts at 0

Table 5.0 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P1, Pin 1	+5V	+5 Volt Power Supply
-2	GND	Ground Common Return (Power and Signal)
-3	SYS CLK	4.915 MHz System Clock
-4	-12V	-12 Volt Power Supply
-5	$\overline{\text{ADDR0}}$	Negative True, Address Bit 0
-6	$\overline{\text{ADDR1}}$	Negative True, Address Bit 1
-7	$\overline{\text{ADDR2}}$	Negative True, Address Bit 2
-8	$\overline{\text{ADDR3}}$	Negative True, Address Bit 3
-9	$\overline{\text{ADDR4}}$	Negative True, Address Bit 4
-10	$\overline{\text{ADDR5}}$	Negative True, Address Bit 5
-11	$\overline{\text{ADDR6}}$	Negative True, Address Bit 6
-12	$\overline{\text{ADDR7}}$	Negative True, Address Bit 7
-13	$\overline{\text{ADDR8}}$	Negative True, Address Bit 8
-14	$\overline{\text{ADDR9}}$	Negative True, Address Bit 9
-15	$\overline{\text{ADDR10}}$	Negative True, Address Bit 10
-16	$\overline{\text{ADDR11}}$	Negative True, Address Bit 11
-17	$\overline{\text{ADDR12}}$	Negative True, Address Bit 12
-18	$\overline{\text{ADDR13}}$	Negative True, Address Bit 13
-19	$\overline{\text{ADDR14}}$	Negative True, Address Bit 14
-20	$\overline{\text{ADDR15}}$	Negative True, Address Bit 15
-21	$\overline{\text{I/O}}$	Negative True, Input Output/Memory
-22	GND	Ground Common Return (Power and Signal)

Table 5.0 Connector Information (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
P1, Pin A	GND	Ground Common Return (Power and Signal)
-B		Not Used
-C		
-D		
-E	$\overline{\text{BUS0}}$	Negative True, Data Bus Bit 0
-F	$\overline{\text{BUS1}}$	Negative True, Data Bus Bit 1
-H	$\overline{\text{BUS2}}$	Negative True, Data Bus Bit 2
-J	$\overline{\text{BUS3}}$	Negative True, Data Bus Bit 3
-K	$\overline{\text{BUS4}}$	Negative True, Data Bus Bit 4
-L	$\overline{\text{BUS5}}$	Negative True, Data Bus Bit 5
-M	$\overline{\text{BUS6}}$	Negative True, Data Bus Bit 6
-N	$\overline{\text{BUS7}}$	Negative True, Data Bus Bit 7
-P	$\overline{\text{WRITE}}$	Negative True, Write/Read Type Cycle
-R		Not Used
-S	$\overline{\text{WAIT}}$	Negative True, Wait Control Line
-T	PRIOR IN	Bus Controller Priority In
-U	PRIOR OUT	Bus Controller Priority Out
-V		Not Used
-W		
-X		
-Y	$\overline{\text{REQ}}$	Negative True, Request (Bus Data Currently Valid)
-Z		Not Used

3.0 FUNCTIONAL DESCRIPTION. Refer to the block diagram (figure 1), schematic diagram (figure 2), timing diagrams (figures 3, 4, and 5), component location diagram (figure 6), and parts list (02640-60144) located in the appendix.

As shown in the block diagram, the Control Store Module contains 8K bytes of ROM, 1K byte of RAM, a RAM select comparator, a RAM select decoder, and associated timing and control logic.

3.1 ROM. The ROM block consists of four EA 4900 chips, each containing 2048 bytes.

3.2 RAM. The RAM provides 1K of 8-bit words of addressable read/write storage. It consists of eight Intel 2102 or equivalent chips, each containing 1024 bits.

3.3 RAM SELECT COMPARATOR. The RAM select comparator applies a RAM SEL signal to the timing logic. The RAM SEL signal is determined by the configuration of starting address jumpers and address bits $\overline{\text{ADDR10}}$ through $\overline{\text{ADDR15}}$.

3.4 ROM SELECT DECODER. The ROM select decoder decodes address bits $\overline{\text{ADDR11}}$ through $\overline{\text{ADDR15}}$. When a ROM address is recognized, a ROM SEL (U311, Pin 6) signal is applied to the timing logic and the appropriate 2K module of ROM is enabled by its SEL signal.

3.5 TIMING AND CONTROL LOGIC.

3.5.1 The timing and control logic generates the necessary signals to perform the read or write operation. The 93L10 counter (U32) drives the logic through the states required for the operation. The counter advances on the negative edge of SYS CLK after the counter is enabled.

3.5.2 ROM READ. The SYS CLK, $\overline{\text{I/O}}$, $\overline{\text{REQ}}$, $\overline{\text{WRITE}}$, and ROM SEL lines enable the 93L10 counter (U32) and asserts the $\overline{\text{READ ADDRESS}}$, $\overline{\text{WAIT}}$, and ROM OUT CLK signals. The counter advances to the states labeled in the timing diagram in figure 3 on the clock edges indicated by arrows. State 2 and the positive half of the SYS CLK drops $\overline{\text{READ ADDRESS}}$. On the sixth

clock, the counter is preset to State 8, thus terminating the $\overline{\text{WAIT}}$ signal. By that time, ROM data ($\overline{\text{BUS0}}$ through $\overline{\text{BUS7}}$) is valid. When $\overline{\text{REQ}}$ is dropped, ROM OUT CLK is terminated and ROM bus gates are disabled.

3.5.3 RAM READ. The SYS CLK, $\overline{\text{I/O}}$, $\overline{\text{REQ}}$, $\overline{\text{WRITE}}$, and RAM SEL signals enable the 93L10 counter, U32. The generated $\overline{\text{WAIT}}$, RAM OUT CLK, $\overline{\text{RAM ENABLE}}$, and READ/WRITE signals are detailed in the RAM read timing diagram in figure 4. When the RAM SEL signal is decoded and $\overline{\text{I/O}}$ is high, the RAM is enabled by the $\overline{\text{RAM ENABLE}}$ signal. READ/WRITE stays high throughout the entire cycle. The counter advances to the states labeled in figure 4 on the clock edges indicated by arrows. On the sixth clock, the counter is preset to State 8, which terminates the $\overline{\text{WAIT}}$ signal. By then, the RAM data $\overline{\text{BUS0}}$ through $\overline{\text{BUS7}}$ is valid. When $\overline{\text{REQ}}$ goes high, RAM OUT CLK is terminated and RAM bus gates are disabled.

3.5.4 RAM WRITE. A RAM write operation is similar to the RAM read operation described in section 3.5.3 above. During RAM writes the $\overline{\text{WRITE}}$ signal is asserted as shown on the RAM write timing diagram, figure 5. In State 1, the latch (U21, Pins, 1, 2, 8, 9, 10, 11, 12, and 13) is reset. The READ/WRITE (U21, Pin 12) signal goes low and data is written into memory. When the counter moves into State 8, the latch is set; the READ/WRITE signal goes high; and the $\overline{\text{WAIT}}$ signal is terminated. The RAM OUT CLK signal remains low during the entire cycle.

4.0 ROM ORDERING INFORMATION.

4.1 VENDOR. The ROM used is Electronic Arrays' EA4900. It is a 16,384-bit static read-only-memory organized as 2,048 words, 8 bits per word.

4.2 SPECIFICATION. Refer to Electronic Arrays' EA4900 specification sheet.

4.3 DATA CARD FORMATTING. Electronic Arrays' requires that the ROM data be supplied on a deck of standard 80-column computer cards. Each card is to be punched as follows: Note that for the EA4900, a 3-digit octal number is used for representing the 8 ROM outputs for each byte.

Card Column No.	Card Contents
EA 4900	
1-4	Punch a 4-digit octal number representing the input address for the first of the 16 output words appearing on this card. (This is the initial address.)
5-7	Punch a 3-digit octal number representing the outputs for the initial input address.
8-10	Punch a 3-digit octal number representing the outputs for the initial input address +1.
11-13	Punch a 3-digit octal number representing the outputs for the initial input address +2.
-	-
-	-
-	-
50-52	Punch a 3-digit octal number representing the outputs for the initial input address +15.
69-80	The unique number assigned to this ROM pattern by EA must be punched in this field enclosed by blank spaces. This number can be obtained by contacting your local EA salesman, representative, or the marketing department at the factory directly.

Each card, therefore carries (in octal) the initial input address for the 16 output words contained on that card, the 16 output words themselves (in octal) and the unique ROM number. The cards must be provided for all possible sequential address locations (in blocks of 16). A 2048 word ROM, therefore, requires 128 cards, with all 16 output words defined on each card.

4.4 ROM PULL-UPS. The ROM has programmable input resistors. To provide minimum high level input voltage (3.5V) at least one ROM chip must be programmed with internal pull-ups.

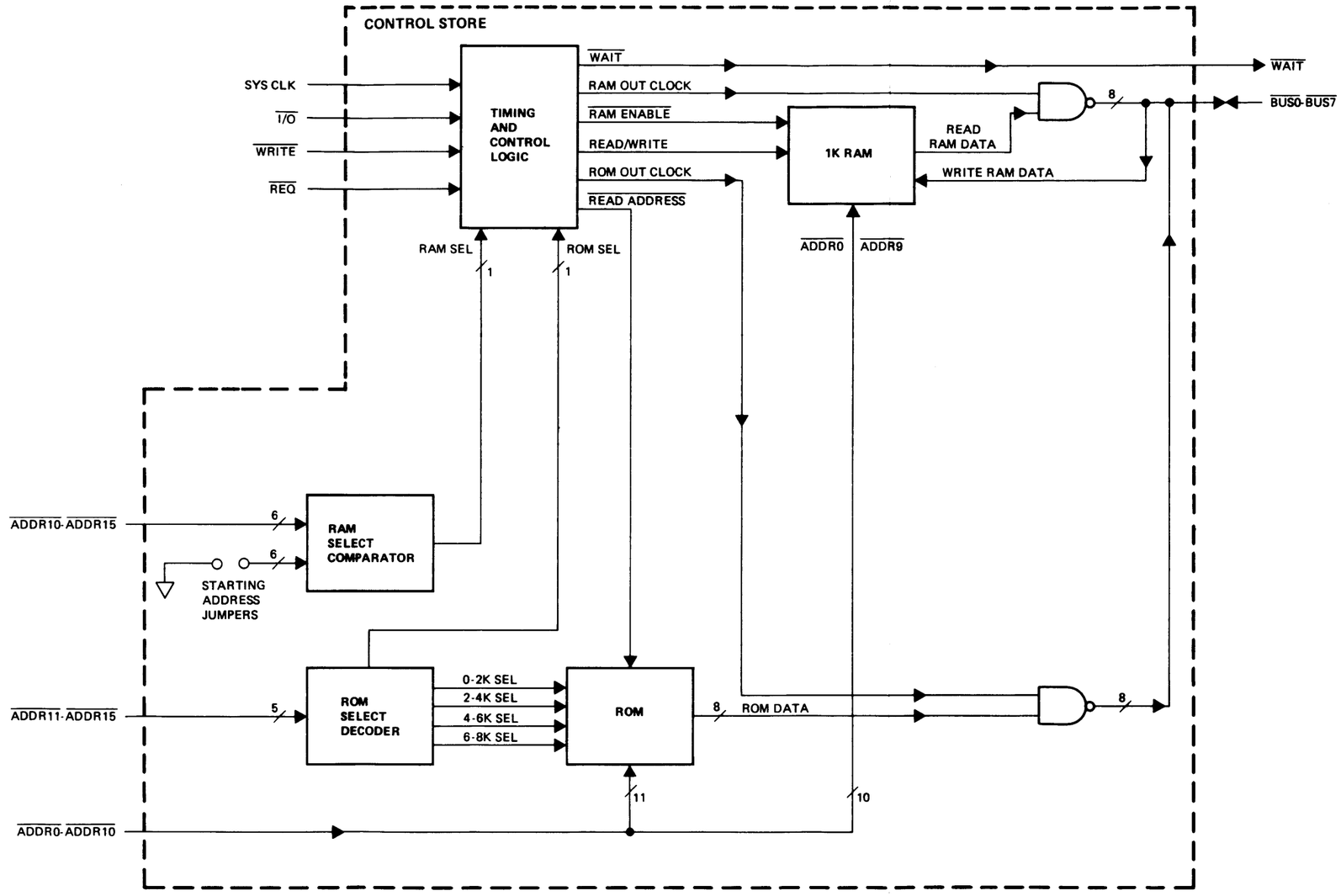

Figure 1
Control Store Module Block Diagram
AUG-01-76 13255-91144

TO BACKPLANE PCA

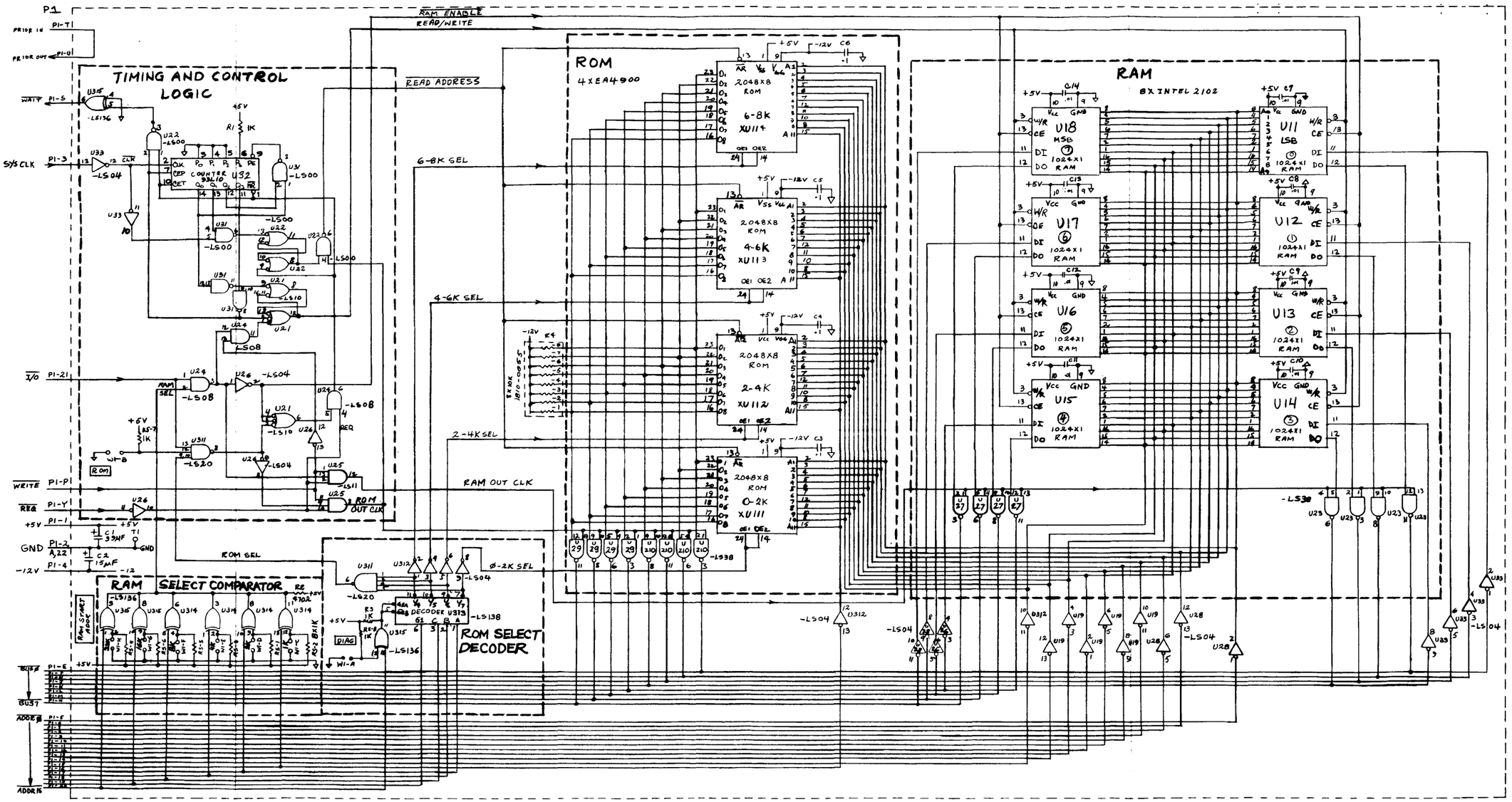

Figure 2
Control Store PCA Schematic Diagram
AUG-01-76 13255-91144

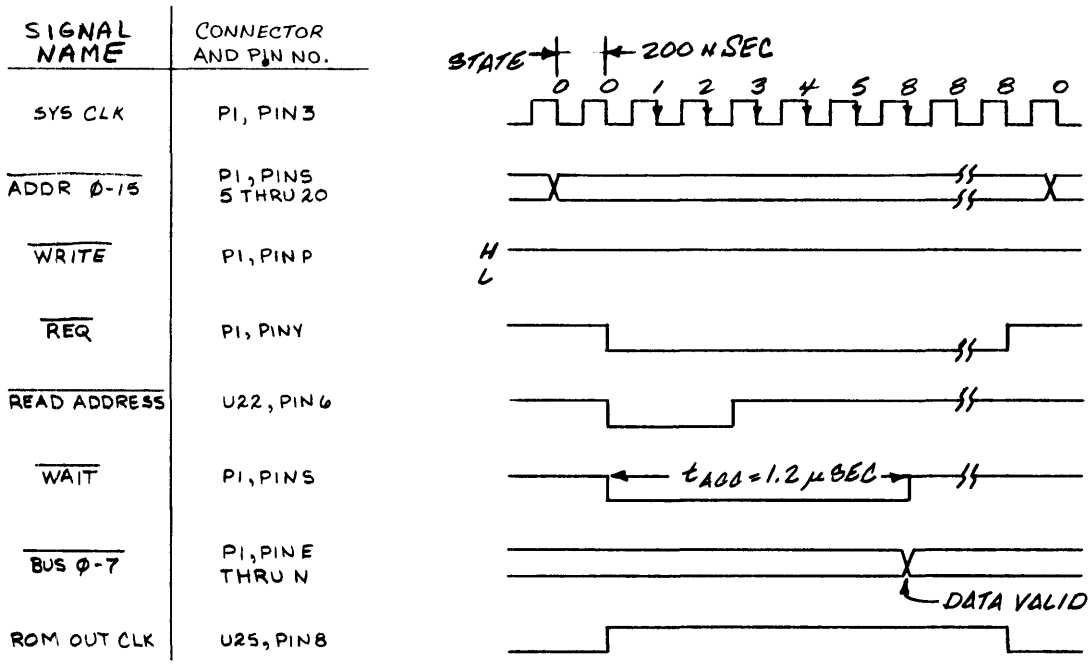

Figure 3
ROM Read Timing Diagram
AUG-01-76 13255-91144

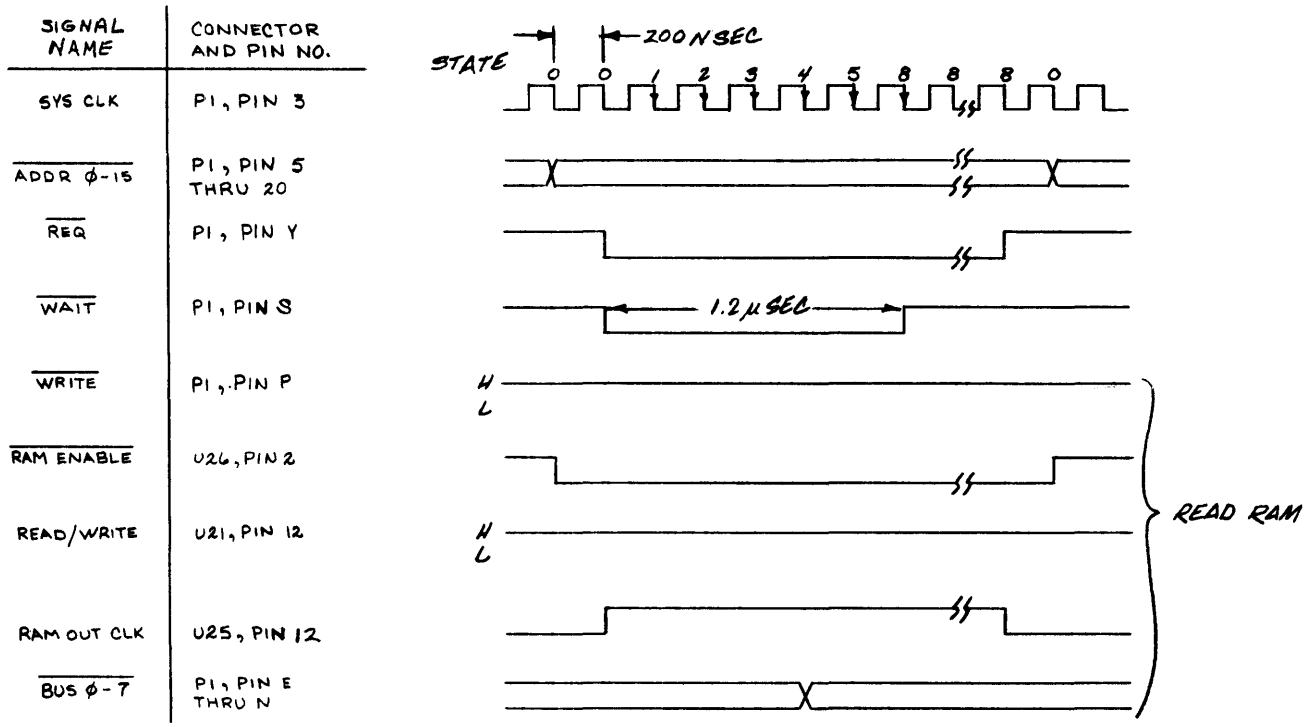

Figure 4
RAM Read Timing Diagram
AUG-01-76 13255-91144

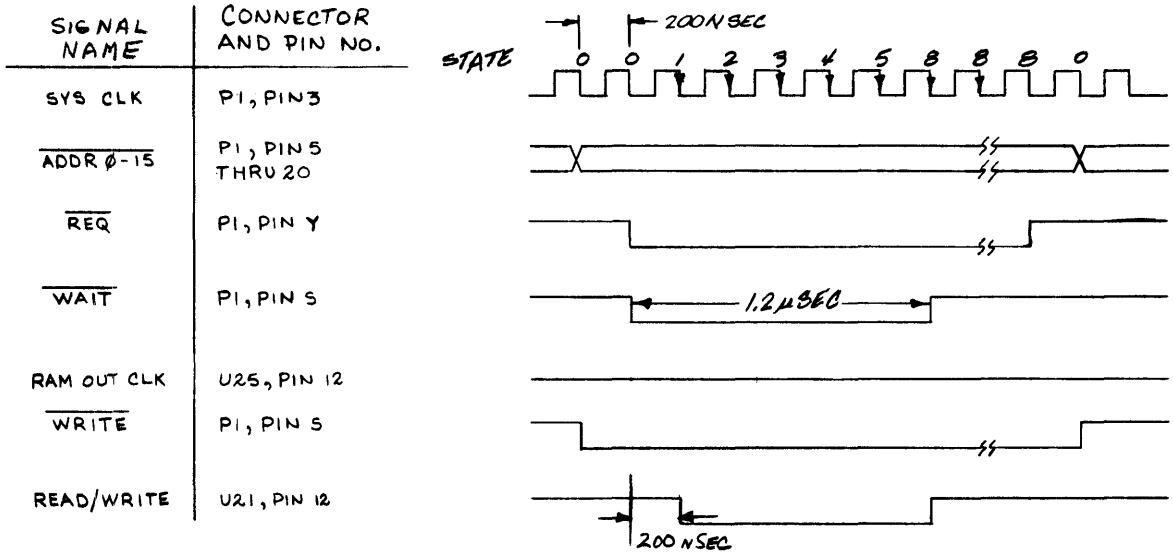

Figure 5
RAM write Timing Diagram
AUG-01-76 13255-91144

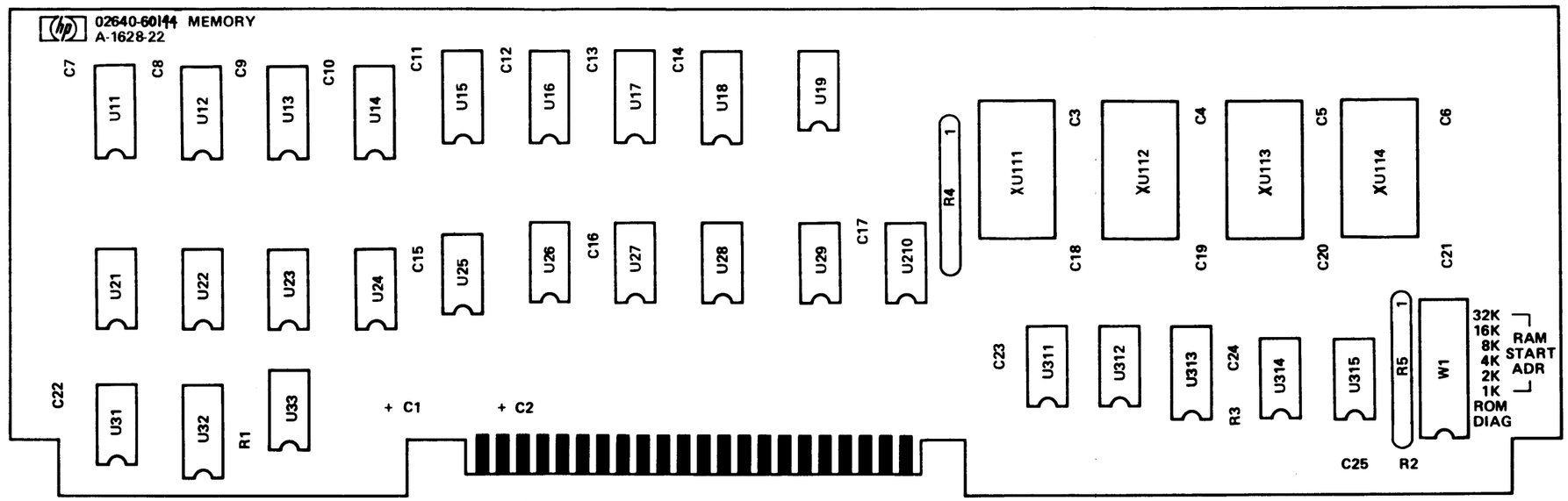

Figure 6
Control Store PCA Component Location Diagram
AUG-01-76 13255-91144

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
	02640-60144	1	GP BASIC MEMORY ASSEMBLY DATE CODE: A-1628-22 REVISION DATE: 08-13-76	28480	02640-60144
C1	0180-0393	1	CAPACITOR-FXD 39UF+-10% 10VDC TA	56289	150D396X9010B2
C2	0180-1746	1	CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
C3	0150-0121	4	CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
C4	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
C5	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
C6	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
C7	0160-2055	19	CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C8	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C9	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C10	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C11	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C12	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C13	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C14	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C15	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C16	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C17	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C18	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C19	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C20	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C21	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C22	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C23	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C24	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C25	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
E1	0360-0124	1	TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
R1	0683-1025	2	RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R2	0683-4715	1	RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R3	0683-1025		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R4	1810-0055	1	NETWORK-RES 9-PIN-SIP .15-PIN-SPCG	28480	1810-0055
R5	1810-0121	1	NETWORK-RES 9-PIN-SIP .15-PIN-SPCG	28480	1810-0121
U11	1820-1078	8	IC 1K RAM NMOS	28480	1820-1078
U12	1820-1078		IC 1K RAM NMOS	28480	1820-1078
U13	1820-1078		IC 1K RAM NMOS	28480	1820-1078
U14	1820-1078		IC 1K RAM NMOS	28480	1820-1078
U15	1820-1078		IC 1K RAM NMOS	28480	1820-1078
U16	1820-1078		IC 1K RAM NMOS	28480	1820-1078
U17	1820-1078		IC 1K RAM NMOS	28480	1820-1078
U18	1820-1078		IC 1K RAM NMOS	28480	1820-1078
U19	1820-1199	5	IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
U21	1820-1202	1	IC-DIGITAL SN74LS10N TTL LS TPL 3 NAND	01295	SN74LS10N
U22	1820-1197	2	IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
U23	1820-1209	4	IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U24	1820-1201	1	IC-DIGITAL SN74LS08N TTL LS QUAD 2 AND	01295	SN74LS08N
U25	1820-1203	1	IC-DIGITAL SN74LS11N TTL LS TPL 3 AND	01295	SN74LS11N
U26	1820-1199		IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
U27	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U28	1820-1199		IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
U29	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U31	1820-1197		IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
U32	1820-0669	1	IC-DIGITAL 93L10DC TTL L BCD SYNCHRO	07263	93L10DC
U33	1820-1199		IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
U310	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U311	1820-1204	1	IC-DIGITAL SN74LS20N TTL LS DUAL 4 NAND	01295	SN74LS20N
U312	1820-1199		IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
U313	1820-1216	1	IC-DIGITAL SN74LS138N TTL LS 3	01295	SN74LS138N
U314	1820-1215	2	IC-DIGITAL SN74LS136N TTL LS QUAD 2	01295	SN74LS136N
U315	1820-1215		IC-DIGITAL SN74LS136N TTL LS QUAD 2	01295	SN74LS136N
W1	1200-0482	1	SOCKET-IC 16-CONT DIP-SLDR	91506	516-AG11D
W1A	1258-0124	2	PIN-PROGRAMMING JUMPER;.30 CONTACT	91506	8136-475G1
W1B	1258-0124		PIN-PROGRAMMING JUMPER;.30 CONTACT	91506	8136-475G1
XU111	1200-0541	4	SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU112	1200-0541		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU113	1200-0541		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU114	1200-0541		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541