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Cross-Coupled Charge-Transfer Sense Amplifier and Latch Sense Scheme for High-Density FET Memories

This paper describes a sense scheme for use on high-density one-device cell field effect transistor random access memories (FET RAMs). The high-sensitivity threshold-independent cross-coupled charge-transfer sense amplifier and latch is used. The IBM 64K-bit one-device dynamic memory cell FET RAM chip design is used as the vehicle for the discussion. Adaptations made on the sense amplifier and latch for use with the sense scheme are discussed. Also described are 1) dummy cell design, 2) subthreshold leakage considerations, 3) single-ended input/output (I/O) circuitry sensing and ramifications, 4) multiple cycle signal degradations, and 5) a maximum supply voltage (V_H) buffer circuit sense scheme improvement.

Introduction

There is a direct relationship between the array density and the sensitivity of the detection circuit (*i.e.*, sense amplifier/latch circuit) for one-device cell field-effect transistor random access memories (FET RAMs). Because of this, there has been considerable interest in the application of the charge-transfer concept to one-device cell FET RAM sense amplifiers to increase detection circuit sensitivity [1-3]. High-sensitivity charge-transfer sense amplifiers [1] and cross-coupled charge-transfer sense amplifiers [2, 3] have been disclosed and discussed in this available literature. This paper discusses the adaptation of the cross-coupled charge-transfer sense amplifier and latch for use on IBM's 64K-bit one-device dynamic memory cell FET RAM [4]. The cross-coupled charge-transfer sense amplifier was chosen over the charge-transfer sense amplifier because of its high-speed preamplification advantage. In addition, there are no disadvantages.

Design problems and their solutions will be discussed. These are 1) amplification capacitor placement, 2) restore shorting (RL) device use and placement, 3) incomplete precharge restore design considerations, 4) one-device dynamic memory cell subthreshold leakage problems, and 5) single-ended I/O circuitry sensing and ramifications. Other design considerations will also be discussed. These are 1) dummy cell design, 2) multiple read signal degradations, and 3) the use of a V_H (most positive voltage) buffer circuit.

The 64K-bit chip memory cell is a conventional one-device cell [5]. $V_H - V_T$ is both the bit line precharge level and the stored high level. Ground is the stored low level. Figure 1 is a schematic of the 64K-bit chip sense scheme with the cross-coupled charge-transfer sense amplifier and latch. Figure 2 shows a timing diagram for the sense scheme. The 64K-bit chip is organized as two independent islands. The array of each island contains 256 bit lines and 128 word lines. There are 64 word lines on each side of the sense amplifier and latch, and a single-ended I/O sensing scheme is used.

Cross-coupled charge-transfer sense amplifier and latch

Figure 3 shows the actual cross-coupled sense amplifier and latch and its associated timings. The charge-transfer principle, the cross-coupled feature, the basic operation, and the threshold-independent advantage of the latch are discussed in the previous references.

The adaptations made will now be covered. However, two points should be noted. First, the AMP pulse rise time (T_R) is approximately 85 ns. Slower amplification does not result in significant density improvement. Second, bucket device (devices T3 and T4) β mismatches are also partially compensated for from cycle to cycle. If the β of one of the bucket devices is lower than the other, its pre-

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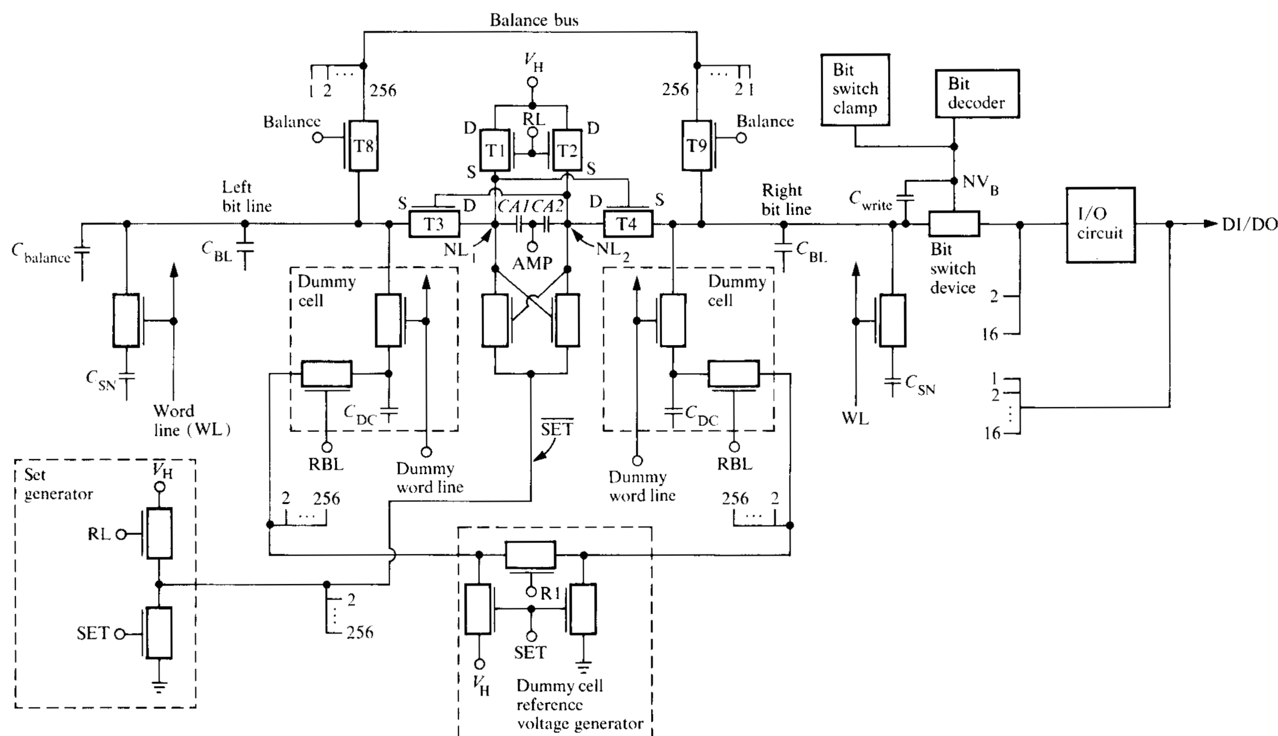


Figure 1 64K-bit RAM chip sense scheme with the cross-coupled charge-transfer sense amplifier and latch.

charge will be slower but its gate drive during amplification will be increased. This partially compensates for the mismatch.

- *Amplification capacitor placement*

Two placements are possible for the amplification capacitors (*CA1* and *CA2*) in the 64K-bit chip cross-coupled charge-transfer type of sense scheme (see Fig. 1): either incoupling into the internal nodes of the sense latch [2, 3] or outcoupling from the bit lines. The 64K-bit chip uses the former of these placements (devices *CA1* and *CA2* in Fig. 1). The advantages of incoupling into the internal nodes of the sense latch are as follows:

1. During amplification, there is a net charge gain on the bit lines, rather than a net positive charge loss. For the 64K-bit design, the array-cell-stored high-level voltage increase is approximately 0.5 V.
2. There is a larger cell-to-bit line transfer ratio for the left bit line:

$$\frac{C_{SN}}{(C_{BL} + C_{balance} + C_{SN})};$$

and for the right bit line:

$$\frac{C_{SN}}{(C_{BL} + C_{write} + C_{SN})}.$$

See Fig. 1.

3. The amplification capacitors are smaller, which results in a smaller required layout area.

Statistical and worst-case computer circuit analysis results, with 3σ worst-case process tracking mismatches included, verify the advantages of the incoupling type of amplification scheme. The Monte Carlo method is used for the statistical analysis, and the worst-case condition is with all parameters and trackings at their simultaneous 3σ worst-case limits. The before-amp signal necessary to drive the sense amplifier and latch (*i.e.*, bit line voltage difference) has to be 15.9% larger for the alternative outcoupling scheme for a worst-case comparison. If a statistical mean $+3\sigma$ comparison is made, this bit line voltage difference has to be 10.9% larger for the alternative outcoupling scheme.

RL shorting device

The use of a device gated by RL to short the two nodes of the sense latch together (nodes NL_1 and NL_2 in Fig. 1) was investigated. Restore time statistical runs were made with and without this added RL shorting device. It was found that for any particular sense latch layout width the restore performance was better with two larger RL restore devices (devices T1 and T2 in Fig. 1) and no shorting device than with two smaller RL restore devices and a shorting device. Both the bucket (*i.e.*, charge-transfer device) drive difference between devices T3 and T4 and the maxi-

mum bucket on drive were always less when the two larger RL restore devices and no shorting device configuration was used. Statistical computer run results show that the mean $\pm 3\sigma$ bucket drive difference is 25% worse, and the maximum bucket on drive is 35% worse, if the shorting device configuration is used. Decreased bucket on drive allows a smaller RL outcoupling voltage swing (see next section), which will minimize any capacitance ratio mismatch noise voltages.

Incomplete precharge restore design

The current literature on charge-transfer sense amplifiers describes precharging the sense amplifier and bit lines at the beginning of the chip cycle [1, 2]. The possibility of an incomplete precharge is also discussed [1], although a degraded sense amplifier sensitivity can result. The 64K-bit chip begins precharging at the end of the chip cycle, rather than at the beginning, to minimize the chip access time. Cycle time is not impacted by such a change. However, this creates a voltage trapping problem which needs to be eliminated. Also any precharge is by necessity incomplete to some degree, and careful design is required for high sensitivity. These problems, their solutions, and some sense latch precharge characteristics are now discussed.

The sequence of events leading to the voltage trapping problem mentioned above is as follows:

1. Assume RL comes up with V_H at its maximum voltage.
2. Nodes NL_1 and NL_2 are charged to the maximum V_H.
3. The bit lines are charged to the maximum V_H minus the V_T of their respective bucket devices (devices T3 and T4 in Fig. 1).
4. Assume V_H now drops. Nodes NL_1 and NL_2 will follow V_H. However, the bit line voltage is trapped.

Thus, after this sequence of events during one precharge period, the bucket devices can be turned off to a very significant degree. This creates a significant noise source and design problem in turning on the charge-transfer devices during the amplification period. The noise source results from capacitance tracking mismatches, β tracking mismatches, and the ΔV amounts that the internal sense latch nodes have to be moved to start the amplification operation. The solution to this problem used on the 64K-bit chip is to terminate the precharge at the end of the minimum chip cycle time and not allow it to continue between cycles. This is done by bringing RL back to V_H (or lower), as indicated in Figs. 1 and 2.

The outcoupling introduced into the sense latch nodes by the RL fall (back to V_H in this case) is a design constraint. The cross-coupled charge-transfer devices have to turn off with the RL outcoupling. They have to turn off

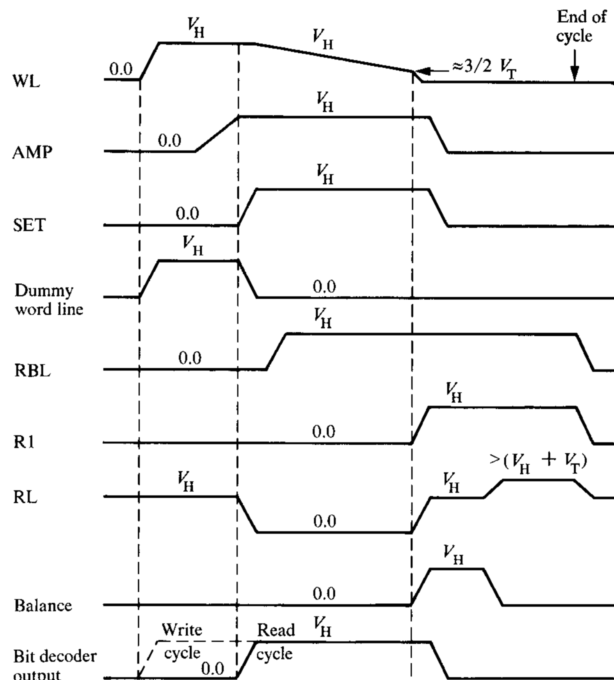


Figure 2 Timing diagram for 64K-bit FET RAM sense scheme.

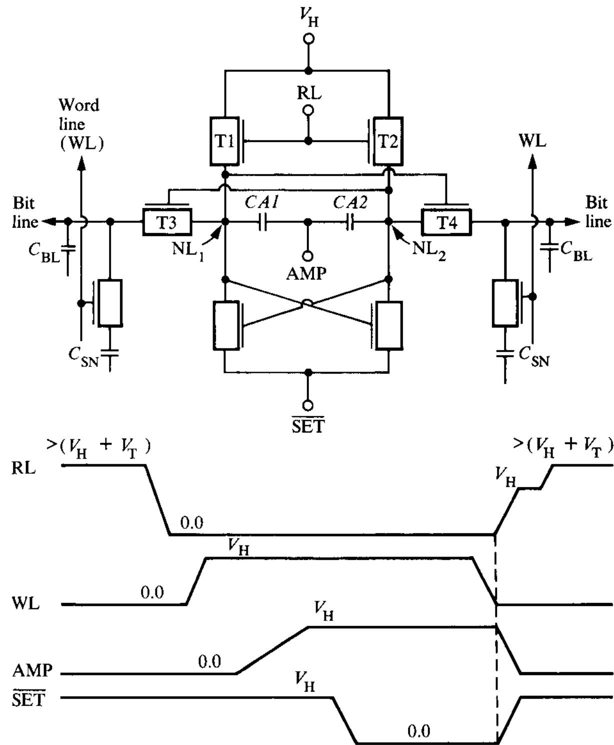


Figure 3 Cross-coupled charge-transfer sense amplifier and latch.

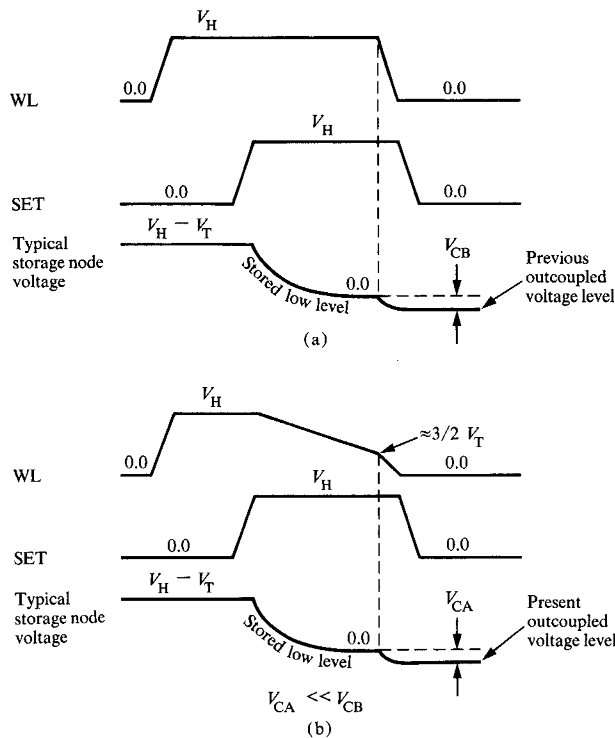


Figure 4 Previous and present timings for stored low-level subthreshold leakage problem.

by a sufficient amount to allow for bit line leakage, and to permit the net cell and dummy cell signal to develop. There should not be an excess of outcoupling. Sufficient RL outcoupling cuts devices T3 and T4 off and allows an incomplete precharge design, eliminating any additional noise resulting from the incomplete precharge.

Another solution is possible to this voltage trapping problem. We can use a circuit to buffer V_H so the sense amplifier and latch can be restored between cycles. Such a circuit is discussed in a later section.

Thus, we have two design solutions for high-frequency V_H noise. The possibility of low-frequency V_H noise dictates that the bit line half that remains at $V_H - V_T$ be discharged partially prior to precharge to account for such a low-frequency voltage change. The balance devices (devices T8 and T9 in Fig. 1) short all the bit lines together and accomplish this purpose [6]. These devices also serve two other purposes. First, the total RL time at the $>(V_H + V_T)$ level required to reach a particular bucket drive difference and maximum on drive is greatly reduced. Second, sense latch RL device hot electron stress can be greatly reduced or eliminated, depending on the timing.

The required precharge time is significantly affected by mismatches in charge-transfer device β tracking and bit line capacitance tracking [1]. It is insensitive to mismatches in bucket device V_T tracking, RL device β tracking, RL device V_T tracking, and latch node capacitance tracking.

Subthreshold leakage problems in one-device dynamic memory cells

Two memory cell subthreshold leakage problems were encountered during the design of the 64K-bit chip. These problems and their solutions are discussed below.

- *Memory cell stored low-level subthreshold leakage problem*

For high-density one-device dynamic memory cells with a conventional two-level word line pulse (see previous typical timing, Fig. 4), a stored low-level subthreshold leakage problem can exist. Word line gate to source memory cell outcoupling of a stored low level (*i.e.*, 0.0 volt level) when the word line falls can cause subthreshold leakage current in the memory cell FET device. This subthreshold leakage current will pull charge out of the respective bit line and charge up the storage node until the memory cell FET device comes out of the subthreshold leakage region.

As discussed in the section on incomplete precharge restore design, the bit lines in the 64K-bit chip design are not clamped between cycles. The long time constant subthreshold leakage current in the memory cell can unbalance the bit lines and can create a significant sense latch noise source. One type of pattern gives the worst problem. It consists of two steps: first, write or read several consecutive minimum cycle time stored low levels on one side of the sense latch in different memory cells; next, read a stored high level in another memory cell on the same side of the sense latch.

The 64K-bit chip uses a three-level word line pulse [7] to eliminate this problem (see present timing in Fig. 4). Pulling the word line slowly to a level greater than V_T allows most of the outcoupled memory cell charge to escape to the bit line. In the case of the 64K-bit chip, this level is approximately (3/2) V_T. The final fall of the word line will not put the memory cell devices in the subthreshold leakage region.

- *Bit switch outcoupling-induced subthreshold leakage problem*

Subthreshold leakage current can also cause a stored high-level memory cell problem. Figure 5 illustrates the problem. Node NV_B fall-induced bit line outcoupling can cause a bit line to go below ground just before the bit line precharge or restore operation begins. This outcoupling below ground can cause subthreshold leakage current in

memory cell devices, particularly next to the bit switch as shown in Fig. 1, which will discharge a stored high level.

Statistical computer run results show that if the problem were allowed to exist, the yield loss would have been an additional seven percent. The problem was solved by turning the bit switch device off at or after the point at which the bit line starts to restore.

Single-ended I/O circuitry sensing and ramifications

The 64K-bit memory chip uses a single-ended I/O sensing scheme (see Fig. 1) to maximize density in the process technology used to manufacture it. The following three sections cover the unique aspects of this scheme, which are 1) write high level on right bit line operation, 2) bit line matching circuitry, and 3) the differential mode noise problem.

- *Write high level on right bit line*

The bit switch device turns on with the word line for a write cycle and with the SET pulse for a read cycle. For a write cycle, the right bit line is either pulled down by a device in the I/O circuitry, or coupled up by the C_{write} capacitor. This section derives the equation for the size of the C_{write} capacitor in order to guarantee sufficient in-coupling to write a one in a memory cell on the right bit line with a stored low level. Figure 6 shows the simplified capacitor circuit schematic.

The memory cell turn-on induces the following bit line voltage change on the right bit line:

$$(\Delta V)_{\text{cell}} = -(V_{\text{H}} - V_{\text{T}})\left(\frac{C_{\text{SN}}}{C_{\text{SN}} + C_{\text{BL}} + C_{\text{write}}}\right).$$

The bit switch device turn-on induces the following bit line voltage change on the right bit line:

$$(\Delta V)_{C_{\text{write}}} = \Delta N_{\text{VB}}\left(\frac{C_{\text{write}}}{C_{\text{SN}} + C_{\text{BL}} + C_{\text{write}}}\right),$$

where

$$\Delta N_{\text{VB}} \geq V_{\text{H}} - 0.5.$$

The design criterion becomes

$$|(\Delta V)_{C_{\text{write}}}| \geq |(\Delta V)_{\text{cell}}|(SF),$$

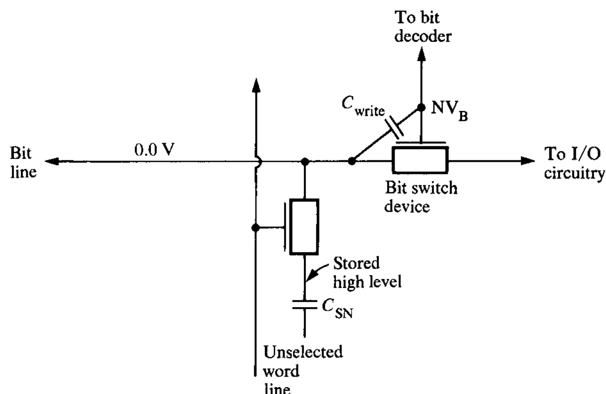
where SF is a design safety factor, arbitrarily chosen to be 1.25 for the 64K-bit chip.

The following equation can be derived for C_{write}:

$$\Delta N_{\text{VB}} \times C_{\text{write}} \geq (V_{\text{H}} - V_{\text{T}})C_{\text{SN}}(1.25),$$

$$C_{\text{write}} \geq C_{\text{SN}}\left(\frac{V_{\text{H}} - V_{\text{T}}}{\Delta N_{\text{VB}}}\right)(SF),$$

$$C_{\text{write}} \geq C_{\text{SN}}\left(\frac{V_{\text{H}} - V_{\text{T}}}{V_{\text{H}} - 0.5}\right)(1.25).$$



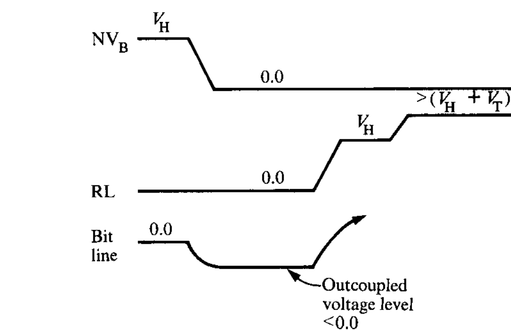


Figure 5 Bit switch outcoupling-induced subthreshold leakage problem. Timing diagram shows a timing which could cause a problem.

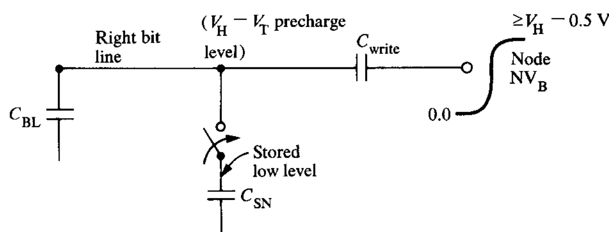


Figure 6 Right bit line write high-level simplified capacitor circuit.

- *Bit line matching*

The single-ended I/O sensing scheme has only one bit switch device at the end of one bit line, which is the right bit line in this case. This needs to be compensated for by increasing the capacitance of the left bit line. This is the purpose of the C_{balance} capacitor in Fig. 1. Ideally, a dummy bit switch device would be used. However, to minimize chip area, an extra piece of diffusion was used on the 64K-bit chip.

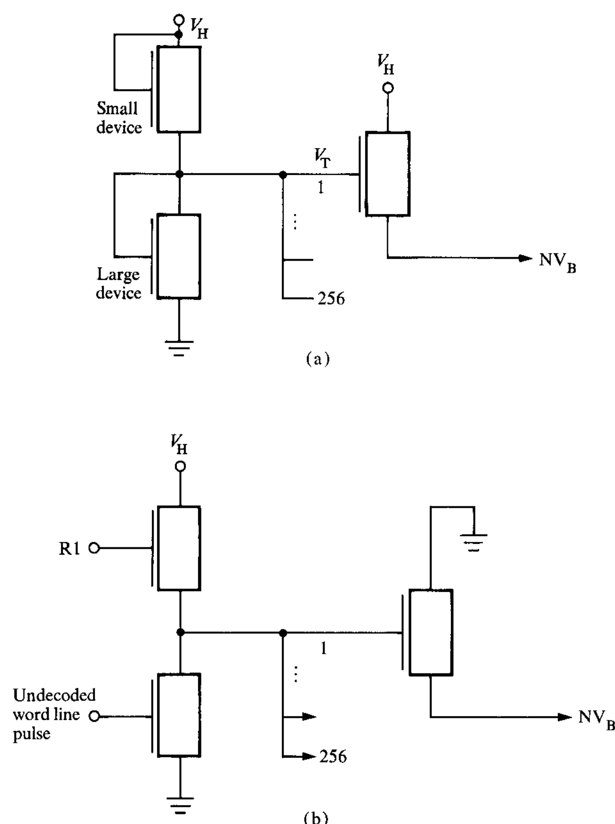


Figure 7 Bit switch clamp circuits: (a) diode clamp; (b) active clamp.

• *Differential mode noise problem*

The main problem with a single-ended I/O sensing scheme is differential mode noise injection onto the bit lines. The differential mode noise introduced in the 64K-bit chip sense scheme (see Fig. 1) will be referred to as bit switch noise.

Bit switch noise results from the act of discharging the unselected bit decoders. This injects noise onto the bit switch gate, which in turn injects noise onto the right bit line. Computer-predicted signal loss results from the 64K-bit chip show that if the problem were allowed to exist, the nominal signal loss would be between 13% and 26% and the maximum signal loss would be between 23% and 41%. Noise can also be injected onto the bit switch gate by the I/O circuitry during a write low-level cycle. An already intolerable situation would be made worse by increasing this noise. The solution to this problem is to clamp node NV_B to ground.

Two single device clamp circuits are possible. The first is a diode clamp and the second is an active clamp. Both, which are illustrated in Fig. 7, significantly reduce the noise source; however, the diode clamp is preferential to the active clamp. The active clamp has two remaining noise sources which are bit switch clamp T_{off} noise and write low-level noise. The bit switch clamp T_{off} noise is the result of the active bit switch clamp gate discharge injecting capacitively coupled noise voltage onto the bit switch device gate. The write low-level noise is the result of the I/O circuit fanout node discharge (see Fig. 5) injecting capacitively coupled noise onto the bit switch device gate. Although the diode clamp is slower because of its source follower pull-up, it is better because these two noise sources are not a factor. Also, the diode clamp is on throughout the entire cycle.

The 64K-bit chip uses an active clamp. Computer-predicted signal loss results predict a signal loss of less than 5.6%. The diode clamp will give even better results.

Dummy cell design

The bit line precharge level in the 64K-bit design is $V_H - V_T$, and the one-device array cell high and low levels are $V_H - V_T$ and ground, respectively. Hence, a dummy cell is needed to generate our reference level such that

$$Q_{dummy} = \frac{1}{2} Q_{cell}.$$

A coupling capacitor can be used to generate the half charge, but a cell-type FET and capacitor structure is preferable for a dummy cell to obtain better trackings. A two-cell-per-bit approach is not at all suited to high-density memory designs [8] such as the 64K-bit chip.

These eliminations leave two remaining choices:

1. A half-voltage dummy cell scheme, where

$$Q_{dummy} = C_{DC}\left[\frac{1}{2}(V_H - V_T)\right],$$

$$C_{DC} \approx C_{SN},$$

Dummy cell restored voltage level $= \frac{1}{2}(V_H - V_T)$.

2. A half-capacitance dummy cell scheme, where

$$Q_{dummy} = (C_{DC})(V_H - V_T),$$

$$C_{DC} \approx 1/2\, C_{SN},$$

Dummy cell restored voltage level = ground.

The first of these two, the half-voltage dummy cell scheme, has three advantages and one key reason for being used. The advantages are as follows:

1. Latch set performance; *i.e.*, bit line discharge with SET pulse, will not tend to increase with increasing V_H and decreasing V_T. It will tend to increase with the half-

capacitance dummy cell because the dummy cell reference level is not moving with V_H and V_T and the bit line has to be discharged from a higher voltage level.
2. Net signal will increase with increasing V_H and decreasing V_T. Again, this is not the case with the half-capacitance dummy cell.
3. The dummy cell structure is more like the storage cell since the diffusion capacitances are approximately equal.

The key reason for using the half-voltage dummy cell scheme in our case is that the half-capacitance dummy cell, with its two associated devices, cannot be built at the density of the 64K-bit chip. The C_{SN} diffusion in the storage cell is too small. Thus, the half-voltage dummy cell is used on the 64K-bit chip. The half voltage is generated on separated busses to minimize the required precharge time (see Figs. 1 and 2) rather than trying to use the shorted bit line voltage. Statistical mean $+3\sigma$ computer analysis runs verify the half-voltage dummy cell choice. The signal required for a half-capacitance dummy cell is 5.5% more than with the half-voltage dummy cell. The signal required for a coupling capacitor dummy cell is 17.5% more than with the half-voltage dummy cell. In addition, the computer runs were made with no tracking mismatches included. Tracking mismatches will accentuate the results for the case of the comparison with the coupling capacitor dummy cell.

Multiple read signal degradation

There are voltage noise source signal degradations in the sense system that are affected by multiple cycles in the same cell. Two are 1) the cell leakage current-induced storage node voltage drop; and 2) the net active cycle cell voltage change due to amplify and latch set operations. These affect cell high-level voltages. The result of multiple cycles in the same cell is to amplify the effect of the noise sources. Assume that the cell leakage current-induced storage node voltage drop is V_{loss}. An equation will be derived for the multiple cycle effect on V_{loss}, and the results will apply to both degradations. The following definition of transfer ratio (TR) will be used:

$$TR = C_{SN}/(C_{SN} + C_{BL}).$$

The stored cell high-level voltage at the end of the first cycle is

$$V_{cell} = V_H - V_T.$$

At the beginning of the second cycle,

$$V_{cell} = V_H - V_T - V_{loss}.$$

At the end of the second cycle,

$$V_{cell} = V_H - V_T - (TR)V_{loss}.$$

At the start of the third cycle,

$$V_{cell} = V_H - V_T - V_{loss} - (TR)V_{loss}.$$

At the end of the third cycle,

$$V_{cell} = V_H - V_T - (TR)V_{loss} - (TR)^2V_{loss}.$$

At the start of the fourth cycle,

$$V_{cell} = V_H - V_T - V_{loss} - (TR)V_{loss} - (TR)^2V_{loss}.$$

Hence, the result is the general geometric progression equation

$$V_{cell} = V_H - V_T - V_{loss}(1 + TR + TR^2 + TR^3 + \cdots).$$

Since $TR < 1$, the series converges and

$$V_{cell} = V_H - V_T - V_{loss}\left(\frac{1 - TR^{n+1}}{1 - TR}\right),$$

where n is the number of consecutive cycles

$$n = 0, 1, 2, \cdots, n.$$

Hence, a loss multiplication factor (LMF) can be defined by

$$(\text{effective } V_{loss}) = (V_{loss})(LMF),$$

$$LMF = (1 - TR^{n+1})/(1 - TR).$$

As $n \to \infty$,

$$LMF = 1/(1 - TR).$$

The loss multiplication factor has to be taken into account when the above noise sources are considered. The single-cycle loss has to be multiplied by the loss multiplication factor.

V_H buffer circuit

A V_H buffer circuit [9] can be used to buffer V_H so that the sense latch can be restored between cycles. When V_H is buffered, the sense latch is not affected by high-frequency V_H voltage dips and the sense latch can be continually precharged between cycles. The use of such a circuit significantly reduces the effect of bit line, sense latch, and array cell device leakage and cell subthreshold leakage-induced problems. Alpha particle-induced [10] bit line and sense latch hit fails are also very significantly reduced. A circuit schematic, a timing diagram, and a block diagram appear in Figs. 8 and 9.

The circuit operates as follows. The high-voltage sense latch restore pulse is RL. The circuit restore pulse ϕA is any pulse which is up sometime when RL is down; ϕA is chosen to be SET in this case, and initializes the circuit as follows:

1. Node NA is precharged to V_H.
2. Node NB is precharged to ground.

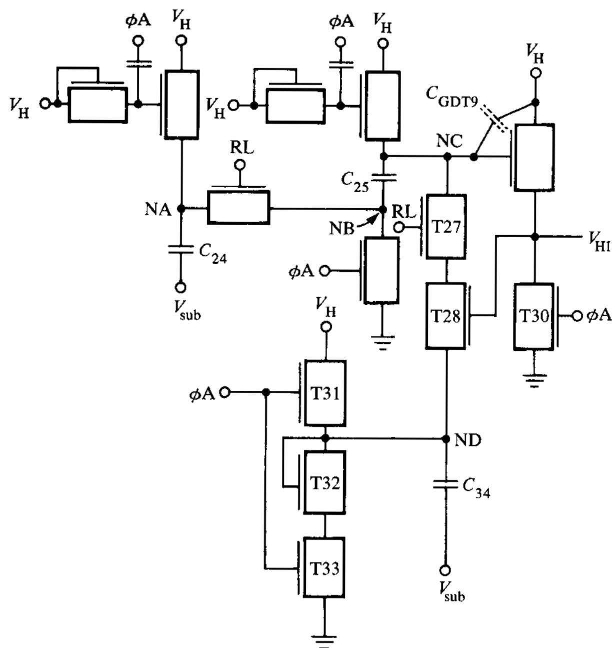


Figure 8 V_H buffer circuit for power supply stabilization function.

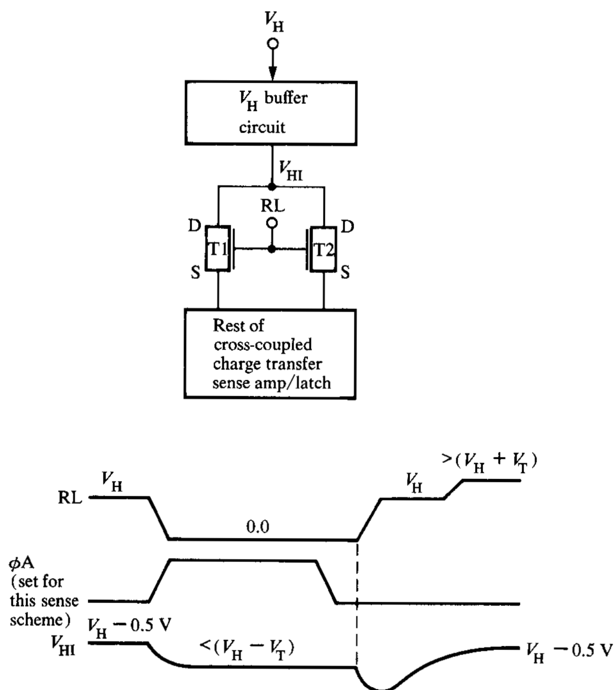


Figure 9 Block diagram and timing diagram for V_H buffer circuit.

3. Node NC is precharged to V_H.
4. Devices T31, T32, and T33 put a reference voltage on node ND.
5. Device T30, which is relatively small, pulls V_{HI} to $V_H - V_T$.

When RL comes up, two things happen. First, the effect of the sense latch node and bit lines that are at ground potential will pull V_{HI} to well below $V_H - V_T$. Node NC bootstraps and starts to charge V_{HI} back to V_H. Second, when V_{HI} gets to a V_T above the reference voltage on node ND, devices T27 and T28 turn on. Because

$$C_{34} >> \frac{C_{24}C_{25}}{C_{24} + C_{25}}$$

is chosen to be five times larger, node NC will be discharged. The reference voltage is picked so that the V_{HI} up level is $\leq V_H - 0.5$. At this point, node NC will be at $V_{HI} + V_T$ and leakage current will be provided for the sense latches and bit lines. The circuit will stay this way until the next cycle. Thus, a high-frequency V_H dip of up to 0.5 volts can be tolerated in this example. The only effect of an effectively permanent V_H dip on V_{HI} can be calculated as follows:

$$\Delta V_{HI} = \Delta V_H \left(\frac{C_{GDT9}}{C_{GDT9} + \frac{C_{24}C_{25}}{C_{24} + C_{25}} + C_{stray}} \right),$$

and the capacitive ratio can be designed to be small.

Acknowledgments

The author is grateful to L. G. Heller and the late D. P. Spampinato for many useful discussions, and to S. C. Lewis, the co-inventor of the V_H buffer circuit.

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Received May 12, 1979; revised November 13, 1979

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