# Design and modeling of equipment used in electrochemical processes for microelectronics

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*This paper presents an overview of the design of electrochemical processing equipment for semiconductor and related microelectronic manufacturing as well as a review of publications that are applicable to electrochemical wafer process equipment. We discuss several types of electrochemical processes applicable to wafer processing and the considerations that go into automated equipment for these processes. The design of such equipment is considered from a general perspective, as well as specifically with respect to several electrochemical processes. We also present results from reactor-scale modeling of several associated systems. The modeling results have been used to understand the effects of process parameters and hardware design on the results achieved.*

## Introduction

Over the last decade, electrochemical processes have become increasingly important in microelectronic manufacturing. Electrochemical deposition (ECD) has been used to deposit metals in the manufacture of magnetic recording heads and compound semiconductor chips for many years [1–9]. During the last decade, ECD copper deposition for multilevel interconnections has become accepted for mainstream silicon chip manufacturing, especially for high-speed logic devices [10]. The ECD copper process associated with damascene interconnect formation has done much to accelerate the learning related to electroplating processes and chemistry, and it is probably the ECD process most widely known in microelectronic manufacturing today. There are many other opportunities for utilizing electrochemical processes in the manufacture of semiconductor devices and other microelectronic components. In this paper, we identify some of them and discuss associated equipment design considerations.

Beginning in the early 1990s, automated wafer processing equipment was adapted for ECD applications on semiconductor wafers and related microelectronic workpieces such as thin-film recording head substrates. Integrating the automation of mainstream wafer processing equipment with ECD processes was a significant engineering challenge. In the years since, several application-specific types of electrochemical processing systems, each with its own specific requirements, have been produced. However, little has been published regarding the design of semiconductor-compatible electrochemical processing equipment [11].

## Design of microelectronic processing equipment

### *Process equipment*

Numerous considerations enter into the design of wafer processing equipment. The methodology for configuring a processing tool begins with the intended process sequence for the wafer, but throughput requirements, safety guidelines, and fab-specific[1] requirements also significantly influence its configuration.

#### *Process sequence*

The process sequence must be defined in the context of the particular application. Typically, microelectronics manufacturers want as many process steps as possible to occur within a processing tool while maintaining high throughput, up-time, and reliability. The final chamber layout is typically the result of an iterative evaluation of the constraints of wafer throughput, space, cost, chemical compatibility, and facility limitations.

[1] Fab: A facility for fabricating microelectronic chips.



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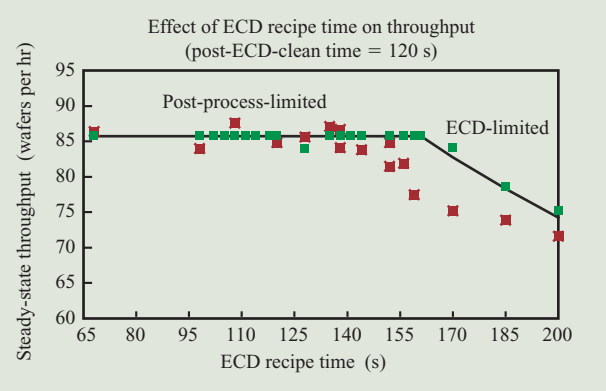



**Figure 1**

Comparison of throughput of an automated wafer ECD tool (six ECD chambers, four bevel etching/rinsing/drying chambers) with model predictions. (Red: empirical throughput; green: simulation prediction.)

Each processing tool must have a defined goal for wafer throughput. This figure is the basis for understanding the required number of each type of chamber in the tool as well as the performance requirements for automation. Electrochemical wafer processing tools are often configured with several different types of chambers to support a processing sequence. Besides the different reactor types for electrochemical deposition of various metals (e.g., copper, gold, platinum, nickel, nickel–iron, and solder alloys), there are chambers for pre-plate processing (pre-alignment, pre-wetting) and post-plate processing (rinsing/drying, edge bevel etching, and annealing). For a given process sequence, the processing time for one of the process steps establishes the bottleneck for wafer throughput. If a single chamber of a given type does not provide the required throughput, additional chambers may be added, with consideration of impacts to other potential throughput bottlenecks within the process sequence. **Figure 1** shows the performance of a copper deposition tool with six ECD chambers and four post-process chambers compared with simulation data. Two distinctly different regimes, representing different throughput-limiting operations, are demonstrated over this particular range of deposition "recipe" times. It is also apparent from the figure that the throughput of a complex manufacturing tool is not monotonic with process time, as might be expected.

### *Automation architecture*

The intended usage of the processing tool dictates the type of automation required within the tool. Simple research and development tools in laboratory environments may have no wafer handling automation if manual loading of the process chambers is acceptable. However, for tools in manufacturing environments, there is typically automation within the wafer loading or work-in-process (WIP) module, as well as within the main processing tool for transferring wafers between process stations. Additionally, tools in production environments may be required to incorporate an appropriate interface with intra-fab automation systems.

WIP automation consists fundamentally of transferring a carrier of product wafers from an ergonomic, operator-load position to a location at which the main transfer robot can move the wafers into the process stations. Such loaders typically incorporate wafer-mapping capability to inventory the wafers and detect wafers that may be improperly located in the carrier, as well as openers for the standardized pod carriers described below.

Additionally, some tool architectures incorporate an additional wafer-handling robot within the WIP area to transfer wafers to and from the main processing tool in order to remove the burden for these transfers from the main process-transfer robot. Although warranted for some applications, such additional wafer-transfer robots add additional cost, complexity, and footprint for the processing tool as a whole.

The size of the wafer or substrate, fab protocol, and cleanliness requirements determine the type of wafer carriers used in a tool. Tools for processing 300-mm-diameter wafers utilize standard SEMI (Semiconductor Equipment and Materials International) and standard FOUP (Front Opening Unified Pod) carriers, such that the electromechanical interface between the WIP automation and the FOUPs is well-defined. Those used for 200-mm-diameter and smaller-diameter wafers, however, have multiple options for carriers. There are environmentally controlled SMIF (Standard Mechanical InterFace) pods and numerous variants of open cassettes; in some instances, fabs are based on proprietary carrier designs. Finally, there are hardware alternatives for "bridge" WIP modules that allow a processing tool to accept different styles of carriers or wafers of different sizes. Although such designs provide alluring flexibility, they come at the cost of significant complexity, not only in the WIP hardware, but also in the chamber designs that must accommodate the different-sized wafers. In any event, the carrier type significantly influences WIP automation. The mechanisms to interface with the 200-mm and 300-mm standardized pod carriers add cost and complexity over open cassette loaders.

The design of the main wafer-transfer robotics within the processing tool is determined by several factors. Robot speed, working envelope, footprint, and method of wafer gripping are important considerations. A desired process sequence, with its corresponding chamber layout

and throughput requirement, dictates robot speed and size. Linear track-style tools offer the advantage of extendibility for larger working envelopes (more chambers) in a smaller overall footprint, but add the cost and complexity of the track axis of motion. Radial-style robots often have fewer axes of motion, but present a working envelope constraint that limits the number of chambers within the tool. Also, access to radial robots for repairs or preventive maintenance work can be difficult, since the robot is located in the middle of the tool.

Vacuum end-effectors are often used to transfer product wafers, but these present limitations for certain types of processes. Intermediate process steps that leave chemical residue or water on the backs of wafers can cause failure with vacuum end-effectors. Also, vacuum end-effectors, which inherently contact the back of the wafer, cause chemical or particle contamination and may be subject to dropping wafers if the wafers are held beneath the end-effectors with vacuum. Edge-gripping end-effectors can surmount the shortcomings of the vacuum end-effectors by contacting the wafer only within a permitted exclusion zone at the perimeter of the wafer. The mechanical gripping employed by edge-grip designs is tolerant of residual chemistry on wafers, and back-side contamination is minimized, since the end-effector does not come into contact with the back of the wafer. An additional benefit of an edge-grip end-effector is its ability to register the wafer in position repeatedly—a tremendous benefit in maintaining reliable wafer transfers between chambers. However, edge-grip end-effectors are typically more complex than vacuum end-effectors, and their larger size can hinder robot motion or access in some situations.

A wafer pre-aligner is another automation component that affects tool design. Such devices position a wafer precisely and/or orient it by its notch or flat, depending on the nature of the wafer. This alignment is important if a process chamber requires the wafer to be in a predetermined orientation. For some electrochemical deposition processes, for instance, the electrical contacts have seal geometry that conforms to the flat of the wafer. Also, in the case of magnetically oriented alloy deposition, the precise orientation of the wafer with respect to the magnetic field in the chamber is critical to the process results. In many applications of electrochemically deposited films on round wafers, however, it is not necessary to orient the wafer to the process chamber, and pre-alignment is not necessary. Eliminating a pre-alignment step offers benefits in the form of a faster process sequence, reduced cost, and smaller tool footprint.

Interface to intra-fab automation is a consideration for tools in manufacturing environments with automated carrier delivery systems. The SEMI E15 standard defines the mechanical and control interface expected on tools incorporating 300-mm FOUPs [12]. Interface standards for 200-mm SMIF pods are established with SEMI E19 [13]. Fabs utilizing open cassettes do not typically have automated delivery of the cassettes to the tool. For fabs without intra-fab wafer-carrier delivery, wafer carriers are delivered to the tool manually for 200-mm and smaller wafers and on carts for 300-mm FOUPs. Standard docking interfaces between process tools and such carts have been established to facilitate ergonomic loading and unloading of pods [14].

### *Safety/environmental considerations*

Safety is a paramount consideration in tool design. SEMI standards S2 [15] and S8 [16] establish guidelines for safe and ergonomic tool design, and many microelectronics manufacturers have additional internal design protocols. Third-party verification of these standards is expensive, and the time required for these verifications must be accommodated in the tool manufacturing and test schedule. Despite the extensive and thorough nature of these guidelines, in order to avoid misperceptions, there are still areas of ambiguity that must be discussed by customers and equipment suppliers early in the tool design process.

Safety guidelines can significantly influence the choice of materials for construction of a processing tool. Materials considered to be fire-safe, which are required by some standards and insurance companies, are significantly more expensive than materials that are typically used in the industry, and chemical compatibility of approved materials must be evaluated carefully. The use of incompatible chemical combinations within a tool necessitates thoughtful design to segregate drains, exhausts, and containment areas. Certain situations may warrant physically separating sections of the tool to prevent mixing of incompatible chemicals.

## *Analysis equipment*

In certain processes, the management of electrolyte chemical concentrations is critical to ensure consistent results. Automating the management ensures consistent control and allows operators to focus on processing. The electrolyte components can typically be divided into two general groups: organic and inorganic. Of primary interest are the metallic ions reduced at the cathode. The concentration of these metal ions can be maintained either by using consumable anodes or by periodically adding concentrates to the electrolyte bath. Organic components are typically added to the electrolyte to

modify the properties (composition, step coverage, grain size, etc.) of the deposited film. These organic components tend to have decomposition rates that are dependent on both applied voltage and elapsed time (bath age).

The most basic requirement for an automatic control system is the ability to dose or replenish the chemicals consumed during the normal operation of the plating bath. This dosing is normally based on the applied charge (usually measured in amp-minutes), elapsed time, and analysis results. Next, the system must be able to perform automatic analysis, including sample extraction if necessary, of all critical bath components. The system controller then calculates replenishment volumes on the basis of the analysis results. More advanced systems also automatically adjust the replenishment rates for the dosing on the basis of accumulated charge and elapsed time.

A number of methods have been developed for analyzing the inorganic and organic components in the electrolyte. The integration of these methods into an automated bath control system presents some unique requirements. An automated analyzer must require very little support to maintain repeatable analysis performance. Automated analyzers are usually set to run as often as possible to obtain close-to-real-time concentration data. Some priorities may be set so that components that tend to change concentration more rapidly, or are more critical to the process, are analyzed more frequently. Nevertheless, minimizing sample consumption is also a critical factor in designing and selecting analysis techniques. The cost of a particular technique, in initial capital equipment, operations, and in the product at risk between analyses, must be weighed against the performance of the analysis and the cost of the chemicals consumed during the analysis.

The methods that have been used or considered for automated plating-bath analysis include titration (potentiometric, colorimetric, or pH), high-performance liquid chromatography (HPLC), X-ray fluorescence, electroanalytical techniques (see below), spectrophotometry, pH monitoring, conductivity monitoring, oxidation-reduction potential (ORP) monitoring, mass spectrometry, and atomic absorption [17].

Titration, one of the oldest and most reliable analytical techniques, is commonly used for the analysis of the inorganic components (metal ions, acid content, trace ions, etc.) in automatic systems. The advantage of titration analysis is that it can easily be automated, and it is usually very accurate and precise. However, it can require a large amount of chemical usage and may require long cycle times.

Electroanalytical techniques, such as cyclic voltammetric stripping (CVS) or pulsed cyclic galvanostatic analysis (PCGA), are often used for the analysis of organic bath components [18–20]. These methods are based on changes in electrodeposition kinetics in the bath sample with respect to the concentration of organic additives. Although this approach is not a direct measurement of the organic species present, it can be quite accurate and reliable. It has disadvantages similar to those of titration methods: A sample must be extracted and consumed to facilitate the analysis.

A number of direct, real-time measurement techniques do not require sample consumption. Using a pH probe is probably the most well known and widely used of such techniques. Ion-specific electrodes, ORP electrodes, and plating-bath conductivity probes are also commonly used. Spectrophotometric techniques can also be used for on-line inorganic and organic analyses.

HPLC and various mass spectrometry techniques are most often used in off-line bench-top applications. They can be configured for automatic on-line analysis, but their use is limited because of high initial capital cost and maintenance requirements [17].

## Electrochemical processes for microelectronics

Many types of electrochemical processes can be used in microelectronic component manufacturing. In addition to metal deposition using electrolytic and electroless processes, electrophoretic deposition, anodization, electrochemical etching, and electropolishing processes are also used. Each of these processes has its own unique requirements that affect associated equipment design and operation.

It is important to understand the strengths and limitations of a particular reactor in order to optimize its performance for a particular application. The same reactor does not work equally well for all electrochemical applications. Reactors that can be utilized for the electrochemical deposition of metals include rack platers, paddle cells, fountain reactors, and other unique configurations designed for single-wafer or batch processing.

Generally, the metal ECD processes utilized in microelectronic manufacturing can be divided into through-mask-deposition and blanket-deposition types. Each has its own specific design requirements and operational characteristics, and there are specific applications within each category that have narrower sets of requirements.

### *Through-mask metal deposition*

Through-mask deposition is an additive process that has been used for many applications in microelectronic

processing [2–7]. A patterned photoresist (or other dielectric) mask is used to prevent deposition where it is not desired. The processing equipment must be able to handle multiple materials exposed on the surface, and some consideration must be given to making electrical contact with the conductive seed layer, which is generally beneath the mask material. The electrical contacts must be designed to penetrate the photoresist, or the photoresist must be removed in the areas where the electrical contacts touch the seed layer. In addition, these processes are affected by the pattern density at the wafer, die, and feature scales [21–23]. If photoresist or a similar polymeric material is used as the plating mask, the surface must typically undergo some sort of prewetting process to ensure that liquid is able to fully wet the features despite the sometimes hydrophobic nature of the plating mask.

### *Blanket metal deposition*

In blanket metal deposition processes, there is no significant masking of the substrate to be plated. Such deposition is utilized when it is desirable to have a fully metallized surface, such as for back-side metallization of GaAs wafers, or where a subtractive method, such as chemical mechanical planarization (CMP) or masking and etching, is to be used to define the areas where metal is removed. The copper damascene interconnect application is becoming the most prominent example of this type of process [10, 24–28].

The electrochemical reactor, in which a product wafer is introduced to electrodeposition chemicals and an electric field (if applicable), includes the wafer fixture with electrical contact and the power supply, and provides both the fluid recirculation path and mounting for the counter electrode(s). Beyond these basic requirements, an electrochemical reactor often provides a variety of other functions. These include wafer-fixture automation, wafer-fixture spinning, mechanisms such as an agitator paddle to affect the hydrodynamic boundary layer at the wafer surface, features to locally affect the hydrodynamic boundary layer, electric-field-shaping elements, auxiliary electrodes, process-monitoring sensors, evolved-gas mitigation features, and wafer-contact maintenance features. A secondary process section is often incorporated into the reactor to allow for pre- and/or post-deposition surface treatment of the wafer. The features that are incorporated into the reactor are determined in large part by the specific process to be performed in the reactor.

### *Copper damascene interconnects*

Copper damascene interconnects have been utilized in the semiconductor industry since the mid-1990s [28–30]. In this application, trenches and vias are etched into a dielectric to define intralevel and interlevel interconnections. Barrier and seed layers are applied to this patterned substrate and copper is electroplated to fill the features. This process requires extremely good repeatability and good uniformity control across the wafer. The contact to the wafer must be extremely repeatable and circumferentially uniform, and the reactor should allow for uniform deposition throughout the entire process.

Because of the relatively thin (less than 2-$\mu$m-thick) deposition, it is possible to use an exposed electrical contact to the wafer. The deposited metal layer covers the contact as well as the wafer surface and provides excellent electrical conductivity; it is detached from the wafer at the end of the process. It is also possible, because of the reversible nature of copper deposition in acid solutions, to reverse the polarity of the current at the contacts after removing the wafer and strip the copper from the contacts before plating the next wafer [31, 32]. This eliminates the need for a seal to prevent deposition onto the contacts. Some of the concerns associated with fluid seals in this application include the complexity of removing a wet seal from the substrate without pulling liquid behind the sealing surface through capillary forces, trapping of residual acid solution during a rinse cycle, and intrusion of the seal and contact elements into the usable area of the semiconductor wafer. Failure to provide a robust hardware design can lead to etching or electrolytic removal of the copper seed layer locally near the contact points, or to oxidation or corrosion of the freshly plated surface. Also, the added profile of a seal protruding beyond the wafer surface can make immersing the wafer in solution and releasing trapped air more difficult, leading to the development of defects on the wafer surface [33].

Another important characteristic of the copper damascene process is that the barrier and seed-layer resistance is appreciable at the beginning of the process, and the total film resistance decreases as the process proceeds. This causes a voltage drop between the contact terminals (at the edge of the wafer) and the center of the wafer, referred to as the *terminal effect* [34–36]. This effect leads to a variation in the applied current density across the wafer in conventional reactors, causing variations in fill capability, additive incorporation, grain size, and thickness.

In addition to this spatial variation, the terminal effect is time-dependent in a typical copper damascene process because the conductivity of the film stack increases during the deposition [37]. To compensate for the changing terminal effect, the reactor must be designed so that the radial potential-field distribution can be adjusted over time through the deposition process [38]. **Figure 2** shows the current density distribution across a wafer (center to edge) as the deposition proceeds. In Figure 2(a), we see

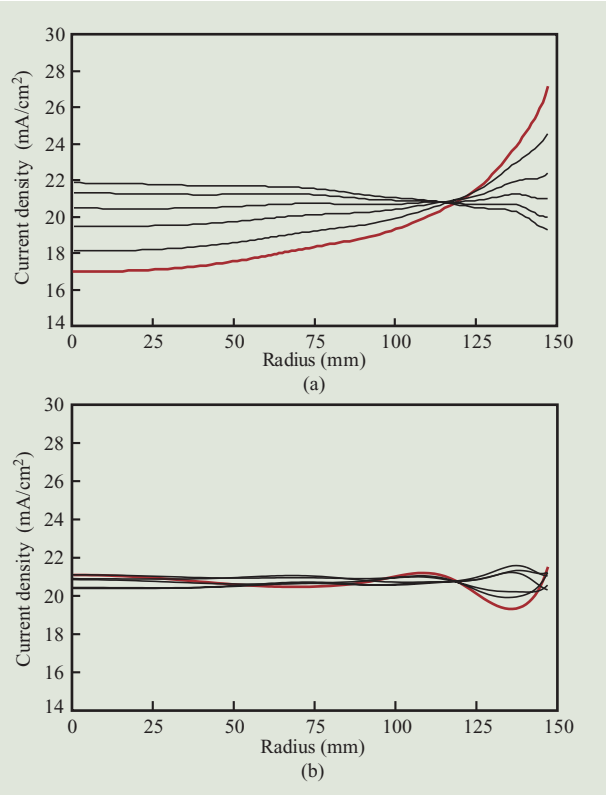



Figure 2

Current density profile evolution during blanket wafer deposition. Red curves indicate initial current density profiles. (a) Profile at constant electric potential throughout deposition. (b) Profile achieved via dynamic current density control providing uniform current density throughout deposition process.

the terminal effect causing high current density at the edge of the wafer during the early part of the deposition process; the effect gradually decreases as the deposition proceeds and the conductivity of the wafer surface increases. When using a (conventional) reactor that operates in this manner, it is necessary to design the hardware so that the primary current distribution results in a center-fast deposition rate in order to compensate for the terminal effect and produce uniform target film thickness. To achieve the profile of Figure 2(b), dynamic current density control was utilized to provide a uniform current density at all points on the wafer throughout the entire deposition process. This was accomplished by using a reactor in which the radial potential-field distribution is adjusted over time through the deposition process to maintain a uniform current density distribution despite the changing terminal effect [39]. This results in a dramatic reduction in the current density (plating rate) variation across the wafer throughout the deposition.

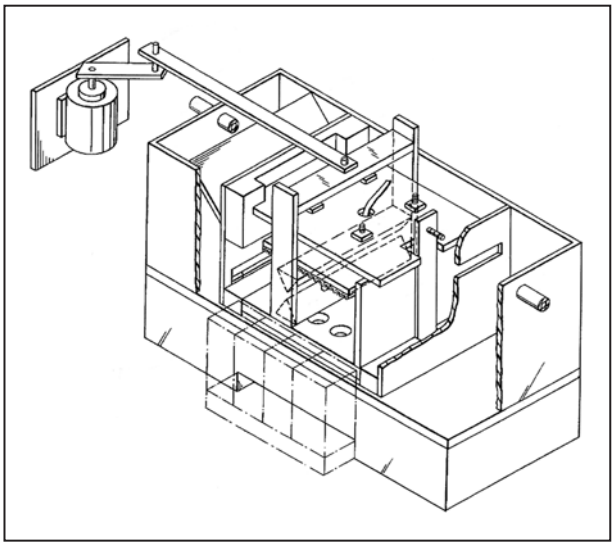


Figure 3

Paddle cell, from U.S. Patent No. 4,102,756 [2].

***Magnetic alloy deposition***

Electrolytic deposition of magnetic alloys has been used for more than thirty years in the fabrication of magnetic recording heads and other devices. Film deposition is performed in a magnetic field that is oriented in one direction parallel to the plane of the wafer in order to provide an easy axis of magnetic alignment. This makes it difficult to rotate the wafer during the deposition, because such rotation would necessitate rotating the >1000-gauss field required synchronously with the wafer. To address this requirement, paddle cells were designed for magnetic alloy deposition [1, 2]. **Figure 3** shows a paddle cell, as presented by Castellani et al. [2]. The other critical factor in magnetic alloy deposition is composition control. It is necessary to have uniform and controlled composition of the binary and ternary alloys across the entire surface of the wafer to ensure consistent device performance.

In the paddle cells that are typically employed in magnetic alloy electroplating, use is made of a single or double triangular paddle in close proximity to the substrate surface to provide fluid agitation [1, 2]. The paddle typically scans linearly across the surface of the substrate at a frequency of the order of one cycle per second. This mode of operation leads to the formation of vortices in the solution behind the trailing edge of the paddle, which provide the major source of fluid agitation in the system. Depending on the paddle shape and speed, the vortices can create standing waves in the reactor cell, affecting the concentrations of the species present in the plating bath [40]. The effect of this type of agitation can be seen in **Figure 4**, which shows simulated results of the

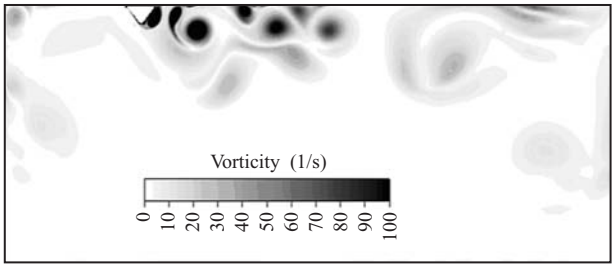



Figure 4

Simulated fluid vorticity at the moment paddle reverses direction.

fluid vorticity at the moment the paddle reverses direction at the left stroke boundary (at $t = 4.285$ s), preparing for the fifth stroke in the simulation. In this simulation, the wafer is at the top surface of the reactor (face down) and the reactor fluid depth is 150 mm, with a triangular paddle having a base of 16.3 mm and a height of 10 mm. The simulation was carried out by utilizing a commercial simulation package [41], assuming that the paddle travels at a peak velocity of 39 cm/s, with a stroke period $T_p$ of 1.07 s required to traverse the entire stroke (both directions) of 19 cm in each direction [40]. The vortices that are shed at the trailing edge of the paddle provide agitation at the wafer surface; the resulting instantaneous metal diffusion layer thickness distributions in a plating bath are shown in **Figure 5**. If the system is operated in a way that produces standing waves or stationary eddies, the nonuniformity of diffusion-layer thickness seen in the figure can produce variations in thickness and/or composition across the substrate.

Operating parameters such as paddle-to-cathode spacing and paddle speed can be used to adjust the mass-transfer characteristics of the paddle cell. Several researchers have investigated the effects of changing various parameters on the mass transfer of metal ions in paddle cells [42, 43]. The effects of changing these parameters can be seen in **Figure 6**, as represented by the average mass-transfer coefficient. Figure 6(a) shows the variation in the mass-transfer coefficient with the paddle-to-substrate gap. In this case, the simulation was for a 10-mm-tall by 4-mm-wide rectangular paddle with a peak paddle speed of 26 cm/s, and with the wafer located at the top of the reactor. The fluid depth was assumed to be 150 mm and the paddle stroke length 50 mm. The mass-transfer coefficient was computed and averaged over many paddle cycles and then compared with experimental values of Schwartz et al. [43]. Figure 6(b) shows the variation in the mass-transfer coefficient with paddle speed. The simulation was for a 30-mm-tall by 4-mm-wide rectangular paddle with a fluid depth of 150 mm, a paddle-to-substrate gap of 10 mm, and a paddle stroke

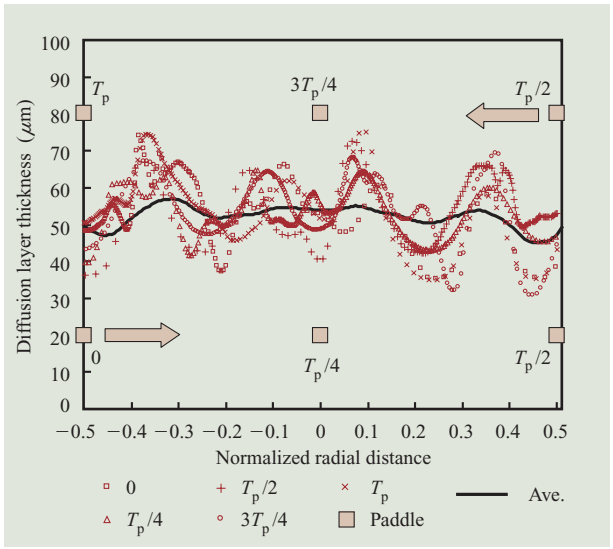


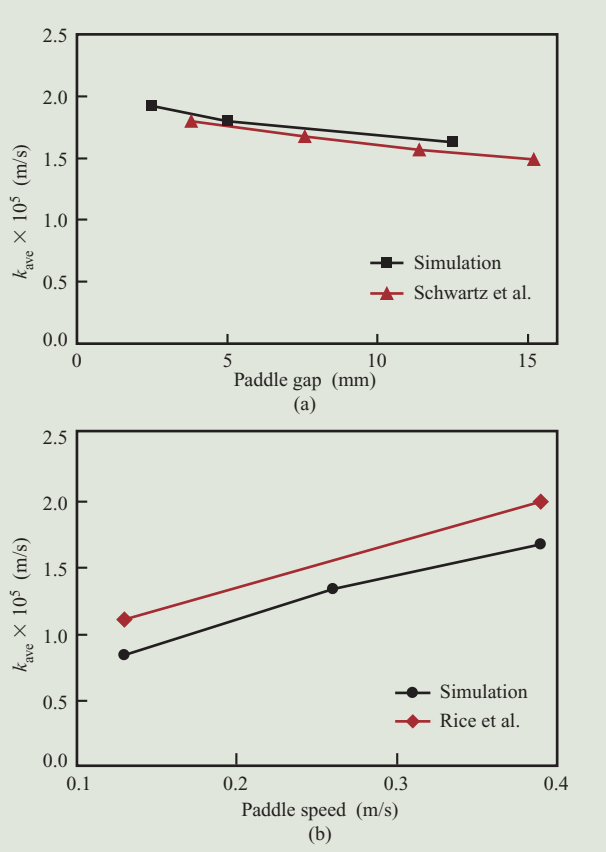

Figure 5

Calculated diffusion layer thickness distributions at the fifth paddle stroke.

length of 190 mm, again with the wafer located at the top of the reactor. The simulation data values are compared with the experimental values of Rice et al. [42]. The data in Figure 6 show that reducing the paddle-to-substrate gap and increasing the paddle speed can reduce the diffusion layer thickness, but there are typically limitations because of the mechanics of the reactor operation. The agreement seen between the simulation trends and the experimental data indicates that a two-dimensional model of the fluid dynamics of a paddle reactor can be used for initial evaluations of different design modifications (paddle-to-substrate gap, paddle speed, etc.) in reactor design.

### *Chip packaging electrochemical deposition*

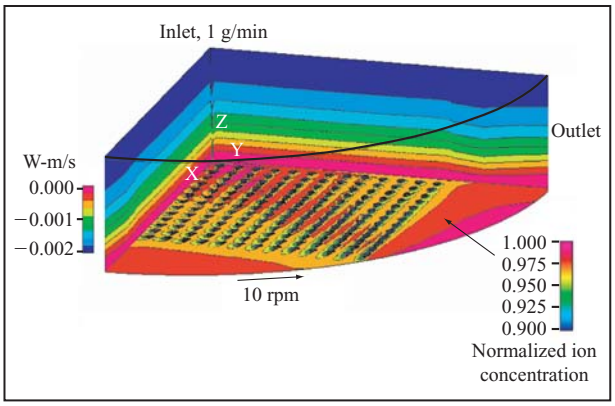
Processes such as solder bump plating for flip-chip or controlled-collapse-chip-connection (C4) processes, redistribution of I/O pads, and related processes are also gaining use in the semiconductor and related industries. The important factors are typically thickness uniformity, deposition rate, and alloy composition control if alloys are being deposited. Thickness uniformity is required in order to ensure that all features on the die will make connection to the substrate on which it is to be mounted. This requirement is sometimes referred to as the "coplanarity" of the finished bumps, since they need only define a relatively planar surface, as opposed to being perfectly uniform. The layers used for these applications are typically fairly thick, so high deposition rates are important for throughput, especially in the single-wafer




## Figure 6

Dependence of average mass-transfer coefficient on (a) paddle-to-substrate spacing; (b) paddle speed. Reproduced from [40], by permission of The Electrochemical Society, Inc.

equipment that is typically utilized for automated wafer processing. It is not unusual to use ECD processes that have deposition rates between 1 and 5 $\mu$m/min [44–47]. Composition control is important when solder alloy is deposited in order to ensure that the alloy consistently melts at the correct temperature. Both the deposition rate and alloy composition can be strongly affected by the mass transfer in the reactor. Limiting current density (LCD) simulations can be used to obtain an estimate of the maximum practical deposition rate (typically $<50\%$ of LCD) as well as the spatial distribution of mass-transfer effects in the system; the latter can lead to compositional variations. Computational models can be used to evaluate these effects during the ECD reactor design [48–50]. **Figure 7** shows a computational grid used in the three-dimensional modeling of metal ion concentration in through-mask plating. Because of the three-dimensional diffusion effects coupled with the localized consumption of metal ions from the solution, a lower limiting current density is seen at the center of the




## Figure 7

Impinging velocity (W) and normalized ion concentration contours for three-dimensional simulation of limiting current density in through-mask ECD applications.

wafer than at the edge, as shown in **Figure 8** [51]. (This is because there is replenishment by solution at or near bulk concentration in the off-center features, which raises the limiting current density in comparison with the rotating disk electrode case, in which the entire surface is plated [52]. This means that the mass transfer of metal ions at the center of the rotating wafer is likely to limit the practical deposition rates in such systems, and that the composition could vary from center to edge if attention is not paid to system design and its interaction with process parameters. In addition to the factors mentioned above, gas management is important in ECD systems for through-mask deposition processes in order to prevent gas bubbles from forming in resist openings, thus preventing deposition.

### *Electrochemical etching*

Electrochemical etching can be used to remove metal layers such as seed layers used in through-mask deposition. This process can be carried out in conventional ECD equipment, but with a few additional considerations. It is important to understand what materials lie beneath those to be removed, especially since it is usually important to maintain a conductive layer that is not removed in order to allow current flow and ensure complete removal of the layer(s) being etched. It may also be important to control the uniformity of the removal rate in order to prevent isolating large areas of unetched metal. These electrolytic processes provide an opportunity for endpoint control by monitoring the current/voltage characteristics during processing.

A specific type of reactor, which uses jets of electrolyte and a scanning cathode, as shown in **Figure 9**, has been developed for electrochemical etching and milling

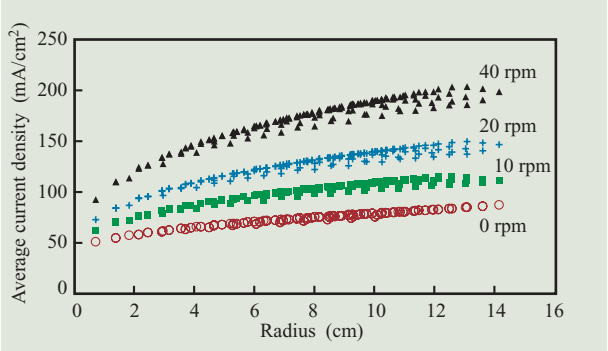



Figure 8

Calculated limiting current density across a wafer for a through-mask electroplating application as a function of wafer rotation rate.

processes. This reactor has been described elsewhere in detail, and has been incorporated into fully automated wafer processing equipment [7, 53, 54].

***Electropolishing***

Electropolishing is a form of electrochemical etching in which the removal process produces a smoother metal surface as the etching proceeds [55]. Electropolishing has received some interest with respect to microelectronic applications such as reducing the need for chemical-mechanical polishing (CMP) in the damascene copper interconnect process [56]. Electropolishing is not a significant process in wafer processing, but can be performed with equipment very similar to that used for electrochemical etching.

***Anodization***

Another electrochemical process that can be used in microelectronic manufacturing, anodization, is the anodic oxidation of a material (usually a metal) to produce another material, such as a metal oxide. This process has been used to grow tantalum pentoxide films from tantalum or tantalum nitride precursor films [57]. Such films can be used as high-dielectric-constant capacitor dielectrics when passive elements are integrated on semiconductor chips. The thickness of the anodized film can be controlled by setting the maximum process voltage. **Figure 10** shows scanning electron micrograph cross sections of samples with different dielectric thickness prepared from the same precursor film. Thickness uniformity is typically fairly easy to achieve because the high resistance of the film being formed acts as a ballast resistor; hence, uniformity requirements do not have a large impact on equipment design. The current follows the path of least resistance, which ensures oxide growth in thinner (less resistive) areas. The electrical contact to the wafer is an important consideration

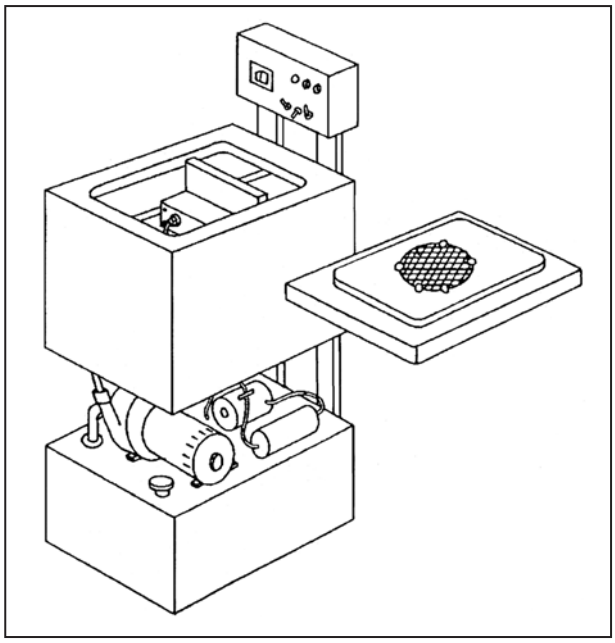


Figure 9

Electrochemical etching chamber, from U.S. Patent No. 5,486,282 [53].

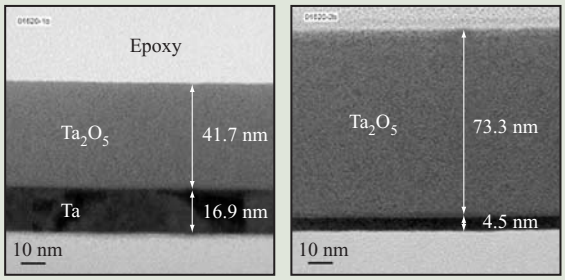



Figure 10

Cross sections of $Ta_2O_5$ films formed by anodization of Ta. Both films had the same thickness of Ta as the precursor film, but the deposition voltages were different.

because it is important to make sure that the passive oxide film does not form between the contact and the conductive metal layer that must distribute current across the wafer. Gas management is also an important consideration because gases can be formed at the wafer (anode) surface as well as at the cathode.

***Electrophoretic deposition***

Electrophoretic deposition has been used to deposit both positive- and negative-tone photoresists for

microelectronic applications [58, 59]. The advantage of the process is that it can provide very conformal deposits over three-dimensional structures that may be hundreds of microns in size. The materials used for the electrophoretic deposition of photoresist are emulsions of organic materials in aqueous solutions, and they must be treated carefully to avoid adversely affecting the solution. This makes the design of the fluid flow system important. In addition, gases are typically generated at the electrodes; hence, gas management must be considered in designing electrophoretic deposition equipment.

### *Electroless deposition*

Electroless deposition is gaining interest in semiconductor and related applications. This type of deposition utilizes complementary electrochemical reactions to cause the deposition of metals. The oxidation of a reducing agent supplies the electrons necessary for reducing metal ions to their metallic state [60]. This encompasses both immersion (substitution) deposition reactions and autocatalytic reactions. Immersion deposition is the case in which a metal on the substrate surface is oxidized (and solvated) to provide the electrons for the reduction and deposition of a more noble metal from the solution, and is self-limiting at the point that the less noble metal is completely covered. In autocatalytic deposition, a reducing agent is used in solution as the electron source. Electroless deposition is useful in cases in which it is desirable to deposit metal on nonconducting surfaces or deposition that is selective to underlying materials is desired. Current applications of interest in the microelectronics industry include the deposition of ternary diffusion barrier alloys on copper lines [61–66], deposition of nickel for contact metallurgy, electroless copper deposition for seed-layer applications, and various processes for wafer-level packaging [67–70].

The equipment utilized for electroless deposition processes is not overly complex; it typically consists of immersion reactors with much attention paid to flow-control or solution handling and process sequencing. Critical factors affecting electroless deposition and the design of reactors include temperature control and uniformity, flow uniformity, and equipment configuration complexity. It is extremely important to maintain elevated temperatures (as high as 90°C) without producing localized hot spots that may lead to autocatalytic deposition on the reactor components. Also, because of the inherent instability of electroless deposition solutions, close attention must be paid to the reactor and plumbing layout within the process tool. Subtle changes in the configuration can have dramatic effects on process and chemistry stability. This instability has even led to the consideration that reducing agents be added immediately before use and to designing reactors for "single-use chemistry" (the processing of one wafer at a time, with no chemical re-use). The processes typically consist of several cleaning, activation, and deposition steps; hence, the concerns described in the equipment design section related to system configuration and throughput tend to be very important [60–68, 71, 72].

## Summary

Building on experience from the broad field of electrochemistry, there have been considerable advances in the understanding of the fundamentals of electrochemical processes and the design of electrochemical processing equipment for microelectronic applications. There are still many opportunities for the increased use of electrochemical processes for such applications. The processes required, although similar in some respects, have their own specific requirements and design considerations. We have highlighted some of these in order to provide a general understanding of the considerations that go into their development. We have also shown how modeling can be used to guide and accelerate the design process and to reduce the number of equipment iterations required to build reactors optimized for a particular process.

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