MODEL 10092 ATbus HARDCOPY INTERFACE

IKON CORPORATION

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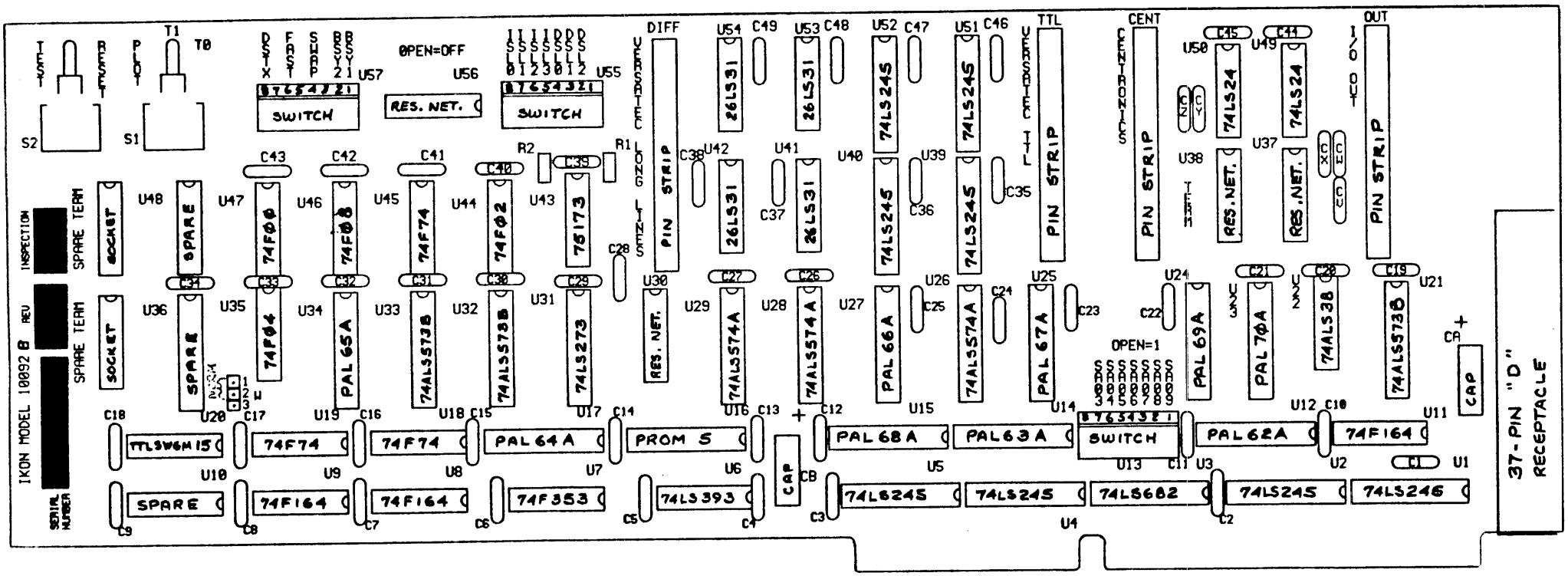

IKON Model 10092 Circuit/Switch Layout

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Introduction

The IKON Model 10092 Hardcopy interface is a very high performance DMA interface for hardcopy output devices including:

Versatec Electrostatic Plotters

Tektronix Color Copiers

Imagen Laser Printers

Any Other Centronics or Versatec-compatible Device

The 10092 is fully compatible with Versatec's "Green Sheet" interface specification and can support both TTL and differential mode printer/plotters. It also has the ability to drive any device which conforms to the Centronics interface specification. It includes sufficient flexibility to accomodate devices that deviate from the Centronics specification -- in particular it is fully compatible with the Tektronix color copier interface and supports data streaming, compressed timing, and the Tektronix preferred cable terminations.

A sigle external 37 pin "D" connector is used to connect to the attached device, with Versatec/Centronics selection done via an internal jumper cable.

Data transfers to the hardcopy device may be done via DMA for maximum speed and efficiency. DMA transfers use AT bus I/O channel DMA and may be byte or word transfers, depending on the DMA channel selected. Byte swapping may be selected for word DMA transfers. (Especially useful with 68xxx processors which do not conform to the byte ordering format that is used on the bus.) DMA channel and interrupt level are selected by DIP switches in the 10092, and may be any DMA channel and interrupt level available on the bus.

A feature of particular importance to field installation personnel is the ability of the 10092 to exercise the attached device without CPU intervention. Operating a pair of board-mounted toggle switches will cause a test pattern to be sent to the attached device. The pattern is PROM-driven, with a choice of two separate patterns per PROM, and the option of customizing the PROM for a particular customer and application. Typical PROM patterns would be a repeating ASCII pattern for devices with print capability, and a color bar pattern for Tektronix, and other color hardcopy devices. Versatec compatible devices may also be exercised in plot mode using the force plot test switch.

Outgoing data and control line drivers are high-drive bipolar devices. The internal TTL and Differential Versatec connectors are driven by separate devices to allow optimizing device type for the particular interface. Centronics connector drivers are capable of sourcing and sinking high currents and can drive the Tektronix-preferred 95 ohm to ground termination load. Cable receivers are true Schmitt triggers with r/c integration for maximum noise rejection. The Centronics connector termination resistors are socket-selectable.

General Specifications

Compatible with IBM personal computer AT bus.

Device Interface

"Data Streaming" capability for Tektronix color copiers.

Diagnostic capability allows testing/exercising of device and cable without CPU intervention.

Device test pattern determined by an on-board PROM which may be custom tailored to device and user requirements.

CPU accessible diagnostic "hooks" allow exercising board and verifying driver software without device attached.

Directly supports all Versatec "Green Sheet" compatible products in both TTL and Differential (long-line) modes. Long-line capability to 300 meters.

Supports any Centronics-compatible device.

High-current output drivers can drive any TTL-type termination. Can source 30ma and sink 48ma.

Socketed input terminators allow matching device manufacturer's preferred terminations.

All inputs received by Schmitt-triggers with r/c integration networks for maximum noise rejection.

On-Board Registers

The Model 10092 on-board registers occupy an 8 byte block of addresses which may be located anywhere in the I/O channel I/O address space. (100 - 3FF hex)

The low order 3 bits of the slave address are used to determine which on-board register is being addressed. The remaining address bits are decoded to determine when the board is being addressed.

On board registers may be accessed only as bytes.

On-Board Register Addressing

xx switch-selectable -- addresses in hex

Address	Write	Read
xx0	Latched Functions	Latched Functions
xx1	Pulsed Functions	Interface Status
xx2	P I/O Data Out	Diagnostic Data In
xx3		Device Status
xx4		Interface Strapping
xx5		
xx6		
xx7		

Register Formats

Bit 7 is the MSB for all registers.

Latched Functions

Bit	Name	Function
07	TENB	enable internal test mode
06	TVRY	assert test ready
05	LRST	latched device reset
04	DMON	DMA enable/disable
03	DSTR	Data Streaming mode
02	IENB	Interrupt enable/disable
01	VSPP	set Versatec spp mode
00	VPLT	set Versatec plot mode

The state of the Latched Functions register may be read back at the same address at which it is written. It is the only interface register that is truly "read-write".

All Latched Function bits are cleared to 0 by a bus initialize (RESET DRV) or by pulsing MCLR in the Pulsed Functions register.

TENB When set to 1 enables internal test mode. In this mode the interface may be tested and exercised without a device attached. If TENB is set, the TVRY bit may be used to simulate transitions on the Versatec READY- input. As this is done the Diagnostic Data register may be used to examine the flow of device data through the interface using both the DMA and Programmed I/O output modes. Ready interrupts may also be tested and exercised using these bits. The hardcopy device should be disconnected from the interface for this diagnostic mode to function correctly. Setting TENB to one disables Centronics and Versatec differential modes if selected, and causes the interface to operate in Versatec TTL mode, although VTTL mode

will not be indicated in the Device Status register unless specifically selected by board strapping.

TVRY — In test mode (TENB set to one), this bit may be used to set and reset the Versatec READY- input. See TENB above.

LRST — The reset signal to the device will be asserted as long as this bit is a 1. This is useful for Centronics-compatible devices that require a reset signal longer than the 550ns pulse generated when the MCLR bit in the Pulsed Functions register is used.

DMON — Setting this bit to a one allows the interface to request service from the system bus DMA logic. Setting it to a zero inhibits DMA. It will be cleared during system reset, by using the MCLR bit in the Pulsed Functions register, or by reaching terminal count (end-of-range) during DMA. If cleared by end-of-range when using a word DMA channel, it will clear before the last byte of the pair is output, and should not be used as an indication that the interface is ready for another operation. In all cases, the DIRY bit in the Interface Status register should be used for this purpose.

DSTR — This bit provides compatibility with the "data streaming" mode used by some Tektronix color copiers. If it is set, the interface will not wait for a handshake when transferring data bytes to the device. Data bytes may be either 7 or 8 bit values as selected by the data streaming mode switch. (See the description of the data streaming mode switch in the Hardware Options section of this manual.) Full handshaking is performed for any control bytes in the data block. See the appropriate Tektronix documentation for further information. This mode should only be used with devices which support a compatible data transfer mode.

IENB — Setting this bit to 1 enables the interface to generate an interrupt request whenever the device and interface become ready for further commands and/or data. The interrupt line driven is determined by swiches.

VSPP — This bit selects Versatec simultaneous print/plot

mode when set, and normal print/plot mode when reset.

VPLT This bit selects Versatec plot mode when set, and print mode when reset.

Pulsed Functions

Bit	Name	Function
07	SACK	software ack
06	MCLR	master clear interface only
05	RINT	reset interrupt flag
04	REST	device reset only
03	VCLR	Versatec clear
02	VTFF	Versatec form feed
01	VEOT	Versatec EOT
00	VLTR	Versatec line terminate

All Pulsed Function register bits generate a 550ns pulse to the associated device/function when written as a one.

SACK — The SACK bit simulates an ack pulse from the attached device (actually a true-false-true sequence if a Versatec attached). It may be used to re-synchronize the interface internal ready logic with the external device after an error.

MCLR — Writing a one to the MCLR bit resets all interface logic, but does not reset the attached device. The Latched Functions register bits will all be cleared to zero and device test mode (selected by rear panel toggle switches) will be terminated.

RINT — The RINT bit resets the interface IFLG (interrupt flag) bit in the Interface Status register when written as a one. It may be used within an interrupt handler to clear the condition that caused the interrupt.

REST — Writing a one to the REST bit resets the device, but does not affect the interface logic. If a reset pulse longer than 550ns is required by the device, it may be generated by using the LRST bit in the Latched Functions register.

VCLR Writing a one to this bit sends a CLEAR- signal to the Versatec.

VTFF Writing a one to this bit sends a FORM FEED- signal to the Versatec.

VEOT Writing a one to this bit sends an EOT- signal to the Versatec.

VLTR Writing a one to this bit sends a REMOTE LINE TERMINATE- signal to the Versatec.

The above commands to the Versatec connector should only be issued when the attached device and the interface are ready. They cause the device to go not ready for a device dependent amount of time. If interrupts are enabled, an interrupt will be generated when the device and interface become ready after receiving one of these commands. Interrupts, or polling of the DIRY bit in the Interface Status register should be used to interlock issuing of device commands and transmission of Programmed I/O or DMA data.

Programmed I/O Output

A byte of data written to the Programmed I/O Output register will be transmitted to the attached device using the same handshake logic as DMA transfers. P I/O output transfers are done through this byte-wide register regardless of whether DMA transfers are bytes or words.

Data may be written to this register when the attached device is not ready, but only if the device has been ready since a previous output. (That is, the data lines should not be changed until the previous output byte has been accepted by the device.) The best approach to using this register is to only write to it when the selected device and the interface are ready. The state of the device and interface may be determined by polling the DIRY bit in the Interface Status register or using the ready interrupt.

Interface Status

The Interface Status register may be used to determine the internal state of the interface. In particular it may be used to determine when the device and interface are ready for another command or data transfer.

Bit	Name	Function
07	DIRY	device and interface ready
06	DVRY	device ready
05	IFLG	interrupt flag
04	WORD	0=16 bit DMA, 1=8 bit DMA
03	SWAP	0=DMA byte swap
02	TSEL	0=test pattern 0, 1=test pattern 1
01	FPLT	0=force plot switch on
00	TEST	0=device test mode on

DIRY This is the master ready bit for the device and interface. A one in this bit indicates that the device and interface are ready for a command or data transfer. It will go to zero during DMA or Programmed I/O transfers, and at any other time that the selected device is not ready, such as after issuing a command to the Versatec port, or when the selected device is offline. If interrupts are enabled by the IENB bit in the Latched Functions register, an interrupt will be generated any time that the DIRY bit makes a false-to-true transition.

DVRY A one in this bit indicates that the selected device is ready. This means that an ACK- pulse has been received from a Centronics-type device and it is not currently asserting BUSY or that a Versatec type device is asserting READY-. This status bit is included for diagnostic purposes and should not be used to interlock data or command transfers.

IFLG A false-to-true transition of the DIRY interface status bit -- while IENB is true -- will cause IFLG to set, indicating that the device and interface are ready for another command or data transfer. If IENB is false, transitions on DIRY will not cause IFLG to set.

WORD A 0 in this bit indicates that the DMA channel selected via on-board switches is a 16 bit channel. A 1 indicates an 8 bit channel.

SWAP A 0 in this bit indicates that the board has been strapped to swap data bytes during 16 bit DMA transfers.

TSEL, FPLT
These bits indicate the position of the test pattern select toggle switch. The test pattern is used when exercising the attached device and cable. IF FPLT is a 0, the pattern select switch is in the PLOT position, and an all ones pattern will be sent to the attached device. In addition, the Versatec PLOT signal will be asserted. If FPLT is a 1, the pattern selected is indicated by the TSEL bit. If TSEL = 0, the T0 pattern is selected. If TSEL = 1, the T1 pattern is selected. See the Device Exerciser section of this manual for further information.

TEST If TEST = 0, the device is being exercised, and is not available to the host CPU. This device exercise and test mode may be cancelled by the MCLR bit in the Pulsed Functions register.

Diagnostic Data

This register contains a copy of the last (latest) byte sent to the selected external device. This copy is updated when the data is actually transmitted, not when it is loaded by the program or DMA logic.

Device Status

Bit	Name	Function
07	VTTL	0=Versatec TTL selected
06	VDIF	0=Versatec differential selected
05	CENT	0=Centronics selected
04	VRDY	1=Versatec READY- asserted
03	CBSY	1=Centronics BUSY asserted
02	PMTY	1=device out of paper
01	ONLN	1=device selected (online)
00	CFLT	1=Centronics FAULT- asserted

VTTL VTTL = 0 indicates that Versatec TTL interfacing has been selected. Interfacing mode is selected by an internal jumper cable on the 10092 board.

VDIF VDIF = 0 indicates that Versatec differential (long lines) interfacing has been selected.

CENT CENT = 0 indicates that Centronics interfacing has been selected.

VRDY VRDY is a 1 whenever the Versatec READY- signal is asserted by the attached device. It is also 1 during the ACK- pulse from a Centronics device. Since the ACK- pulse is brief, this bit will normally be a 0 when a Centronics compatible device is attached.

CBSY CBSY is a 1 whenever an attached Centronics-compatible device is asserting the BUSY signal. BUSY is used in combination with ACK- to determine when the device is ready for data transfer. A switch option may be used to eliminate busy from the ready equation.

PMTY PMTY will be read as a 1 whenever the attached device is asserting its paper empty signal. This is

true for both Versatec and Centronics-compatible devices.

ONLN — ONLN = 1 indicates that a Versatec-compatible device is online, or a Centronics-compatible device is selected.

CFLT — CFLT = 1 whenever a Centronics-compatible device is asserting the FAULT- signal.

Interface Strapping

Bit	Name	Function
07	TERM	Terminator Status
06	DSL2	DMA select switches
05	DSL1	
04	DSL0	
03	ISL3	Interrupt select switches
02	ISL2	
01	ISL1	
00	ISL0	

The TERM bit (terminator status) indicates what type of resistor network is installed in the terminator socket at U38. If a pull-up or resistive bridge type network is installed (470ohms to +5 or a 220/330ohm net), TERM will be a one. If a pull-down network (100ohm to ground) is installed, TERM will be a 0. Consult appropriate device documentation for network selection.

The DSLx and ISLx bits indicate which DMA channel and Interrupt level have been selected by on-board DIP switches. A register value of (hex) 3F would indicate that the board had been strapped for DMA channel 3 and Interrupt level 15. This register is primarily diagnostic in nature, and allows the software to determine whether the board is correctly strapped before enabling DMA and interrupts.

See the Hardware Options section of this manual for further information.

DMA Operation

The 10092 uses the DMA logic provided by the AT-compatible system for DMA transfers. DMA may be 8 or 16 bits per transfer, depending on which DMA channel is selected. If a 16 bit channel is selected, byte swapping may also be selected. This is useful when the host CPU does not use the usual byte ordering, and avoids the extra software overhead of reversing the bytes in memory prior to transferring them to the device.

DMA is initiated by first loading the host's DMA logic with the starting address and length of the buffer -- see appropriate host documentation -- and setting the DMON bit in the Latched Functions register. DMA transfers to the attached device will begin and continue without further processor intervention. When the range count has been exhausted, and the device again becomes ready, the DIRY bit in the interface status register will set, indicating that the device is ready for further data or commands.

If a 16 bit DMA channel has been selected, the buffer must contain an even number of valid data bytes and start on an even byte address.

Interrupts

The 10092 is capable of generating an interrupt request on any of the interrupt lines available on the bus. Interrupt selection is via switches on the 10092.

Interrupts are enabled by first setting up the system's interrupt logic -- see appropriate system documentation -- and setting IENB in the Latched Functions register. Interrupts will occur whenever the IENB and IFLG bits in the Interface Status register are true, and the host system has the selected interrupt level enabled. IFLG sets on any 0-to-1 transition of the DIRY bit in the Interface Status register that occurs while IENB is true. It will set whenever the interface and device become ready for another data transfer or command, and may be used to request an interrupt after a command, Programmed I/O, or DMA data transfer.

Typically the interrupt code will clear the INTF flag by using the RINT bit in the Pulsed Function register and re-enable interrupts prior to exiting the interrupt handler code. Alternatively, the program will leave interrupts disabled until the next DMA or command operation is initiated.

Interface Diagnostics

The 10092 ATbus Hardcopy interface provides several internal "hooks" that allow exercising and testing most features of the board without a hardcopy device attached. These internal diagnostic features also allow initial program development to be done without a device attached. (Usually saving a lot of paper!)

The internal diagnostic featues of the 10092 consist of three elements: 1) the Latched Functions register bits, 2) the Diagnostic Data register, and 3) the test bits in the Latched Function register.

The Latched Functions register bits are useful as a way of verifying that the interface and device modes specified by the software are actually reflected in the interface state; e.g., if the software has selected data streaming mode, the DSTR bit in the Latched Functions register should be set.

The Diagnostic Data register is an internal register that contains a copy of the last byte sent to the external device. It can be used during actual data transfer to the device to monitor the data sent, or it can be used with a software simulated device to verify that the data passing through the interface is what was expected.

There are two test bits in the Latched Function register: TENB and TVRY. When TENB is set to 1 it enables the TVRY bit to drive the Versatec READY- input. The TVRY bit can then be used to simulate transitions on the READY- line. If Programmed I/O or DMA data transfers are attempted in this mode, the first byte will be transmitted when READY- (TVRY) is true. Subsequent bytes will each be transmitted after the READY- line makes a true-false-true transition. The data can be verified during this process by monitoring the Diagnostic Data register. Interrupts may also be tested by enabling an end-of-range interrupt or by simply using a true-false-true sequence of the READY- input to generate a ready interrupt without setting up for data transfer. The TENB bit will force Versatec TTL mode and should not be set when a device is connected to the interface.

Device Exerciser

Board-mounted toggle switches allow exercising the attached device without CPU and software intervention. This is normally done at installation time to verify that device strapping, interface selection (Versatec TTL, Differential, or Centronics), interface strapping, and cable all agree.

Setting S2 momentarily to the TEST position will begin the transmission of a test pattern to the attached device. The test pattern will repeat indefinitely until S2 is moved momentarily to the RESET position. Switching S2 to the RESET position will also send a reset to the attached device, and reset the latches in the interface.

The test pattern to be sent to the attached device is selected by toggle switch S1. If S1 is in the PLOT position, the data sent to the device will be an "all ones" pattern, and Versatec PLOT mode will be selected. This should produce an all black plot on a black and white plotter. If S1 is in the T1 position, the "upper" pattern in the installed test PROM will be sent to the attached device. This pattern is normally a repeating ASCII character set, which can be used to exercise any device which can emulate a line printer. This character set does not include carriage return or line-feed characters, and may not produce output on some printers which require these characters to initiate a print cycle. If S1 is in the T0 position, the test pattern in the "lower" portion of the test PROM will be selected. This pattern is normally a color bar for Tektronix color copiers, but may be customized for almost any device.

Hardware Options

NOTE: The 3-pin jumper block W1-3 is for factory use only!

Board Address Selection

The location of the 10092's register set in the I/O channel I/O address space is determined by DIP switches at U13. The correspondence between switches and channel address bits is shown below:

U13	address bit
1	SA09
2	SA08
3	SA07
4	SA06
5	SA05
6	SA04
7	SA03
8	unused

"NOTE:" Address switches are complemented. A switch set to off (OPEN) will cause a one to be decoded in that bit position.

The board's register set may be located anywhere in the range (hex) 00 to 3FF, although it is customary to use an address in the range (hex) 100 to 3FF. An address of (hex) 310 would be selected by setting switches 1, 2, and 6 OFF, and 3, 4, 5, and 7 ON.

U55	Function
1	unused
2	DSL2
3	DSL1
4	DSL0
5	ISL3
6	ISL2
7	ISL1
8	ISL0

DMA Channel Selection

Switches U55-2, 3, and 4 determine which DMA channel is selected. Channel selection is binary, with switch 1 being the most significant bit, and a switch ON equalling a 1. DMA channel 6 would be selected by setting switches 2 and 3 ON, and switch 4 OFF.

Channels 0 through 3 are 8 bit channels, and 5, 6, and 7 are 16 bit channels. The 10092 will automatically configure itself to the appropriate data width depending on which DMA channel is selected. Channel 4 is not available on the I/O channel. If DMA is not to be used in a particular application, channel 4 should be selected, to prevent driving a channel used by another device.

Interrupt Selection

Switches U55-5, 6, 7, and 8 determine which Interrupt level is to be used by the board. Like DMA channel selection, Interrupt level selection is binary, with switch 5 being the most significant bit, and a switch ON equalling a 1. Interrupt level 10 would be selected by setting switches 5 and 7 ON, and 6 and 8 OFF.

Interrupt levels 3 through 7, 9, 10, 11, 12, 14, and 15 are available on the I/O channel. If interrupts are not to be used, level 0, 1, 2, 8, or 13 should be selected to avoid driving an Interrupt level used by another device.

U57	Function
1	BUSY 1
2	BUSY 2
3	unused
4	SWAP
5	unused
6	FAST
7	unused
8	DSTX

Byte Swapping

If a 16 bit DMA channel is selected, the order of bytes transmitted to the device is determined by switch U57-4. If that switch is OFF, the bytes will be sent low byte first (standard for processors such as the 8086 and 80286). If U57-4 is ON, data will be sent high byte first, which may be useful in systems using a 68000-type processor. This switch has no effect on data sent via the Programmed I/O Output register, or when an 8 bit channel is selected.

Device Interface Options

Interface Mode

The device interface mode is selected by the position of the on-board jumper cable. One end of this cable is always connected to the I/O Out pin-strip. The other end is connected to the appropriate pin-strip to select either Centronics, Versatec TTL, or Versatec differential (long-lines) interfacing.

Data Streaming

The "Data Streaming" mode available for use with Tektronix color copiers is selected by DIP switch U57-8. If it is ON, only data bytes with the MSB set will be streamed; bytes with the MSB off will cause the interface to wait for a handshake from the color copier. If U57-8 is off, all bytes will be "streamed". This data streaming function is active only when the DSTR bit in the Latched Function register is a one. Data streaming should only be selected when connected to a Tektronix device which is also in streaming mode.

In general, the mode that streams all bytes should be used for new applications, regardless of which type of streaming the copier supports. The other mode is included for compatibility with existing applications.

Timing

The timing of data transfers to the attached device is fixed for Versatec mode interfacing, and selectable for Centronics mode interfacing. Versatec mode provides approximately 200ns of data set-up time prior to the leading edge of the PICLK data strobe, approximately 500ns of data strobe, and a minimum of 200ns data hold after the data strobe (or until the device becomes ready, whichever is later). The standard Centronics timing is selected if U57-6 is OFF. It gives (approximately) 1us set-up, 1us strobe, and 1us minimum hold time. If U57-6 is ON, the compressed Centronics timing is selected, which gives (approximately) 200ns set-up, 800ns data strobe, and 200ns hold time. This compressed timing is compatible with the Tektronix compressed timing mode, and may be useful with other devices which can tolerate the shortened timings.

Centronics BUSY/ACK Selection

Switches U57-1 and U57-2 determine how the Centronics signals BUSY and ACK are used in the device to interface handshake. Normally, U57-1 should be ON, and U57-2 should be OFF. This will cause the interface to use both ACK and BUSY in the data transfer handshake. If BUSY is not to be used (some devices use ACK only), both switches should be set to OFF. Other combinations of switch settings are not currently used.

These switches have no effect when Versatec interfacing is selected.

Termination Selection

The termination resistor installed in the socket pins at U38 must agree with the interfacing mode selected, and with the device to which the interface is attached. The 10092 is normally shipped with a 220/330 ohm network installed which is appropriate for most Centronics applications, and ALL Versatec applications, whether TTL or differential. For Centronics-type devices that use gates, rather that drivers to drive status, and handshake lines, it may be necessary to use a 470 ohm network. For Tektronix 4691 and 4692 color copiers, a 100 ohm network should be installed UPSIDE DOWN in the termination socket. This will match the "long cable" option available on these color hardcopy devices, and will give the best signal quality.

Spare termination resistor networks will be found in sockets labelled "SPARE TERM".

Device Cabling

All interfacing modes are supported through a single 37-pin "D" subminiature connector on the rear panel of the interface. This connector may be used directly for Versatec applications (Versatec uses a 37-pin "D"). For Centronics applications, a special cable must be used which has a 37-pin "D" on one end and a 36-pin "delta ribbon" connector on the other. This cable may be used to go directly to the device (normally a "male" cable connector), or may be used with a "female" cable connector as an adapter to another manufacturer's "delta ribbon" to "delta ribbon" cable. It is also possible to fabricate other cable/connector combinations to match other existing cabling schemes.

Versatec Cable Run-List

Signal Name		37 pin "D"
TTL	Differential	Connector
IN01	IN01+D	1
GND	IN01-D	20
IN02	IN02+D	2
GND	IN02-D	21
IN03	IN03+D	3
GND	IN03-D	22
IN04	IN04+D	4
GND	IN04-D	23
IN05	IN05+D	5
GND	IN05-D	24
IN06	IN06+D	6
GND	IN06-D	25
IN07	IN07+D	7
GND	IN07-D	26
IN08	IN08+D	8
GND	IN08-D	27
CLEAR-	CLEAR-D	9
GND	CLEAR+D	28
PICLK	PICLK+D	10
GND	PICLK-D	29
READY-	READY-D	11
GND	READY+D	30
PRINT	PRINT+D	12
GND	PRINT-D	31
PARALLEL	N-C	13
ONLIN-	INOP-D	32
SPP-	SPP-D	14
GND	SPP+D	33
RESET-	RESET-D	15
GND	RESET+D	34
RFFED-	RFFED-D	16
GND	RFFED+D	35
REOTR-	REOTR-D	17
GND	REOTR+D	36
RLTER-	RLTER-D	18
GND	RLTER+D	37
NOPAP	INOP+D	19

Centronics Cable Run-List

Signal Name	37-pin "D"	Delta Ribbon
STROBE-	1	1
GND	20	19
DATA 1	2	2
GND	21	20
DATA 2	3	3
GND	22	21
DATA 3	4	4
GND	23	22
DATA 4	5	5
GND	24	23
DATA 5	5	6
GND	25	24
DATA 6	7	7
GND	26	25
DATA 7	8	8
GND	27	26
DATA 8	9	9
GND	28	27
ACK-	10	10
GND	29	28
BUSY	11	11
GND	30	29
PE	12	12
GND	31	30
SLCT	13	13
INPUT PRIME-	32	31
N-C	14	14
FAULT-	33	~~14~~ 32

all other pins -- no connection