intel

iRMX® II
MULTIBUS® I
Bus-Specific Information

Order Number: 463737-001

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Bus-Specific Information

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Intel Corporation
3065 Bowers Avenue
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PREFACE

INTRODUCTION

This manual is the MULTIBUS® I bus-specific information for the iRMX® II Release 4 operating system.

READER LEVEL

This manual is written for readers who are unfamiliar with the iRMX II Operating System, but who have general micro-computing experience.

CONVENTIONS

This manual uses the following conventions:

- Information appearing as UPPERCASE characters when shown in keyboard examples must be entered or coded exactly as shown. You may, however, mix lower and uppercase characters when entering the text.
- Fields appearing as lowercase characters within angle brackets (< >) when shown in keyboard examples indicate variable information. You must enter an appropriate value or symbol for variable fields.
- Information appearing in blue print indicates user input.
- The term "iRMX II" refers to the iRMX II.4 Operating System.
- The term "iRMX I" refers to the iRMX I (iRMX 86) Operating System.
- All numbers unless otherwise stated are assumed to be decimal. Hexadecimal numbers include the "H" radix character (for example, 0FFH).

CONTENTS

MULTIBUS® I And the Standard Definition Files

1.1 MULTIBUS® I Bus Standard 1-1
1.2 The MULTIBUS® I Standard Definition Files 1-5
1.3 Nucleus Configuration in the Standard Definition Files 1-6
1.4 System Debugger Configuration in the Standard Definition Files 1-7
1.5 BIOS Configuration in the Standard Definition Files 1-7
1.6 EIOS Configuration in the Standard Definition Files 1-8
1.7 Application Loader Configuration in the Standard Definition Files 1-8
1.8 HI Configuration in the Standard Definition Files 1-9
1.9 UDI Configuration in the Standard Definition Files 1-11
1.10 I/O Controller Boards in the Standard Definition Files 1-12
1.11 Interrupt Levels Used in the Standard Definition Files 1-13
1.11.1 Interrupt Level Assignments For iSBC® 286/12 and 386/12 Boards 1-14
1.11.2 Interrupt Level Assignments In 38620.DEF 1-15
1.11.3 Interrupt Level Assignments In SXM386.DEF 1-16

Tables

1-1. MULTIBUS® I Definition Files 1-5
1-2. Definition Files for the iSBC® 286/12 and 386/12 Boards 1-11
1-3. Definition Files for the iSBC® 386/2X/3X Boards 1-11

Figures

1-1. MULTIBUS® Connectors 1-2
1-2. Parallel Priority Resolution for MULTIBUS® I Bus 1-3

Index

MULTIBUS® I AND THE STANDARD DEFINITION FILES 1

1.1 MULTIBUS® I BUS STANDARD

For the most part, software developers may safely ignore the bus their system uses, allowing the system hardware to take care of it. However, it helps to understand the basic principles of the bus structure when adding new boards. Also when examining any of the Intel-supplied iRMX® definition files, a working knowledge of your system bus is helpful. The following sections give a high-level description of the MULTIBUS® I architecture.

The basic MULTIBUS concept defines two printed circuit board edge connectors, an 86-pin connector (P1) and a 60-pin connector (P2) (See the figure titled MULTIBUS® Connectors). The pins on the 86-pin P1 connector are divided up into power supplies, bus controls and bus addresses, interrupts, address, and data lines. The 60-pin P2 connector is has for active pins (55 through 58) the remainder are reserved.

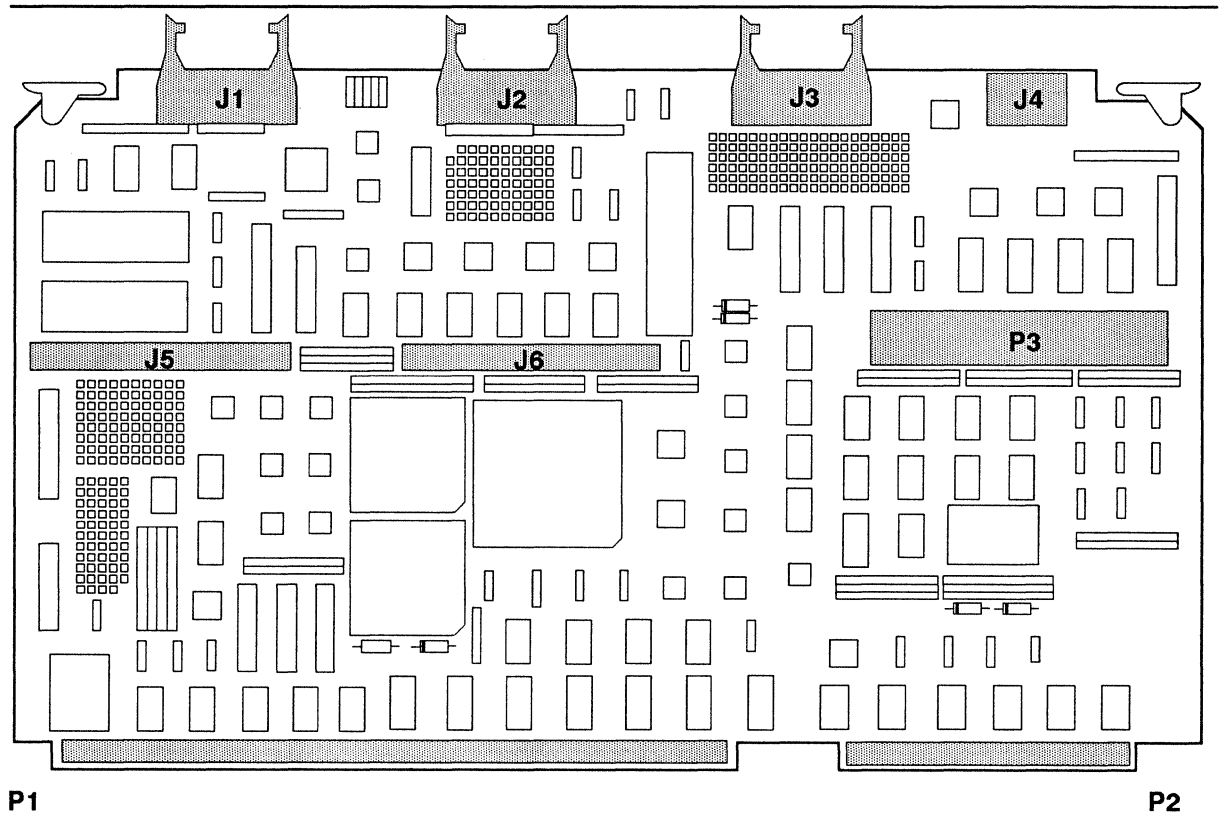

Figure 1-1. MULTIBUS® Connectors

Modern bus structures use a number of approaches to increase a computer system's total processing power while limiting the expense of a system. Using a system bus that permits the sharing of expensive system resources such as hard disks is a typical approach. The approach of placing several microcomputer boards on a single system bus and sharing system resources can be termed a loosely-coupled system approach. The term loosely-coupled describes systems in which CPU boards that are virtually independent systems share a common bus structure. In loosely-coupled systems, shared resources are reached by way of the system bus. In MULTIBUS systems, boards that can control the system bus are called **masters**; boards that are only written to or read from are called **slaves**.

A common problem in systems that have more than one bus master is what to do when two or more masters need to access the bus at the same time. The process of deciding which master gets the bus is called bus arbitration. In MULTIBUS systems, two methods can be used, **serial** and **parallel** bus priority. The serial bus priority scheme is no longer widely used so it is not explained in this book. The parallel priority method is the most common approach in current systems. Bus arbitration is accomplished using the following protocol.

When a master needs the bus to transfer data, it must assert the BREQ/ signal. This signal, along with signals from other masters, goes into a priority encoder chip (See the figure titled Parallel Priority Resolution for MULTIBUS I). The priority encoder outputs a three-bit code which goes into a one-of-eight low decoder. The one-of-eight low decoder will assert the BPRN/ input of the highest bus master currently requesting service.

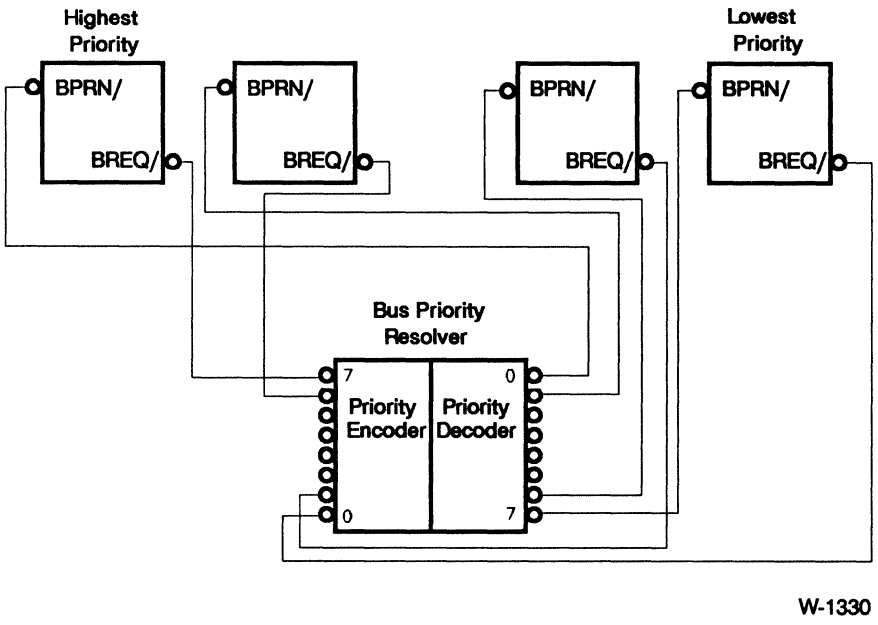

Figure 1-2. Parallel Priority Resolution for MULTIBUS® I Bus

While a bus master is using MULTIBUS I to transfer data, it holds the BUSY/ line low. No other master can take over the bus until the BUSY/ line is released. Typically a bus master releases the bus after each byte transfer. This prevents a high priority master from blocking a lower priority master from using the bus. Some operations though require more than one bus cycle to complete. An example of this is the XCHG (exchange) instruction which swaps the contents of a register with the contents of a memory location. If the master performing this operation gave up the bus after the first half of the exchange another master could use the contents of the memory location before it gets updated. To prevent this, a special mechanism called LOCK is used. This prefix allows the master to keep the bus until the operation is completed. Although the prefix can be generated from several sources, the most common is directly from the CPU. This chapter lists the contents of the definition files that you receive with the IRMX II Interactive Configuration Utility (ICU) for MULTIBUS I systems. A definition file contains values for the configurable parameters of the iRMX II Operating System and is manipulated using the ICU. When you change a parameter using the ICU, the change is saved in the definition file at the time you exit the ICU. The updated definition file is used in generating a custom version of the Operating System. This chapter lists the attributes of the systems defined by the standard definition files: the iRMX II layers, the device drivers selected, and the interrupt levels and I/O and memory addresses assigned.

1.2 THE MULTIBUS® I STANDARD DEFINITION FILES

These definition files define the standard systems for Intel Microcomputers and are supplied to allow you to easily regenerate versions of the Operating System with the latest Updates applied. They are also a convenient starting point for creating your own custom version of the Operating System. All the standard definition files include the Nucleus, System Debugger (SDB), Basic I/O System (BIOS), Extended I/O System (EIOS), Application Loader, Human Interface (HI) and Universal Development Interface (UDI). Note that the MSC driver listed in Table 1-1 supports the iSBC® 214, 215G, and 221 boards.

Table 1-1. MULTIBUS® I Definition Files

CPU Board	Definition File	MSC Driver	8251 Driver	8274 Driver	544A Driver	TCC Driver	iRMX-NET Server	iRMX-NET Consumer
iSBC 286/12	28612.def	Yes	No	Yes	Yes	Yes*	No	No
iSBC 286/12	28612net.def	Yes	No	Yes	Yes	Yes*	Yes	Yes
iSBC 286/12	28612rsd.def	No	No	Yes	Yes	Yes*	No	Yes
iSBC 386/12	38612.def	Yes	No	Yes	Yes	Yes*	No	No
iSBC 386/12	38612net.def	Yes	No	Yes	Yes	Yes*	Yes	Yes
iSBC 386/12	38612rsd.def	No	No	Yes	Yes	Yes*	No	Yes
iSBC 386/20	38620.def	Yes	Yes	No	No	Yes**	No	No
iSBC 386/20	38620net.def	Yes	Yes	No	No	Yes**	Yes	Yes
iSBC 386/20	38620rsd.def	No	Yes	No	No	Yes**	No	Yes

* Supports combinations of the iSBC 188/48 board or iSBC 188/56 board and the iSBC 548 board, see Table 1-2 for more information.

** Supports combinations of the iSBC 188/48 board or the iSBC 188/56 board and the iSBC 546/547 boards, see Table 1-3 for more information.

The Standard Definition Files for the iSBC 286/12 board on a System 310AP microcomputers are the 28612.def, 28612net.def, and 28612rsd.def. These files are used as follows:

- The 28612.def file is used when no networking is required and the system has local peripherals.
- The 28612net.def file is used when networking is required and the system has no local peripherals.
- The 28612rsd.def file is used when networking is required, but the system has no local peripherals.

The Standard Definition Files for the iSBC 386/2X/3X boards on a System 320 microcomputer are 38620.def, 38620net.def, and 38620rsd.def. These files are used as follows:

- The 38620.def file is used when no networking is required and the system has local peripherals.
- The 38620net.def file is used when networking is required and the system has no local peripherals.
- The 38620rsd.def file is used when networking is required, but the system has no local peripherals.

The Standard Definition Files for the iSBC 386/12 board are 38612.def, 38612net.def, and 38612rsd.def. Note that no Intel microcomputer comes with this processor board installed. These files are used as follows:

- The 38612.def file is used when no networking is required and the system has local peripherals.
- The 38612net.def file is used when networking is required and the system has no local peripherals.
- The 38612rsd.def file is used when networking is required, but the system has no local peripherals.

1.3 NUCLEUS CONFIGURATION IN THE STANDARD DEFINITION FILES

The iRMX II Nucleus is defined identically in the standard definition files with the exception of the MULTIBUS II definition files. The following description is a summary of its default features.

- All system calls are selected.
- 4000 GDT entries in MULTIBUS I definition files. 256 IDT entries are available for the Operating System and application systems.

- Parameter validation is enabled.
- The System Debugger is the default system exception handler.
- Any NMI interrupts received by the CPU will be ignored.
- A Double Fault will cause the responsible task's job to be deleted.
- The Numeric Data Processor is enabled.
- Round Robin scheduling is enabled. Each task which has a priority of 140 or lower (numerically higher) is given 5 clock ticks (50 milliseconds) before the next task of the same priority, if one is ready to run, is scheduled.
- Initialization Error Reporting is enabled allowing the Operating System to report errors to the system console encountered during system initialization.
- Random Access Memory (RAM) for the standard definition files is different for each file, see the "Memory Addresses" section later in this chapter for information; the iRMX II operating system requires a minimum of 896 KBytes of RAM when the CPU is in Real Mode during Bootstrap Loading.

1.4 SYSTEM DEBUGGER CONFIGURATION IN THE STANDARD DEFINITION FILES

The iRMX II SDB is defined identically in the standard definition files for all MULTIBUS I systems. The following description is a summary of its default features.

- Master PIC interrupt level 1 (encoded level 18H) is used to enter the SDB. To use the SDB, your system must include the iSDM™ System Debug Monitor.

1.5 BIOS CONFIGURATION IN THE STANDARD DEFINITION FILES

The iRMX II BIOS is defined identically, except for the Global Clock parameter, in the standard definition files. The following description is a summary of its default features.

- All system calls are selected.
- The System Manager ID is required. This gives the user with the ID 0 (zero) special privileges to change the access of any file.
- The BIOS memory pool minimum size is 0D00H and the maximum size is 0FFFFFH. A maximum size of 0FFFFFH allows the BIOS to borrow up to the limit of physical memory in the system if required.
- The stream, physical and named file drivers are selected. The remote file driver is selected in the networking definition files. iRMX-NET must be configured into the Operating System to supply support for remote files.
- The BIOS task priorities are selected to function properly with the task priorities of the Extended I/O System and the Human Interface.

- The Global Clock on the iSBC 546 board is selected in the definition files for the iSBC 386/2X/3X boards.
- All of the configurable interfaces are selected.

1.6 EIOS CONFIGURATION IN THE STANDARD DEFINITION FILES

The iRMX II EIOS is defined identically, except for the line printer physical name, in the standard definition files. The following description is a summary of its default features.

- All system calls are selected.
- No I/O users are created by the EIOS.
- The maximum number of entries in the EIOS job's directory is 50.
- The EIOS memory pool minimum size is 0180H and the maximum size is 0FFFFFH. A maximum size of 0FFFFFH allows the EIOS to borrow up to the limit of physical memory in the system if required.
- Recognition of the Bootstrap Device is selected. The device from which the system was bootstrap loaded will become the system device. The logical name of the system device is :SD:. This logical name should never be changed unless you have a specific reason to do so. If the system was not bootstrap loaded, the physical device name W0 will be attached as the system device.
- The following logical devices are attached by the EIOS when it is initialized:

Physical Device Name	Logical Name Name	Definition Files For:
BB (Byte Bucket)	:BB:	All Boards
STREAM	:STREAM:	All Boards
W0 or Bootstrap Device	:SD:	All Boards
LP	:LP:	iSBC 286/12, 386/12 boards
T546 LP	:LP:	iSBC 386/2X/3X boards

1.7 APPLICATION LOADER CONFIGURATION IN THE STANDARD DEFINITION FILES

The iRMX II Application Loader is defined identically in the standard definition files. The following description is a summary of its default features.

- All system calls are selected.
- The read buffer is set to 1000H. The default memory pool for all definition files is set to 500H.

1.8 HI CONFIGURATION IN THE STANDARD DEFINITION FILES

The iRMX II HI is defined identically in the standard definition files. The following description is a summary of its default features.

- All system calls are selected.
- The HI memory pool minimum size is 0260H and the maximum size is 0FFFFFH. A maximum size of 0FFFFFH allows the HI to borrow up to the limit of physical memory in the system if required.
- The maximum number of characters in the CLI invocation line and SUBMIT invocation is 64.
- The Resident Recovery User is selected in the event there is an error while accessing the user or terminal configuration files.
- The System Command File, :CONFIG:R?INIT, is executed before any users can log on to the system.
- There are two users defined when the system is installed: SUPER and WORLD. The user SUPER, also referred to as the 'system manager' has the ID 0 and the password 'passme' (in lower case). The user WORLD has the ID 65535 and a null password (a carriage-return). The user WORLD has special privileges when accessing files and should always have a null password. The HI PASSWORD command can be used to define new users in your system.
- Logical names for common directories are defined as follows:

Directory	Logical name
:SD:SYS286	:SYSTEM:
:SD:WORK	:WORK:
:SD:UTIL286	:UTILS:
:SD:LANG286	:LANG:
:SD:RMX286/ICU	:ICU:

- The search path used by the HI when a command name is entered is:

  :PROG:
  :UTILS:
  :SYSTEM:
  :LANG:
  :ICU:
  :$:

  This allows you to use a custom version of a command, which is also supplied with the Operating System, by placing it in the :PROG: or :UTILS: directories. When you invoke the command with no prefix specified, your custom version is executed instead of the version supplied with the Operating System. The :PROG: directory is unique to each user of the HI. The :UTILS: directory is common to all users of the HI. The :ICU: directory is included to make accessing the Interactive Configuration Utility easier. The :$: directory is placed last because typically commands you invoke are not contained in the current default directory (:$:).

- Initially, one terminal is configured for use by HI users. More terminals can be added by modifying the file :CONFIG:TERMINALS. This is described in the *Guide to the iRMX® II Interactive Configuration Utility* and the *Operator's Guide to the iRMX® II Human Interface*. The following tables describe the maximum number of terminals (and hence users) that can be supported by the systems defined by the standard definition files. The different combinations indicate the different types of terminal controllers which may be used at the same time. If a different combination is needed, you must run the ICU to change the interrupt level, flag byte address and the dual port buffer addresses of the necessary terminal controller boards.

Table 1-2. Definition Files for the iSBC™ 286/12 and 386/12 Boards

Terminal Device	Combination #1	Combination #2	Combination #3
CPU board	2 users	2 users	2 users
iSBC 544A	4 users		
iSBC 188/48 or iSBC 188/56		8 users	
iSBC 548			8 users
TOTAL USERS	6 users	10 users	10 users

Table 1-3. Definition Files for the iSBC™ 386/2X/3X Boards

Terminal Device	Combination #1	Combination #2	Combination #3	Combination #4
CPU board	1 user	1 user	1 user	1 user
iSBC 546	4 users	4 users	4 users	
iSBC 547 #1	8 users	8 users	8 users	
iSBC 547 #2		8 users	8 users	
iSBC 547 #3			8 users	
iSBC 188/48 or iSBC 188/56				8 users
TOTAL USERS	13 users	21 users	29 users	9 users

1.9 UDI CONFIGURATION IN THE STANDARD DEFINITION FILES

The iRMX II UDI is defined identically in the standard definition files. There are no configurable parameters to the UDI.

1.10 I/O CONTROLLER BOARDS IN THE STANDARD DEFINITION FILES

This section lists the I/O controller boards that are selected in the standard definition files. Whenever you see an "or" with a series of I/O boards, you may use only one of the I/O controllers in the system because they use a common system resource (such as an interrupt level or a port address) which cannot be shared. If you need to use a different combination of I/O controllers, you can either create a new definition file or modify one of the standard definition files. Depending on what changes you make to the device configuration screens in the definition files, you may need to jumper the I/O controllers differently than described in this manual.

The definition files for the iSBC 286/10, iSBC 286/10A, iSBC 286/12, and iSBC 386/12 processor boards support the following I/O controllers:

- 8274 Channels A and B
- iSBC 544A
  or
  iSBC 548
  or
  iSBC 188/48
  or
  iSBC 188/56
- iSBC 214
  or
  iSBC 215G/iSBX™ 217C/218A
- On-board Line printer

The definition files for the iSBC 386/2X and iSBC 386/3X processor boards in a System 320 Microcomputer support the following I/O controllers:

- 8251A
- iSBC 546, includes line printer and global clock
- iSBC 547 Number 1
- iSBC 547 Number 2
- iSBC 547 Number 3
- iSBC 548
  or
  iSBC 188/48
  or
  iSBC 188/56
- iSBC 214
  or
  iSBC 215G/iSBX 217C/218A

1.11 INTERRUPT LEVELS USED IN THE STANDARD DEFINITION FILES

All of the Intel 80286- and 386™-based processor boards that can run the iRMX II Operating System contain an master and a slave 8259A programmable interrupt controller (PIC). This section describes the interrupt level assignments (both MULTIBUS and PIC) in the standard definition files. In order to accommodate a large number of configurations, the definition files may assign a single MULTIBUS or PIC interrupt level to two or more different functions. You may use only one of these functions at a time without changing the configuration. If you need to use more than one at a time, you must run the ICU and generate a version of the Operating System which reflects your needs.

In the discussions that follow, the term 'dedicated' means the function is not selectable with a jumper; the board fixes the input and output of the signal. In the discussions that follow, the term 'available' means the function is not assigned any function in the standard definition files and may be used without worry of conflict in your application. Some of the definition files allow you to use multiple iSBC 547 boards. These boards are indicated: iSBC 547 number 1, iSBC 547 number 2 and iSBC 547 number 3.

The iSBC 552A Ethernet Communication Controller board is listed in the following tables. It is not supported in the standard definition files you receive with the iRMX II Operating System, but is supported in the definition files you receive with the iRMX-NET Software. If you are not using the iRMX Networking Software, the interrupt level assigned to the iSBC 552A board is available for another use.

1.11.1 Interrupt Level Assignments For iSBC® 286/12 and 386/12 Boards

The definition files for the iSBC 286/10(A), iSBC 286/12, or iSBC 386/12 processor boards have the interrupt level assignments for the MULTIBUS and the Master and Slave PIC as follows:

MULTIBUS Interrupt	Master PIC Interrupt	Function or Connection
None	0	System clock (8254 timer 0)
INT0	NMI	Memory Parity errors
INT1	1	System Debugger (SDB)
INT2		Available
INT3	3	iSBC 188/48/56 or iSBC 548 or iSBC 544A
INT4	4	iSBC 552A
INT5	5	iSBC 214 or iSBC 215G/iSBX 217C/218A
None	6	On-board 8274 Channels A and B
None	7	On-board Slave PIC (dedicated)

MULTIBUS Interrupt	Slave PIC Interrupt	Function or Connection
INT6	0	Available
INT7	1	Available
None	2	Available
None	3	iSBX Interrupt (dedicated)
None	4	iSBX Interrupt (dedicated)
None	5	iSBX Interrupt (dedicated)
None	6	iSBX Interrupt (dedicated)
None	7	on-board Line Printer (dedicated)

1.11.2 Interrupt Level Assignments In 38620.DEF

The Definition files for the iSBC 386/2X or iSBC 386/3X boards have the interrupt level assignments for the MULTIBUS and the Master and Slave PIC as follows:

MULTIBUS Interrupt	Master PIC Interrupt	Function or Connection
None	0	System clock (8254 timer 0)
INT0	NMI	Memory Parity errors
INT1	1	System Debugger (SDB)
INT2	2	iSBC 547 number 1
INT3	3	iSBC 546 or iSBC 188/48/56
INT4	4	iSBC 552A
INT5	5	iSBC 214 or iSBC 215G/iSBX 218A
None	6	Available
None	7	On-board Slave PIC (dedicated)

MULTIBUS Interrupt	Slave PIC Interrupt	Function or Connection
INT6	0	iSBC 547 number 2
INT7	1	iSBC 547 number 3
None	2	Available
None	3	iSBX Interrupt (dedicated)
None	4	iSBX Interrupt (dedicated)
None	5	Available
None	6	8251A USART Receive Interrupt
None	7	8251A USART Transmit Interrupt

1.11.3 Interrupt Level Assignments In SXM386.DEF

The Definition file, SXM386.DEF, defines a version of the iRMX II Operating System to run on the iSBC 386/2X when installed as part of the SXM386AP Kit in a System 310AP microcomputer. The interrupt level assignments for the MULTIBUS I and the Master PIC are as follows:

MULTIBUS Interrupt	Master PIC Interrupt	Function or Connection
None	0	System clock (8254 timer 0)
None	NMI	On-board Memory Parity errors
INT0		Available
INT1	1	System Debugger (SDB)
INT2		Available
INT3	3	iSBC 188/48/56 or iSBC 548 or iSBC 544A
INT4	4	iSBC 552A
INT5	5	iSBC 214 or iSBC 215G/iSBX 217C/218A
None	6	Available
None	7	On-board Slave PIC (dedicated)

MULTIBUS Interrupt	Slave PIC Interrupt	Function or Connection
INT6	0	Available
INT7	1	Available
None	2	Available
None	3	iSBX Interrupt (dedicated)
None	4	iSBX 350 Line Printer
None	5	Available
None	6	8251A USART Receive Interrupt
None	7	8251A USART Transmit Interrupt

INDEX

A

Application loader configuration in MULTIBUS I definition files 1-8

B

Basic I/O System in MULTIBUS I definition files 1-7
BIOS configuration in MULTIBUS I definition files 1-7

D

Definition of MULTIBUS 1-1

E

EIOS configuration in MULTIBUS I definition files 1-8
Extended I/O System configuration in MULTIBUS I definition files 1-8

H

HI configuration in MULTIBUS I definition files 1-9
Human Interface configuration in MULTIBUS I definition files 1-9

I

I/O controller board in standard definition files 1-12
Interrupt levels assigned in SXM386.def 1-16
Interrupt levels in the standard definition files 1-13
Interrupts assigned for iSBC 286/12 and iSBC 386/12 boards 1-14
Interrupts assigned in 38620.def file 1-15

M

MULTIBUS, a definition 1-1
MULTIBUS I 1-1
MULTIBUS I Standard Definition Files 1-5

N

Nucleus Configuration, MULTIBUS I 1-6

S

SDB configuration in MULTIBUS I Definition files 1-7
System Debugger in MULTIBUS I definition files 1-7

U

UDI configuration in the MULTIBUS I definition files 1-11

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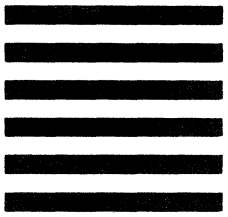

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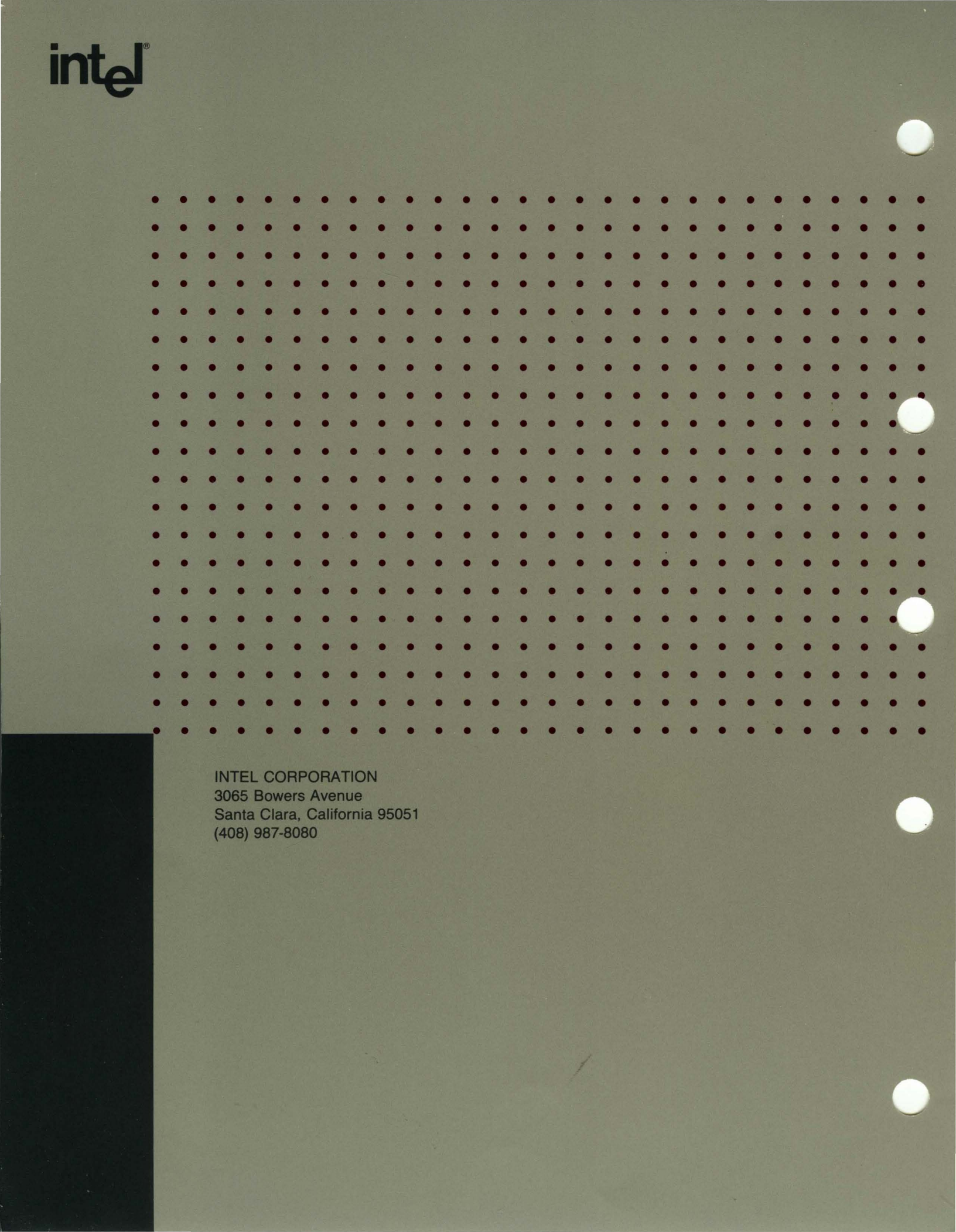

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