AMPEX model DM-323
MOD-1 A

Publication Number 29-387R04

M46-429
40 MEGA-BYTE DISC SYSTEM
INSTRUCTION MANUAL

CONSISTS OF:

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MAINTENANCE SPECIFICATION	02-357R02A21
PROGRAMMING SPECIFICATION	02-357A22
INTERFACE SCHEMATIC	02-359R08D08
CONTROL PANEL SCHEMATIC	09-067B08
INFORMATION DRAWING	02-357D12
COMPONENT LOCATOR	35-532R06E03

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36-37	R02	9/76						
38-48	R01	6/74						
02-357A22 Programming Specification R00 6/74								
1-14	R00	6/74						
A1-1 thru A1-4	R00	6/74						

M46-429
40 MEGA-BYTE DISC SYSTEM INSTALLATION SPECIFICATION

1. INTRODUCTION

This specification provides system installation and system configuration information for INTERDATA 40 Mega-Byte Disc Systems.

Table 1 indicates the relationship between Product Numbers and Part Numbers for the hardware components required for different configurations of the disc system.

TABLE 1. DISC SYSTEM CONFIGURATIONS

PRODUCT NUMBER	PART NUMBER	CONTENTS	DESCRIPTION
M46-429 (208 Volts 3 Phase 50Hz or 230 Volts Single Phase)	02-357F01	1 each 35-531 1 each 35-532 1 each 09-067 1 each 27-060F01 1 each 24-057	File Control Board Disc Control Board Control Panel Disc File Formatted Disc Pack
M46-430 (230 Volts Single Phase, 50Hz)	02-357F01	1 each 35-531 1 each 35-532 1 each 09-067 1 each 27-060F02 1 each 24-057	File Control Board Disc Control Board Control Panel Disc File Formatted Disc Pack
M46-431 (Expansion File 208 3 phase/ 230 Single Phase 50 Hz)	02-358F01	1 each 27-060F03 1 each 17-315 1 each 24-056	Disc File Expansion Cable Disc Pack
M46-432 (Expansion File 230 Volts Single Phase 50 Hz)	02-358F02	1 each 27-060F04 1 each 17-315 1 each 24-056	Disc File Expansion Cable Disc Pack
M46-433 (Controller Only)	02-359	1 each 35-531 1 each 35-532 1 each 09-067	File Control Board Disc Control Board Control Panel

NOTE: 1 each 16-502 Miscellaneous Hardware Kit for mounting 09-067 is supplied with M46-429, M46-430, and M46-433.

2. MECHANICAL ASSEMBLY

The 40 Mega-Byte Disc System consists of two (35-531 and 35-532) 15" printed circuit boards, a control panel (09-067), and from one to four disc files (27-060). The installation for the two printed circuit boards and the control panel is shown in Information Drawing 02-359D12 which is provided in the 40 Mega-Byte Disc System Instruction Manual, Publication Number 29-387.

3. UNPACKING INSTRUCTIONS

Refer to the Disc File Vendor manual 29-400 which is included for Disc File Unpacking Instructions.

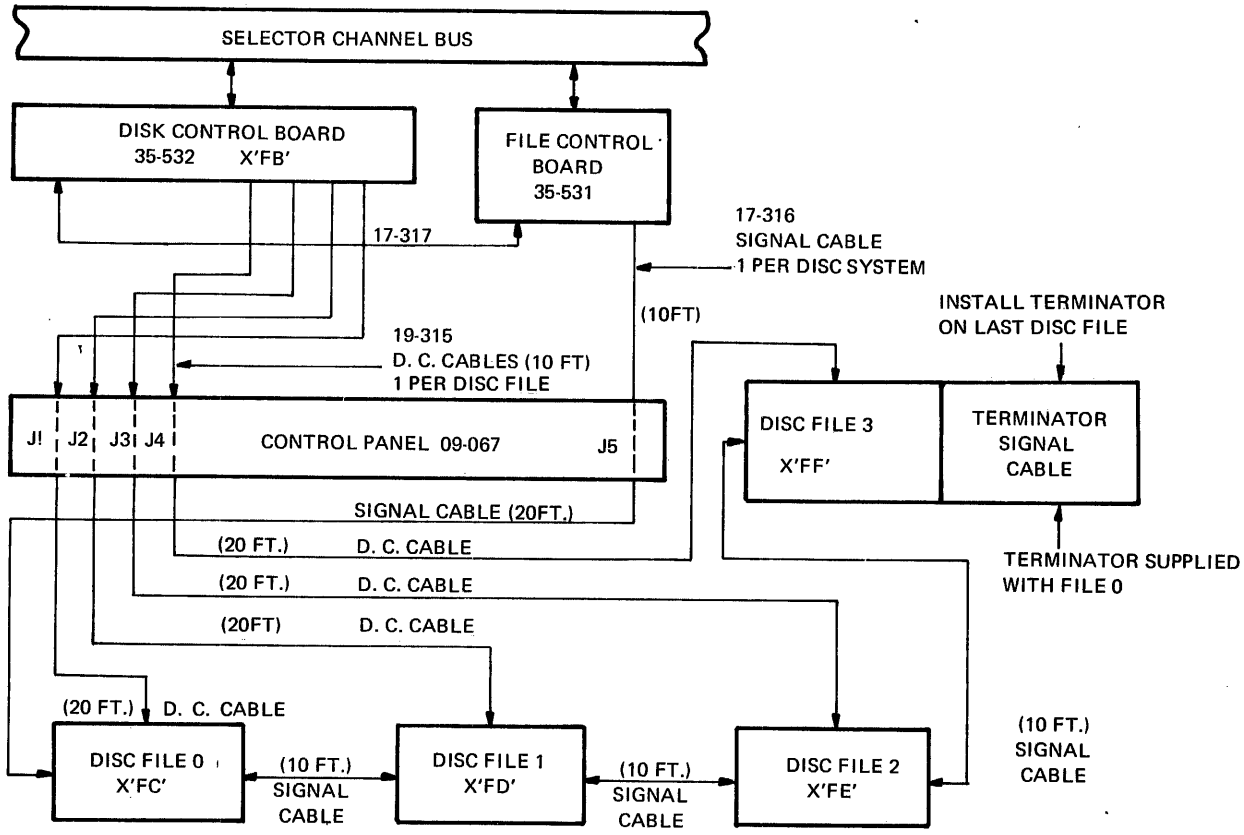
4. MOUNTING INSTRUCTIONS

The control panel (09-067) can be mounted in any standard 19 inch RETMA cabinet or rack. For mounting instructions and procedures, refer to Information Drawing 02-359D12.

5. SYSTEM CONFIGURATION

The two 15 inch printed circuit boards may be installed in any two adjacent 15 inch I/O slots on an INTER-DATA Processor or Expansion Card File. The Controller must be supported by a SELCH or ESELCH to handle the 312K byte transfer rate of the disc file. Remove the RACK0/TACK0 strap between back panel terminal 122-1 and 222-1 at the locations of the two boards. The disc control board (35-532) must be placed at the higher priority on the Selector Channel Bus. To provide the correct priority of interrupts, the two disc controller boards must be installed in adjacent card slots. Refer to Information Drawing 02-359D12.

Figure 1 illustrates the overall system configuration for the 40 Mega-Byte Disc System.



NOTE
THE EXTERNAL CABLES TO THE CONTROL PANEL
ARE SUPPLIED WITH DISC FILE

FIGURE 1 DISC SYSTEM CONFIGURATION

The INTERDATA Standard 40 Mega-Byte Disc System (M46-429/M46-430) is a single file system. The system can be expanded by Product M46-431/M46-432 to a four file system. The following procedure is used for the expansion of the disc system.

1. Install the 17-315 DC cable between the disc control board (35-532) and the control panel (09-067) (see Information Drawing 02-359D12). Cable 17-315 is supplied with the expansion Product M46-431/M46-432.

2. Remove the signal cable terminator from last file on system and install it on the expansion file.

3. Install the DC cable between the control panel and the expansion drive.

4. Install the signal cable between the last file on the system and the expansion file.

6. AC POWER INSTALLATION (DISC FILE)

Figure 2 illustrates the preferred AC power installation for the 208/230 60Hz and the 230 50Hz systems.

The control panel requires an AC source of 115 volts 50/60Hz or 230 volts 50/60Hz. The desired operating voltage is selected by a 115/230V control switch located on the rear of the control panel.

7. AC POWER REQUIREMENTS

Disc Drive: Voltage Requirements

27-060F01/F03	208/230 volts 60Hz $\pm$ 5Hz
27-060F02/F04	230 volts 50Hz $\pm$ 0.5Hz

Disc Drive: Current Requirements

27-060F01/F02/F03/F04	Starting current 20 amperes for 7 seconds Running current 4.5 amperes

8. APPLICATION OF AC POWER

The following procedure must be followed when initial AC power is applied to the disc files.

A. Insure that all AC power input connections are correct.
B. Place the controller ground switch (S1) on the control panel in the up position.
C. Set the Start/Stop Switch for the first disc file to the STOP position.
D. Set the AC Input Power Switch to the OFF position on all files.

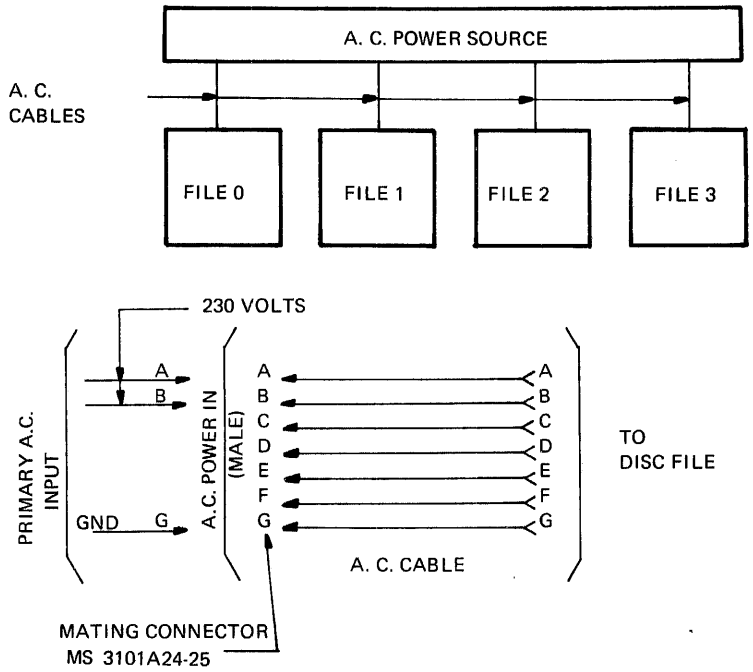
NOTE

This switch is located just above the AC power cable connector in the rear of the disc file.

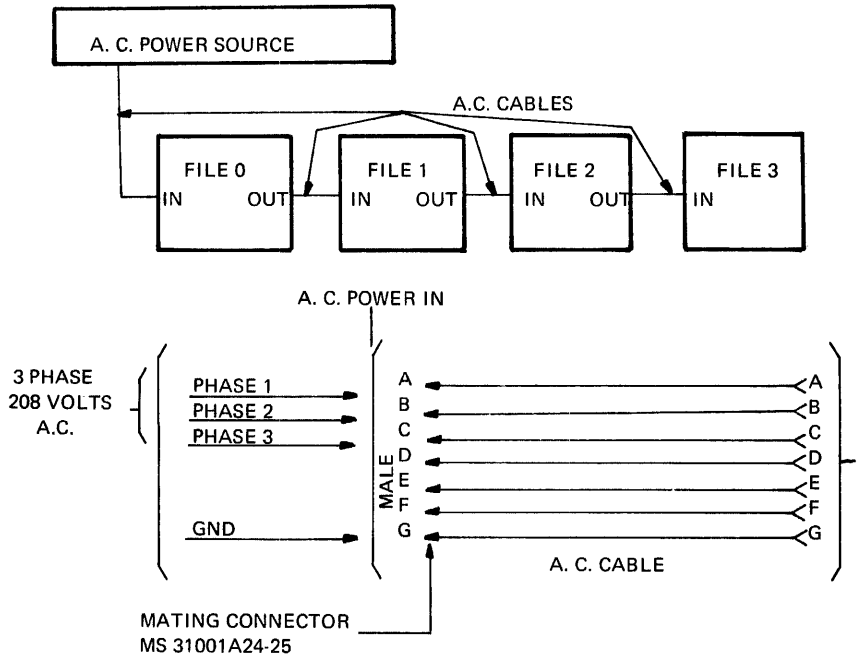
E. Apply Primary AC power.
F. Set the AC Input Power Switch to the ON position for the first drive in the system. The fans in the disc file should operate when AC power is applied.
G. Set the START/STOP switch to the START position. The disc pack should start to rotate when switch is turned on. If rotation does not occur, check the following:

   1. Controller Ground from Control Panel.
   2. AC Input Power.
   3. Fuses in Disc File.

H. Repeat Steps F and G for each succeeding disc file in system.



230 VOLTS 50 Hz or 60 Hz
SINGLE PHASE
POWER CONFIGURATION



208 3 PHASE
POWER CONFIGURATION

FIGURE 2. POWER CONFIGURATION

9. TESTING

Load test program 06-164 and run the test as described in 06-164A15.

NOTE

The disc pack must be formatted before the test program can be run.
Test 5 of the test program is the formatting test for the system.

10. ADDITIONAL INFORMATION

Additional information for the disc file may be found in the Vendor Operation and Maintenance Manual (29-400).

11. INSTALLATION OF DISC CONTROLLER ON MUX BUS SWITCH

In some system configurations, it may be required that the Disc Controller be installed on a Mux Bus Switch which is between the Disc Controller and the Selector Channel. In this configuration a 47pf (22-007F04) must be added to the disc controller. Refer to the Functional Schematic 02-359D08, Sheet 14 and Component Locator 35-532E03 for location to add the 47pf capacitor.

M46-429

40 MEGA-BYTE DISC SYSTEM MAINTENANCE SPECIFICATION

1. INTRODUCTION

The INTERDATA 40 Megabyte Removable Pack Disc system consists of the following:

1 each 35-531	File Control Board (15 Inch)
1 each 35-532	Disc Control Board (15 Inch)
1 each 09-067	Control Panel
1 to 4 27-060	Disc Drives
1 each 24-057	Formatted Disc Pack

The controller (35-531 and 35-532), which is used on the SELCH Bus, handles all communications between the Processor and the disc drives. Each controller can support from one to four disc drives with overlapping Seek and Restore.

For a relationship between product numbers and part numbers for the hardware components required for the different disc systems, refer to the Installation Specification, 02-357A20, provided in the 40 Megabyte Disc System Instruction Manual, Publication Number 29-387.

A simplified block diagram of the system is illustrated in Figure 1.

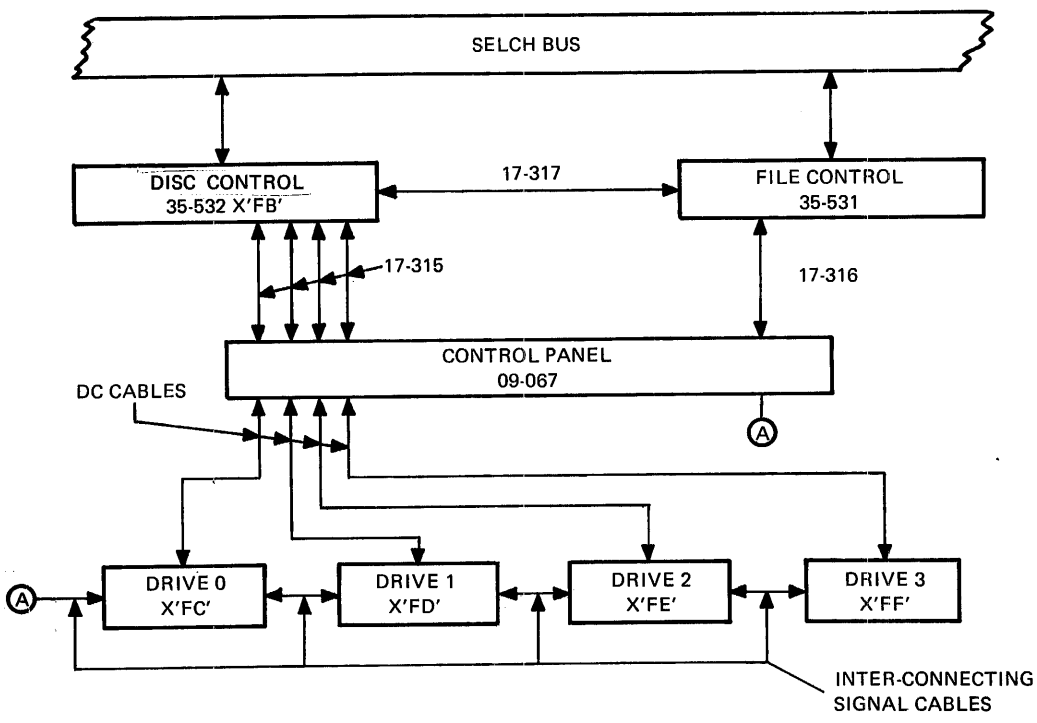


Figure 1. Simplified Block Diagram

2. SCOPE

This specification provides the information necessary to maintain the 40 Megabyte Disc Controller. Included in this specification is a block diagram, functional schematic analysis, timing information, and device address information.

3. BLOCK DIAGRAM ANALYSIS

3.1 Introduction

Refer to the block diagram 02-359D08, Sheet 2 for the following description.

The INTERDATA 40 Megabyte Disc Controller consists of two 15 inch printed circuit boards plus a control panel. The two printed circuit boards are installed in adjacent slots on the Selector Channel Bus, with the disc control board having the highest interrupt priority. Interconnection between the two boards, is made by cable (17-317) on Connector 2 of each board.

The control panel has three functions:

1. Service panel for connecting the cables between the disc drive and the control board.
2. Provides +5 volts for the signal cable terminator.
3. Provides a master control signal to the disc drive (controller ground).

The higher priority of the Disc Control Board (35-532) is obtained by the RACK0 - TACK0 priority wiring on the back panel. The Disc Control Board is placed at one priority on the SELCH Bus and the File Control Board (35-531) is placed at the next lower priority.

The priority of the interrupts of the disc drive is via the interrupt priority circuit on the File Control Board.

3.2 Disc Drive Address Selector and Module Select Circuit

The selection of the desired disc drive is via this selector circuit. It derives the disc drive address from the address portion of the control signals from the I/O circuit (DAG, SRG and CMG).

The module select circuit obtains its control from the address selector. The module select line of the desired disc drive is activated and sent to the disc drive via its unique D. C. cable.

3.3 Head/Cylinder Register

The Head/Cylinder register serves as a dual register. On a set head command, it contains the head selection information for the disc drive, and on a set cylinder command, it contains the cylinder address information for the disc drive.

3.4 Tag Line Control and Timing

There are three tag lines (control lines) associated with the information sent to the selected drive.

1. Set Cylinder Tag
2. Set Head Tag
3. Control Line Tag

The Tag Line Control and Timing Circuit derives its information from either the I/O circuit of the File Control Board or from the Disc Control Board depending upon the operation to be performed. Its purpose is to provide the necessary control signals and timing of these signals for all control information sent to the selected disc drive.

3.5 Module Selected MUX

The module selected multiplexor (MUX) determines if the desired disc drive has been selected after the module select signal is activated.

3.6 Selected Drive Status Circuit

Part of the status of the selected disc drive is condensed and fed to the Disc Control Board status circuits and to the I/O for the File Control Board.

3.7 Bus Line Multiplexor

The Bus Line MUX Multiplexes the control information to the selected disc onto nine bus lines.

3.8 Bus Line Drive/Receivers

The I/O buffering between the signal cable and the File Control Board is provided by the Bus Line Drivers and Receivers.

3.9 Cabling Definition

1. DC Cable - This is a unique cable to each disc drive.
2. Signal Cable - This provides a daisy-chain bus to the disc drives. The signal cable to the first drive is connected to the control panel.

3.10 Sector Counter

The Sector Counter counts the sector pulses from the selected disc drive. Its output information is used in the sector match circuit.

3.11 Sector Sync. Circuit

The Sector Sync Circuit inhibits a sector match condition from occurring until the sector counter is in sync after a disc drive address change.

3.12 Sector Match Circuit

The matching condition between the Sector Counter and the Sector Register occurs in the Match Circuit. Its function on a match is to generate a sector match signal which activates the Read/Write gate control logic.

3.13 Cylinder/Head/Sector Registers

The information for the header field of the sector data is contained in these registers. The registers are loaded from the Processor before a normal Read/Write command is issued. The information contained in these registers is used to compare the header field of the data read from the disc file. The contents of the registers is serialized via the parallel to serial converter and is fed to the Header Match Circuit.

3.14 Header Check Circuit

The Header Check Circuit compares the header field of the data being read (normal Read/Write) from the disc drive to the serialized data information from the parallel to signal converter on a bit by bit basis.

3.15 Read/Write Control

The Read/Write control derives control signals for performing data transfer to and from the selected disc drive. The input information to the Read/Write control is from an output command from the Processor.

3.16 Buffer Registers

There are two buffer registers for data transfer from the selected disc drive and the Processor. The functions of the two registers are:

Write Operation:

Buffer Register 1	Parallel Load Register Data load from the Processor
Buffer Register 2	Shift Register Shifts out data to the disc drive

Read Operation:

Buffer Register 1	Shift Register Shifts in data from the disc drive
Buffer Register 2	Parallel load register Data fetched via the Processor

3.17 Write Oscillator/Write Data Control

The Write Oscillator is a crystal controlled clock which provides the timing source for the Write Data Control Circuit. The final double frequency data stream is generated via the Write Data Control Circuit from the data shifted out of Buffer Register 2.

3.18 Sync Byte Match Circuit

The Sync Byte (X'03') which appears between the data burst of all zeros and the first data character is detected by the Match Circuit.

3.19 Read Data MUX Logic

These circuits multiplex the Read Data Lines of the four unique DC cables into a single data signal. The MUX is under the control of the disc drive address selection logic.

3.20 VFO (Variable Frequency Oscillator)

The VFO provides the necessary timing and logic for separating the data and clock signals of the incoming double frequency read data stream.

3.21 Write Data Select Logic

The output double frequency write data stream is sent to the disc drives by the four unique write data lines of the DC cable.

3.22 Byte Counter

The byte counter is a twelve stage binary which serves as a bit and byte counter. The first three least significant stages function as a bit counter and the other stages function as a byte counter.

3.23 LRCC Register and Check Circuit

The LRCC Register generates a sixteen bit check character. On writing to the selected disc drive, this check character is inserted in the data field after the last byte of data. On reading data from the selected disc drive, the LRC Characters are regenerated and compared to the LRC Character written at the end of the data field. The Check Circuit makes the comparison and on a mis-match, an error flag is set.

3.24 Read/Write Control

This controls the activation and de-activation of the control gates (Write Gate, Read Gate, and Erase Gate) signals for reading and writing to the selected disc drive.

3.25 Disc Control Status

The Disc Control Board status is derived and passed to the I/O circuits.

3.26 Interrupt Circuit

The interrupt from the controller idle status line is generated.

4. INTERFACE DEFINITION (All Signals Are Low Active)

4.1 DC Cable

4.1.1 WRITE DATA (WD). Unique coax line * used to transfer Write Data to the selected Disc Drive.

4.1.2 READ DATA (RD). Unique coax line used to transfer Read Data from the selected drive.

4.1.3 MODULE SELECT (SMOD). A unique line used to select the disc drive.

4.1.4 SELECTED MODULE (MSEL). A unique line indicating that the disc drive is selected and not unsafe.

4.1.5 GATED ATTENTION (GATN). A unique line from the disc drive indicating the following:

1. The power-on sequence is completed.
2. Seek operation is completed.
3. A Restore operation is completed.

Gated Attention remains active until:

1. Disc drive is selected and Read Gate is activated.
2. A new Seek operation is initiated.
3. A Reset Gate Attention output command from the Processor is received.

4.1.6 +5 Volts for Terminator. This line supplies the +5 volt source for the signal cable terminator.

4.1.7 DC Ground. This line provides a DC ground path between control panel and the disc drive.

* A unique line is a separate line between the controller and each disc drive.

4.2 Signal Cable

The signal cable contains the nine bus lines and associated tag lines (control) to transmit control information to the selected disc drive along with the return status signals from the selected disc drive.

4.2.1 Control Tag (CT). This tag line enables the selected disc drive to perform the operation as specified on the nine bus lines. Table 1 indicates the Bus Line Definitions.

4.2.2 Set Cylinder Tag (SCT). This tag line loads the Cylinder Address Register of the selected disc drive with the contents of the nine bus lines (see Table 1).

4.2.3 Set Head Tag (SHT). This tag line loads the Head Address Register of the selected disc drive with the contents of the bus line (Bus Line 4-8, see Table 1).

BUS LINE	CONTROL FUNCTIONS	CYLINDER REGISTER	HEAD REGISTER
0		256	
1	WRITE GATE	128	
2	READ GATE	64	
3	SEEK	32	
4	RESET HEAD REG.	16	16
5	ERASE GATE	8	8
6	SELECT HEAD	4	4
7	RESTORE	2	2
8	HEAD ADVANCE	1	1

Table 1. Bus Line Definitions

4.2.4 Bus Line Definition (Control Lines to Selected Disc Drive).

4.2.4.1 Bus 1-Write Gate (WRTG). This bus line specifies to the selected disc drive that the data on the Write Data Line is to be written on the current location of the disc pack.

4.2.4.2 Bus 2-Read Gate (RGAT). This bus line specifies to the selected disc drive that the data at the current location of the disc pack is to be transferred on the Read Data Line to the controller.

4.2.4.3 Bus 3-(Seek). This bus line (pulse) signal starts a seek operation on the selected disc drive.

4.2.4.4 Bus 4-(Reset Head Register). This bus line (pulse) signal resets the Head Address Register of the selected disc drive to the 0 state (Head 0).

4.2.4.5 Bus 5-Erase Gate (ERASG). This bus line enables the selected head of the selected disc drive to straddle erase the data being written. It goes active at the same time as Write Gate and remains active until 20 microseconds after Write Gate is inactive.

4.2.4.6 Bus 6 (Select Head). This bus line selects the head of the selected disc drive to Read or Write. The contents of the Head Address Register determines which head is to be selected.

4.2.4.7 Bus 7 (Restore). This bus line (pulse) signal restores the selected disc drive to Cylinder 000.

4.2.4.8 Bus 8 (Head Advance). This bus line (pulse) signal increments the Head Address Register of the selected disc drive by one.

4.2.5 Signal Cable Status Lines (Selected Disc Drive to Controller).

4.2.5.1 Ready (DRYD). This status line indicates that a seek command has completed successfully and the disc drive is ready to Write or Read.

4.2.5.2 On-Line (ONL). This status line indicates that the drive is ready to be operated by the controller.

4.2.5.3 Index (INEX). This status line provides a pulse indicating the beginning of a track.

4.2.5.4 Unsafe (USAF). This status line indicates that the disc drive is unsafe.

4.2.5.5 Seek Incomplete (SIC). This status line indicates that the disc drive has failed to complete the following:

1. An initial Seek in 600 milliseconds.
2. A Restore in 600 milliseconds.
3. A normal Seek in 100 millisecond.

4.2.5.6 End of Cylinder (EOCY). This status line is activated if the contents of the Head Address Register are equal to or greater than a decimal 20. It remains active until the contents of the Head Address Register are changed.

4.2.5.7 Write Current Sense (WCUR). This status line indicates that write current has been sensed by the drive. It becomes active within 10 microseconds of the Write Gate signal.

4.2.5.8 Sector (SECM). This status line provides a pulse each time that a sector slot of the pack has been detected.

4.2.5.9 Ready Only (ROLY). This status line is activated via the Read-Only Switch of the drive. It indicates that the drive is in the Write Protect state.

4.2.5.10 Controller Ground (CG). This is a bussed line in the signal cable used for master control of all disc drives connected to the controller. It is generated in the control panel (09-067). When active, it energizes the sequence relay of the drive which allows the powering up to the drive. On de-activation of the controller ground signal, the following sequence takes place:

1. Immediate Head Retraction.
2. Enters the power down sequence.

4.2.5.11 Sequence Power (First Drive to Controller). This line provides a voltate (+24 volts) to the controller which indicates that the controller ground signal is active and power is applied to the drive.

4.2.5.12 Sequence (IN/OUT). The sequence power signal is returned to the first drive via the control panel. On the receipt of this signal, the Power On sequence is initiated.

When more than one drive is connected to the controller, the sequence IN/OUT signal is developed by the preceding drive. When the pack rotation speed is approximately 70% of the operating speed, the sequence IN/OUT signal is applied to the next drive, thus initiating the Power On sequence for the next drive.

5. BUS LINE AND CONTROL TAG TIMING (From Controller to Selected Drive)

The Bus Line and Control Tag Timing is illustrated in Figure 2. This relationship holds for all pulse type control functions such as Set Head Register, Set Cylinder Register, Seek, Restore and Reset Head Register. For a read/write operation, the Control Line Tag (CT) is active for the duration of the operation (see Figure 3).

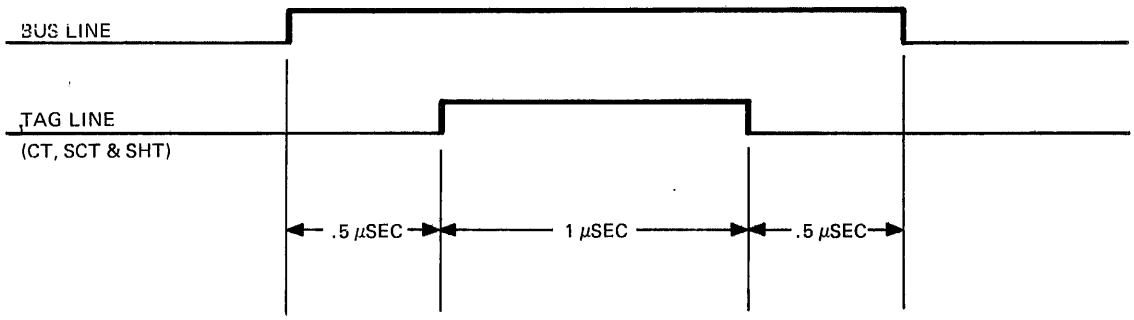


Figure 2. Bus Line and T A G Line Timing

6. CONTROL FUNCTION SEQUENCES

A certain set of control functions must be initiated in the proper sequence to read or write from a given location on the disc pack. Figure 3 illustrates a typical sequence of the control functions to read and/or write to a given location on the disc pack. Refer to 02-357A22, 40 Megabyte Programming Specification which is provided in the 40 Megabyte Disc System Instruction Manual, Publication Number 29-387 for the proper programming operations to initiate the sequence of the control functions.

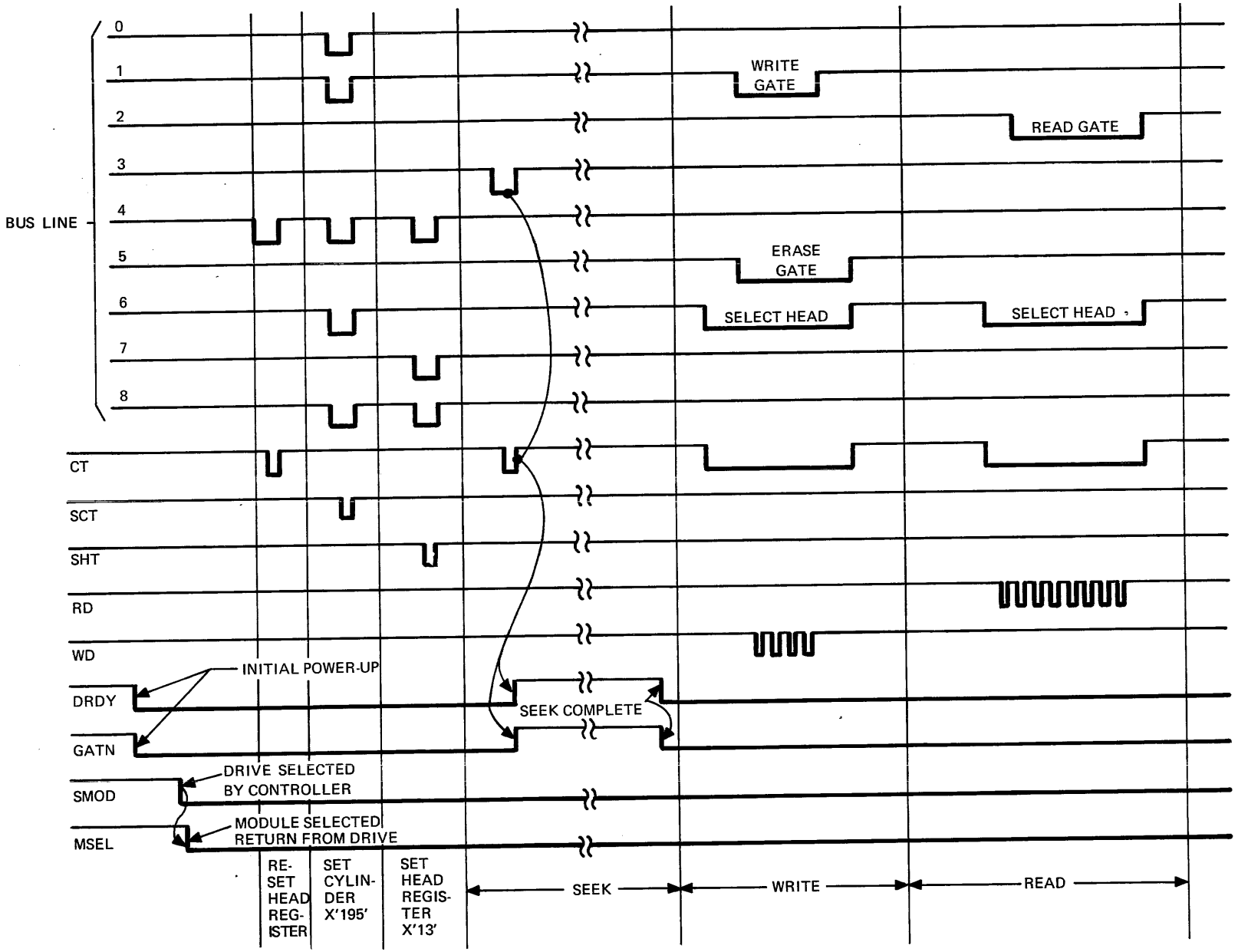


Figure 3. Control Functions Sequence

7. FUNCTIONAL SCHEMATIC ANALYSIS

7.1 Introduction

The INTERDATA 40 Megabyte Controller is designed to connect from one to four disc drives to an INTERDATA Processor equipped with a Selector Channel.

Refer to functional schematic 02-359D08 and 09-067D08 and to the timing diagrams provided in this specification during this functional schematic analysis. The File Control Board Circuits are provided on Sheets 3 to 6 of 02-359D08 and the Disc Control Board Circuits on Sheets 7 to 15 of 02-359D08.

7.2 Device Addresses

The disc controller and each disc file (drive) has a unique device address. The preferred device addresses are:

Controller Address	X'FB'
Disc File 0	X'FC'
Disc File 1	X'FD'
Disc File 2	X'FE'
Disc File 3	X'FF'

The device addresses of the Disc Control Board and the File Control Board are set by the hexadecimal code switches. The following setting of the switches provides the preferred device address (Sheets 3 and 7 of 02-359D08):

Disc Control Board

Location	Switch Postiion
A53	X'F'
A42	X'B'

File Control Board

Location	Switch Position
A49	X'F'
A38	X'C'

The hex switches may be set in combinations to provide different device addresses. An example is:

Disc Control Board	Switch Position
A53	X'C'
A42	X'1'

File Control Board	Switch Position
A49	X'D'
A38	X'0'

With the preceding switch setting, the disc controller responds to the following set of addresses:

Disc Controller	X'C1'
Disc File 0	X'D0'
Disc File 1	X'D1'
Disc File 2	X'D2'
Disc File 3	X'D3'

7.3 Processor Communication

Communication between the Processor via the Selector Channel bus is handled by the standard INTERDATA I/O sections of the two control boards (Sheets 3 and 7 of 02-359D08). Refer to the INTERDATA User's Manual, Publication Number 29-261, for a description of the I/O operation.

7.4 Initialization

The controller can be initialized by one of two operations: System Clear, or by a Reset output command. The status of the disc controller, X'FB', is X'OB' after initialization. The status of the disc drive is a function of the state of the address drive.

Upon initialization, the interrupt control circuit of both the Disc Control Board and the File Control Board is placed in the disarm state (interrupts are not queued).

7.5 Interrupt Control, Generation and Priority

7.5.1 File Control Board. Each file has its own interrupt control circuits and interrupt generation circuits. (See Sheet 4 of 02-359D08). The interrupt generation circuit can be controlled independently of the other files. The interrupt control functions are:

1. Disarm - no queueing of interrupts.
2. Disable - queueing of interrupts.
3. Enable - permits interrupt to be passed to the Processor.

The desired interrupt control can be provided by issuing an output command to the desired disc file.

The interrupt generation circuit consists of a queueing flip-flop and gating for setting the flip-flop for each disc file (Sheet 4 of 02-359D08).

Interrupts are generated under the following conditions providing the interrupt control for the associate circuit is not in the disarm state.

1. GATN-1——►1
2. An interrupt is generated on any command (SRG, DAG, or OC) directed to the file if the file is: 1) unsafe, 2) not on line, and 3) not selected.

The interrupt priority for the file control board is set by the interrupt priority circuits (Sheet 4 of 02-359D08). It is configured to provide the following priority of the four disc drives.

Priority	Disc Drive	Device Address
Highest	0	X'FC'
Next	1	X'FD'
Next	2	X'FE'
Next	3	X'FF'

The interrupt priority circuits also control the least two significant bits (IAD11 and IAD21) of the address byte that is returned on an acknowledge interrupt instruction. The following shows the relationship between the interrupting drive and the states of the IAD11 and IAD21 address control bits.

Drive	Device Address	IAD11	IAD21
0	X'FC'	0	0
1	X'FD'	1	0
2	X'FE'	0	1
3	X'FF'	1	1

The interrupt circuit of the File Control Board is placed in the disable state when the Disc Control Board is not idle by (FCNI0).

7.5.2 Disc Control Board. The Disc Control Board has its own interrupt generation and control circuits (Sheets 7 and 11 of 02-359D08). The interrupt control functions for the disc control board are:

1. Disarm - no queuing of interrupts.
2. Disable - queuing of interrupts.
3. Enable - permits interrupt to be passed to the Processor.

The interrupting source for the disc controller is the status function controller idle (see Sheet 11 02-359D08) which generates an interrupt on the following signal change:

CIDEL ——→1

Priority of the Disc Control Board with respect to the File Control Board is set via the Rack0/Tack0 back panel wiring.

7.6 File Address Selection

The disc file is selected by means of the File Address Selection Logic (see Sheet 5 02-359D08). The two least significant bits (D151 and D141) of the data byte associated with ADRS0 are decoded to provide a one out of four file selection signal. The result of the one out of four decoding of D151 and 141 is loaded into the four bit latch (FSEL00 to FSEL30) on the positive edge of the file address gate (FADGO) (see Timing Diagram, Figure 4) after which it is buffered (SMOD01 to SMOD31) and sent to the disc file as a module select signal on the DC cable (via way of the Disc Control Board).

7.7 File Address Change Logic

The File Address Change Logic (Sheet 5 02-359D08) generates a signal (FCGO) on each file address change. FCGO (see Figure 4, Timing Diagram) occurs during the address portion (ADRSO) of any command (SRG, DAG and CMG) directed to a disc file, if the preceding file address selection is not the same as the address of the command being issued. The results of the one out of four decoding of D151 and 141 and the File Select Signals (FSEL00 to FSEL30) is sampled by FADG (see Figure 4 for timing) to produce the file change signal FCGO. Its function is to indicate to the Sector Sync. Circuit of the Disc Control Board that a file change has been made.

7.8 Sync Return (File Control Board)

The Sync return pulse (SYNCO) to the Processor is delayed until the ADSYD delay times (see Figure 4) out (approx. 700 nanoseconds). This allows time for the module selected signal (MODS1) to be returned to the controller from the disc drive before continuing the command (SRG, DAG and CMG). The sync return pulse is delayed by 100 nanoseconds for the SRG, DAG and CMG control pulse from the processor. On the Disc Control Board, a fixed delay of 100 nanoseconds is incorporated for the sync return pulse for ADRS, SRG, CMG, DRG and CMG.

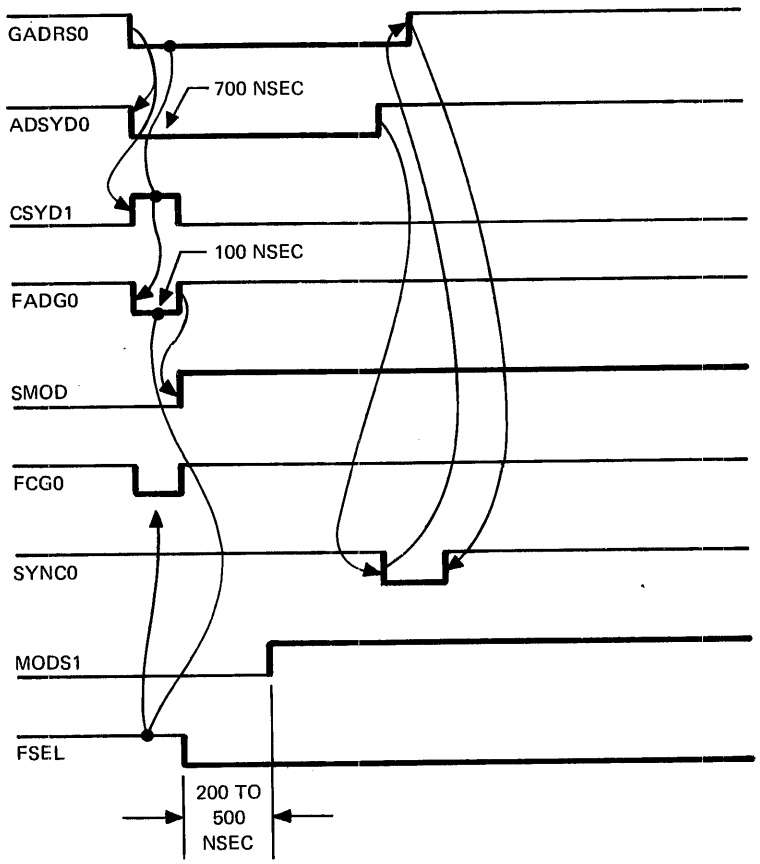


Figure 4. File Address Selection Timing

7.9 File Status (Sheet 5 of 02-359D08)

There are four unique status lines from the disc files (GATN00 to GATN30) which are used for interrupt generation (GATN01 to GATN31) and to provide the gated attention status bit. The gated attention status bit (GATNSY) is derived by gating the four gated attention signals with the file select signals (FSEL01 to FSEL31) providing the gated attention status for the selected disc file.

The rest of the file status (USAF0, WCUR0, ROLY, etc.) is derived directly from the file status line (Refer to Programming Specification 02-357A22 for definitions of the file status.) The file status is also condensed for use on the Disc Control Board. The two condensed status lines, FST11 and FST21, are active on the following conditions:

FST11

1. Drive is unsafe (USAF).
2. Seek Incomplete (SIC).
3. File not on line (ONL).
4. File is not ready (DRDY).

FST21

1. If an attempt to write to a write protected file, FST11 becomes active (ROLYF0).
2. If the write current sense status of the file is not present within 25 microseconds of the erase gate becoming active, the FST11 status signal will be active (WCURF1).

The module selected status lines are unique for each disc file. The four status lines (MSEL11 to MSEL21) are gated by the file select signal (FSEL11 through FSEL21) to produce a module selected status (MODS1) for the select disc file.

The following three file status signals are buffered on the File Control Board and then fed to the Disc Control Board.

1. Sector Mark (SECM).
2. Index Mark (INEX).
3. End of Cylinder (EOCY).

7.10 Head/Cylinder Register (Sheet 6 of 02-359D08)

The Head/Cylinder Register (12 bits) is the storage register for retaining the Head/Cylinder information for the Set Head Register and Set Cylinder Command. It is loaded under control of the Head/Cylinder Load Control Circuit (Sheet 4 of 02-359D08). To load the register, two consecutive write data instructions or a write halfword instruction must be issued from the Processor. The four most significant bits of the register are loaded on the first write data (DAG) by the load signal (LFB0). The lower order eight bits are loaded by the second write data (DAG) by the load signal (LSB0).

7.11 File Command (Sheet 6 of 02-359D08)

There are seven flip-flops associated with the generation of the file commands. Each file command is set into one of the flip-flops by an output command from the Processor, except the Advance Head Command which is generated by the Disc Control Board. The following is the relationship between the output command from the Processor and the active file Command flip-flop:

Output Command	Command Flip-Flop
Set Head Register	SHF
Set Cylinder Register	SCF
Reset Gated Attention	RGAF
Seek	SEKF
Reset Head Register	RSHF
Restore	RESF0
Command from Disc Control Board	
Advance Head Register	HADVF

The Command flip-flop associated with the output command from the Processor is set on accepting the command and is reset by the end of Tag Delay Gate (ETDG0). (See Figure 5, Tag Gate Generation Timing.)

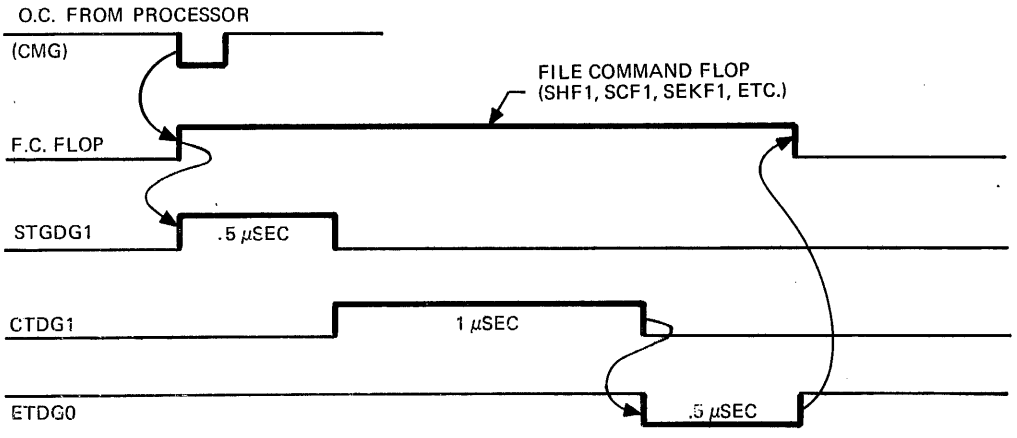


Figure 5. T A G Gate Generation Timing

7.12 Tag Gate Generation (Sheet 6 of 02-359D08)

The control tag gate is generated from the File Command flip-flops (see Figure 5, Tag Gate Generation Timing). The Tag Gate (CTDG1) is centered with respect to time, such that the File Command flip-flop is set approximately 0.5 microseconds before the tag gate and remains set until approximately 0.5 microseconds after the tag gate.

7.13 Bus Line Mux (Sheet 6 of 02-359D08)

The multiplexing of the Head/Cylinder register information and the file commands onto the nine bus lines to the disc file is derived by three 2:1 multiplexors. The Bus Line Multiplexor is under the control of the Set Cylinder Head (SCH1) signal. If SCH1 is low, the contents of the Head/Cylinder register are gated onto the bus lines. If SCH1 is high, the file command information is gated onto the bus lines. The Bus deactivate signal (BUSDA1) is a master control for the bus lines. It is normally low which enables the multiplexors. The bus lines are disabled (all bus lines high) when the power is removed or lost on the control panel (09-067). On the loss of Power On, the control panel BUSDA1 goes high.

7.14 Sector Counter (Sheet 12, 02-359D08)

The following discussion pertains to the Disc Control Board.

The Sector Counter is an eight bit counter (the two most significant bits are not used) which counts the sector pulses returning from the selected disc file (see Figure 6, Sector Counter Timing). The counter is synchronized to state 0 each time the sector mark representing sector 0 is present. When the index mark (INEX) is present, the INF flip-flop is set. It remains set until the trailing edge of sector mark 0. The counter is clear and held in the clear state (state 0) by the coincidence of the INF flip-flop being set and the presence of sector mark 0. The leading edge of the sector mark pulse (SECM1) is used to generate DSECM0 which advances the sector counter.

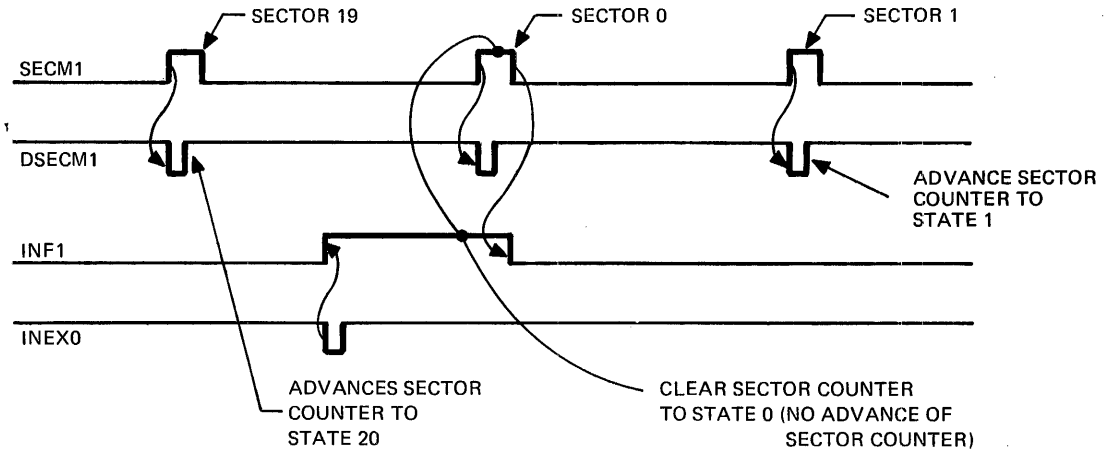


Figure 6. Sector Counter Timing

7.15 Sector Synchronization (Sheet 12 of 02-359D08)

The Sector Synchronization circuit is not used to synchronize the sector counter, but is used to allow synchronization with the Index mark (pulse) on a file address change. The IEXS flip-flop (see Figure 7, Sector Sync Timing) is reset on any file address change by FCG0 and is set on the trailing edge of the Index pulse, INEX0. If the IEXS flip-flop is reset, it inhibits (by IEXS0) the Sector Match circuit (Sheet 9 of 02-359D08) from indicating a match condition until an index pulse is present after a file address change.

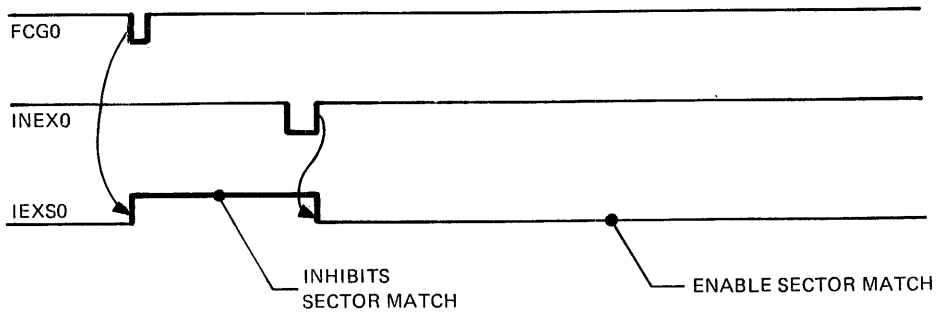


Figure 7. Sector Sync Timing

7.16 Sector, Head and Cylinder Registers (Sheet 8 of 02-359D08)

The Sector, Head, and Cylinder registers are loaded by three consecutive write data instructions or by a write data instruction followed by a write halfword instruction from the Processor. On the first write data (DAG), the sector register is loaded by LSRG0. The second write data (DAG) loads the head register and the two most significant bits of the cylinder register by LHRG0. The eight least significant bits of the cylinder register are loaded on the third write data (DAG) by LCRG0. The three load signals for the registers are generated under the control of the Sector/Head/Cylinder load control circuit (Sheet 11 of 02-359D08).

On multi-sector operations, the sector register is advanced by one state by CONTG0 and cleared to state 0 by GINEX0. Also on multi-sector operations, the Head Register is advanced by one state on the occurrance of GINEX0. The cylinder register is not advanced for multi-sector operation.

7.17 Parallel to Serial Converter (Sheet 8 of 02-359D08)

The function of the parallel to serial converter is to serialize the parallel information of the sector, head, and cylinder registers for a bit by bit comparison to the formatted header field of the data being read from the selected disc file.

The parallel to serial conversion is accomplished by selecting the inputs to the eight to one multiplexors on a bit by bit basis. The three least significant bits (B11, B21, B41) of the Byte counter are used to control the selection of the multiplexor inputs. In conjunction with the bit by bit selection of the parallel input, the multiplexors are enabled by three enable functions, ESECTD0, EHEDD0, and ECLCD0, which are generated on an eight bit basis. These three enable functions are generated in the following order:

1st	ESECTD0
2nd	EHEDD0
3rd	ECLCD0

The final result of the parallel to serial conversion is the head data (HD1).

7.18 Sector Match (Sheet 9 of 02-359D08)

A sector match (SMAT1) occurs when the contents of the sector counter (SCM11 to SCM321) is equal to the contents of the sector register (SER11 to SER321) providing that the end of cylinder status (EOCY1) is not present or that the Sector Synchronication flip-flop (IEXS) is not reset. When either of the signals, EOCY1 or IEXS0, is high, the Sector Match circuit is inhibited.

The sector match condition is retained in the SMF flip-flop. On the trailing edge of the sector pulse. SECM1, the SMF flip-flop is set (see Figure 8, Sector Match Timing) and remains set until the clear signal (CLRA0) is present and resets the flip-flop. The SMF flip-flop is used to generate the Select Head signal (SELHS1) which selects the head that is specified by the Head Address Register of the selected disc drive.

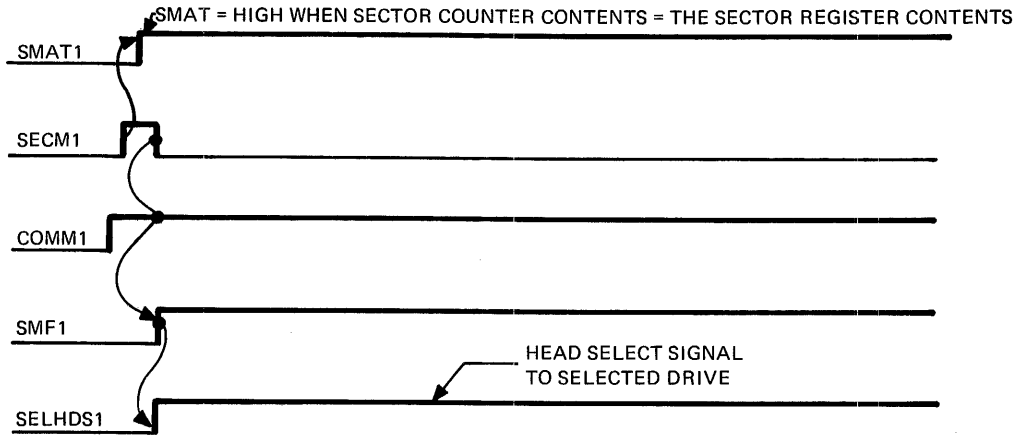


Figure 8. Sector Match Timing

7.19 Disc Command Logic (Sheet 9 of 02-359D08)

The operational command (Read, Write, Read format, Write format, or Write with Protect) specified by an output command from the processor is retained in four flip-flops (RF, WF, FMF and WPB). These flip-flops are decoded by a 1 out of 10 decoder to generate a control signal (READ, WRT, RCK, RFOMT or WFOMT) specified by the output command. The Command flip-flops are reset by the following:

1. RESET0
2. SCLR0A
3. OPEND0

On the occurrance of the End of Cylinder status (EOCY1), the control signals are deactivated by disabling the 1 of 10 decoder.

Format Switch (Sheet 9 of 02-359D08)

The format switch is a hexidecimal code switch located on the left front side of the disc control board. Its function is to allow the formatting control signals (WFOMT and RFOMT) to be activated on a format command from the Processor, if it is placed in the format position. In the non-format position, the switch inhibits the format operation from taking place. The Format position of the hex switch is position X'0'. Any other position of the switch is for normal operation.

If a format command (Read or Write format) is issued when the switch is not in the format position, the Write Protect Violation signal (WPVO) is activated. WPVO sets the Header Write Protect bit (Bit 0 of status byte for disc control board) and inhibits the read or write functions after the header data field is read.

7.20 Write Gate/Erase Gate (Sheet 11 of 02-359D08)

The sequence to generate the Write and Erase gates for a Write Format operation or a Write operation is very similar. On a Write format operation, the sequence is started on a sector match condition. On a write operation, the sequence is started after the header data field is read. Figures 9 and 10 illustrate the Write gate timing for the two operations. The Erase gate for both operations is held active for 20 microseconds after the deactivation of the write gate to provide the correct tunnel erasure of the data written.

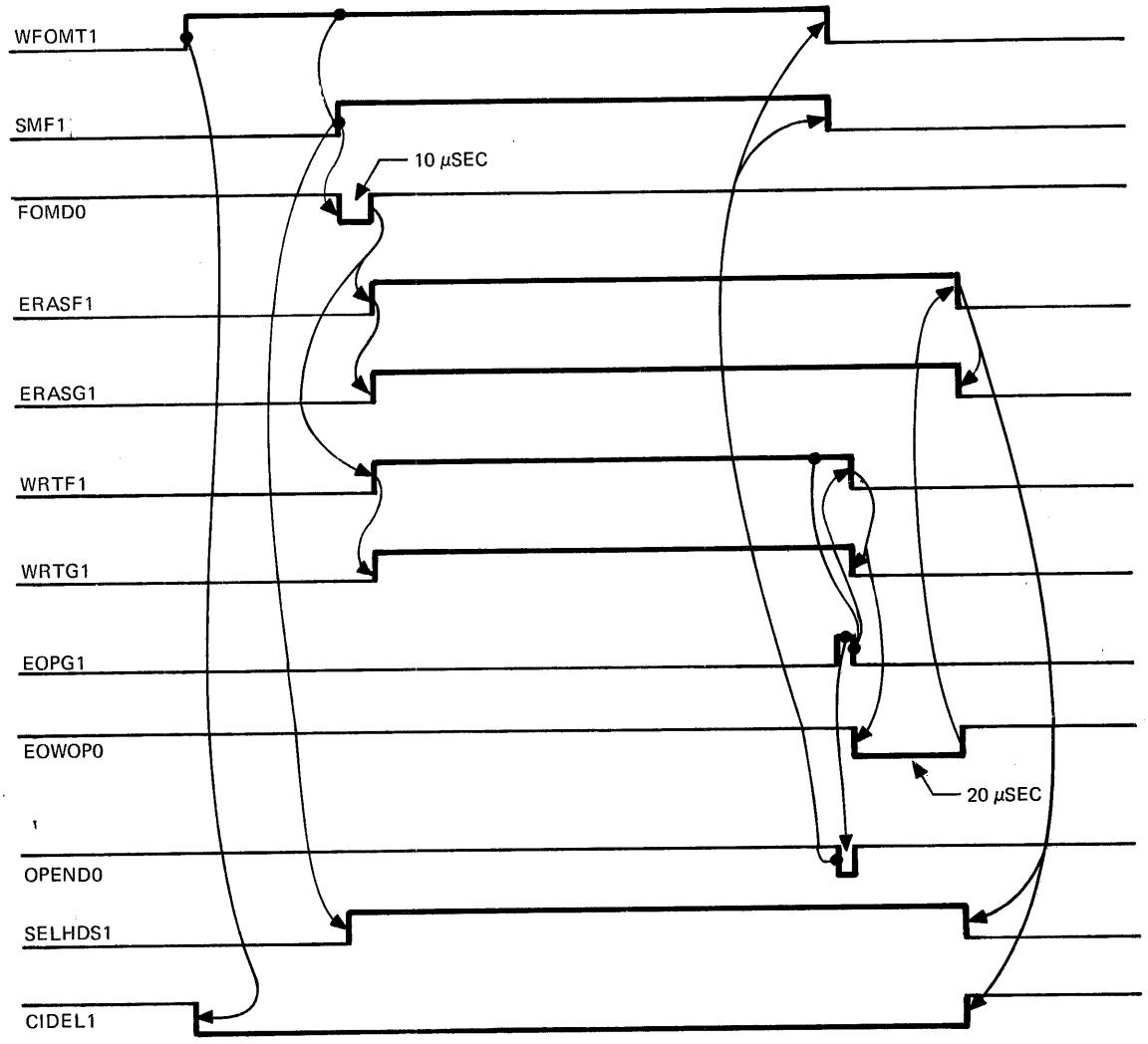


Figure 9. Erase and Write Gate Timing Format Mode

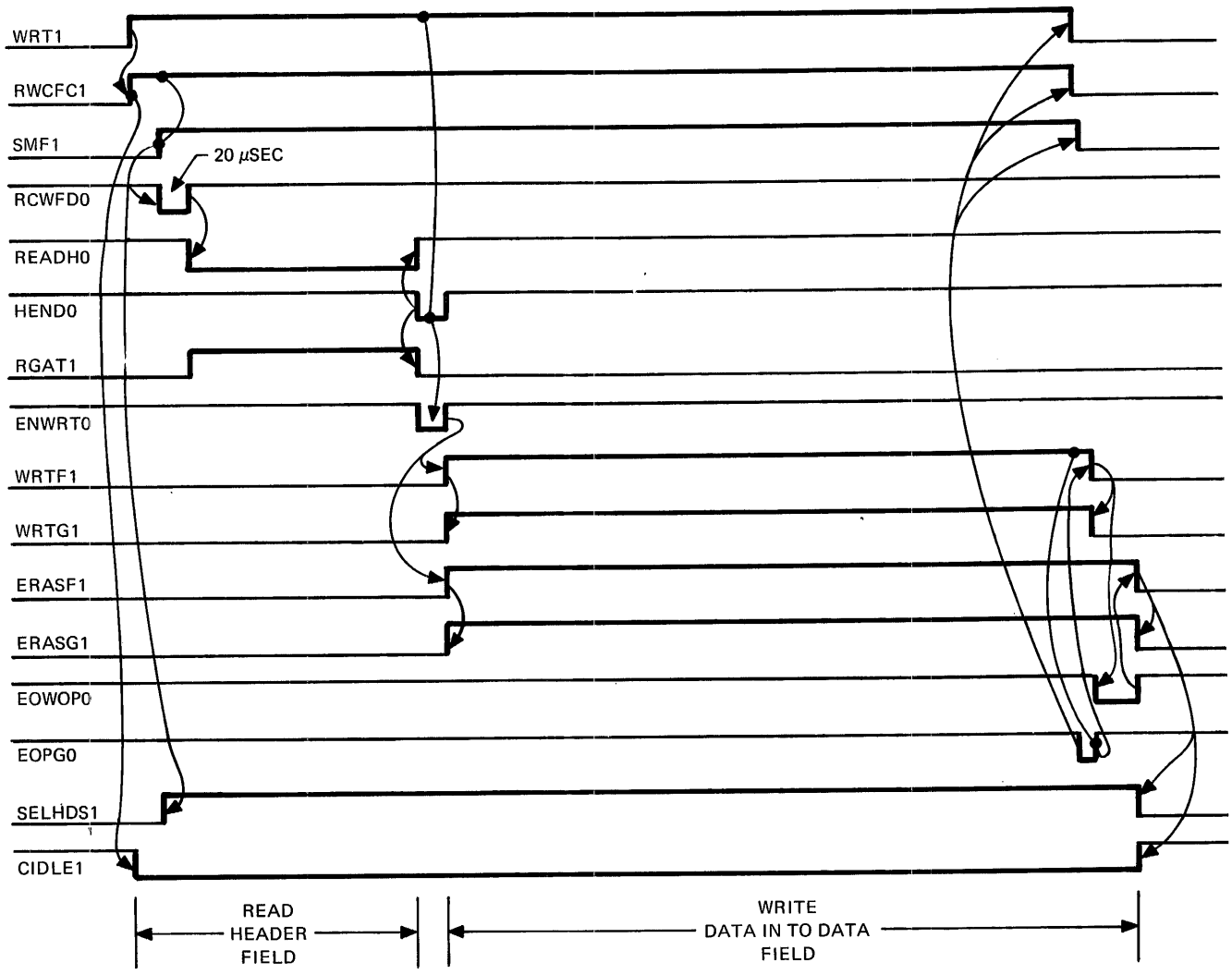


Figure 10. Write Gate Timing Normal Write Mode

7.21 Read Gate (Sheet 10 of 02-359D08)

The sequence for generating the Read Gate for the three read operations (Read, Read Check and Read Format) is very similar. Figures 11 and 12 illustrate the Read Gate Timing for the three modes of operation. The only difference in the generation sequence is that, in the Read and Read Check mode, the Read Gate signal is deactivated for 40 microseconds after the Header Data field is read. In all three modes, the operation is terminated when the end of operation signal (EOPG0) occurs.

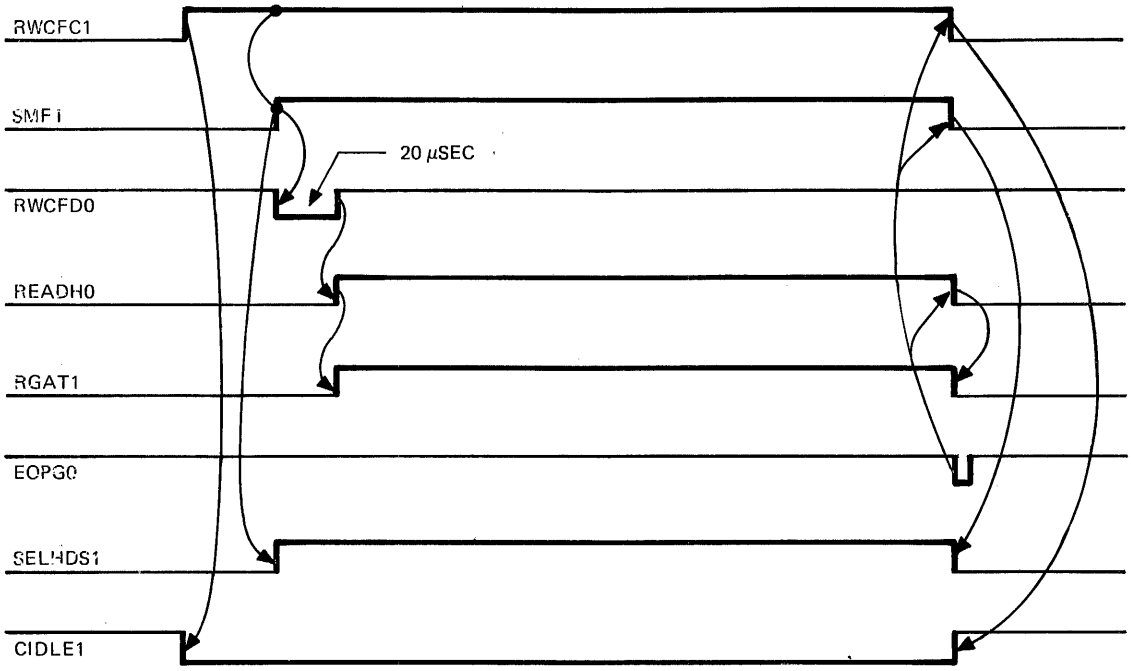


Figure 11. Read Gate Timing Format Mode

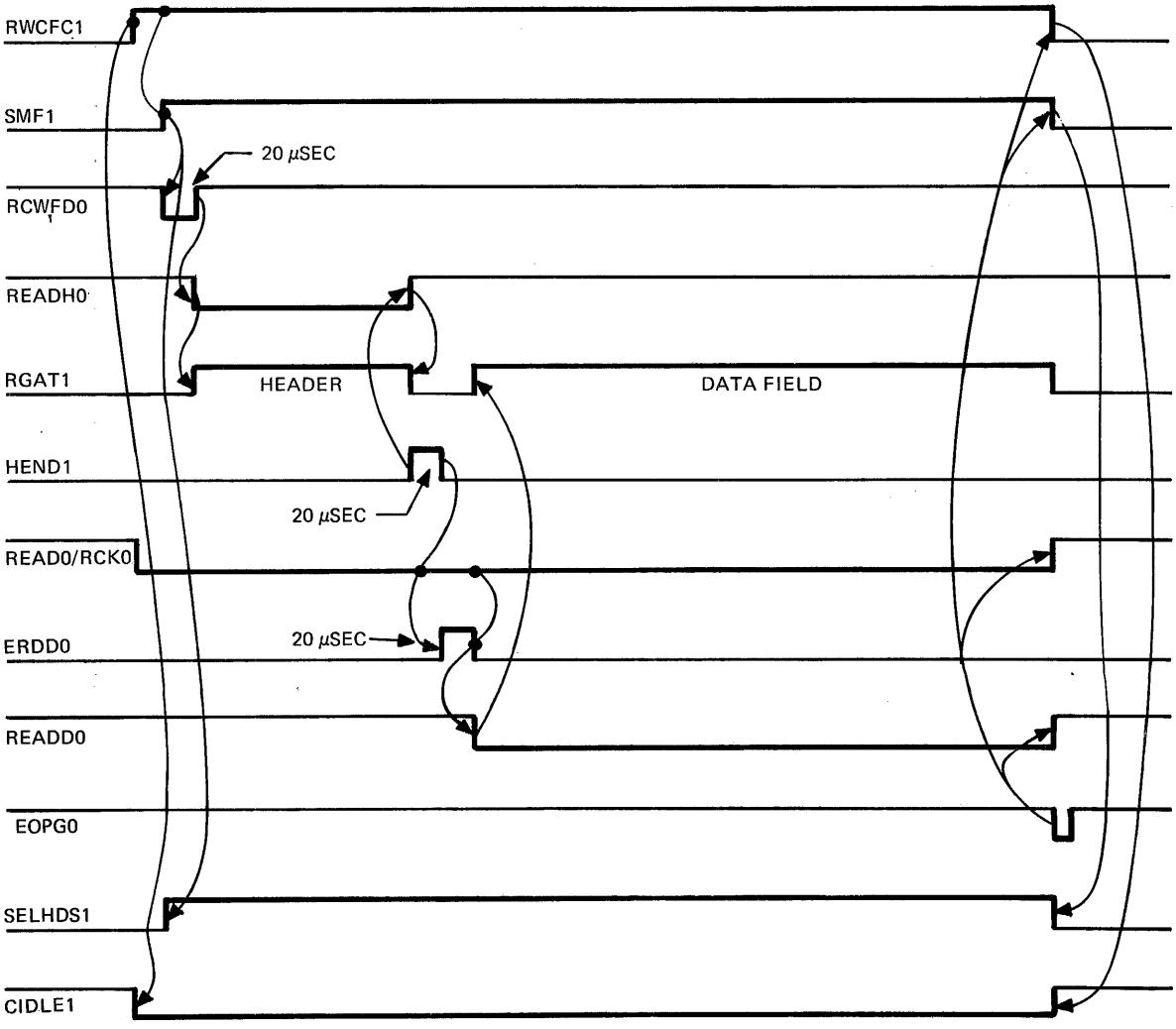


Figure I2. Read Gate Timing Normal Read and Read Check Mode

7.22 Buffer Register (Sheet 9 of 02-359D08)

There are two buffer registers associated with the transfer of data between the Processor and the selected disc file. The functions of these registers are different for the Read and Write operation modes. On a read (Read or Read Format) operation, Buffer Register 1 functions as a shift register and Buffer Register 2 functions as a parallel load register for retaining data to be fetched. In the Write (Write, Write Format) mode, the functions are in reverse to that of the Read mode. Buffer Register 1 functions as a parallel load register for retaining data to be written and Buffer Register 2 functions as a shift register.

The 19-072 four bit shift register used in the buffer registers has two control inputs (S0 and S1) for changing the operational modes of the four bit register. The four operational modes of the 19-072 are:

S0	S1	Mode
0	0	Inhibit Clock
1	0	Shift Right
0	1	Shift Left (not used on controller)
1	1	Parallel Load

The operational modes of the two buffer registers are controlled by control inputs of the four bit registers.

Write Operation (See Figure 13, Buffer Register Timing)

In the Write mode, Buffer Register 1 is parallel loaded on the leading edge of DAG0. The content of Buffer Register 1 is then parallel loaded into Buffer Register 2 on the trailing edge of the Write Bit Clock (WBCG0) during the time that PLD11 is high (PLD01 is high on a write operation). The content of Buffer Register 2 is shifted out (DAT081) on the trailing edge of WBCG0 during the time PLD11 is low.

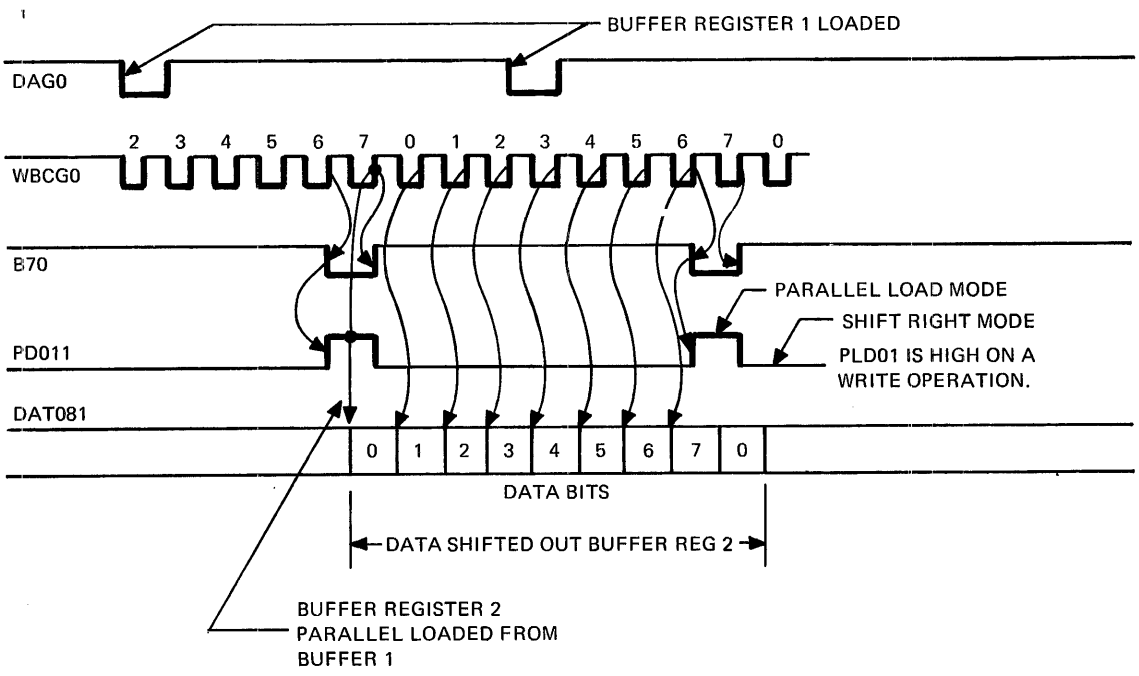


Figure 13. Buffer Register Timing Write and Write Format Modes

Read Operation (See Figure 14, Buffer Register Timing)

In the Read mode, the content of IDATA1 is shifted into Buffer Register 1 on the leading edge of RCLK0. The content of Buffer 1 is then parallel loaded into Buffer Register 2 on the trailing edge of the Read Bit Clock (RBCG0) at the time the mode controls are high (PLD01 and PLD11). During the time that PLD01 and PLD11 are low, Buffer Register 2 is in the Inhibit Clock mode which inhibits any change in the register content.

The data is fetched from Buffer Register 2 by the data request (DRG0).

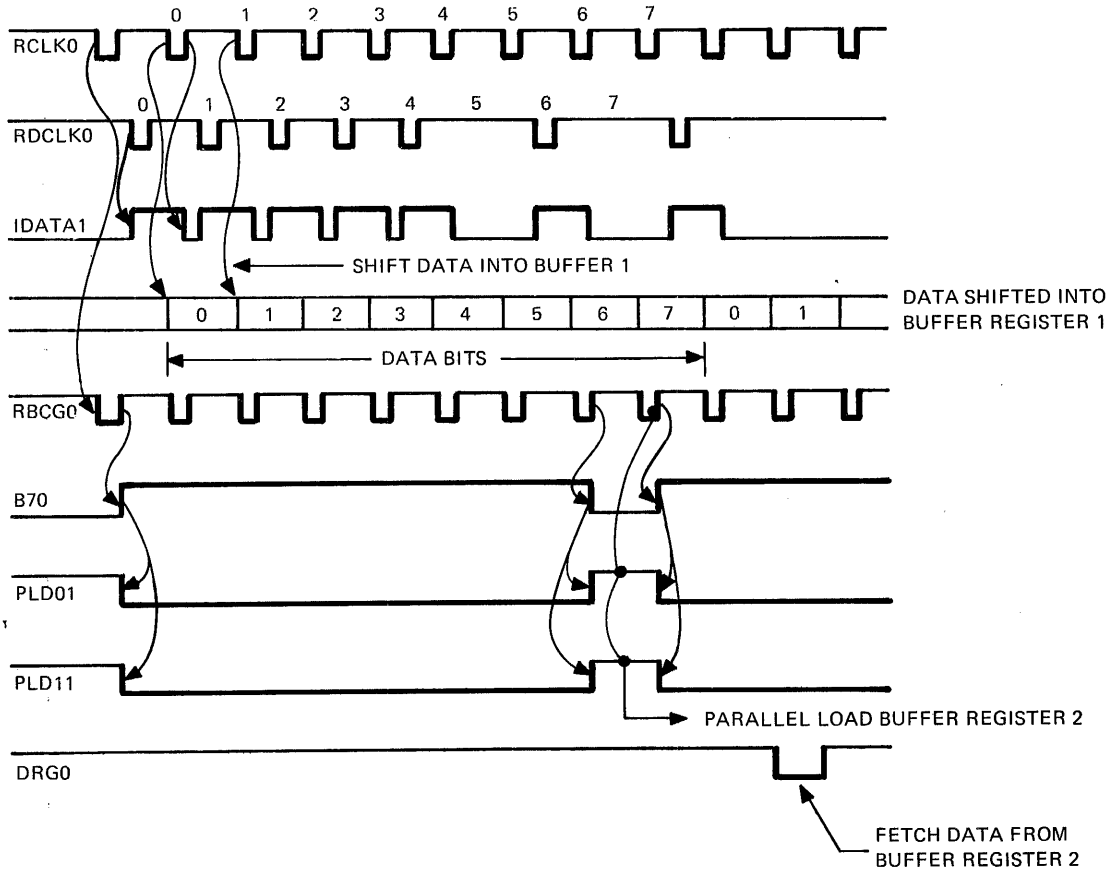
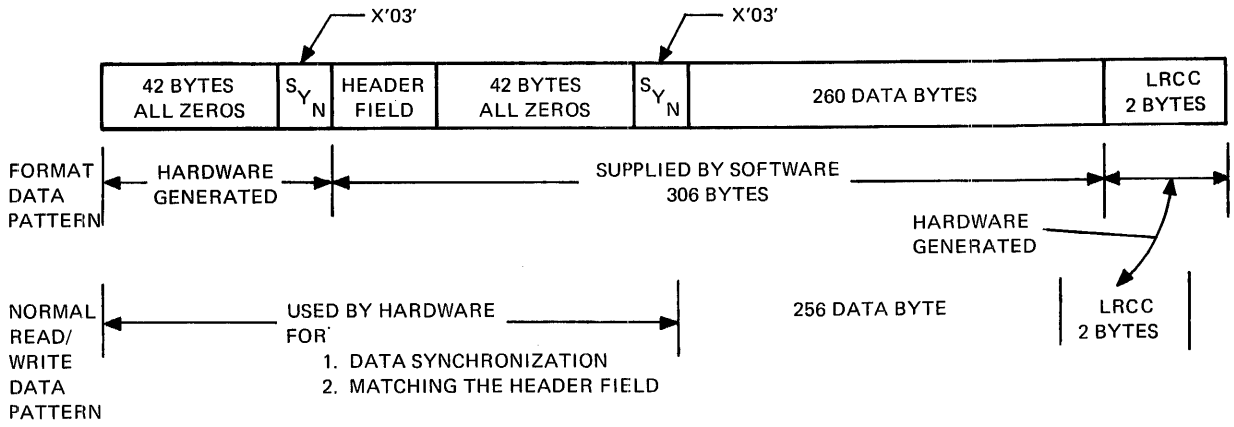


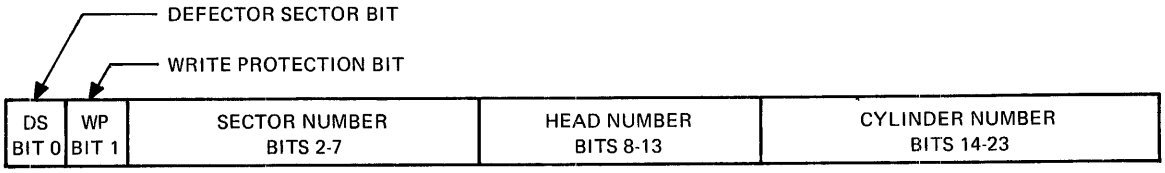
Figure 14. Buffer Register Timing Read and Read Format Mode

7.23 Data Synchronization

Data Synchronization on any operation (all operations except write format) that reads data from the selected disc file is accomplished by detecting a previous written synchronization byte (see Figure 15, Data Format). The synchronization bytes are written by the controller except when the disc pack is formatted. In which case, the second synchronization byte is supplied as part of the formatting data on a write format operation. The data for the synchronization byte is a hexadecimal (X'03') three. Both synchronization bytes are preceded by a field of all zeros (42 bytes). The detecting of the synchronization bytes is done by the Sync Byte Circuit (Sheet 13 of 02-359D08). The input data is shifted into the four bit shift register and when the data content of three low order bits is equal to a binary 3, the Synchronization Match signal (SBMT1) is generated. The synchronization byte timing is illustrated in Figure 16.



DATA FORMAT



HEADER FIELD (3 BYTES)

Figure 15. Data Format

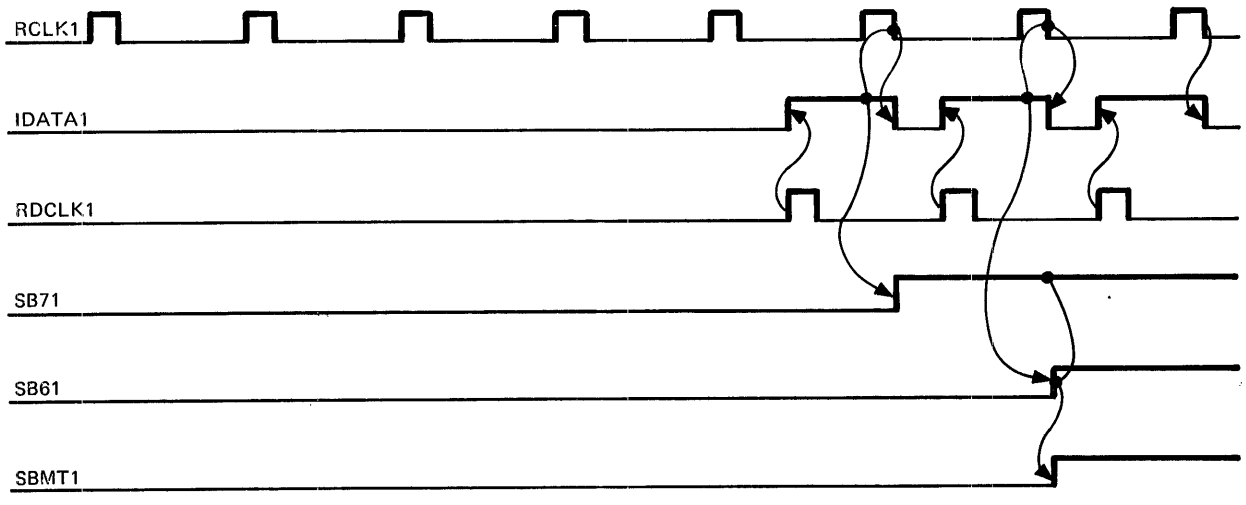


Figure 16. Synchronization Byte Timing

7.24 Read Operation

The three read operations of the disc controller are very similar in operation. The read check operation is the same as a normal read operation with the exception that no data is transferred to the Processor on the read check operation. The difference between the read format operation and the normal read operation is that on a format operation, the header field, the 42 bytes of all zeros, the sync byte and the 260 data byte are all transferred as data (see Data Format, Figure 16) to the Processor. The header field is not checked on a read format operation. The timing for a normal read operation is illustrated in Figure 17.

After the read gate (RGAT1) is activated, the operation to start the read operation occurs, when the synchronization byte is detected. Upon detection of the synchronization byte, the following signals are activated:

1. Enable Read Data (ENRD)
2. Check Header Data (CHEDF)

Head Field Check

When the Check Header Data flip-flop (CHEDF1) (Sheet 12 of 02-359D08) becomes set, it enables the necessary circuits for checking the header field on a bit-by-bit basis. During the time that the CHEDF flip-flop is set, the following operations are performed:

1. The parallel to serial converter (Sheet 8 of 02-359D08) is enabled by ESECTD0, EHEDD0, and ECLCD0.
2. The Defective Sector bit of the header is checked. If the Defective Sector bit is equal to a one, the Defective Sector flip-flop (DFSEC) (Sheet 12, 02-359D08) is set.
3. The Write Protection bit of the header is compared against the output of the Write With Protect flip-flop (WPB1), (Sheet 9 of 02-359D08). If the Write With Protection bit equals a one and the WPB flip-flop is set, the Header Write Protect flip-flop (SWP) is set.
4. Bits 2 through 23 of the header field are compared against the head data HD on a bit by bit basis. If a mismatch occurred, the Header Error flip-flop (HERRF) is set.

The comparison circuits for checking the header data are controlled by the FRCF and SRCF flip-flops (Sheet 13 of 02-359D08). The Defective Sector Comparison circuit is enabled for time T1 (See Figure 17). During the Time T2, the Write With Protection Comparison Circuit is enabled. The Comparison Circuit for checking the rest of the header is disabled during the time T1 + T2.

Read Enable (ENRD)

When the Enable Read flip-flop (ENRD) (Sheet 10 of 02-359D08) becomes set, the following occurs:

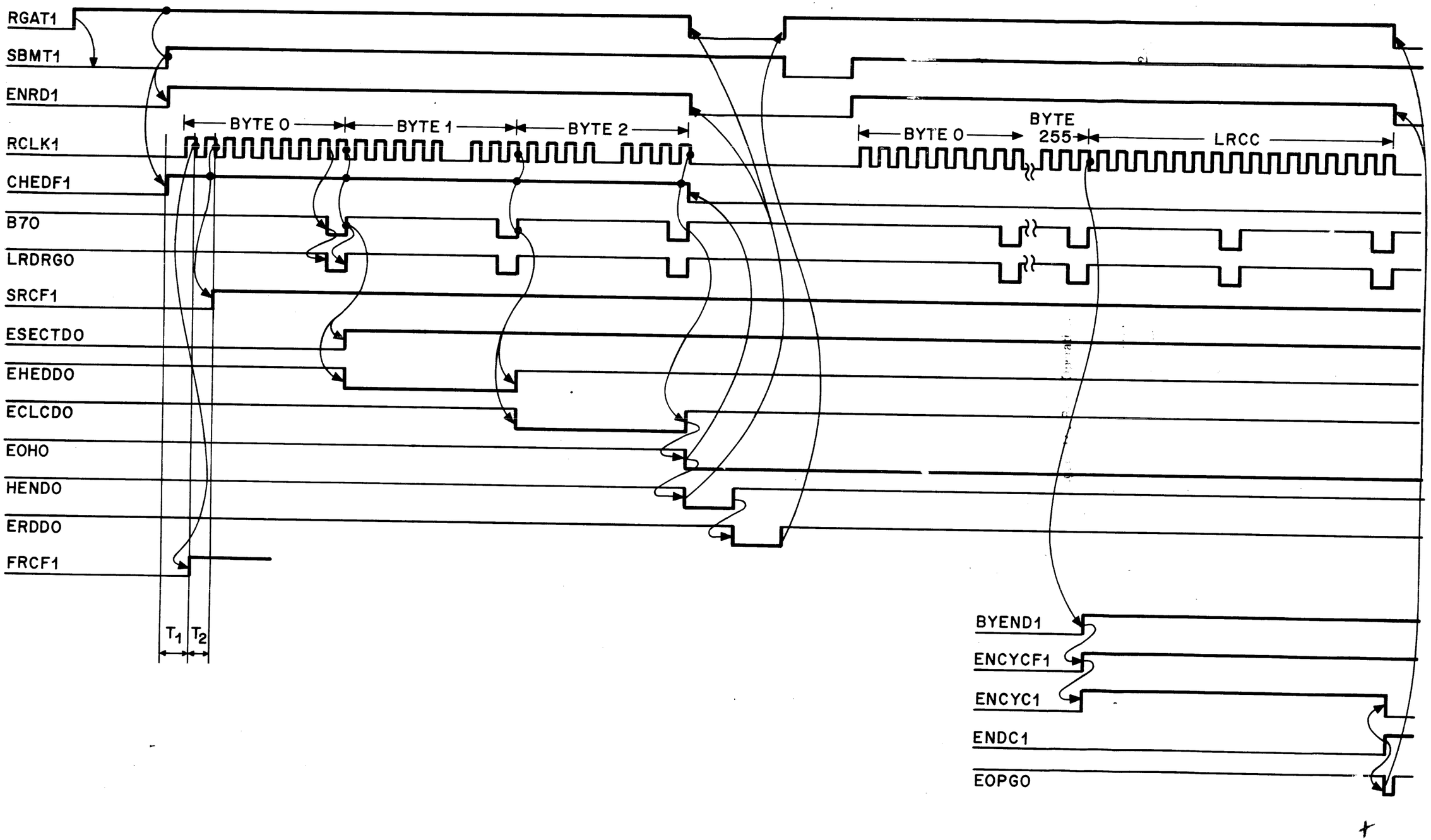
1. The Read Byte Clock (RBCG0) is enabled, which advances the byte counter.
2. The LRCC Register is enabled.

On the occurrance of the EOH0 signal, RGAT1, CHEDF1, and ENRD1 are deactivated. The Header End Delay (HEND0) is triggered from the transition of EOH0, which is used as a reset function to clear the byte counter and associated circuits.

After the header field is read, the read sequence is again initiated to read the data field. After the 256 data bytes are read, the circuit for checking the two byte LRC character is enabled by BYEND1.

7.25 Write Operation

The normal write and format write operations are very similar. On a write format operation, the operational sequence to write data to the disc file is initiated on the sector match condition (SMF1) (see Figure 18, Write and Write Format Timing). The writing of the leading 42 bytes of all zeros begins when the Enable Write Clock (ENWCLK1) (Sheet 11 of 02-359D08) is activated. During the time that ENSYN1 (Sheet 10 of 02-359D08) is high, the Synchronization byte is written. The data for the Synchronization byte is generated from B21 and B41 of the Byte Counter. On the trailing edge of the first LWDRG0 pulse after the Enable sync (ESG1) flip-flop is set, the Enable Data (ENDAT) (Sheet 10 of 02-359D08) signal is activated.


RGAT1
SBMT1
ENRD1
RCLK1
CHEDF1
B7O
LRDRGO
SRCF1
ESECTDO
EHEDDO
ECLCDO
EOHO
HENDO
ERDDO
FRCF1
BYTE 0
BYTE 1
BYTE 2
T1
T2
BYTE 0
BYTE 255
LRCC
BYEND1
ENCYCF1
ENCYC1
ENDC1
EOPGO

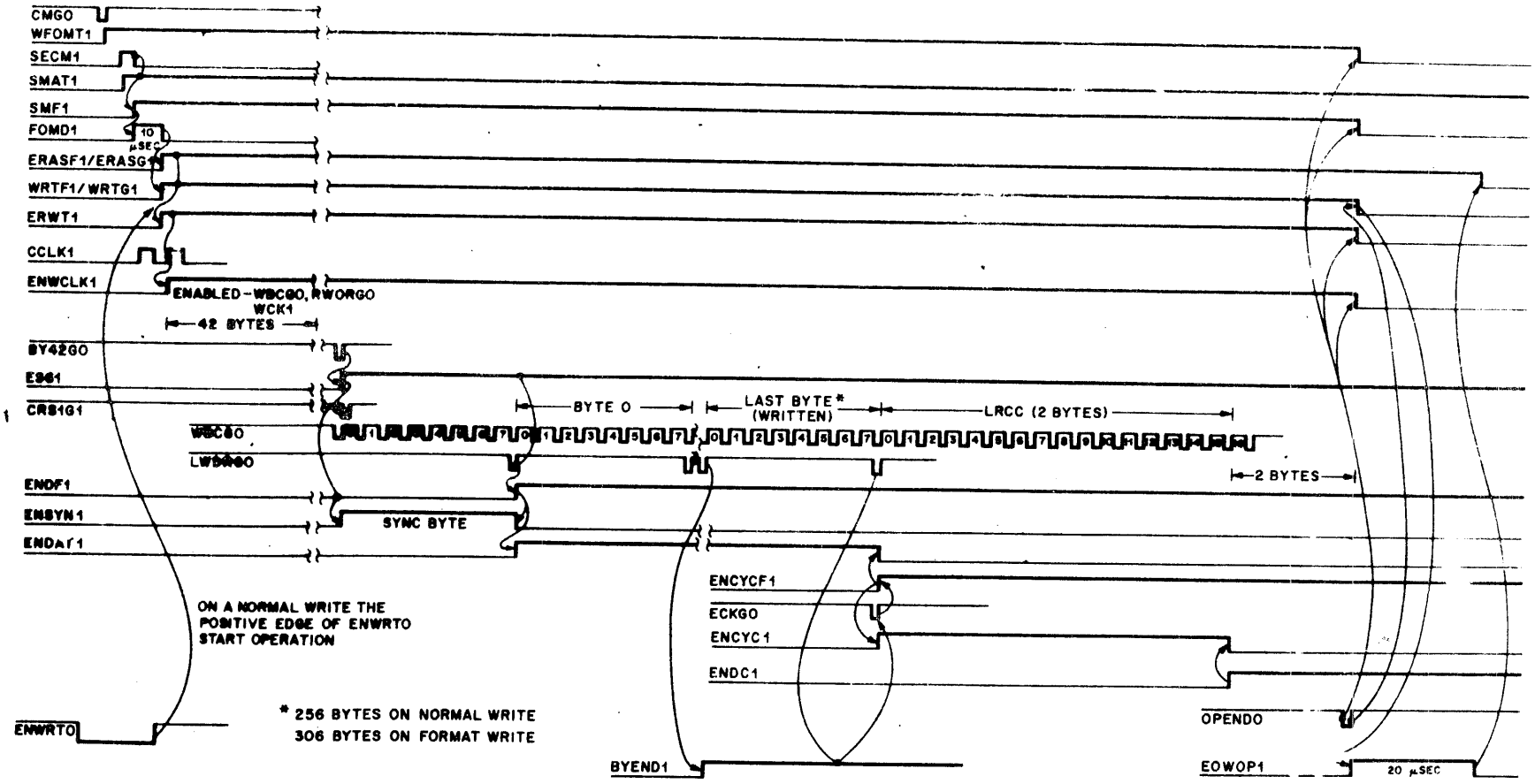


Figure 18 Write Format and Write Operation Timing

During the time that ENDAT1 is high, the data for generating the format (see Figure 15, Data Format) is transferred from the Processor to the disc file. After 306 bytes of data is transferred, BYEND1 becomes active and conditions the controller for writing the two byte LRC character. After the last data byte is written, ENCYC1 is generated. The two byte LRC character is written during the time ENCYC1 is high.

The write operation control signals (WRTG1, WFOMT1, etc.) are deactivated after two bytes of zeros are written.

The sequence for a normal write operation is the same as that of the write format operation except the sequence is initiated on the trailing edge of ENWRT0 instead of a sector match.

7.26 Write Clock Phasing (Sheet 11 of 02-359D08)

The write oscillator is a crystal controlled oscillator which generates the basic frequency for writing data to the disc file. The write oscillator (see Figure 19, Write Clock Phasing and DFR Format) frequency is divided by two to generate the WOSC1/2 signal. The phasing for generating the Double Frequency Data recording format is controlled by the Phase flip-flop (DPF).

DPF1 = High = Clock Phase
DPF1 = Low = Data Phase

The data to be written (DATG1) and Write Clock are combined to provide the Double Frequency data stream as illustrated in Figure 19.

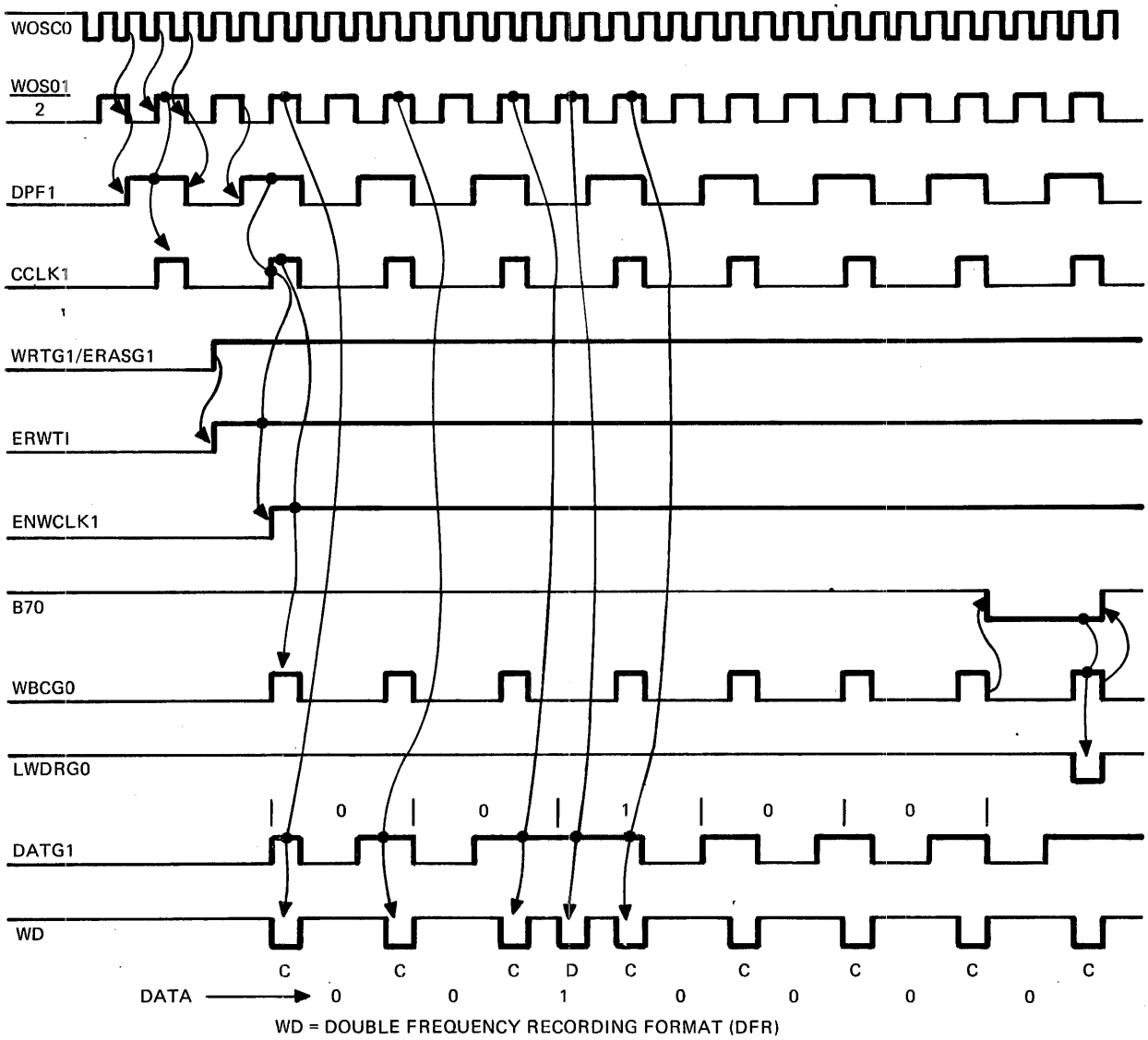


Figure 19. Write Clock Phasing: D F R Format

7.27 Data Separation

The data which is read from the disc file is in the Double Frequency Recording (DFR) data format. To utilize the data read from the disc file, the data must first be separated from the DFR pulse train. The separation is accomplished by means of a Variable Frequency Oscillator (VFO). The VFO is synchronized with the incoming DFR pulse train during the 42 bytes of zeros (see Figure 15, Data Format). The function of the VFO is to generate the correct logic signals for Data separation. The timing for the separation of the DFR pulse train is illustrated in Figure 20.

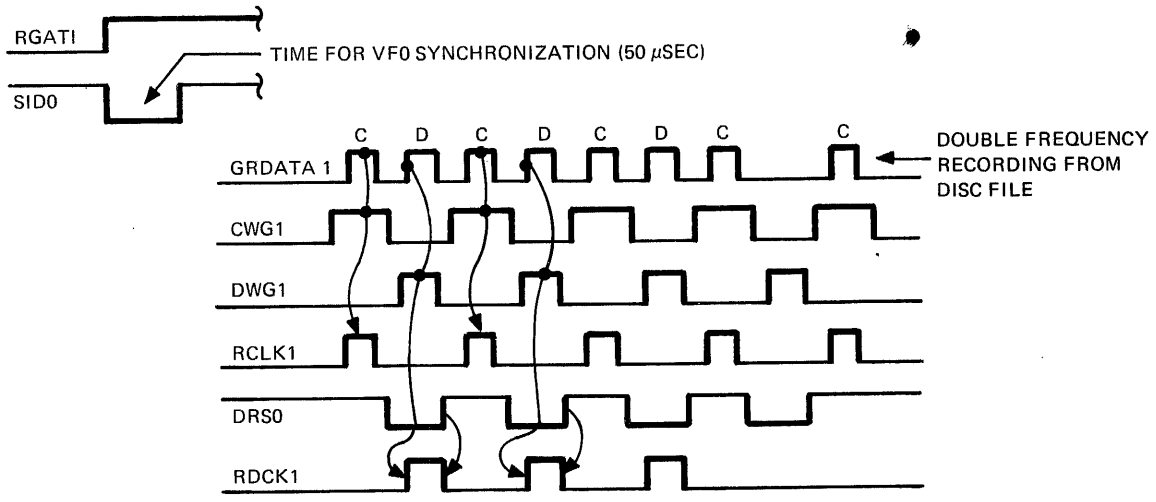


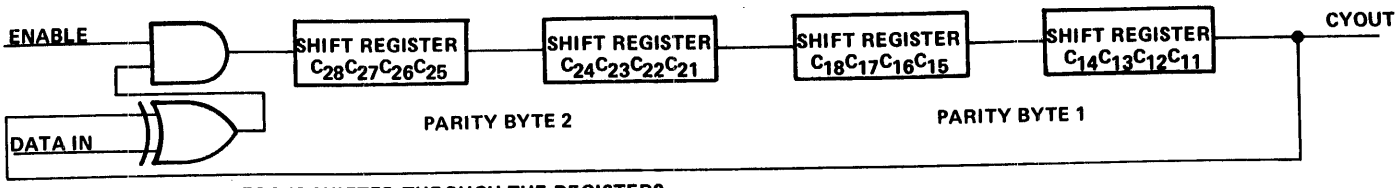
Figure 20. Data Separation Timing

7.28 Longitudinal Record Check

The Longitudinal Record Check (LRC) character is a 16 bit (2 bytes) cyclic generated character (see Figure 21 for Derivation of the LRC Character). The LRC is generated by the LRCC Register (Sheet 13 of 02-359D08).

Write Operation: The LRC to be written to the disc file is generated as the data is written. At the end of the data field, the content of LRCC Register is then written. On a Write Format operation, the LRC is generated over 306 data bytes and on the write operation it is generated over 256 data bytes.

Read Operation: On a read operation the LRC is generated as the data is being read. After the data field is read, the content of the LRCC register is compared to the LRC previously written on a bit by bit basis. If a mismatch occurs, the LRC Error flip-flop (CYCEF) is set.



INITIAL CONDITION: ZERO IS SHIFTED THROUGH THE REGISTERS.
AFTER ENABLE:

BIT COUNT 1: $C_{11} = C_{12} = C_{13} = C_{14} = C_{15} = C_{16} = C_{17} = C_{18} = C_{21} = C_{22} = C_{23} = C_{24} = C_{25} = C_{26} = C_{27} = 0$;
$C_{28} = B_{11} \oplus 0 = B_{11}$

BIT COUNT 8: $C_{11} = C_{12} = C_{13} = C_{14} = C_{15} = C_{16} = C_{17} = C_{18} = 0$.
$C_{21} = B_{11} \oplus 0 = B_{11}$
$C_{22} = B_{12} \oplus 0 = B_{12}$
$C_{23} = B_{13} \oplus 0 = B_{13}$
$C_{24} = B_{14} \oplus 0 = B_{14}$
$C_{25} = B_{15} \oplus 0 = B_{15}$
$C_{26} = B_{16} \oplus 0 = B_{16}$
$C_{27} = B_{17} \oplus 0 = B_{17}$
$C_{28} = B_{18} \oplus 0 = B_{18}$

BIT COUNT 16:
$C_{11} = B_{11}$
$C_{12} = B_{12}$
$C_{13} = B_{13}$
$C_{14} = B_{14}$
$C_{15} = B_{15}$
$C_{16} = B_{16}$
$C_{17} = B_{17}$
$C_{18} = B_{18}$
$C_{21} = B_{21}$
$C_{22} = B_{22}$
$C_{23} = B_{23}$
$C_{24} = B_{24}$
$C_{25} = B_{25}$
$C_{26} = B_{26}$
$C_{27} = B_{27}$
$C_{28} = B_{28}$

BIT COUNT 17:
$C_{28} = B_{11} \oplus B_{31}$
$C_{27} = B_{28}$
$C_{26} = B_{27}$
$C_{25} = B_{26}$
$C_{24} = B_{25}$
$C_{23} = B_{24}$
$C_{22} = B_{23}$
$C_{21} = B_{22}$
$C_{18} = B_{21}$
$C_{17} = B_{18}$
$C_{16} = B_{17}$
$C_{15} = B_{16}$
$C_{14} = B_{15}$
$C_{13} = B_{14}$
$C_{12} = B_{13}$
$C_{11} = B_{12}$

BIT COUNT 32:
$C_{28} = B_{28} \oplus B_{48}$
$C_{27} = B_{27} \oplus B_{47}$
$C_{26} = B_{26} \oplus B_{46}$
$C_{25} = B_{25} \oplus B_{45}$
$C_{24} = B_{24} \oplus B_{44}$
$C_{23} = B_{23} \oplus B_{43}$
$C_{22} = B_{22} \oplus B_{42}$
$C_{21} = B_{21} \oplus B_{41}$
$C_{18} = B_{18} \oplus B_{38}$
$C_{17} = B_{17} \oplus B_{37}$
$C_{16} = B_{16} \oplus B_{36}$
$C_{15} = B_{15} \oplus B_{35}$
$C_{14} = B_{14} \oplus B_{34}$
$C_{13} = B_{13} \oplus B_{33}$
$C_{12} = B_{12} \oplus B_{32}$
$C_{11} = B_{11} \oplus B_{31}$

BIT COUNT 33:
$C_{28} = B_{11} \oplus B_{31} \oplus B_{51}$
$C_{27} = B_{28} \oplus B_{48}$
$C_{26} = B_{27} \oplus B_{47}$
$C_{25} = B_{26} \oplus B_{46}$
$C_{24} = B_{25} \oplus B_{45}$
$C_{23} = B_{24} \oplus B_{44}$
$C_{22} = B_{23} \oplus B_{43}$
$C_{21} = B_{22} \oplus B_{42}$
$C_{18} = B_{21} \oplus B_{41}$
$C_{17} = B_{18} \oplus B_{38}$
$C_{16} = B_{17} \oplus B_{37}$
$C_{15} = B_{16} \oplus B_{36}$
$C_{14} = B_{15} \oplus B_{35}$
$C_{13} = B_{14} \oplus B_{34}$
$C_{12} = B_{13} \oplus B_{33}$
$C_{11} = B_{12} \oplus B_{32}$

FINAL:
$C_{11} = B_{11} \oplus B_{31} \oplus B_{51} \oplus B_{71} \oplus \cdots\cdots \oplus B_{2551}$
$C_{12} = B_{12} \oplus B_{32} \oplus B_{52} \oplus B_{72} \oplus \cdots\cdots \oplus B_{2552}$
$C_{13} = B_{13} \oplus B_{33} \oplus B_{53} \oplus B_{73} \oplus \cdots\cdots \oplus B_{2553}$
$C_{14} = B_{14} \oplus B_{34} \oplus B_{54} \oplus B_{74} \oplus \cdots\cdots \oplus B_{2554}$

$C_{15} = B_{15} \oplus B_{35} \oplus B_{55} \oplus B_{75} \oplus \cdots\cdots \oplus B_{2555}$
$C_{16} = B_{16} \oplus B_{36} \oplus B_{56} \oplus B_{76} \oplus \cdots\cdots \oplus B_{2556}$
$C_{17} = B_{17} \oplus B_{37} \oplus B_{57} \oplus B_{77} \oplus \cdots\cdots \oplus B_{2557}$
$C_{18} = B_{18} \oplus B_{38} \oplus B_{58} \oplus B_{78} \oplus \cdots\cdots \oplus B_{2558}$

$C_{21} = B_{21} \oplus B_{41} \oplus B_{61} \oplus B_{81} \oplus \cdots\cdots \oplus B_{2561}$
$C_{22} = B_{22} \oplus B_{42} \oplus B_{62} \oplus B_{82} \oplus \cdots\cdots \oplus B_{2562}$
$C_{23} = B_{23} \oplus B_{43} \oplus B_{63} \oplus B_{83} \oplus \cdots\cdots \oplus B_{2563}$
$C_{24} = B_{24} \oplus B_{44} \oplus B_{64} \oplus B_{84} \oplus \cdots\cdots \oplus B_{2564}$
$C_{25} = B_{25} \oplus B_{45} \oplus B_{65} \oplus B_{85} \oplus \cdots\cdots \oplus B_{2565}$
$C_{26} = B_{26} \oplus B_{46} \oplus B_{66} \oplus B_{86} \oplus \cdots\cdots \oplus B_{2566}$
$C_{27} = B_{27} \oplus B_{47} \oplus B_{67} \oplus B_{87} \oplus \cdots\cdots \oplus B_{2567}$
$C_{28} = B_{28} \oplus B_{48} \oplus B_{68} \oplus B_{88} \oplus \cdots\cdots \oplus B_{2568}$

THE FIRST LONGITUDINAL PARITY BYTE EQUALS THE EVEN LONGITUDINAL PARITY BYTE OF ODD-NUMBER DATA BYTE.
THE SECOND LONGITUDINAL PARITY BYTE EQUALS THE EVEN LONGITUDINAL PARITY BYTE OF EVEN-NUMBER DATA BYTE.

Figure 21. Derivation of Longitudinal Parity Bytes

The timing for shifting data into and from the LRC register for both a read and write operation is illustrated in Figures 22 and 23.

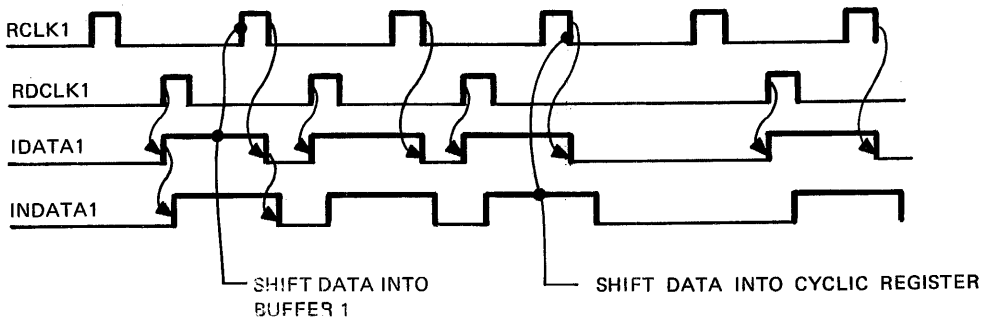


Figure 22. LRCC Register Timing Read Operation

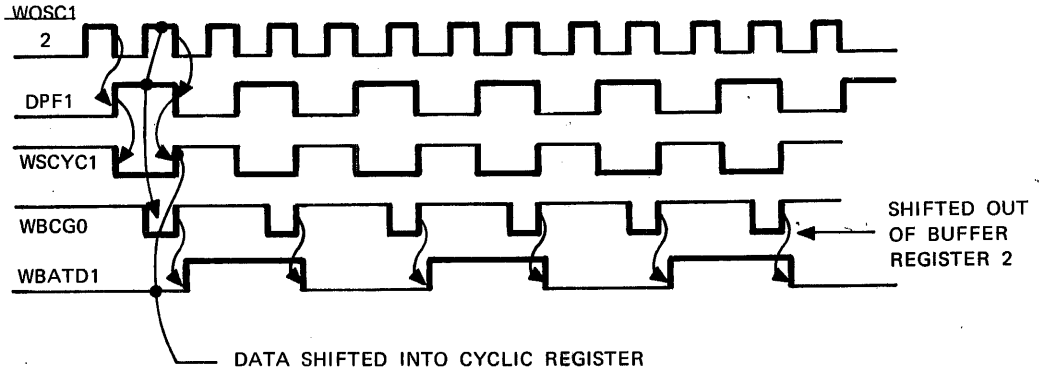


Figure 23. LRCC Register Timing Write Operation

7.29 Data Transfer

Data Transfer between the controller and the Processor via the selector channel is accomplished in the standard fashion. If the selector channel is set up for data transfer, the data byte is transferred on the negative transition of the busy status bit (BSY1). Figure 24 illustrates the timing for data transfer for both the read and the write modes of operation.

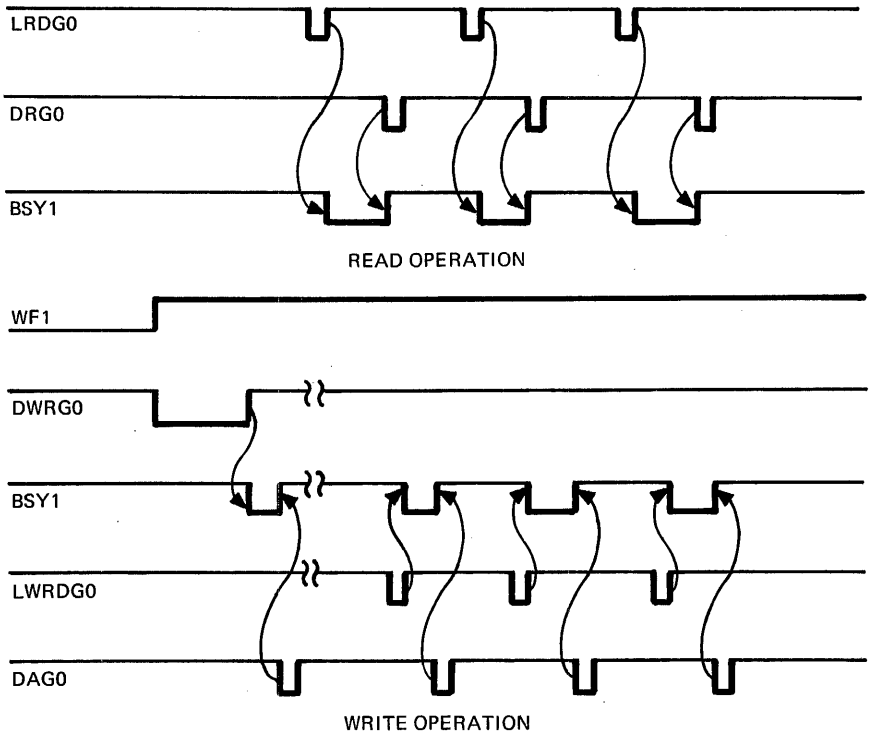


Figure 24. Data Transfer Timing

7.30 Byte Counter (Sheet 10 of 02-359D08)

The byte counter is a 12 bit binary counter with the three least significant bits functioning as a bit counter. The function of the byte counter is to count the number of data bytes read or written in a given sector. The number of bytes written or read per sector during a normal read or write operation (Read, Write, and Read Check) is 256. For a format operation, the number of data bytes per sector is 306.

The byte counter is initialized on the following:

1. System Clear (SCLR0) or an output command from the Processor.
2. After the 42 bytes of all zeros are written preceding the synchronization byte by CRS1G0.
3. On the leading edge of the Header Delay signal (HEND0).
4. When the Read or Write operation is completed by EOPG0.

On a normal read or write operation, the output of the byte counter is used to generate the BYEND1 signal after 256 bytes are written or read. On a format operation, BYEND1 is generated after 306 bytes are written or read.

7.31 Multi Sector Operation

The multi sector operation is initiated by specifying that more than the number of bytes per sector (256 bytes for normal operation and 306 bytes for a format operation) are to be transferred by the selector channel. This is accomplished under software control. Figures 25 and 26 illustrate the timing for initiating multi sector operation. Multi sector operation can be initiated in the following modes:

1. Read Format
2. Write Format
3. Normal Read
4. Normal Write

The following technique is used for determining if a multi sector data transfer is to be made. The status request (SRG0) signal is sampled for a period of 200 nanoseconds after the data request (DRG or DAG0) is made after the determined data mode signal (DD0) is activated. In the Read mode if SRG0 is present within 200 nanoseconds after the 256 or 306th byte is transferred, it means that the selector channel is set up to transfer more than the number of bytes in a given sector.

For a write operation, the selector channel presents a data request (DAG0) to the controller after the DD0 signal is active if the selector channel is set up to transfer more than the number of bytes in a given sector.

In either mode, the Continue flip-flop (CONT1) is set by GTNS0. When the Continue flip-flop is set, it conditions the controller for multi sector data transfer.

During a multi sector operation, the following operations are initiated by the controller:

1. The content of the sector register is advanced by one.
2. If the crossing of a head boundary is necessary to complete the data transfer, the content of the head register is advanced by one and the advanced head register signal (HADVG1) is generated.

The advancing of the sector register, head register, and the advance head register signal is required for a multi sector operation to allow the header data field of each sector to be compared on a bit by bit basis.

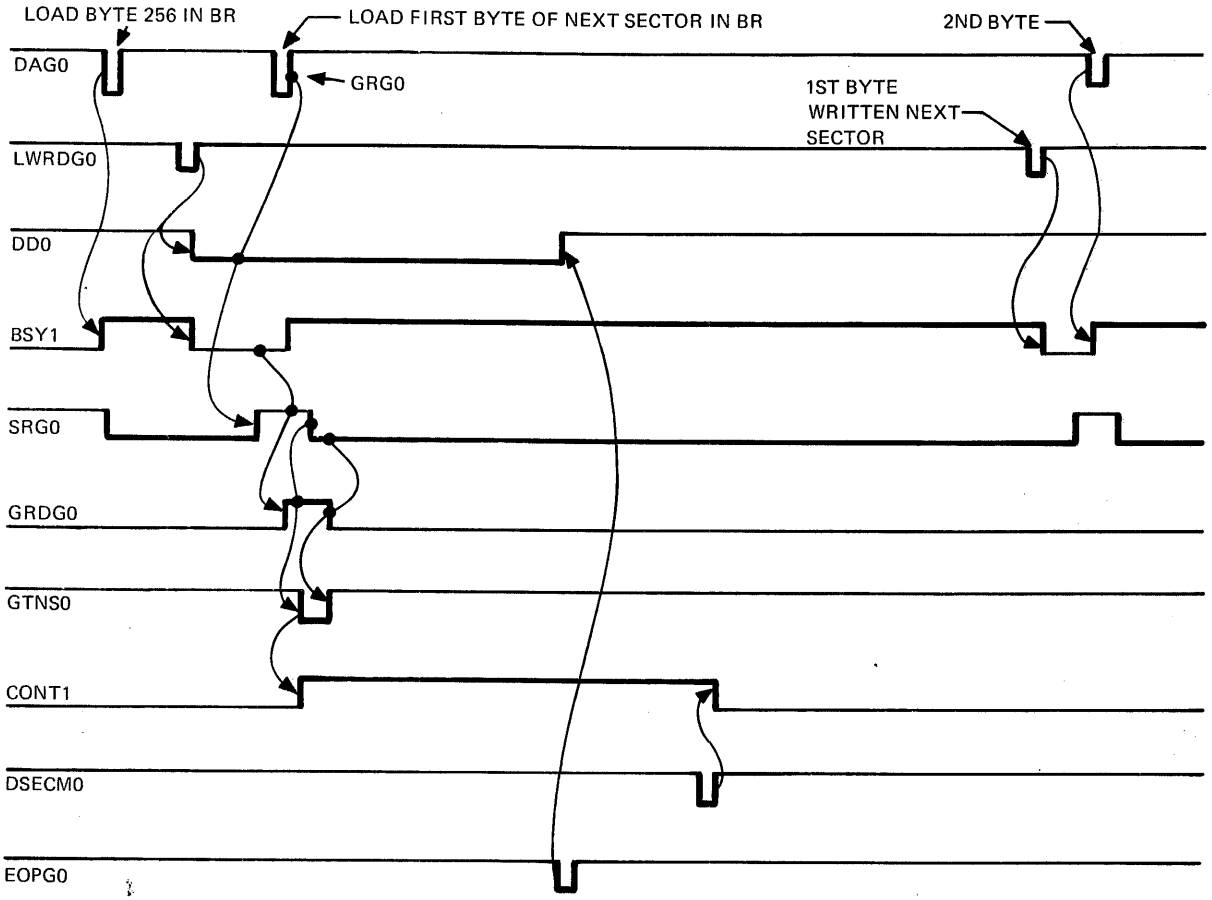


Figure 25. Multi-Sector Control Write Mode

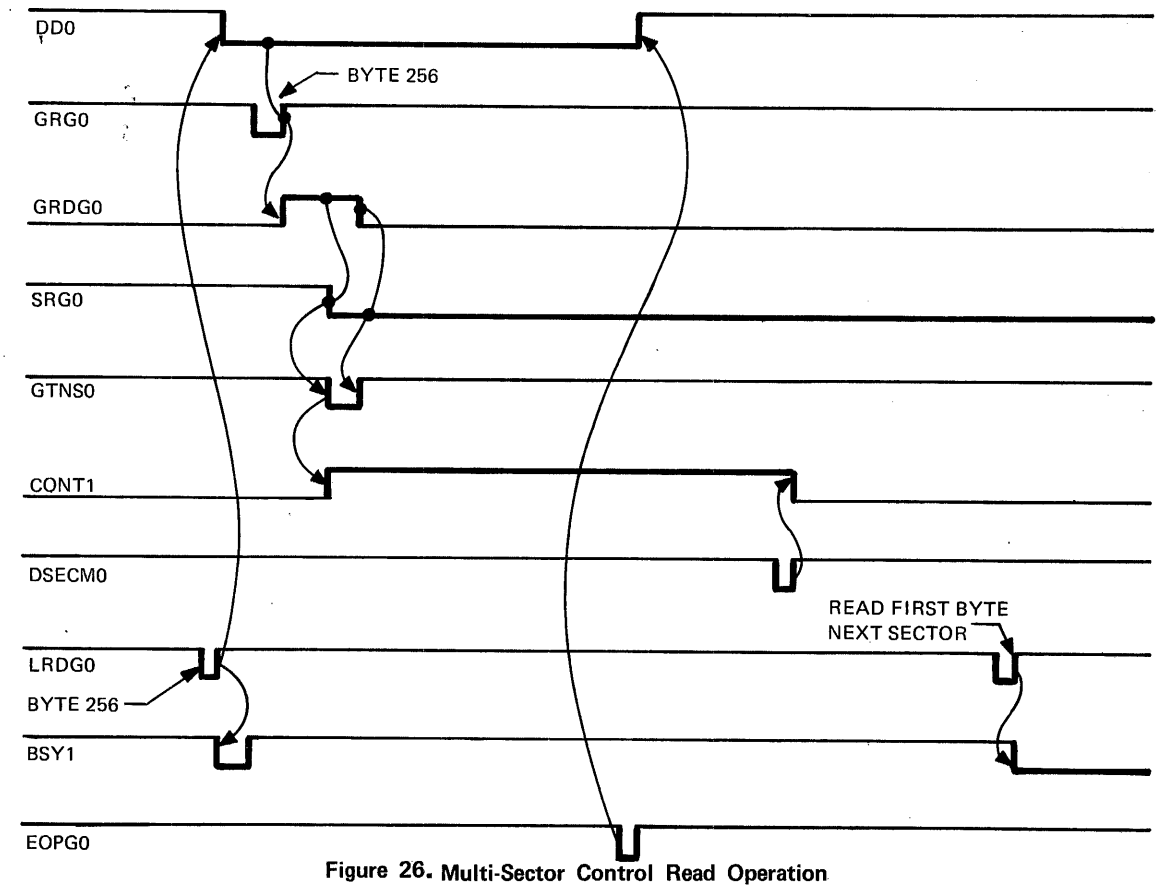


Figure 26. Multi-Sector Control Read Operation

The timing for the sector counter and head register advance is illustrated in Figures 27 and 28 for both the Read and Write modes.

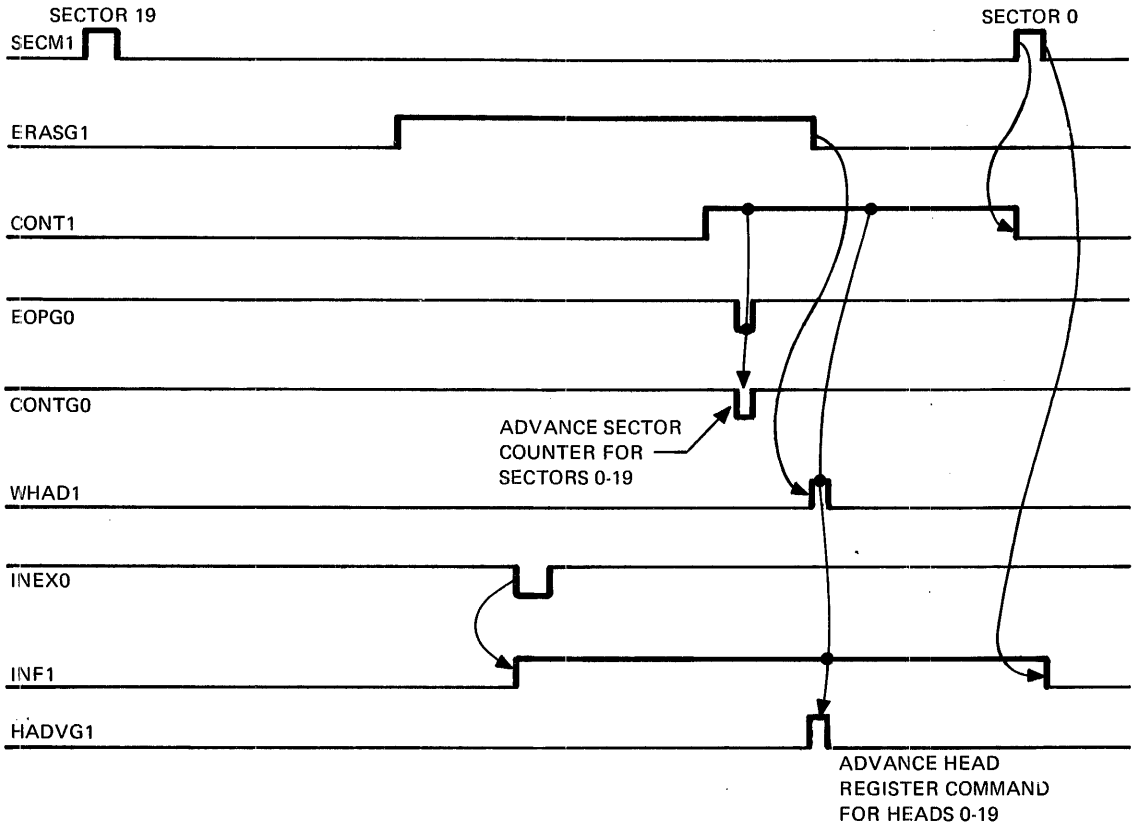


Figure 27. Sector Counter/Head Register Advance Timing Multi-Sector Write Operation

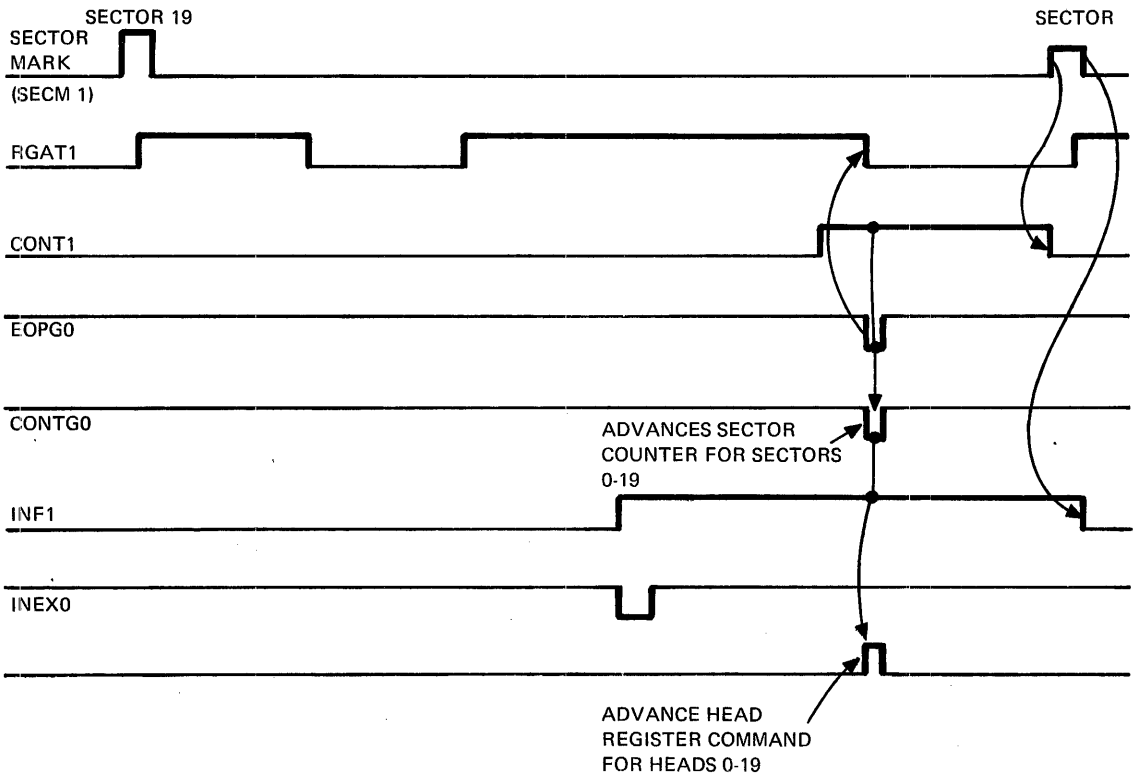


Figure 28. Sector Counter/Head Register Advance Timing Multi-Sector Read Operation

Figure 29 illustrates the command timing for a multi sector read operation. The multi sector write operation follows the same sequence except that the Write flip-flop (WF1) and the Write Gate/Erase Gate are active instead of the read signals, READ0, RFOMT0 or RCK0.

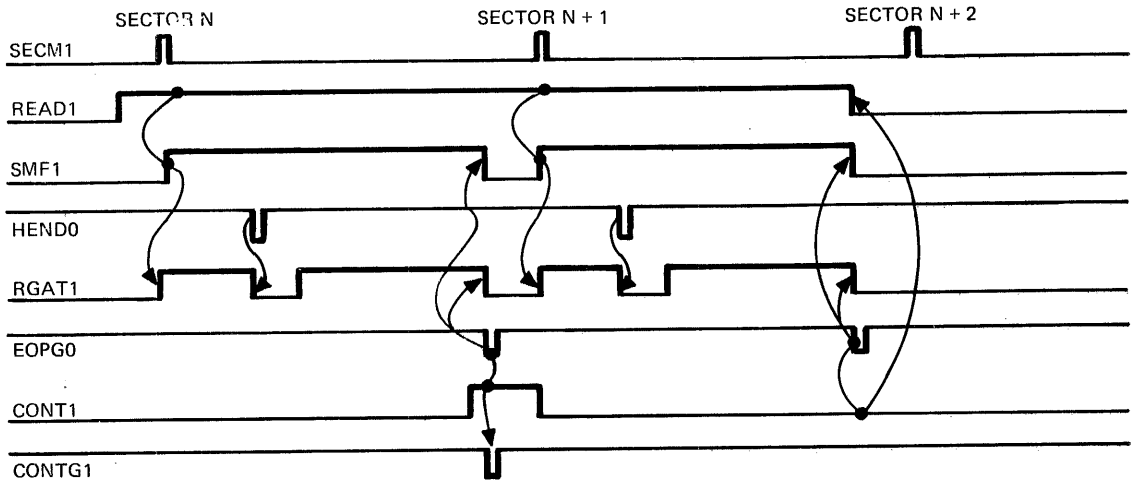


Figure 29. Multi-Sector Operation Read Mode

7.32 Variable Frequency Oscillator (Sheet 15, 02-359D08)

The Variable Frequency Oscillator (VF0) consists of the following:

1. Voltage Controlled Oscillator (VC0)
2. Phase Detector - 4 bit magnitude comparator
3. Several Binary counters

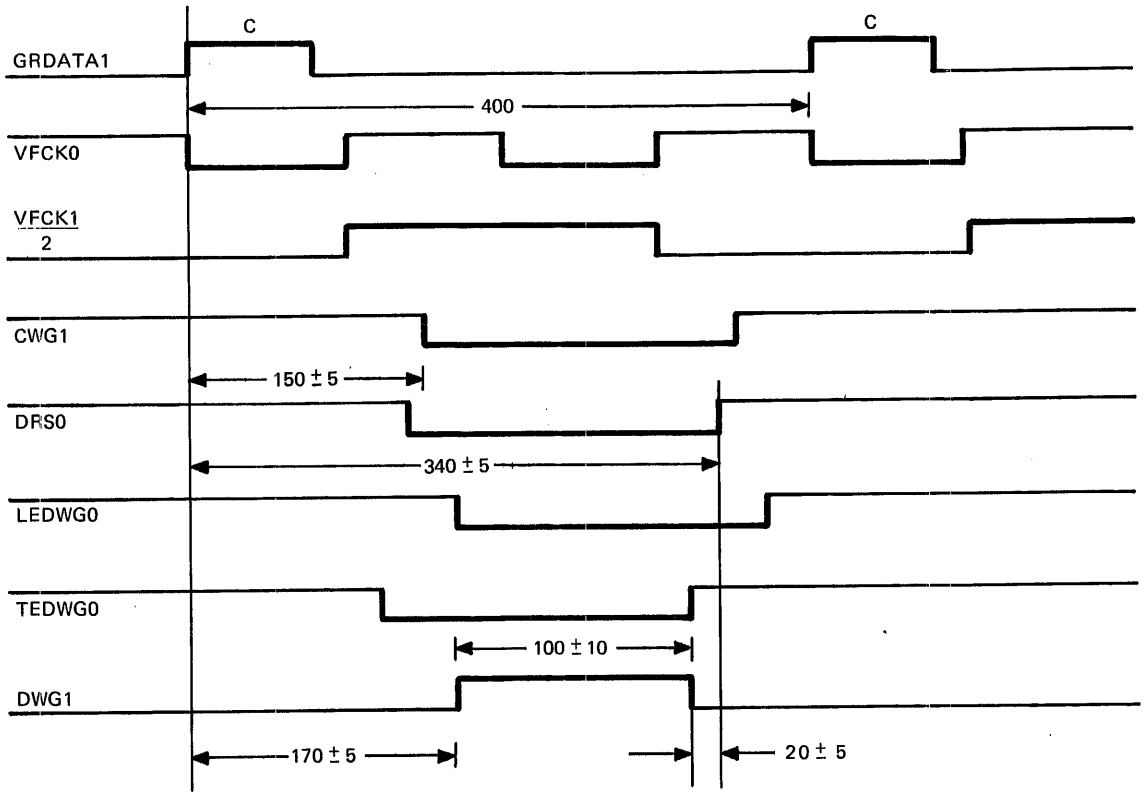
Its function is to provide means of separating the double frequency record (DFR) data being read from the disc file. (See Figure 20 and Data Separation, Section 7-23).

The frequency of the VC0 is approximately 5 megahertz. When the incoming DFR data is present, the VC0 is locked with incoming data frequency and the frequency of the VC0 is then four times the frequency of the DFR data. During the time of the 42 byte of all zeros data (see Data Format), the VC0 is synchronized.

The frequency of the VC0 is determined by the voltage level on the range input. The phase comparator (four bit magnitude comparator) measures the phase difference between DCLK0 and VFCK0/4. When the phase difference is 90°, the circuit is synchronized. (VFC0 = 4 GRDATA1). If the incoming frequency changes, the phase comparator will make a correction to the voltage that controls the VC0 by the RC network in the range input circuit.

The windows for separating the DFR is accomplished by using the tapes on the delay line to provide proper gating. Figure 30 illustrates the timing of the VF0 for the zero bit of the DFR data.

CWG1 disables the input to the DCLK0 flip-flop during the time that the data bit is present. DWG1 is a window for sampling the data bit if it is present.



ALL TIMES ARE IN NANO-SECONDS

Figure 30. V F O Timing

7.33 Bus Line Disable (Sheet 14 of 02-359D08)

The multiplexors which provide the signal to the bus lines are disabled by the relay (K1). The relay is activated when the CG0 signal is grounded. This ground is furnished by the control panel (09-067) when power is applied. When power is removed or lost from the control panel, the path to ground for CG0 is opened and the bus lines are deactivated.

7.34 Control Panel (09-067) (09-067D08)

The control panel (09-067) has the following functions:

1. Provides cable interfacing to the disc file.
2. Provides +5 volts DC for the disc file terminator.
3. Generates the controller ground control signal.

When AC power is applied to the panel, K1 is energized and the path to ground for CG0 (Sheet 14 of 02-359D08) is established. On the closure of S1, K2 becomes energized and establishes a closed path for the sequence in/out power signal from the disc file and the controller ground signal.

8. ADJUSTMENTS

The only adjustment for the Disc Controller is on the Disc Control Board (35-532). This adjustment is for the VF0 circuit.

Adjustment Procedure:

1. Load test program 06-164 and format cylinder X'CA' (refer to 06-164A15 for formatting procedures).

NOTE: A disc pack which has been formatted may be used.

2. Run Test D of test program. Set the following options:

    1. Loop = X'FFFE'
    2. SL Mode = 0 (normal R/W operation)
    3. Scope = 1 (Read only)
    4. Sector = 0000

Execute program and turn TTY off.

3. Connect a dual trace (454A) Scope as follows:

    1. Connect Channel 1 to GRDATA1 (A145-10)
    2. Connect Channel 2 to VFCK0 (A134-03)
    3. Connect EXT. trigger input (A trigger) to SID0 (A145-05)

4. Connect EXT trigger input (B trigger) to GRDATA1 (A145-10)
5. Set Sweep mode to (left) B Sweep mode triggerable after delay.
6. Using the delay sweep of the scope (horiz. display position) obtain a stable data signal on Channel 1 by expanding the time base. Select the portion of the DFR data stream where the 42 byte of all zeros occurs. Figure 30 shows the timing for the VF0. The GRDATA1 signal shown is for a zero bit of the DFR data.
7. Set mode to ALT.
8. Set potentiometer (R1) at approximately the center of the adjustment range.
9. Adjust capacitor (C3) for an oscillator frequency (VECKO) of 5 mega hertz (2 clock cycles is 400 nanoseconds).
10. Connect Channel 2 to CWG1 (A145-09). Adjust potentiometer (R1) until the leading edge of CWG1 (negative edge) is 150 ± 10 nanoseconds after the positive edge of GRDATA1 (see Figure 30).
11. Check the timing for DRS0 and DWG1. The timing relationship between GRDATA1 and DRS0 and DWG1 is shown in Figure 30. The taps on the delay line (A146) may have to be altered to obtain the time specified in Figure 30.

VFO ADJUSTMENT PROCEDURE (35-532 R06 or higher)

NOTE

A Formatted Disc Pack must be used.

1. Load Test Program 06-173F01.

2. Run Test D of Test Program. Set the following options.

    a) LOOP X'FFFE'
    b) LOCYL = X'175'
    c) SCOPE = 0
    d) DATA = X'FFFF'
    e) OTHER OPTIONS = NORMAL OPTIONS FOR 40 MEGABYTE SYSTEM.

3. Connect a dual trace (454A) scope as follows:

    a) Connect Channel 1 to CWG1 (A145-9).
    b) Connect Channel 2 to GRDATA1 (A145-10).
    c) Sync Scope positive on Channel 1.

Execute Test Program.

4. Adjust P5 to A122-16 to 5.00± .025 volts.

5. Connect CWG1 to A146-2 (Delay Line Tap) if not already connected.

6. Monitor waveforms CWG1 and GRDATE1 and adjust C3 until the time relationship between CWG1 and GRDATA1 is obtained as shown in Figure 1. ($T_1 = T_2$).

7. Change Test from Test D to Test A and margin controller. (P5 at A122-16 = 4.70 to 5.20 volts.)

8. If errors occur while making margin test, change the Delay Line Tap for CWG1 to A146-5 and repeat steps 4, 6 and 7.

NOTE

It may be necessary to connect CWG1 to other taps on the Delay Line (A146) other than taps 12 and 5. Choose the tap that provides optimum performance over the 4.70 to 5.20 volt margin range. Each time a new tap is used, steps 4, 6 and 7 must be repeated.

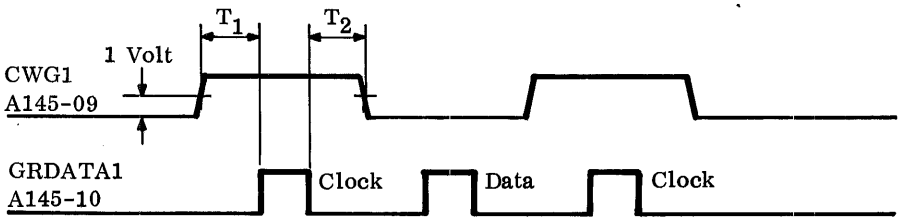


Figure 31. Timing Diagram

$T_1 = T_2$
Nominal time for T_1 and T_2 will be 125 nsec with a pulse width of 50 nsec for GRDATA. T_1 and T_2 will vary depending upon the pulse width of GRDATA1 which is a function of the drive.

9. MAINTENANCE

There is no maintenance required on the Disc Controller, however, there is preventive maintenance required on the Disc File. Refer to the Vendor Maintenance Manual, 29-400, for maintenance procedures.

10. OPTION

There is one wire wrap option on the Disc Control board. This option will allow disabling of the Write with protection of the controller. To Disable the Write with protection function, ground WPB1 (see sheet 9 of 02-359D08).

11. MUX BUS SWITCH INSTALLATION

In an installation which requires a Mux Bus Switch between the Disc Control and the Selector Channel, a capacitor must be added to the Disc Control Board (35-452). The capacitor is to be added at the C2 location (refer to sheet 14 of 02-359D08 and 35-452E03). The value of the capacitor is 47 pf.

12. MNEMONICS

The following sections provide a list of the mnemonics found in the Disc System. The meaning and the 02-359D08 schematic location are also provided.

12.1 Disc Control Mnemonics

MNEMONIC	MEANING	SCHEMATIC LOCATION
ADRS0	Address Gate	7F1
ATN0	Attention	7A1
BCG0	Byte Clock Gate	10C1
BSY1	Busy	11H7
BUSDA1	Bus Deactivate	14M7
BYC 161	Byte 16	10E3
BYC 21	Byte 2	10E2
BYC 2561	Byte 256	10E4
BYC 321	Byte 32	10E4
BYC 81	Byte 8	10E3
BYEND1	Byte End	10H5
BYH2G0	Byte 42 Gate	10F3
BY3061	Byte 306	10F5
B11	Bit Counter Bit 1	10F1
B21	Bit Counter Bit 2	10F1
B41	Bit Counter Bit 3	10F1
B70	Bit Counter Equal 7	10G2
B71	Bit Counter Equal 7	10G2
CBG0	Clear Byte Counter Gate	10G1
CCLK1	Control Clock	11E3
CCLR0	Clear A	10G9
CG0	Control Ground Signal	14J8
CHEDF0	Check Header Data Flop	12E4
CHEDF1	Check Header Data Flop	12F4
CIDEL1	Controller Idle	11N4

MNEMONICS	MEANING	SCHEMATIC LOCATION
CLRA0	Clear Read A	10F8
CMD0	Command Gate	7C1
CMG0	Gated Command Gate	7D5
COMM0	Command Signal	9K9
COMM1	Command Signal	9K9
CONTG0	Continue Gate	10N5
CONTG1	Continue Gate	10N5
CONT0	Continue Flop	11H8
CONT1	Continue Flop	11H8
CRSIG0	Byte Counter Reset 1	10M2
CWG1	Clock Window Gate	15B5
CYCD1	Cyclic Register Data	13K7
CYCEF0	Cyclic Error Flop	13C5
CYCEF1	Cyclic Error Flop	13C5
CYCE1	Cyclic Error Flag	13G2
DAG0	Gated Data Available	7D9
DAG1	Gated Data Available	7D9
DATG1	Data Gate	11G2
DAT081-DAT151	Data Bit 8-15	9K3-9K1
DA0	Data Available	7D1
DCCLR0	Disc Control Command Gate	10M9
DCLK0	Data Clock	15B4
DCNI0	Disk Control Not Idle	11N2
DD0	Determine Data Transfer	11N9
DFSEC0	Defector Sector Flop	12H3
DFSEC1	Defector Sector Flop	12H2
DPF0	Data Phase Flop	11D4
DPF1	Data Phase Flop	11D4
DRG0	Gated Data Request	7E9

MNEMONICS	MEANING	SCHEMATIC LOCATION
DR0	Data Request	7E1
DRG0	Data Reset	15D5
DSECM0	Delay Sector Mark	12J7
DSECM1	Delay Sector Mark	12J6
DTE1	Data Transfer Error	12N2
DWG1	Data Window Gate	15E7
DWRG0	Delay Write Register Gate	13N6
D080-D150	Data Line	7G1-7N1
D080A-D150A	Data Line	7G3-7N3
D081A-D151A	Data Line	7G3-7N3
ECKG0	End Counter Gate	10J5
ECLCD0	Enable Cylinder Data	12G8
EHEDD0	Enable Header Data	12G7
ENCYCF0	Enable Cyclic Flop	10D7
ENCYCF1	Enable Cyclic Flop	10D7
ENDAT0	Enable Write Data	10N4
ENDAT1	Enable Write Data	10N4
ENDC0	End of Count	10E7
ENDC1	End of Count	10E7
ENRD0	Enable Read Data	10K7
ENRD1	Enable Read Data	10K7
ENSYN1	Enable Sync. Byte	10N3
ENWCLK0	Enable Write Clock	11E3
ENWCLK1	Enable Write Clock	11E2
ENWRT0	Enable Write Signal	12L9
EOCY0	End of cylinder	12K4
EOCY1	End of cylinder	12J4
EOH0	End of Header	12G8
EOPG0	End of Operation	10K6

MNEMONICS	MEANING	SCHEMATIC LOCATION
EOPG1	End of Operation	10K6
EOS0	End of Sector	10H6
EOWOP0	End of Write Operation	11D5
ERASF0	Erase Flop	11F5
ERASF1	Erase Flop	11F4
ERASG1	Erase Gate	11H5
ERDD0	Enable Read Data Delay	12N9
ERWRT1	Enable Write	11G4
ESECTD0	Enable Sector Data	12G7
ESG1	Enable Sync. Flop	10H2
EX1	Examine	12M4
FCB1	File Control Board Busy	11K4
FCG0	File Change Gate	12A5
FEG0	Format Enable	9C7
FEG1	Format Enable	9D8
FMF1	Format Flop	9D8
FOMD0	Format Delay	9R7
FRCF1	First Read Clock Flop	12D1
FST11	File Status	12K2
FST21	File Status	12K2
GINEX0	Gate Index Gate	10N5
GRDATA1	Gated Read Data	14K2
GRDG0	Gated Request Delay Gate	14L5
GRG0	Gated Request Gate	11E9
GTNS0	Go to Next Sector	14N3
HADUG1	Head Register Advance Gate	13S3
HDE0	Head Error	12K5
HD1	Header Data	8N4
HEND0	Head End Delay	12J8

MNEMONICS	MEANING	SCHEMATIC LOCATION
HEND1	Head End Delay	12J8
HERRF0	Header Error Flop	12H3
HERRF1	Header Error Flop	12H4
IDATA1	Input Data	13C3
IEXS0	Index Sync. Flop	12F5
IEXS1	Index Sync. Flop	12F5
INDATA1	Input Data to Cyclic Register	13F2
INEX0	Index Pulse	12C5
INEX1	Index Pulse	12A5
INF1	Index Flop	12H5
LCRG0	Load Cylinder Register	11N6
LEDWG0	Leading Edge of Data Window	15C6
LHRG0	Load Head Register	11N7
LRDRG	Load Data Register	10N7
LRDG0	Load Read Data	11L9
LRG0'	Load Register	10J4
LSRG0	Load Sector Register	11N8
LWDRG0	Load Write Data Register	11G3
OPEND0	Operation End	10N5
OR0	Over Run Flop	12H4
OVF1	Overflow Flop	11F9
PLD01	Parallel Load Control	9H3
PLD11	Parallel Load Control	9G4
RACK0	Receive Acknowledge	7B1
RBCG0	Read Bit Clock	10N7
RCK0	Read Check Command Signal	9G7
RCLK0	Read Clock	13B3
RCLK1	Read Clock	15A3
RDATA1	Combine Read Data	14G2

MNEMONICS	MEANING	SCHEMATIC LOCATION
RDCLK0	Read Data Clock	15G5
RDCLK1	Read Data Clock	15G5
RD00-RD30	Read Data	14A1-14A2
RD01-RD31	Read Data	14C1-14C2
READ0	Read Command Signal	9G6
READD0	Read Data Flop	10K8
READH0	Read Header Flop	10K9
RESET0	Reset Gate	10E8
RESET0B	Reset Gate	10G8
RFOMT0	Read Format Command Signal	9G7
RF1	Read Flop	9C6
RGAT0	Read Gate	10N8
RGAT1	Read Gate	10N9
RRCR1	Read or Read Check	12K9
RWCFC1	Read/Write/Read Check/Format Command	9K8
RWCFD0	Read/Write/Read Check/Read Format Delay	9R9
SATN0	Set Attention Gate	11R5
SBMT1	Synchronization Byte Match	13H6
SB41	Sync Bit 3	13F7
SB61	Sync Bit 2	13F6
SB71	Sync Bit 1	13F6
SCLR0	System Clear	7E1
SCLR0A	System Clear	7E9
SCM11-SCM321	Sector Counter Bits	12N5-12N7
SECM1	Sector Mark	12E6
SELHDS1	Select Head	9R5
SER11-SER21	Sector Register	8J1-8J2
SID0	Sync Byte Inhibit Delay	13C9
SMAT1	Sector Match	9M5

MNEMONICS	MEANING	SCHEMATIC LOCATION
SMD00-SMD30	Select Module	14F4-14F6
SMF1	Sector Match Flop	9N6
SMOD01-SMOD31	Select Module	14C4-14C6
SRCF0	Second Read Clock Flop	12D3
SRCF1	Second Read Clock Flop	12D2
SRG0	Gated Status Request Gate	7D5
SR0	Status Request	7D1
SWP0	Write Protect Flop	12H1
SWP1	Write Protect Flop	12H1
SYNC0	Sync	7H8
TACK0	Transmit Acknowledge	7A5
TEDWG0	Trailing Edge of Data Window	15C6
VFCK0	VFO Output	15G4
VFCK0/4	VFO Output $\div$ 4	15D3
VFCK0/2	VFO Output $\div$ 2	15E4
VFCK1/2	VFO Output $\div$ 2	15E3
WDATD1	Write Data	11D2
WBCG0	Write Bit Clock	11G3
WCLK1	Write Clock	11G2
WD00-WD30	Write Data	11J2-11J4
WF0	Write Flop	9C7
WF1	Write Flop	9C7
WFOMT0	Write Format Command Signal	9H8
WFOMT1	Write Format Command Signal	9H8
WHAD1	Write Head Advance Gate	13M4
WOSC0	Write Oscillator	11A5
WOSC0/2	Write Oscillator $\div$ 2	11A3
WPB1	Write With Protect Flop	9D9
WPV0	Write Protect Violation	9E5

MNEMONICS	MEANING	SCHEMATIC LOCATION
WRTF0	Write Flop	11G7
WRTF1	Write Flop	11D7
WRTG1	Write Gate	11H6
WRT0	Write Command Signal	9H6
WRT1	Write Command Signal	9H6
WSCYC1	Shift Cyclic on Write	11F1

12.2 File Control Mnemonics

MNEMONICS	MEANING	SCHEMATIC LOCATION
AD	Address Flop	3G9
ADRS0	Address Request	3F2
ADSYD0	Address Sync Delay	3J7
ATN0	Attention	3A1
ATN1	Attention	4N7
BUSDA1	Bus Deactivate	6R7
CCLR0B	Command Clear	4C7
CMD0	Command	3D2
CMG0	Gated Command Gate	3D5
CMG1	Gated Command Gate	3D9
CSYD	Command Sync Delay	3J9
CTDG1	Tag Gate Delay	6N4
CT0	Control Tag	6M9
CT1	Control Tag	6L6
DAG0	Gated Data Request	3E9
DARM	Interrupt Queued	4E2, 4E4, 4E5, 4E6
DA0	Data Available	3D2
DB00-DB80	Drive Bus Line	6D9-6L9
DCCLR0	Disc Control Command Gate	5R6
DCNI0	Disc Control Not Idle	6H2
DRDY0	Drive Ready	5A9
DRDY1	Drive Ready	5C9
DRDY0A	Drive Ready	5D9
DU	Device Unavailable	4A1
D080-D150	Data Line	3G1-3N2
D080A-D150A	Data Line	3G3-3N3
D081-D151	Data Line	3G3-3N3
ENBL	Reset Head Register Flop	4E3, 4E4, 4E5, 4E7

MNEMONICS	MEANING	SCHEMATIC LOCATION
EOCY0	End of Cylinder	5L9
EOCY1	End of Cylinder	5N9
ERASG1	Erase Gate	6J6
ETGD0	End Tag Gate Delay	6L5
EX1	Examine	5F6
FADG0	File Address Gate	3M7
FCB1	File Control Busy	6N1
FCG0	File Change Gate	5N4
FCNI0	File Control Not Idle	6K2
FSEL00-FSEL30	File Select	5K1-5K2
FSEL01-FSEL31	File Select	5H3
FST11	File Status	5F8
FST21	File Status	5F6
GADRS0	Gated Address Gate	3H6
GATN00-GATN30	Gated Attention	5A1-5A4
GATN01-GATN31	Gated Attention	5C1-5C4
GATNS1	Gated Attention Status	5F4
GCLG1	Gated Command Line	3D9
HADVF0	Head Reg. Advance Flop	6D2
HADVG1	Head Reg. Advance Gate	6A?
HC11	Head/Cylinder Register	6L6
HC21	Head/Cylinder Register	6K6
HC41	Head/Cylinder Register	6J6
HC81	Head/Cylinder Register	6J6
HC161	Head/Cylinder Register	6J6
HC321	Head/Cylinder Register	6H6
HC641	Head/Cylinder Register	6G6
HC1281	Head/Cylinder Register	6F6
HC2561	Head/Cylinder Register	6B9

MNEMONICS	MEANING	SCHEMATIC LOCATION
HC5121	Head/Cylinder Register	6C9
IAD11	Interrupt Address Return	4R3
IAD21	Interrupt Address Return	4R5
IAKF	Reset Head Register Flop	4M2, 4M3, 4N5, 4N6
INEX0	Index Mark	5L8
INEX1	Index Mark	5N8
IQF01:31	Interrupt Queued	4J2, 4J3, 4J5, 4J6
LFB0	Load First Byte	4K9
LSB0	Load Second Byte	4K8
MODS1	Module Selected Status	5M7
MSEL00-MSEL30	Module Selected	5H6-5H8
MSEL01-MSEL31	Module Selected	5J7-5J8
ONL0	On-Line	5A8
ONL1	On-Line	5A9
RACK0	Receive Acknowledge	3B1
RACK0B	Receive Acknowledge	3B9
RACK1B	Receive Acknowledge	3B9
RESET0B	Reset Gate	4A2
RESF0	Restore Flop	6K3
RESF1	Restore Flop	6K6
RGAF0	Reset Gated Attention Flop	6H3
RGAT0	Read Gate	6F1
RGAT1	Read Gate	6H1
ROLY0	Read Only	5A6
ROLY1	Read Only	5C7
ROLYF0	Read Only Flop	5R7
RSHF0	Reset Head Register Flop	6J3
RSHF1	Reset Head Register Flop	6J6
SCF0	Set Cylinder Flop	6F3

MNEMONICS	MEANING	SCHEMATIC LOCATION
SCF1	Set Cylinder Flop	6F3
SCH1	Select Head/Cylinder	6F2
SCLR0	System Clear	3E2
SCLR0A	System Clear	3E8
SCLR1	System Clear	3E8
SCT0	Set Cylinder Tag	6R9
SCT1	Set Cylinder Tag	6G2
SECM0	Sector Mark	5G9
SECM1	Sector Mark	5H9
SEKF0	Seek Flop	6H3
SEKF1	Seek Flop	6H6
SELH01	Select Head	6J6
SHF0	Set Head Flop	6E2
SHF1	Set Head Flop	6D2
SHT0	Set Head Tag	6N9
SHT1	Set Head Tag	6G2
SIC0	Seek Incomplete	5A7
SIC1	Seek Incomplete	5C8
SMOD01-SMOD31	Select Module	5M1-5M2
SRG0	Gated Status Request	3E5
SR0	Status Request	3E2
STGDG1	Start Tag Gate Delay	6M3
SYNC0	Sync	3M8
TACK0	Transmit Acknowledge	3A5
USAF0	Unsafe	5A5
WCUR	Write Current Check	5A5
WCURF1	Write Current Check Flop	5S5
WCUR0A	Write Current Check	5E5
WRTG1	Write Gate	6G6

AMPEX

M46-429
40 MEGA-BYTE DISC SYSTEM PROGRAMMING SPECIFICATION

02-357A22
June 1974

1. INTRODUCTION

The INTERDATA Removable Pack Disc System (Product Numbers M46-429, M46-430, M46-431, M46-432 and M46-433) provides a random access, removable media, rotating memory, storage facility for the INTERDATA family of computers. The system contains a dual 15 inch Controller which can handle up to four disc drives.

Data is recorded in a fixed-sector format, where each sector contains 256 data bytes. Data transfers are under control of a Selector Channel and can be from 1 to 102,400 bytes since the Controller permits data transfers across sector and head boundaries. Simultaneous seek and overlapping seek/data transfers are permitted in multiple disc systems.

Table 1 indicates the specifications pertinent to programming the system. Appendix 1 provides Sample Program Sequences.

TABLE 1. DISC SYSTEM SPECIFICATIONS

Data Storage Characteristics: Uses IBM 2316-type Packs, with double frequency recording at 2200 bits per inch and 200 tracks per inch.	
Transfer Rate:	312K Byte/Sec. Nominal 325K Byte/Sec. Max.
Start-Up Time:	45 sec.
Access Time:	
Average Latency:	12.5 ms.
Maximum Latency:	25 ms.
Average Head Positioning:	32 ms.
Maximum Head Positioning:	58 ms.
Maximum Between Adjacent Cylinders	8 ms.
Capacity:	
Sector	256 bytes
Track	5,120 bytes
Cylinder	102,400 bytes
Format:	
Sectors per Track	20
Tracks per Cylinder	20
Cylinders per Pack	406 (400 (6 Spares))
Tracks per Pack	8120
Parity:	Halfword even longitudinal
Write Protect:	Protect entire Pack
Sector Write Protect (optional)	Write protection on desired sectors (software controlled)

2. CONFIGURATION

The Removable Pack Disc System must operate through a Selector Channel. The Selector Channel must be assigned a high priority on the memory bus to insure that the 312K byte transfer rate can be maintained.

3. OPERATING PROCEDURES

The disc provides the following switches and indicators.

START/STOP	This two position switch is located at the left of the top panel. In the STOP position, the drive is not operating, the door may be opened, and Packs may be loaded or unloaded. When the switch is in the START position, the drive begins its start-up cycle which lasts for approximately 45 seconds. Checks are made to insure that the door is closed, a Pack is in place, and that the correct spindle speed has been reached. After 45 seconds have elapsed, and the checks are completed successfully, the drive is ready for operation.
DISABLE	This switch/indicator, when ON indicates that the drive is off line and cannot be selected. When Off, the drive can be selected. The transition from on to off line is achieved by depressing the switch/indicator when the file is not selected.
WRITE PROTECT	This switch/indicator, when ON, indicates that the drive is Write Protected and write operations cannot be performed on the Pack. When OFF, normal Read-Write operations can be performed. The transition from Protected to Not Protected is achieved by depressing the switch/indicator when the file is not selected.
READY	This indicator is ON when the drive is ready to receive commands. This indicator lamp goes ON at the same time the File Ready Line goes "true".
WRITE PROTECT	This indicator is ON when the drive is Write Protected. This indicator is ON in conjunction with the Write Protect switch/indicator.
SELECTED (ADDRESS)	This indicator is ON when a command has been directed to the drive. It remains ON until a command of "Reset" is directed to the selected drive, or another drive is given a command.
SELECT LOCK	This indicator lamp is ON when a condition occurs that prohibits the drive from executing a command.

4. DATA FORMAT

4.1 Disc Format - Normal

The disc is segmented into 20 sectors per track. Each sector contains a three byte header field, a 256 byte data field, and a two byte longitudinal parity field. Figure 1 illustrates the Data Format.
The number of bytes in a data transfer is not limited to sector or track boundaries. Therefore, as few as one byte and as many as 102,400 bytes may be transferred at one time. (See Figure 2 - Disc Format.) However, the controller continues the write or read operation until a complete sector is encountered, even if a complete sector is not specified. In a write operation, the sector is "filled" with the last byte specified.

In the read mode, the number of bytes that were specified are read into the Selector Channel (SELCH) and the SELCH interrupts when this is complete, but the controller continues reading until the sector boundary is reached. At this time, the user may interrogate the controller status to verify that the data transfer was error free.

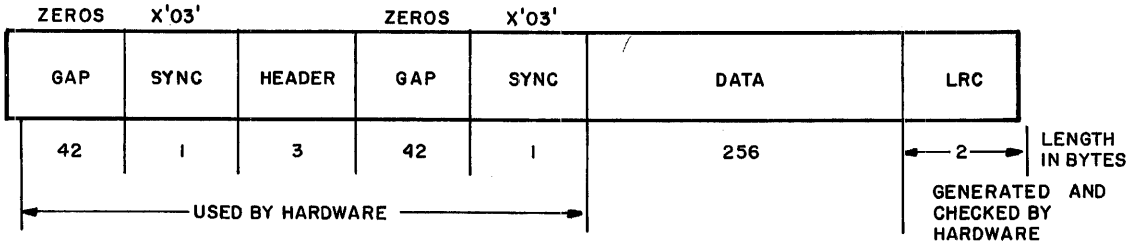
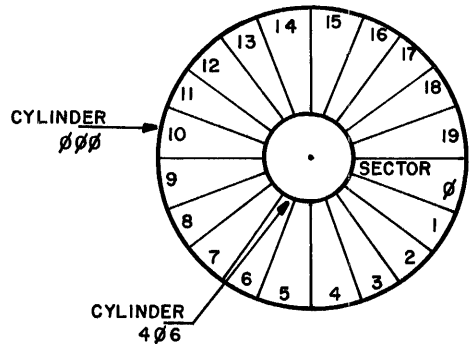


Figure 1. Data Format



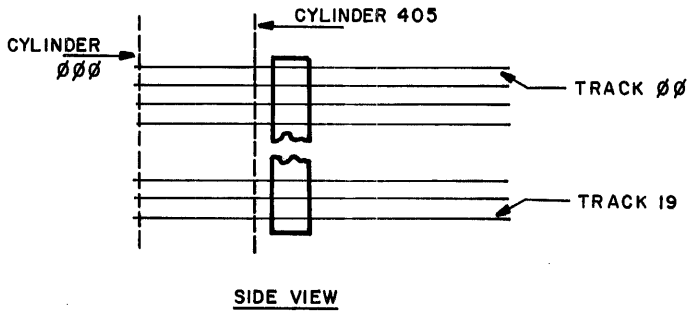


Figure 2. Disc Format

The header field illustrated in Figure 1 is not normally written or read. It is used when formatting the disc. A disc format program is run on each pack to insure the integrity of the pack. This is normally performed by commanding the controller into the write format mode then writing a worse case pattern (or patterns) into the complete sector including header and data fields. The program then commands the controller into the read format mode and reads the sector. If the data compares, the user may then write the correct address into the header field with the DEF SECTOR bit = 0 and continue to the next sector.

If the data does not compare, the user may choose to do a more complete surface analysis and, based on the results, program the DEF SECTOR bit to a 1 or 0. The user can access the header field by programming the FORMAT mode and operating the FORMAT switch in the controller. The hardware uses the header field for three purposes:

To inhibit data transfers on sectors which are flagged as defective.
To inhibit writing on sectors which are write protected.
To prevent the transfer of data when the heads are not properly positioned.

4.2 Disc Format - Test

Each pack supplied by INTERDATA is tested to insure the integrity of the disc surface. The Disc Test/Format Program performs this qualification.

In the format mode, the controller writes and reads 306 bytes of data as illustrated in Figures 3 and 4. Note that the data field in this case is 260 bytes. This permits testing the field which contains the longitudinal parity bytes in the normal data mode. For this reason, the sequence Normal Write/Format Read or Format Write/Normal Read generally produces longitudinal parity errors.

The format program writes a prescribed pattern, reads it back a specified number of times, and verifies that the data is correct and that there are no longitudinal parity errors. If there are no errors on any of the read operations, the program writes the header with the correct address with the DEF SECTOR bit = 0. If a data or longitudinal parity error is detected on any of the read operations, the program sets DEF SECTOR = 1.

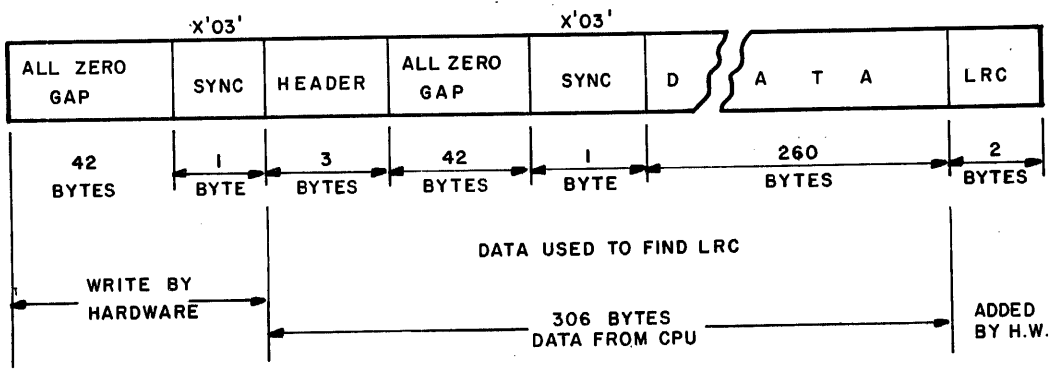


Figure 3. Sector Format

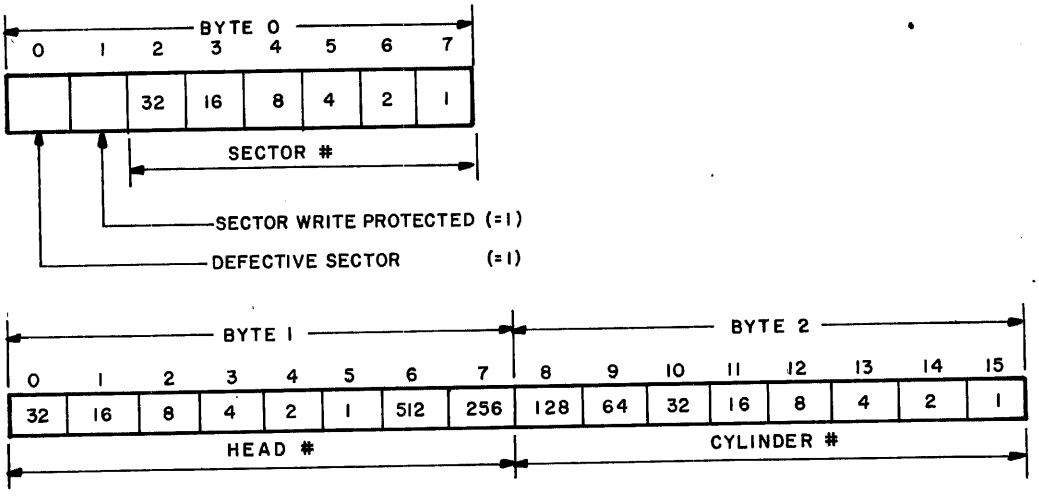


Figure 4. Header Format

5. PROGRAMMING INSTRUCTIONS

5.1 Processor Instructions

Data transfers to and from the Disc are accomplished via the SELCH; but the processor I/O instructions are used to communicate with the Disc, Controller, and SELCH. The following is a brief description of each of these instructions.

Sense Status (SS Or SSR) - Used to interrogate the disc and controller to insure that data transfers are complete and correct. It may also be used to determine if the SELCH is busy.

Output Command (OC or OCR) - Used to control disc operations and to set up the desired mode of operation and to initialize and start the SELCH.

Write Data (WD or WDR) - Loads the cylinder address, sector number, and head number in the controller, and loads the SELCH

Write Data Halfword (WH or WHR) - Loads the cylinder address.

Read Data (RD or RDR) - Used to interrogate the address register in the SELCH to determine if a data transfer terminated correctly.

Acknowledge Interrupt (AI or AIR) - Used to service the controller, SELCH and disc drive interrupts.

The controller and each disc have a separate address. This is a strap option which can be altered with a minor wiring modification. The controller is always the lowest address. The disc addresses follow in sequence by adding one to the most significant hexadecimal digit. The standard addresses are:

X'FB'	Controller
X'FC'	Disc 0
X'FD'	Disc 1
X'FE'	Disc 2
X'FF'	Disc 3

6. CONTROLLER COMMANDS

Table 2 indicates the Disc System Controller commands.

TABLE 2. CONTROLLER COMMANDS

	0	1	2	3	4	5	6	7
	DIS	EN		PROTECT	RESET	FORMAT	WRITE	READ
READ	X	X		0	0	0	0	1
WRITE NO PROTECTION	X	X		0	0	0	1	0
WRITE PROTECTION	X	X		1	0	0	1	0
READ CHECK	X	X		0	0	0	1	1
READ FORMAT	X	X		0	0	1	0	1
WRITE FORMAT	X	X		0	0	1	1	0
RESET	0	0		0	1	0	0	0

Interrupt Control

DIS/EN

Bit #

1 1 - DISARM	Interrupts are not queued
1 0 - DISABLE	Interrupts are queued, but not passed to the Processor.
0 1 - ENABLE	Interrupts are passed to the Processor as they occur.
0 0 - NO CHANGE	

READ

Enables the controller to perform a normal data read. The SELCH must be set up prior to the command, the heads must be positioned, and the sector header loaded into the controller. The data transfer from the controller is delayed at least 10 microseconds after a sector match. The SELCH must be started before this time. If the last sector read is not a complete sector, the SELCH terminates after the last byte is read into memory but the controller continues reading until the longitudinal parity error is verified, then sets CONT IDLE.

WRITE WITH NO PROTECTION

Enables the controller to perform a normal data write. The SELCH must be set up prior to the command, the heads must be positioned, and the sector header must be loaded into the controller. Data transfer to the controller is delayed at least 10 microseconds after a sector match. The SELCH must be started before this time. If the last sector written is not a complete sector, the SELCH terminates after the last data byte is written, but the controller continues and fills the remainder of the sector with the last data byte, writes the longitudinal parity characters, and then sets CONT IDLE. This write always takes place regardless of the state of the write protection flag in the sector header.

WRITE WITH PROTECTION

This write takes place only when the write protection flag in the sector header is reset. For a multi-sector write, the write protection flag is checked before writing any sector.

NOTE

The write protection feature is a hardware option.

READ CHECK

Causes the controller to perform an off-line read of a single sector. The SELCH is not used, but the heads must be positioned and the sector header must be loaded before this command is issued. While in the READ CHECK mode, no data is passed to the SELCH, but the interface cannot be used until this mode is terminated (CONT IDLE = 1). The controller status bits have their usual meaning.

WRITE FORMAT

This command, together with the FORMAT switch in the controller ON, permits writing into the header field of the sector. This is normally used only when performing a surface analysis of a new pack. The write format operation transfers are the sync. field, header, gap, data, and longitudinal parity characters as shown in Figure 1.

READ FORMAT — This command, together with the FORMAT switch in the controller ON, permits reading the information written with the write format.

RESET — This command has the same functions as system clear. Note that this command should not be used in normal programming sequences.

1. disarms controller and drive interrupt
2. deselects any drive which may be selected

6.1 Controller Status

Table 3 indicates the Disc System Controller status.

TABLE 3. CONTROLLER STATUS

0	1	2	3	4	5	6	7	
Write P Protect	Header Failure	Defect Sector	Cyl Overflow	Busy	EX	Controller Idle	Data Error	
✓	✓	✓	✓					Sets EXAMINE
✓	✓	✓	✓				✓	Sets CONT IDLE
✓	✓	✓			✓	✓	X	Reset by Cont. Cmd
						✓		Sets at end of XFER
						✓		Generates Cont. Int.
								at the end of transfer
						✓		Reset by Disc Cmd.
0	0	0	Y	1	0	1	1	State After OC Reset

X - The state of this status bit depends on the state of drive status Bits 3, 4, 6, 7.

Y - Once set, this bit can only be reset by a reset head command to the drive.

BIT #

0 Header Write Protection Violation

This status bit is set when an attempt is made to write on a sector whose write protection bit is set in the sector and protection is specified in the write command. This status bit is also set when a FORMAT command is attempted and the FORMAT switch is "OFF".

1 Header Compare Failure

This status bit is set in the normal READ, normal WRITE, or READ CHECK modes if the header from the Processor does not agree with that read from the disc. The header compare is carried out before transferring any sector to and from the disc. Header compare failures cause the operation to abort without transferring any data.

This status bit is also set when a transfer has stalled for two index pulses. That is:

- internal sector counter cannot match the sector number from the Processor.

- Sync. cannot be obtained for a read operation.

This bit is also set if the controller has not completed a transfer when a sector mark occurs.

2 Defective Sector

This status bit is set only in normal READ, normal WRITE, or READ CHECK modes when a data transfer is attempted on a sector which has the defective sector bit set in the sector header.

3 Cylinder Overflow

The status bit is set when a data transfer is attempted across a cylinder boundary (Head 19 Sector 19). This bit is also set when an attempt is made to select a head greater than 19.

Once set, this bit remains set until a reset head command to the drive is executed.

4 Busy

This status bit is used to control data transfers to and from the SELCH.

5 Examine

This bit is set whenever one of Bits 0 through 3 is set.

6 Controller Idle (CONT IDLE)

This bit is set when the controller is free to initiate another operation.

7 Data Transfer Error

This status bit is set under the following conditions:

Longitudinal Parity Error - If the controller is in the READ, READ FORMAT, or READ CHECK mode, this bit is set if a longitudinal parity error occurs. In the case of a partial sector read operation, the SELCH interrupts after the last byte is read from the disc, but the controller continues reading until the end of the sector and sets CONT IDLE. If the sector has longitudinal parity error, this status is set before CONT IDLE →1. For multi-sector operations, this bit may set at the end of any sector thus aborting the operation.

Data Overflow - This condition occurs when the SELCH cannot provide or remove data quick enough to satisfy the required transfer rate. If the Data Overflow condition occurs, the SELCH is terminated, thus aborting the data transfer operation. The recovery routine for the Data Overflow condition is to repeat the operation attempted.

Disc Status - All operations: Drive status bits B_3, B_4, B_6 or B_7 for the selected drive are set before starting the transfer or become set during the transfer.

Write Operations: Drive status bits B_0, B_1 for the selected drive are set before starting the transfer or become set during the transfer.

NOTE

When Data Transfer Error is set because of disc status bits 0, 1, it can be reset by an output command to the controller. When Data Transfer Error is set because of disc status bits 3, 4, 6 or 7, it cannot be reset by an output command to the controller.

6.2 Controller Write Data

A write data to the controller address is used to set the required sector header before a data transfer.

The header data can be provided with either one WD (or WDR) and one WH (or WHR) instruction or with three WD (or WDR) instructions. Figure 5 illustrates the Controller Write Data Format.

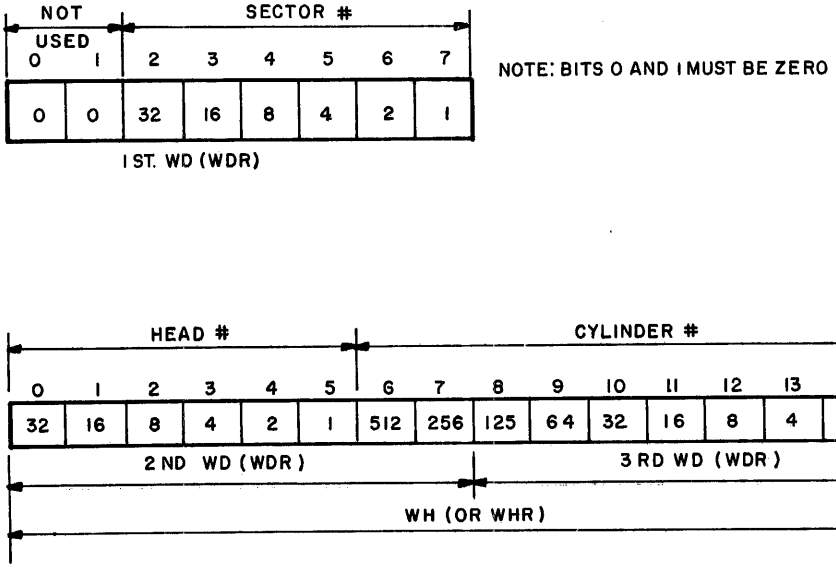


Figure 5, Controller Write Data Format

6.3 Controller Interrupt

The controller generates a device interrupt, if enabled, when the controller idle bit sets at the completion of a controller command.

It does not generate a device interrupt when the controller idle bit sets at the completion of a disc command.

6.4 Controller Programming

The sense status instructions can be directed at the controller address regardless of the state of CONT IDLE.

All other Processor instructions can only be directed at the controller address when CONT IDLE = 1 (except OC Reset which can be used at any time). See Appendix 1 for preferred programming sequences.

NOTE

Any Processor instruction directed at a disc drive device address causes that drive to be selected.

7. DRIVE COMMANDS

7.1 Drive Command Format

Figure 6 illustrates the Drive Command Format.

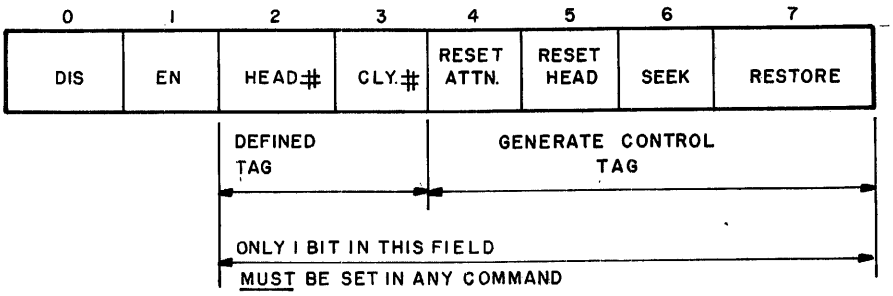


Figure 6. Drive Command Format

BIT #

1 1 DISARM — Interrupts are not queued

1 0 DISABLE — Interrupts are queued, but not passed to the Processor.

0 1 ENABLE — Interrupts are passed to the Processor as they occur.

0 0 NO CHANGE

2 Set Head Number

This command bit causes a Set Head tag to be generated.

3 Set Cylinder Number

This command bit causes a Set Cylinder tag to be generated. This command must be followed by a Seek Command for preferred programming sequences).

4 Reset Attention

This command bit causes the Gated Attention from the disc to be reset which resets the Gate Attention Status Bit.

5 Reset Head Register

This command bit causes a Reset Head Register control sequence to be generated.

6 Seek

This command bit causes a start Seek control sequence to be generated. This command must follow all set cylinder number commands. See Appendix 1 for preferred programming sequences.

7 Restore

This command bit causes a restore control sequence to be generated.

7.2 Drive Status

Figure 7 illustrates the Drive Status Byte.

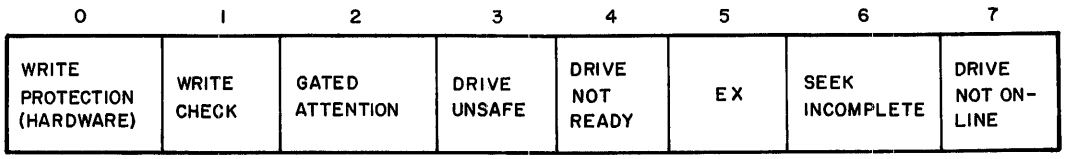


Figure 7. Drive Status Byte

Bit #

0 Write Protection

This bit is set when the READ ONLY switch on the disc drive is ON.

1 Write Check

This bit is set when write current is not present within 10 microseconds of Write Gate. Note that this bit is reset by an output command to the controller address.

2 Gated Attention

This bit is set when Gated Attention from the selected drive is set.

3 Drive Unsafe

This bit is set when the drive is in an unsafe condition. This bit is also set when a drive cannot be selected.

4 Drive Not Ready

This bit is set when the drive is not ready to start a seek, read or write. This normally means that a seek or restore is in progress.

5 Examine

This bit is set whenever one of bits 0 through 3 is set.

6 Seek Incomplete

This bit is set whenever the drive fails to complete a seek or restore operation in a set time.

7 Drive Not On-Line

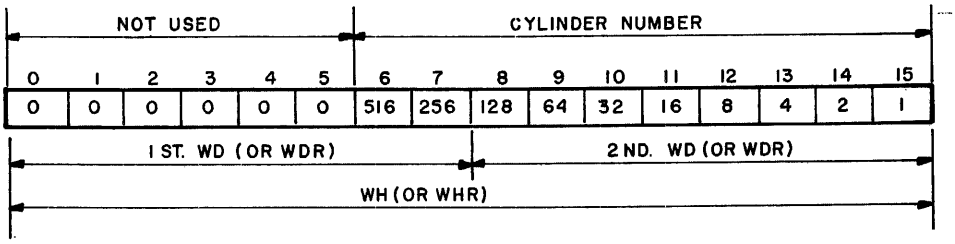
This bit is set when the drive is either unsafe or off-line. It is also set when the drive cannot be selected.

7.3 Drive Write Data

A Write Data to the disc address is used to provide:

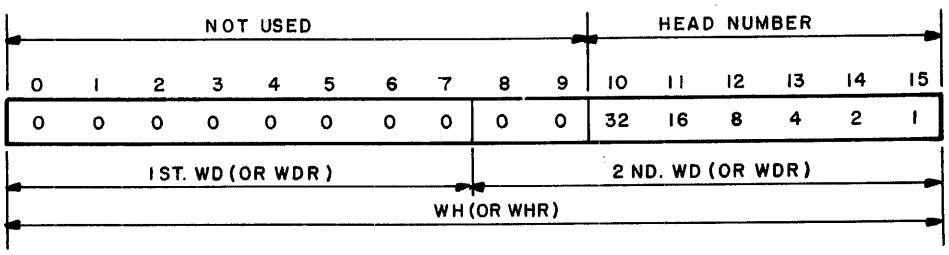
- Cylinder number required for the set cylinder command.
- Head Number required for the set head command.

Figures 8 and 9 illustrate Cylinder and Head Number Data.



Cylinder Number — The Cylinder Number can be provided either with one WH (or WHR) instruction or two WD (or WDR) instructions.

Figure 8. Cylinder Number Data



Head Number — The head number can be provided either with one WH (or WHR) instruction or two WD (or WDR) instructions.

Figure 9. Head Number Data

NOTE

Cylinder bit 6 and head bit 10 are not used and should be set to zero.

7.4 Disc Drive Programming

Processor instruction directed at a disc drive address can only be used when CONT IDLE = 1.

To start a seek and set the head number, see the preferred programming sequences in Appendix 1.

7.5 Disc Interrupt

Figure 10 illustrates the Seek Start Sequence and Figure 11 illustrates the Transfer Sequence.

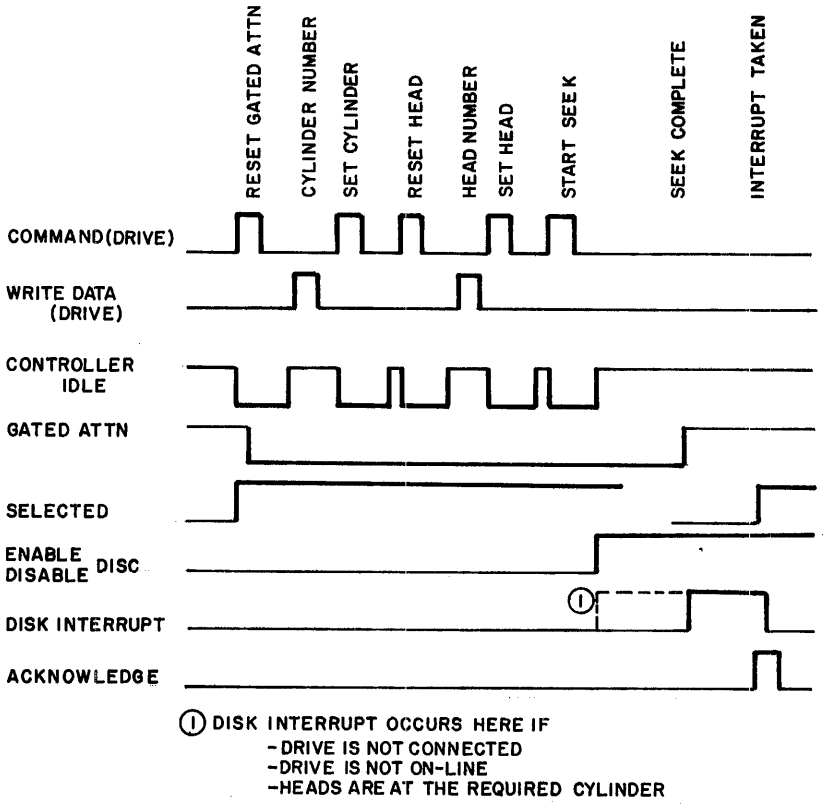


Figure 10. Seek Start Sequence

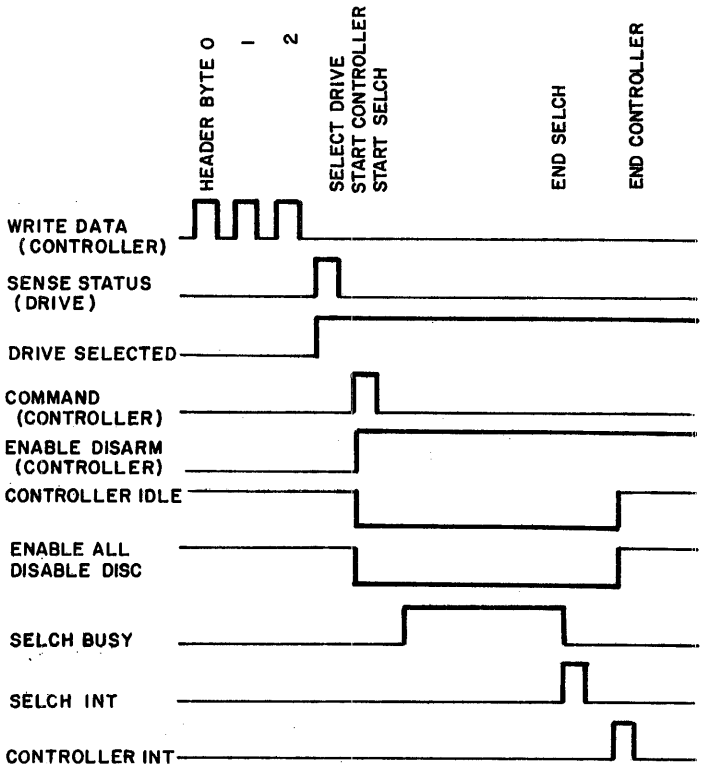


Figure 11. Transfer Sequence

A disc interrupt is generated, if enabled, under the following conditions. The disc interrupt (from all drivers) is disabled when Controller Idle = 0; i.e., drive interrupts are only passed to the Processor when the controller is idle.

- Seek completion or time out (including the case in which the heads are already at the required cylinder).

- Restore completion or time out.

- Power-on sequence completed.

- Drive unsafe bit is set when the attempt is made to select the drive (i.e., drive cannot be selected).

Acknowledge Interrupt for Disc Drive:

When a disc drive interrupt is acknowledged, the following functions are performed:

- Disc drive device address is returned to the CPU.
- The drive is selected.
- Return the status of the selected drive to the Processor.

APPENDIX 1

PREFERRED PROGRAM SEQUENCES

```
*
*   SAMPLE PROGRAM SEQUENCES
*
*      THIS IS NOT A COMPLETE PROGRAM
*      BUT GIVES EXAMPLES OF SEQUENCES
*
*
*
*     STAT = STATUS
*     CYL  = CYLINDER #
*     FILE = FILE ADDRESS
*     CONT = CONTROLLER ADDRESS
*    SELCH = SELCH ADDRESS
*
START     SSR    FILE,STAT        CHECK DISC
          THI    STAT,X'19'       STATUS OK ?
          BTC    2,ABORT          NO -
*
* SEEK SUBROUTINE
*
SEEK      WHR    FILE,CYL         WRITE CYL # TO FILE
          OC     FILE,CYLCMD
SEEL      SSR    CONT,STAT        WAIT FOR IDLE
          BNP    SEEL
          OC     FILE,RSTATT      RESET ATTENTION
SEEM      SSR    CONT,STAT        WAIT FOR IDLE
          BNP    SEEM
          OC     FILE,RSTHED      RESET HEAD
SEEN      SSR    CONT,STAT        WAIT FOR IDLE
          BNP    SEEN
          WH     FILE,HEAD        WRITE HEAD TO FILE
          OC     FILE,HEDCMD      SET HEAD
SEEP      SSR    CONT,STAT        WAIT FOR IDLE
          BNP    SEEP
          OC     FILE,SEEK        SEEK
*
* AT THIS POINT WAIT FOR AN INTERRUPT FROM THE DISC, OR
*  WAIT FOR GOOD STATUS.
* EXAMPLE OF SENSE STATUS
SKSTAT    SSR    FILE,STAT        GET STATUS
          THI    STAT,7            BAD STATUS ?
          BTC    ERROR             YES
          BNZ    SKSTAT            SEEK COMPLETE ? - NO
          B      TRANS             YES - TRANSFER DATA
*
*  CONTINUE TO DATA TRANSFER
*
*
* EXAMPLE OF INTERRUPT
*
SKINT     LHI    R7,SKRTN         INDICATE RETURN
          STH    FILRTN            FROM INT.
          B      SKINT
*
SKRTN     B      TRANS            TRANSFER DATA
*
*
```

```
* TRANSFER DATA
*
TRANS    WH    SELCH,SA        STARTING ADDRESS
         WH    SELCH,FA        ENDING ADDRESS
         OC    FILE,RSTATT     RESET ATTENTION
X        SSR   CONT,STAT       WAIT FOR
         BNP   X                  CONTROLLER IDLE
         OC    FILE,RSTHED     RESET HEAD
Y        SSR   CONT,STAT       WAIT FOR
         BNP   Y                  CONTROLLER IDLE
         WH    FILE,HEAD       WRITE HEAD # TO FILE
         OC    FILE,HEDCMD     SELECT HEAD
Z        SSR   CONT,STAT       WAIT FOR
         BNP   Z                  CONTROLLER IDLE
         WD    CONT,HED1       WRITE THE 3 BYTES OF HEADE
         WH    CONT,HED2-3       INFO. TO THE CONTROLLER
         OC    CONT,READ/WRITE
         OC    SELCH,GO(READ/WRITE)
*
* IF USING INTERRUPTS WAIT FOR A SELCH AND CONTROLLER
*  INTERRUPT (ENABLE IN THE COMMAND) TO OCCURE.
*
* IF NOT USING INTERRUPTS DO A SENSE STATUS ON THE SELCH AND
*  WAIT FOR SELCH NOT BUSY. THEN DO A SENSE STATUS ON THE CONT-
*  ROLLER AND WAIT FOR IDLE.
* EXAMPLE USING SENSE STATUS
*
SSTWAY   SSR   SELCH,STAT     WAIT FOR SELCH NOT
         BC    SSTWAY             BUSY
         OC    SELCH,STOP      STOP SELCH
         SSR   CONT,STAT       WAIT FOR CONTROLLER
         BNP   SSTWAY           IDLE
         BTC   5,ERROR          IF BAD STATUS - ERROR
*
*  GOOD STATUS-TRANSFER COMPLETE
*
*
* EXAMPLE USING INTERRUPTS
*
*
INTWAY   LHI   R8,INTX         INDICATE RETURN
         STH   R8,SELRTN
         B     INTWAY          WAIT FOR INTERRUPT
INTX     LHI   R8,START        WAIT FOR CONTROLLER
         STH   R8,CNTRTN         INTERRUPT
         B     INTX
*
**    7/32 PROCESSOR
*
*  THE USER MUST SET UP THE INTERRUPT VECTOR TABLE BY
*  MULTIPLYING THE DEVICE ADDRESS BY 2, AND ADDING X'D0'
*
*      2(DEVICE ADD.)+X'D0' = ADDRESS OF POINTER TO
*                              THE INTERRUPT ROUTINE
*
* SELCH INTERRUPT - 7/32
```

B6 * 2 + D0 = 23C

```
*
SINT     LR     R3,R3          GET SELCH STATUS
         BNZ    ERROR          BUSY SET = ERROR
         OC     SELCH,STOP
         LHL    R1,SELRTN
         LPSWR  R0             RETURN TO NEXT STEP
*
* CONTROLLER INTERRUPT  -  7/32
*
CINT     LR     R3,R3
         BTC    5,ERROR        ERROR
         LHL    R1,CNTRTN
         LPSWR  R0
*
* FILE INTERRUPT  - 7/32
*
FINT     LHR    R3,R3          GET FILE STATUS
         BNZ    ERROR          BAD STATUS - ERROR
         LHL    R1,FILRTN
         LPSWR  R0             RETURN
*
* INTERRUPT FOR 16 BIT MACHINE
*
INT      AIR    R8,STAT
         CLH    R8,FILE        DISC INTERRUPT ?
         BE     INTD           YES
         CLH    R8,CONT        CONTROLLER INTERRUPT ?
         BE     INTC           YES
         CLH    R8,SELCH       SELCH INTERRUPT ?
         BE     INTS           YES
         B      ABORT          UNWANTED INTERRUPT
*
* DISC INTERRUPT  -  16 BIT PROCESSOR
*
INTD     LHR    STAT,STAT
         BNZ    ERROR
         LPSW   FILRTN-2
*
* CONTROLLER INTERRUPT  - 16 BIT PROCESSOR
*
*
INTC     LHR    STAT,STAT
         BTC    5,ERROR        BAD STATUS
         LPSW   CNTRTN-2
*
*
* SELCH INTERRUPT
*
INTS     OC     SELCH,STOP
         LPSW   SELRTN-2
*
*
ABORT     ERROR ROUTINES
ERROR       TO HANDLE BAD STATUS AND INTERRUPTS
CYLCMD   DC     X'10'
RSTATT   DC     X'08'
```

```
RSTHED   DC    X'04'
HEDCMD   DC    X'20'
SEEK     DC    X'C2',OR X'42'
STOP     DC    X'08'
FA       DS    XX
SA       DS    XX
FILRTN   DS    XX
CNTRTN   DS    XX
SELRTN   DS    XX
*
```

INTERDATA

DISC CONTROLLER
35-532

FRONT PANEL MAP

ROW 2	ROW 1	TERM. NO.	CONN
	RESETOB	16	
	DCNIO	15	
	FCGO	14	
	FCBI	13	
	DCCLRO	12	
FST2I	FST1I	11	
EGATO	HADVGI	10	
WETGI	BUSDAI	09	3
SECMI	INEXI	08	
CGO	EOCYI	07	
SMOD3I	SMOD2I	06	
GATN30	SMOD1I	05	
MSEL10	MSEL00	04	
GATN10	SMOD0I	03	
MSEL20	GATN00	02	
	MSEL30	01	
GND		00	
GND		24	
		23	
		22	
		21	
		20	
		19	
		18	
		17	
		16	
	MSEL30	15	
	SMOD30	14	
	GATN30	13	2
		12	
	MSEL20	11	
	SMOD20	10	
	GATN20	09	
		08	
	MSEL10	07	
	SMOD10	06	
	GATN10	05	
		04	
		03	
	MSEL00	02	
	SMOD00	01	
GND	GATN00	00	

FILE CONTROLLER
35-531

FRONT PANEL MAP

ROW 2	ROW 1	TERM. NO.	CONN
	RESETOB	16	
	DCNIO	15	
	FCGO	14	
	FCBI	13	
	DCCLRO	12	
FST2I	FST1I	11	
EGATO	HADVGI	10	
EERSGI	SELHDI	09	3
WETGI	BUSDAI	08	
SECMI	INEXI	07	
CGO	EOCYI	06	
SMO3I	SMOD2I	05	
GATN30	SMOD1I	04	
MSEL10	MSEL00	03	
GATN20	SMOD0I	02	
GATN10	GATN00	01	
MSEL20	MSEL30	00	
	CGO	24	
		23	
		22	
S.GND		21	
S.GND	EOYLO	20	
	WCUBO	19	
	SECMO	18	
	EOCYO	17	
	SICO	16	
	USAFO	15	
	INEXO	14	
	ONLO	13	2
	DRYDO	12	
	SCTO	11	
	SHTO	10	
	CTO	09	
	DB80	08	
	DB70	07	
	DB60	06	
	DB50	05	
	DB40	04	
	DB30	03	
	DB20	02	
	DB10	01	
S.GND	DB00	00	

DISC & FILE CONTROLLERS

* DENOTES SIGNAL USED ON DISC CONTROLLER ONLY.

BACK PANEL MAP

ROW 2	ROW 1	TERM. NO.	CONN
		41	
		40	
		39	
		38	
		37	
		36	
		35	
		34	
		33	
		32	
		31	
		30	
		29	
		28	
		27	
	SCLEO	26	
		25	
		24	
RINO	SYNCO	23	
TACKO	EACKO	22	1
DAO	CLOTO	21	
CMDDO	DZO *	20	
ADRSO	SZO	19	
D120	D140	18	
D130	D120	17	
D110	D100	16	
D090	D080	15	
		14	
		13	
		12	
		11	
		10	
		09	
		08	
		07	
		06	
		05	
		04	
		03	
		02	
		01	
		00	

DISC CONTROL CONN 3 — 17-317 (INTERNAL CABLE) — FILE CONTROL CONN 3

DISC CONTROL CONN 3		FILE CONTROL CONN 3
100	MSEL30	100
200	MSEL20	200
101	GATN00	101
201	GATN10	201
102	SMOD0I	102
202	GATN20	202
103	MSEL00	103
203	MSEL10	203
104	SMOD1I	104
204	GATN30	204
105	SMOD2I	105
205	SMOD3I	205
106	EOCYI	106
206	CGO	206
107	INEXI	107
207	SECMI	207
108	BUSDAI	108
208	WRTGI	208
109	SELHDI	109
209	ERRSGI	209
110	HADVGI	110
210	EGATO	210
111	FST1I	111
211	FST2I	211
112	DCCLRO	112
212		212
113	FCBI	113
213		213
114	FCGO	114
214		214
115	DCNIO	115
215		215
116	RESETOB	116
216		216

17-315 (INTERNAL CABLE)

DISC CONTROLLER (35-532)

RDD0	READ DATA 00	J1	12
WDD0	WRITE DATA 00		5
CONN 2			
100	GATN00	P	21
200	GND		26
101	SMOD00	P	23
201	GND		27
102	MSEL00	P	22
202	GND		28
203	SHIELD GND		25
P5	+5 TERMINATOR		13
DCG	DC GND		3

17-315 (INTERNAL CABLE)

RD10	READ DATA 10	J2	12
WD10	WRITE DATA 10		5
CONN 2			
105	GATN10	P	21
205	GND		26
106	SMOD10	P	23
206	GND		27
107	MSEL10	P	22
207	GND		28
208	SHIELD GND		25
P5	+5 TERMINATOR		13
DCG	DC GND		3

17-315 (INTERNAL CABLE)

RD20	READ DATA 20	J3	12
WD20	WRITE DATA 20		5
CONN 2			
110	GATN20	P	21
210	GND		26
111	SMOD20	P	23
211	GND		27
112	MSEL20	P	22
212	GND		28
213	SHIELD GND		25
P5	+5 TERMINATOR		13
DCG	DC GND		3

17-315 (INTERNAL CABLE)

RD30	READ DATA 30	J4	12
WD30	WRITE DATA 30		5
CONN 2			
115	GATN30	P	21
215	GND		26
116	SMOD30	P	23
216	GND		27
117	MSEL30	P	22
217	GND		28
218	SHIELD GND		25
P5	+5 TERMINATOR		13
DCG	DC GND		3

17-316 (INTERNAL CABLE)

FILE CONTROL (35-531) CONN 2

P (TYP. 22 PLACES)

101	DB10	J5	01
201	GND		02
102	DB20		03
202	GND		
103	DB30		04
203	GND		05
104	DB40		07
204	GND		
105	DB50		08
205	GND		10
106	DB60		11
206	GND		
107	DB70		12
207	GND		13
108	DB80		14
208	GND		
100	DB00		15
200	GND		16
111	SCTO		17
211	GND		
110	SHTO		18
210	GND		20
109	CTO		21
209	GND		
112	DRYDO		52
212	GND		53
113	ONLO		54
213	GND		
114	INEXO		55
214	GND		56
115	USAFO		57
215	GND		
116	SICO		58
216	GND		59
117	EOCYO		60
217	GND		
118	SECMO		62
218	GND		63
119	WCUBO		64
219	GND		
120	EOYLO		67
220	GND		66
221	SHEILD GND		80
222	GND		82
124	CGO	→ TB1-5	
P			
TB1-6	CONTROLLER GND		76
K2-6	SEQUENCE PICK		77
K2-9	+36V SEQ. PWR		78

NOTE: THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT.

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL

DISC CONT.	35-532 R07	SHT. 7-15
FILE CONT.	35-531 R04	SHT 3-6

REVISIONS

RELEASED FOR PRODUCTION
ENG. [illegible] DATE 9/21/74

WIRES 22 & 23 WERE REVERSED(4). 35-532 R01 WAS R00. REVISED SHEETS 7, 9 THRU 13 & 15.					
JHB	HEH	ECN 2313	—	10-29-74	R01
REVISED SHT 5					
JHB	HEH	2383	—	1-6-75	R02
REVISED SHTS. 10 & 15. P.C. BD. REV. LEVEL TABLE BELOW: 35-532 WAS R01					
PE	HEH	2399	—	1-28-75	R03
REVISED SHTS. 3, 4 & 6. P.C. BD. REV. LEVEL TABLE BELOW: 35-531 WAS R01.					
JHB	HEH	2581	—	8-8-75	R04
REVISED SHT. 5. P.C. BD. REV. LEVEL TABLE BELOW: 35-531 WAS R03.					
JHB	HEH	2586	—	8-12-75	R05
REVISED SHT 15. P.C. BD. REV LEVEL TABLE BELOW; 35-532 WAS R02.					
RC		2627	—	9-26-75	R06
REVISED SHT 15. P.C. BD REV LEVEL BELOW; 35-532 WAS R05					
DS	JT	2963A	—	2-13-76	R07
REVISED SHT 15, 35-532 REV LEVEL WAS R06					
DS	JT	3084	—	6-30-77	R08

SHEET INDEX	REV.	8	1	1	2	1	1		1	2	1	1	1		5					
	SHT. NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15				

NOTES

THIS INFORMATION IS PROPRIETARY AND IS SUPPLIED BY INTERDATA FOR THE SOLE PURPOSE OF MAINTAINING AND USING INTERDATA SUPPLIED EQUIPMENT AND SHALL NOT BE USED FOR ANY OTHER PURPOSE UNLESS SPECIFICALLY INDICATED

NAME	TITLE	DATE
R. EDWARDS	DRAFT	8-19-74
R. F. CERO	CHK	9-26-74
R. STAGER	ENGR	9-26-74
D. BOPP	SYS TST	9-26-74
J. PISARCIK	MGR	9-26-74

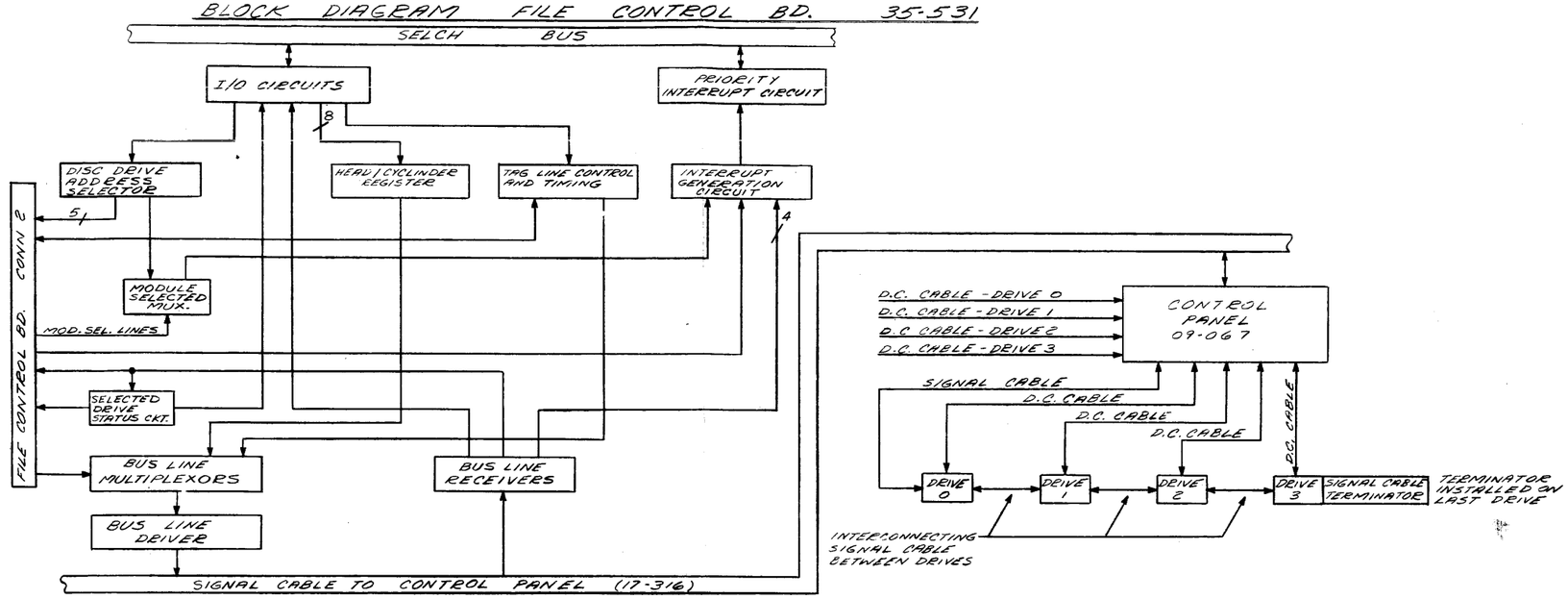
TITLE FUNCTIONAL SCHEMATIC
40 MEGABYTE
DISC

TASK NO. 03080 DWG NO. 02-359 R09 D08 SHEET OF 1 — 15

BRUNING 44-231 16042

INTERDATA®

BLOCK DIAGRAM FILE CONTROL BD. 35-531



BACK PANEL PIN INDEX

MNEMONIC	FILE CONT.	DISC CONT.
ADRS0	3F1	7E1
ATN0	3A1	7A1
CLOT0	3C1	7C1
CMD0	3D1	7D1
DO80	3N1	7N1
DO90	3M1	7M1
DI00	3L1	7L1
DI10	3L1	7L1
DI20	3K1	7K1
DI30	3J1	7J1
DI40	3H1	7H1
DI50	3G1	7G1
DR0	3D1	7D1
DR0		7E1
EACK0	3B1	7B1
SCLR0	3E1	7E1
SR0	3D1	7D1
SYNC0	3N8	7K9
TACK0	3A5	7A5

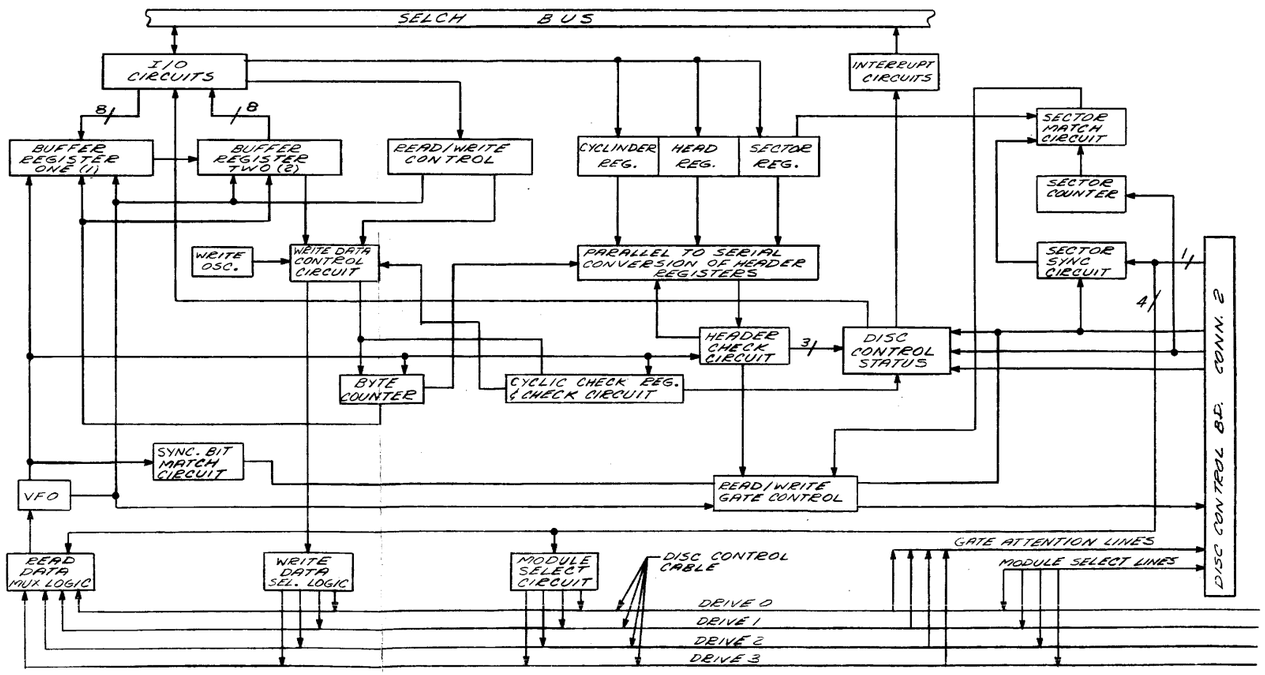
CONNECTOR 2 PIN INDEX

MNEMONIC	FILE CONT.	DISC CONT.
CG0	3M9	
CT0	6M9	
DB00	6D9	
DB10	6E9	
DB20	6F9	
DB30	6G9	
DB40	6G9	
DB50	6H9	
DB60	6J9	
DB70	6K9	
DB80	6L9	
DBYDO	5A9	
EOCY0	5L9	
GATN00		1AG7
GATN10		1AG7
GATN20		1AG8
GATN30		1AG8
INEX0	5L8	
MSEL00		1AG7
MSEL10		1AG7
MSEL20		1AG8
MSEL30		1AG8
ONL0	5A8	
BOYL0	5A6	
SC70	6N9	
SECM0	5G9	
SHT0	6H9	
SI00	5A7	
SMOD00		1AG6
SMOD10		1AG6
SMOD20		1AG5
SMOD30		1AG4
USAF0	5A5	
WCUR0	5A5	

CONNECTOR 3 PIN INDEX

MNEMONIC	FILE CONT.	DISC CONT.
BUSDAI	6R7	1AM7
CG0	3E9	1AJ8
DCCLR0	5S6	10N9
DCNI0	5H2	11R3
EOCYI	5N9	12K4
ERASGI	6J6	11J5
FOBI	6N2	11K4
FCG0	5R5	12R5
FST1I	5F8	12K2
FST2I	5F7	12K2
GATN00	5A1	1AC7
GATN10	5A2	1AC7
GATN20	5A3	1AC8
GATN30	5A4	1AC8
HADVGI	6A2	1354
INEXI	5N8	12R5
MSEL00	5G6	1AC7
MSEL10	5G7	1AC7
MSEL20	5G8	1AC8
MSEL30	5G8	1AC8
RESETOB	4H2	10M8
RGATO	6F1	10N9
SECMI	5K9	12E6
SELMDI	6R6	9R6
SMOD0I	5N1	1AC6
SMOD1I	5N2	1AC6
SMOD2I	5N2	1AC5
SMOD3I	5N2	1AC4
WRTGI	6G6	11J7

BLOCK DIAGRAM DISC CONTROL BD. 35-532



NOTES

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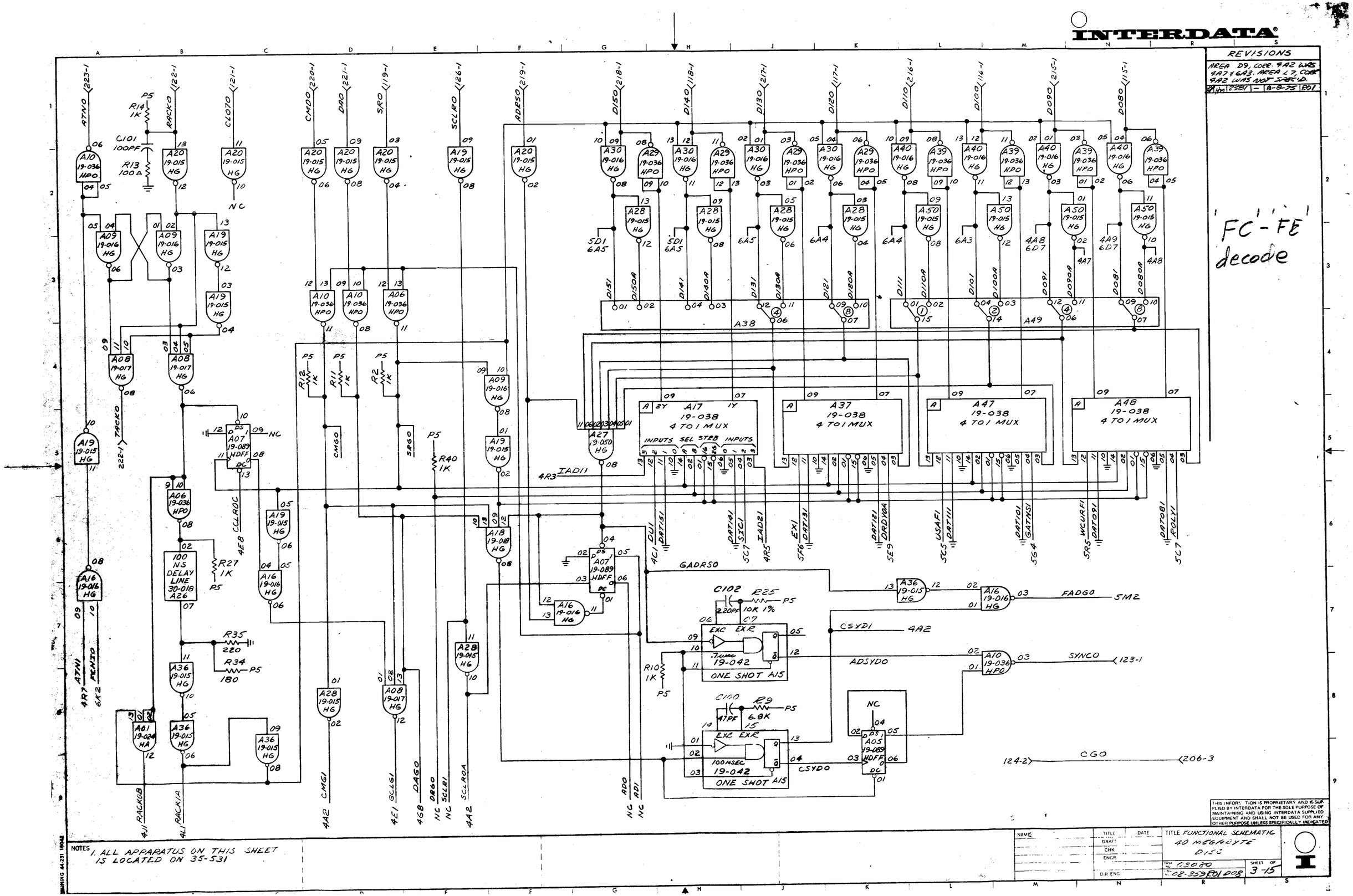
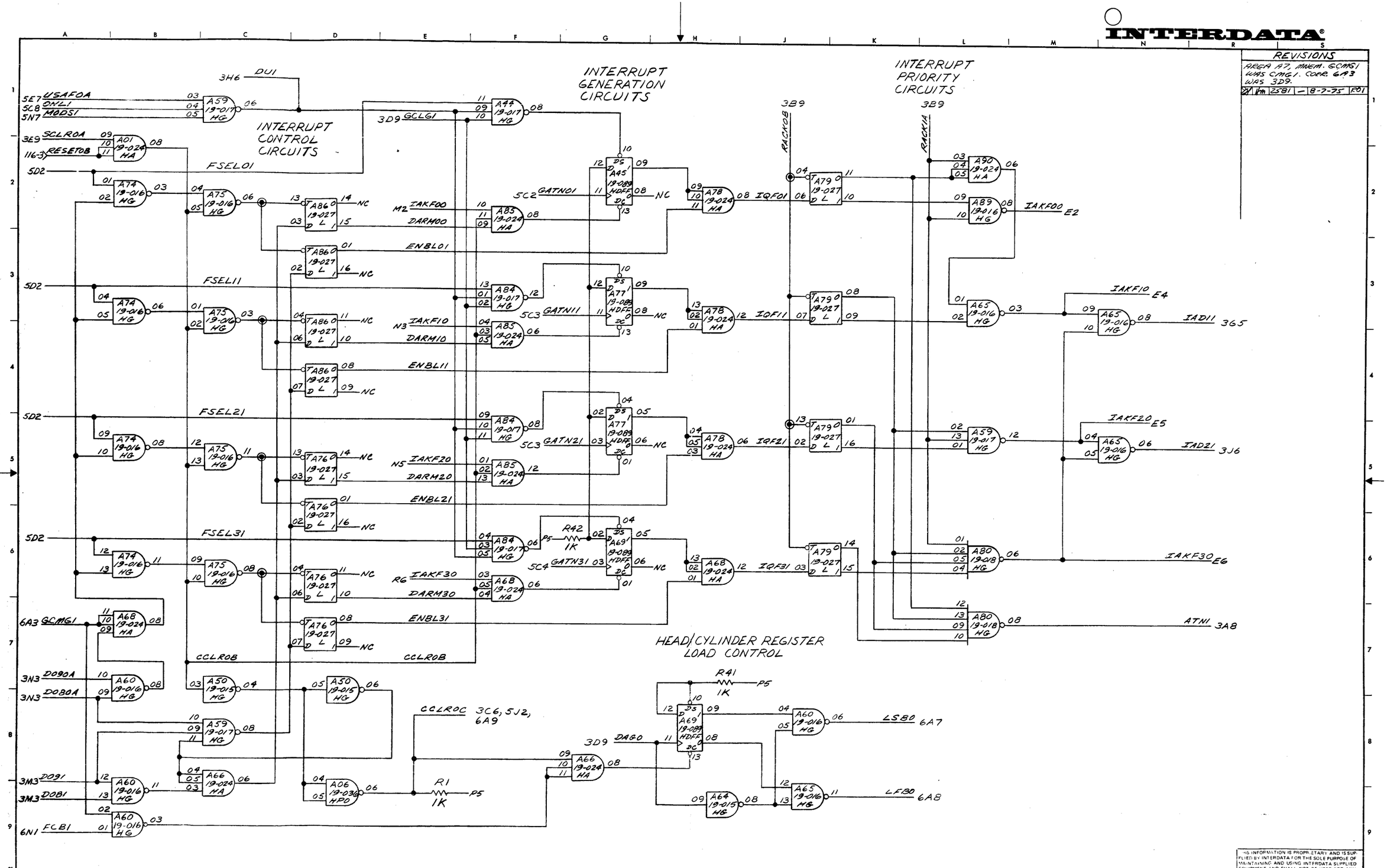
NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
40 MEGABYTE DISC

TASK NO. 03080
DWG NO. 02-359 D08
SHEET OF 2-13

BRUNFIG 44-231 16042


INTERDATA
REVISIONS
AREA D9, CORR. 4A2 WAS 4A7 & 6A3. AREA L7, CORR 4A2 WAS NOT SPEC'D.
2581 - 8-8-75 R01
'FC'-'FE' decode
A17 19-038 4 TO 1 MUX
A37 19-038 4 TO 1 MUX
A47 19-038 4 TO 1 MUX
A48 19-038 4 TO 1 MUX
100 NS DELAY LINE 30-018 A26
ONE SHOT A15
ONE SHOT A15
GADRSO
FADGO
CSYDI
ADSYDO
SYNCO
CSYDO
CGO
NOTES 1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-531
THIS INFORMATION IS PROPRIETARY AND IS SUPPLIED BY INTERDATA FOR THE SOLE PURPOSE OF MAINTAINING AND USING INTERDATA SUPPLIED EQUIPMENT AND SHALL NOT BE USED FOR ANY OTHER PURPOSE UNLESS SPECIFICALLY INDICATED
TITLE FUNCTIONAL SCHEMATIC 40 MEGABYTE DISC
03080
02-359 R01 D08
SHEET 3 OF 15


INTERDATA
REVISIONS
AREA A7, MNEM. GCMG1 WAS CMG1. CORR. 6A3 WAS 3D9.
INTERRUPT CONTROL CIRCUITS
INTERRUPT GENERATION CIRCUITS
INTERRUPT PRIORITY CIRCUITS
HEAD/CYLINDER REGISTER LOAD CONTROL
USAFOA
ONL1
MODS1
SCLROA
RESETOB
FSEL01
FSEL11
FSEL21
FSEL31
GCLG1
GATN01
GATN11
GATN21
GATN31
IAKF00
DARM00
ENBL01
IAKF10
DARM10
ENBL11
IAKF20
DARM20
ENBL21
IAKF30
DARM30
ENBL31
CCLROB
CCLROC
GCMG1
D090A
D080A
D091
D081
FCB1
RACKOB
RACK1A
IQF01
IQF11
IQF21
IQF31
IAKF00
IAKF10
IAKF20
IAKF30
IAD11
IAD21
ATN1
LSB0
LFB0
DAG0
R42 1K
R41 1K
R1 1K
P5
NOTES
1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-531
THIS INFORMATION IS PROPRIETARY AND IS SUPPLIED BY INTERDATA FOR THE SOLE PURPOSE OF MAINTAINING AND USING INTERDATA SUPPLIED EQUIPMENT AND SHALL NOT BE USED FOR ANY OTHER PURPOSE UNLESS SPECIFICALLY INDICATED
NAME
TITLE
DATE
DRAFT
CHK
ENGR
DIR ENG
TITLE FUNCTIONAL SCHEMATIC 40 MEGABYTE DISC
TASK NO 02080
DWG NO 02 359R01D08
SHEET 4 OF 15
BRUNING 44-231 16042

INTERDATA®

REVISIONS				
AREA E6 & E7 DELETED CONN. BETWEEN A91-12 & A13-10.				
DN	12383	—	1-8-75	R01
AREA 12-9, CO-ORDINATION 'N9' WAS NOT SPECD., AREA N-8 @ B1 PIN 12 WAS SHOWN THUS: 13 A81 19-015 HG 12 INEX1 <107-3				
25886	—	12 AUG 75	R02	

FILE STATUS LINES

R18 330, R17 PS 220 — 101-3 GATN00 — A11 19-015 HG pin 03 — pin 04 GATN01

R16 330, R15 PS 220 — 201-3 GATN10 — A11 19-015 HG pin 01 — pin 02 GATN11

R20 330, R19 PS 220 — 202-3 GATN20 — A11 19-015 HG pin 05 — pin 06 GATN21

R4 330, R3 PS 220 — 204-3 GATN30 — A11 19-015 HG pin 13 — pin 12 GATN31

R54 330, R53 PS 220 — 115-2 USAF0 — A81 19-015 HG pin 05 — pin 06

R58 330, R57 PS 220 — 119-2 WCUR0 — A91 19-015 HG pin 03 — pin 04

R56 330, R55 PS 220 — 120-2 ROLY0 — A91 19-015 HG pin 01 — pin 02

R52 330, R51 PS 220 — 116-2 SIC0 — A81 19-015 HG pin 03 — pin 04

R46 330, R45 PS 220 — 113-2 ONL0 — A81 19-015 HG pin 11 — pin 10

R48 330, R47 PS 220 — 112-2 DRDY0 — A81 19-015 HG pin 09 — pin 08

4F2, 4F3, 4F5, 4F6

USAF1 3L6

WCUR0A N5

EX1 3J6

WCURF1 S5 — A82 19-015 HG pin 09 — pin 08

3R6, N7

ROLY1 — A91 19-015 HG pin 13 — pin 12

3J6

ROLYF0 S7

FST21 <211-3

USAF0A 4A1

SIC1 — A91 19-015 HG pin 09 — pin 08

FST11 <111-3

ONL1 4A1

DRDY1 — A82 19-015 HG pin 11 — pin 10 — DRDY0A 3K6

FILE STATUS

GATED ATTENTION STATUS

4A6, 4A4, 4A3, 4A2

A21 19-026 HG: pins 13, 12, 04, 05, 03, 11, 10, 01, 02 — pin 08 GATNS1 3M6

A82 19-015 HG pin 01 — pin 02

FILE ADDRESS SELECTION LOGIC

3G3 DI51 15, 3H3 DI41 14, 13, 12 — A25 19-032 1 OF 10 DECODER (A I B N C P D S — O 0 1 2 3 OUTPUTS) — 01, 02, 03, 04

R26 PS 1K — A24 19-015 HG pin 11 — pin 10

R28 PS 1K — A24 19-015 HG pin 05 — pin 06

R29 PS 1K — A24 19-015 HG pin 13 — pin 12

R30 PS 1K — A24 19-015 HG pin 03 — pin 04

A23 19-071 CLR HDFF: D 13, 04, 12, 05, 09 CLK, 01 CLR — Q 15, 14, 02, 03, 10, 11, 07, 06

CCLR0C 4E8

FSEL00, FSEL01, FSEL20, FSEL30, FSEL31, FSEL21, FSEL11, FSEL01

FADG0 3N6

A12 19-015 HG: pin 05 — pin 06 SMOD01 <102-3

A12 19-015 HG: pin 13 — pin 12 SMOD11 <104-3

A12 19-015 HG: pin 09 — pin 08 SMOD21 <105-3

A12 19-015 HG: pin 11 — pin 10 SMOD31 <205-3

A24 19-015 HG: pin 09 — pin 08

A14 19-017 HG: pins 02, 01, 13 — pin 12

A14 19-017 HG: pins 10, 09, 11 — pin 08

A14 19-017 HG: pins 03, 04, 05 — pin 06

A04 19-017 HG: pins 03, 05, 04 — pin 06

FILE CHANGE LOGIC

A02 19-025 HA: pins 02, 04, 01, 05 — pin 06 FCG0 — N9 — <114-3

WRITE CURRENT SENSE LOGIC & STATUS FLOP

C103 .0039μf, R31 20K 1% PS

N6, 6J6 ERASG1 01 — A24 19-015 HG pin 02 — pin 01

6K6 SELHD1 02

A34 (2 SECTIONS) ONE SHOT 19-042: pins 14, 15, EXC, EXR, 1, 0, 13 NC, 04, 03 — B01 — 6A8

A33 19-089 HDFF: DS 04, D 02, DC 01 — 05 WCURF1 C6, 3N6; 06 NC

DCCLR0 <112-3

A33 19-089 HDFF: DS 10, D 09 NC, DC 13 — K6 ERASG1/2; C7 ROLY1 11 — 08 ROLYF0 F7

READ ONLY STATUS FLOP

MODULED SELECTED STATUS

R6 330, R5 PS 220 — 103-3 MSEL00 — A11 19-015 HG pin 11 — pin 10

R8 330, R7 PS 220 — 203-3 MSEL10 — A11 19-015 HG pin 09 — pin 08

R24 330, R23 PS 220 — 200-3 MSEL20 — A12 19-015 HG pin 03 — pin 04

R22 330, R21 PS 220 — 100-3 MSEL30 — A12 19-015 HG pin 01 — pin 02

R60 330, R59 PS 220 — 118-2 SECM0 — A91 19-015 HG pin 05 — pin 06 SECM1 <207-3

P/O FILE STATUS LINES

MODULE SELECTED MUX

MSEL00, MSEL10, MSEL20, MSEL30, MSEL01, MSEL11, MSEL21, MSEL31

A22 19-026 HG: pins 12, 13, 05, 03, 04, 01, 02, 10, 11 — pin 08 MODS1 4A1

R44 330, R43 PS 220 — 114-2 INEX0 — A81 19-015 HG pin 13 — pin 12

R50 330, R49 PS 220 — 117-2 EOCY0 — A81 19-015 HG pin 01 — pin 02 EOCY1 <106-3

R61 1K PS5

A93 19-016 HG: pins 01, 02 — pin 03

A92 19-089: DS 07, D 02, CK 0, DC 01 — 05 NC

A93 19-016 HG: pins 04, 05 — pin 06; pins 09, 10 — pin 08

R4 FCG0 — 107-3 <NEX1

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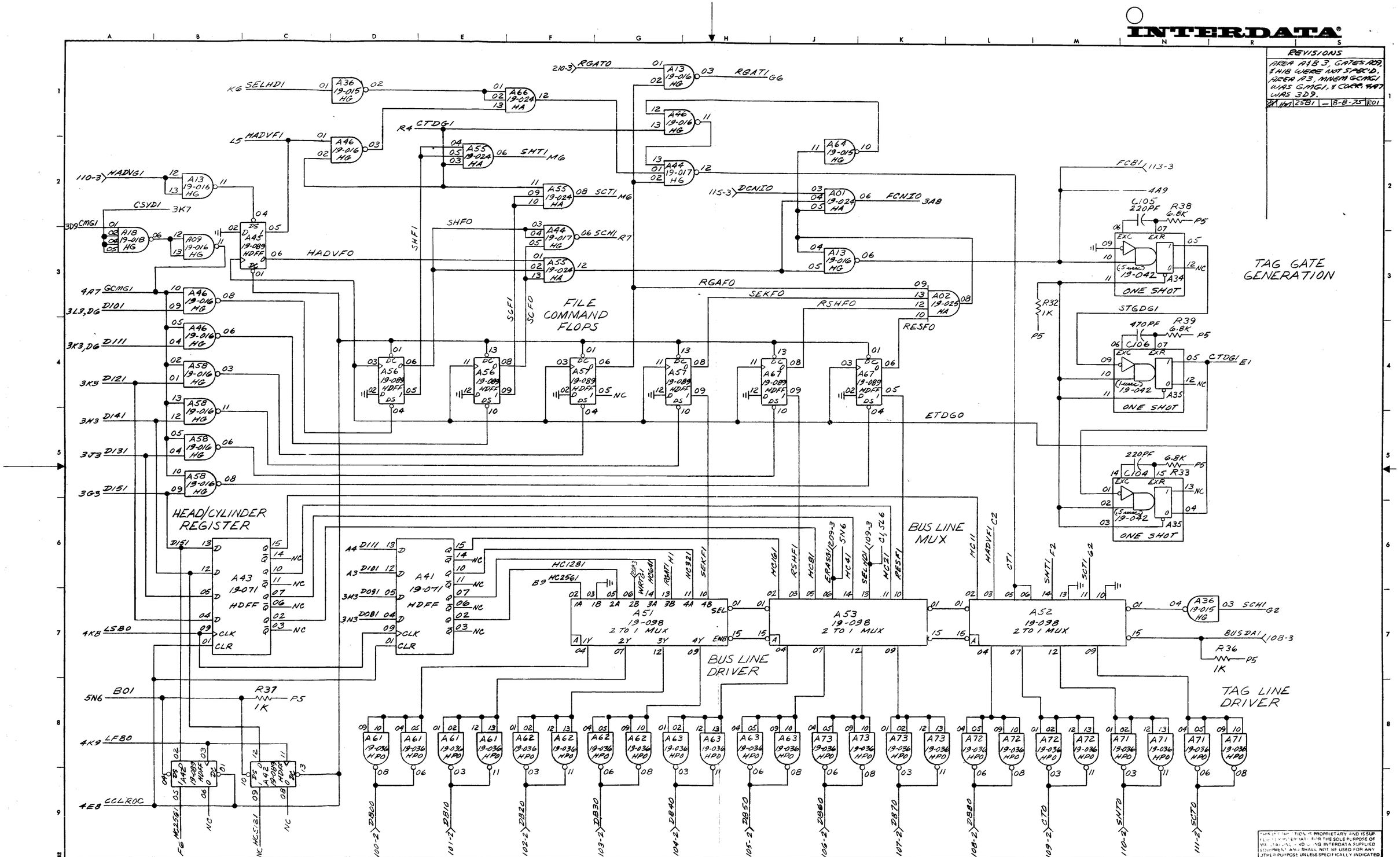
NOTES
1. ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-531

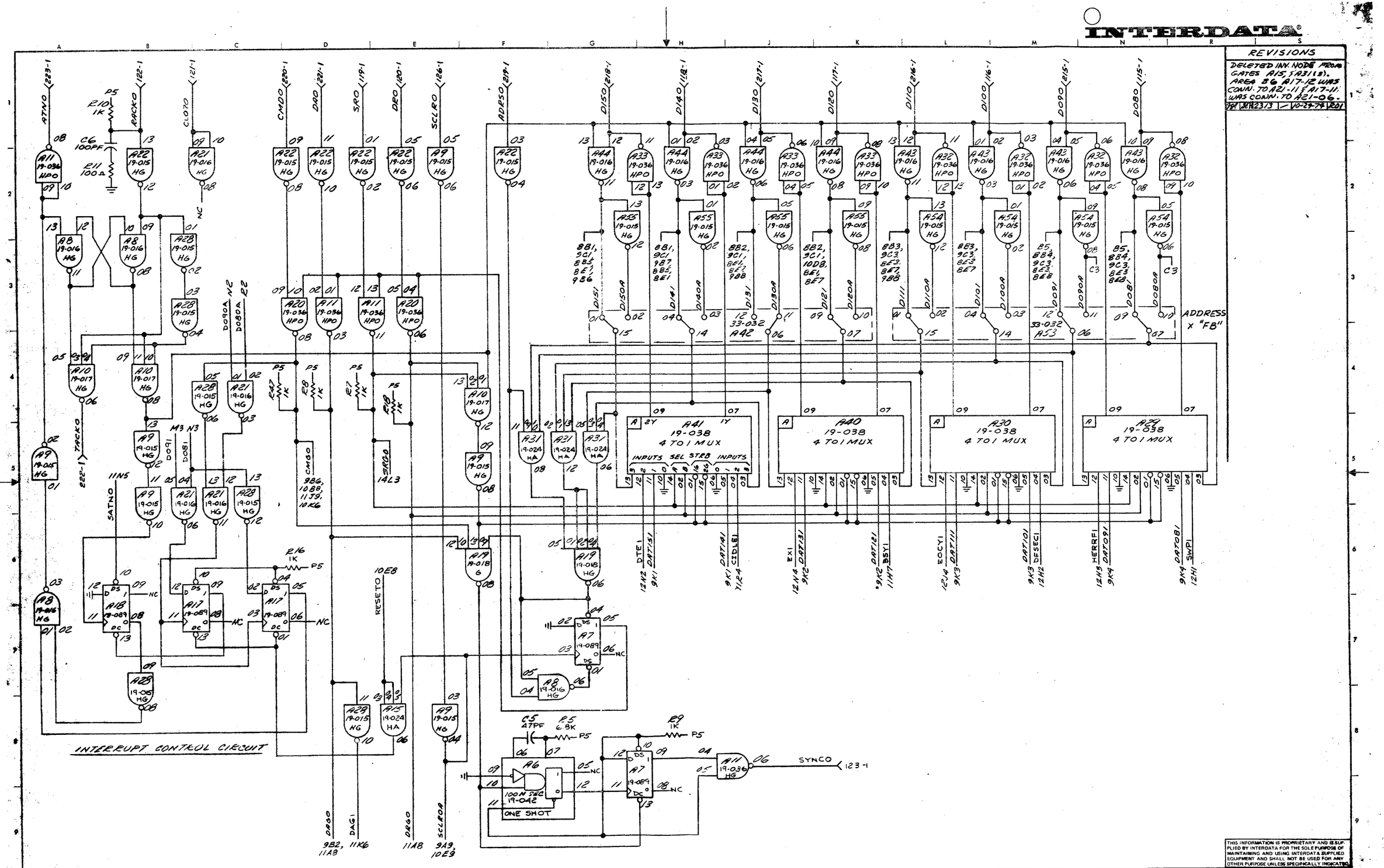
NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

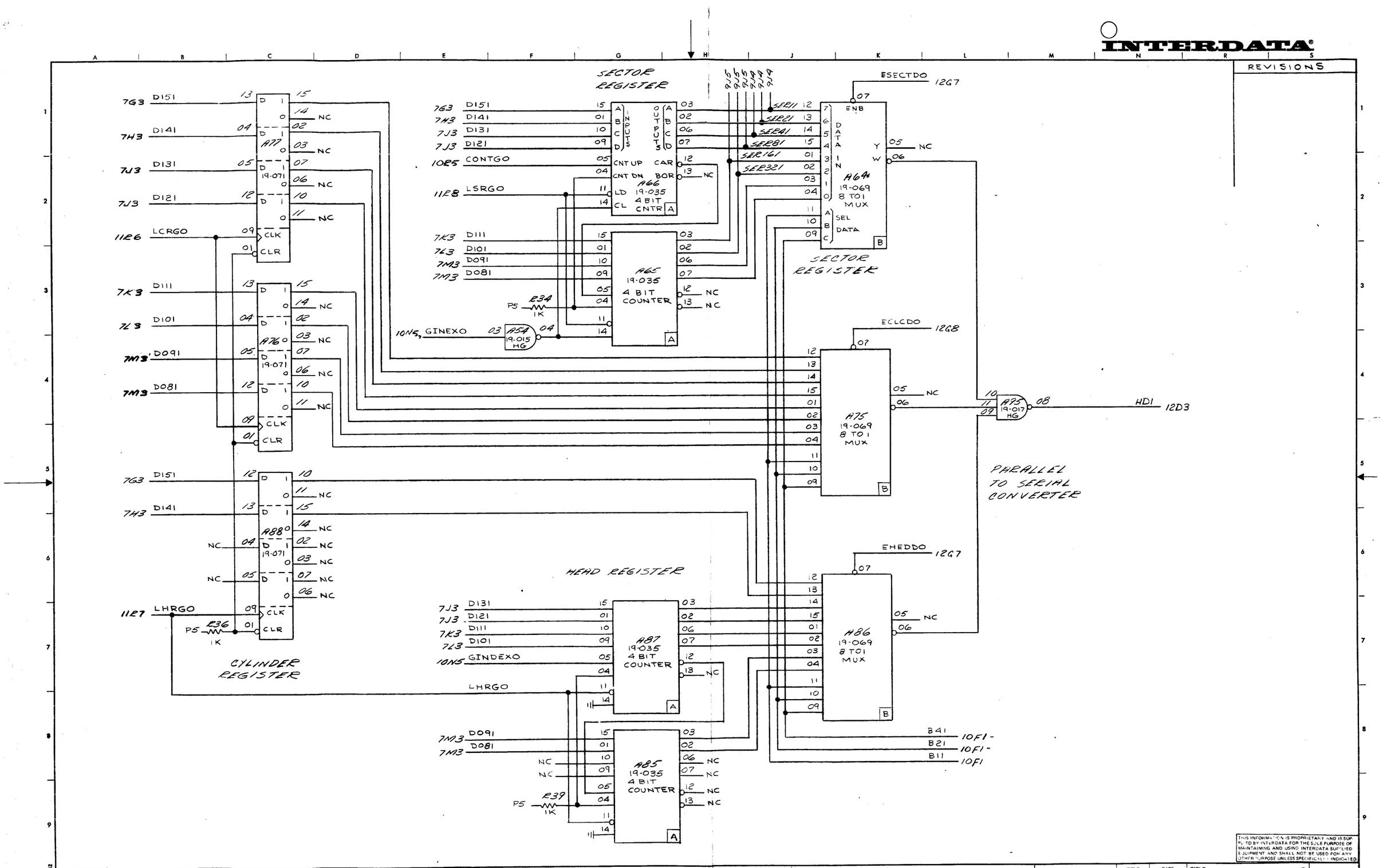
TITLE FUNCTIONAL SCHEMATIC 40 MEGABYTE DISC

TASK NO. 27280 — SHEET OF 5-15

BRUNING 44-231 16042


INTERDATA
REVISIONS
AREA A1 & B3, GATES A09, & H18 WERE NOT SPEC'D. AREA A3, MNEM GCMG1 WAS GMG1, & CORR. 4A7 WAS 3D9.
2581 — 8-8-75 R01
TAG GATE GENERATION
FILE COMMAND FLOPS
HEAD/CYLINDER REGISTER
BUS LINE MUX
BUS LINE DRIVER
TAG LINE DRIVER
ONE SHOT
A51 19-098 2 TO 1 MUX
A52 19-098 2 TO 1 MUX
A53 19-098 2 TO 1 MUX
A43 19-071 HDFF
A41 19-071 HDFF
A45 19-089 HDFF
A56 19-089 HDFF
A57 19-089 HDFF
A67 19-089 HDFF
A42 19-089 HDFF
A61 19-036 HPO
A62 19-036 HPO
A63 19-036 HPO
A71 19-036 HPO
A72 19-036 HPO
A73 19-036 HPO
A36 19-015 HG
A13 19-016 HG
A46 19-016 HG
A44 19-017 HG
A55 19-024 HA
A01 19-024 HA
A02 19-025 HA
A18 19-018 HG
A09 19-016 HG
A58 19-016 HG
A64 19-015 HG
A66 19-024 HA
A02 19-025 HA
C105 220PF
C106 470PF
C104 220PF
R38 6.8K
R39 6.8K
R33 6.8K
R32 1K
R36 1K
R37 1K
SELHD1
HADVF1
HADVG1
CSYD1
CMG1
GCMG1
D101
D111
D121
D141
D131
D151
LSB0
B01
LF80
CCLROC
RGATO
RGATI
CTDG1
SHTI
SCTI
SCHI
SHFO
HADVFO
RGAFO
SEKFO
RSHFO
RESFO
ETDGO
DCNIO
FCNIO
FCB1
STGDG1
BUSDA1
HC1281
HC2561
HC1161
RSHF1
HC81
HC41
HC21
RESF1
HADVF1
CT1
SHT1
SCT1
SEKF1
SHF1
SCF1
SCF0
NC
P5
NOTES
ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-531
NAME E. ROE
TITLE DRAFT CHK ENGR DIR ENG
DATE 3-21-74
TITLE FUNCTIONAL SCHEMATIC 40 MEGABYTE DISC
TASK NO. 03080
DWG NO. C2-359B01D08
SHEET OF 6-15
BRUNING 44-231 16042


INTERDATA
REVISIONS
DELETED INV. NODE FROM GATES A15, & A31(8). AREA B6 A17-12 WAS CONN. TO A21-11 & A17-11 WAS CONN. TO A21-06.
ADDRESS X "FB"
A41 19-038 4 TO 1 MUX
A40 19-038 4 TO 1 MUX
A30 19-038 4 TO 1 MUX
A29 19-038 4 TO 1 MUX
INPUTS SEL STRB INPUTS
INTERRUPT CONTROL CIRCUIT
ONE SHOT
SYNCO
RESETO
ATNO
RACKO
CLOTO
CMDO
DAO
SRO
DRO
SCLRO
ADRSO
D150
D140
D130
D120
D110
D100
D090
D080
TACKO
SATNO
DAGO
DAGI
DRGO
SCLROA
DTE1
DAT151
DAT141
CIDLE1
EX1
DAT131
DAT121
BSY1
EOCY1
DAT111
DAT101
DFSEC1
HERRF1
DAT091
DAT081
SWP1
NOTES ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-532, DISC CONTROL.
THIS INFORMATION IS PROPRIETARY AND IS SUPPLIED BY INTERDATA FOR THE SOLE PURPOSE OF MAINTAINING AND USING INTERDATA SUPPLIED EQUIPMENT AND SHALL NOT BE USED FOR ANY OTHER PURPOSE UNLESS SPECIFICALLY INDICATED.
TITLE FUNCTIONAL SCHEMATIC
40 MEGABYTE DISC
030.50
02-359 R01 D08
SHEET 7 OF 15



NOTES ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-532 DISC CONTROL.

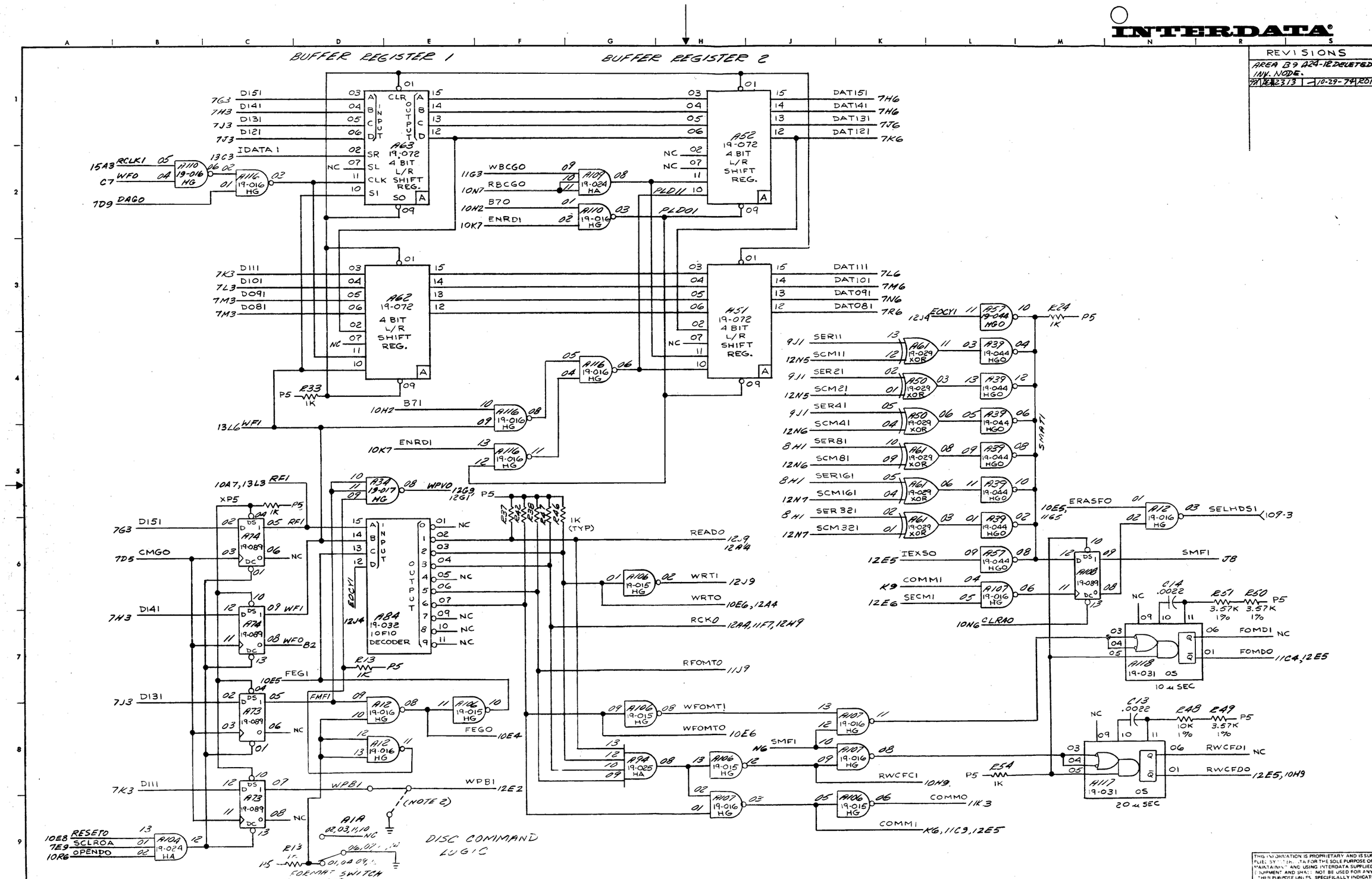
THIS INFORMATION IS PROPRIETARY AND IS SUPPLIED BY INTERDATA FOR THE SOLE PURPOSE OF MAINTAINING AND USING INTERDATA SUPPLIED EQUIPMENT AND SHALL NOT BE USED FOR ANY OTHER PURPOSE UNLESS SPECIFICALLY INDICATED.

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
40 MEGABYTE DISC

TASK NO. 03080
DWG NO. 02-359 D08
SHEET 8 OF 15

BRUNING 44-231 16042



REVISIONS

AREA B9 A24-12 DELETED INV. NODE.

9A 2313 10-29-74 R01

NOTES ALL APPARATUS ON THIS SHEET IS ON 35-532, DISC CONTROL.

2. FORMAT SWITCH FOR NORMAL MODE OF OPERATION.

2. TO INHIBIT THE WRITE WITH PROTECTION FUNCTION GROUND WPB1.

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC 40 MEGABYTE DISC

TASK NO 03080

DWG NO 02-3.59 R01 D08

SHEET 9 OF 15

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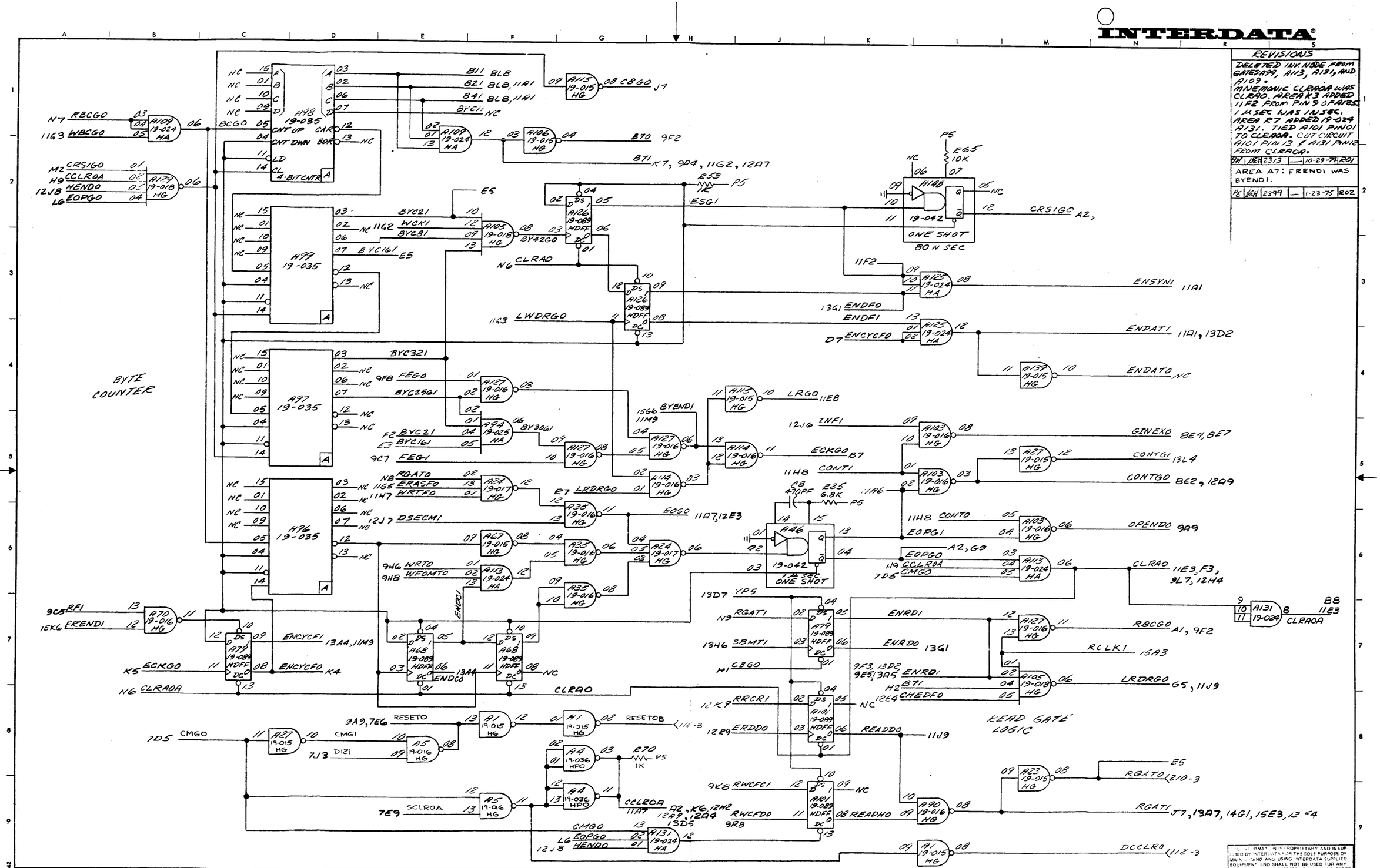
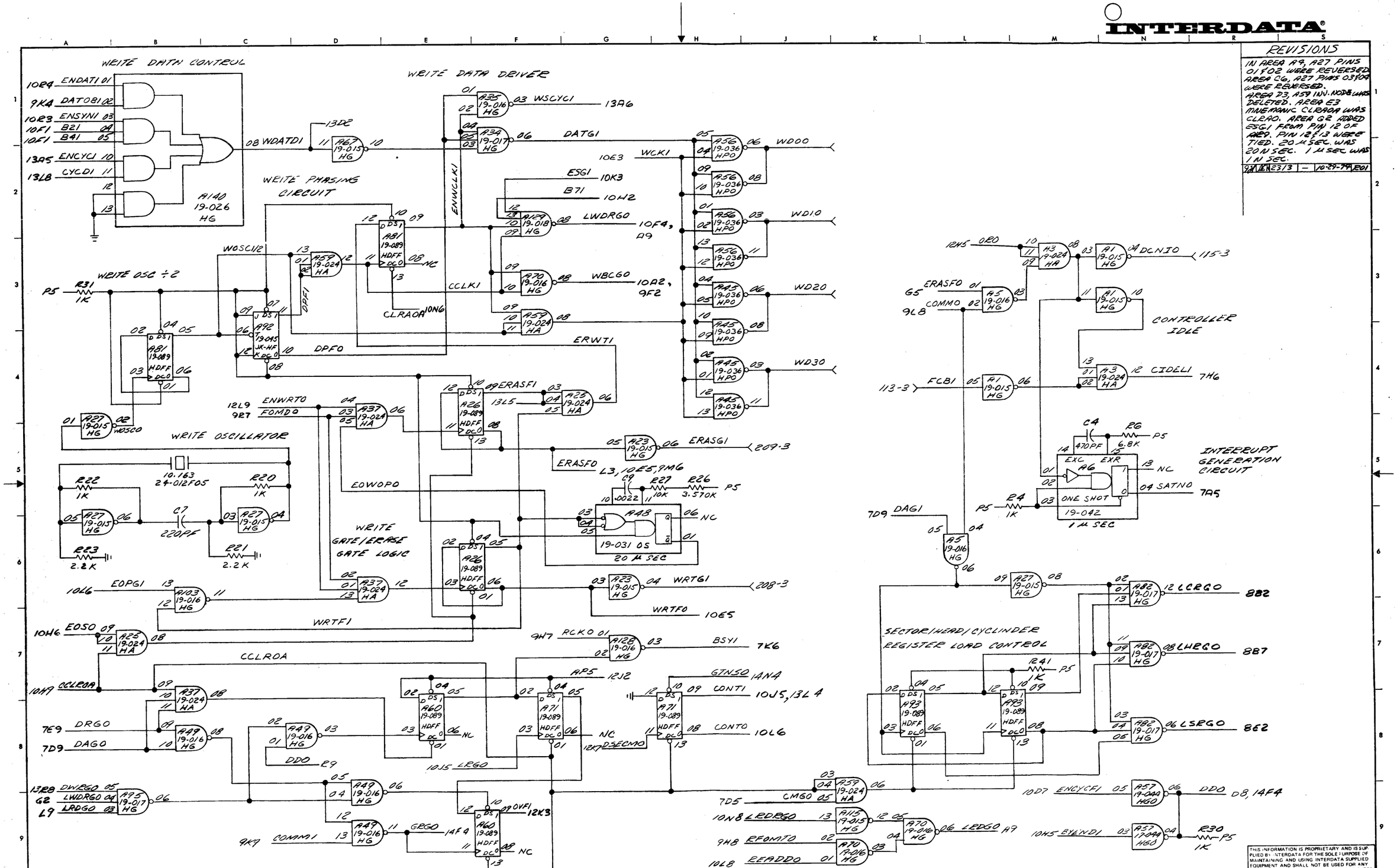
BRUNING 44-231 16042

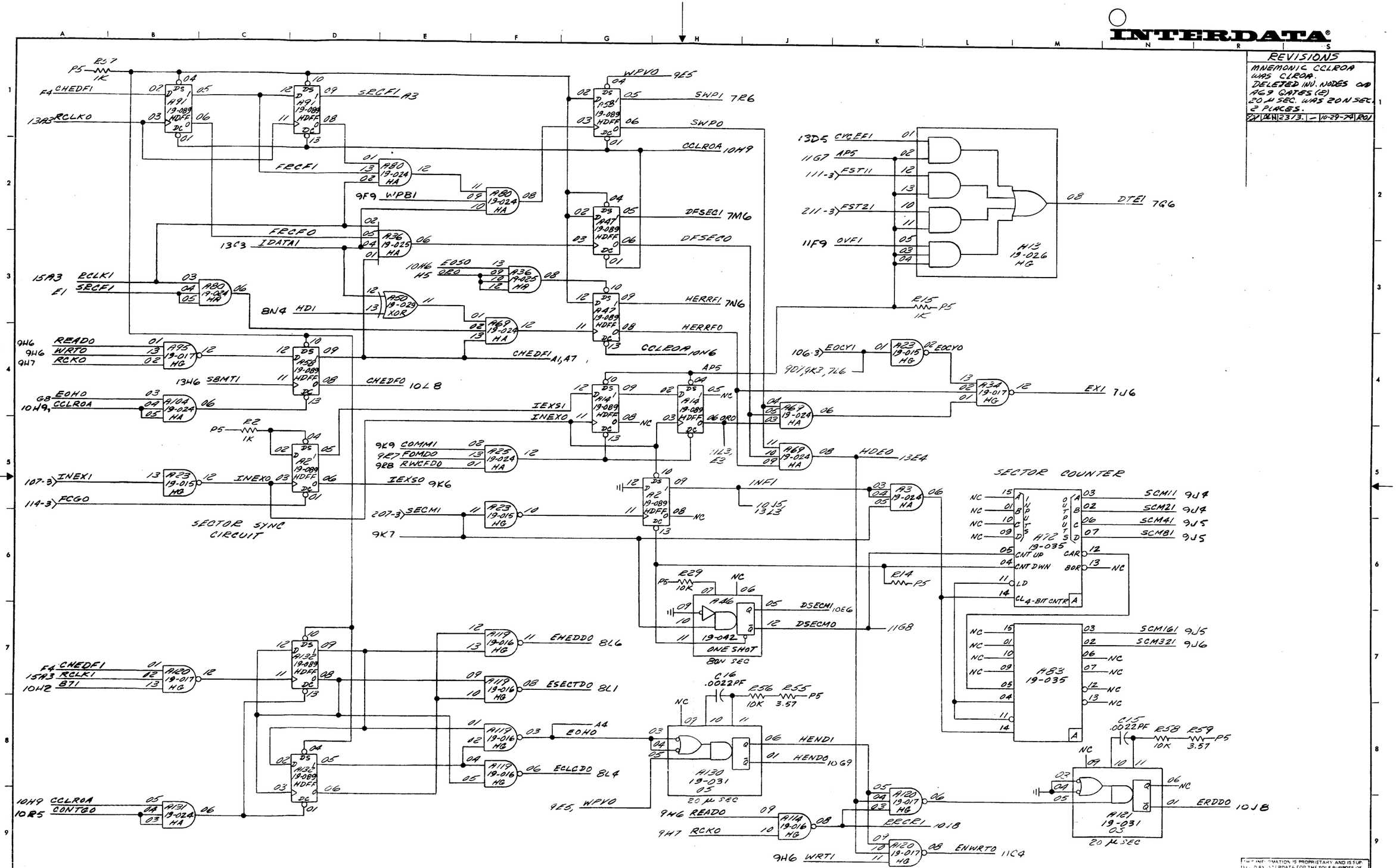

INTERDATA
REVISIONS
DELETED INV. NODE FROM GATES A99, A113, A131, AND A109. MNEMONIC CLRAOA WAS CLRAO. AREA K3 ADDED 11F2 FROM PIN 9 OF A125. 1 μSEC WAS 1 NSEC. AREA R7 ADDED 19-024 A131. TIED A101 PIN 01 TO CLRAOA. CUT CIRCUIT A101 PIN 13 & A131 PIN 12 FROM CLRAOA.
AREA A7: FRENDI WAS BYENDI.
BYTE COUNTER
READ GATE LOGIC
ONE SHOT
80 N SEC
1 μSEC ONE SHOT
4-BIT CNTR
CLRAOA
RBCGO
CRSIGO
CCLROA
HENDO
EOPGO
RFI
FRENDI
ENCYCF1
ENCYCFO
CLRAO
RESETO
RESETOB
CMGO
SCLROA
RGATO
RGATI
DCCLRO
ENSYNI
ENDATI
ENDATO
GINEXO
CONTGI
CONTGO
OPENDO
RCLKI
LRDRGO
CHEDFO
READDO
READHO
RWCFDO
RWCFCI
RRCRI
ERDDO
SBMTI
CBGO
YP5
RGATI
ENRDI
ENRDO
ENDFO
ENDFI
ENCYCFO
LWDRGO
CLRAO
BYENDI
ECKGO
CONTI
CONTO
EOPGI
EOPGO
CCLROA
CMGO
EOSO
LRDRGO
ENDCO
ENDCI
ESGI
CRSIGO
ENDFO
ENDFI
ENCYCFO
LRGO
INFI
ECKGO
CONTI
CONTO
EOPGI
EOPGO
CCLROA
CMGO
CLRAO
RBCGO
RCLKI
LRDRGO
RGATO
RGATI
DCCLRO
NOTES ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-532 DISC CONTROL.
NAME E. ROE
TITLE FUNCTIONAL SCHEMATIC 40 MEGABYTE DISC
TASK NO. 03080
DWG NO. 02-359 R02 D08
SHEET 10-15
BRUNING 44-231 16042



REVISIONS

IN AREA A9, A27 PINS 01 & 02 WERE REVERSED. AREA C6, A27 PINS 03 & 04 WERE REVERSED. AREA D3, A59 INV. NODE WAS DELETED. AREA E3 MNEMONIC CLRAOA WAS CLRAO. AREA G2 ADDED ESG1 FROM PIN 12 OF A29. PIN 12 & 13 WERE TIED. 20 μ SEC. WAS 20 N SEC. 1 μ SEC WAS 1 N SEC.

9/81 | 23/3 | – | 10-29-79 | R01



REVISIONS

MNEMONIC CCLROA WAS CLROA. DELETED INV. NODES ON A69 GATES (2) 20 μ SEC. WAS 20 N SEC. 2 PLACES.

5/7	DEN	2373.	—	10-29-74	R01

NOTES ALL APPARATUS ON THIS SHEET IS LOCATED ON 36-532 DISC CONTROL.

THIS INFORMATION IS PROPRIETARY AND IS SUPPLIED BY INTERDATA FOR THE SOLE PURPOSE OF MAINTAINING AND USING INTERDATA SUPPLIED EQUIPMENT AND SHALL NOT BE USED FOR ANY OTHER PURPOSE UNLESS SPECIFICALLY INDICATED.

NAME	TITLE	DATE
E. ROE	DRAFT	3-23-74
	CHK	
	ENGR	
	DIR ENG	

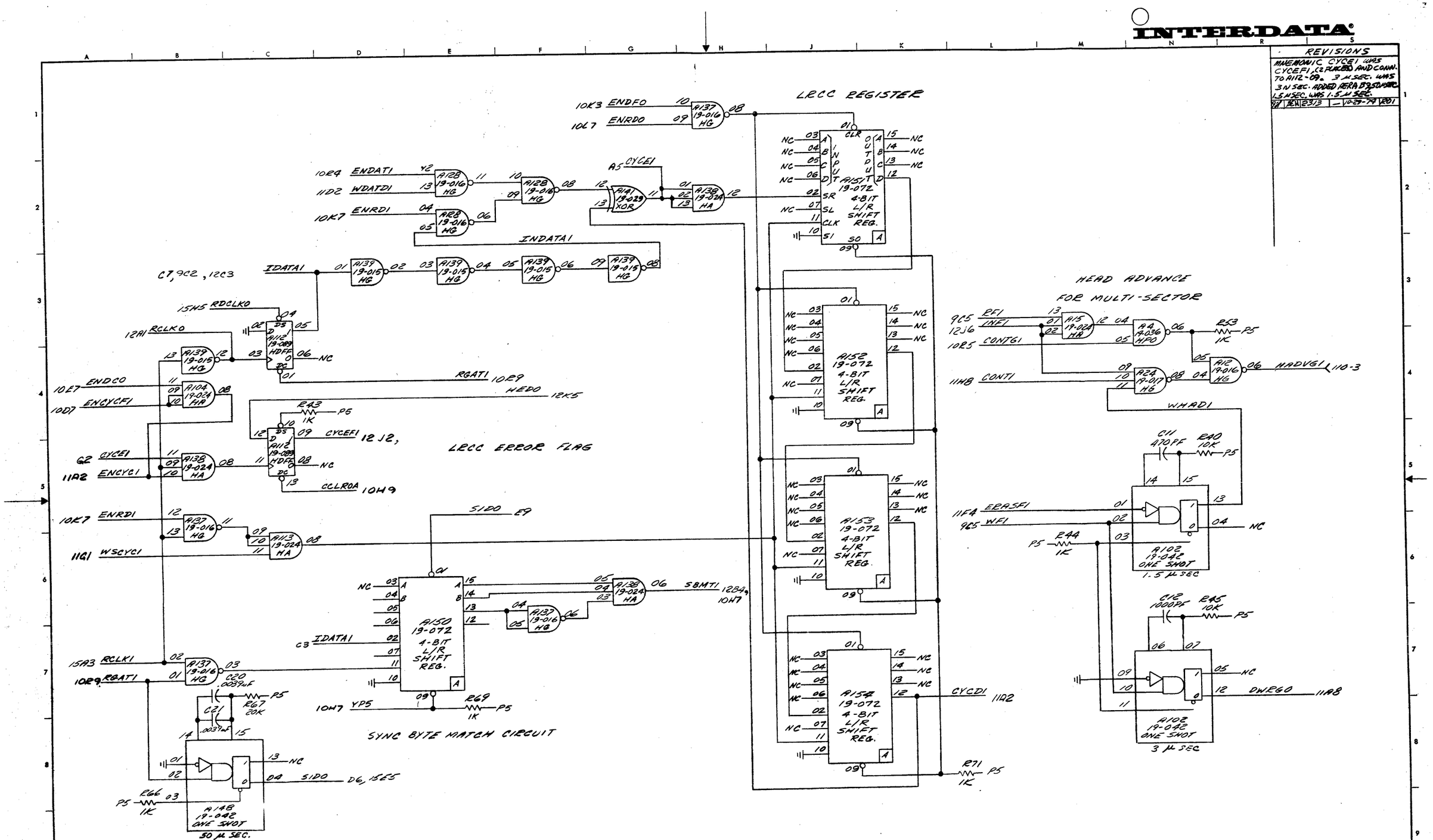
TITLE FUNCTIONAL SCHEMATIC 40 MEGABYTE DISC

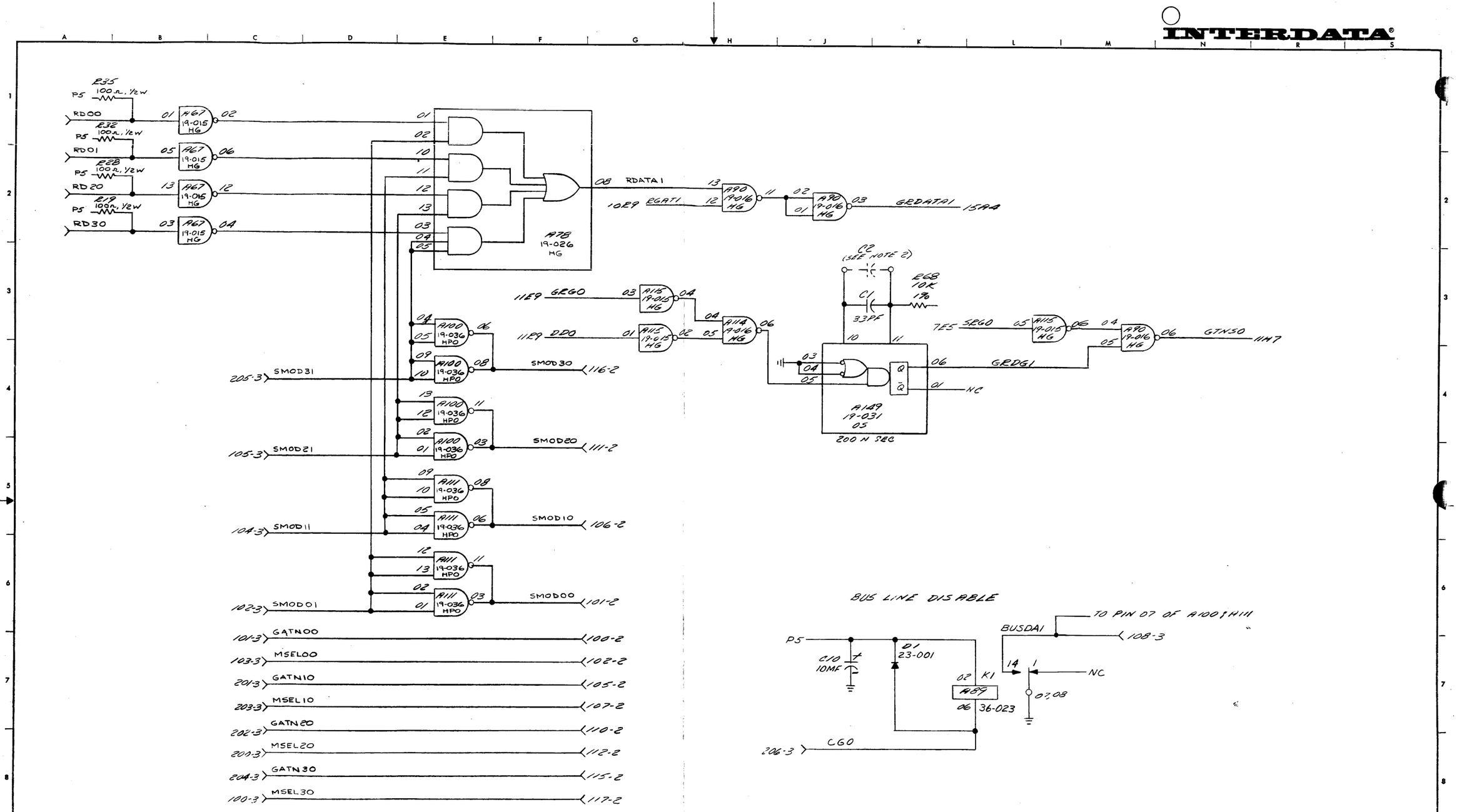
TASK NO 03080

DWG NO 02-359R01D08

SHEET 12 OF 15

BRUNING 44-231 16042


INTERDATA
REVISIONS
MNEMONIC CYCE1 WAS CYCEF1, (2 PLACES) AND CONN. TO A112-09. 3 μ SEC. WAS 3 N SEC. ADDED AERA B9 50 μ SEC. 1.5 μ SEC. WAS 1.5 μ SEC.
LRCC REGISTER
LRCC ERROR FLAG
SYNC BYTE MATCH CIRCUIT
HEAD ADVANCE FOR MULTI-SECTOR
A151 19-072 4-BIT L/R SHIFT REG.
A152 19-072 4-BIT L/R SHIFT REG.
A153 19-072 4-BIT L/R SHIFT REG.
A154 19-072 4-BIT L/R SHIFT REG.
A150 19-072 4-BIT L/R SHIFT REG.
A102 19-042 ONE SHOT 1.5 μ SEC
A102 19-042 ONE SHOT 3 μ SEC
A148 19-042 ONE SHOT 50 μ SEC.
A112 19-089 HDFF
A137 19-016 HG
A138 19-024 HA
A139 19-015 HG
A141 19-029 XOR
A128 19-016 HG
A104 19-024 HA
A113 19-024 HA
A15 19-024 HA
A4 19-036 HPO
A24 19-017 HG
A12 19-016 HG
10K3 ENDFO
10L7 ENRDO
10R4 ENDAT1
11D2 WDATD1
10K7 ENRD1
A5 CYCE1
INDATA1
C7, 9C2, 12C3
IDATA1
15H5 RDCLKO
12A1 RCLKO
10E7 ENDCO
10D7 ENCYCF1
RGAT1 10R9
HEDO 12K5
R43 1K
CYCEF1 12J2,
G2 CYCE1
11A2 ENCYC1
CCLROA 10H9
10K7 ENRD1
11G1 WSCYC1
SIDO E9
SBMT1 12B4, 10H7
C3 IDATA1
15A3 RCLK1
10R9 RGAT1
C20 .0039μF
C21 .0039μF
R67 20K
R69 1K
10H7 YP5
SIDO D6, 15E5
R66 1K
9C5 RF1
12J6 INF1
10R5 CONTG1
11H8 CONT1
R53 1K
HADVG1 110-3
WHAD1
C11 470PF
R40 10K
11F4 ERASF1
9C5 WF1
R44 1K
C12 1000PF
R45 10K
DWRGO 11A8
CYCD1 11A2
R71 1K
P5
NC
NOTES ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-532 DISC CONTROL.
THIS INFORMATION IS PROPRIETARY AND IS SUPPLIED BY INTERDATA FOR THE SOLE PURPOSE OF MAINTAINING AND USING INTERDATA SUPPLIED EQUIPMENT AND SHALL NOT BE USED FOR ANY OTHER PURPOSE UNLESS SPECIFICALLY INDICATED
NAME E. ROE
TITLE DRAFT CHK ENGR DIR ENG
DATE 3-23-74
TITLE FUNCTIONAL SCHEMATIC 40 MEGABYTE DISC
TASK NO. 03080
DWG NO. 02-359R01D08
SHEET 13 OF 15



NOTES ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-536 DISC CONTROL.
2. ADD 47PF CAPACITOR IN C2 POSITION WHEN DISC CONTROLLER IS INSTALLED ON MUX. BUS SWITCH

THIS INFORMATION IS PROPRIETARY AND IS SUPPLIED BY INTERDATA FOR THE SOLE PURPOSE OF MAINTAINING AND USING INTERDATA SUPPLIED EQUIPMENT AND SHALL NOT BE USED FOR ANY OTHER PURPOSE UNLESS SPECIFICALLY INDICATED.

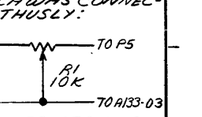
NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

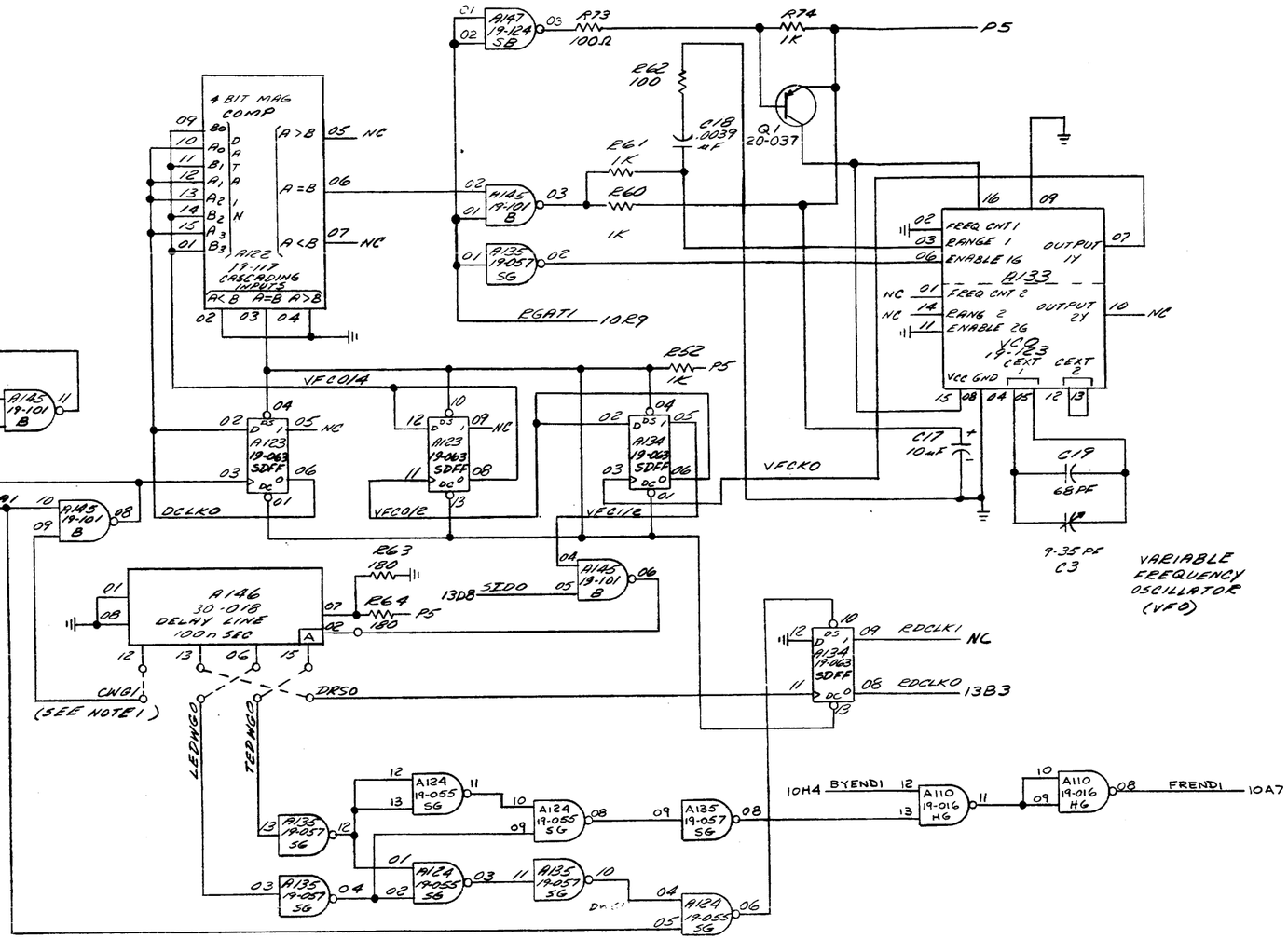
TITLE FUNCTIONAL SCHEMATIC 40 MEGABYTE DISC

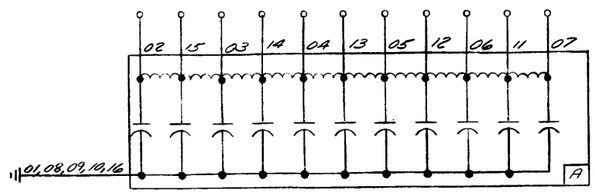
TASK NO. 03080 DWG NO. 02-359 D08 SHEET 14 OF 15

BRUNING 44-231 16042

INTERDATA®

REVISIONS			
AREA C2, A2 WAS B2, B2 WAS A2, A3 WAS B3, & B3 WAS A3.			
PK	EN 2313	—	10-29-74 R01
AREA D6, E6, F6, H6, & J6 ADDED A124-11, 12 & 13; A124-08, 09, & 10; A135-08, 09; A110-11, 12, & 13; AND A110-08, 09, & 10			
PE	RH 2399	—	1-23-75 R02
AREA J3 A133-12 & 13 WERE NOT CONN. A133-11 WAS SPEC'D N.C.			
PK	RC 2621	—	9-26-75 R03
AREA G1: DELETED R1, WHICH WAS CONNECTED THUSLY:  A147, R73, R74, Q1, & RELATED CIRCUITRY WERE NOT SPEC'D. A133-16 WAS TO P5.			
WS	# 2963 A	-	9-13-76 R04
ARE- E-1 ADDED PIN NO'S TO GATE A147.			
GS	AV 3089	-	6-30-77 R05





30-018
DELAY LINE

NOTES 1. THE STRAPPING FOR CWGI, LEDWGO, TEDWGO, & DRSO MAY HAVE TO ALTER TO OBTAIN CORRECT TIMING FOR VFO. (REFER TO 02-3594A1 FOR ADJUSTMENT PROCEDURE.

2. ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-532 DISC CONTROL.

NAME	TITLE	DATE
P. EDWARDS	DRAFT	4-17-74
	CHK	
	ENGR	
	D.E. ENG	

TITLE FUNCTIONAL SCHEMATIC 40 MEGABYTE DISC

TASK NO. 03080 DWG NO. 02-3579R05D08 SHEET OF 15-15

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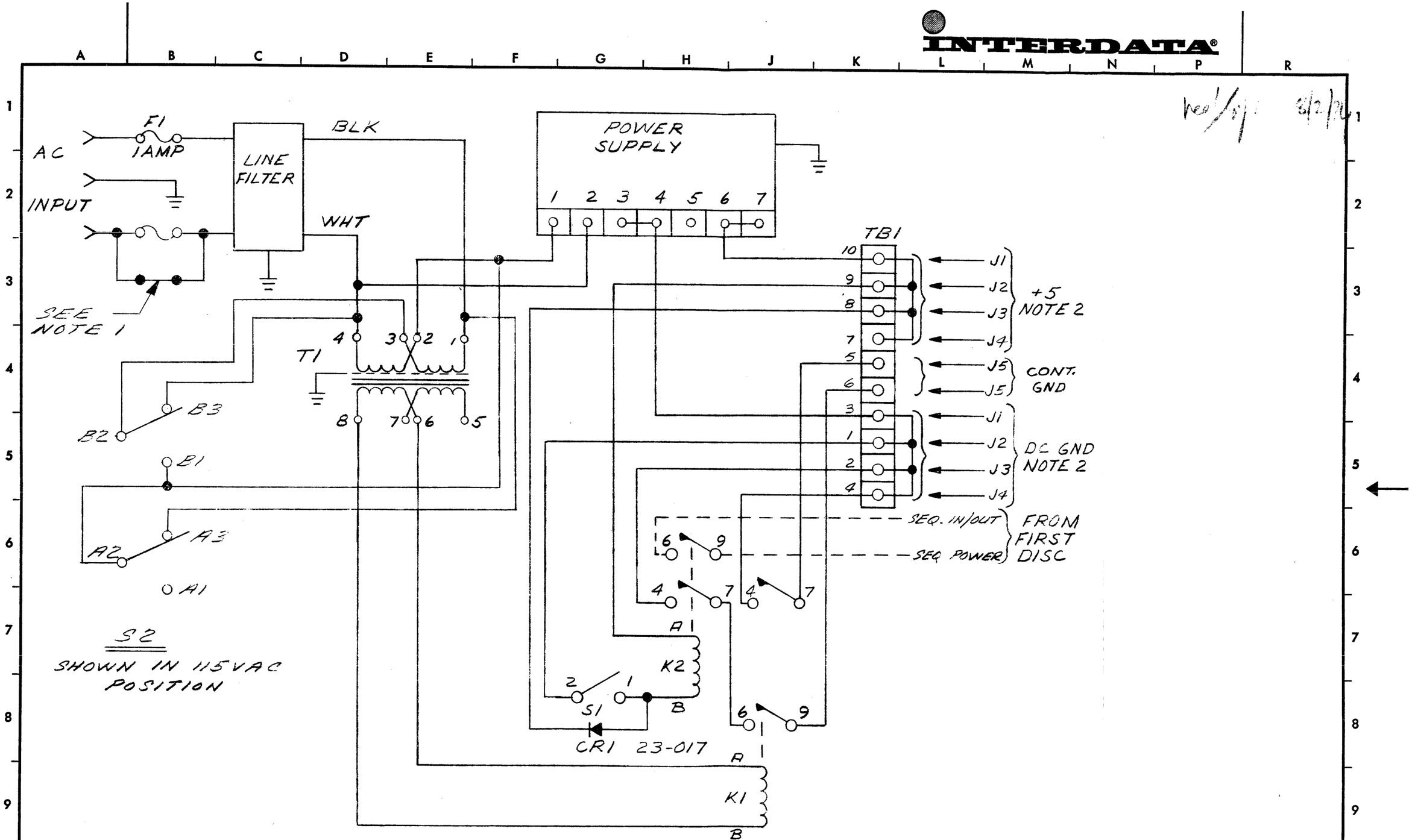
BRUNING 44-231 18042



NOTES
1. JUMPER REMOVED FOR 220 VOLT 2 PHASE OPERATION.
2. THE NUMBER OF CONNECTIONS TO +5 & GND DEPEND UPON THE NUMBER OF DISK FILE PER SYSTEM

NAME	TITLE	DATE
B. GRAY	DRAFT	2-27-74
R. CERO	CHK	[illegible]
[illegible]	ENG	6-26-74
H. ROSS	QC	7-1-74
J. P. [illegible]	MGR	7-8-74

TITLE FUNCTIONAL SCHEMATIC POWER CONTROL

TASK NO. 03080

DWG. NO. [illegible]-067 B08

SHEET 1 OF 1

D & W REPROGRAPHICS 40055-2

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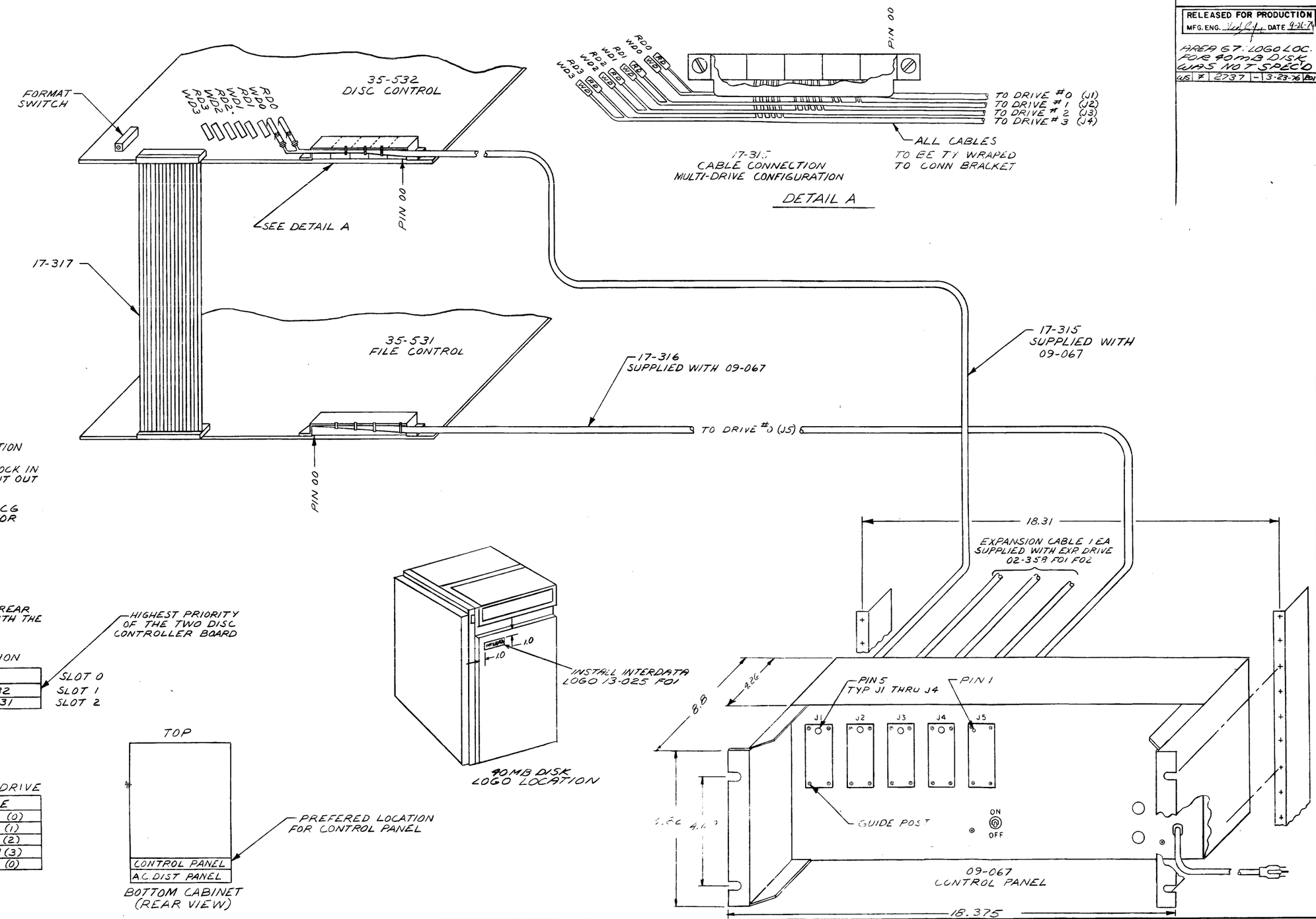
RELEASED FOR PRODUCTION
MFG. ENG. [signature] DATE 9-26-74

AREA 67: LOGO LOC. FOR 40MB DISK WAS NOT SPEC'D

WS	#	2737	-	3-23-76	R01



EXP. CABLE INSTALLATION

1. MOUNT CONNECTOR BLOCK IN DESIRED CONNECTOR CUT OUT J2, J3 OR J4
2. CONNECT THE P5 & DCG LEAD PER CONNECTOR AS FOLLOWS:
   - J2 - P5 TO TB1-9, DCG TO TB1-1
   - J3 - P5 TO TB1-8, DCG TO TB1-2
   - J4 - P5 TO TB1-7, DCG TO TB1-4
3. SECURE CABLE ON REAR OF PANEL 09-067 WITH THE PROVIDED TY WRAP

TYPICAL INSTALLATION

SELECTOR CHANNEL	
DISC CONTROL 35-532	SLOT 0
FILE CONTROL 35-531	SLOT 1
	SLOT 2

CABLE CONNECT TO DISC DRIVE

	FROM	TO FILE
DC	J1	FIRST (0)
DC	J2	SECOND (1)
DC	J3	THIRD (2)
DC	J4	FOURTH (3)
SIGNAL	J5	FIRST (0)

NOTES

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NAME	TITLE	DATE
B. GRAY	DRAFT	7-18-74
R. CERO	CHK	9-26-74
R. SAGER	ENGR	9-26-74
H. ROSS	QC	9-26-74
C. WALKER	PROD	9-26-74

TITLE INFORMATION CONTROLLER INSTALLATION

TASK NO. 03080 SHEET 1 OF 1

DWG NO. 02-357 R01 D12

BRUNING 44-231 16042

REVISIONS			
RELEASED FOR PRODUCTION MFG. ENG. [illegible] DATE 9/16/74			
ADDED ITEMS 73, 74 & STRAPS 1-6. NEAR A49 R27 & C9 WERE REVERSED. NEAR A26 R68 & C62 WERE REVERSED. NEAR A26 ADDED R37.			
RE WM 2318	-	10-28-74	R01
ADDED STRAPS 5 & 6, 47			
RE WM 2399	-	1-23-75	R02
ADDED R36, ITEM 40, NEAR A32. C31, C61 WERE ITEM 40.			
DR WM 2810	-	12-5-75	R03
R24, ITEM 40, ABOVE A33 WAS NOT SHOWN			
RE WM 2550	-	7-16-75	R04
REVISED CIRCUITRY TO REFLECT NEW COPPER, Q1, R33, R74 & R147 WERE NOT SHOWN. DELETED R1 NEAR R33, WHICH WAS P10K, VAR. RESISTOR, ITEM 70.			
RE [illegible]	-	9-12-75	R05
JC CABLE A13S WAS SHOWN AS A3S. RUN TO GND R74 ITEM 40 WAS SHOWN INCORRECT. COPPER RUN FROM R73 ITEM 39 TO R74 ITEM 40 WAS NOT SHOWN. COPPER RUN FROM C3 TO C19 ITEM 55 WAS NOT SHOWN			
05 WM 3089	-	6-30-77	R06

NOTES:

1. APPLY DOUBLE-BACKED ADHESIVE TAPE, 37-110 TO BOARD SURFACE UNDER CRYSTAL, ITEM 63 ON TOP OF TAPE APPROX. AS SHOWN. DO NOT ALLOW CRYSTAL TO COME IN CONTACT WITH BOARD.
2. ADD 47 PF CAPACITOR IN C2 POSITION WHEN DISC CONTROLLER IS INSTALLED ON I/O BUS SWITCH, NOT REQUIRED AT THIS ASSY.
3. STIFFENER BAR (ITEM 2) TO BE SOLDERED TO GND BUS AT TWO (2) END POINTS & CENTER POINT.
4. CONTACTS CLOSEST TO EDGE OF BOARD TO BE BENT INWARD PRIOR TO SOLDERING.

DETAIL A

DETAIL B

PARTIAL VIEW A-A

LAST STRAP IS NUMBER 7.

COMPONENT	REF DESIGNATION
TRANSISTOR	Q1
CRYSTAL	Y1
CAPACITOR	C1-C32
RESISTOR	R2-R74
INT. CKT.	A1-A6, A11-A33, A37-A39, A43, A47-A49, A135, A137
C-RIB	

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D. EDWARDS	DRAFT	8-22-74	ASSEMBLY DISC CONTROL
M. MATTER	CNC	9-24-74	
E. LACER	QUC	9-24-74	
L. BARTLETT	MAT	9-24-74	
M. ROSS	Q.C	9-24-74	SIZE C DRAWING NO. 5312 R06 803 SHEET 1-1

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