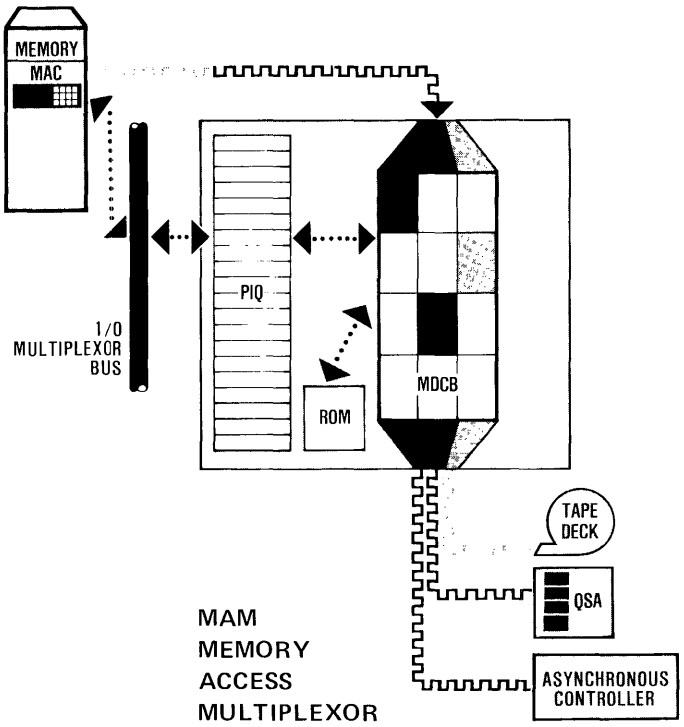
INTERDATA®

COMMUNICATIONS



MAM Memory Access Multiplexor

PRODUCT DESCRIPTION

Interdata's Memory Access Multiplexor (MAM) enhances and simplifies the use of telephone utilities for high speed data transmission.

Part of Interdata's array of advanced data communications aids, MAM interfaces directly to memory, thus relieving the user of handling data on a programmed character basis.

MAM provides a Direct Memory Access (DMA) block-transfer facility for up to 63 half-duplex devices or 31 full-duplex devices. MAM interfaces with the DMA bus of the 32-bit processors, and the I/O bus and generates a private bus of its own called the MAM bus. A typical configuration is shown.

MAM's full duplex DMA capability is a significant advance over previous DMA capability of a single device operating half duplex. Again, MAM achieves system flexibility and configurat on economy.

Typically, MAM is used with communication interfaces such as the Programmable Asynchronous Line Adapter (PASLA) and the Quad Synchronous Adapter (QSA).

Other peripherals that interrupt on the character/half-word basis, such as A/D units, mag tape controllers, printers, and card equipment, can be used.

For data management, MAM automatically changes or switches buffer locations.

For communications, MAM can be instructed to recognize special binary synchronous character sequences and, on reception, alert the interrupting mechanism and the user task. This automatic recognition frees the user from reviewing input character streams and allows implementation of simpler data handling programs.

FEATURES

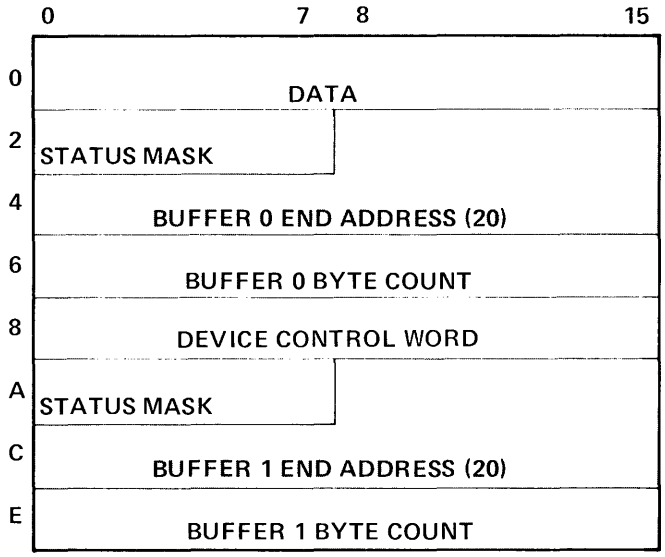
- 63 half duplex addresses or 31 full duplex addresses
- Data Chaining or Buffer Switching on Device Addresses
- PIQ-255-interrupt queue
- Special Character Protocol Recognition
- Maximum Throughput of 195K Bytes (375 Bytes/sec halfword devices)
- Compact Board Packaging

FUNCTIONAL CHARACTERISTICS

MAM provides multiplexing of character interrupting controllers by incorporating 512 x 16 bits of random access memory (RAM) control. RAM allows the user to dynamically store and modify buffer-address and word-count information contained in the Device Control Blocks (MDCB) used in conjunction with each address.

Each data transfer over the MAM bus requires information listed in MDCB, including the end address of the first and second buffers, each buffer size, status, and a device control word. As the first buffer completes filling, MAM automatically switches data flow to the second buffer and an interrupt is posted in the Processor Interrupt Queue (PIQ). As the data continue to flow into the second buffer, the user must update the information in the MDCB relative to the first buffer, such as status, byte count, and address. Through similar repetitive update procedures, data can be stored throughout all of memory.

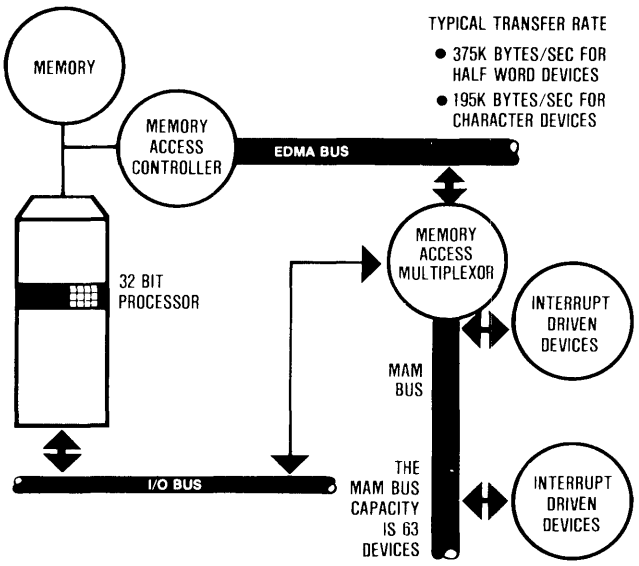
MAM DEVICE CONTROL BLOCK



PROCESSOR INTERRUPT QUEUE

The Processor Interrupt Queue (PIQ) is the MAM interrupt mechanism; it interrupts the processor when MAM has completed or sensed a specific function. MAM continues to generate interrupts to the processor as long as the PIQ has entries. The PIQ is 255 x 16 bit RAM. When an interrupt occurs, MAM loads a halfword in PIQ. The upper bytes are status codes and the lower bytes indicate the device address. After a data transfer has been initiated interrupts are posted in the PIQ when the following events occur:

- Device Status Error
- Buffer Full
- End-of-Block Transfer
- Error Condition
- Special Character Sequence Received



MAM'S POSITION IN THE SYSTEM

When an interrupt occurs, the automatic interrupt service mechanism of the processor provides the MAM address and status in registers two and three of the appropriate register set in the processor. The processor must then read the halfword entry from the MAM PIQ.

SPECIAL CHARACTER RECOGNITION

MAM also incorporates a 512 x 8 bit ROM for special character recognition. The various binary synchronous characters, shown below in predefined combinations cause interrupts and effect mode changes or terminate operation. MAM can accommodate a maximum of four special character codes: EBCDIC, USASCII, Six Bit Transcode and one customer defined. The particular protocol is selected by two bits in the device control word of the MDCB.

SPECIAL CHARACTERS				
	DEL	ETB	SOH	
NAK	ENQ	ETX	STX	STOP
	EOT	ITB	SYN	

MAM throughput typically is 195K characters per second when used with 750ns memory. As many as seven MAM's can be installed on a system. Care must be taken in configurating systems because of the possible variations and system throughput.

The Interdata Systems Group is responsible for supporting MAM system integration and also responsible for supplying all MAM pricing information.

PHYSICAL CONFIGURATION

The MAM consists of two 15-inch boards installed in the processor chassis in specific locations.

INTERDATA PART NUMBER

M47-010 Memory Access Multiplexor
(Quoted by Systems Group)

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