I R O N I C S

IV-1624 8-PORT INTELLIGENT
SERIAL I/O CARD

U s e r G u i d e

IRONICS
Incorporated

IV-1624 8-PORT INTELLIGENT SERIAL I/O CARD

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This manual has been carefully checked for accuracy. We can, however, assume no responsibility for errors, nor can we assume any liability which arises from the use or application of this board.

As part of our continuing effort to improve the quality of the Ironics VMEbus productivity series, we solicit comments, criticism and suggestions of our customers. We would greatly appreciate your taking the time to provide us with any feedback. Your comments, positive or negative, about the manual, hardware or software are especially welcome. Send your remarks to:

Ironics Incorporated
Quality Assurance
798 Cascadilla Street
Ithaca, New York 14850

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0. READ THIS BEFORE UNPACKING

Welcome to the family of **IRONICS** users. To expedite the integration of your card into a target system, the board has been shipped in a standard configuration. We hope that you will follow the UNPACKING, INSPECTION, and FUNCTIONAL CHECKOUT procedures outlined in chapter 2 before attempting your own configuration.

NOTE:

The preliminary functional tests outlined in section entitled "FUNCTIONAL CHECKOUT" require a specific board configuration. Your new board has been configured for test procedures. Do not alter jumper or shunt configuration prior to testing!

1. GENERAL INFORMATION

1.1 History of the IRONICS multiprocessing family

Members of the multiprocessing family represent the second generation of **IRONICS** high-performance, cost-effective CPU and intelligent I/O boards. The members of this family include:

[1] the IV-1601 VMXCPU board
[2] the IV-1602 Single Board Computer
[3] the IV-1624 8-port Intelligent Serial I/O board
[4] the IV-3201 68020 VME/VMX CPU board
[5] the IV-3273 System Controller board

All members of this family conform to the Eurocard dual-height form factor without compromising the high performance levels pioneered by the IV-1600 System Foundation Module. This performance package has been achieved by coupling the IV-1600's 68000/VME architecture to designs with higher board density and with the use of chips with greater levels of internal integration.

1.2 Philosophy of Design: Multiprocessing Engines

IRONICS has created a family of products designed to function as "multiprocessing engines". This implies:

[1] that all family boards are designed to function and communicate with other CPU and intelligent I/O cards meeting VME (revision C) specifications;
[2] that each board acts as an "engine": that is, each is **dedicated** to a range of system control and I/O functions for the VME multiprocessing environment.

These functions provide the basis for a complete, fully-integrated, multiprocessing system. The family architecture addresses specific needs of the multiprocessing environment, including:

[1] the need for a diverse range of system tools
[2] the need for maximum processing speed
[3] the need for large amounts of local RAM, available to other processors with minimum latency
[4] the need for efficient data transfer mechanisms

[5] the need for interprocessor communications tools (i.e., semaphoring tools and interrupt-on-access ("mailbox") interrupts)

Each of these needs is addressed in more detail in the following section.

1.3 System performance considerations

1.3.1 Functional diversity

Tables 1.1 and 1.2 show a comparison of major features available on **IRONICS** multiprocessing family boards. In spite of the functional diversity of the individual boards, all multiprocessing family members share a common, modular design which will, we believe, once mastered, reduce the overall time and effort required to integrate cards into a multiple processor system.

1.3.2 CPU performance

Multiprocessing members use either the 68010 CPU (IV-1601, IV-1602, and IV-1624) operating at 10 or 12.5 MHz, or the 68020 CPU (IV-3201) operating at 12.5 or 16 MHz.

1.3.3 Memory

The **IRONICS** multiprocessing architecture includes large amounts of local, no wait-state, dead-lock protected shared (dual-ported) memory. The large local memory ensures that each processor within the multiple processor environment executes at close to full speed. Up to 1 Mbyte of wait-state free memory can be provided on the IV-1601, IV-1602 and IV-3201 with a 512K RAM daughter board. Additional wait-state free memory can be provided on boards possessing a VMXbus interface (the IV-1601 and IV-3201 CPU boards). (Note: the RAM chips required to obtain full speed operation over the VMXbus or VMEbus are faster than those required to obtain full speed operation of local RAM.)

A single, large local RAM is the least expensive path to high performance except for very large systems requiring multiple megabytes of RAM, which benefit from a cache. Note also that systems in which the CPUs are required to fetch instructions over the VMEbus typically run with two or three wait states. When more than two such CPUs are installed in the system, additional wait states are required because their VMEbus bandwidth is almost entirely consumed by instruction fetches. Thus, large local RAMs are essential to multiprocessing.

The **IRONICS** multiprocessing architecture provides a large local memory for each processor. As a result, each board may execute instruction fetches out of its own local memory, virtually eliminating the need for trans-VMEbus instruction fetching. This allows high bandwidth peripherals (local area networks, SMD drives, camera input devices, etc.) to be added to the system without degrading individual CPU performance.

1.3.4 Data transfer mechanisms

The performance of the multiprocessing system described above is optimized by improving the efficiency of the basic data transfer mechanism. This involves increasing the data pathwidth, reducing the amount of time required to obtain access to the data pathway, and finally, by forcing the bus master to vacate the bus rapidly once a transfer has completed.

1.3.4.1 Interprocessor communication pathways

The data transfer mechanism for interprocessor communication is a 32-bit data path to dual-ported static RAM (available on the IV-1624 8-port Intelligent Serial I/O board and IV-1601 CPU). The path width and rapid access time (less than 120 ns) provide a data rate that is four to twelve times faster than that available with dual-ported dynamic RAM with a 16-bit data pathway.

1.3.4.2 Dual port access time

The static RAM access time is further reduced because of its separation from the local CPU, isolated from the CPU by a set of buffers. Accesses to the static RAM through its dual-port interface do not slow the local CPU unless the CPU is, simultaneously, trying to access the local static RAM. In addition, this memory is equipped with a fast, asynchronous arbiter which doesn't require that local CPU cycles be retried in order to resolve a deadlock.

NOTE:

This is not the case with dynamic RAM dual port arbiters such as that of the IV-1601 VMXCPU or that of other manufacturer's CPU boards. For a more detailed description of dynamic RAM dual-port lockout, see chapter 3.

1.3.4.3 Rapid strobe deassertion

In a multiprocessing environment, the speed with which a bus master vacates the bus after completing a transaction is as important as the slave's access time in determining overall system performance. All members of the **IRONICS** multiprocessing family utilize a feature called "rapid strobe deassertion" on VMEbus write cycles. This feature gets them off the bus almost two CPU clock cycles faster than is characteristic of CPU boards without rapid strobe deassertion. This feature also allows more rapid interprocessor message interrupt/response time. More specifically: processors communicate by writing to another's MAILBOX RAM location, then poll their own local dual-ported memory for the response. Thus, the majority of VMEbus traffic of this type are write cycles which require half as much bandwidth as read cycles. Fast strobe deassertion also frees the dual-port memory for use by its local master sooner.

1.3.5 Interprocessor communication primitives

A major concern within the multiprocessing environment is the integrity of interprocessor communication. In addition to the obvious advantages of having a fast message/response cycle, the system which can insure the integrity of semaphores sent from processor to processor greatly reduces the probability of system failure and loss of data. The **IRONICS** architecture has deadlock-protected, shared memory, interrupt mechanisms, and guaranteed indivisibility of semaphore operations. As part of the communications scheme, a mailbox interrupt (MBOXIRQ*) is issued to the local processor when a message or semaphore is written to the upper 256 bytes of static RAM through the dual-port pathway (note: the interrupt occurs only when one or more of the upper 256 bytes of static RAM are written to, and only on a write cycle). This comprises a complete set of interprocessor communications primitives which are required to take full advantage of multiple processors.

1.4 **IRONICS** multiprocessing family members

The following sections provide a brief overview of individual family members. Block diagrams of each product are shown in figures 1-1 through 1-5. To obtain technical information, contact an IRONICS customer service representative.

1.4.1 The IV-1601 VMXCPU board: the multiprocessing engine

The 68010-powered IV-1601 provides the functionality of a "multiprocessing engine"; that is, a auxilary CPU with the intelligence and resources distribute and facilitate system tasks. Its self-contained resources (e.g., floating point processor) equip it for number crunching applications. Its VMEbus interface allows it to offload I/O control tasks from a main CPU: it simply uses the VMEbus to control "dumb" VMEbus I/O cards and to communicate with the master CPU. With the VMXbus, a user can quickly implement a two to six card intelligent I/O system using the VMXbus interface to I/O controllers.

1.4.2 The IV-1602 Single Board Computer

The IV-1602 VMEbus Single Board Computer provides all the self-contained resources for a central CPU. The IV-1602 is a VMEbus CPU board with optional memory management, optional floating point processor, large amounts of onboard, dynamic, wait-state free, dual-ported RAM (expandable to 1 Megabyte with a RAM daughter board). In contrast to its sibling, the IV-1601 VMXCPU, the IV-1602 has serial ports to accomodate a system console, and supports system controller functions. Its on board functions allow it to stand alone as a single-board computer. The IV-1602 architecture also includes a SCSI bus interface for connection to mass storage peripherals.

1.4.3 The IV-1624 8-port Intelligent Serial I/O board

The IV-1624 8-Port Intelligent Serial I/O card retains many of the features as well as the modularity of design of other members of the Ironics multiprocessing family. The IV-1624 card has, in addition to onboard dual-ported static and dynamic RAM, an optional four channel DMA and 8 full-duplex multi-protocol serial I/O channels. It is ideally suited as a communications processor for UNIX systems, especially 68020-based multi-user systems. The DMA controller option allows transfers on up to 6 channels at up to 9600 baud asynchronously plus two channels at 1 Mbaud synchronously. A downloadable driver for multichannel asynchronous operation is currently in development. The IV-1624 is user-programmable for this and other protocols. Complete electrical and physical specifications are included in Appendix A.

1.4.4 IV-3201 68020 VME/VMX CPU board

The IV-3201 68020 VME/VMX CPU is the 32-bit analog of the IV-1601 VMX CPU. It provides up to 1 Megabyte of local, wait-state free RAM. Powered by a 16 or 12.5 MHz 68020 CPU, and supported the large local, dual-ported memory, the IV-3201 achieves superior performance without the cost of a cache. In addition, it has two independent 32-bit bus interfaces. This allows expansion of tightly coupled resources via the VMXbus (private) bus and interprocesssor communication and global resource utilization via the VMEbus. The IV-3201 VME/VMX shares all of the interprocessor
communications primitives of its sibling, the IV-1601, including: bus interrupter and interrupt handler modules, mailbox interrupts, indivisible read-modify-write cycles, etc.

1.4.5 IV-3273 System Controller board

The IV-3273 is a non-processor board which provides all VMEbus system controller functions plus additional functions

needed to complete a system with the IV-1601, IV-3201, IV-1602, and/or IV-1624 boards. Its four level, parallel/round-robin arbiter design is fully asynchronous for optimum speed, yet fully protected from metastable states. Its SCSI bus interface supports full bus protocol including host to host communications and supports over 1 million transfers per second. The SCSI bus interface is DMA-driven and utilizes 16 or 32 bit VMEbus data transfers. The parallel Centronics printer interface is interrupt-driven. The IV-3273 also includes a clock/calendar chip with battery backup, a power monitor module, system clock, system reset generator and two programmable timers.

TABLE 1-1. IRONICS multiprocessing family feature comparison

FEATURE	PRODUCT				
	1601	1602	1624	3201	3273
CPU:					
68010 10 MHz	+	+	+	-	-
12.5 MHz	+	+	+	-	-
68020 12.5 MHz	-	-	-	+	-
16 MHz	-	-	-	+	-
DRAM*: 64K	-	-	+	-	-
128K	+	+	-	-	-
512K	+	+	-	+	-
1 Mbyte	+	+	-	+	-
SRAM*: 16K	+	-	+	-	-
64K	+	-	+	-	-
EPROM: 8Kx8	+	+	+	+	-
16Kx8	+	+	+	+	-
32Kx8	+	+	+	+	-
64Kx8	+	+	+	+	-
128Kx8	+	+	+	+	-
INTERRUPTER:	+	+	+	+	+
INTERRUPT HANDLER:	+	+	+	+	-
FPP: NS32081	+	+	-	-	-
MC68881	-	-	-	+	-
VME INTERFACE:					
master	+	+	+	+	+
slave	+	+	+	+	+
VMX INTERFACE	+	-	-	+	-

* All RAM dual-ported

(table continued on next page)

TABLE 1-2. IRONICS multiprocessing family feature comparison (continued)

FEATURE	PRODUCT				
	1601	1602	1624	3201	3273
SERIAL I/O:					
MC68681	-	+	-	-	+
Z8530	-	-	+	-	-
PARALLEL I/O:					
SCN68230	-	+	-	-	+
COUNTER/TIMER:					
MC68B40	+	-	+	-	-
CLOCK/CALENDAR	-	+	-	-	+
MMU: MC68851	-	+	-	+	-
ARBITER:					
MC68451 round-robin/parallel	-	-	-	-	+
single-level	-	+	-	-	-
SYSCLOCK GENERATOR:	-	+	-	-	+
SCSI INTERFACE					
NCR5380	-	+	-	-	+
DMA: MC68450	-	-	+	-	-
MC68430	-	-	-	-	+
POWER FAIL MONITOR:	-	-	-	-	+
CENTRONICS PORT:	-	+	-	-	+

IRONICS MULTIPROCESSING FAMILY BLOCK DIAGRAMS

Figure 1-1. IV-1601 VMXCPU block diagram

(see drawing on opposite page)

IV-1601 BLOCK DIAGRAM

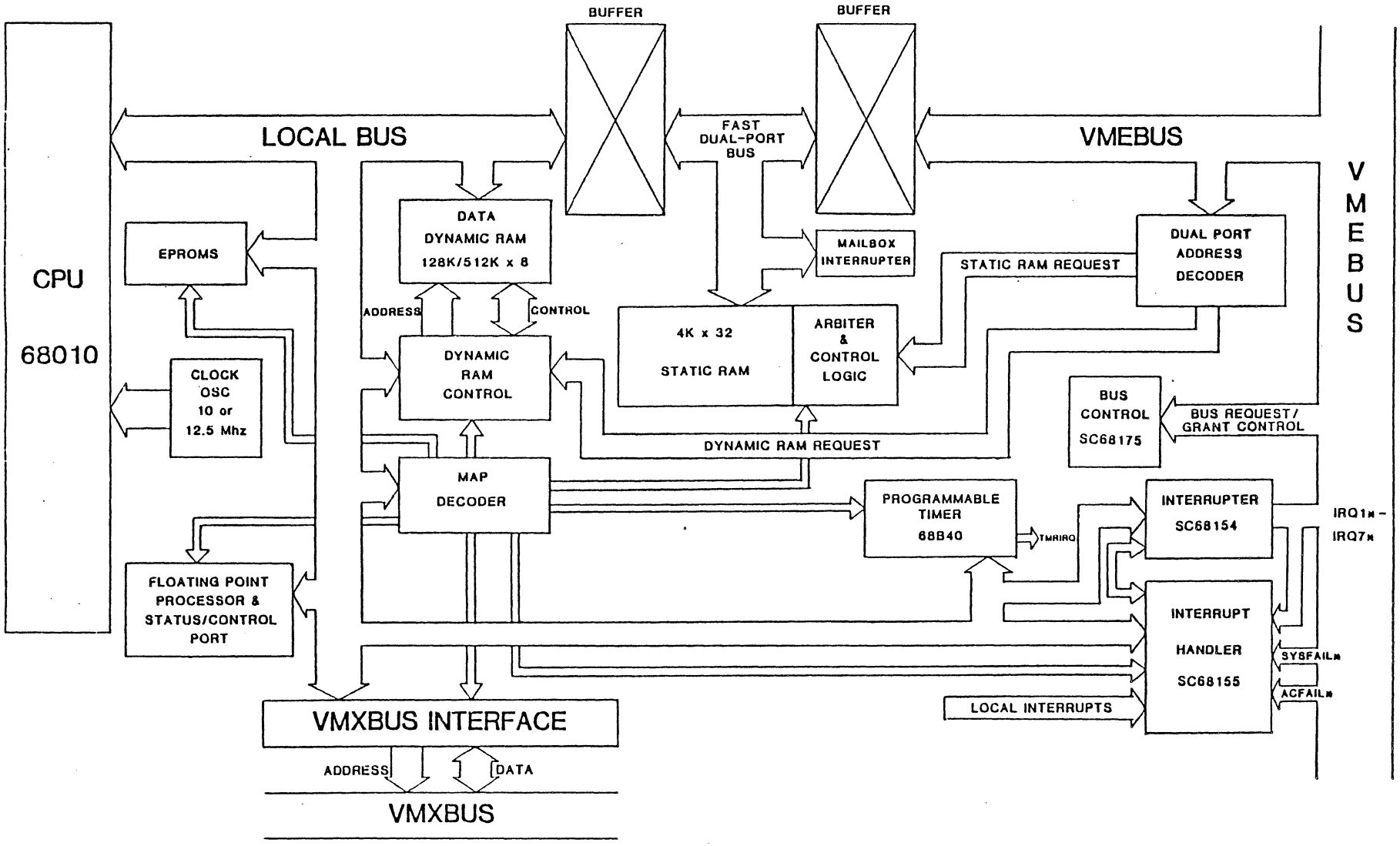


Figure 1-2. IV-1602 CPU block diagram

(see drawing on opposite page)

IV-1602 SINGLE BOARD COMPUTER

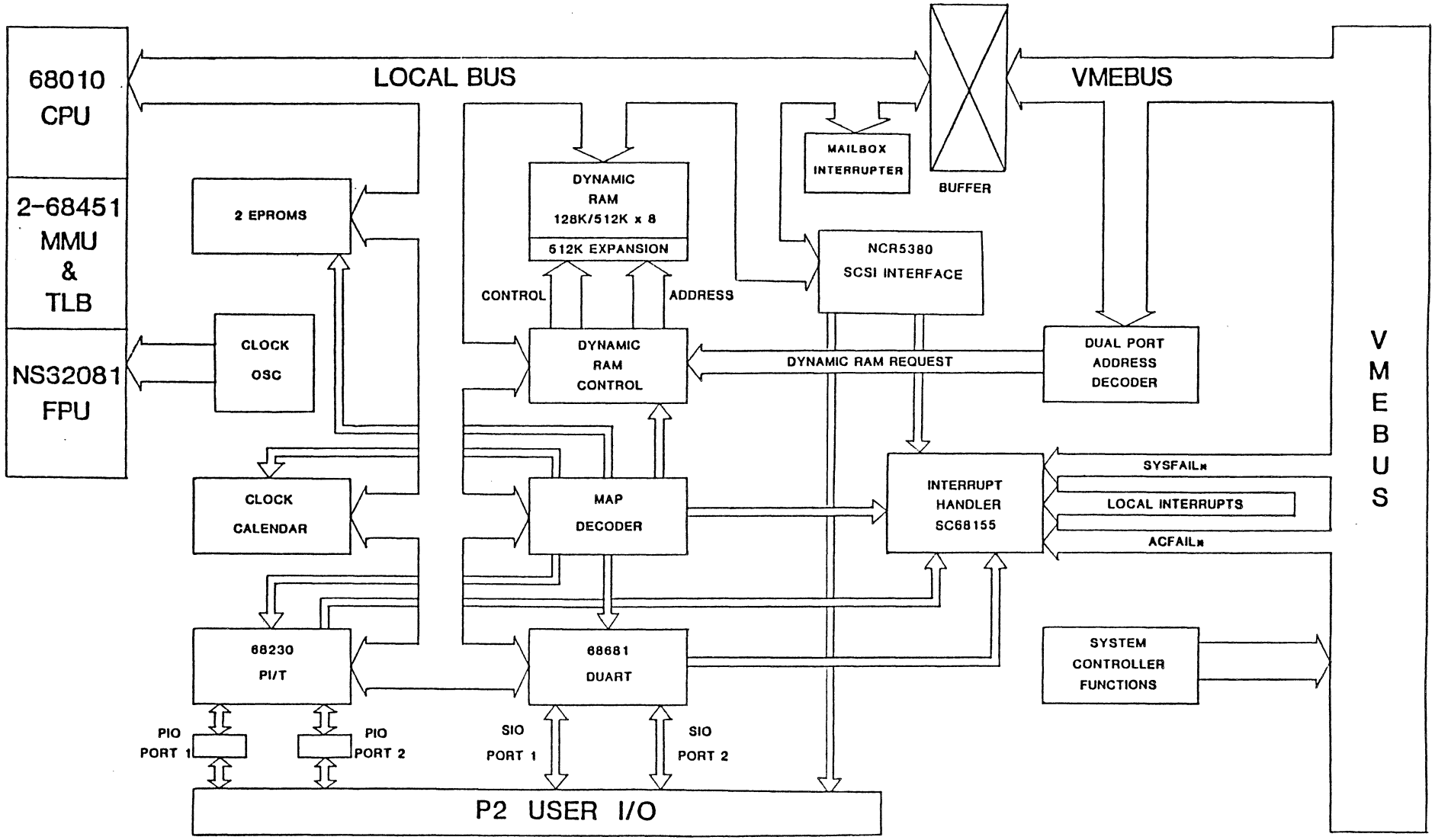


Figure 1-3. IV-1624 8-port Intelligent SIO board block diagram

(see drawing on opposite page)

IV-1624 BLOCK DIAGRAM

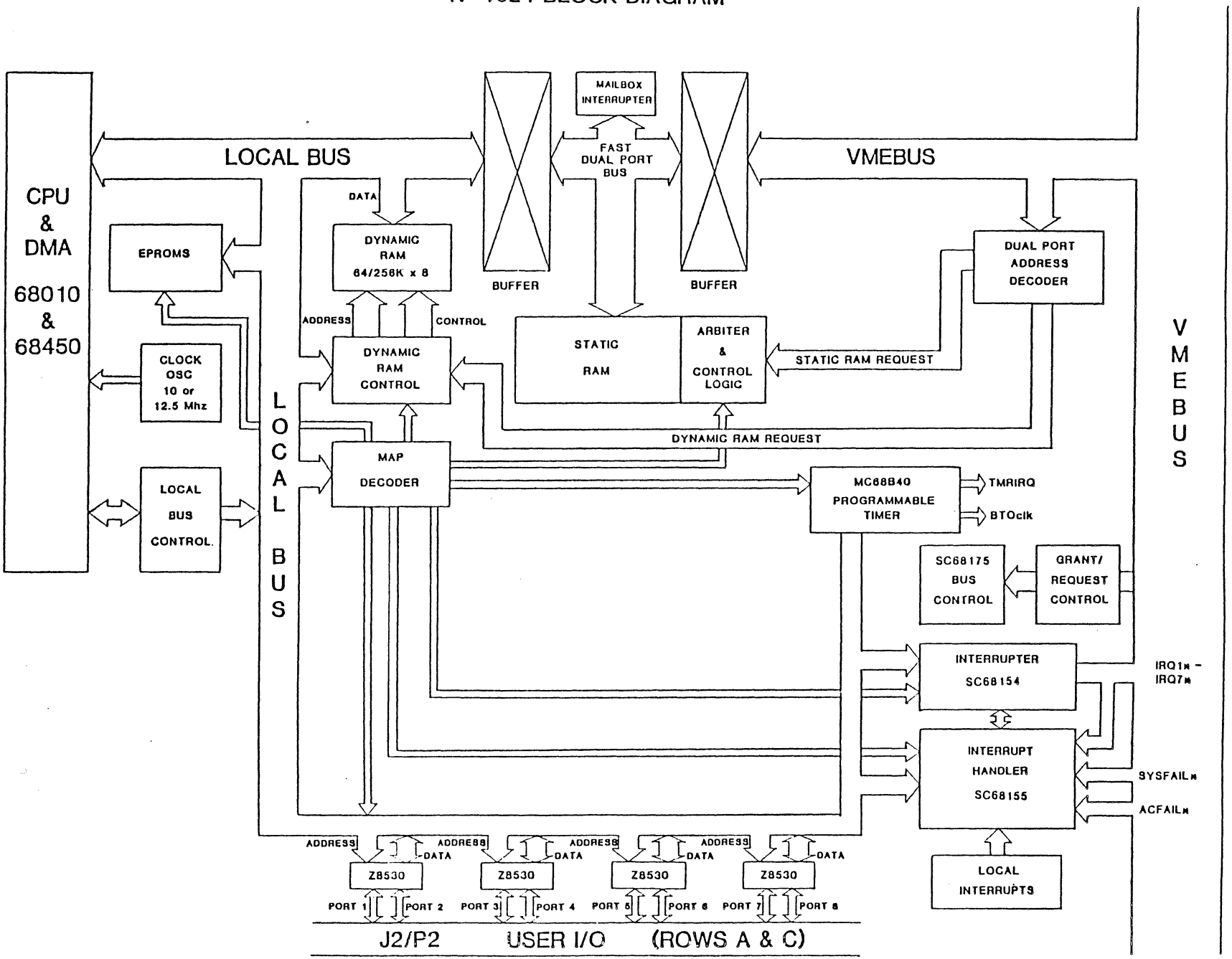


Figure 1-4. IV-3201 32-bit CPU block diagram

(see drawing on opposite page)

IV-3201 BLOCK DIAGRAM

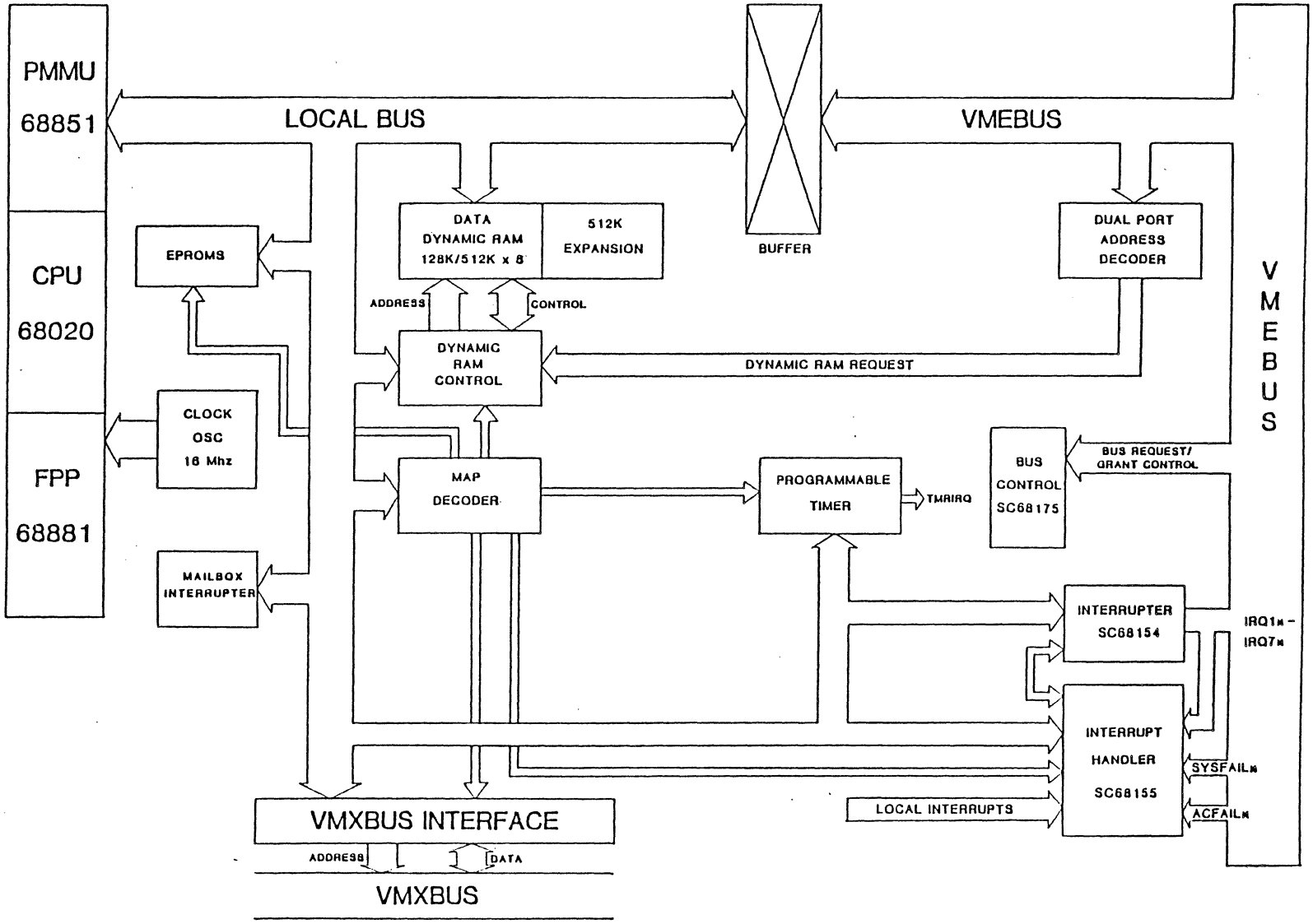
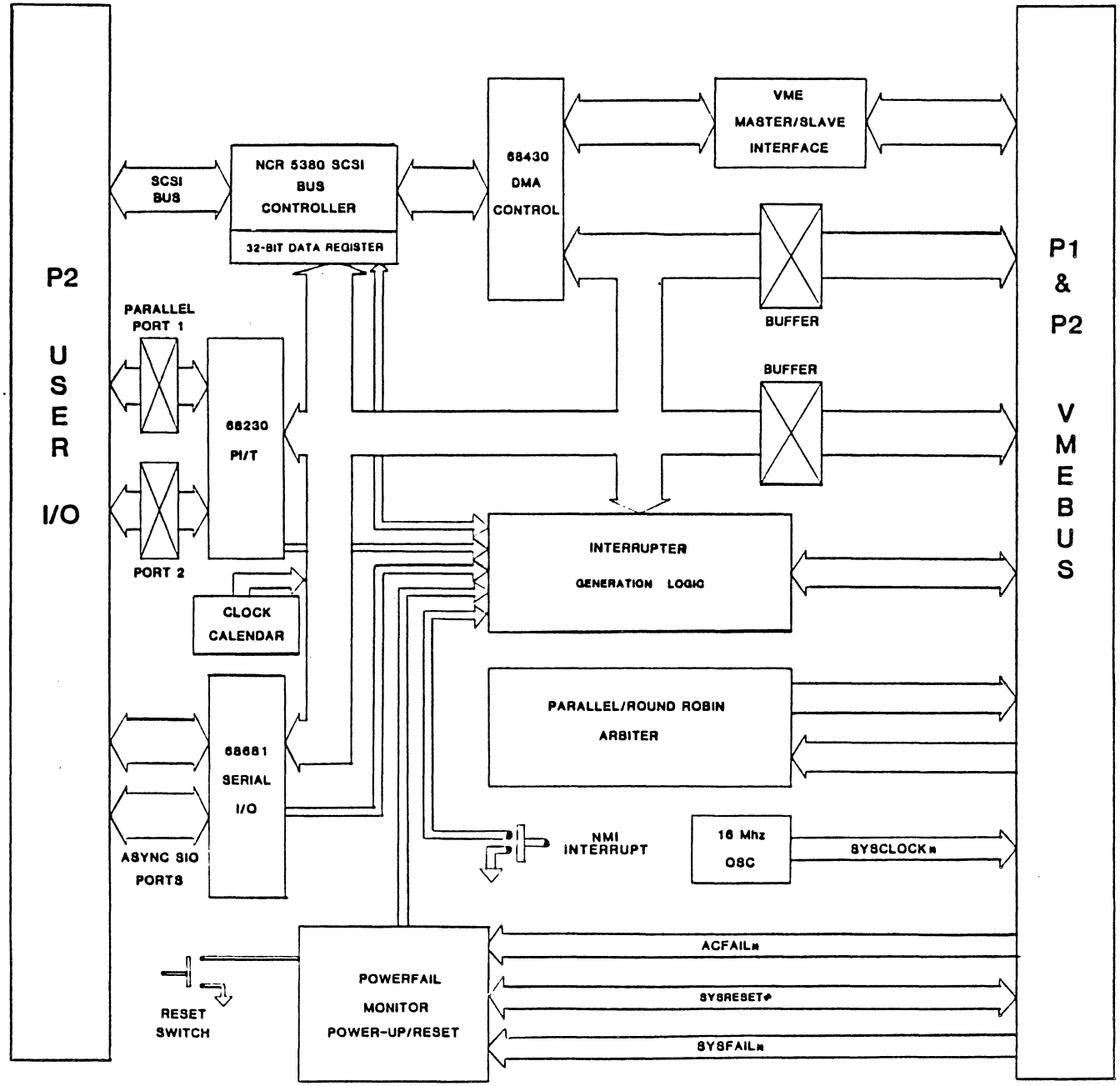


Figure 1-5. IV-3273 System Controller block diagram

(see drawing on opposite page)

IV-3273 SYSTEM CONTROLLER



1.5 Technical references

1.5.1 General references

The following publications will be useful to all users of family products. We recommend that all users obtain and familiarize themselves with these documents. Each is available from the vendor.

TABLE 1-3. General references

MANUAL	VENDOR
MC68010 User's Manual	Motorola
MC68010 Programmer's Manual	Motorola
MC68010 Data Sheet	Motorola
MC68B40 Programmable Timer Data Sheet	Motorola
VMEbus Specifications (Revision C)	Motorola
SC8X821/68175 VME Bus Controller Data Sheet	Signetics
SC8X824/68155 VME Interrupt Handler Data Sheet	Signetics
SC8X825/68154 VME Interrupter Data Sheet	Signetics

1.5.2 Specific references

The following table shows specific technical references which should be obtained by users of specific multiprocessing family boards. Copies of these documents may be obtained from vendors.

TABLE 1-4. Specific references

IRONICS PRODUCT	MANUAL	VENDOR
IV-1601	VMXbus Specification (revision A)	VME Users' Group
	NS32081 FPP Data Sheet	National Semiconductor
IV-1602	SCN68230 PI/T Data Sheet	Signetics
	SCN68681 DUART Data Sheet	Signetics
	MOS Microprocessor Data Manual	Signetics
	MM58274 Clock/calendar Data Sheet	National Semiconductor
IV-1624	MC68450 DMA Controller Data Sheet	Motorola
	Z8530 Data Sheet	Zilog
	Z8030/Z8530 SCC Technical Manual	Zilog
	Z8030/Z8530 SCC Application Note	Zilog
IV-3201	MC68851 HCMOS PAGED MMU	Motorola
	MC68881 Floating Point Processor Data Sheet	Motorola
	MC68020 Data Sheet	Motorola
	MC68020 User's Manual	Motorola
	VMXbus Specification (revision A)	VME Users' Group
IV-3273	NCR5380 SCSI Bus Controller Data Sheet	NCR
	SCN68430 DMA Interface Data Sheet	Signetics
	MOS Microprocessor Data Manual	Signetics
	SCN68230 PI/T Data Sheet	Signetics
	SCN68681 DUART Data Sheet	Signetics
	MM58274 Clock/calendar Data Sheet	National Semiconductor

1.6 Customer service

For more information about **IRONICS** multiprocessing products, contact a customer service representative by writing or calling:

IRONICS Customer Service
798 Cascadilla Street
Ithaca, New York 14850
(607) 277-4060

2. INSPECTION, INSTALLATION, AND CHECKOUT

2.1 Unpacking Instructions

All **IRONICS** products are manufactured in a static-free environment to insure minimal degradation in component performance due to electrical discharge. All boards are shipped in conductive wrapping for protection during shipping. The following precautions should be observed during unpacking and installation:

[1] All board handlers should be properly grounded and working in static-free work areas.
[2] Boards should be handled by board edges, avoiding contact with all connector surfaces.
[3] Avoid touching any MOS components.

2.2 Inspection

After removing the board from its protective wrapping, inspect the board. Any loose debris should be be removed from the board surface. Inspect the following:

[1] Check all chips in sockets (EPROMs, PLAs, etc.) for loose seating. Apply even pressure on top of chip to reseat, if necessary.
[2] Check socketed chips for bent pin legs or bad connections.
[3] Check bottom of the board for broken or loose jumper wires (if present).
[4] Check the board surface for warping.

Report any serious board irregularities IMMEDIATELY to:

CUSTOMER SERVICE REPRESENTATIVE
IRONICS, INC.
798 Cascadilla Street
Ithaca, New York
(607) 277-4060

2.3 Installation procedure

Before proceding, read the manual. Many of the board's finer design aspects have been described in chapter 3. Basic familiarity with the board could save hours of debugging, and will make our job of maintaining and servicing your IRONICS purchase faster and easier.

2.3.1 Minimum system requirements for checkout

The minimum amount of hardware and software required for a board test is as follows:

[1] IMON1624 v3.1 DEBUG MONITOR installed in the IV-1624 EPROM sockets (or some other suitable debug monitor allowing memory accesses).
[2] VMEbus system controller card
[3] IV-1624 8-Port Intelligent Serial I/O Board
[4] Serial I/O module + cable assembly

2.3.2 Shunt installation

The board (as shipped) should have the shunts in place for minimum system functions (i.e., EPROM, local and dual port RAM access, etc). Verify that IV-1624 shunt installation is correct by comparing installation with descriptions in chapter 3. Make sure that the bus request/ bus grant shunts are installed.

Note:

The bus request/grant jumpers must be configured to level 3 when configured with the IV-1600 System Foundation Module or with any other CPU card with a single-level arbiter!

2.3.3 VMEbus cable installation

The data and control lines which comprise eight serial ports are bussed to row A and row C of the P2 connector (J2/P2 pin assignments are provided in the Appendix section of the manual). These signals are relayed from the backplane to

line driver/receiver cards (and the eight female or male connectors) via a serial I/O module/cable assembly. This assembly and its installation will be described in more detail next.

WARNING:

Proper installation of the serial module/cable assembly is critical. Improper installation may result in damage to the board. Please read the next sections THOROUGHLY before attaching the cable and applying power!

2.3.4 Serial I/O adapters

IRONICS provides the ability to transfer serial data through one of three standard electrical interfaces adapters. The three standard interfaces may be purchased with DTE or DCE connectors. The following table shows the available serial I/O adapters:

TABLE 2-1. IV-1624 serial I/O adapter description

Ironics Product Number	Description	Application Note
IV-1040-C	RS-232 DCE	IV-1624 only
IV-1040-T	RS-232 DTE	" "
IV-1041	RS-449 DCE	" "
IV-1042	RS-449 DTE	" "
IV-1043-C	Current loop	" "
IV-1043-T	Current loop	" "

Modules may be purchased in groups of four (4). One cable is required for each group of four serial ports desired. Hence, two cables are required to use more than four (4) ports.

NOTE:

The type of serial interface (e.g., RS-232, RS-449 or current loop), connector sex (male or female), and the connector mode (DCE/DTE) should be specified at the time of purchase.

Modules are shipped assembled with the cable assembly attached.

2.3.5 Adapter cable installation

The cable required to connect the backplane serial I/O pins on P2 rows A or C to the serial I/O adapters is a 64-wire ribbon A 64-pin female connector busses the serial data and control lines from the 4 serial ports of row A or from row C (see figures 1.1 and 1.2; refer to the Appendix section of the manual for P2 channel designations).

The opposite end of the cable is split into four parts, each of which is terminated by a 16-pin female connector. Each of the four 16-pin connectors attach to a unique serial I/O adapter to interface a serial channel. Two cables are included.

To use ports 1 through 4:

- The cable marked "A" busses those serial ports (ports 1-4) which originate from row "A" of the backplane and the ground row immediately below it. The red cable stripe should be closest to pin 1 of P2 (refer to figures 2.2 and 2.3).

- The cable marked "C" busses those serial ports (ports 5-8) which originate from row "C" of the backplane and the ground row immediately above it. The red cable stripe should be closest to pin 1 of P2 (refer to figures 2.2 and 2.3).

- There is no cable "B": Connection of a cable to pins on row B will result in the shorting of power (+5V) to ground and in serious damage to the board.

Figure 2-1. Backplane pin designation

This figure shows the backplane pins as viewed by someone looking at the back of the card cage.

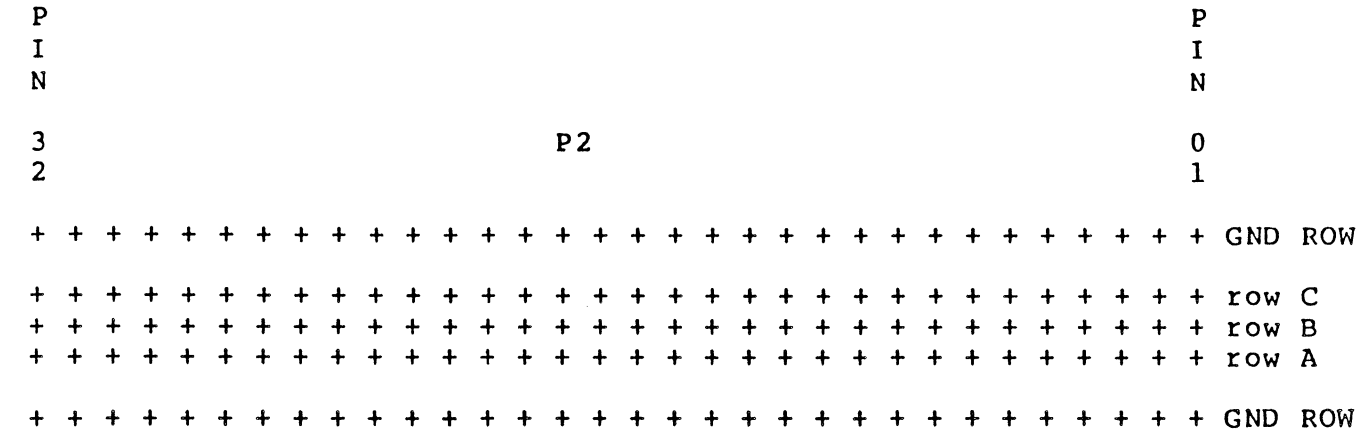


Figure 2-2. IV-1624 cable installation

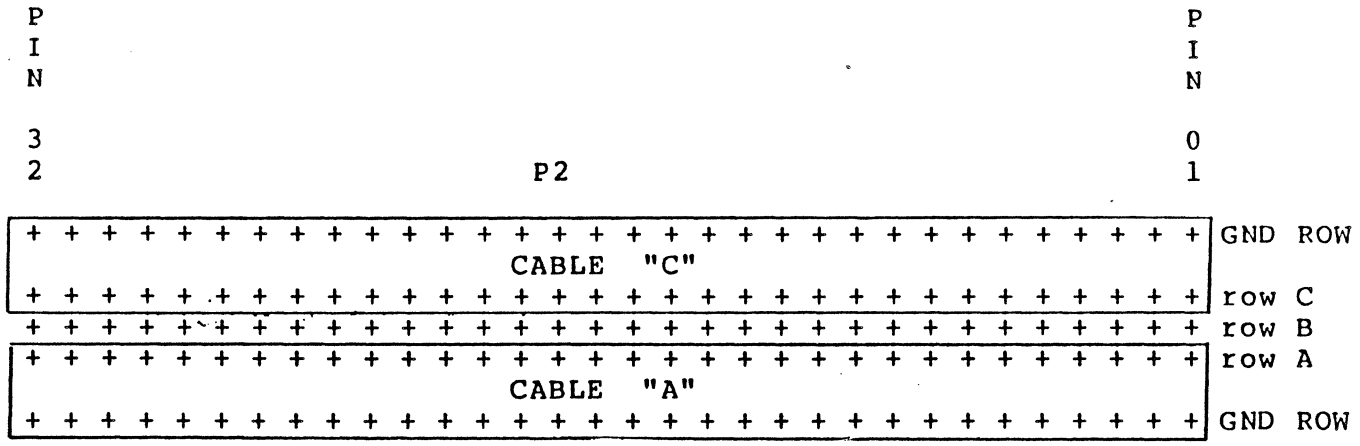
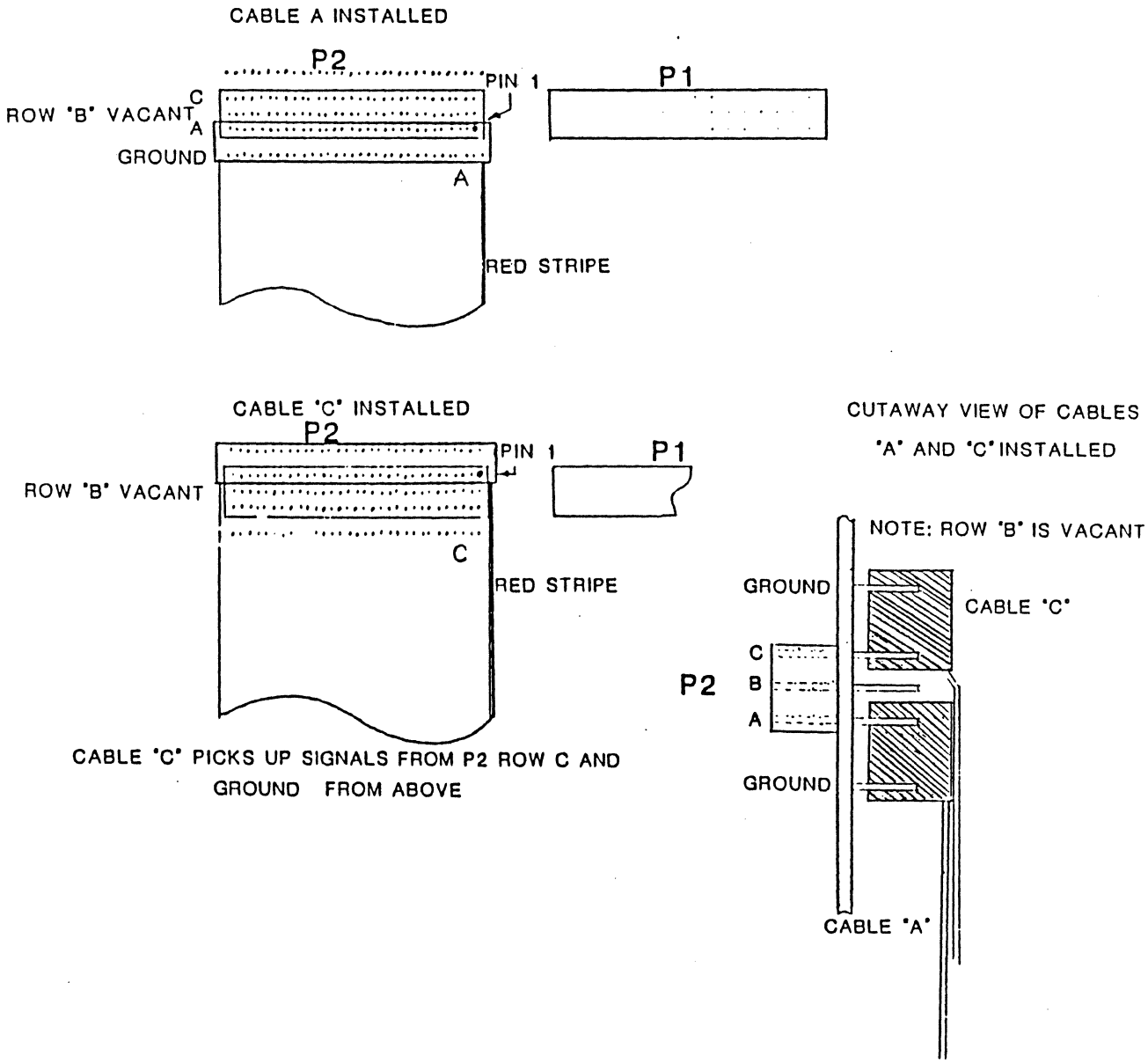


Figure 2-3. Proper installation of cables 'A' and 'C' to backplane

This view shows the 64-pin connector installed on the backplane. Cable "A" picks up signals from P2 row A and ground below. Cable "C" picks up signals from P2 row C and ground above. Note that row B is bussed on the P2 backplane. Neither cable should connect to P2 row B.

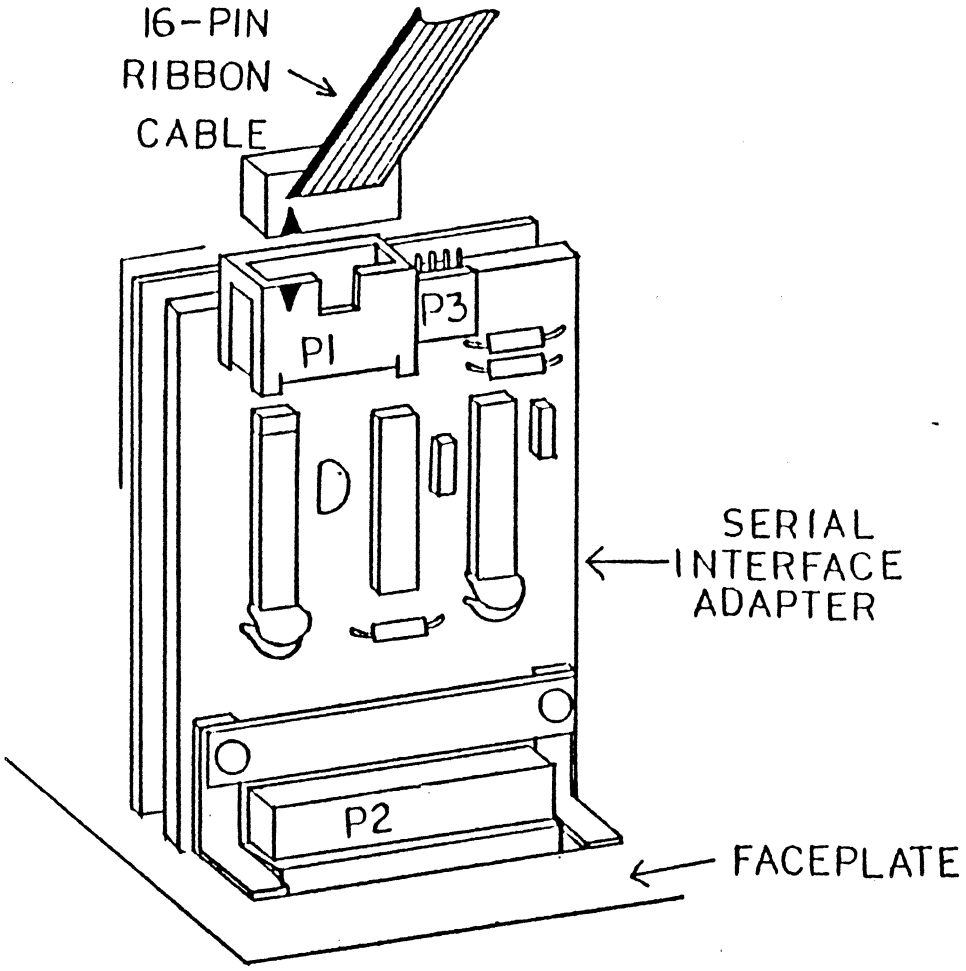


The opposite end of the cable (the four ends terminated with 16-pin male connectors should be shipped already attached to an electrical interface adapter. Refer to Figure 2-4 to insure that the SIO adapter end has been properly installed.

The board is now ready for power-up and test.

Figure 2-4. Proper installation of cable 'A' or 'C' on serial I/O adapter

Cables 'A' and 'C' terminate in eight 16-pin connectors which attach to one of eight electrical interface adapters. The diagram shows one of the cable ends attaching to an adapter. The arrows on the connector and adapter should be aligned.



Power is supplied to the serial I/O adapters by way of a four-wire cable (refer to figure 2-5). Table 2-2 shows the voltage supplied by each wire. Make sure that each connector is properly inserted before applying power!

Figure 2-5. Proper installation of power wires to serial I/O adapters

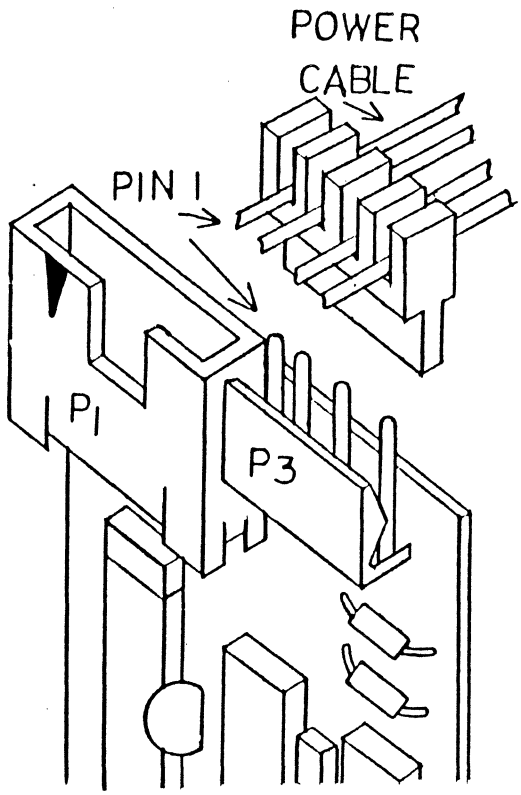


TABLE 2-2. Power cable pin assignment for electrical interface adapters

Adapter Pin No.	Adapter Type RS-232	RS-449
1	+5	+5
2	GND	GND
3	-12	NC
4	+12	CHASSIS GND

2.3.6 Power up and test procedure

Turn on power and look for the IMON1624 monitor prompt:

```
IMON1624 v3.1>
```

2.3.6.1 EPROM checkout

Verify that the entire EPROM address range can be read by typing:

```
IMON1624 v3.1>  MD F00000 FFFF <CR>
```

If the "MD" command terminates before F0FFFF, contact factory immediately and describe the failure. If the entire range may be read, attempt to write to the EPROM address space with the following command:

```
IMON1624 v3.1> MM F00000 F0FFFE 00 <CR>
```

The monitor response should be:

```
IMON1624 v3.1> MM F00000 F0FFFE 00 <CR>
Physical Address= 00F00000 0F0FFFE

Data did not store
```

Follow up by displaying the entire range again with the command:

```
IMON1624 v3.1> MD F00000 FFFF <CR>
```

The display of memory should show that the '00' pattern written to memory did not store. If the EPROM address

space appears to be written with a solid '00' pattern, notify the factory immediately.

2.3.6.2 On board RAM checkout

Attempt to write and read the entire range of dynamic RAM using the following commands:

IMON1624 v3.1> MD 0 100000 <CR>

This read should terminate with a bus error at the end of the dynamic RAM address range (i.e., bus error at 10000H for 64K or bus error at 040000H for 256K option). If the read terminates before the expected address range, verify that shunts are properly installed.

Attempt to write the entire dynamic RAM address range using the command:

IMON1624 v3.1> BF 0 100000 FF <CR>

Verify visually that the entire range was successfully written. If problems continue (e.g., bus errors before the predicted end of memory, imcomplete writing of the address range), notify the factory.

Repeat the above procedure for the static RAM address range.

2.3.6.3 Dual port access checkout

Attempt to read the IV-1624's dual ported static and dynamic RAM from a remote bus master with the IV-1624 withdrawn from its slot. A bus trap error should result, indicating that no conflicting device has been installed. Insert the IV-1624 and verify that its memory can be read over the entire dual port address.

2.3.6.3.1 VMEbus grant/request daisy chain checkout

Verify that the bus request/bus grant daisy chain is complete up to the IV-1624 slot (shunt BGIN* to BGOUT* on empty slots).

2.3.6.3.2 VMEbus access checkout

Test the VMEbus by attempting to read from and write to another VMEbus slave.

3. IV-1624 THEORY OF OPERATION

This chapter is intended to provide an general overview of IV-1624 operation. The board is divided up by functional areas outlined below. Users of other **IRONICS** multiprocessing boards will be able to see the simularities between the IV-1624 and other family members. We hope that these similarities will lead more rapid understanding of all multiprocessing family members, and hence, faster integration of **IRONICS** multiprocessing boards into a system.

3.1 Board control logic

Much of the onboard control logic is contained within high-density programmable logic arrays (PLAs and PALs). The following table shows all programmable logic chips and their functions. More detailed descriptions of all PLA and PAL functions are included in the following section. Partial PLA and PAL table contents are provided in Appendix E.

TABLE 3-1. IV-1624 PLA/PAL descriptions

PLA#	V	U#	Type	Description
501	-	U22	82S152	*IV-1624 Reset-retry PLA
503	-	U13	82S153A	IV-1624 Dual port control PLA#1
504	-	U38	82S153A	IV-1624 Dual port control#2
505	0	U74	82S153	IV-1624 Dual port address decoder (64K)
505	2	U74	82S153	IV-1624 Dual port address decoder(256K)
50C	-	U31	82S153	*IV-1624 Local I/O decoder
50D	-	U33	82S153	*IV-1624 IACK decoder
50E	2	U47	82S153A	*IV-1624 Memory map decoder PLA (256K)
50E	3	U47	82S153A	*IV-1624 Memory map decoder PLA (64K)
510	-	U27	82S159	IV-1624 Control port and SCC timing
518	-	U10	82S153A	IV-1624 Dynamic RAM control PLA
518	-	U26	82S153	IV-1624 Local bus arbiter PLA
51A	-	U73	82S153	IV-1624 Bus release and AMchecker
51B	-	U81	82S153	IV-1624 Mail box interrupter

V = version number
U = location number

Asterisk (*) indicates that logic tables are provided in this manual;

3.1 Board level description

The block diagram of the IV-1624 board is provided in figure 1-3. The board is divided into six functional areas:

1. The CPU core containing:

   - CPU
   - Map decoding circuitry
   - EPROMs
   - RESET/RETRY circuitry
   - clock/timer
   - LED indicators
   - Local bus arbitration circuitry

2. The dynamic RAM interface containing:

   - dynamic RAM and dynamic RAM controller

3. The static RAM interface containing:

   - Static RAM and control circuitry

4. The VMEbus interface containing:

   - Interrupt requesting and handling circuitry
   - VMEbus controller
   - Bus release circuitry
   - VME address, data lines, and buffers
   - Dual port RAM control and arbitration circuitry

5. The serial I/O interface containing:

   - serial ports
   - serial port control interface

6. DMA controller interface

Each section will be treated in detail in the following section.

3.3 The CPU core

The CPU core is comprised of the CPU, memory map decoder, EPROMS, RESET/RETRY generator, clock timer, and local bus aritration circuitry.

3.3.1 The 68010 CPU

The 68010 microprocessor, coupled with innovative hardware design, forms the base for the IRONICS performance standard. The IV-1624 uses the 68-pin grid array (PGA) packaging. 68010 data (pin assignments and layout) are provided in Appendix B. It is assumed that the user has a basic knowledge of 68010 microprocessor architecture. For a review of this architecture see the **MC68000 16/32-bit Microprocessor: Programmers Reference Manual (4th edition)** available from Motorola.

3.3.2 Memory map and local I/O decoding

Global memory mapping is accomplished by logic contained within a single PLA (50E). Table 3-2 shows the standard memory map configuration. Figure 3-1 shows map decoder pin assignments. The upper eight address lines (A23-A16) are read by the map decoder which asserts a device select line for the corresponding device. (See Appendix E for map decoder PLA logic).

EXAMPLE:

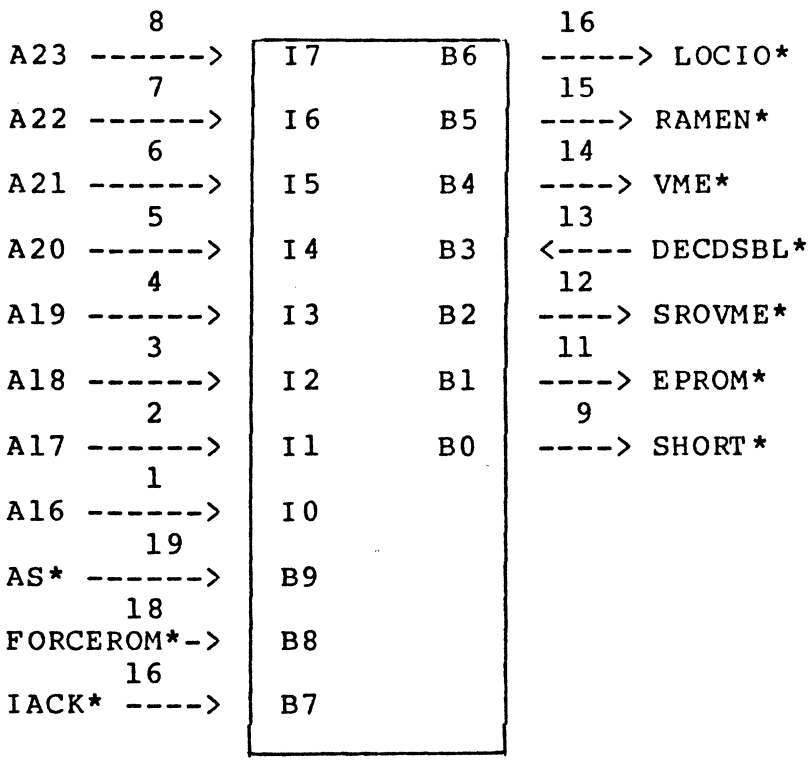
The CPU requests a byte-length read from location 001000H. The map decoder responds by asserting the chip select for dynamic RAM (RAMEN*).

TABLE 3-2. IV-1624 standard memory map configuration

Description	Address Range	Map Decoder Output	PLA Pin #
Local Dynamic RAM	000000-00FFFF (64K)	RAMEN*	15
Local Dyncmic RAM	000000-03FFFF (256K)	RAMEN*	15
EPROM address space	F00000-F0FFFF	EPROM*	11
Local I/O	F70000-F7FFFF	LOCIO*	16
Static dual port RAM	FE0000-FEFFFF	SROVME*	12
VMEbus address (A23)	010000-DFFFFF(64K)	VME*+SROVME*	14+12
VMEbus address (A23)	040000-DFFFFF(256K)	VME*+SROVME*	14+12
VMEbus address (A23)	F10000-F7BFFF	VME*+SROVME*	14+12
VMEbus address (A23)	F7D000-F7FFFF	VME*+SROVME*	14+12
VMEbus address (A23)	F90000-FEFFFF	VME*+SROVME*	14+12
VMEbus address (A16) (see note below)	FF0000-FFFFFF	SHORT*+VME* +SROVME*	9+14 12

note: refers to valid address bus bits per address modifier codes

Figure 3-1. Map decoder pin assignments



Note that the SROVME* ("static RAM or VMEbus") output selects both the VMEbus and static RAM whenever a VMEbus or static RAM address is received. The VME* output acts as a secondary select: if VME* is asserted, the VMEbus transceivers are selected. If VME* is not asserted, static RAM is enabled. The SHORT* output is used as a VMEbus address modifier.

3.3.2.1 Altering the memory map

It is possible to change the memory map for custom system configurations: for instance, the map decoder logic could be changed to address the bottom of dynamic RAM at 040000H instead of 000000H. A change of this nature would require a custom map decoder PLA which can either be designed and programmed by the user using the PLA table provided in Appendix E, or can be, in most cases, supplied by IRONICS. To request about a custom map decoder, contact an IRONICS customer service representative.

3.3.2.2 Local I/O decoding

The local I/O memory space is located in the range F70000-F7FFFFH. The memory map decoder PLA (506) asserts LOCIO* when it sees an address within this hexadecimal range. This output enables the local I/O decoder (PLA 50C), which further decodes this range. The local I/O decoder asserts the chip select line for the designated device. All local I/O devices and their addresses are shown in table 3-3. The local I/O decoder PLA is included in Appendix E.

TABLE 3-3. IV-1624 Local I/O map

Output	Memory Map	A9	Description
SCC0CS*	F7E0XX	0	SIO channel 0 chip select
SCC1CS*	F7E4XX	0	SIO channel 1 chip select
SCC2CS*	F7E8XX	0	SIO channel 2 chip select
SCC3CS*	F7ECXX	0	SIO channel 3 chip select
SCC or CONTROL*	F7Exxx	1	SIO control port
IVHANCS*	F7F0xo	--	Interrupt Handler chip select
IGORCS*	F7F4xo	--	Interrupt Generator chip select
TMRCS*	F7F8xe	--	Timer chip select
DMACS*	F7FCxw	--	DMA controller chip select

o = chip selected when odd low byte written (byte accesses only!)
e = chip selected when even low byte written (byte accesses only!)
w = chip selected when "word" (16-bit) length data written
-- = don't care
* = signal active low

3.3.3 EPROM theory of operation:

The IV-1624 has two bytewide EPROM sockets capable of holding the devices specified in the following table.

TABLE 3-4. Bytewide Devices

Device	Size	Organization
2764	64K	(8192 X 8 bit)
27128	128K	(16384 X 8 bit)
27256	256K	(32768 X 8 bit)
27512	512K	(65536 X 8 bit)

The standard addressing range is F00000-F0FFFFH.

3.3.3.1 EPROM DTACK* generation

EPROM data transfer acknowledge (DTACK*) is generated within the RESET/RETRY generator. DTACK* is controlled by an RC circuit, whose discharge time, coupled with EPROM internal access speed, determine the number of wait states incurred during an EPROM data transfer. The following table shows RC capacitor values and EPROM internal access times necessary to perform data transfers with a minimum of wait states. The number of EPROM wait states desired should be specified at the time of purchase.

TABLE 3-5. EPROM DTACK* speed

CPU speed	# of wait states	EPROM speed	capacitor value
10 MHz	0	170 ns	0 pf
10 MHz	1	250 ns	120 pf

3.3.4 RESET/RETRY generation

The RESET/RETRY generator performs the following functions:

[1] it initiates power-up (cold), local, and system resets
[2] it initiates a processor retry cycle when necessary
[3] it monitors the watchdog timer

Each of these topics will be discussed in more detail.

3.3.4.1 Reset generation

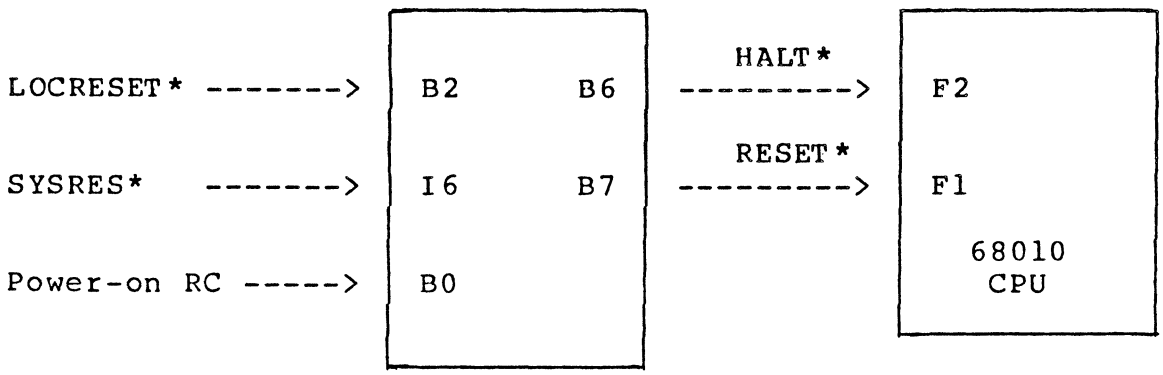
In 68000/68010 architecture, a "reset" is indicated by the assertion of the HALT* and RESET* lines. These lines are bidirectional: they can be driven "internally" (i.e., driven by the CPU to signal a reset to all local (onboard) devices), or "externally" (i.e., driven by either a local (onboard) or remote (offboard) device). An internal reset is triggered by execution of a software "RESET" instruction, asserting the RESET* line for 124 clock pulses, and resulting in the resetting of all onboard LSI devices.

The RESET/RETRY PLA (501) monitors all of the external devices (onboard or offboard) capable of requesting a reset. The RESET/RETRY PLA responds to an external reset request by driving the HALT* and RESET* lines to the CPU (see figure 3-2).

3.3.4.1.1 Power-on (cold) resets

When power (Vcc) is initially applied to the IV-1624, an RC circuit generates a high input to B0 for a minimum of 250 milliseconds. The RESET/RETRY PLA responds by asserting FORCEROM*, HALT* and RESET*. The simultaneous assertion of HALT* and RESET* forces the 68010 CPU to begin a reset cycle. The assertion of FORCEROM* forces the selection of the EPROM address space. The CPU begins to read 4 words from memory address $000000. Since the EPROM address space has been selected, the CPU reads address $F00000H. These 4 words are comprise the reset vector. The first longword (32 bits) is vector number 0, which provides the initial value of the supervisor stack pointer (SSP). The following

Figure 3-2. Reset/Retry PLA inputs



RESET/RETRY PLA (501)

longword contains the initial program counter value (PC), which is the monitor entry point.

3.3.4.1.2 Local resets

Two members of the IRONICS multiprocessing family provide a 3-post connector for attaching a reset switch. The members of the family currently providing this capability are:

[1] the IV-1601 VMX/VME CPU board
[2] the IV-1624 8-Port Serial I/O board

The following members of the IRONICS multiprocessing family provide a local reset switch which is mounted through the front bezel:

[1] the IV-1602 Single Board Computer
[2] the IV-3201 32-bit CPU
[3] the IV-3273 System Controller board

Depression of the local reset switch causes assertion of input B2 of the RESET/RETRY generator. The RESET/RETRY PLA responds by asserting HALT* and RESET* inputs to the CPU.

3.3.4.1.3 System ('warm') resets

A system reset occurs when a VMEbus master asserts the VMEbus system reset (SYSRES*) line. The SYSRES* line is monitored by the RESET/RETRY PLA, which responds by asserting the HALT* and RESET* inputs to the CPU. Since the IV-1624 is not a system controller, it does not have the capability to generate a system reset.

NOTE:

The IV-1602 VME CPU and the IV-3273 System Controller I/O board have the capability to generate a system reset.

3.3.4.2 Retry cycles

In a bus architecture requiring handshakes between the CPU and an external device, the possibility exists that the handshake might not occur. If the handshake fails to complete, some action must be taken to retry the uncompleted bus cycle and, to terminate any cycle that cannot be completed. The processor must see HALT* and BERR* driven low by some external device in order to initiate a retry. The CPU will put its address, data, function code and control lines in high impedance state until the halt signal is removed by external logic. The CPU then re-runs the previous cycle, using the same address, function codes and data (for a write operation). If the retry fails, the external logic asserts the BERR* line, forcing the CPU to begin exception processing. The user should be aware of the following conditions and how they are resolved.

3.3.4.2.1 Transient arbitration conflicts

The RESET/RETRY PLA provides the external logic to monitor local bus activity and tells the CPU when a retry is required. Occasionally, a transient conflict arises between a DRAM dual port request and the local CPU or DMA controller request of the VMEbus. The RESET/RETRY logic causes the local CPU to remove its request for the bus and allow the DRAM dual port access to be completed. After the dual port transfer has completed, the CPU will request the bus again and retry its last uncompleted cycle.

3.3.4.2.1.1 Deadlock protection

68000/68010 architecture guarantees indivisibility of the read-modify- write cycle. If the CPU is executing a "test and set" (TAS) instruction when a local bus conflict (or "deadlock") occurs, the instruction will not be retried once the CPU regains the bus. Instead, the CPU enters into bus error exception processing. Software can detect this condition in a bus error handling routine which polls the XCPRTY line on the interrupt handler chip. If XCPRTY is asserted, exception processing began during a retry, and software may recover by executing a return from exeption (RTE) and re-executing the instruction.

NOTE:

Deadlock can only be caused by DRAM dual port accesses; static dual port RAM accesses cannot cause deadlocks or retry exceptions.

3.3.4.2.2 VMEbus retries

A retry will also occur when BUSERR* is asserted on a VMEbus access. This condition is monitored by the bus controller chip, which asserts both LBERR* and HALT* to cause a retry.

3.3.4.3 Bus timeout generation

The role of the RESET/RETRY PLA in bus timeout generation is covered in the description of MC68B40 programmable timer (channel 2) operation.

3.3.5 MC68B40 programmable timer

The MC68B40 Programmable Timer Module (PTM) is an integrated set of three counter/timers. Channel 2 is the hardware-dedicated watchdog timer, respectively. Channels 1 and 3 are free for user applications. Please be aware of the following restrictions on use of the programmable timer:

[1] Any software running on the IV-1624 must contain initialization and for channels 1 and 2 to insure proper functioning of memory and generation of bus timeouts.
[2] The CPU's "E" output (its clock frequency divided by 10) must be used as each counter's input. External clock inputs C1, C2, and C3 (pins 28, 4, and 7) and their gate enables, G1, G2 and G3 (pins 26, 2, and 5) are tied to ground.

Theory of operation and sample initialization software is provided in the following sections.

3.3.5.1 Channel 2 bus timeout clock

The bus timeout counter is cleared when address strobe (AS*) is high and increments on the rising edge of BTOCLK, the 68B40's channel 2 output. If the counter reaches state 15 before LDTACK* is asserted, a bus timeout condition is said to exist and LBERR* is asserted to the local processor by the RESET/RETRY PLA. Thus the bus timeout period is 15 times the period of BTOCLK and is under software control by programming channel 2 of the MC68B40.

Note:

The bus timeout clock (Channel 2) is inhibited while the local CPU is waiting for a VMEbus grant. This prevents the watchdog timer from issuing a timeout while another bus master (e.g., a DMA controller) is completing a lengthy bus transfer.

3.3.5.2 Channels 1 and 3 (User programmable channels)

Channels 1 and 3 of the programmable timer module are available for user applications. Timer interrupt requests are generated by programming either channel to generate a waveform on TMRIRQ (pin 6 (O3) of MC68B40). This generates an interrupt request on level 5 (IRQ5). The SC68155 interrupt handler chip must be programmed for active-low, level sensitive interrupt requests to process interrupts.

3.3.5.3 Timer initialization

The local I/O decoder maps the timer base address at F7F600H. The following table contains the memory mapped addresses of all of the chip internal buffers and registers (refer to the MC68000 Microprocessor Data Manual for internal further programming details).

TABLE 3-6. Programmable timer I/O map

Address	Description	
	Write	Read
F7F600H	CR20=0 Write control register #3 CR20=1 Write control register #1	
+02H	Write control register #2	Read status register
+04H	Write MSB buffer register	Read timer #1 counter
+06H	Write timer #1 latch	Read LSB buffer register
+08H	Write MSB buffer register	Read timer #2 counter
+0AH	Write timer #2 latch	Read LSB buffer register
+0CH	Write MSB buffer register	Read timer #3 counter
+0EH	Write timer #3 latches	Read LSB buffer register

3.3.5.3.1 Sample initialization

The following code will initialize channel 1 to allow RAM refresh, provide a 4 microsecond timeout period on the watchdog timer (channel 2), and generate a a square wave on the user channel (channel 3).

```
                ********************************
                * Sample initialization code   *
                *          for the             *
                *       MC68B40  PTM           *
                *        version 1.0           *
                *     23 Jan 85 Ironics Inc    *
                ********************************

FIRST
        .long   0x444           |initial SP for reset
        .long   START           |initial PC
START
        lea     0xF7F600,a0     |PTM base address
        move.b  #0x83,2(a0)     |chan 2 mode & sel chan 1
        move.b  #0x83,(a0)      |chan 1 mode & hold cmd
        move.b  #0x82,2(a0)     |chan 2 mode & sel chan 2
        move.b  #0x83,(a0)      |chan 3 mode & prescale
        move.b  #0x83,2(a0)     |chan 2 mode & sel chan 1
        move.b  #0x00,4(a0)     |16 us period on chan 1
        move.b  #0x00,6(a0)
        move.b  #0x00,8(a0)     |4 us period on chan 2
        move.b  #0x01,10(a0)
        move.b  #0x00,12(a0)    |32 us period on chan 3
        move.b  #0x0F,14(a0)
        move.b  #0x82,(a0)      |chan 1 mode & start cmd
EXDRAM
        lea     0x000000,a0     |point to DRAM
        move.l  #0x3ff00,d0     |d0 holds count
drloop
        move.w  d0,(a0)         |write data
        move.w  (a0)+,d1        |read data
        subq.l  #1,d0           |count
        bne     drloop
        bra     EXDRAM
        END
```

3.3.6 Front panel LED indicators

The CPU core has two front panel LED indicators. The HALT indicator (RED LED) is turned on when the HALT* line is asserted, indicating that the processor is in the halted state. The ACTIVE indicator (GREEN LED) is turned off when the FAIL line is asserted, indicating a catastrophic system failure.

3.3.7 Local bus arbitration

Dual port dynamic RAM, local RAM refresh circuitry, and the DMA controller are three onboard resources which compete for the local bus. The local bus arbiter PLA (518) controls and sets the priority of local bus traffic.

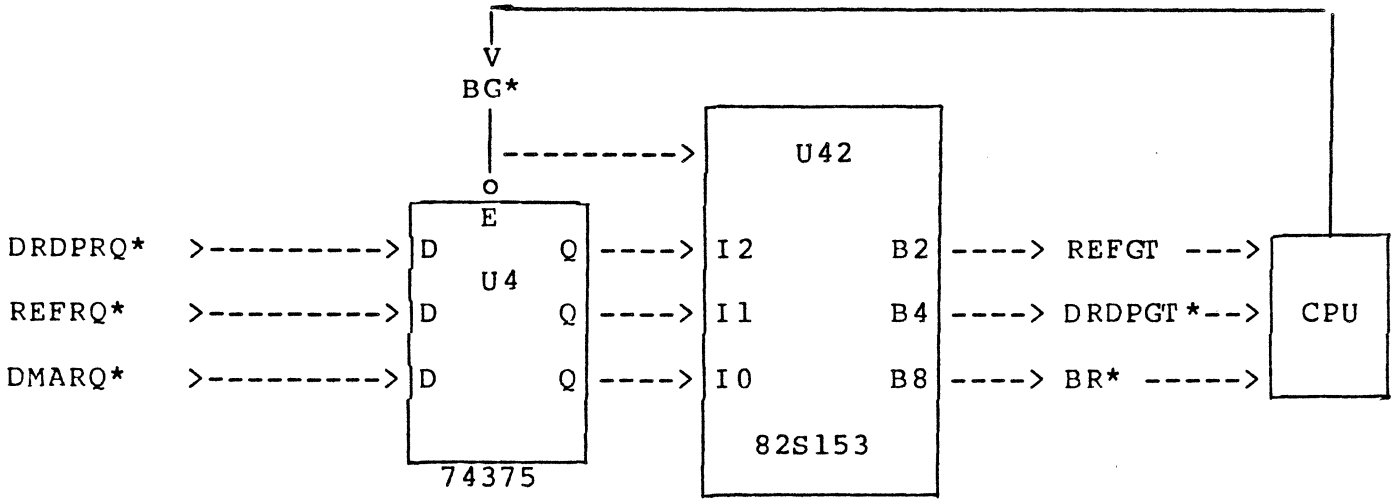
3.3.7.1 Requesting the local bus

Figure 3-3 shows a simplified diagram of the bus request circuit. The device request inputs pass through a transparent latch which allows its outputs to follow its inputs while BG* is inactive. When one or more of the local device bus requests is asserted, the local bus arbiter asserts the bus request (BR*) line to the processor. When bus grant (BG*) is asserted, the latch outputs are frozen to hold off incoming requests.

3.3.7.2 Local bus priorities

If more than one request is received by the local arbiter, the given the priorities listed below. Note that request priorities are fixed in the local bus arbiter logic and cannot be reassigned without reprogramming the arbiter PLA.

Figure 3-3. Bus request circuit



Arbiter bus priorities:

1) Refresh request (highest priority)
2) Dual port dynamic RAM request
3) DMA controller (IV-1624 8SIO only) (lowest priority)

The bus grant is routed to the highest priority requester at the end of the CPU cycle in which BG* is asserted. If refresh request is active for 8 microseconds without being satisfied, the loccal arbiter issues a refresh grant without waiting for the current CPU cycle to end. This can happen when the processor addresses non-existent memory and its cycle does not complete, or when the local CPU must wait for access to the VMEbus during periods of heavy VMEbus activity. The local arbiter issues refresh grant immediately upon sensing RESET* becoming active and maintains the integrity of local RAM.

3.4 Dynamic RAM and control interface

The IV-1624 contains 64K or 256K bytes of dual ported, wait-state free dynamic RAM. The dynamic RAM map decoder (50E) logic is included in Appendix E.

Note:

The IV-1624 uses dynamic RAM chips supporting "CAS before RAS" (or "hidden") refresh cycles. Dynamic RAMs not supporting this feature may not be substituted!

3.4.1 Dynamic RAM address decoding

Address line A0 is internally decoded by the CPU to generate the data strobes (UDS* and/or LDS*) which enable the CAS* strobe to even or odd bytes of memory. If a word transfer is taking place, the CPU asserts UDS* and LDS* and 16 data lines are enabled (D15-D0). If a byte transfer is taking place, the CPU asserts UDS* or LDS* and 8 data lines (D15-D8 or D7-D0) are enabled.

A18-A1 are multiplexed onto 9 lines to provide the memory chip with the 18 internal bits needed to identify a unique memory cell. The internal row address is clocked into RAM by the RAS* signal (S=1). The internal column address (A16-A9) is clocked into RAM in the subsequent CAS* edge (S=0).

Note:

All memory cycles initiate a memory chip RAS* cycle, regardless of whether local RAM is selected or not. A CAS* cycle will follow only if onboard RAM has been selected.

3.5 Static RAM controller and interface:

The high speed static RAM provides enhanced interprocessor communications capability with minimum degradation of the local CPU's real-time performance or of the performance of the other CPUs in the system. A 32-bit wide static RAM array sits on the "fast dual port" bus between the CPU's local bus and the VMEbus. The array is composed of (8) 4K X 4 chips with 45 nanosecond access times. This board may be easily upgraded to 16K X 4 static RAMs. Static RAM can be accessed with 8, 16, or 32-bit transfers by a remote VMEbus master and by 8 or 16 bits by the local CPU. Despite arbitration and buffer delays it is fast enough to provide wait-state free access to up to a 12.5 MHz local CPU and single wait state access to the remote bus master such as an 8 MHz CPU board.

A PLA decodes VMEbus addresses to both static and dynamic RAM dual port access requests. These are connected to the local bus and "fast dual port RAM" bus arbiters as required. When a bus grant is received in response to the dual port request, the arbiter enables the address bus transceivers to receive the VMEbus address. After a settling time, it asserts chip enable to the addressed RAMs, waits the access time, then asserts DTACK*.

3.6 VMEbus interface

The VMEbus interface is comprised of two functional units: control and address/data interfaces. The VMEbus control interface contains interrupt handling and requesting circuitry, and VMEbus release and control circuitry. The VMEbus address and data interface contains the logic, buffers, address and data lines necessary to control outgoing traffic (i.e. a CPU to VMEbus data transfers) and incoming (dual port) transfers. These are discussed in more detail in the following sections.

3.6.1 VMEbus address and data interface

The VMEbus address and data interface consists of bidirectional buffers, address and data line, and the dual port RAM map decoder. (Refer to sheet 5 of IV-1624 schematics in Appendix F.)

3.6.2 VMEbus connector/ backplane specification

The IV-1624 interfaces to the VMEbus through the J1/P1 and J2/P2 connectors. All data, address, control , and power characteristics meet the VMEbus specifications (revision C) established by the VME User's Group. Connector/backplane pin assignments are shown in appendices C and D. Detailed specifications can be obtained by consulting the VMEbus Specification (revision C).

3.6.3 Dual port accesses

Dual ported RAM is an indispensible feature of a multiprocesor system. The dual port pathway provides the path by which bus masters may read (or, optionally, write) another CPU's local RAM. This provides the means through which multiple CPUs synchronize processes and communicate.

3.6.3.1 Dual port address selection

Static and dynamic dual port addresses are shunt-selectable (see chapter 0 for details of shunt installation). Table 3-7 shows the dual port ranges which may be assigned to a CPU's local RAM. Note that each CPU in a system must have a **unique** dual port address, and that installation of the dual port shunts fixes both static and dynamic dual port addresses.

The IV-1624 block diagram (figure 1-3) shows the logical location of the dual port address decode circuitry within the VMEbus interface. A remote bus master requests a data transfer by placing a request on the VMEbus. The dual port address decoder (505) monitors addresses on the VMEbus: if it decodes an address within it static or dynamic dual port range, it will issue a dual port request. The decoder also reads the address modifier lines (AM0-AM5) to restrict accesses to data only.

TABLE 3-7. Dynamic and static RAM dual port address ranges

RAM Option	RAM Address (Local CPU Access)	RAM Address (Dual Port Access)	Dual Port AM Codes
64K DRAM	000000-00FFFF	D00000-D0FFFF	3D/39
	000000-00FFFF	D80000-D8FFFF	" "
	000000-00FFFF	E00000-E0FFFF	" "
	000000-00FFFF	E80000-E8FFFF	" "
256K DRAM	000000-03FFFF	D00000-D3FFFF	3D/39
	000000-00FFFF	D80000-DBFFFF	" "
	000000-00FFFF	E00000-E3FFFF	" "
	000000-00FFFF	E80000-EBFFFF	" "
16K SRAM	FE0000-FEFFFF	F80000-F8FFFF	3D/39
	FE0000-FEFFFF	F90000-F9FFFF	" "
	FE0000-FEFFFF	FA0000-FAFFFF	" "
	FE0000-FEFFFF	FB0000-FBFFFF	" "
64K SRAM	FE0000-FEFFFF	F80000-F8FFFF	3D/39
	FE0000-FEFFFF	F90000-F9FFFF	" "
	FE0000-FEFFFF	FA0000-FAFFFF	" "
	FE0000-FEFFFF	FB0000-FBFFFF	" "

Note that a 64K byte address range is decoded regardless of whether 16K or 64K bytes of RAM exists.

3.6.3.2 Dual Port Arbitration

Dual port arbitration is controlled by two controllers (PLAs 503 and 504). These control data transfer between the local bus and the VMEbus. When the static RAM is idle, the fast dual port bus arbiter connects SRAM to the local CPU to maximize local CPU performance. The "fast dual port bus" must be connected to the local CPU in order for the local CPU to get onto the VMEbus. Because of local bus is normally connected to the VMEbus, the time usually required to arbitrate and establish connection between the CPU and the VMEbus or static RAM is drastically reduced.

3.6.3.3 Bus controller logic

The Signetics 8X821/68175 Bus Controller (BUSCON) is a high-speed requester designed to interface to a local bus master (e.g., a DMA controller or microprocessor). The use of the Signetics 8X821/68175 chip ensures that VMEbus specifications are met for arbitration and the timing of bus occupancy and bus vacancy operations. The fast, asynchronous bus grant daisy chain arbiter provides a high performance bus interface. The requester controls all the timed sequencing required for obtaining and using the bus. This includes both strobe and and buffer timing. Consult the "Signetics 8X821/68175 Data Sheet" for additional information.

3.6.3.3.1 Bus release modes

BUSCON supports two modes of bus release: "release-when-done" (RWD) mode and "release-upon-request" (ROR) mode. The IV-1624 supports both modes. "Release-when-done" mode releases the bus after each cycle. "Release-when- done" allows the user to specify whether the bus will be released when the bus is cleared (i.e., BCLR* becomes active) or when a bus request is received. Instructions for selecting the proper mode are included in chapter 4.

In a system configuration where many users are requesting the VMEbus, it may be desirable for a VMEbus user to release the bus as soon as another VMEbus request is received, giving all users equal access to the bus. This mode is supported by the Signetics 8X821/68175 Bus Controller chip ("release-when-done" or "RWD" mode). On the

IV-1624, "RWD" mode is selected by installing a shunt. Complete instructions for shunt installation are presented in chapter 4 (see "Bus release control configuration").

In a system configuration where one user must be given priority

3.6.3.4 Interrupt Structure

The IV-1624 design uses three Signetics Bus Interface family chips to insure high-performance and versatility. The Signetics 8X821/68175 Bus Controller was described in the preceeding section. The other two members of the Signetics 8X824/68155 Interrupt Handler (IVHAN) and the 8X825/68154 Interrupt Generator (IGOR) provide all of the necessary features for efficient interrupt generation and handling.

3.6.3.4.1 IVHAN

IVHAN monitors each of the seven VMEbus interrupt request lines (IRQ1*-IRQ7*) and may be programmed to handle any or all of them. In addition, IVHAN allows a local interrupt, or a general purpose input, on seven additional lines: NMI* and LRQ1-LRQ6*. On the IV-1624 these lines are dedicated to the functions shown in table 3-8.

NOTE:

The IVHAN chip must be properly programmed to recognize interrupts from all local sources. Note that the local devices must also be properly initialized to generate the interrupts requests and to provide interrupt vectors.

NOTE:

If an interrupt driven process is desired, IVHAN must be initialized to the mode implicit in the hardware design.

TABLE 3-8. Interrupt handler inputs

Interrupt	Level	Type	Source	Vector Source	Comments
NMI*	7	VMEbus	ACFAIL*	note 3	note 1
LRQ6*	6	" "	SYSFAIL*	note 3	note 2
LRQ5*	5	Local	TMRIRQ*	note 3	note 2
LRQ4*	4	" "	SIOIRQ01*	note 4	note 2
LRQ3*	3	" "	SIOIRQ23*	note 4	note 2
LRQ2*	2	" "	MAILBOXIRQ*	note 4	note 2
LRQ1*	1	" "	DMAIRQ*	DMAC	note 4

NOTES:

1. Interrupt input is negative-edge triggered.
2. Interrupt input is active low.
3. For system bus responses, IVHAN works with a bus requester to acquire the Status/ID byte (interrupt vector) during an interrupt acknowledge cycle.
4. Interrupting device must supply vector. See "Device-Supplies-Vector" mode description in the Signetics 8X824/68155 Data Sheet.

3.6.3.4.2 IGOR

The Signetics Interrupt Generator (8X825/68154) provides an interface between an interrupting device and the VMEbus. It provides three functions:

[1] IGOR generates bus interrupt requests (IRQ1*-IRQ7*).
[2] IGOR sits in the interrupt acknowledge daisy chain
[3] IGOR allows an interrupt vector to be supplied to the system (if needed).

IGOR provides a vehicle for interprocessor communications on an intelligent peripheral I/O contrller board (e.g., the IV-1624) or a CPU board. IGOR's local data pins (LD1-LD7) serve as an interface to the local data bus, allowing a local master to read or write its two internal registers. During an interrupt acknowledge, IGOR supplies the system with 7 of the 8 status/ID bits comprising the interrupt

vector. For detailed operation instructions, consult the **Signetics 8X825/68154 Data Sheet.**

3.7 Serial port I/O and interface

The IV-1624 contains four Serial Communication Controllers. These devices, Z8530 (Zilog), provide the multifunction support for handling the large variety of serial communication protocols available. The SCC can be programmed to satify special serial communications requirements as well as to follow standard formats such as byte-oriented synchronous, bit-oriented synchronus, ans asynchronous. Once programmed, the SCC relieves the CPU of tasks formerly accomplished by the CPU or its associated hardware.

3.7.1 Operating modes

With access to 14 write registers and 7 read registers per channel, the user can configure the SCC so that can handle all asynchronous formats regardless of data size, number of stop bits or parity requirements. The SCC also accomodates all synchronous formats including character, byte, and bit oriented protocols.

Within each operating mode, the SCC also allows for protocol variations by checking odd or even parity bits, character insertion or deletion, CRC generation and checking, break and abort generation and detection, and many other protocol-dependent features.

The internal registers are accessed through two ports for each channel, control and data. The data port may be read (RR8) and written (WR8) at any time for direct access to the Rx and Tx registers. The status register (RR0) may be read directly by reading the control port. The other registers are accessed by first writting the register number to the control port and then reading data from or writting data to the control port.

Channel 5, 6, 7 and 8 provide a WAIT/REQ signal used to initiate the DMA controller. Channels 7 and 8 also have another DMA request line DTR/REQ which may be connected to

the DMA controller. The configuration section describes the possibilities and their applications.

3.7.2 Interrupts

3.7.2.0.0.1 Serial I/O interrupts

The interrupt requests for the four Z8530 chips are grouped in two pairs. The interrupt outputs of the chips U53 and U54 are wire "OR"ed on level 3 (SIOIRQ01* for channels 1 and 2); U55 and U56 are wire "OR"ed on level 4 (SIOIRQ23* for channels 3 and 4). The Z8530s implement an interrupt acknowledge daisy chain which further prioritizes interrupts from the two levels.

NOTE:

The proper operation of this daisy chain requires that the "Reset Interrupt Under Service" bit command be issued to the Z8530 at the end of the interrupt service routine.

The interrupts from U56 are at a higher priority than those from U55. Similarly, U54 interrupts have priority over U53 interrupts. The Z8530s each internally prioritize 6 different (3 per channel) interrupt conditions and can modify the bits of the interrupt vector to indicate the exact interrupting condition. The user should refer to the Z8530 Technical Manual and data sheet for detailed discussion of interrupt generation.

3.7.2.0.0.1.1 Per channel interrupts

Each channel may generate interrupts based on three conditions. The per channel priority is described in the following table. Two composite interrupts are generated and presented to the interrupt handler, one for channels 1-4 and one for chanels 5-8. The channel priority is sequential the highest being channel 1 and lowest being channel 8.

TABLE 3-9. SCC Interrupt Priority

Event	Priority
Rx ready	highest
Tx ready	
Ext/Status	lowest

3.8 DMA controller

The 68450 DMA controller is available as an option on 10 MHz (12.5 MHz DMA controller chips are not yet available from their manufacturers). The 68450 provides four independent channels, each capable of memory to memory, memory to device, and device to memory transfers. The DMA controller may affect serial I/O data transfers for two channels in full duplex mode, or four channels in half duplex mode. See chapter 4 for complete configuration instructions.

3.8.1 DMA controller performance notes

The Z8530 SIO chips are each capable of one megabit per second data rates on each channel. The processor alone can handle eight channels (full duplex) at up to 19.2 Kbaud. At such a throughput rate, the processor has sufficient time only to move the data and to manage its buffers. Programming the 68450 for data transmission for four channels to should reduce the interrupt overhead by a minimum of 25%. This reduction will free up a similar fraction of CPU bandwidth which can then be applied to preprocessing the received character stream and offloading the host. If two of the data channels are at a much higher baud rate than the remaining channel, a similar result is acheived.

3.8.2 DMAC applications

How, as well as whether or not the DMA controller is applied is dependent upon the overall system architecture. Possible DMAC applications include:

[1] **Message processing:** transferring messages to and from buffer memory on the 1-3 to main system memory or to local memory on another CPU board.

3.8.3 DMAC operation

The DMA controller has an active low interrupt request output which is interfaced to the processor on level 1. It (optionally) requests interrupts when a DMA transfer is completed or when an error condition occurs.

4. IV-1624 CONFIGURATION GUIDE

4.1 Chapter overview

The IV-1624 has twenty onboard shunts for selecting board options. The table below shows shunts grouped according to specific board functions. Detailed installation instructions are included in for each shunt.

TABLE 4-1. IV-1624 shunts

SHUNT FUNCTION	SHUNT NUMBER (J#)																			
	J01	J02	J03	J04	J05	J06	J07	J08	J09	J10	J11	J12	J13	J14	J15	J16	J17	J18	J19	J20
EPROM size	-	-	-	-	-	-	X	-	-	X	-	-	-	-	-	-	-	-	-	-
Static RAM size selection	X	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Dual port base selection	-	-	-	-	X	-	-	-	-	-	-	-	-	-	-	-	-	X	-	-
Dynamic RAM control	-	X	-	X	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Bus release control	-	-	-	-	-	-	-	-	X	-	-	-	-	-	-	-	X	-	-	-
Bus grant level selection	-	-	-	-	-	-	-	-	-	-	-	-	-	X	X	-	-	X	X	
Bus request level selection	-	-	-	-	-	X	-	X	-	-	-	-	-	-	-	-	-	-	-	-
DMA/SIO control	-	-	-	-	-	-	-	-	-	-	X	X	X	X	-	-	-	-	-	-

4.1.1 EPROM shunt options

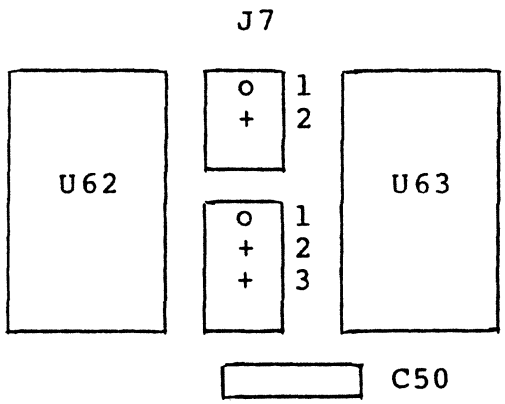
Table 4-2 shows the proper installation for EPROM shunts for each EPROM option. Figure 4-1 shows the board location of each shunt.

TABLE 4-2. EPROM shunt installation matrix

EPROM type	Shunt # J7	J10	J10
2764	out	[1-2] in	[2-3] out
27128	out	[1-2] in	[2-3] out
27256	in*	[1-2] in	[2-3] out
27512	in*	[1-2] out	[2-3] in

* Cut required in addition to jumper change. All cuts are done at the factory

Figure 4-1. EPROM shunt header locations



4.1.2 Dynamic RAM shunt installation

The IV-1624 offers 64K or 256K of onboard dynamic RAM. The following tables show the proper shunt installation for these configurations. Figure 4-1 shows the board location of the dynamic RAM shunts.

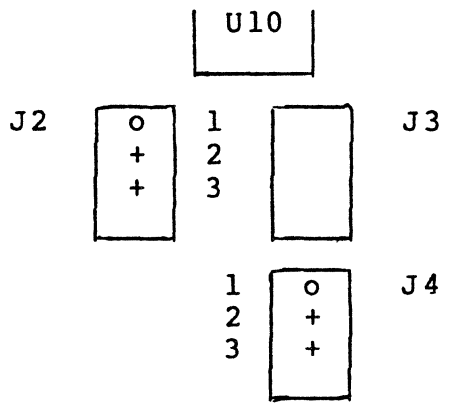
TABLE 4-3. Dynamic RAM shunt installation matrix (J4)

RAM Access time (ns)	Shunt# J4 [1-2]	[2-3]
100	in	out
150	out	in

TABLE 4-4. Dynamic RAM shunt installation matrix (J2)

RAM Size Option	Shunt# J2 [1-2]	[2-3]
64K	in	out
256K	out	in

Figure 4-2. Dynamic RAM shunt locations (J2 and J4)



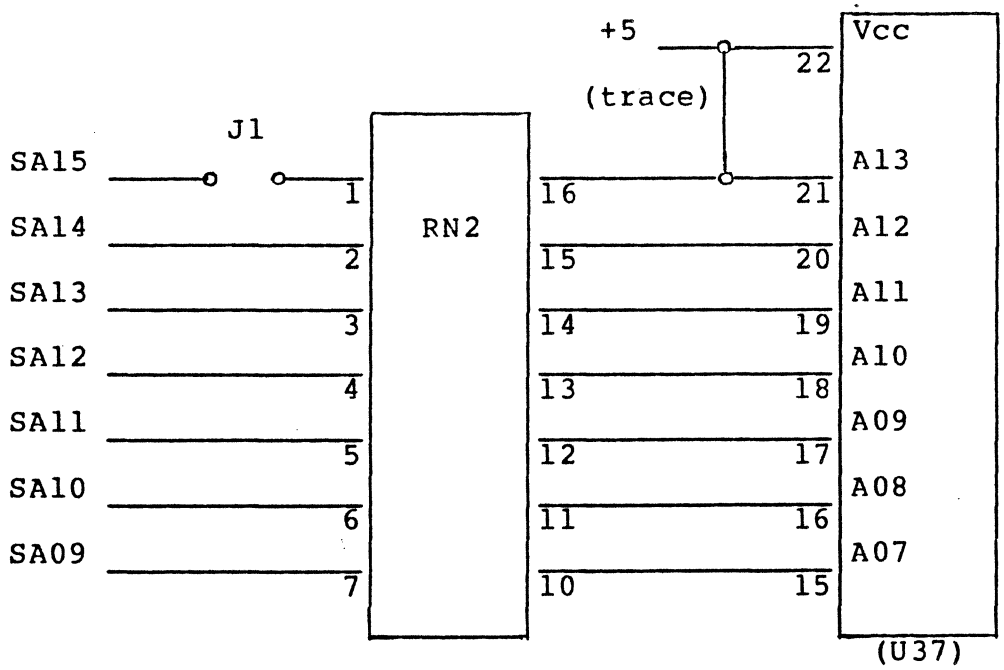
4.1.3 Static RAM shunt installation

The IV-1624 can optionally address 64K or 256K bytes of static RAM using either (4Kx4) or (16Kx4) chips. One shunt header (J1) enables the upper static RAM address line SA15 (see figure 4-3). Please note that the static RAM trace shown in the figure is cut at the factory during RAM installation.

TABLE 4-5. Static RAM shunt installation matrix

RAM type	RAM option	J1
(4Kx4)	16Kx32	[1-2] out
(16Kx4)	64K	[1-2] in

Figure 4-3. Static RAM schematic representation



4.1.4 Dual port RAM shunt installation

Two shunts (J18 and J5) determine the base address of static and dynamic dual port RAM. The addressing options and corresponding shunt installation are shown in the tables below. Note that a 64K address space is always decoded for dual port static RAM, regardless of how much static RAM (16K or 64K) exists. The dynamic RAM dual port address range will be either 64K or 256Kbytes. The following figure shows the location of shunts J18 and J5.

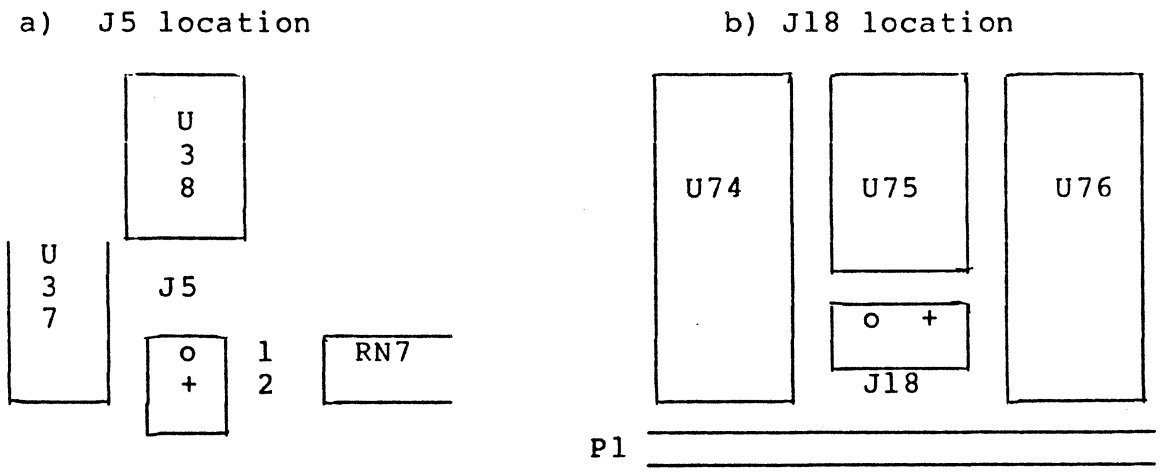
TABLE 4-6. Dual port shunt installation for 64K DRAM option

DRAM Dual Port Range	SRAM Dual Port Range	Shunt# J18	J5
D00000- D0FFFF	F80000- F8FFFF	in	in
D80000- D8FFFF	F90000- F9FFFF	in	out
E00000- E0FFFF	FA0000- FAFFFF	out	in
E80000- E8FFFF	FB0000- FBFFFF	out	out

TABLE 4-7. Dual port shunt installation for 256K option

DRAM Dual Port Range	SRAM Dual Port Range	Shunt# J18	Shunt# J5
D00000-D3FFFF	F80000-F8FFFF	in	in
D80000-DBFFFF	F90000-F9FFFF	in	out
E00000-E3FFFF	FA0000-FAFFFF	out	in
E80000-EBFFFF	FB0000-FBFFFF	out	out

Figure 4-4. Dual port shunt locations



4.1.5 VMEbus shunt installation

Several option for VMEbus control are available on the These options include bus release control options, VMEbus request level selection, and VMEbus grant level selection. More coverage of these topics is included in chapter 3 (Theory of Operation). The following sections illustrate proper shunt installation.

4.1.5.1 Bus release options

Two shunts (J9 and J17) allow the user to specify the conditions under which the VMEbus will be released. (See chapter 3 section on VMEbus control for discussion of control options.

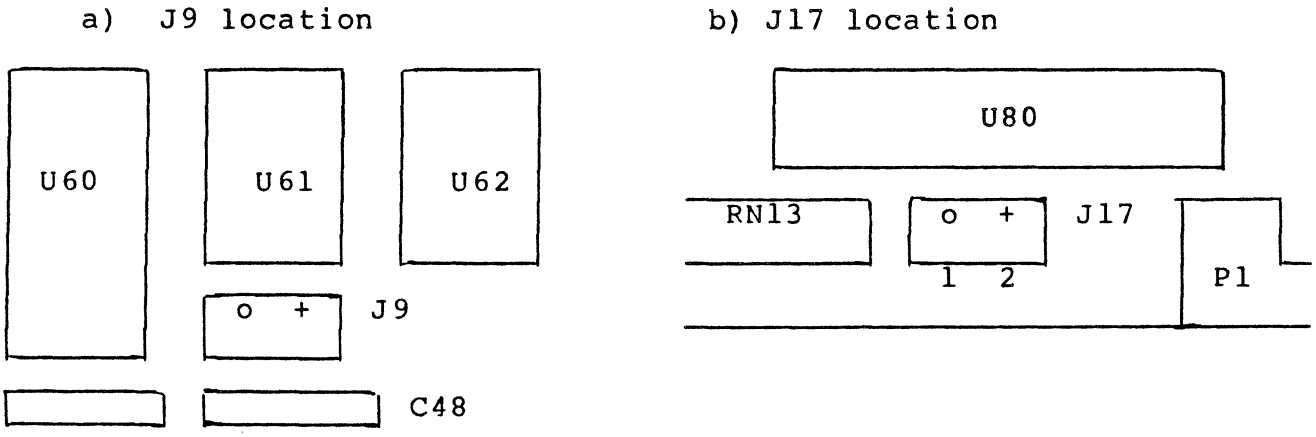
The following table shows the shunt installation matrix for the three selectable bus release conditions. The following figure shows the board location of each shunt.

TABLE 4-8. Bus release shunt installation matrix

Description	Shunt# J9	J17
Release on bus clear	out	in
Release on bus request	in	in
Release every cycle	--	out

-- don't care

Figure 4-5. Bus release shunts (J9 and J17)



4.1.5.2 VMEbus request and grant control

Each board within a system must have a unique bus request and grant level assigned to it. Moreover, an individual board's bus grant and bus request levels must be identitical (e.g., a board is configured to request the VMEbus on level 2; its bus grant level must also be configured to level 2).

Insertion of bus grant and bus request shunts connects the VMEbus to the Signetics Bus Controller (BUSCON) chip, which controls local VMEbus activity. Insertion of the bus grant shunts (BG0*-BG03*) or insertion of the bus request shunts (BR0*-BR3*) selects one of four levels. The four levels are assigned priority in descending order (i.e., level 3 being the highest priority level).

To assign bus grant level, refer to the following table. Set the level shunt to a "daisy chained" configuration and set all other levels to "pass through" their bus grant signals.

TABLE 4-9. VMEbus grant level selection shunt installation

Description	Shunt Number	Pin Number [1-2]	[2-3]	[3-4]
Daisy chain (level 0)	J16	in	out	in
Pass through (level 0)	J16	out	in	out
Daisy chain (level 1)	J20	in	out	in
Pass through (level 1)	J20	out	in	out
Daisy chain (level 2)	J19	in	out	in
Pass through (level 2)	J19	out	in	out
Daisy chain (level 3)	J15	in	out	in
Pass through (level 3)	J15	out	in	out

To assign a bus request level, refer to the following table. Insert the appropriate bus request shunt.

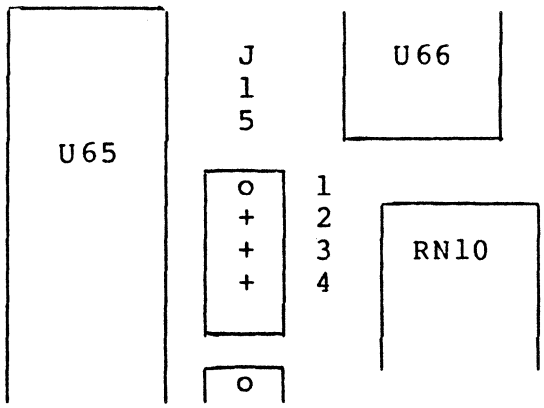
TABLE 4-10. VMEbus request level selection

Description	#J6		#J8	
	[1-2]	[2-3]	[1-2]	[2-3]
Bus request (level 0)	out	in	out	out
Bus request (level 1)	in	out	out	out
Bus request (level 2)	out	out	out	out
Bus request (level 3)	out	out	out	in

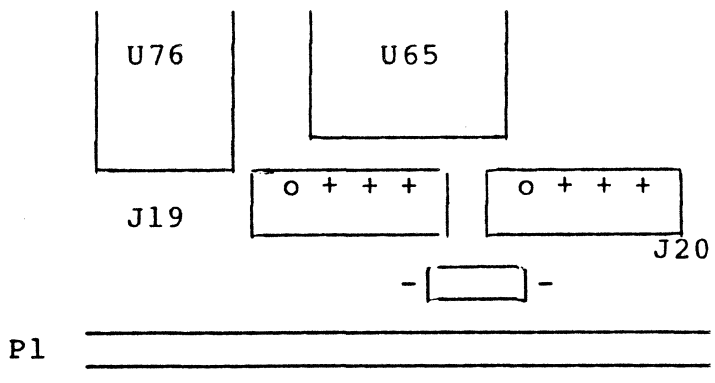
The following figures show the locations of bus grant and request shunts.

Figure 4-6. Bus grant shunts

a) J15 location



b) J19 and J20 locations



4.1.6 Serial and DMA controller shunt installation

The IV-1624 can be programmed to provide four channels of half-duplex I/O without DMA or two channels of full duplex serial I/O with DMA. The Z8530 SIO pins 10 and 30 must be initialized to provide full modem control if not DMA is desired, or to act as DMA request lines by inserting two shunts.

4.1.6.1 Serial I/O shunt configuration

The following table shows the proper shunt installation to provide serial port operation without DMA.

TABLE 4-11. Shunt installation for serial I/O without DMA

Shunt			
J11	J12	J13	J14
---	---	in	in

--- don't care

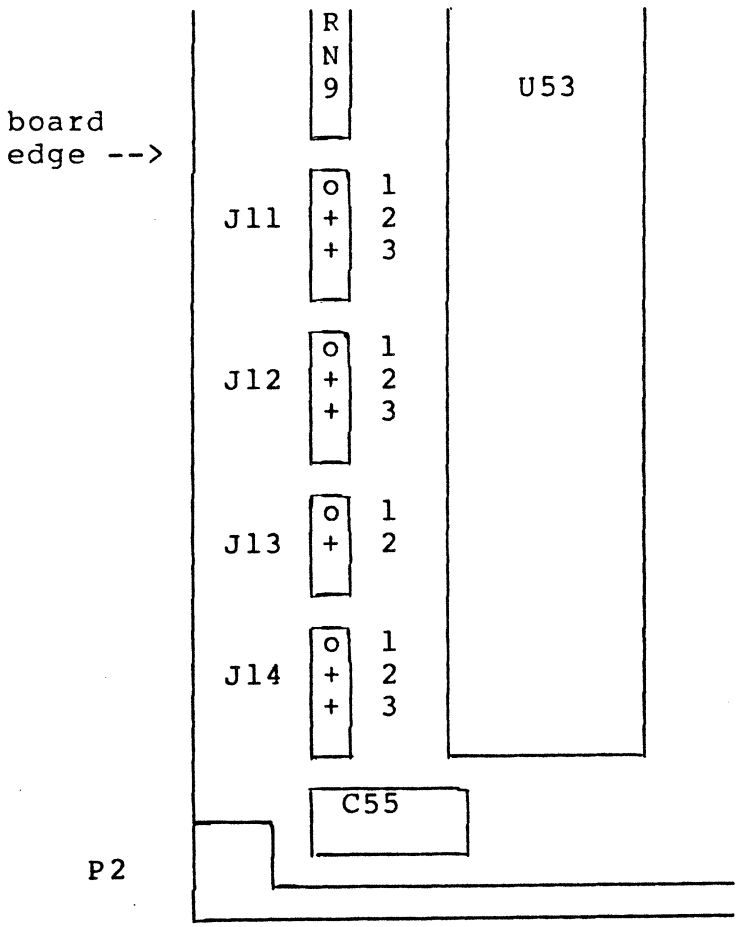
The following table shows the shunt installation required to provide serial I/O in half- or full-duplex modes.

TABLE 4-12. Half duplex and full duplex mode shunt installation

Mode	J11		J12		J13	J14
	[1-2]	[2-3]	[1-2]	[2-3]		
half-duplex	in	out	in	out	in	in
full-duplex	out	in	out	in	out	out

The following figure shows the location of all serial I/O and DMA shunt (J11-J14).

Figure 4-7. Location of serial I/O and DMA shunts



5. IV-1624 1.1 PARTS LIST

TABLE 5-1. Abbreviations for manufacturers

Abbreviation	Manufacturer
AMD	Advanced Micro Devices
APT	APTR
AUG	Augat
AVX	AVX
BEL	BEL
BOU	Bourns
CAM	Cambion
CEN	Centralab
CTS	CTS Corporation
EC2	EC2 Incorporated
ERN	Erni
FUJ	Fujitsu
GI	General Instruments
HIT	Hitachi
IDT	Integrated Device Technologies
IRO	Ironics
ILL	Illinois Capacitor
INT	Intel
MET	Methode
MIC	Micron
MM	Monolithic Memories
MOS	Mostek
MOT	Motorola
MUP	Mupac
NAT	National Semiconductor
NEC	NEC
SAM	Samtec
SIG	Signetics Corporation
TI	Texas Instruments

5.1 Core assembly

5.1.1 Integrated Circuits

Brackets () indicate an alternate component selection.

Loc No.	Manu	Manufacturer's Part No.	Ironics Part No.	Description
U1	SIG	74LS375	441-375	Transparent latch
U2-U9	---	see dynamic RAM option section ---		
U10	CAM	703-4220-01-04-01	335-020	20-pin socket
U10	SIG	82S153A	450-154	PLA 510
U11	SIG	74LS393	441-393	Binary ripple counter
U12	MOT	MC68B40	461-007	Counter/timer
U13	SAM	SS-132-T-2	338-015	12-pin socket strips
U13	AMD	AMPAL22V10ADC	450-000	PAL (503) (.3")
U14	SIG	74LS164	441-164	8-bit shift reg
U15	SIG	74LS161	441-161	4-bit counter
U16	TI	74AS258	449-258	Address MUX
U17	SIG	74F02	444-002	2-input NOR
U18	TI	74AS258	449-258	Address MUX
U19-U20	SIG	74F245	444-245	Octal transceiver
U21-U24	---	see static RAM option section ---		
U25	SAM	SS-132-T-2	338-015	2 10-pin socket strips
U25	SIG	82S152	450-152	PLA 501

U26	SAM	SS-132-T-2	338-015	2 10-pin socket strips
U26	SIG	82S153	450-153	PLA 518
U27	SAM	SS-132-T-2	338-015	2 10-pin socket strips
U27	SIG	82S159	450-159	PLS 50F
U28-U29	SIG	74LS245	441-245	
U30	SIG	74LS373	441-373	Octal latch
U31	CAM	703-4220-01-04-01	335-020	20-pin socket
U31	SIG	82S153	450-153	PLA 50C
U32	SIG	74LS373	441-373	Octal latch
U33	CAM	703-4220-01--04-01	335-020	20-pin socket
U33	SIG	82S153	450-153	PLA 50D
U34	EC2	MTTLDL-15	620-015	Triple 15 ns delay line
U35	EC2	MTTLDL-50	621-000	Triple 50 ns delay line
U36-	SAM	SS-132-T-2	335-015	2 14-pin socket strips
U36-	---	See EPROM option section ---		
U37	SAM	SS-132-T-2	338-015	2 14-pin socket strips
U37-	---	See EPROM option section ---		
U38	CAM	703-4220-01 --04-01	335-020	socket
U38	SIG	82S153A or	450-154	PLA 504
U39-U40	SIG	74F245	444-245	Octal transceiver
U41-U44	---	See option sheet for static RAM selection --		
U45	---	See DMA controller option --		
U46	AUG	#PGM68-1A-1005-L	335-068	PGA socket
	(AUG	#PPS68-1A-1005-L	335-068	PGA socket)
U46	--	See CPU option section --		
U47	CAM	703-4220-01--04-01	335-020	socket

U47	--	see dynamic RAM option section ---		
U48-U49	SIG	74F245	444-245	Octal transceiver
U50	SIG	74F132	444-132	Schmitt trigger
U51	EC2	MTTLDL-35	620-035	Triple 35 ns-delay line
U52	SIG	74F74	444-074	D-type flipflop
U53-U56	AMD (ZIL	AMZ8530APC Z8530	462-039	6 MHz Serial I/O controller 6 MHz Serial I/O controller)
U57	SIG	74F244	444-244	Tristate buffer
U58	CAM	703-4240-01--04-01	335-020	socket
U58	SIG	SCN68155	462-041	VME interrupt handler (8X824)
U59-U60	SIG	74F245	444-245	Octal transceiver
U61	TI	74AS257	449-257	Tristate MUX
U62	SIG	74F245	444-245	Octal transceiver
U63	SIG	74F244	444-244	Tristate buffers
U64	SAM	SS-132-T-2	338-015	2 12-pin socket strips
U64	SIG	SCN68175 (.4")	462-042	Bus controller (8X821)
U65	CAM	703-4240-01--04-01	335-020	socket
U65	SIG	SCN68154	462-043	VME interrupter (8X825)
U66	SIG	74F244	444-244	Tristate buffer
U67-U68	SIG	74F245	444-245	Octal transceiver
U69	SIG	74F10	444-010	3-input NAND
U70-U71	SIG	74F245	444-245	Octal transceiver
U72	SIG (TI	74F621 or 74AS621	444-621	Bus transceiver)

U73	CAM	703-4220-01--04-01	335-020	socket
U73	SIG	82S153	450-153	PLA 51A
U73	CAM	703-4220-01--04-01	335-020	socket
U74	---	See dynamic RAM option section ----		
U75	SIG	74F32	444-032	Quad 2-input OR
U76	SIG	74F244	444-244	Octal buffer
U77-U78	SIG	74F245	444-245	Octal transceiver
U79	SIG	74F08	444-008	2-input AND
U80	SIG	74F38	444-038	Quad 2-inpt NAND
U81	CAM	703-4220-01--04-01	335-020	socket
U81	SIG	82S153	450-153	PLA 51B

5.1.2 Resistor networks and sips

Brackets () indicate an alternate component selection.

Loc No.	Manu	Manufacturer's Part No.	Ironics Part No.	Description
RN1, RN9	BOU	4610X-101-222	604-012	2.2K 10-pin SIP
RN4-RN5	BOU	4116R-064-200-102	604-009	(20 ohm x 1K RN)
RN2-RN3, RN8, RN10-RN13	BOU	4610X-101-472	604-007	4.7K 10-pin SIP
RN6-RN7	BOU	4116-001-330	604-004	8 resistor pack (33 ohm)

5.1.3 Resistors

Brackets () indicate an alternate component selection.

Loc No.	Manu	Manufacturer's Part No.	Ironics Part No.	Description
R1, R2	----		600-471	470 ohm 1/4W 5%
R3			600-472	4.7 Kohm 1/4W 5%
R5			602-560	56 ohm 1/2W 5%
R7			600-241	240 ohm 1/4W 5%
R4, R6			600-102	1 Kohm 1/4W 5%
R8			600-101	100 ohm 1/4W 5%

5.1.4 Diodes

Brackets () indicate an alternate component selection.

Loc No.	Manu	Manufacturer's Part No.	Ironics Part No.	Description
DS1	TI	TIL220	410-000	"HALT" LED (red)
DS2	GI	MV5454A	410-008	"FAIL" LED (green)
CR1	MOT	1N4001	400-000	Diode

5.1.5 Capacitors

Brackets () indicate an alternate component selection.

Loc No.	Manu	Manufacturer's Part No.	Ironics Part No.	Description
C27, C56, C55	ILL	#476RSS016M	614-466	47uF 16V rad lead electrolytic (case dia: 0.248; 0.098 lead spacing)
C29	---	See EPROM option section		-----
C35	CEN	DD-470	611-470	100 pF disc ceramic 10% (0.25" lead spacing)
C1-C26, C28, C30-C34, C36-C55	AVX	MD015E10-4ZAA	610-104	.1 uF dipguard (0.3" lead spacing

5.1.6 Miscellaneous

Brackets () indicate an alternate component selection.

Loc No.	Manu	Manufacturer's Part No.	Ironics Part No.	Description
---	IRO	C01-1209 rev 1.0	303-035	PC board
---	BIC	174-12934F &	860-004	Bezel with 2-holes &
	BIC	173-12525B	860-003	Bezel hardware
P1, P2	ERN	533-602	332-000	DIN 96-pin right angle connectors
	---			Shunts (20)
J1, J5, J7,J9, J13,J14,J17,J18,J21	APT	9298-3401-36	334-015	2 x 1 shunt headers (0.324H x 0.1 ctr)
J2, J3, J4, J6,J8, J10,J11,J12,J22	APT	9298-3401-36	334-015	3 x 1 shunt headers (0.324H x 0.1 ctr)
J15, J16, J19,J20	APT	9298-3401-36	334-015	4 x 1 shunt headers (0.324H x 0.1 ctr)

5.2 Option section

5.2.1 10 MHz CPU option

Brackets () indicate an alternate component selection.

Loc No.	Manu	Manufacturer's Part No.	Ironics Part No.	Description
U46	MOT	MC68010R10	461-018	CPU
Y1	CTS	MX0-55-2-19.6608 MHz	631-019	19.6608 MHz oscillator

5.2.2 12 MHz 68010 CPU option

Brackets () indicate an alternate component selection.

Loc No.	Manu	Manufacturer's Part No.	Ironics Part No.	Description
U46	MOT	MC68010R12	461-019	CPU
Y1	CTS	MX0-55-2-24 MHz	631-024	24 MHz oscillator

5.2.3 64K dynamic RAM option (8 or 10 MHz CPU)

Brackets () indicate an alternate component selection.

Loc No.	Manu	Manufacturer's Part No.	Ironics Part No.	Description
U2-U9	FUJ	MB81416-15	470-015	Dynamic RAM
	(INM	IMS2620-15)		
U74	SIG	82S153A (505)	450-153	PLA
U47	SIG	82S153A (50E)	450-153	PLA

5.2.4 64K dynamic RAM option (12.5 MHz CPU)

Brackets () indicate an alternate component selection.

Loc No.	Manu	Manufacturer's Part No.	Ironics Part No.	Description
U2-U9	FUJ	MB81416-10	470-003	Dynamic RAM
	(INM	IMS2620-10		)
U74	SIG	82S153A (505)	450-153	PLA
U47	SIG	82S153A (50E)	450-153	PLA

5.2.5 256K dynamic RAM option (10 MHz)

Brackets () indicate an alternate component selection.

Loc No.	Manu	Manufacturer's Part No.	Ironics Part No.	Description
U2-	FUJ	MB81464-15	470-013	
U9	(TI	TMS4464-15		)
	(NEC	UPD41254-15		)
	(HIT	HM50464-15		)
U74	SIG	82S153A (505)	450-153	PLA
U47	SIG	82S153A (50E)	450-153	PLA

5.2.6 256K dynamic RAM option (12.5 MHz CPU)

Brackets () indicate an alternate component selection.

Loc No.	Manu	Manufacturer's Part No.	Ironics Part No.	Description
U2-	FUJ	MB81464-10	470-012	
U9	(TI	TMS4464-10		)
	(NEC	UPD41254-10		)
	(HIT	HM50464-10		)
U74	SIG	82S153A (505)	450-153	PLA
U47	SIG	82S153A (50E)	450-153	PLA

5.2.7 (4Kx32) static RAM option (10 MHz CPU)

Brackets () indicate an alternate component selection.

Loc No.	Manu	Manufacturer's Part No.	Ironics Part No.	Description
U21-U24; U41-U44	AMD INM IDT	AM2168-55 or IMS1420-55 or IDT6168-55	471-002	Static RAM (see note below)

Note:

Static RAM are soldered into bottom 20 pins of a 22-pin slot (pins 1 and 22 should be empty)

5.2.8 (4Kx32) static RAM option (12.5 MHz CPU)

Brackets () indicate an alternate component selection.

Loc No.	Manu	Manufacturer's Part No.	Ironics Part No.	Description
U21-U24; U41-U44	AMD (INM (IDT	AM2168-45 IMS1420-45 IDT6168-45	471-001	Static RAM (see note below)))

Note:
Static RAM are soldered into bottom 20 pins of a 22-pin slot (pins 1 and 22 should be empty)

5.2.9 DMA Controller option (10 MHz)

Brackets () indicate an alternate component selection.

Loc No.	Manu	Manufacturer's Part No.	Ironics Part No.	Description
U45	HIT	HD68450-Y10	461-012	DMA controller
U45	AUG	#PGM68-1A-1006-L	335-068	socket
U28-U29;	SIG	74LS245	441-245	
U30-U32	SIG	74LS373	441-373	

5.2.10 No DMA Controller option

Brackets () indicate an alternate component selection.

Loc No.	Manu	Manufacturer's Part No.	Ironics Part No.	Description
U45		--no chip--	-------	
U28-U29;		--no chip--	-------	
U30-U32		--no chip--	-------	

5.2.11 2764 EPROM option (10 MHz CPU; 0 wait state)

Brackets () indicate an alternate component selection.

Loc No.	Manu	Manufacturer's Part No.	Ironics Part No.	Description
U36-U37	---	To be specified	-------	EPROM (170 ns access time or less)
C29	---	no chip --		

5.2.12 2764 EPROM option (10 or 12.5 MHz CPU; 1 wait state)

Brackets () indicate an alternate component selection.

Loc No.	Manu	Manufacturer's Part No.	Ironics Part No.	Description
U36-U37	AMD	AM2764-2	472-064	EPROM (200 ns) 5 %
C29	CEN	DD-101	611-101	100 pF disc ceramic 10% (0.25" lead spacing)

5.2.13 27128 EPROM option (10 MHz; 0 wait state)

Brackets () indicate an alternate component selection.

Loc No.	Manu	Manufacturer's Part No.	Ironics Part No.	Description
U36-U37	---	To be specified	-------	EPROM (170 ns access time or less)
C29	---	No chip	--	

5.2.14 27128 EPROM option (10 or 12.5 MHz; 1 wait state)

Brackets () indicate an alternate component selection.

Loc No.	Manu	Manufacturer's Part No.	Ironics Part No.	Description
U36-U37	AMD	AM27128-2	472-071	EPROM (200 ns) 5%
C29	CEN	DD-101	611-101	100 pF disc ceramic 10% (0.25" lead spacing)

5.2.15 27256 EPROM option (10 MHz CPU; 0 wait state)

Brackets () indicate an alternate component selection.

Loc No.	Manu	Manufacturer's Part No.	Ironics Part No.	Description
U36-U37	---	To be specified	-------	EPROM (170 ns or less)
C29	---	No chip ----		

5.2.16 27256 EPROM option (10 or 12.5 MHz CPU; 1 wait state)

Brackets () indicate an alternate component selection.

Loc No.	Manu	Manufacturer's Part No.	Ironics Part No.	Description
U36-U37	AMD	AM27256-2	470-072	EPROM (200 ns) 5%
C29	CEN	DD-101	611-101	100 pF disc ceramic 10% (0.25" lead spacing)

5.2.17 27512 EPROM option (10 MHz CPU; 0 wait state)

Brackets () indicate an alternate component selection.

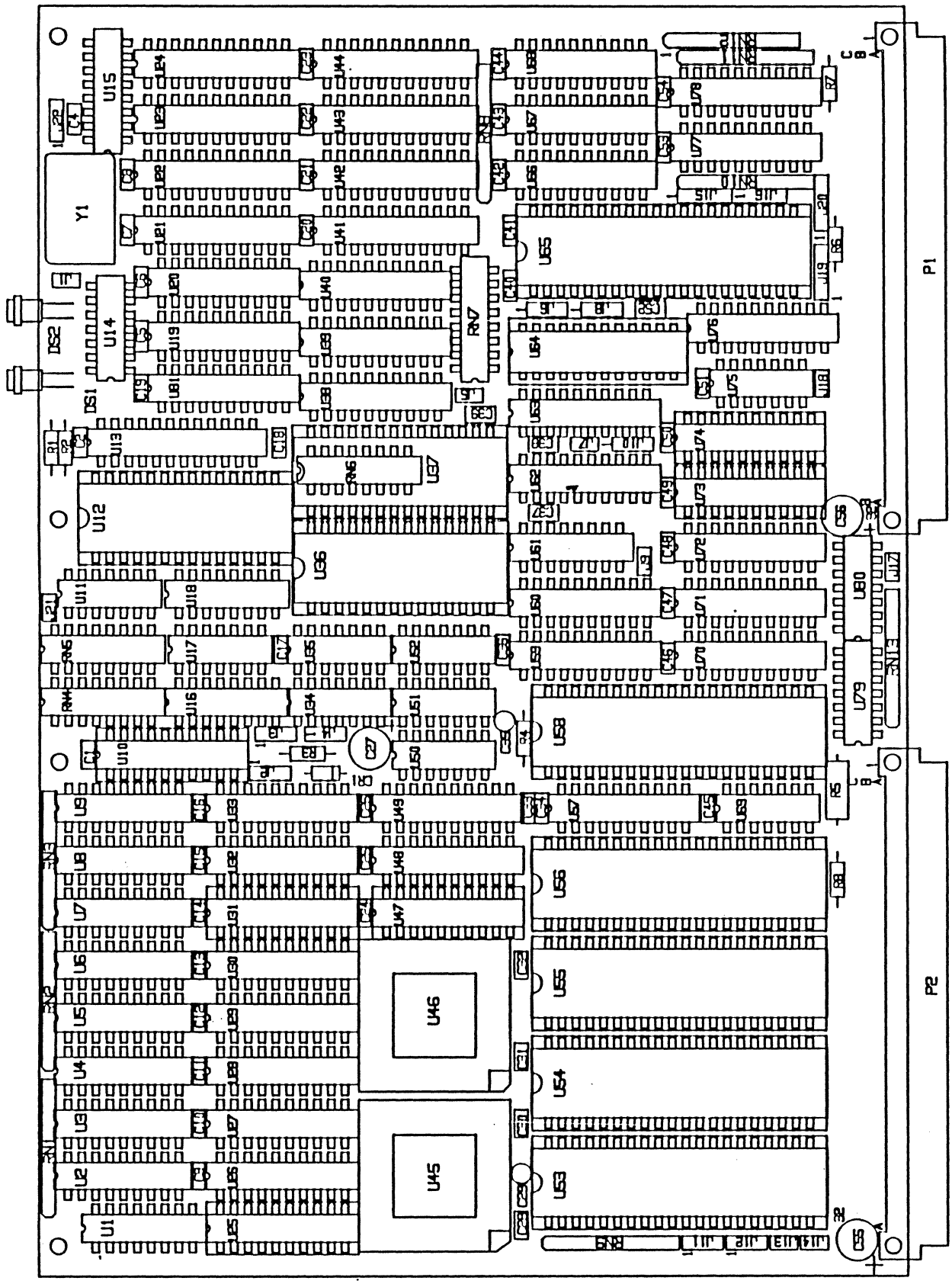
Loc No.	Manu	Manufacturer's Part No.	Ironics Part No.	Description
U36-U37	---	To be specified	-------	EPROM (170 ns) 5%
C29	---	No chip ----		

5.2.18 27512 EPROM option (10 or 12.5 MHz CPU; 1 wait state)

Brackets () indicate an alternate component selection.

Loc No.	Manu	Manufacturer's Part No.	Ironics Part No.	Description
U36-U37	---	To be specified	-------	EPROM (200 ns) 5%
C29	CEN	DD-101	611-101	100 pF disc ceramic 10% (0.25" lead spacing)

5.3 IV1624 component layout diagram (1X)



Appendix A IV-1624 features

This appendix provides a quick summary of IV-1624 features and specifications. VMEbus electrical and mechanical characteristics, as well as protocols and terminology are defined in the VMEbus Specification (Revision B) published by the VME User's Group. It is recommended that all users of IRONICS products obtain these manuals and familiarize themselves with these standards.

A.1 Physical specifications

[1] Physical size: Double Eurocard format
[2] Power consumption: 5V @ 5A typical
[3] P1/P2 connectors: DIN 603-2-IEC-C096M

A.2 Environmental specifications

The following operating conditions are recommended to achieve optimum performance levels:

[1] Temperature: 0-55 C
[2] Humidity: 0-85% non-condensing

A.3 Optional features

The following are optional features of the IV-1624 8-Port Serial I/O board:

[1] MC68010 CPU at 10 or 12.5 Mhz
[2] DMA Controller:

- 10 MHz only
- usable for full duplex on 2 channels, half duplex on 4 channels or independent of serial I/O operations
- use 68450 for 4 channels of memory-to-memory or device-to-memory in 16 Mbyte space
- DMAC may transfer over VMEbus

[3] Local Memory:

Type	Amount	#waits, local	#waits, VMEbus
DRAM	64K, 256K	0	3-7
SRAM	4K X 32	0	1
EPROM	8K to 64K X 16	*note	not dual ported

*note : User supplied 170 ns for 0 wait states at 10 Mhz
or 250 ns for 1 wait state at 10 Mhz

A.4 Standard features

The following are standard features of the IV-1624 8 Port Intelligent Serial I/O board:

[1] Serial I/O:

- 4 Z8530 SCC protocol controllers
- Async,bisync,or SDLC protocols
- Capable of 8 channels of full duplex ASYNC at 19.2 Kbaud
- Serial I/O from IV-1624 is at TTL levels on user I/O lines of P2 to/from IRONICS Electrical Interface Adapters. Interface adapters support the following protocols:

  - RS232 (DTE or DCE)
  - RS449 (DTE)
  - Current loop

  These line driver/receiver paddle boards mound directly to the rear panel of your chassis via their D-shell connectors. Full mode m control and clock options available on each channel.

[2] 4K/16Kx32 Dual Port Static RAM
[3] Two Bytewide EPROM sockets
[4] MC68B40 counter/timer:

- 1 channel dedicated to watchdog timer
- 2 channels dedicated to user application

[5] SC68155 (8X824) Interrupt handler
[6] SC68154 (8X825) Interrupter

[7] Local Interrupts:

level	source
7	ACFAIL*
6	SYSFAIL*
5	TIMER
4	SCC0 and SCC1
3	SCC2 and SCC3
2	Mailbox interrupt
1	DMA Controller

[8] VMEbus Interface:

DTB Master	A24, A16, D16, D8
DTB Slave	A24, D32, D16, D8
Interrupter	levels 1-7, dynamic
Interrupt Handler	levels 1-7, dynamic

[9] Indicators:

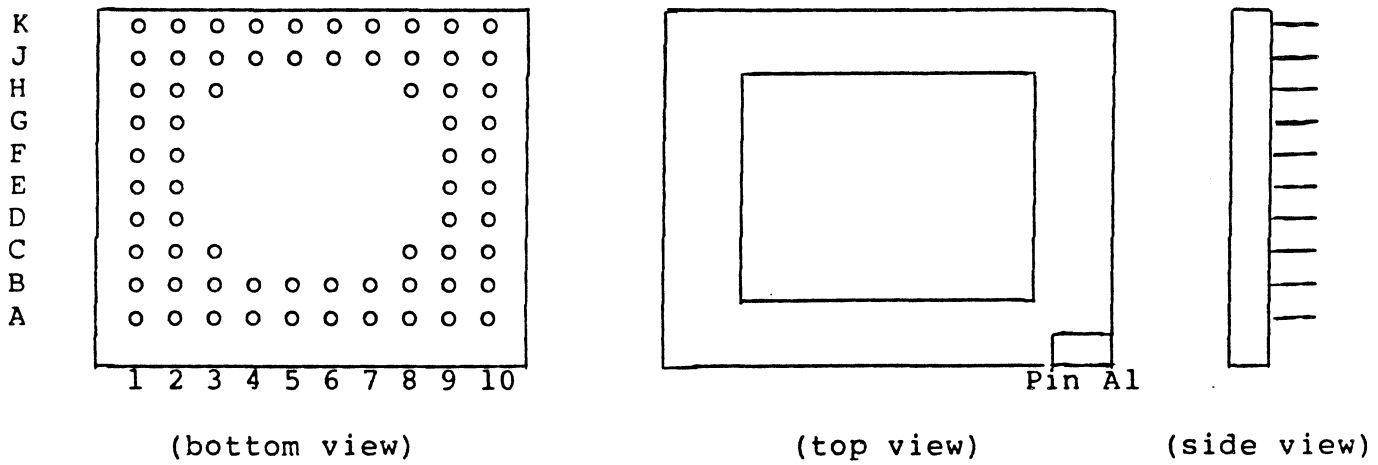
- "Failed" LED
- "Halted" LED

[10] Onboard programmable devices:

- MC68010 CPU
- MC68B40 PTM
- SC68155 (8X824) IVHAN
- SC68154 (8X825) IGOR
- SC68175 (8X821) BUSCON
- Four Z8530 SIO controller
- MC68450 DMA controller

Appendix B 68010 data

Figure B-1. Socket layout and footprint



(bottom view) (top view) (side view)

TABLE B-1. 68010 68-Terminal PGA pin designations

PIN NUMBER	FUNCTION	PIN NUMBER	FUNCTION
A1	Do not connect	F1	HALT*
A2	AS*	F2	RESET*
A3	D1	F9	A18
A4	D2	F10	A19
A5	D4	G1	VMA*
A6	D5	G2	VPA*
A7	D7	G9	A15
A8	D8	G10	A17
A9	D10	H1	E
A10	D12	H2	IPL2*
B1	DTACK*	H3	IPL1*
B2	LDS*	H8	A13
B3	UDS*	H9	A12
B4	D0	H10	A16
B5	D3	J1	BERR*
B6	D6	J2	IPL0*
B7	D9	J3	FC1
B8	D11	J4	Do not connect
B9	D13	J5	A2
B10	D15	J6	A5
C1	BGACK*	J7	A8
C2	BG*	J8	A10
C3	R/W*	J9	A11
C8	D13	J10	A14
C9	A23	K1	Do not connect
C10	A22	K2	FC2
D1	BR*	K3	FC0
D2	Vcc	K4	A1
D9	Vss	K5	A3
D10	A21	K6	A4
E1	CLK	K7	A6
E2	Vss	K8	A7
E9	Vcc	K9	A9
E10	A20	K10	Do not connect

Appendix C VMEbus backplane pin assignments

TABLE C-1. VMEbus J1/P1 Row A Pin Assignments

Pin	VMEbus Spec Assignment	IV-1624 Signal Assignment
A1	D00	D00
A2	D01	D01
A3	D02	D02
A4	D03	D03
A5	D04	D04
A6	D05	D05
A7	D06	D06
A8	D07	D07
A9	GND	GND
A10	SYSCLK	not used
A11	GND	GND
A12	DS1*	DS1*
A13	DS0*	DS0*
A14	WRITE*	WRITE*
A15	GND	GND
A16	DTACK*	DTACK*
A17	GND	GND
A18	AS*	AS*
A19	GND	GND
A20	IACK*	IACK*
A21	IACKIN*	IACKIN*
A22	IACKOUT*	IACKOUT*
A23	AM4	AM4
A24	A07	A07
A25	A06	A06
A26	A05	A05
A27	A04	A04
A28	A03	A03
A29	A02	A02
A30	A01	A01
A31	-12V	not used
A32	+5V	+5V

TABLE C-2. VMEbus J1/P1 Row B Pin Assignments

Pin	VMEbus Spec Assignment	IV-1624 Signal Assignment
B1	BBSY*	BBSY*
B2	BCLR*	BCLR*
B3	ACFAIL*	ACFAIL*
B4	BG0IN*	BG0IN*
B5	BG0OUT*	BG0OUT*
B6	BG1IN*	BG1IN*
B7	BG1OUT*	BG1OUT*
B8	BG2IN*	BG2IN*
B9	BG2OUT*	BG2OUT*
B10	BG3IN*	BG3IN*
B11	BG3OUT	BG3OUT*
B12	BR0*	BR0*
B13	BR1*	BR1*
B14	BR2*	BR2*
B15	BR3*	BR3*
B16	AM0	AM0
B17	AM1	AM1
B18	AM2	AM2
B19	AM3	AM3
B20	GND	GND
B21	SERCLK	GND
B22	SERDAT*	DTACK*
B23	GND	GND
B24	IRQ7*	IRQ7*
B25	IRQ6*	IRQ6*
B26	IRQ5*	IRQ5*
B27	IRQ4*	IRQ4*
B28	IRQ3*	IRQ3*
B29	IRQ2*	IRQ2*
B30	IRQ1*	IRQ1*
B31	+5V STDBY	not used
B32	+5V	+5V

TABLE C-3. VMEbus J1/P1 Row C Pin Assignment

Pin	VMEbus Spec Assignment	IV-1624 Signal Assignment
C1	D08	D08
C2	D09	D09
C3	D10	D10
C4	D11	D11
C5	D12	D12
C6	D13	D13
C7	D14	D14
C8	D15	D15
C9	GND	GND
C10	SYSFAIL*	SYSFAIL*
C11	BERR*	BERR*
C12	SYSRESET*	SYSRESET*
C13	LWORD*	LWORD*
C14	AM5	AM5
C15	A23	A23
C16	A22	A22
C17	A21	A21
C18	A20	A20
C19	A19	A19
C20	A18	A18
C21	A17	A17
C22	A16	A16
C23	A15	A15
C24	A14	A14
C25	A13	A13
C26	A12	A12
C27	A11	A11
C28	A10	A10
C29	A09	A09
C30	A08	A08
C31	+12V	not used
C32	+5V	+5V

TABLE C-4. VMEbus J2/P2 Row B Pin Assignments

Pin	VMEbus Spec Assignment	IV-1624 Signal Assignment
B1	+5V	+5V
B2	GND	GND
B3	RESERVED	not used
B4	A24	not used
B5	A25	not used
B6	A26	not used
B7	A27	not used
B8	A28	not used
B9	A29	not used
B10	A30	not used
B11	A31	not used
B12	GND	GND
B13	+5V	+5V
B14	D16	D16
B15	D17	D17
B16	D18	D18
B17	D19	D19
B18	D20	D20
B19	D21	D21
B20	D22	D22
B21	D23	D23
B22	GND	GND
B23	D24	D24
B24	D25	D25
B25	D26	D26
B26	D27	D27
B27	D28	D28
B28	D29	D29
B29	D30	D30
B30	D31	D31
B31	GND	GND
B32	+5V	+5V

Appendix D User-defined I/O backplane pin assignments

TABLE D-1. J2/P2 Row A Pin Assignments

Pin	VMEbus Spec Assignment	IV-1624 Signal Assignment
A1	user-defined	RxDA (channel 1)
A2	user-defined	TxDA " "
A3	user-defined	CTSA " "
A4	user-defined	RTSA " "
A5	user-defined	DTR/RQA " "
A6	user-defined	DCDA " "
A7	user-defined	TxCA " "
A8	user-defined	RxCA " "
A9	user-defined	RxDA (channel 3)
A10	user-defined	TxDA " "
A11	user-defined	CTSA " "
A12	user-defined	RTSA " "
A13	user-defined	DTR/RQA " "
A14	user-defined	DCDA " "
A15	user-defined	TxCA " "
A16	user-defined	RxCA " "
A17	user-defined	RxDA (channel 5)
A18	user-defined	TxDA " "
A19	user-defined	CTSA " "
A20	user-defined	RTSA " "
A21	user-defined	DTR/RQA " "
A22	user-defined	DCDA " "
A23	user-defined	TxCA " "
A24	user-defined	RxCA " "
A25	user-defined	RxDA (channel 7)
A26	user-defined	TxDA " "
A27	user-defined	CTSA " "
A28	user-defined	RTSA " "
A29	user-defined	DTR/RQA " "
A30	user-defined	DCDA " "
A31	user-defined	TxCA " "
A32	user-defined	RxCA " "

TABLE D-2. J2/P2 Row C Pin Assignments

Pin	VMEbus Spec	IV-1624 Signal
A1	user-defined	RxDB (channel 2)
A2	user-defined	TxDB " "
A3	user-defined	CTSB " "
A4	user-defined	RTSB " "
A5	user-defined	DTR/RQB " "
A6	user-defined	DCDB " "
A7	user-defined	TxCB " "
A8	user-defined	RxCB " "
A9	user-defined	RxDB (channel 4)
A10	user-defined	TxDB " "
A11	user-defined	CTSB " "
A12	user-defined	RTSB " "
A13	user-defined	DTR/RQB " "
A14	user-defined	DCDB " "
A15	user-defined	TxCB " "
A16	user-defined	RxCB " "
A17	user-defined	RxDB (channel 6)
A18	user-defined	TxDB " "
A19	user-defined	CTSB " "
A20	user-defined	RTSB " "
A21	user-defined	DTR/RQB " "
A22	user-defined	DCDB " "
A23	user-defined	TxCB " "
A24	user-defined	RxCB " "
A25	user-defined	RxDB (channel 8)
A26	user-defined	TxDB " "
A27	user-defined	CTSB " "
A28	user-defined	RTSB " "
A29	user-defined	DTR/RQB " "
A30	user-defined	DCDB " "
A31	user-defined	TxCB " "
A32	user-defined	RxCB " "

Appendix E Selected PLA logic tables

E.1 IV-1601/1624 Reset-retry PLA

PLA number : 501.0
PLA type : 82S152
Revision date : 03/27/85
Status : current
Location (U#) : U22/U25
Application note:

Signal	active level	pin
SYSRES*	L	I7
EPROM*	L	I6
RETRY*	L	I5
OFFBD*	L	I4
AS	L	I3
IACK*	L	I2
BTO RC	H	I1
STBDIS	H	I0
LDTACK*	L	B9
LBERR*	L	B8
RESET*	L	B7
HALT*	L	B6
CYCLE END	L	B5
IACKAS	L	B4
force ROM*	L	B3
CLR/ BTO CNTR (AS/)/	H	B2
EPROM DTACK delay RC	H	B1
RESET time constant	H	B0

```
*POL LLLLLLLHLL
*P 00 *I ------H- *BI ---------- *BO .A........
*P 01 *I ----L--- *BI ---------- *BO .......A..
*P 02 *I ----H--- *BI HH-------- *BO ....A.....
*P 03 *I ---H---- *BI ---------- *BO ..........
*P 04 *I --L----- *BI ---------- *BO ..........
*P 05 *I -------- *BI -------H-- *BO ..........
*P 06 *I ----LL-- *BI ---------- *BO .....A....
*P 07 *I L------- *BI ---------- *BO ..AA..A...
*P 08 *I -------- *BI ---------H *BO ..AA..A...
*P 09 *I -H------ *BI ---------- *BO ........A.
*P 10 *I ----H--- *BI ---------- *BO ........A.
*P 11 *I -L--L--- *BI --------H- *BO A.........
*P 12 *I -L--L--- *BI L--------- *BO ..........
*P 13 *I -------H *BI ---------- *BO A.........
*P 14 *I -------- *BI ---------L *BO .........A
*P 15 *I -------- *BI ---------- *BO ..........
*P 16 *I --LL---- *BI ---------- *BO ..........
*P 17 *I --L----- *BI H--------- *BO ...A......
*P 18 *I --LL---- *BI H--------- *BO .A........
*P 19 *I 00000000 *BI 0000000000 *BO AAAAAAAAAA
*P 20 *I 00000000 *BI 0000000000 *BO AAAAAAAAAA
*P 21 *I 00000000 *BI 0000000000 *BO AAAAAAAAAA
*P 22 *I 00000000 *BI 0000000000 *BO ..........
*P 23 *I 00000000 *BI 0000000000 *BO ..........
*P 24 *I 00000000 *BI 0000000000 *BO ..........
*P 25 *I 00000000 *BI 0000000000 *BO ..........
*P 26 *I 00000000 *BI 0000000000 *BO ..........
*P 27 *I 00000000 *BI 0000000000 *BO ..........
*P 28 *I 00000000 *BI 0000000000 *BO ..........
*P 29 *I 00000000 *BI 0000000000 *BO ..........
*P 30 *I 00000000 *BI 0000000000 *BO ..........
*P 31 *I 00000000 *BI 0000000000 *BO ..........
*P D9 *I -------- *BI ----------
*P D8 *I -------- *BI ----------
*P D7 *I -------- *BI ----------
*P D6 *I -------- *BI ----------
*P D5 *I -------- *BI ----------
*P D4 *I -------- *BI ----------
*P D3 *I -------- *BI ----------
*P D2 *I -------- *BI ----------
*P D1 *I -------- *BI ----------
*P D0 *I -------- *BI ---------L
```

E.2 IV-1624 Local I/O decoder

PLA number : 50c.0
PLA type : 82S153
Location (U#) : U31
Revision date : 01/30/85
Status : current

INPUTS	ACTIVE LEVEL	DESIGNATOR	PIN#
A15	H	I7	
A14	H	I6	
A13	H	I5	
A12	H	I4	
A11	H	I3	
A10	H	I2	
LOCIO*	L	B9	
UDS*	L	I1	
LDS*	L	I0	

OUTPUTS	POLARITY	PIN	ADDRESS
SCC0CS*	L	B8	F7E0xx, A9=L
SCC1CS*	L	B7	F7E4xx, A9=L
SCC2CS*	L	B6	F7E8xx, A9=L
SCC3CS*	L	B5	F7ECxx, A9=L
SCC or CONTROL*	L	B4	F7Exxx, A9=H
IVHANCS*	L	B3	F7F0xo
IGORCS*	L	B2	F7F4xo
TMRCS*	L	B1	F7F8xe
DMACS*	L	B0	F7FCxw

```
*POL HLLLLLLLLL
*P 00 *I HHHL--L- *BI L--------- *BO .....A....
*P 01 *I 00000000 *BI 0000000000 *BO AAAAAAAAAA
*P 02 *I HHHLLLL- *BI L--------- *BO .A........
*P 03 *I HHHLLHL- *BI L--------- *BO ..A.......
*P 04 *I HHHLHLL- *BI L--------- *BO ...A......
*P 05 *I HHHLHHL- *BI L--------- *BO ....A.....
*P 06 *I HHHHLL-L *BI L--------- *BO ......A...
*P 07 *I HHHHLH-L *BI L--------- *BO .......A..
*P 08 *I HHHHHL-L *BI L--------- *BO ..........
*P 09 *I HHHHHH-L *BI L--------- *BO .........A
*P 10 *I HHHHHLL- *BI L--------- *BO ........A.
*P 11 *I HHHHHHL- *BI L--------- *BO .........A
*P 12 *I 00000000 *BI 0000000000 *BO AAAAAAAAAA
*P 13 *I 00000000 *BI 0000000000 *BO AAAAAAAAAA
*P 14 *I 00000000 *BI 0000000000 *BO AAAAAAAAAA
*P 15 *I 00000000 *BI 0000000000 *BO ..........
*P 16 *I 00000000 *BI 0000000000 *BO ..........
*P 17 *I 00000000 *BI 0000000000 *BO ..........
*P 18 *I 00000000 *BI 0000000000 *BO ..........
*P 19 *I 00000000 *BI 0000000000 *BO ..........
*P 20 *I 00000000 *BI 0000000000 *BO ..........
*P 21 *I 00000000 *BI 0000000000 *BO ..........
*P 22 *I 00000000 *BI 0000000000 *BO ..........
*P 23 *I 00000000 *BI 0000000000 *BO ..........
*P 24 *I 00000000 *BI 0000000000 *BO ..........
*P 25 *I 00000000 *BI 0000000000 *BO ..........
*P 26 *I 00000000 *BI 0000000000 *BO ..........
*P 27 *I 00000000 *BI 0000000000 *BO ..........
*P 28 *I 00000000 *BI 0000000000 *BO ..........
*P 29 *I 00000000 *BI 0000000000 *BO ..........
*P 30 *I 00000000 *BI 0000000000 *BO ..........
*P 31 *I 0-0-0000 *BI --00000000 *BO ..........
*P D9 *I 00000000 *BI 0000000000
*P D8 *I -------- *BI ----------
*P D7 *I -------- *BI ----------
*P D6 *I -------- *BI ----------
*P D5 *I -------- *BI ----------
*P D4 *I -------- *BI ----------
*P D3 *I -------- *BI ----------
*P D2 *I -------- *BI ----------
*P D1 *I -------- *BI ----------
*P D0 *I -------- *BI ----------
```

E.3 IV-1624 IACK decoder

PLA number : 50d.2
PLA type : 82S153
Revision date : 06/24/85
Location (U#) : U33
Status : current
Application note: use with 50F.2 for recovery time

INPUTS	ACTIVE LEVEL	DESIGNATOR
DELAY1*	L	I7
LIACK*	L	I6
UDS*	L	I5
LDS*	L	I4
R/W*	H	I3
A3	H	I2
A2	H	I1
A1	H	I0
BLOCK*	L	B0
DELAY2*	L	B7
RESET*	L	B5
RAMEN*	L	B0

OUTPUTS	POLARITY	PIN
LDTACK*	L	B9
SCC01IACK*	L (level 4)	B8
SCC23IACK*	L (level 3)	B6
SCCRD*	L	B4
SCCWR*	L	B3
SIOIACK*	L	B2
DMAIACK*	L (level 1)	B1

```
*POL LLLLLLLLLH
*P 00 *I -L-L-HLL *BI ---------- *BO .A.....A.A
*P 01 *I -L-L-LHH *BI ---------- *BO ...A...A.A
*P 02 *I -L-L-LLH *BI ---------- *BO ........AA
*P 03 *I -HL-H--- *BI ---------- *BO .....A...A
*P 04 *I L--L---- *BI -------L-L *BO .....A...A
*P 05 *I -HL-L--- *BI H--------- *BO ......A..A
*P 06 *I L-L----- *BI --L----H-L *BO A........A
*P 07 *I L--L---- *BI --L----L-L *BO A........A
*P 08 *I -------- *BI ----L----H *BO .....AA..A
*P 09 *I 00000000 *BI 0000000000 *BO AAAAAAAAAA
*P 10 *I 00000000 *BI 0000000000 *BO AAAAAAAAAA
*P 11 *I 00000000 *BI 0000000000 *BO AAAAAAAAAA
*P 12 *I 00000000 *BI 0000000000 *BO AAAAAAAAAA
*P 13 *I 00000000 *BI 0000000000 *BO AAAAAAAAAA
*P 14 *I 00000000 *BI 0000000000 *BO AAAAAAAAAA
*P 15 *I 00000000 *BI 0000000000 *BO AAAAAAAAAA
*P 16 *I 00000000 *BI 0000000000 *BO AAAAAAAAAA
*P 17 *I 00000000 *BI 0000000000 *BO AAAAAAAAAA
*P 18 *I 00000000 *BI 0000000000 *BO AAAAAAAAAA
*P 19 *I 00000000 *BI 0000000000 *BO AAAAAAAAAA
*P 20 *I 00000000 *BI 0000000000 *BO AAAAAAAAAA
*P 21 *I 00000000 *BI 0000000000 *BO AAAAAAAAAA
*P 22 *I 00000000 *BI 0000000000 *BO AAAAAAAAAA
*P 23 *I 00000000 *BI 0000000000 *BO AAAAAAAAAA
*P 24 *I 00000000 *BI 0000000000 *BO AAAAAAAAAA
*P 25 *I 00000000 *BI 0000000000 *BO AAAAAAAAAA
*P 26 *I 00000000 *BI 0000000000 *BO AAAAAAAAAA
*P 27 *I 00000000 *BI 0000000000 *BO AAAAAAAAAA
*P 28 *I 00000000 *BI 0000000000 *BO AAAAAAAAAA
*P 29 *I 00000000 *BI 0000000000 *BO AAAAAAAAAA
*P 30 *I 00000000 *BI 0000000000 *BO AAAAAAAAAA
*P 31 *I 0-0-0000 *BI --0-0000HH *BO ..........
*P D9 *I L------- *BI --L------L
*P D8 *I -------- *BI ----------
*P D7 *I 00000000 *BI 0000000000
*P D6 *I -------- *BI ----------
*P D5 *I 00000000 *BI 0000000000
*P D4 *I -------- *BI ----------
*P D3 *I -------- *BI ----------
*P D2 *I -------- *BI ----------
*P D1 *I -------- *BI ----------
*P D0 *I 00000000 *BI 0000000000
```

E.4 IV-1624 Map decoder PLA (256K)

PLA number : 50E.2
PLA type : 82S153A
Location (U#) : U47
Revision date : 06/17/85
Status : current
Application note: make static ram independent of AS* for some set up time.

Key to inputs:

SIGNAL	POLARITY	PIN #
A23	H	I7
A22	H	I6
A21	H	I5
A20	H	I4
A19	H	I3
A18	H	I2
A17	H	I1
A16	H	I0
AS*	L	B9
FORCE ROM*	L	B8
IACK*	L	B7
DRDPGT*	L	B3

Outputs:

LOCIO*	L	B6
RAMEN*	L	B5
VME*	L	B4
SROVME*	L	B2
EPROM*	L	B1
SHORT*	L	B0

1/28-- make VME* decode depend on AS* to remove glitch to avoid false logic analyzer trigger

FUNCTIONAL DESCRIPTION:

OUTPUT	ADDRESS RANGE	IACK/	AS/
LOCIO/	F70000-F7FFFF	H	-
RAMEN/	000000-03FFFF (256Kb)	H	-
EPROM/	F00000-F0FFFF	H	L
SHORT/	FF0000-FFFFFF	H	-
SROVME/	none of the above	H	L
VME/	same as SROVME/ except not asserted for static dual port ram at FE0000-FEFFFF	H	-

DRDPGT* inhibits all decodes except RAMEN* which it forces

```
*POL LLLLLLHLLL
*P 00 *I HHHHHLHHH *BI LHH---H--- *BO ...A......
*P 01 *I LLLLLL-- *BI LHH---H--- *BO ....A.....
*P 02 *I HHLH---- *BI LHH---H--- *BO ..........
*P 03 *I HHHHLLLL *BI LHH---H--- *BO ........A.
*P 04 *I HHHHHHHH *BI LHH---H--- *BO .....A.A.A
*P 05 *I -------- *BI LLH---H--- *BO ........A.
*P 06 *I L----H-- *BI -HH---H--- *BO ..........
*P 07 *I L---H--- *BI LHH---H--- *BO .....A.A..
*P 08 *I LH------ *BI LHH---H--- *BO .....A.A..
*P 09 *I L-H----- *BI LHH---H--- *BO .....A.A..
*P 10 *I L--H---- *BI LHH---H--- *BO .....A.A..
*P 11 *I HL------ *BI LHH---H--- *BO .....A.A..
*P 12 *I HHHL---- *BI LHH---H--- *BO .....A.A..
*P 13 *I HHHH-HLL *BI LHH---H--- *BO .....A.A..
*P 14 *I HHHH--LH *BI LHH---H--- *BO .....A.A..
*P 15 *I HHHH-LH- *BI LHH---H--- *BO .....A.A..
*P 16 *I HHHHH-LL *BI LHH---H--- *BO .....A.A..
*P 17 *I HHHHHHHL *BI -HH---H--- *BO .......A..
*P 18 *I HHLL---- *BI LHH---H--- *BO .....A.A..
*P 19 *I -------- *BI ------L--- *BO ....A.....
*P 20 *I HHLH---- *BI LHH---H--- *BO .....A.A..
*P 21 *I 00000000 *BI 0000000000 *BO AAAAAAAAAA
*P 22 *I 00000000 *BI 0000000000 *BO AAAAAAAAAA
*P 23 *I 00000000 *BI 0000000000 *BO AAAAAAAAAA
*P 24 *I 00000000 *BI 0000000000 *BO AAAAAAAAAA
*P 25 *I 00000000 *BI 0000000000 *BO AAAAAAAAAA
*P 26 *I 00000000 *BI 0000000000 *BO ..........
*P 27 *I 00000000 *BI 0000000000 *BO ..........
*P 28 *I 00000000 *BI 0000000000 *BO ..........
*P 29 *I 00000000 *BI 0000000000 *BO ..........
*P 30 *I 00000000 *BI 0000000000 *BO ..........
*P 31 *I 0-0-0000 *BI ---00000HH *BO ..........
*P D9 *I 00000000 *BI 0000000000
*P D8 *I 00000000 *BI 0000000000
*P D7 *I 00000000 *BI 0000000000
*P D6 *I -------- *BI ----------
*P D5 *I -------- *BI ----------
*P D4 *I -------- *BI ----------
*P D3 *I 00000000 *BI 0000000000
*P D2 *I -------- *BI ----------
*P D1 *I -------- *BI ----------
*P D0 *I -------- *BI ----------
```

E.5 IV-1624 Map decoder PLA (64K)

PLA number : 50E.3
PLA type : 82S153A
Revision date : 06/18/85
Status : current
Location (U#) : U47
Application note: static ram decode indep. of AS*

Key to inputs:

SIGNAL	POLARITY	PIN #
A23	H	I7
A22	H	I6
A21	H	I5
A20	H	I4
A19	H	I3
A18	H	I2
A17	H	I1
A16	H	I0
AS*	L	B9
FORCE ROM*	L	B8
IACK*	L	B7
DRDPGT*	L	B3
Outputs:		
LOCIO*	L	B6
RAMEN*	L	B5
VME*	L	B4
SROVME*	L	B2
EPROM*	L	B1
SHORT*	L	B0

1/28-- make VME* decode depend on AS* to remove glitch
to avoid false logic analyzer trigger

FUNCTIONAL DESCRIPTION:

OUTPUT	ADDRESS RANGE	IACK/	AS/
LOCIO/	F70000-F7FFFF	H	-
RAMEN/	000000-00FFFF (64Kb)	H	-
EPROM/	F00000-F0FFFF	H	L
SHORT/	FF0000-FFFFFF	H	-
SROVME/	none of the above	H	L
VME/	same as SROVME/ except not asserted for static dual port ram at FE0000-FEFFFF	H	-

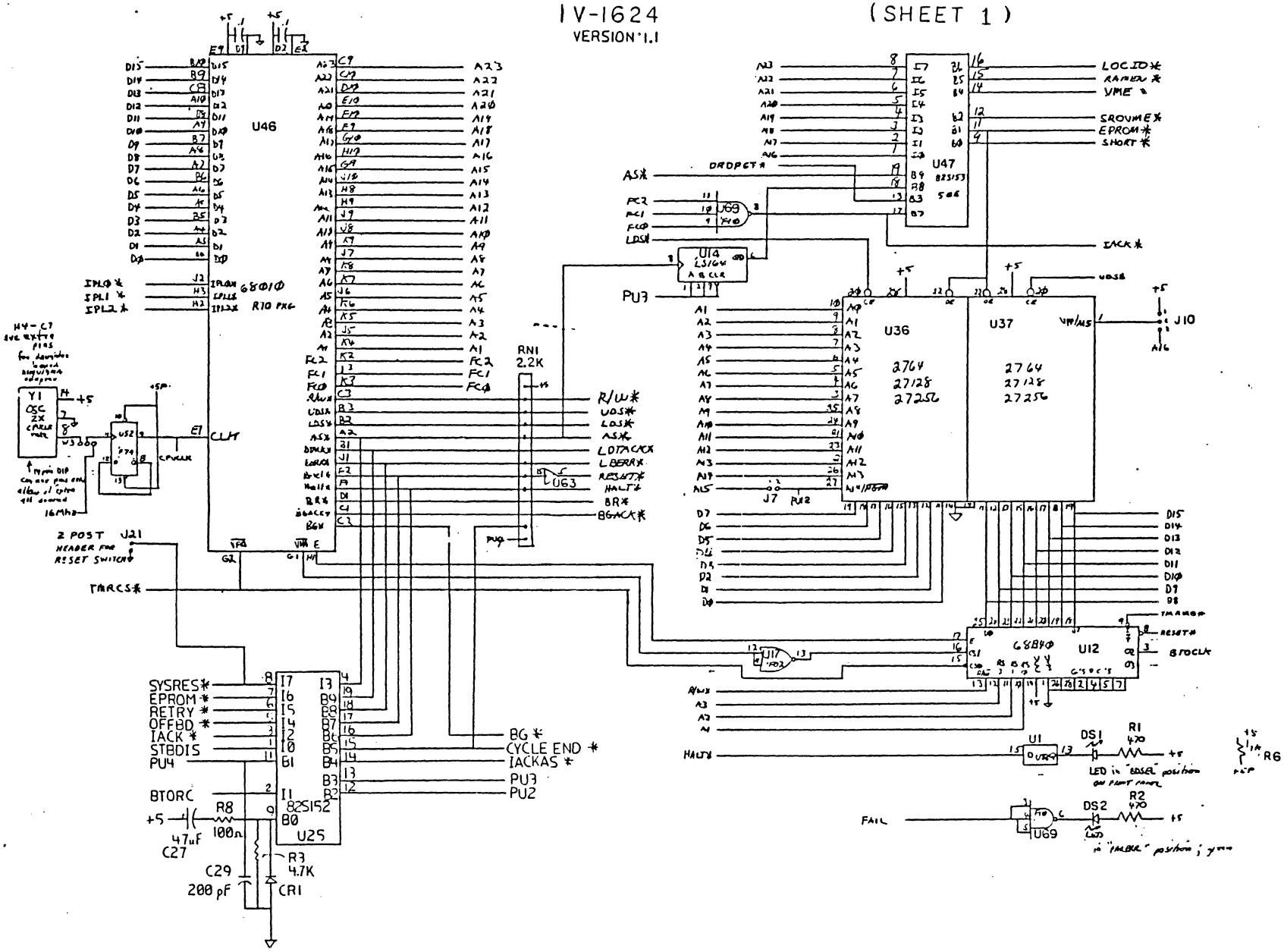
DRDPGT* inhibits all decodes except RAMEN* which it forces

```
*POL LLLLLLHLLL
*P 00 *I HHHHLHHH *BI -HH---H--- *BO ...A......
*P 01 *I LLLLLLLL *BI LHH---H--- *BO ....A.....
*P 02 *I 00000000 *BI 0000000000 *BO AAAAAAAAAA
*P 03 *I HHHHLLLL *BI LHH---H--- *BO ........A.
*P 04 *I HHHHHHHH *BI LHH---H--- *BO .....A.A.A
*P 05 *I -------- *BI LLH---H--- *BO ........A.
*P 06 *I L----H-- *BI -HH---H--- *BO ..........
*P 07 *I L---H--- *BI LHH---H--- *BO .....A.A..
*P 08 *I LH-H---- *BI LHH---H--- *BO .....A.A..
*P 09 *I L-H----- *BI LHH---H--- *BO .....A.A..
*P 10 *I L--H---- *BI LHH---H--- *BO .....A.A..
*P 11 *I HL------ *BI LHH---H--- *BO .....A.A..
*P 12 *I HHHL---- *BI LHH---H--- *BO .....A.A..
*P 13 *I HHHH-HLL *BI LHH---H--- *BO .....A.A..
*P 14 *I HHHH--LH *BI LHH---H--- *BO .....A.A..
*P 15 *I HHHH-LH- *BI LHH---H--- *BO .....A.A..
*P 16 *I HHHHH-LL *BI LHH---H--- *BO .....A.A..
*P 17 *I HHHHHHHL *BI -HH---H--- *BO .......A..
*P 18 *I HHLL---- *BI LHH---H--- *BO .....A.A..
*P 19 *I -------- *BI ------L--- *BO ....A.....
*P 20 *I HHLH---- *BI LHH---H--- *BO .....A.A..
*P 21 *I 00000000 *BI 0000000000 *BO AAAAAAAAAA
*P 22 *I 00000000 *BI 0000000000 *BO AAAAAAAAAA
*P 23 *I 00000000 *BI 0000000000 *BO AAAAAAAAAA
*P 24 *I 00000000 *BI 0000000000 *BO AAAAAAAAAA
*P 25 *I 00000000 *BI 0000000000 *BO AAAAAAAAAA
*P 26 *I 00000000 *BI 0000000000 *BO ..........
*P 27 *I 00000000 *BI 0000000000 *BO ..........
*P 28 *I 00000000 *BI 0000000000 *BO ..........
*P 29 *I 00000000 *BI 0000000000 *BO ..........
*P 30 *I 00000000 *BI 0000000000 *BO ..........
*P 31 *I 0-0-0000 *BI ---0000HHH *BO ..........
*P D9 *I 00000000 *BI 0000000000
*P D8 *I 00000000 *BI 0000000000
*P D7 *I 00000000 *BI 0000000000
*P D6 *I -------- *BI ----------
*P D5 *I -------- *BI ----------
*P D4 *I -------- *BI ----------
*P D3 *I 00000000 *BI 0000000000
*P D2 *I -------- *BI ----------
*P D1 *I -------- *BI ----------
*P D0 *I -------- *BI ----------
```

Appendix F Schematics

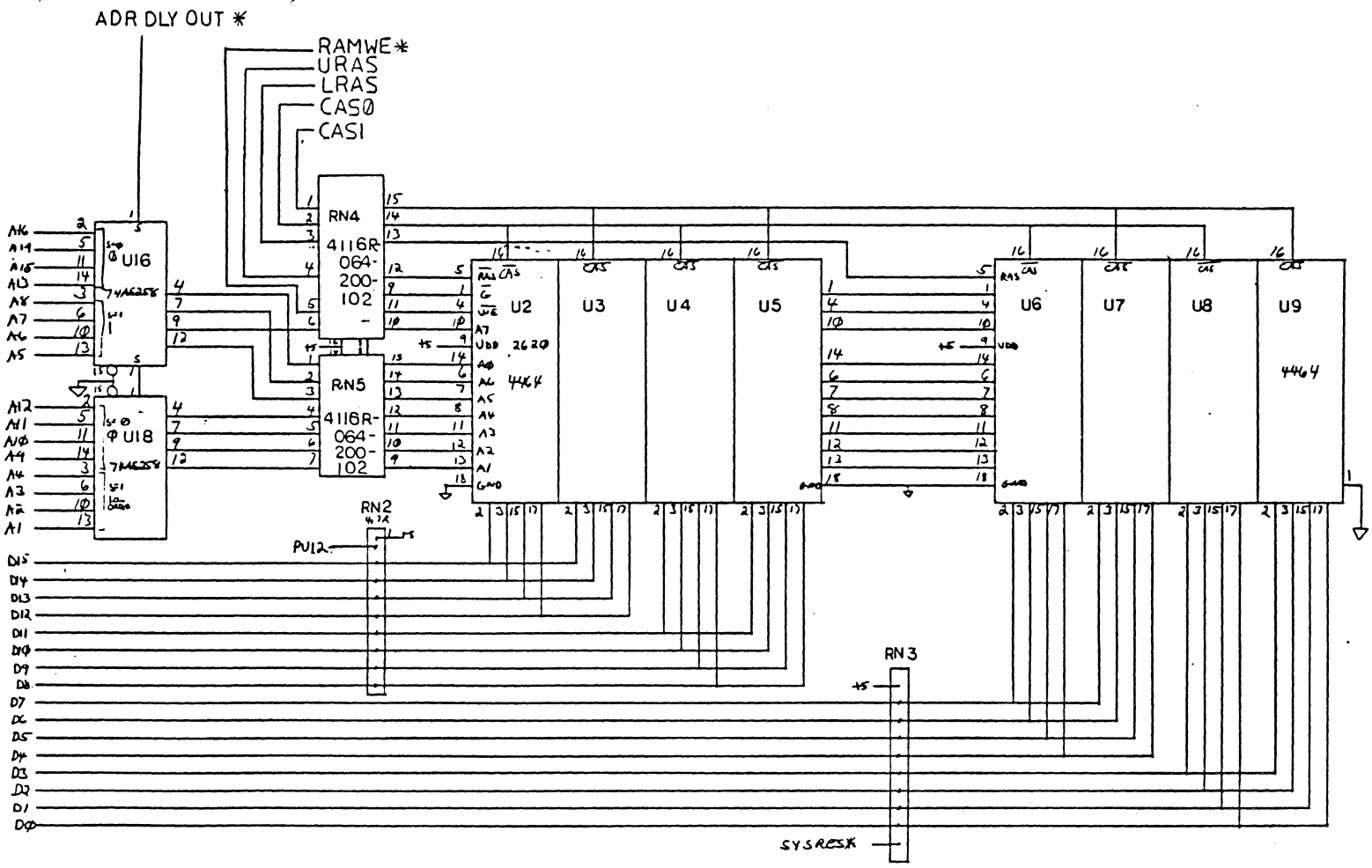
IV-1624 (SHEET 1)

VERSION 1.1



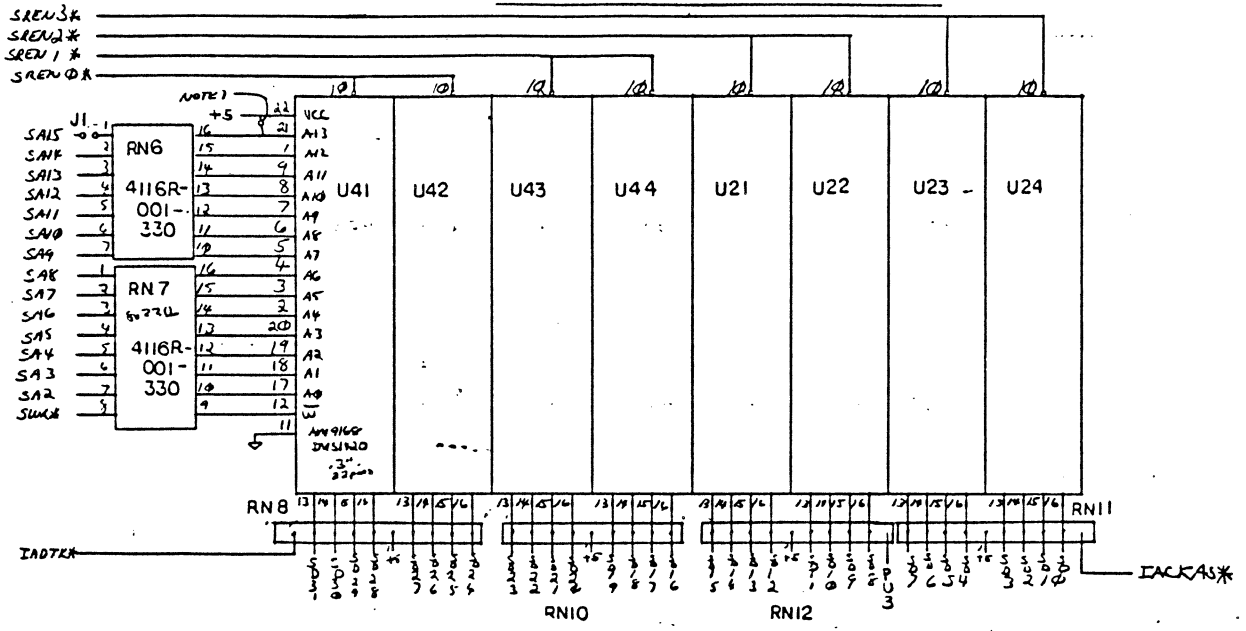
IV-1624 VERSION 1.1

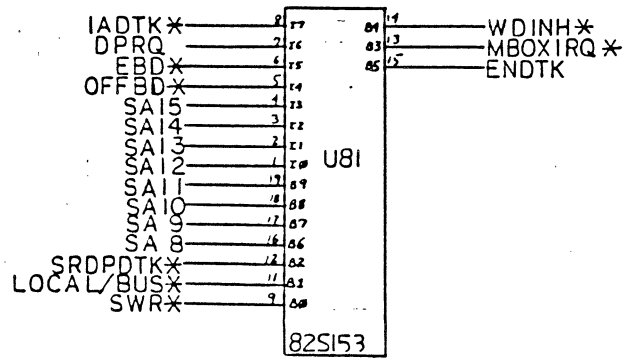
(SHEET 2)



IV-1624 1.100

STATIC RAM INTERFACE (SHEET 3)



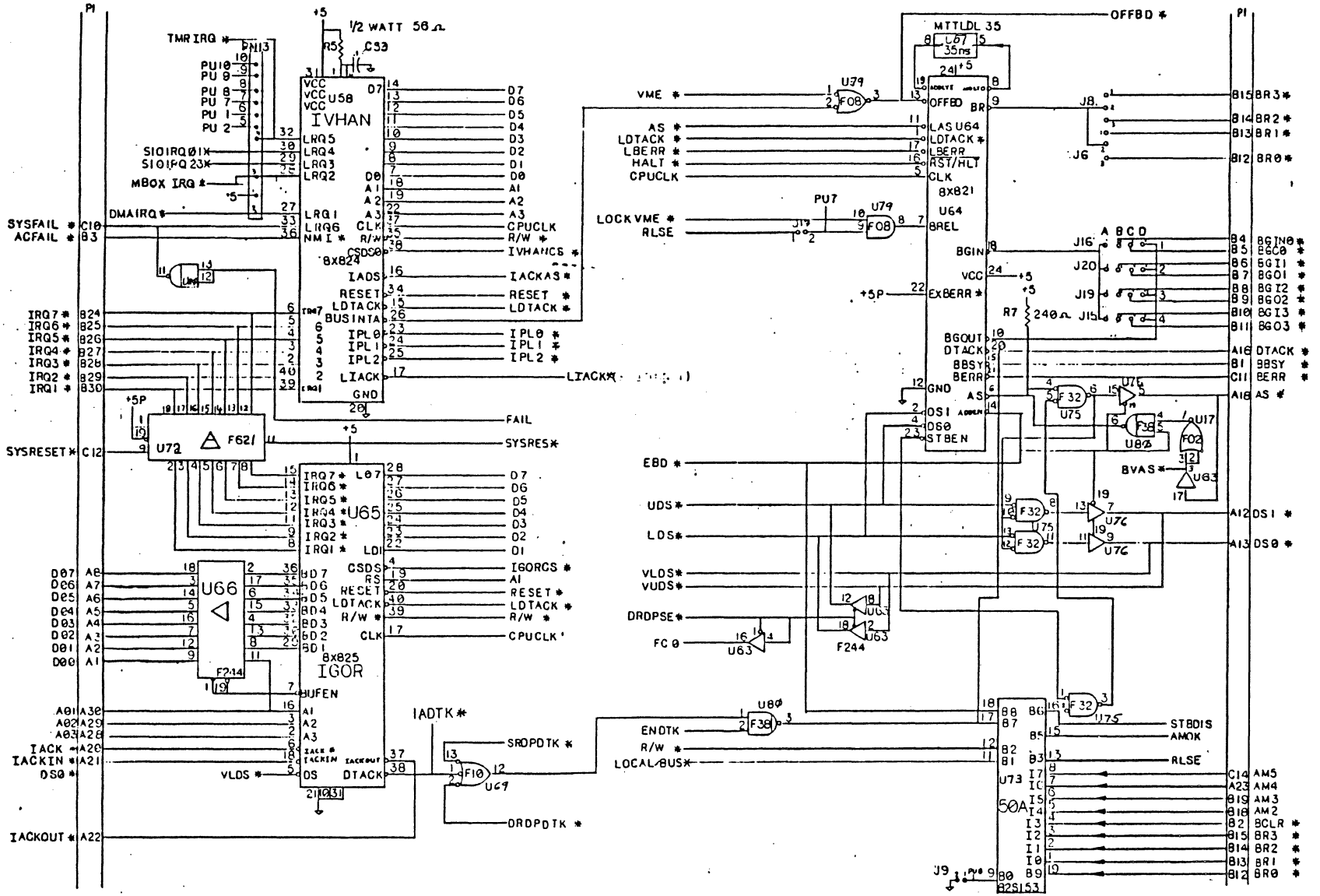


3-23-85

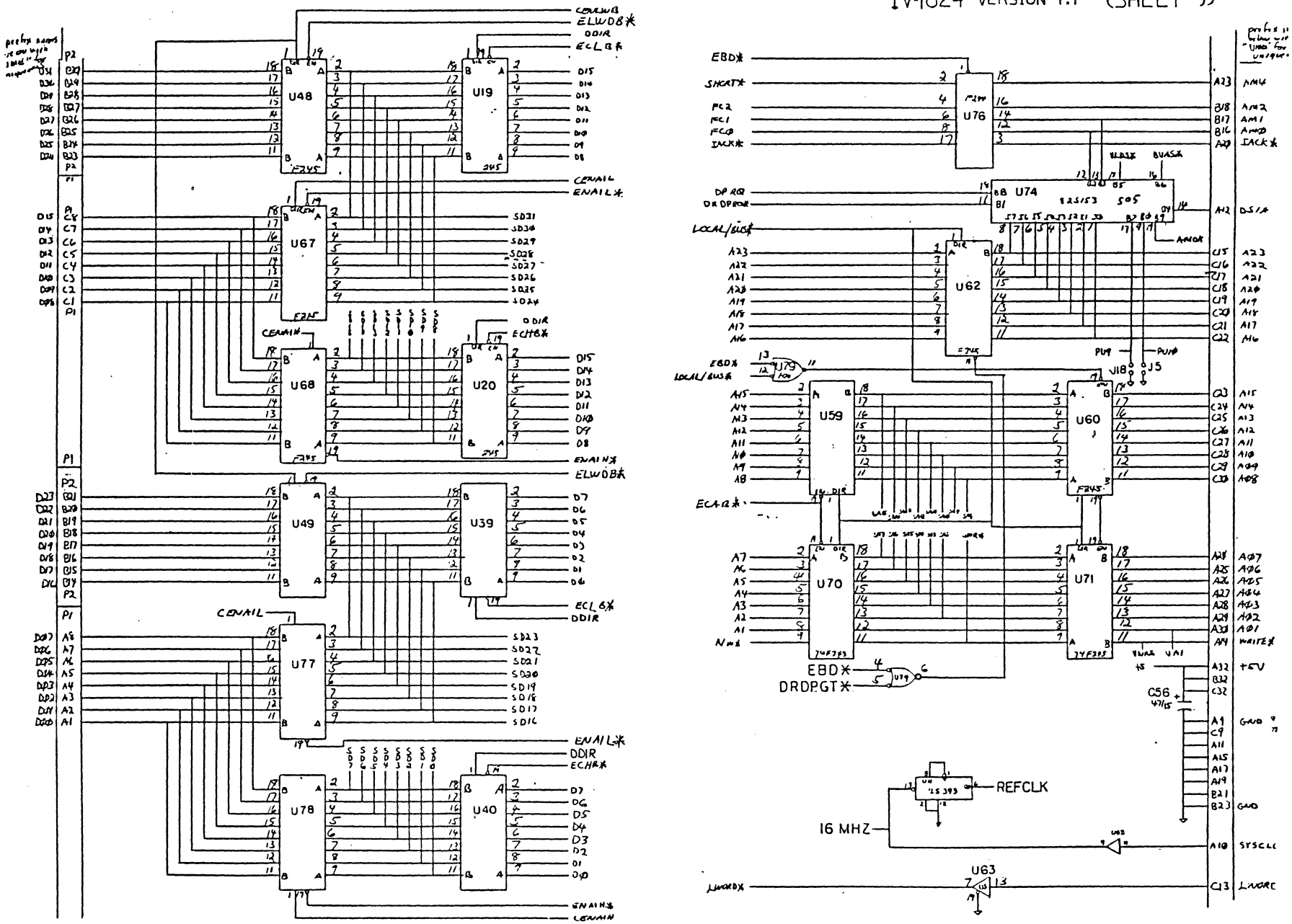
IV1624-1.100-G

VME CONTROL

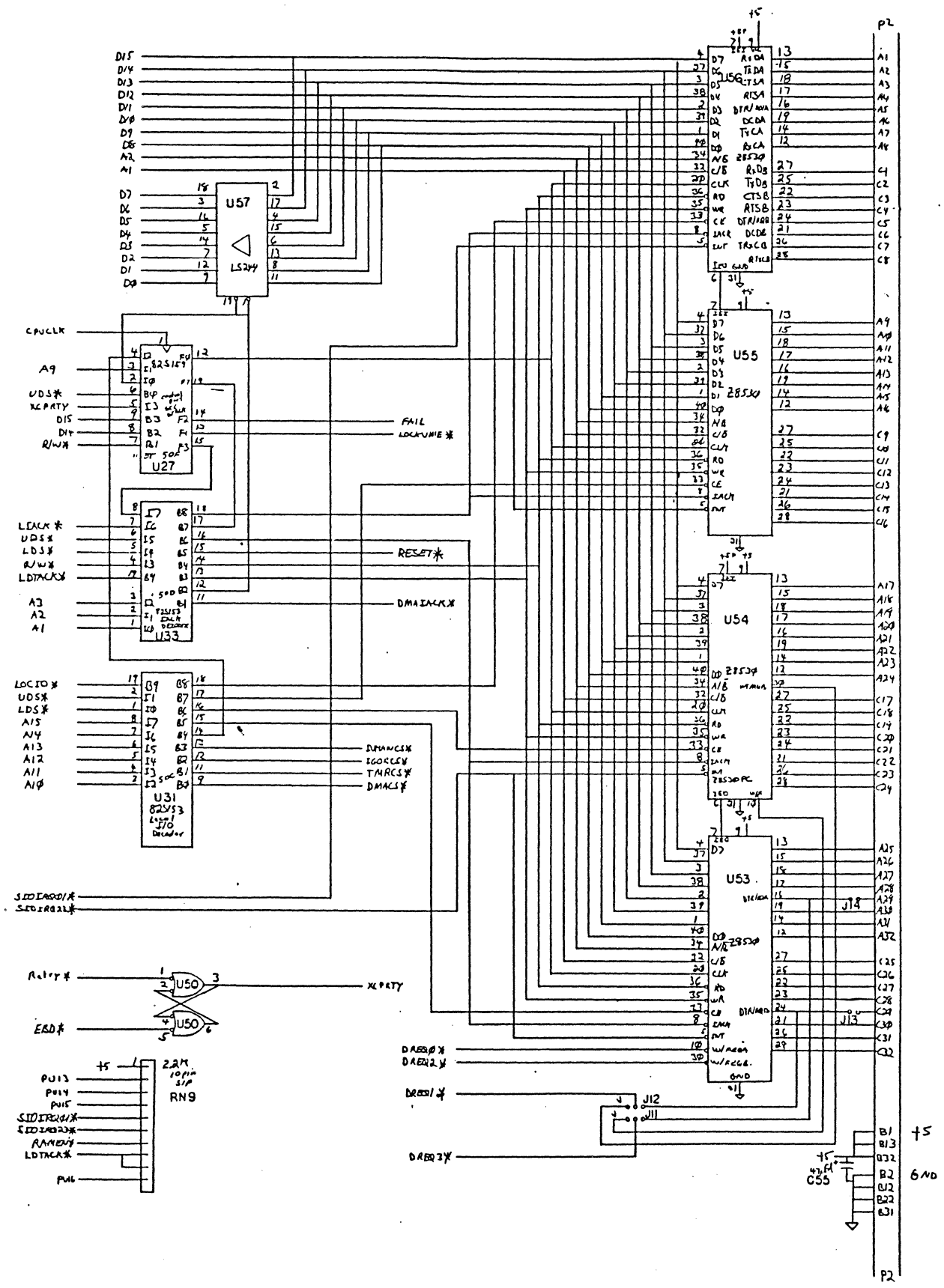
(SHEET 4)



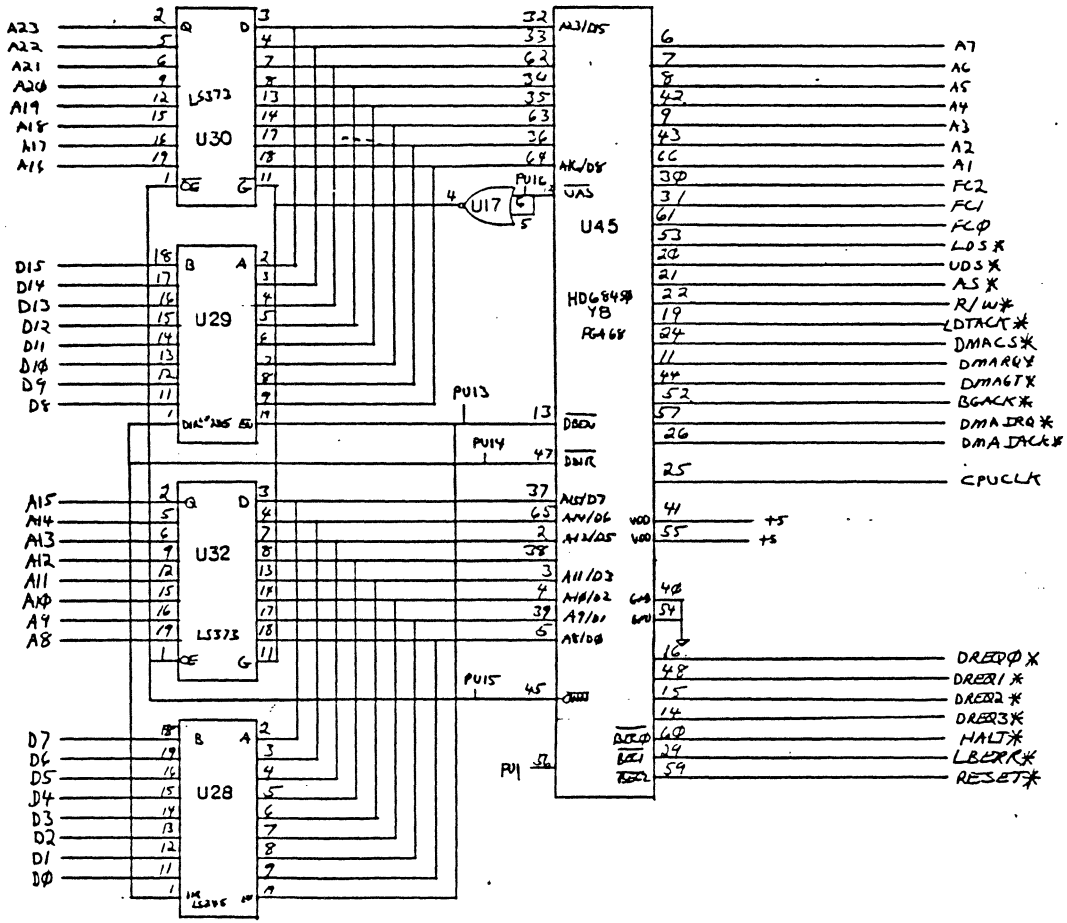
IV-1624 VERSION 1.1 (SHEET 5)



IV-1624 VERSION 1.1 (SHEET 6)



IV-1624 VERSION 1.1
(SHEET 7)



1624-1.2 MANUAL ERRATA

The following errors have been found in the current printing of the IV1624 manual and will be corrected in the next manual printing:

Table 4-11 (page 4-13)

Shunts J11 and J12 should be removed for proper operation of serial ports without DMA.

Table 4-12 (page 4-13)

Table 4-13 should read as follows:

TABLE 4-12. Half duplex and full duplex mode shunt installation (with DMA).

Mode	J11 [1-2]	J11 [2-3]	J12 [1-2]	J12 [2-3]	J13	J14
Half-duplex	in	out	in	out	out	out
Full-duplex	out	in	out	in	out	out

TABLE 4-10 (page 4-12)

Table 4-10 should read as follows:

Description	J6 [1-2]	J6 [2-3]	J8 [1-2]	J8 [2-3]
Bus request level 0	out	in	out	out
Bus request level 1	in	out	out	out
Bus request level 2	out	out	out	in
Bus request level 3	out	out	in	out

Figure 4-7 (page 4-14)

J14 is shown as a 3-pin shunt header. J14 is a two pin shunt header.

Appendix C (page C-3)

Table C-1: Signal A10 ("SYSCLK") is marked as "not used" on the IV1624. Signal A10 should read "SYSCLK" in the IV1624 signal assignment column.

Appendix D (page D-3)

Table D-2: J2/P2 row C pin assignments list pins as A1 through A32. Pin assinments should read C1 through C32.

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