Operation and Maintenance Manual
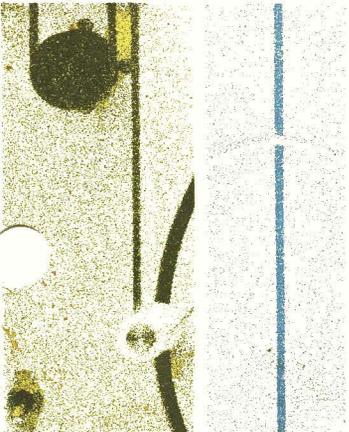
KENNEDY

AI ALLEGHENY INTERNATIONAL

Model 6455

Tape Cartridge System
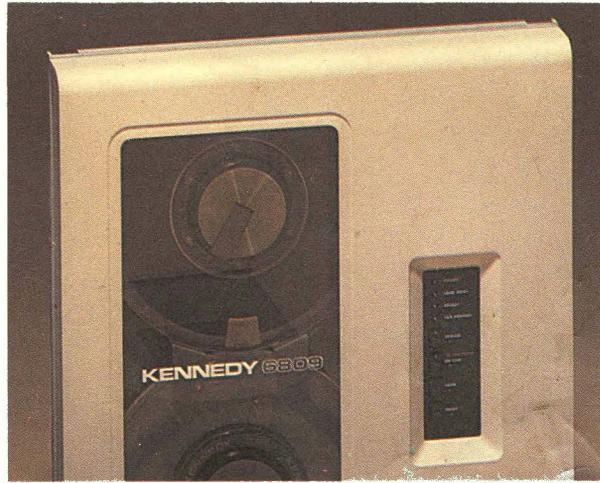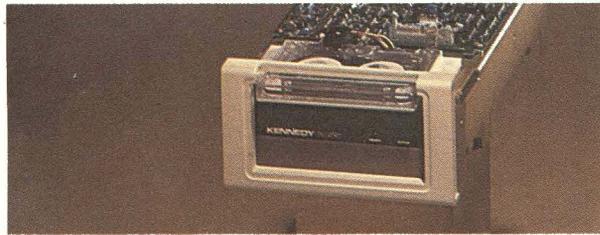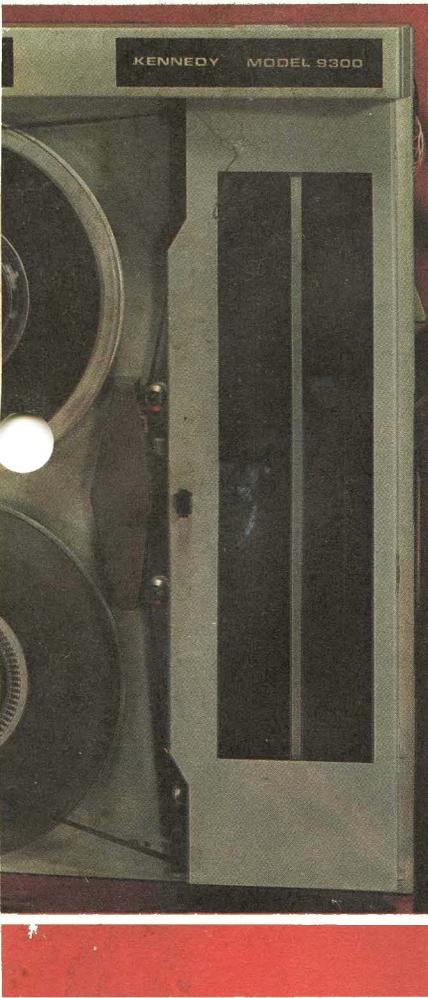
FCC CERTIFIED COMPUTER EQUIPMENT

SECTION I

APPLICATION DATA

1.1 INTRODUCTION

The Kennedy Model 6455 Cartridge Tape System consists of a highly reliable 6400 bpi GCR recorder with an embedded formatter. The system provides efficient backup for 8" and 14" Winchester disk drives. With an optimal data packing density of 4 KByte blocks, the Model 6455 yields a formatted capacity of over 13.9 MBytes on 450' tapes, and a formatted capacity of over 18 MBytes on 600' tapes. When 16 KByte records are used, the maximum allowed record length, the formatted data capacity on 600' tapes exceeds 21.5 MBytes. Use of serpentine recording allows for nearly continuous data transfer, reducing the dump time of 20 MBytes to only 14.7 minutes.

The Model 6455 formatter controls read and write functions, translating the parallel, logic level data supplied by the host to serial, GCR coded data, and provides serial error detection. The formatter responds to space one file and space one block commands in either the forward or reverse directions. These commands are translated to motion control inputs which satisfy all interlock and timing requirements while generating the interrecord gaps. The formatter also generates and detects file marks. The Model 6455 is also capable of tape editing, as required for file updating and maintenance. There are no external controls used on the Model 6455. The optional front panel has two indicators, one for "ready," indicating that the cartridge is properly loaded and ready for data transfer operations, and one for "drive active," indicating that the drive is performing an operation and cannot accept new commands.

The formatter design is centered around a microcomputer and two microsequencers. The microcomputer oversees overall system operation, handling the interface requirements and the transport commands. The two microsequencers process the data, one handling the write data and the other handling the read data.

The Model 6455 interface, designated as the Pico bus, allows the sharing of a common bus between the cartridge recorder and the disk which it backs up. This reduces the host interfacing requirements to a single controller, which can request status information from either the disk or the cartridge unit, responding with the appropriate commands.

The outstanding data reliability of the Model 6455 is achieved by using a uniquely designed filtering network and the inclusion of variable threshold levels, for maximum data recoverability. Due to its unique design approach the system offers additional features not commonly found in backup systems, yet is quite reasonably priced. Some of the features included in the Model 6455 are:

. A serpentine head, which eliminates time consuming rewinds between tracks.

. Automatic tape tensioning upon cartridge insertion.

. A radial interface, allowing direct selection of the device and immediate availability of status information.

. A floppy disk profile, allowing easy insertion into existing enclosures.

. A full complement of off line diagnostics, allowing servicing and adjustments without using valuable computer time.

. The incorporation of signature analysis into the formatter, minimizing down time required to isolate faulty components.

. Low system power consumption.

. Infrared BOT/EOT detectors, offering maximum reliability and immunity to ambient light conditions.

For host and controller programming information refer to the Model 6455 Application Notes, Kennedy document number 102-0032-002.

210-2071-001 B

TOP OF CARTRIDGE

CARTRIDGE REF PLAN "B"

8-32 2 PLACES

BOTTOM OF CARTRIDGE

8-32 4 PLACES

6-32 4 PLACES

14.00

8.56

4.27

3.70

0.72

13.95

1.00 ±.08

4.19 MAX.

4.62

2.50

0.80

8.00

2.28

4.00

2.50

0.38

0.25

0.49

7.33

7.58

3.40 MIN.

2.88
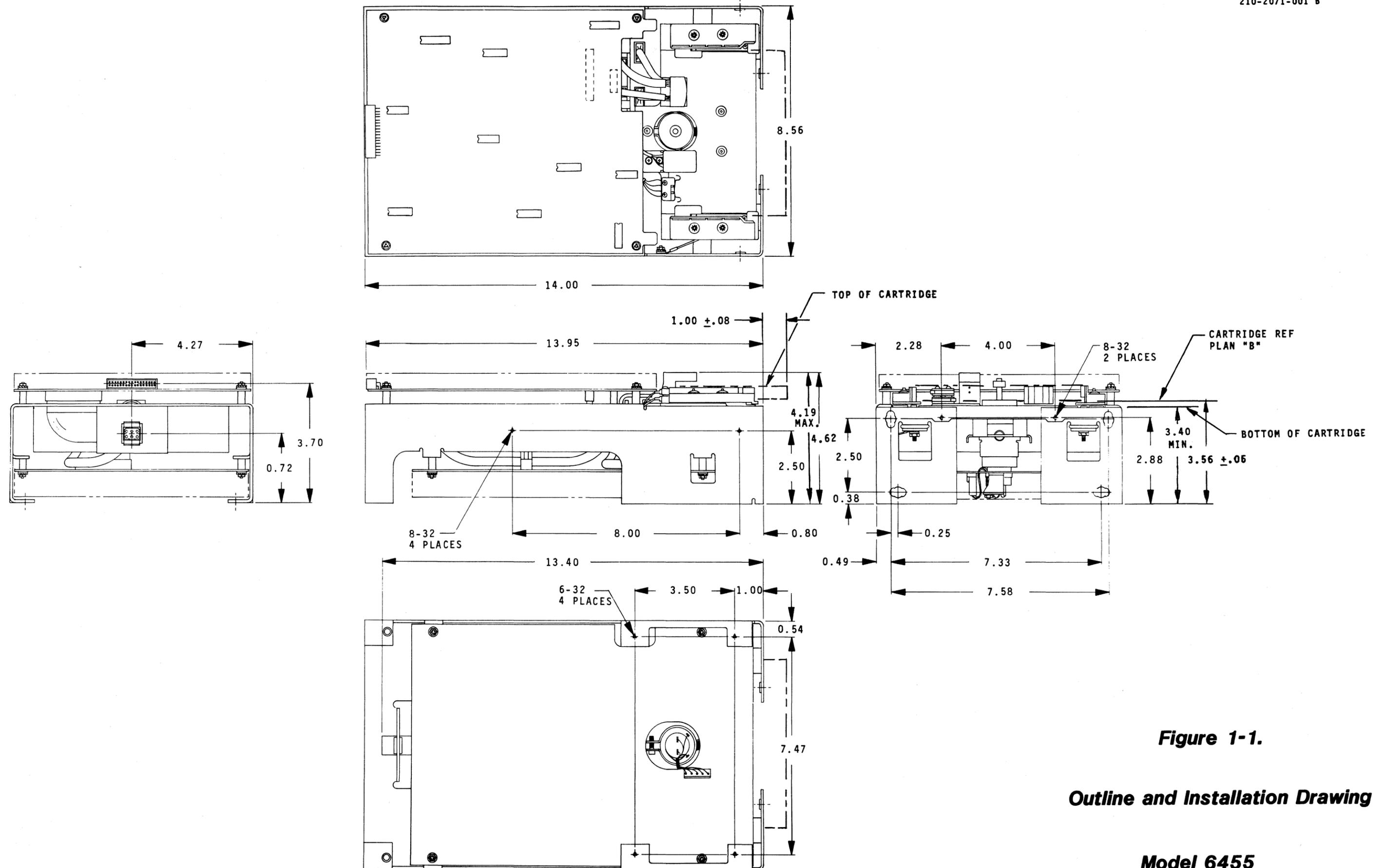
3.56 ±.05

13.40

3.50

1.00

0.54

7.47

Figure 1-1.

Outline and Installation Drawing

Model 6455

1.2 ELECTRICAL/MECHANICAL SPECIFICATION

Table 1-1 lists the general specifications for the
6455. Figure 1-1 is an outline and installation guide.

Cartridge Type	3M DC300A type Isoelastic Data Cartridge	Power Consumption	21 W idle, 27 W Read/Write, 31 W Rewind/Track Select
Tape Length	300, 450 or 600 feet	Weight	5 lbs
Capacity	11.5 MBytes at 300 feet 17.3 MBytes at 450 feet 23.0 MBytes at 600 feet	Dimensions	8.5"w x 4.5"h x 14"d
Recording Density	6400 bpi	Interface	
Number of Tracks	4 tracks arranged in a serpentine configuration	Host	Pico Bus, TTL low true, 34 pin 3M flat cable
Recording Head	Serpentine with read after write capability and selective erase	Power	6 pin molex
Record Format	Self-clocking Group Coded Recording (GCR)	Operating Environment	
		Ambient Temperature	+40 to +115 degrees Fahrenheit, 2 degrees F/minute temperature rise
Record Mode	Single track serpentine serial	Relative Humidity	20-80% (noncondensing)
Data Reliability	1 read soft error in 1 e10 bits 1 read hard error in 1 e11 bits	Altitude	To 10,000 feet operational, 30,000 feet nonoperational
Read/Write Speed	30 ips	Shock	
Fast Tape Motion	90 ips	Operational	2.5 g maximum at 1/2 sine wave, 11 ms duration
Erase Speed	90 ips		
Start/Stop Time	25 msec @ 30 ips 75 msec @ 90 ips	Nonoperational	50 g maximum at 1/2 sine wave, 11 ms duration
Data Transfer Rate	192,000 bits/sec 24,000 bytes/sec	Vibration	
		Operational	1 g maximum at 0 to 63 Hz
Power Requirements	+5 Vdc +/-5%, 3A typical, 5A maximum; +24 Vdc +/-10%, 1.5A average, 3A peak	Nonoperational	1.5 g maximum at 0 to 500 Hz

Table 1-1.

Model 6455 Specifications

1.3 INTERFACE AND POWER CONNECTORS

1.3.1 INTERFACE

The interface connector on the Kennedy Model 6455 Cartridge Tape System is a 34 pin flat cable connector. The recommended type is Scotchflex PN 3399-xxx. Maximum cable length between the controller and the Model 6455 system is 10 feet.

1.3.2 POWER

The power connector is a 6 pin molex type 1261, PN 03-09-1064. The molex pin part number is 02-09-1118. The Kennedy part number is 121-0102-005. The Kennedy part number for the connector is 121-0075-002. The connectors are located at the rear of the unit. Power connector pin assignments are shown in table 1-2.

1.4 CONTROL LINES

1.4.1 GENERAL

These interface signals control the flow of information on the bus lines. Figure 1-2 shows the interface configuration with the direction of signal flow indicated. Table 1-2 summarizes all interface and power connections, including connector pin numbers. The interface signals are described individually below.

Interface Connector		
Pin	Mnemonic	Description
02	FCLR	Formatter Clear
04	CREQ	Control Request
06	DRDY	Data Ready
08	HPAR	Host Parity
10	STRB	Strobe
12	CBSY	Command Busy
14	DBSY	Data Busy
16	FPAR	Formatter Parity
18	BUS0	Data Bus
20	BUS1	Data Bus
22	BUS2	Data Bus
24	BUS3	Data Bus
26	BUS4	Data Bus
28	BUS5	Data Bus
30	BUS6	Data Bus
32	BUS7	Data Bus
34	CMON	Cable Monitor

All odd numbered pins are ground

Power Connector

Pin	Description
1	-Sense
2	+5v GND*
3	+24v GND*
4	+Sense
5	+5 vdc
6	+24 vdc

*+5v and +24v ground lines should be tied together at the power supply.
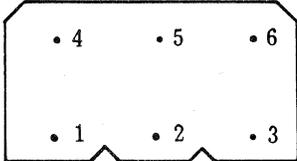
```
   ┌─────────────────────┐
   │ • 4     • 5     • 6  │
   │                      │
   │ • 1     • 2     • 3  │
   └────────┐   ┌─────────┘
            └─┘
```
Rear View, Pin Location

Table 1-2.
Model 6455
Interface and Power Connectors Summary

1.4.2 CONTROL REQUEST (CREQ)
Pins 4/3

This signal is asserted by the host to initiate a transfer of a command or parameter byte to or from the formatter. The interpretation of the transferred byte depends on the state of CBSY at the time CREQ is first asserted as follows:

1. If CBSY is false, the formatter is in an idle state and CREQ causes a command byte to be transferred to the formatter.

2. If CBSY is true the formatter is executing the most recent command byte. The nature and direction of the transfer initiated by CREQ is determined by that command.

CREQ is subject to the following timing restrictions, which must be strictly observed:

1. The data bus must be valid and stable (if output) or disabled (if input) for a minimum of 150 nanoseconds prior to the assertion of CREQ.

2. The data bus must remain stable throughout the assertion of CREQ.

3. CREQ must be maintained at a true level until the leading edge of STRB is received by the host. If STRB is not received within 500 microseconds, the host should flag this as an error condition (CREQ TIMEOUT) and take corrective action by first denying CREQ and then performing a formatter clear operation (see below).

4. CREQ must not become true unless STRB is false.

1.4.3 STROBE (STRB)
Pins 10/9

This signal is used by the formatter to acknowledge reception of a CREQ signal from the host during a command or argument transfer and to strobe read or write data during data transfer operations. Each of these cases is discussed below.

Command/Argument Transfers from Host to Formatter

In this case, CREQ and STRB form a handshake transfer protocol. Please refer to figure 1-3. The transfer begins with the host placing the command or argument on the data bus and then asserting CREQ. The formatter then signifies that it has accepted the data by asserting STRB. Once the host sees that STRB is asserted, it may deny CREQ and remove the command or argument from the data bus. Once CREQ is denied, the formatter will then deny STRB.
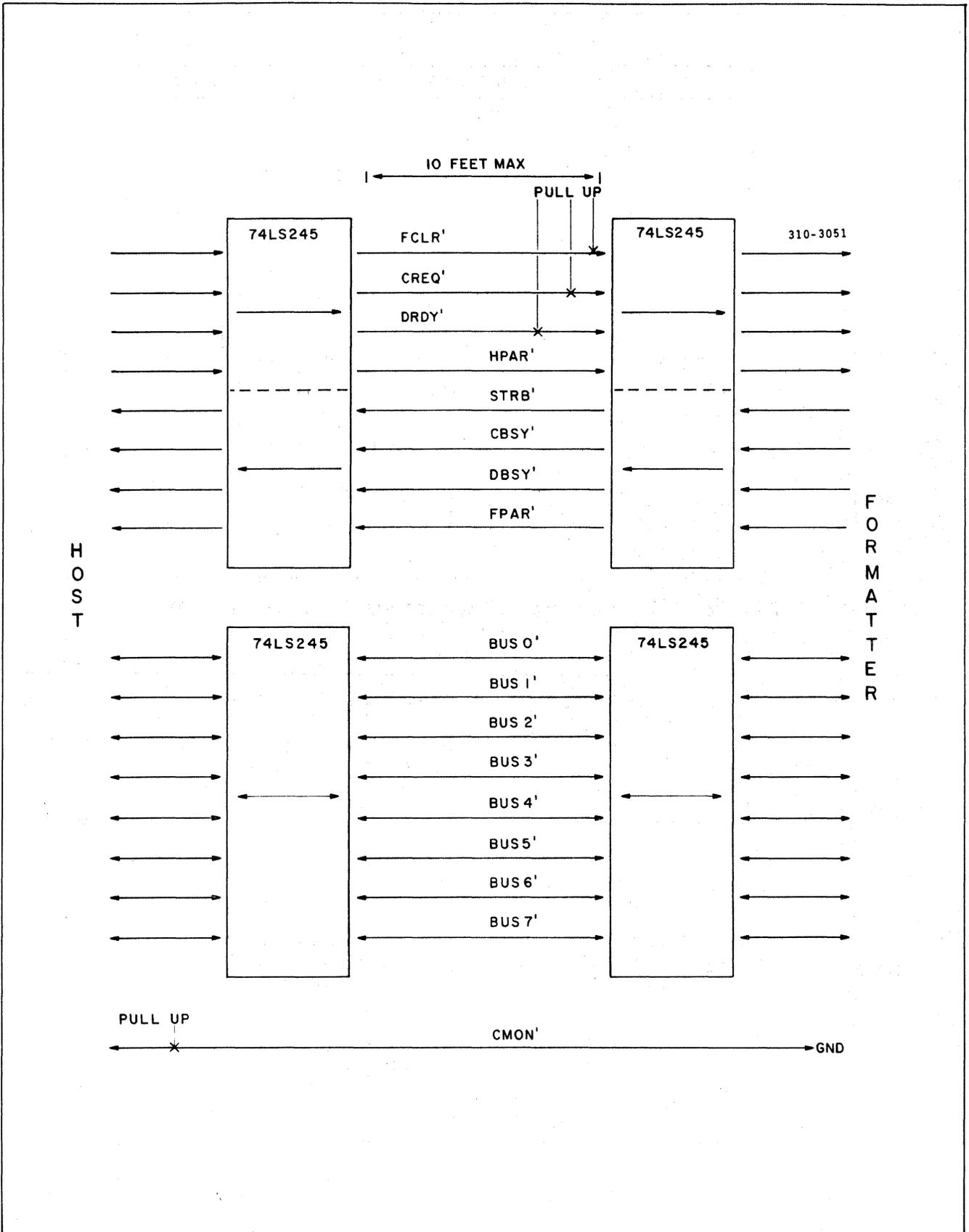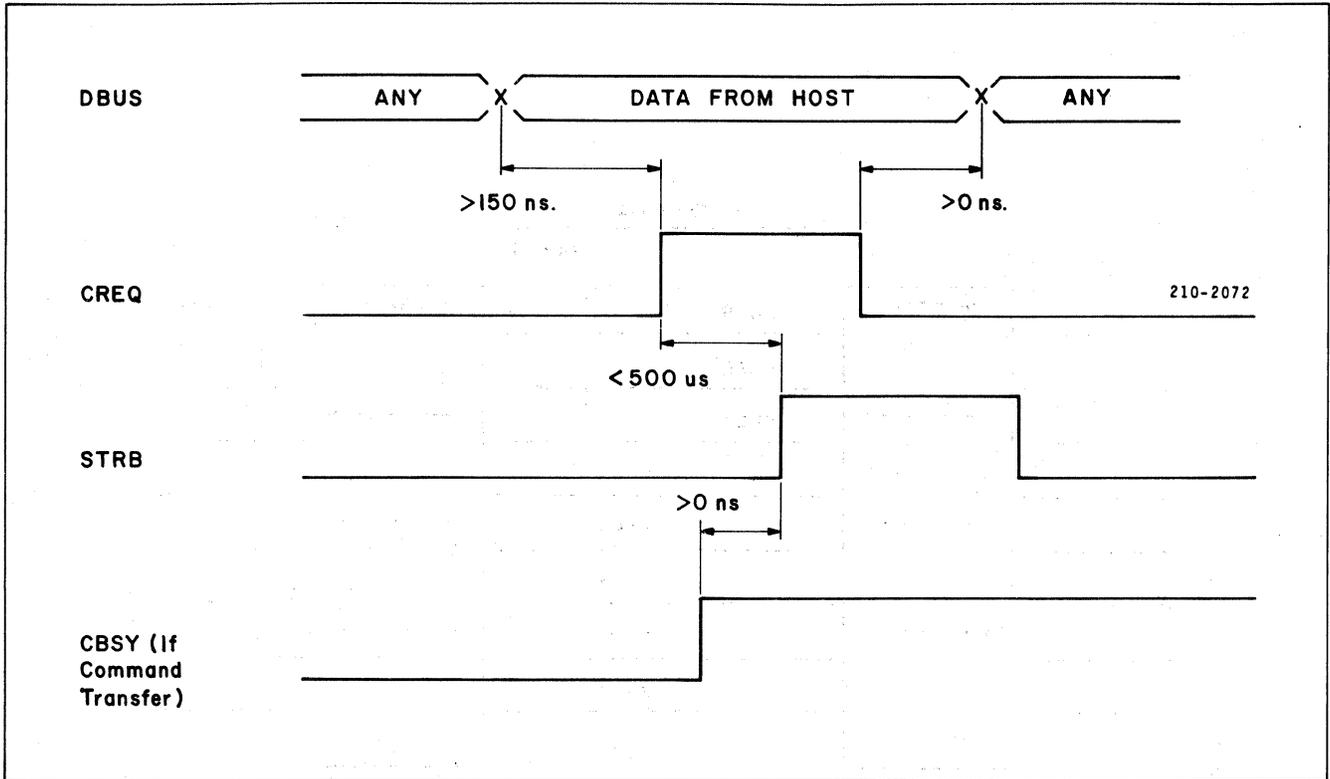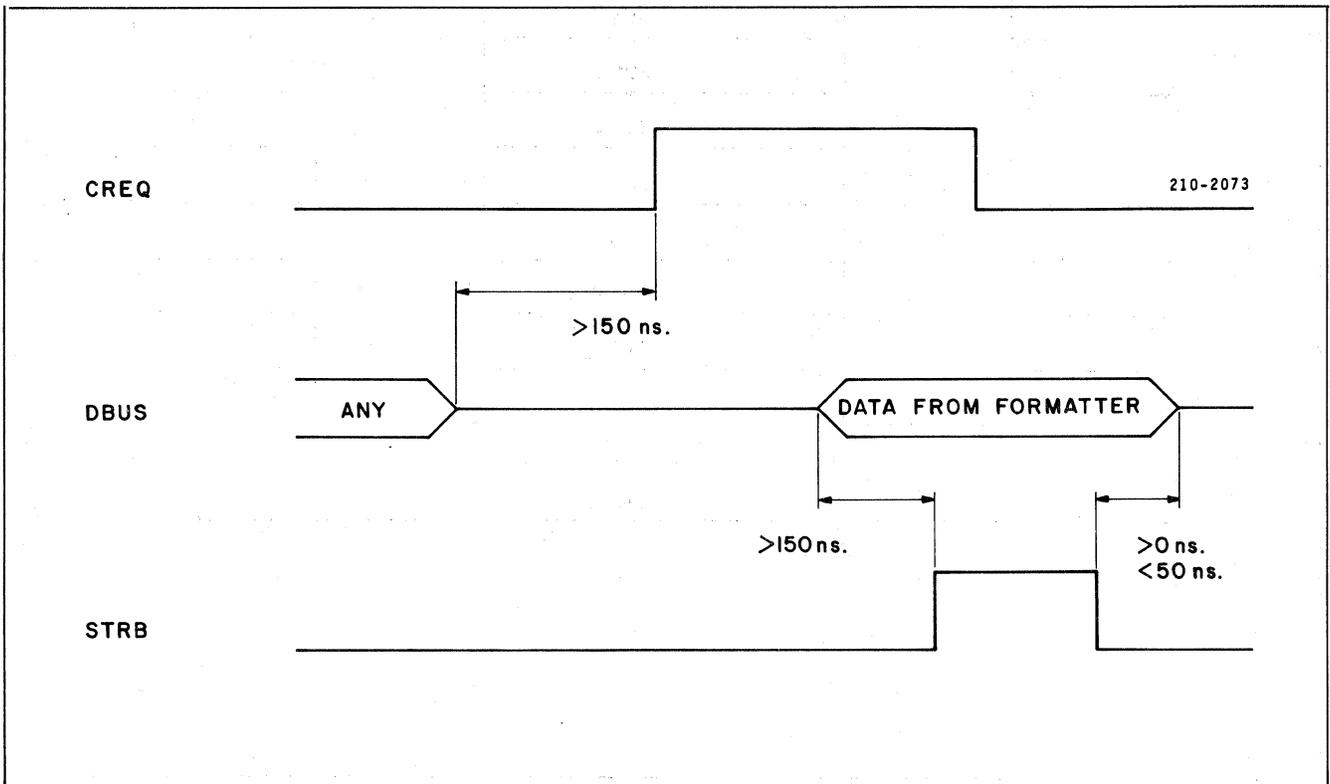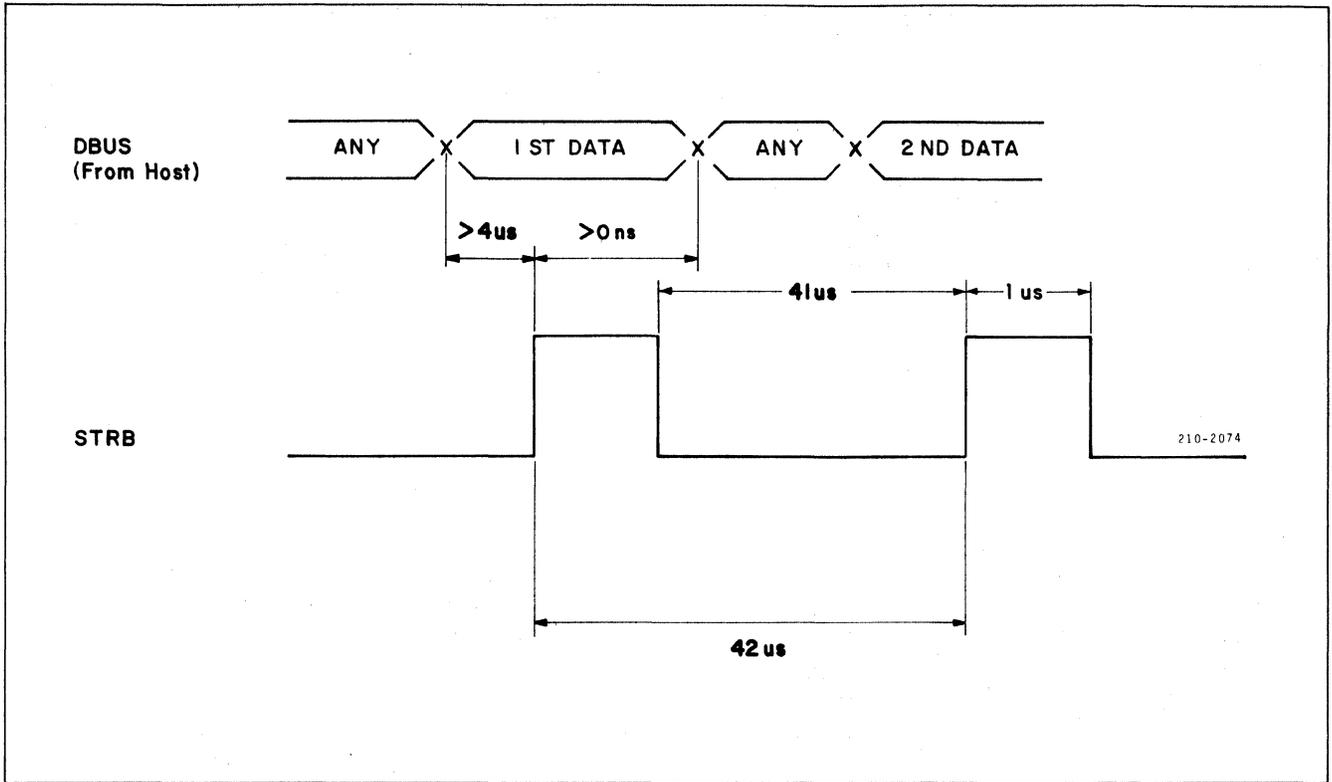
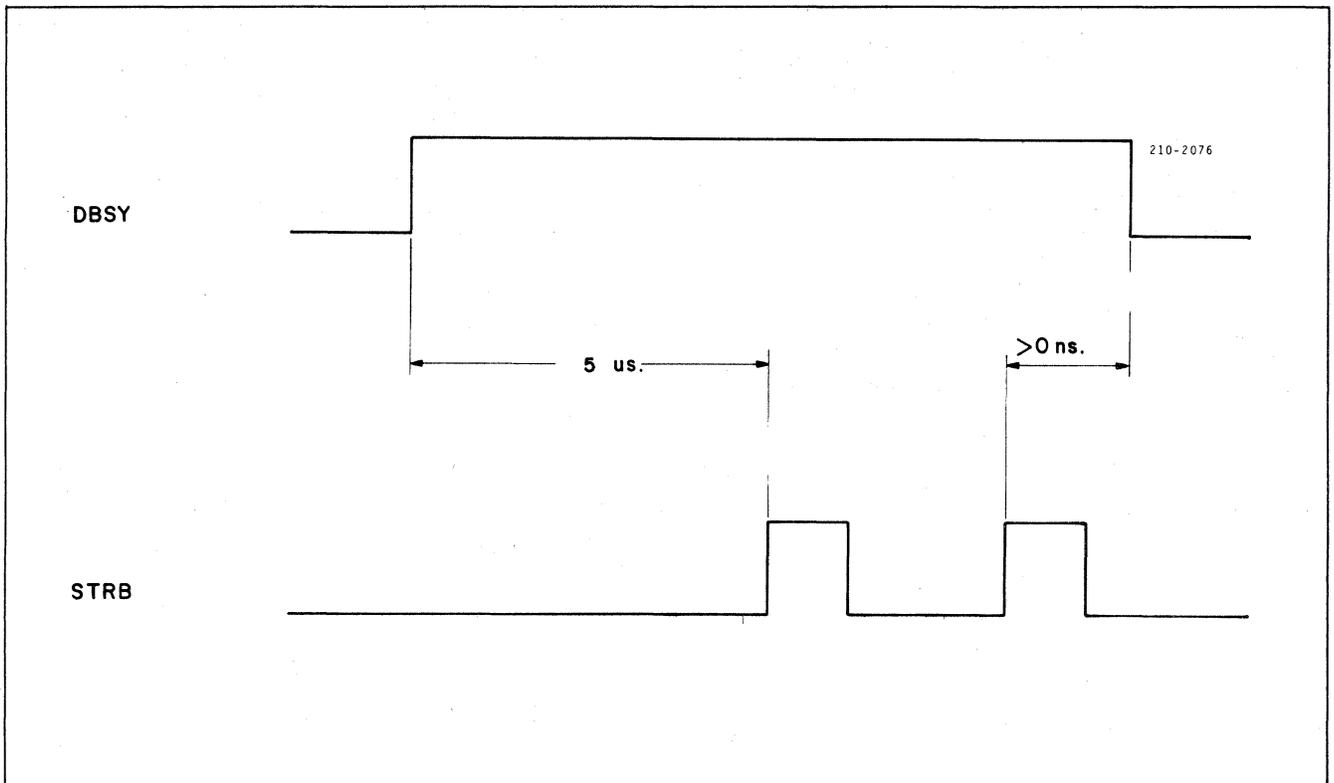**Figure 1-2. Model 6455 Interface Configuration**

Figure 1-3. Command/Argument Output Transfer

Figure 1-4. Command/Argument Input Transfer

Figure 1-5. Data Output Transfer (Write)
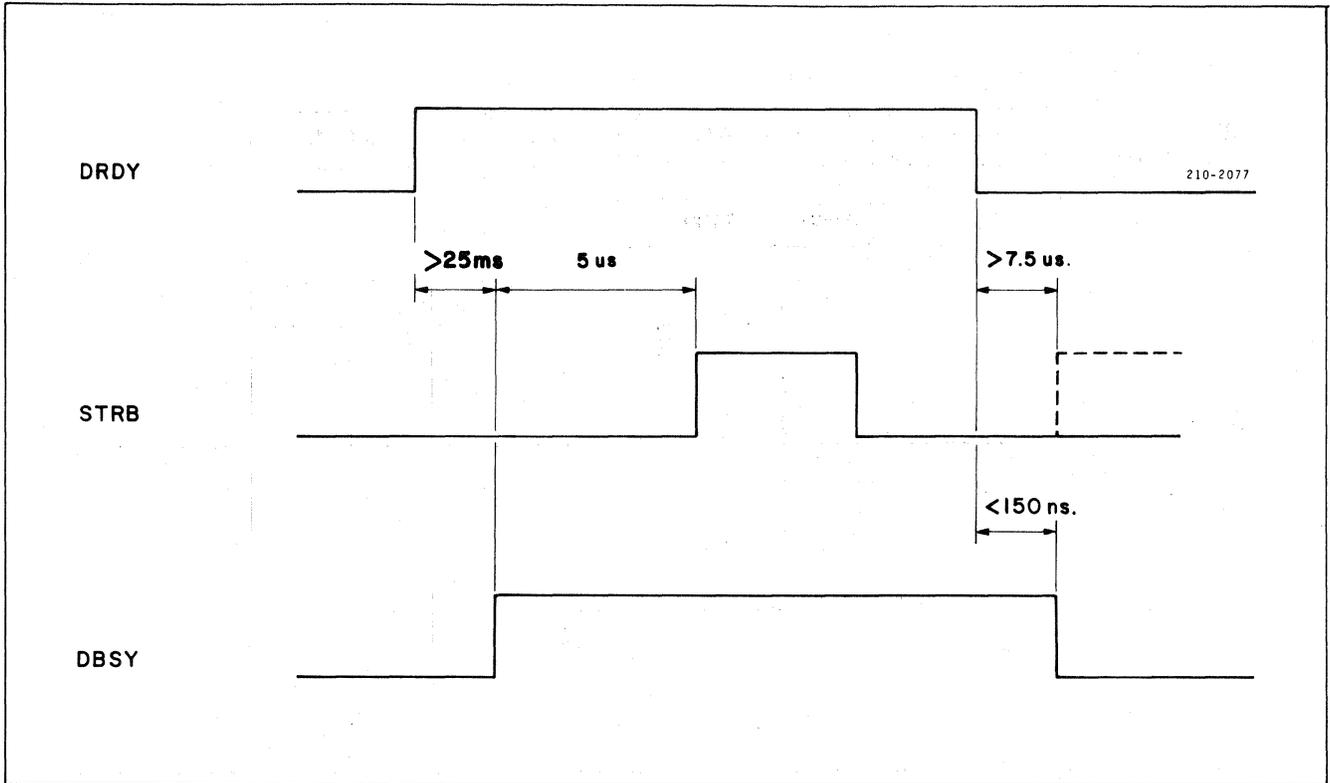

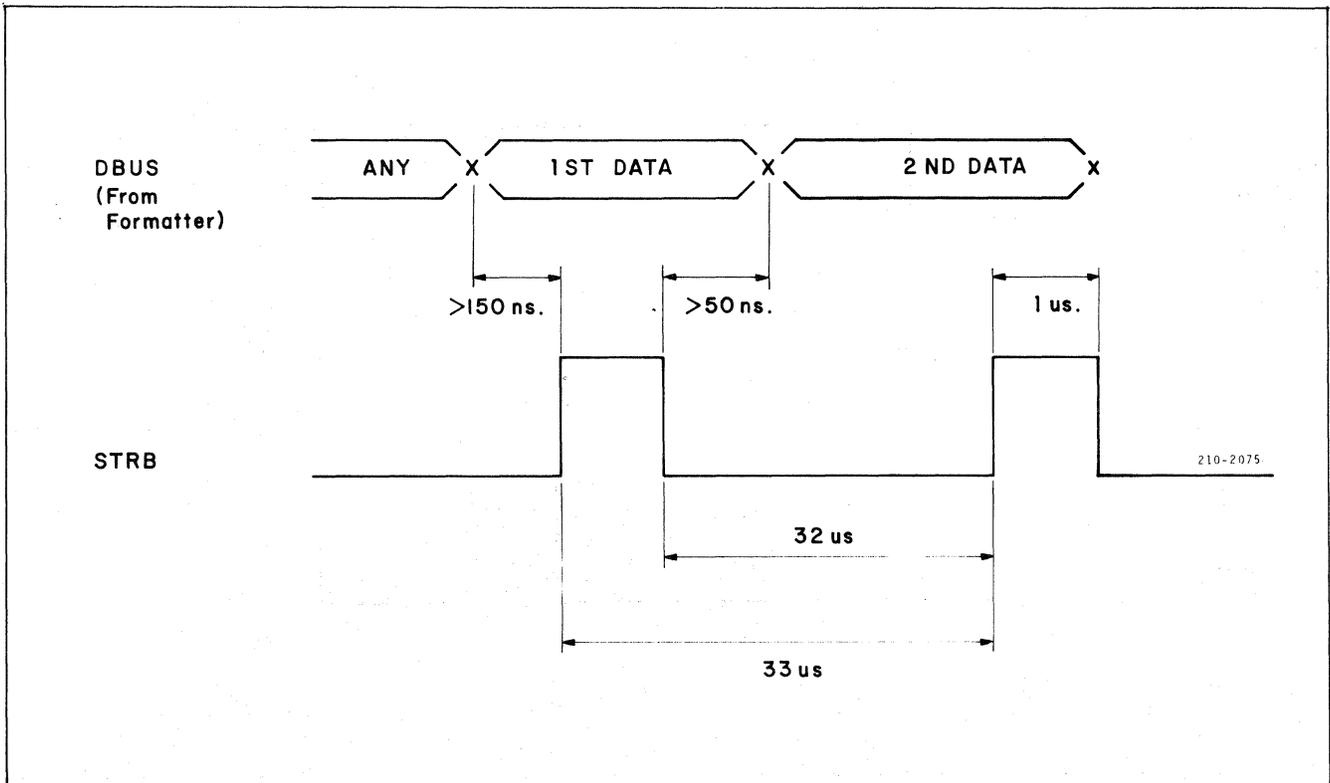**Figure 1-6. Data Busy Timing**

Figure 1-7. Data Ready Timing

Figure 1-8. Data Input Transfer (Read)

Argument Transfers from Formatter to Host

In this case, the transfer proceeds in a manner similar to the above except the data moves in the opposite direction. Please refer to figure 1-4 during this description. The transfer begins by the host releasing its control over the data bus and asserting CREQ. The formatter then places the argument on the data bus and asserts STRB. The host signifies to the formatter that it has accepted the data by denying CREQ. The formatter will then release its control over the data bus and deny STRB.

Data Transfer from Host to Formatter (Write)

In this case, STRB is used in conjunction with DRDY, DBSY, and CBSY to control the transfer of a block of data. Refer to figures 1-5, 1-6, and 1-7. The operation begins with the host placing the first data byte to be transferred on the data bus and asserting DRDY. When the formatter is able to transfer data, it asserts DBSY and 10 microseconds later, it asserts STRB. The leading edge of this pulse signifies to the host that the formatter has accepted the data and that the host should place the next data byte on the data bus. The host must accomplish this task 150 nanoseconds before the next STRB pulse arrives. This amounts to no more than 40 microseconds after the leading edge of STRB is received at the host. The operation is terminated either when the host signifies to the formatter that no more data is to be transferred (DRDY denied) or when an attempt is made to write more than 16,384 bytes (CBSY denied).

Data Transfer from Formatter to Host (Read)

In this case, the transfer proceeds in a manner similar to the write transfer described above except the data moves in the opposite direction. Refer to figure 1-8.

The operation begins by the host releasing control over the data bus and asserting DRDY. When the formatter is able to transfer data, it asserts DBSY and takes control over the data bus. A minimum of 1.5 microseconds later, it places the first data byte on the data bus and it asserts a 500 nanosecond pulse on STRB. The data will remain stable for at least another 50 nanoseconds after the trailing edge of STRB. The host must check the data bus parity while STRB is asserted.

1.4.4 COMMAND BUSY (CBSY)
Pins 12/11

This line is used by the formatter to inform the host that it is executing a command. CBSY is asserted simultaneously with STRB in the event of a valid command transfer. The duration of CBSY varies depending on the command, but it will always be true at least until the denial of STRB. This line will also be asserted by the formatter in response to the FCLR line being asserted by host. This is a useful mechanism for determining whether or not the formatter is powered up and operational. Also, CBSY is not asserted by the formatter if it does not recognize the command to be performed.

1.4.5 DATA BUSY (DBSY)
Pins 14/13

This signal is asserted by the formatter to indicate a data transfer. It remains true throughout the transfer of a block of data and can be used to "prime" the host's DMA channel. DBSY will meet a setup time of at least 1 microsecond before the first STRB; it will go false no sooner than the leading edge of the last STRB pulse of a block of data. The timing of this signal is depicted in figure 1-6.

1.4.6 DATA READY (DRDY)
Pins 6/5

This signal is asserted by the host to indicate its readiness to begin the data transfer in a read or write operation, and denied by the host following the last byte of data in such an operation. The denial of DRDY must meet the same setup time requirements as a data byte. The timing of this signal is depicted in figure 1-7.

1.4.7 FORMATTER CLEAR (FCLR)
Pins 2/1

This signal is false for normal operations. A true pulse of at least 20 microseconds will be followed by negation of the current command and the clearing of all registers. This will result in an idle condition with all formatter controlled interface lines except CBSY at a false level within 50 microseconds of the end of the FCLR pulse. The CBSY signal shall become true within 15 microseconds after FCLR is asserted if the formatter is powered up and operational. CBSY will remain asserted as long as FCLR is asserted.

Warning: FCLR may result in write errors if transmitted during a write operation.

1.4.8 CABLE MONITOR (CMON)
Pins 34/33

This line is always true when the cable between the host and formatter is properly connected.

1.4.9 DATA BUS LINES

The data bus lines include the eight bit bidirectional data bus and two unidirectional parity lines, formatter parity and host parity.

Data Bus (BUS0-BUS7)
Pins 18-32/17-33

The eight data bus lines are used by the host and the formatter to exchange command, status, read, and write data. The type and direction of each transfer is determined by preexisting conditions within the formatter as described below.

Formatter Parity (FPAR)
Pins 16/15

This signal transmits generated odd parity on the data bus from the formatter to the host, and is valid whenever the data bus contains valid data from the formatter.

Host Parity (HPAR)
Pins 8/7

This signal transmits generated odd parity on the data bus from the host to the formatter, and must be valid whenever the data bus contains valid data from the host.

1.5 FUNCTIONAL DEFINITION

1.5.1 GENERAL

All formatter functions are initiated by a command transfer while CBSY is false. One or more parameters may be transferred thereafter to or from the formatter, or read or write data may follow. This section defines the formatter functions in terms of the commands.

1.5.2 COMMAND FORMAT

Command bytes are formatted as positive binary integers. Valid commands (function codes) are in the range 00000000-00010010. All other function codes are illegal and will result in command errors.

This section describes the valid function codes. For brevity, the valid codes are referred to by their least significant five bits.

The host places a function code on the data bus and issues a CREQ. The formatter will respond with a STRB. Certain function codes will be followed with a series of bytes containing parameters required to perform the function. In the case of a status request, the formatter will supply one or more bytes containing the status information. The drive will assert CBSY for all function codes.

1.5.3 FUNCTION CODES

The 19 function codes are listed in table 1-3 and are individually described below.

Function Code 00000 (Sense Identity)

This command function requests an identity byte from the formatter. After this command is sent to the formatter, the host will issue another CREQ which will cause the formatter to place the identity byte on the data bus. The identity byte is interpreted as a single eight bit positive integer. A value of 00001 identifies the device as a cartridge tape drive/formatter system. Other values are given to other Kennedy peripherals.

Function Code	Function Name	Parameter from Host	Bytes to Host
00000	Sense Identity	0	1
00001	Sense Configuration	0	1
00010	Sense Status	0	2
00011	Rewind	0	0
00100	Load	0	0
00101	Unload	0	0
00110	Track Select	1	0
00111	Erase	0	0
01000	Space Forward	0	0
01001	Space Reverse	0	0
01010	Space Forward FM	0	0
01011	Space Reverse FM	0	0
01100	Read	0	0
01101	Write	0	0
01110	Write Extended	0	0
01111	Write FM	0	0
10000	Write FM Extended	0	0
10001	Edit	0	0
10010	Fixed 3" Erase	0	0

Table 1-3.
Functional Codes

Function Code 00001 (Sense Configuration)

This command function requests a version identity byte from the formatter. After this command is sent to the formatter, the host will issue another CREQ which will cause the formatter to place the version number of the particular unit on the data bus. The configuration byte is interpreted as a single eight bit positive integer. The version is the revision level of the drive.

Function Code 00010 (Sense Status)

This function code will cause the formatter to supply two status bytes which give the host a formatter/tape drive error summary and tape drive position status. The host will output two CREQ pulses following the command. CBSY will remain true during the entire two byte transfer. The formatter will reset the error status bits after this function code is received and status is transmitted. The summary bytes are listed below. Numbers in parentheses are the bit references.

	Byte 1 **Summary Status**		**Byte 2** **Position Status**
NOT READY (7)	The tape drive is not ready because a tape cartridge is not properly loaded.	LOGICAL LOAD POINT (LLP) (7)	The formatter has detected and placed the logical load point of the tape.
DRIVE FAULT (6)	A physical or electrical fault has occurred in the formatter/tape drive system or a broken tape condition exists.	LOGICAL END OF TAPE (LEOT) (6)	The formatter has detected the logical end of tape.
NO CARTRIDGE (5)	The tape cartridge is not inserted in the cartridge tape drive.	FILE MARK DETECTED (5)	The formatter has detected the special file mark character on tape.
FORMATTER ERROR (4)	The formatter has failed the self-test which is done during the execution of the load sequence, or noise was detected in the gap region during a write. If this bit is set, off line diagnostics are required to isolate the fault within the formatter board.	WRITE PROTECT (4)	The write protect plug on the tape cartridge has been detected.
COMMAND ERROR (3)	An illegal function code was sent. This may have been caused by a parity error (q.v.) or by a host processor error.	END OF TAPE (EOT) (3)	Indicates the physical end of tape. This bit is returned after the unload command.
PARITY ERROR (2)	The previous operation involved a function code, address, or data byte with a parity error.	TRACK SELECT BIT 1 (1)	Along with track bit 0, track bit 1 defines the currently selected track.
LENGTH ERROR (1)	A one in this bit position indicates that a record in excess of 16,384 bytes has been transferred by the host. Only 16,384 bytes will be written on tape.	TRACK SELECT BIT 0 (0)	Along with track bit 1, track bit 0 defines the currently selected track.
DATA ERROR (0)	A tape record with a CRC or format error has been detected during a write or read operation. A faulty erase will also issue a data error status.		

Function Code 00011 (Rewind)

This function code will cause the transport to rewind and position the tape at logical load point of track 0 regardless of where the tape is initially positioned. CBSY will remain true from 1 millisecond to 90 seconds.

Function Code 00100 (Load)

This function code is employed whenever a cartridge is freshly loaded into the tape drive, or whenever an initialize is required by the host. When the cartridge is properly inserted summary status bit 5 (NO CART) will go false. Summary Status bit 7 (NOT READY), however, will remain true. The unit will then execute a self test of the formatter electronics. Further operation of the unit is contingent on the formatter's successful completion of the test. Tape tension is

then established by moving the tape at 90 ips to the end of track 0, and rewinding the tape at 90 ips to the load point of track 0. On completion of the loading routine summary status bit 7 (NOT READY) goes false and the READY indicator (optional) is illuminated. CBSY will remain true from 1 to 160 seconds, depending on initial tape position of the cartridge.

Function Code 00101 (Unload)

This function code will cause the formatter to move tape to the physical end of tape (EOT) of track 0. This will allow proper removal of the tape cartridge and minimize the tensioning time required in the Load Command that must follow. The EOT (bit 3) status of the Position Status byte will be set. The NOT READY (bit 7) status of the Summary Status byte will be set.

Note: The only commands allowed after an unload command are load, sense identity, sense configuration and sense status.

Function Code 00110 (Track Select)

This function code in combination with a track address tape position byte will cause the formatter to select the track address and tape position defined in the parameter byte, reposition the tape at 90 ips to LLP or LEOT (5 inches in front of the physical BOT or EOT depending on track address) of the selected track and update the position status byte.

Employing this function code in conjunction with function codes defined below will allow the host to incorporate track selection to enhance file partitioning on tape. CBSY will remain true from 100 microseconds to 90 seconds.

Bit 7	Bit 1	Bit 0	Track Address	Tape Position
0	0	0	0	LLP
0	0	1	1	LLP
0	1	0	2	LLP
0	1	1	3	LLP
1	0	0	0	LEOT
1	0	1	1	LEOT
1	1	0	2	LEOT
1	1	1	3	LEOT

Note: All references to tracks in this document will be made to logical track address rather than ANSI track definitions.

Function Code 00111 (Erase)

This function code causes the drive to erase tape at 90 ips rate in the forward direction. The drive will sense LEOT and automatically stop. CBSY will go false allowing the host to check sense status.

Function Code 01000 (Space Forward)

This function code causes the drive to proceed from an IBG (Inter Block Gap) at 30 ips and move to the next IBG. One record on tape will be traversed. This function is limited to the current track address. If a file mark or LEOT is encountered during the space forward, it will be reported in the position status byte.

Note: A space command given when no data is present is an illegal command and will be flagged as such by setting the command error bit in the sense status byte.

Function Code 01001 (Space Reverse)

This function initiates reverse motion at 30 ips from an IBG to the preceding IBG, covering one data block. The function is limited to the current track address.

If a file mark or LLP is encountered during the space reverse, it will be reported in the position status byte.

Note: The drive will position itself at LLP and stop if no data is encountered before LLP.

Function Code 01010 (Space Forward FM)

This function code causes the drive to proceed at a 30 ips rate in the forward direction until a file mark (FM) is sensed. When a tape file mark is encountered the drive will ramp to a stop in the IBG following the FM. The drive position status byte will indicate that an FM was found. CBSY will go false when FM is encountered. If no FM is sensed, the formatter will stop the drive at LEOT.

Note: A command error will result if no data is encountered before EOT.

Function Code 01011 (Space Reverse FM)

This function code initiates reverse tape motion at 30 ips until a file mark is sensed. When a file mark is detected the drive will ramp down and a file mark indication will be supplied by the position status byte. If no file mark is detected the drive will stop at LLP.

Function Code 01100 (Read)

This function code causes the formatter to read one tape record in the forward direction. After the host issues the command, the formatter will set CBSY true. The host then sets DRDY true. The formatter will then start the drive in motion. When the drive is up to proper speed, the formatter will set DBSY true. A minimum of 1.5 microseconds later the first decoded data byte will be put on data bus. STRB pulses shall be issued continuously until the end of the record, at that time DBSY and CBSY will go false. The formatter decodes the data, removes special format characters, checks the integrity of these characters, and detects data errors using a CRC

(Cyclic Redundancy Check) character. If an error is encountered STRB and DBSY will be denied.

Note: A command error will result if no data is encountered before EOT.

Function Code 01101 (Write)

This function causes a record to be written on tape with standard IBGs. After the host issues the command, the formatter will set CBSY true. The host then sets DRDY true. The formatter will then start the drive in motion. When the drive is up to proper speed the formatter will set DBSY true. A minimum of 1.5 microseconds later the first STRB will be issued to transfer the first byte of data from the host to the formatter. STRB pulses will be issued continuously until DRDY is set false by the host or 16,384 bytes are transferred. If 16,384 bytes are sent, DBSY and CBSY will go false and the record is truncated. The length error bit will be set in the position status byte.

The formatter will perform a read-after-write as the record is being written. Improperly written data, special format characters or a CRC failure will result in the data error status bit being set true.

Write commands initiated from LLP will start the actual writing of data 3 inches from the LLP hole.

Before any write commands are attempted by the host, the write protected bit (position status bit 4) should be checked. A command error bit status will be returned if a write is attempted on a write protected cartridge.

Function Code 01110 (Write Extended)

This function erases 3 inches of tape prior to the writing of the data record. This function is used when rewriting a record with a read-after-write error to move past a potentially damaged area of tape. The function should follow a host initiated space reverse over the erroneous data block. Write Extended cannot be used when the record to be

rewritten is located past LEOT. Command Error and LEOT will be indicated by the status words if this is attempted. Write Edit should not be used for tape editing as tape position will be lost.

Function Code 01111 (Write FM)

This function causes the formatter to write a special coded field on tape to be employed as a tape file mark. Standard IBGs will be placed on either side of the special field.

Function Code 10000 (Write FM Extended)

This function causes an erased gap of approximately 3 inches to be placed on tape prior to writing the file mark. This is done to lower the risk of encountering a physical failure area on tape that may have caused a data error when a write FM was previously attempted. This function should be employed after a write FM function with a read-after-write error and a subsequent host initiated space reverse. This function assumes that blank tape exists beyond the record being written.

Write FM extended cannot be used when the file mark to be rewritten was written past the LEOT. The command error and LEOT bits will be set in the status words if write FM extended is attempted under this condition.

Function Code 10001 (Edit)

This function causes the device to determine the distance between the block to be edited and the head; if necessary, the tape is then repositioned to allow the unit to ramp up to speed and edit the block properly.

Function Code 10010 (Fixed 3" Erase)

This function causes the device to erase 3" of tape at 30 ips. This function could be used in a write error recovery routine instead of the use of the WRITE EXTEND function code. This routine is useful when the user wants to emulate a 1/2" tape unit.

SECTION II

INSTALLATION AND OPERATION

2.1 INSTALLATION

2.1.1 MOUNTING

Physical dimensions and outline of the transport are shown in figure 1-1. The transport requires 4.5 inches of vertical mounting space on an 8.5 inch rack, 14 inches deep. The transport should be located so that the cabling length between the transport and the host controller unit does not exceed 10 feet.

2.1.2 SERVICE ACCESS

Service access to the electronics of the unit is easily available, as the Formatter board is exposed from the top and the Transport Electronics PC board, including the control, servo and analog read and write electronics, is exposed from the bottom of the unit. For replacement of parts it may be necessary to remove one or both boards. To do so, turn the power off, disconnect the connectors to the board and remove the four retaining screws. When replacing the board replace the connectors and mounting spacers and washers in the reverse order of removal. Note that board removal is not required for the replacement of the motor. Access holes for the motor mounting screw are available on both sides of the frame.

2.1.3 INTERCABLING AND POWER CONNECTIONS

The connector pin assignments and cable requirements are specified in Section I of the manual. An external power supply is required for the tape transport. The power supply requirements and connections are listed in tables 1-1 and 1-2, respectively.

2.2 OPERATION

Before operating the unit make certain that all power supply and formatter connections have been made.

2.2.1 CONTROLS AND INDICATORS

There are no external controls on the Model 6455, with the exception of the diagnostic switch described in Section IV of the manual, used to initiate off line test functions. The optional front panel has two indicators — READY and DRIVE ACTIVE. The READY indicator illuminates when a cartridge is properly inserted and the unit has completed its load sequence with the tape properly tensioned and positioned at BOT. The DRIVE ACTIVE indicator illuminates when the drive is performing a function and is not available for other commands.

2.2.2 OPERATING PROCEDURE

After the interface connections have been made as required and the power supply is properly connected to the transport, proceed as follows:

a. Clean the transport magnetic head to prevent degradation of magnetic tape.

b. Using a screwdriver, rotate the write enable plug on the cartridge to the SAFE position for protected read only mode, or away from the SAFE indication for unprotected read or write modes.

c. To insert cartridge, place bottom plane of the cartridge on the lower ridge of the cartridge guide. Slide cartridge all the way in while applying equal pressure at both edges of the cartridge until the cartridge is fully engaged. Following insertion a LOAD command should be issued.

d. To remove cartridge issue an UNLOAD command and wait until the unload sequence, in which the cartridge is advanced to EOT at high speed, is complete. In units with the optional front panel wait until the DRIVE ACTIVE indicator is extinguished. Remove the cartridge by pulling evenly at both edges of the cartridge until it is disengaged.

SECTION III

THEORY OF OPERATION

3.1 INTRODUCTION

The electronics of the Model 6455 are located on two PC boards — the Control/Read/Write board, situated on the bottom of the unit, and the Formatting Electronics board, on top of the unit. The write data and commands are supplied from the host computer to the Formatter board, which handles all the PICO bus handshake protocol, and translates the host commands to transport motion commands. The write data is encoded by the formatter and is sent, along with the motion commands and read threshold select levels, to the transport electronics board. The latter board generates the power output to drive the capstan motor. It also modifies the write data and supplies it to the write head. The transport electronics also contain the read circuitry, which accepts the data from the read head, amplifies it, filters it, digitizes it, then returns it to the formatter for decoding and error correction.

3.2 TRANSPORT ELECTRONICS

3.2.1 INTRODUCTION

The transport electronics are contained on Control/Read/Write board type 6478, located on the bottom of the unit. This board performs all the motion control functions necessary for the operation of the tape drive, as well as the analog read and write functions.

The GO, FAST and FORWARD command lines, supplied from the Formatter board, are decoded to produce one of four possible input voltage references, corresponding to the four motion modes — forward and reverse in high and low speeds. A ramp generator provides linear voltage rise, as required for the acceleration of the capstan. The ramp rise time and the steady state velocity are adjustable using two different potentiometers, as described in Section IV of the manual. Current feedback from the motor, voltage feedback from the tachometer and the input voltage are summed to produce an error voltage supplied to a servo preamplifier. The preamplifier output is modulated by a triangular wave generator, supplying a constant frequency, pulse width modulated driving voltage to the servo power amplifier. The power amplifier then drives the capstan motor in the desired speed and direction. Additional circuits provide a servo disable in the event of power loss or a jammed cartridge, and a dead zone to prevent capstan creep.

The write circuitry accepts the encoded GCR data from the formatter, along with a 16 — BIAS square wave signal, Select Write Status SWS/ and the track select lines. The track select lines are decoded, energizing the head winding of the selected track. A

high amplitude step is superimposed on the data to improve signal symmetry, and an AC bias at 8 times the data frequency is added to reduce read-after-write cross talk. Provision is also made to increase the write current when using 600 foot tapes.

The read circuits on this board differentially amplify the read head signal, filter it, detect the crossover point, and digitize it. Threshold circuits eliminate erroneous decoding due to base line noise. The threshold voltage level is determined by the state of the THRES.A and THRES.B lines, supplied from the Formatter board. The threshold is changed during error recovery routines in order to optimize read data recovery. The digitized data is then supplied to the Formatter board for decoding and error detection. Also included on the board are the A and B hole detection circuits, and the SAFE and Cartridge In Place (CIP) circuits.

3.2.2 REFERENCE VOLTAGE GENERATOR

(Schematic 645, sheet 2)

The Forward (FWD/) and FAST/ command lines supplied from the formatter are decoded by binary-to-BCD decoder IC25 when the GO/enabling level is low. One of the four outputs of IC25 goes low, as tabulated below, causing the output from its associated gate to go high. Depending on the selected speed and direction, one of resistors R101 through R104 determines the proper current to be applied to two stages of operational amplifier IC38. The Forward and Fast Forward reference voltages are applied to the inverting input of operational amplifier IC38-9; the reverse and fast reverse reference voltages are applied to the noninverting input. Thus, forward speed reference voltages will be negative, while reverse speed reference voltages will be positive, as tabulated.

Input Command	IC25 Active Output	Reference Voltage (IC38-8)
Forward	10	-2.5v
Fast Forward	12	-8.0v
Reverse	9	+2.5v
Fast Reverse	11	+8.0v

3.2.3 RAMP GENERATOR

(Schematic 645, sheet 2)

The ramp generator circuit develops the start and stop ramps necessary for the linear acceleration of

the capstan motor to the desired speed. It consists of two operational amplifiers IC38, a full wave bridge (CR26, CR27, CR28 and CR33), ramp timing capacitor C75 and related components.

Reference voltage from the reference generator is applied to the inverting input of IC38-13. The output of IC38 is applied to steering diodes CR26, 27, 28 and 33, and resistors R130, 145, 146 and 150. This network comprises a bidirectional constant current switch. Initially, the output at IC38-1 is saturated for the time required to charge ramp timing capacitor C75. After it charges, feedback at IC38-12 causes voltage and current to level off. Potentiometer R145 is used for ramp time adjustment. Ramp adjustment procedure is included in the maintenance section of the manual.

3.2.4 SERVO PREAMP AND POWER AMPLIFIER

(Schematic 645, sheet 2)

The servo preamp consists of 3 sections of quad comparator IC39, with outputs at pins 1, 7 and 14. In addition it includes comparator IC31-14 and related circuitry. The ramp input supplied from the ramp generator is summed with the tach output at IC39-13 to provide a speed correction voltage which is amplified and appears at IC39-14. The motor speed is adjusted by potentiometer R144. Motor current is sensed through resistors R152 and R154 which act as current to voltage converters. This voltage is differentially amplified by IC39-7 and summed with the speed correction voltage to provide speed stabilization. The signal is then integrated by IC39-1 and capacitor C81 to produce an overall error signal which drives the servo power amplifier. Comparator IC31-14 is used as a driver to turn off FET switch Q13 when SERVO DISABLE/ is generated either due to a power failure or during the servo input dead zone, which falls at +/-10% of the base line. Resistors R138 and R139 provide current limiting for the power amplifier.

The network including transistor Q14, FET Q15 and their associated components is used to increase the current supplied to the servo power amplifier during ramps by connecting resistor R159 to the current limiting network.

The constant frequency, pulse width modulated switching power amplifier is comprised of a triangle generator IC31-1, comparators IC31, pins 2 and 13, power drivers IC29, IC30 and a switching bridge that includes Q9 through Q12 and CR20 through CR23. Comparator IC31-1 is configured as a square wave relaxation oscillator and generates a triangle waveform. This triangle wave acts as a reference voltage which is applied to the inputs of comparators IC31 at pins 4 and 11. The error signal developed by the servo preamp is applied to the IC31 comparators at pins 5 and 10. When the input correction voltage at IC31-5 exceeds the triangular wave amplitude at IC31-4, the output of the comparator at IC31-2 swings high, enabling driver ICs 30-5 and 29-3. These in turn switch on transistors Q9 and Q12, routing the

current through pin J6-6 to the motor and returning it through J6-5. Similarly, when the correction voltage at IC31-10 is exceeded by the triangular wave amplitude at IC31-11, the comparator output at IC31-13 swings high, activating drivers IC30-3 and IC29-5. These in turn switch on transistors Q11 and Q10, routing the current through J6-5 to the motor and returning it through J6-6, causing the current to flow in the opposite direction through the motor.

Resistors R81 and R84 insure that IC31-10 is always higher in voltage than IC31-5, thus providing a voltage guard band or dead zone twice during each switching cycle. During this dead zone, comparators IC31-13 and IC31-2 are low, turning off drivers IC29 and IC30 as well as all the bridge transistors to prevent power bridge cross conduction. The power bridge may also be turned off by the application of SERVO DISABLE/ which similarly turns off drivers IC29 and IC30.

Inductor L6 dampens the motor current pulses to reduce RMS heating of the motor. Catch diodes CR20 through CR23 form a return path for the motor current when the bridge is turned off. Baker clamps in the form of Q7 and Q8 provide current limiting.

3.2.5 TAPE MOTION SENSING CIRCUITRY

(Schematic 645, sheet 2)

This circuit, consisting of ICs 33, 40 and 26, threshold detects the tachometer output voltage and supplies MOTION true whenever the tach output exceeds either the negative (-0.1v) or the positive (+0.1v) threshold voltages. Threshold detection is performed by two sections of quad comparator IC33, using scaled positive and negative 12v supply voltages as reference. When the tach output falls between +0.1v and -0.1v, the outputs of both comparators are high, are inverted by IC40, setting both inputs to exclusive-OR IC26 low, keeping MOTION low. When the threshold voltages are exceeded in either direction the output of one comparator swings low, setting one input to the exclusive-OR gate high, generating MOTION high true. MOTION is supplied by bus interface chip IC20 (schematic 645, page 1) to the formatter where it is monitored by the microprocessor.

3.2.6 SERVO DISABLE CIRCUITS

(Schematic 645, sheet 2)

SERVO DISABLE/ true is generated either when the supply voltages fall below the specified limits or when the magnitude of the servo driving voltage falls below 0.1v.

The voltage dependent disable circuit includes 4 sections of quad comparator IC32, transistor Q6 and their associated components. A 4.3v reference voltage is established by zener diode CR24 and resistor R122. The reference voltage is supplied to comparators IC32-4 and IC32-8. When either the +24, +5 or -12 volt supplies fall below the allowed limits (+15.3, +4.77 and -10.9, respectively) as established

by the resistor networks, the output of the respective comparator swings low, causing the output of comparator IC32-1 to swing high, turning on transistor Q6 and generating DISABLE/ low true. DISABLE/ is supplied to the write circuitry (see schematic 645, sheet 4) to inhibit the write current. DISABLE/ is also wire-OR'ed with the servo generated disable to generate SERVO DISABLE/ true. The latter signal causes the output of comparator IC31-14 to swing high, turning on FET Q13 and shorting the output of servo preamp IC39-1, discharging capacitor C81. This prevents any bias voltage from accumulating and inhibits the output to the servo power amplifier, inhibiting all tape motion.

SERVO DISABLE/ is also generated by a servo dead zone circuit consisting of two sections of comparator IC33, inverter IC40-4, and associated components. Voltage references VREF1 and VREF2 establish plus and minus 0.1v threshold levels, respectively, for the two comparator sections. When the output of the ramp generator falls below +/-0.1v in magnitude the output of either IC33-2 or IC33-13 swings high. The RC network including R147 and C87 filters the output for high frequency transients. The high output is then inverted by IC31-14 to generate SERVO DISABLE/true.

3.2.7 CURRENT MONITOR CIRCUIT

(Schematic type 645, sheet 2)

The summed tachometer and ramp generator voltage, SUM OUT, is rectified by diodes CR36, CR37 and op amp IC39-8. The rectified voltage is applied to an integrator including IC38-7 and capacitor C86. Schmitt-Trigger inverter IC7-6 is biased to the on state by a dividing network including R167, R168; consequently IC7-6 is normally low, generating CURRENT LIMIT FALSE, or Current Monitor CMON/ true. When the SUMOUT voltage is high enough for a long enough period of time to cause excessive motor current, integrating capacitor C86 would accumulate enough negative voltage to lower the input voltage at IC7-5 below 0.9v. This is low enough to swing the output high and generate CURRENT LIMIT TRUE. CURRENT LIMIT is supplied to the Formatter board through J1-34, where it is polled by the microprocessor.

3.2.8 A AND B HOLE DETECTION CIRCUITS

(Schematic type 645, sheet 1)

The A and B holes are sensed by these circuits, converted into DC coupled TTL signals and output to the formatter to indicate tape position. Since both hole detection circuits are identical, only the hole A circuit will be discussed.

An infrared light source is generated by an infrared emitting diode driven by a constant current source consisting of transistor Q5 and its associated components. When a hole A is detected the infrared light is collected by the base of the phototransistor, increasing the output voltage at its emitter. When the voltage level exceeds the reference (0.2v) at the noninverting input of comparator IC18 at pin 5, the output of the comparator at pin 7 swings low. Resistor R52 in the feedback path provides DC hysteresis for noise immunity. The signal is appropriately filtered by R53 and C46, stretching the output by an additional 2 to 3 milliseconds. This compensates for mechanical sensor and hole skew to ensure A-B hole overlap when both A and B holes are present simultaneously. The signal is then shaped and limited by Schmitt-Trigger IC19-2, is inverted by IC19-12 and is presented to the formatter through transceiver IC20 when DISABLE/ is false.

3.2.9 SAFE AND CARTRIDGE IN PLACE SWITCHES

(Schematic type 645, sheet 1)

When a cartridge is properly inserted, the Cartridge in Place switch CIP is closed, applying +5v to inverter IC40-9. The output of the inverter goes low, supplying CIP/ true to the formatter through transceiver IC20-13. When the cartridge is improperly inserted the switch remains open, supplying CIP/ false (high).

When the SAFE plug on the inserted cartridge is in the file-protect position the SAFE switch on the transport remains open. This inhibits the write current by grounding the WRITE CURRENT signal and grounds the input to inverter IC40-11. The inverter output supplies SAFE high true to the formatter through transceiver IC20-12, indicating that the inserted cartridge is file protected and cannot be written on. When the SAFE plug is in the write enable position the SAFE switch is closed upon cartridge insertion, enabling the write current and supplying SAFE false to the formatter.

3.2.10 POWER REGULATION

The Model 6455 requires externally supplied +24vdc +/-25% and +5vdc +/-5% inputs. These input power levels are internally stepped down and regulated to produce +12 vdc by IC36, and -12 vdc by IC37 (schematic type 645, sheet 1). The +12v and -12v lines are in turn stepped down by regulators IC13 and IC14 (schematic type 645, sheet 3) to produce +6v and -6v supplies, respectively. The latter are used to power the video amplifiers in the read chain.

3.2.11 ANALOG READ ELECTRONICS

(Schematic 645, sheet 3)

The analog read electronics section differentially amplifies the head output, filters it, differentiates it, detects the zero-cross-overs and generates a clock pulse that is delayed approximately one-half a data cell. The clock pulse latches the read data, provided its amplitudes exceed the selected threshold. The data is then supplied to the formatter for decoding and error detection.

The track select lines, TRK SEL0/ and TRK SEL1/, are converted from TTL to CMOS levels by voltage

translator IC11, and are supplied to dual 4 channel analog data selector IC10. The state of the track select lines determines which data track will be read, as tabulated below.

TRK SEL 0/	TRK SEL 1/	SELECTED TRACK
Low	Low	1
Low	High	2
High	Low	3
High	High	4

Positive and negative read data signals from the head are differentially amplified by the first of 3 video amplifiers, IC4. The first stage amplifies the signal by a factor of 100, approximately. The amplified data is then passed through a third order Bessel filter — a low pass, constant time delay filter. The filter attenuates the high frequency noise while minimizing peak shift. The data itself is also attenuated by a factor of 2, approximately. The filtered data is supplied to the second video amplifier, IC5, configured as an active band pass differentiator. The differentiator converts the peak voltages to transitions through zero while providing gain equalization at the different data frequencies. The output data is shifted by 90 degrees and supplied to the third video amplifier, IC6. This amplifier stage has adjustable gain. Using potentiometer R16, the gain is adjusted to 3v peak-to-peak while writing all 1s file marks. The amplified data is filtered once again by another Bessel filter, identical to the first, and supplied to the digitizing stages. These consist of a zero-cross-over detector, a pulse generator and a time domain one-shot, in addition to threshold circuits, a gap detect one-shot and a data latch. The zero-cross-over detector, IC22, is extremely sensitive, saturating in the positive direction each time the analog data exceeds zero, and returning to ground each time the data amplitude falls below zero. The resulting square wave is supplied to a pulse generating circuit consisting of 2 sections of exclusive-OR gate IC23, resistor R63 and capacitor C42. The pulse generator produces a 0.16 us pulse on both the positive and negative going edges of the square waves. The leading edge of each pulse triggers one-shot IC24, producing a 2 us pulse, equivalent to approximately half a data cell. During 90 ips operation FAST/ true, supplied from the formatter, is inverted by IC27-3, an open collector gate, adding R64 in parallel to R68. This reduces the RC time constant of one-shot IC24 by a factor of 3, generating a 600 ns pulse, as required for the shorter data cell period in high speed operation.

The negative edge of the pulse output by IC24 clocks J-K flip-flop IC28. The state of the data to be stored by the latch is determined by the output of the two IC35 comparators. The inverting input of each comparator section is connected to the threshold voltage, as determined by the threshold circuit described below. The noninverting input of each comparator is connected to the +v and -v of the read signal. Since +v and -v are 180 degrees out of phase, +v goes positive during positive transitions and -v

goes positive during negative transitions. Thus only a single positive threshold voltage is necessary.

Whenever the threshold voltage is exceeded by the positive data signal, the output of IC35-12 swings high, setting the J input of flip-flop IC28-3 high. This causes the READ DATA output to go high following the next clock pulse. Similarly, when the negative voltage output exceeds the threshold, the output of comparator IC35-7 swings high at the K input of the flip-flop, causing READ DATA to swing low following the next clock pulse. READ DATA is supplied to the formatter where it is decoded, checked for errors, reformatted and output to the controller on the data bus.

The threshold voltage selection circuit includes ICs 26, 27 and their associated components. The threshold level is determined by the state of the HI THRESH, LO THRESH/, and FAST/ lines, supplied from the formatter microprocessor. During a normal read operation the voltage threshold is set at 5.7% of the signal by resistors R71, R66 and R69. Capacitors C58 and C53 provide filtering. Note that the amplitude of the read signal varies according to the data pattern, and that the threshold percentage calculation is based on the low amplitude signal. If a read error is detected by the formatter, an error recovery routine is initiated, in which the threshold level is alternately lowered, in an attempt to recover partial dropouts, and then raised, eliminating possible base line noise. The different threshold levels are tabulated below.

	Voltage (mv)	% of Read Signal
Low	14.6	2.9
Normal	28.4	5.7
High	108.3	21.7
Fast	200.0	40.0

During the interrecord gap the data latch, IC28-6, is returned to a known state by one-shot IC24-13. During the data block the one-shot is triggered each time comparator IC35-12 switches to a high state. The one-shot is consequently retriggered by each negative transition in a block, keeping the Q output of the one-shot high. When no data is detected for a period of 18 us, equivalent to approximately 4 data cells, the output of the one-shot goes low, clearing the data flip-flop at IC28-4.

3.2.12 ANALOG WRITE CIRCUITRY

(Schematic type 645, sheet 4)

Write data is supplied from the formatter along with the 16xBIAS signal, track select lines TRK SEL0/ and TRK SEL1/, and Set Write Status SWS/. When SWS/ is true and DISABLE/, generated on this board in the event of a power loss (see page 2 of the schematic) is false, IC17 decodes the track select lines, enabling a single track as tabulated below.

TRK SEL 0/	TRK SEL 1/	SELECTED TRACK
low	low	1
low	high	2
high	low	3
high	high	4

The low output of IC17 turns on one of transistors Q1 through Q4, routing the write current to the head winding of the selected channel. Note that the write current is disabled if the SAFE switch of the inserted cartridge is in the safe position.

The write data from the formatter is routed to a pair of exclusive-OR gates, IC16-2 and IC16-13. Note that one input to IC16-1 is tied to +5v while one input to IC16-12 is tied to ground. When the input data is low the upper exclusive-OR output will be high, activating the write buffer connected to the positive side of the head winding; normally this would be IC1-11, but when 600 foot tapes are used it would be IC1-3. When the input write data is high, the output of exclusive-OR IC16-11 will go high, activating write buffer IC3-8 (IC3-6 for DC600A cartridges), energizing the negative side of the selected head winding.

A high amplitude write step is generated by the edge detection network consisting of 2 D-type flip-flops IC15 and exclusive-OR gate IC16-8, and by one-shot IC7. Following each write data transition, positive or negative, exclusive-OR gate IC16-8 generates a delayed positive pulse which triggers one-shot IC7, generating a pulse approximately 2 us long, equivalent to about one half of a data period. That pulse is gated either through IC8-6 or IC8-3, depending on the state of the data, and activates write buffer IC1-6 when the input write data is low and IC3-11 when the input data is high. The activated buffer superimposes a doubled amplitude step on the first half of each data cell, either in the positive or negative direction. This improves the wave symmetry and maximizes the readability of the data.

The 16xBIAS square wave supplied from the formatter is halved by D-flip-flop IC9-3. The Q and Q/ outputs of the flip-flop alternately activate buffers IC2-3 and IC2-8 (or IC2-11 and IC2-6 for 600 foot tapes), superimposing a high frequency AC bias on the heads. The AC bias is of too high a frequency to actually be written on tape, and is used to minimize read-after-write cross talk.

When a 600 foot tape is used the higher coercivity of the tape requires higher write current to be used. To adjust for that, jumper J2 is moved to ground one input to exclusive-OR gate IC16-5, the output of the gate going high. This enables an alternate set of write buffer gates with smaller valued resistors at their outputs, increasing the resultant write current.

Diodes CR1, 6, 11 and 12 are used to eliminate reverse current spikes when writing is terminated.

3.3 FORMATTING ELECTRONICS

3.3.1 INTRODUCTION

The formatter performs all necessary functions to read and write cartridge tapes in 6400 bits per inch, GCR coded format, operating at 30 inches per second. All formatting electronics are contained on a single board mounted on top of the Model 6455. The formatter accepts commands and write data from the host computer, converts the data into GCR coded format and translates controller commands into transport motion commands, satisfying all interlock and timing requirements. The formatter also decodes GCR encoded data supplied from the Transport Electronics board in digitized form, performs error checks, and supplies the appropriate logic levels to the host controller. A block diagram of the formatter is shown on sheet 1 of schematic 5563. The formatter consists of the following functional blocks:

a. An Intel 8035 microprocessor, which controls all aspects of host/formatter communication, oversees tape drive operation, drive and status processing, and initiates the read and write sequences by forcing the read and write sequencers to a particular address. The microprocessor also assembles the two status bytes — the summary status byte used to flag error conditions, and the position status byte used to identify transport condition.

b. A crystal oscillator network which generates all the internal clocks.

c. A read microsequencer network which oversees read data decoding, read CRC check, read timing network synchronization, and host/formatter read handshake logic. The read microsequencer controls the mode of operation of the read timing network.

d. A read timing section consisting of a phase locked oscillator (PLO) and support logic, used to synchronize the read clock with the detected data transitions.

e. A write microsequencer network, used to control data encoding, write parity check, CRC generation, and host/formatter write handshake logic.

f. A write precompensation network which determines write timing, providing precompensation for peak shift.

3.3.2 GCR ENCODING

The formatter encodes host data into a high efficiency 4 to 5 bit run length serial data stream in which a one is represented as a transition and a zero

by a lack of transition through a data period. The preamble supplies 80 consecutive transitions at 8000 frpi to allow the PLO to achieve frequency and phase synchronization.

Every four bit length nibble from the host is encoded into a five bit length Group Coded Record (GCR) having at most two consecutive zeros (see table below). The formatter precedes each block of data with an interblock gap, a preamble of 80 consecutive 1s, and a synchronization test character (00111). Encoded data is followed by a distinct end mark character (11111) and a 16 bit CRC character. Each block terminates with a postamble of 80 consecutive 1s, and is followed by an interblock gap. A file mark consists of a preamble, sync, reverse sync (11100), postamble combination. Write precompensation is applied to written data to reduce the effect of transition peak shift encountered at high density.

GCR CODE

Host Data	Coded Data
0000	11001
0001	11011
0010	10010
0011	10011
0100	11101
0101	10101
0110	10110
0111	10111
1000	11010
1001	01001
1010	01010
1011	01011
1100	11110
1101	01101
1110	01110
1111	01111

GCR BLOCK FORMAT

Preamble (80 1s)
Sync (00111)
Data
End mark (11111)
CRC (16 bits)
Postamble (80 1s)
Interblock gap

3.3.3 CRYSTAL OSCILLATOR NETWORK

(Schematic sheet 6)

The crystal oscillator timing network is used to supply the formatter with a master write timing clock, W64.CLK. Various divisions of this clock are used to synchronize the different write and read functions.

The master frequency for the formatter is supplied by a 15.36 MHz crystal in a feedback loop between two inverter sections of D10. The resultant 15.36 MHz square wave, W64.CLK, is divided by 4 bit counters H10 and H11, connected in tandem. The counters

provide W32.CLK, W16.CLK, W8.CLK, WSEQ.CLK (W4.CLK), and GAP.CLK (W1.CLK) operating at 1/2, 1/4, 1/8, 1/16, and 1/64 the frequency of W64.CLK, respectively. W64.CLK is used to clock the data transition detector and the PLO comparator stage. At 7.68 MHz, W32.CLK is used to clock the write precompensation circuitry. W16.CLK, operating at 3.64 MHz, is sent to the write head as 16x.BIAS, to optimize the writing of the data. It is also used to replace VCO.CLK during signature analysis testing, effectively bypassing the tape drive and PLO network. At 1.92 MHz, W8.CLK serves to synchronize the jamming of microprocessor commands onto the write microsequencer bus at the appropriate point in the microsequencer timing cycle. WSEQ.CLK, the write microsequencer clock, running at 0.96 MHz, is used to clock all write microsequencer/write precompensation timing. This clock also enables the processor/write sequencer interface. GAP.CLK, the slowest of the write clocks, is used by the PLO network during the gaps to keep the oscillator running at the data rate.

3.3.4 CENTRAL MICROPROCESSOR

(Schematic sheets 2, 3 and 4)

An Intel 8035 microprocessor with a 6.0 MHz clock is used to coordinate drive motion, resolve logical load point/end of tape conditions, attend to tape hole status monitoring, manage the serpentine tape track control, and assign microsequencer tasks. The microprocessor also oversees the 6455/host interface, accepting host commands with a handshake CREQ/CBSY protocol and initiating the appropriate functions. The central processor is also used as a debug tool to test microsequencer logic nodes, stimulating roughly 80% of the 6455 circuitry for signature analysis testing. Other microprocessor diagnostic tools are also available.

The microprocessor contains an arithmetic logic unit (ALU), an instruction decoder, 128 x 8 bit bytes of random access data memory, a 12 bit program counter, an 8 level program stack, a maskable interrupt, an 8 bit timer/counter, two eight bit I/O ports (P1, P2), and a tristate 8 bit I/O port (P0), all on one integrated circuit. The microprocessor is the main control element for the Formatting board.

The microprocessor program is contained in EPROM A3. During the instruction fetch cycle the contents of the program counter internal to the processor are presented on the data bus and on the lower 4 bits of port P2. On the trailing edge of Address Latch Enable (ALE) the address is latched into 8 bit latch A5. PSEN/ indicates that an external instruction fetch is in progress and is used to enable the ROM. The data bus is then switched to the input mode and accepts the 8 bit instruction word.

The lower 4 bits of P2 are also used to transmit I/O information, which is latched into A2 on the rising edge of ALE. The lower 3 bits of P2 are used as the address lines for the read I/O decoder (B7) and the

write I/O decoder (B8). The two decoders are used to select the devices on the control bus and to control some of the diagnostic functions.

The 8 bit I/O port P1 is assigned as the data bus for the formatter. All formatter commands and data are transmitted on this bus, but only commands and status are actually received and generated by the processor. All data are routed to the read and write sequencers.

The host interface signals are buffered by two 8 bit transceivers (A8, A10, schematic page 2). A8 is the data bus transceiver and its direction is controlled by bit four of port P2 (DATA.BUS.IN/). A10 buffers all of the formatter control and handshaking lines. The data on the data bus are checked for correct parity on input by parity generator/checker A7, which also generates the output parity when the data is output to the host. The parity is made available to the processor and the write sequencer on the FMTR.PAR/ line.

Eight bit latch B1 (schematic page 2) is enabled by the RD.IO.EN/ line from the read I/O decoder and is used by the microcomputer to read the status of the Data Ready (DRDY/) line during normal write operations. The other seven lines are used by the processor to load the contents of diagnostic switch SW1. The processor then responds by selecting the required diagnostic routine.

The drive control lines include three motion control lines (FWD, FAST and GO), two track select bits (TSA and TSB), two read threshold bits (THRES.A/, THRES.B/) and Set Write Status (SWS). The control lines are sent to the transport electronics board via the control bus. They are latched into 8 bit latch H1 (schematic sheet 4) by DRV.OUT.EN/ and are buffered by J1. Inputs from the transport electronics board include A and B hole indications (A.HOLE, B.HOLE), digitized GCR data (RD.DATA), Cartridge In Place flag (CIP), motion flag, and a write protect indication (SAFE). These lines are buffered by J2 and are read by the processor via 8 bit latch H2 when DRV.INP.EN/ is activated.

The processor controls the write sequencer (E6, sheet 5) via 8 bit tristate latch E1. The processor jams the program starting address of the write sequencer routine to be executed into latch E1. Flip-flops H7, C7 and gate K9 synchronize the start address onto the sequencer address bus during the proper address cycle. The sequencer continues executing instructions from the new address until the routine is terminated. When the write sequencer is idle it loops on address zero. The processor controls the read sequencer (C6, schematic sheet 7) via 8 bit latch C1. The processor jams the read sequencer starting address into latch C1. Flip-flops A14 (schematic sheet 8), C7 (sheet 7) and gate A13 (sheet 8) synchronize the starting address onto the microsequencer address bus during the address cycle. Upon completion of read activity RD.STAT.EN is used to obtain a summary status byte from the read

sequencer, indicating read/write error conditions. RD.STAT.EN causes this byte to be loaded from the read sequencer general purpose counter to CNTR.BUS. Upon termination of read activity the read sequencer loops on address zero.

3.3.5 READ TIMING NETWORK
(Schematic sheets 9, 10 and 11)

The read timing network consists of a phase locking oscillator (PLO) which generates VCO.CLK, a frequency 16 times the read data rate, used to clock data recovery operations. This frequency is derived using a voltage controlled oscillator (VCO) whose center frequency is 16 times the bit encoding rate. The VCO output is divided by 16 and its phase is compared with the phase of the read channel during the data, and a crystal derived reference frequency, GAP.CLK, during the gaps. The output of the phase comparator is supplied to an integrating operational amplifier network which provides the corrective voltage to the VCO. If the VCO phase lags the phase of the read reference input, an increased corrective voltage will be supplied to the VCO. Conversely, if the VCO phase leads that of the input data, the VCO corrective voltage is decreased until the VCO matches the read reference. The read timing network has two modes of operation: acquire mode and track mode. During the gaps and the initial portions of the preambles the timing network functions in the acquire mode, with enhanced comparator feedback. Tracking mode is selected after successful preamble recovery. During the tracking mode the comparator feedback is reduced to emphasize correction of tape speed variance, rather than individual magnetic bit drift. The clock output by the read timing network, VCO.CLK, is halved to provide the read sequencer clock RSEQ.CLK, and divided by 16 to provide VCO.STRB, used to clock the data retrieval functions.

As mentioned earlier, during the gaps the crystal generated GAP.CLK is used to maintain the PLO frequency at the data rate. Once data is detected DATA/, the GCR data supplied from the transport electronics board, is input to an edge detection circuit consisting of flip-flops K13 and exclusive-OR K12. K12-6 supplies a pulse 1/64 of a character wide upon each data transition, labeled DATA.STRB. DATA.STRB is supplied to two read envelope detection circuits (schematic page 9). One consists of counter F13 and flip-flop J13. The arrival of each data transition presets the counter to count 9, and clocks flip-flop J13 to the set state, supplying R.ENV/ true to the microprocessor.

If 6 data periods pass without the arrival of DATA.STRB, the carry output of the counter goes low, resetting R.ENV/ false. This signal informs the microprocessor of the beginning of the gap. The other read envelop detector is used by the read sequencer. It consists of two C9 flip-flops. The first is set by DATA.STRB while the second is clocked by R.SEQ.CLK/, supplying R.ENV.ENBL to the read

sequencer input. Upon detection of the read envelope the sequencer issues RD.GATE true, used to switch the PLO reference frequency from GAP.CLK to DATA.STRB. The sequencer then issues PLO.JAM, which is synchronized by RD.DATA.STRB to produce JAM.LD/ (schematic page 9). JAM.LD/ presets the comparator flip-flops and counters of the PLO, synchronizing the PLO to the data stream. After 60 bits of the preamble the read sequencer issues PLO.TRK.EN to switch the PLO from the acquire to the tracking mode. The acquire and track modes differ in that the timing network receives continuous DATA/transisionts in the acquire mode, used during the interblock gaps and the preambles. In the track mode, while decoding actual data, there will be gaps of up to two bit cells in incoming data transitions, representing up to two consecutive zeros permissible in GCR data. The effect of the corrective feedback during the tracking mode is reduced by the larger resistor values used in tracking mode (R25, R28) as opposed to those used in the acquire mode (R26, R27), reducing the input current to the integrator network. This slows down the response of the PLO to peak shift variation while correcting for tape speed variation.

In the acquire mode, the VCO output is compared to the data strobe by flip-flops E15-5, E15-9. If the RD.DATA.STRB/ and VCO.CLK/ are synchronized, both comparator flip-flops are clocked to the set state simultaneously, generating PMP.AQ high and PMP.AQ/ low. When the two lines are in opposite states, the correction input to the phaselock loop is self-cancelling, and the same VCO frequency is maintained. The set-reset flip-flop consisting of two sections of D14 will be reset following a propagation delay, and D14-3 will clear both E14 flip-flops, again returning PMP.AQ and PMP.AQ/ to opposite, self-cancelling states.

When the VCO phase lags the data strobe flip-flop E14-5 will be set while E15-9 will remain cleared for the duration of the phase discrepancy. During this time both PMP.AQ and PMP.AQ/ will be high. These signals are inverted once and are supplied to the inverting input of the first of three cascaded op amps, E16, F16 and H16 (see schematic page 11) connected as a second order integrator. The final integrator stage supplies an increased positive voltage to VCO K16, increasing its output frequency until it matches that of the incoming reference frequency. Similarly, when the VCO phase leads the data strobe, E15-9 will be set while E15-5 will remain cleared for the duration of the lead, and both PMP.AQ/ and PMP.AQ will be low. This reduces the input voltage to the integrator stages and to the VCO, reducing the output frequency.

In the data tracking mode two H15 flip-flops are used to generate the feedback voltage to the PLO. The output of one-shot flip-flop H15-5 goes low 50% of a data period after each read strobe transition, and it is this output which is compared to the VCO output. This half a cell delay provides a look-ahead ability which allows the loop to not respond to lack of transitions. Each RD.DATA.STRB/ clocks flip-flop

H15-5 to the set state, generating PMP.TRK/ low. The high Q output also enables 5 bit counter F15, F14 by activating D15-3. The counter is clocked at 64 times the data rate by crystal generated W64.CLK. Following 32 counts, equivalent to the ideal half bit period, F15-5 goes high, resetting flip-flop H15 at pin 15 and switching PMP.TRK/ to a high state Thus PMP.TRK/ is low for the first half of a character period and high for the second half following each data transition. The correction to the VCO frequency is provided by the second H15 flip-flop. VCO.CLK/ is divided by 16 by counter H14 to provide a data frequency pulse. The pulse is inverted by K12-3 and clocks F15 to the set state on its trailing edge, setting the Q/ output at F15-7 low. If the VCO phase leads that of the data strobe, the Q/ output would direct set flip-flop H15-10, setting PUMP.TRK low. This reduces the input voltage to the integrator and to the VCO, slowing it down. Conversely, if the data strobe leads the VCO, RD.DATA.STRB clocks H15-7 to the clear state, generating PUMP.TRK high, increasing the input voltage to the VCO, thus speeding it up until its phase matches that of the incoming data.

The integrator bias is set by a resistor network including potentiometer R31. The bias adjustment is made with the tape at rest by observing the output of the acquire comparator flip-flops at test points TP1 and TP2, using an oscilloscope set to 1 usec, 2v/division, with channels 1 and 2 added. Potentiometer R31 is then adjusted until minimum amplitude is displayed.

VCO.CLK/, the output of the PLO, is divided by two by flip-flop C13 to provide the read sequencer clocks, RSEQ.CLK and RSEQ.CLK/. VCO.CLK is also divided by 16 by counter H14 to supply VCO.STRB, the clock used to synchronize the GCR data separator. The data separator includes two H13 flip-flops and flip-flop J13 (see schematic page 9). VCO.STRB clocks the first H13 flip-flop to the set state, the Q/ output going low to direct set the second H13 flip-flop. The Q/ output of the second flip-flop returns the first flip-flop to a clear state. If a data transition is detected following VCO.STRB, indicating a 1 bit, DATA.STRB is generated to clock the second H13 flip-flop to the clear state, its Q output going low. The following VCO.STRB/ would clock flip-flop J13 to the clear state, its Q/ output supplying R.DATA high, representing the 1 bit. If no data transition is detected between two VCO.STRB/ pulses, the second H13 flip-flop remains set and its high Q output would be transferred to J13, outputting R.DATA low to represent a 0 bit. R.DATA is routed to the read sequencer where it is decoded; it is then checked for errors and output to the controller.

3.3.6 READ MICROSEQUENCER NETWORK

(Schematic sheets 7 and 8)

The digital read section, like the write section, is centered around an 8X02 microsequencer — C6. This device selects the next address of a control word to

be output by a control store consisting of three 512 bit ROMs — C2, C3 and C4. The control store outputs a 21 bit control word, which includes the decoded 4 bit nibble on bits REMIT.0-3. Bits REMIT.0-8 of the control word are supplied to the branch address inputs of the microsequencer. The next address control, determining the action to be taken by the sequencer, is performed by bits RAC0-2 of the control word. Address 00, for example, contains the Read Address Control code of 111 — reset to location 0. This is the sequencer idle loop, to which it returns following each read activity. Bits RTSEL0-2 select the test input to the sequencer from the 6 inputs presented to data selector D4. The state of the test input determines the outcome of conditional branching commands. Bits RTSEL0-2 also determine the output to be selected by addressable latch D3. Bit RTSEL3 selects the input polarity, determining whether a test outcome will be true when the input is high or when it is low; this bit also determines the polarity of the selected output.

The read sequencer has two functional routines: READ at address 03 and Read After Write at address 01. To access the read sequencer, the central processor loads the address of the desired routine onto CNTRL.BUS and pulses RD.SEQ.LD. This causes latch C1 to impose the contents of CONTRL.BUS onto the address inputs of the control store, resulting in a jump to the desired routine. RSEQ.GATE resolves the microprocessor/sequencer interface timing.

A sequencer controlled 8 bit general purpose counter (D1 and D2) is loaded from the 8 low microinstruction bits REMIT.0-7, upon the lowering of the eighteenth microinstruction bit, and incremented on the seventeenth bit. Its overflow forms the RDLTC input to the sequencer test input, enabling it to count task repetition. Upon completion of read activity an error status byte is left in this counter. The microprocessor accesses it by raising and lowering RD.STAT.EN. The following format is utilized:

7	6	5	4
FM	0	PARITY ERROR	POST ERROR

3	2	1	0
CRC	CODE	SYNC ERROR	PREAMBLE ERROR

In addition to RDLTC the inputs of the sequencer include R.DATA, which signifies the arrival, between the last two VCO.STRB pulses, of a DATA.STRB. CRC.ER is a hardware generated flag indicating a discrepancy between the prerecorded CRC code and the newly generated CRC check, based upon incoming data. R.ENV.ENBL is true if DATA.STRB arrived within the previous RSEQ.CLK period.

Read data is received by the edge detector consisting of two sections of K13 (see page 10 of schematic) that creates DATA.STRB. DATA.STRB goes through

envelope detector C9 (page 9) whose output, R.ENV.ENBL, is returned to the sequencer. When the sequencer determines that the envelope is valid the PLO.JAM signal is given to the phase-lock loop to synchronize the sequencer clock and the data stream. After 60 bit times the sequencer issues PLO.TRK.EN to put the phase-lock-loop in the data tracking mode. Data is then converted to 0s and 1s by data separator H13, J13 (page 11) and R.DATA is supplied to the test input of the sequencer. The R.DATA is tested first for the valid synch character, then for actual data. Data is tested for five bit times, then a corresponding 4 bit nibble is loaded into the 4 bit parallel to serial shift register B11 (page 8). The data is then shifted into the CRC checker B13 and another shift register, B12. Five more data bits are tested and converted to a four bit code, then loaded into 4 bit shift register B11. Data is again shifted into the CRC checker, and into shift register B12. The data in shift register B12 is shifted back into shift register B11, thus assembling the 8 bit byte to be sent to the host. The read sequencer issues a data strobe to the host at this time.

The decoding process continues until an end mark character is received, signifying the end of actual data. When the end mark is received the sequencer decodes the next four 5 bit groups as the CRC character, and shifts them into the CRC checker. The characters are assembled in a similar manner to the data, but no data strobe is issued to the host.

After the CRC has been loaded the sequencer tests the CRC checker output pin for an error. If any errors are detected the appropriate error code is reported via the 8 bit counter/timer status latch.

FWRT is used by the read sequencer as a reminder that it is performing a read after write operation, in which no data strobes are issued to the host. W.PAR is set by the write sequencer when erroneous parity is detected in the write data, informing the read sequencer that the parity error bit in the error status byte is to be set. R.FLAG is set by the read sequencer when it wants to remind itself that it has seen a file mark and that the routine exit is to flag the file mark bit in the status byte.

Other sequencer outputs provided by multiplex decoder D3 include ENV.EN, which is raised and lowered by the read sequencer in order to clear latch C9, enabling a subsequent test of R.ENV.ENBL. The R.DBSY and R.STRB signals are ORed with the corresponding lines from the write sequencer and central processor to provide H.DBSY and H.STRB, used for host/formatter handshake protocol. The remaining three lines, PLO.JAM, PLO.TRK.EN and RD.GATE control the operation of the read timing network. PLO.JAM clears the phase locked oscillator comparator counters, and initializes the PMP.TRK and PMP.AQ lines in preparation for preamble synchronization. This is done only after a valid preamble has been detected. PLO.TRK.EN is raised near the end of the preamble in order to enable the tracking mode. Lastly, RD.GATE controls whether

GAP.CLK or DATA.STRB is to provide reference to the read timing network.

3.3.7 WRITE MICROSEQUENCER NETWORK

(Schematic 5563, sheets 5 and 6)

The write encoder section is centered around a Signetics 8X02 microsequencer, ICE6. The device selects the next address of a control word to be output by a control store consisting of three 512 bit ROMs — E2, E3, and E4. The ROMs are connected in parallel, forming a 21 bit wide word (3 ROM output lines are not used). Three control word bits, Write Address Control lines AC0-2 (output by the control word at E3-7, 8, 9) determine the next action to be taken by the sequencer. The test input at pin E6-26 is used to poll the sequencer inputs, determining the outcome of conditional branching commands. The sequencer outputs the next control word address on lines WA0-8. Write Emit lines WEMIT0-8, output by E4 and E3-6, are supplied to the branch address inputs of the sequencer. The lower five lines, WEMIT0-4, are also used to transmit a 5 bit GCR nibble to parallel-to-serial shift register IC38 (schematic page 6). The input data and other status lines enter the sequencer at the T pin through 8-to-1 data selector ICH4, with bits WTSEL0-3 of the control word performing the input selection. Only six inputs are used. The output of the sequencer is handled by addressable latch ICH3, with lines WTSEL0-3 again performing the line and status selection. A more detailed description of write sequencer operation follows.

In accordance with host/formatter handshake protocol the write sequencer loads each data byte to be encoded from the DATA.BUS onto 8 bit parallel-to-serial shift register ICD8. The sequencer proceeds to shift each 4 bit nibble into CRC generator D9, and into the microsequencer test input as W4.DATA. Descending a conditional jump tree with each bit passed before it, the write sequencer arrives at a microinstruction which loads the appropriate 5 bit GCR code into the five rightmost bits of eight bit parallel-to-serial shift register E8 (schematic page 6), and proceeds to shift each bit, four WESQ.CLKS apart, into the write precompensation network described below.

The write sequencer, like the read sequencer, has an idle loop at location 0. The write sequencer has three microprocessor accessible routines: WRITE at address 00, WRITE FM at address BC and WRITE ONES at address DF. To access one of these, the microprocessor loads the desired address into CNTRL.BUS and toggles WRT.SEQ.LD. This causes bus latch E1 to impose the routine address upon the address inputs of the control store (E2, E3, and E4). Microprocessor/sequencer interface timing differences are resolved by associated logic (H7, K9, C7) and through the use of a dummy jump to next microinstruction initializing each routine. Write error status is reported by A7, causing the write sequencer to set W.PAR, a multiplex output

signifying bad parity in the write data. This is tested by the read sequencer and incorporated in the read sequencer status byte.

As mentioned above, the write sequencer has a 21 bit microinstruction. Five bits of the word, WTSEL.3-0 and WLATCH.EN are used to control an eight bit multiplexer, and an eight bit addressable latch providing six test inputs (H4) and six output lines (H3). WLATCH.EN controls whether the instruction in question is to test an input or set/reset an output. WTSEL.3 determines whether to skip on a high or a low test input, or if WLATCH.EN is high, whether to set or reset an output. Precisely which input/output is to be tested/set is determined by WTSEL.2-0.

Multiplex chip H4 provides the following sequencer test inputs: W.DLTC, a line indicating overflow of the write sequencer's general purpose counter E7; DRDY, used to implement write handshake protocol; FMTR.PAR, signifying the incoming byte's parity; W4.DATA, the incoming data bit to be encoded; W.FLAG, used by the write microsequencer as an indication that it is processing the second nibble of a byte, and that a new byte should be fetched upon completion.

Of the six output lines set up by H3, we have already encountered four: W.STRB and W.DBSY, used to implement the handshake data transfer protocol, W.FLAG, used to indicate the second nibble of a byte, and W.PAR, used to inform the read sequencer of a write parity error. W.DATA.STRB is the line which loads shift register D8 from the DATA.BUS with each byte to be encoded. W.RST raises the write signal during interblock gaps. Four other sequencer control lines are supplied by the write control store: W4.SHFT.EN and W5.SHFT.EN shift register D8 and E8, respectively. W5.LD is toggled upon determination of the appropriate GCR code, loading it into shift register E8. W.CRC.LD causes the CRC generator to pass the CRC code, as W.CRC for GCR encoding.

The write microsequencer utilizes 4 bit counter E7 to count ones in the preamble and postamble and to count the 16 bits of the CRC character. This counter is loaded by toggling W.CNT.LD, and is incremented whenever W5.LD shifts a nibble into the write precompensation network.

3.3.8 WRITE PRECOMPENSATION CIRCUITRY

(Schematic 5563, sheet 6)

When GCR patterns of 110 or 011 are written on tape, the middle one bit transition tends to drift towards the transitionless zero, away from the other one transition. The purpose of the precompensation network is to shift the middle one transition towards the other one's transition, compensating for the magnetic drift that occurs during the recording process. Patterns of 010 or 111 are left unchanged,

since the middle one bit is symmetrically affected by its accompanying bits. Patterns with 0 in the middle are also unaffected, since no transition is written on tape.

The write compensation network includes shift registers E8 and H8, 4 bit counter J9, flip-flops A11-6 and J8-7, and their associated gates. Upon determining a 5 bit GCR code for each nibble, the write microsequencer loads it onto the low five bits of the microsequencer emit field, WEMIT.0-4, and raised W5.LD and W5.SHFT.EN lines, loading the GCR data in parallel into the right five bits of shift register E8. During the next five Write Sequencer Clock pulses W5.LD is held low while W5.SHFT.EN is raised high, shifting the five bits serially into shift register H8. The three lower bits of H8 are examined by logic gates on E9 and H9. The present bit to be written is located at the Q1 output of the register while the preceding and following bits are at the Q2 and Q0 outputs, respectively. Counter J9 is preloaded each time the write sequencer raises W5.SHFT.EN, setting flip-flop A11-2 on the next WSEQ.CLK pulse; the Q/ of the flip-flop goes low to activate the load input of the counter. Counter J9 will be preloaded to a count of 7 if no precompensation is required, as for data patterns of 111, 010, or any pattern with a 0 in the middle. The counter will be loaded to a count of 8 if the data pattern is 110, delaying the middle 1 by 4 counts, thus pushing it towards the following 1 bit. The counter will be preloaded to a count of 11 if the data pattern is 011, clocking the middle bit sooner, thus pushing it towards the trailing 1 bit. Once counter J9 is preloaded, it will be clocked by W32.CLK until it reaches the count of 15, when its carry output goes high, is inverted by ICJ10-8 and clocks J-K flip-flop J8-13. The Q1 output of register H8 is connected to the J-K inputs of the flip-flop, performing the actual GCR data inscription. If the Q1 output is high the flip-flop will toggle, generating a transition as required for a 1 bit. If the Q1 output is a zero, the flip-flop will maintain the same state, generating no transition. The Q/ output of the flip-flop supplies WRITE DATA/ to the transport electronics board, where the write head drivers are loacted, and where an AC bias and a step are imposed on the data before it is written on tape.

SECTION IV

MAINTENANCE INSTRUCTIONS

4.1 GENERAL

Kennedy Company tape transports are highly reliable precision instruments which will provide years of trouble-free performance when properly maintained. A planned program of routine inspection and maintenance is essential for optimum performance and reliability. The units require very few adjustments and these should not be performed unless there is a strong reason to believe they are required. All electrical adjustments are preset at the factory and should not require readjustment except after long periods of use.

4.2 PREVENTIVE MAINTENANCE

To assure continuing trouble-free operation a preventive maintenance schedule should be kept. The items involved are few and simple but very important to proper tape transport operation. The frequency of performance will vary somewhat with the environment and degree of use of the transport, so a rigid schedule applying to all machines is difficult to define.

4.2.1 DAILY CHECK

Visually check the machine for cleanliness and obvious misadjustment. If items in the tape path show evidence of dirt or oxide accumulation, clean thoroughly.

4.2.2 CLEANING

All items in tape path must be kept scrupulously clean. This is particularly true of the head. When cleaning heads, it is important to be thorough yet gentle and to avoid certain dangerous practices.

4.2.2.1   Head Cleaning

Oxide or dirt accumulations on the head surfaces are removed using a mild organic solvent and a swab. Q tips are convenient but must be used with caution. Be sure the wooden portion does not contact head surfaces.

An ideal solvent is 1.1.1 trichloroethane contained in the Kennedy K21 maintenance kit. However, other solvents such as isopropyl alcohol will do.

DO NOT USE - acetone or lacquer thinner
- aerosol spray cans
- rubbing alcohol

Do not use an excess of any solvent, and be extremely careful not to allow solvent to penetrate the ball bearings of the capstan motor, since it will destroy their lubrication.

4.2.2.2   Other Cleaning

Use a vacuum cleaner to remove accumulations of dust. Compressed air may be used if caution is exercised to avoid blowing dirt into bearings.

4.3 ROUTINE ADJUSTMENT

There are no routine adjustments. Need for adjustment becomes manifest when malfunction occurs. Under normal circumstances adjustment will be more likely to cause trouble than to prevent it.

4.4 LUBRICATION

No bearing lubrication is required. All bearings are lubricated for life and introduction of oil may destroy their lubrication.

4.5 HEAD WEAR

Head wear is generally signaled by an increase in error rate. Confirmation is a sizable increase in output voltage from the read head as measured at the read preamplifier. When the head becomes worn it must be replaced. Head replacement is described in paragraph 4.10.4.

Worn heads usually can be resurfaced at least once if returned to the factory. This is more economical than replacement with a new head.

4.6 PERIODIC INSPECTION

Every two months, it is advisable to make a more thorough check of machine operating parameters to insure that no progressive degradation goes unnoticed. The recommended sequence for checks is shown in table 4-1.

4.7 DIAGNOSTICS AND ADJUSTMENTS

4.7.1 GENERAL

This section describes the on line and off line diagnostic routines used to isolate faults within the 6455 subsystem.

4.7.2 ON LINE DIAGNOSTICS

The formatter performs a self-test routine prior to each LOAD command. Successful completion of the self-test is required before the rest of the load sequence is allowed to continue. The self-test routine is a loop write to read of a file mark. This effectively stimulates about 80 percent of the formatter circuitry, including the data separation circuit. If the self-test fails, further off line testing is necessary.

```
┌─────────────────────────────────────────────────────────────────────────────┐
│                                         ┌──────────────────────────┐          │
│  ┌──────────────────────────┐           │      TAPE SPEED          │          │
│  │    UNKNOWN MACHINE       │           │     ADJUSTMENT           │          │
│  │  (Parts Assumed Good)    │           │  (Paragraph 4.7.3.2)     │          │
│  └──────────────────────────┘           └──────────────────────────┘          │
│              │                                       │                          │
│              ▼                                       ▼                          │
│  ┌──────────────────────────┐           ┌──────────────────────────┐          │
│  │      POWER ON            │           │     READ LEVEL           │          │
│  │  CHECK POWER SUPPLY      │           │    ADJUSTMENT            │          │
│  │      LEVELS              │           │  (Paragraph 4.7.4.3)     │          │
│  └──────────────────────────┘           └──────────────────────────┘          │
│              │                                       │                          │
│              ▼                                       ▼                          │
│  ┌──────────────────────────┐           ┌──────────────────────────┐          │
│  │   PHOTOSENSOR CHECK      │           │    RAMP TIME CHECK       │          │
│  │  (Paragraph 4.7.4.4)     │           │  (Paragraph 4.7.3.2)     │          │
│  └──────────────────────────┘           └──────────────────────────┘          │
└─────────────────────────────────────────────────────────────────────────────┘
```
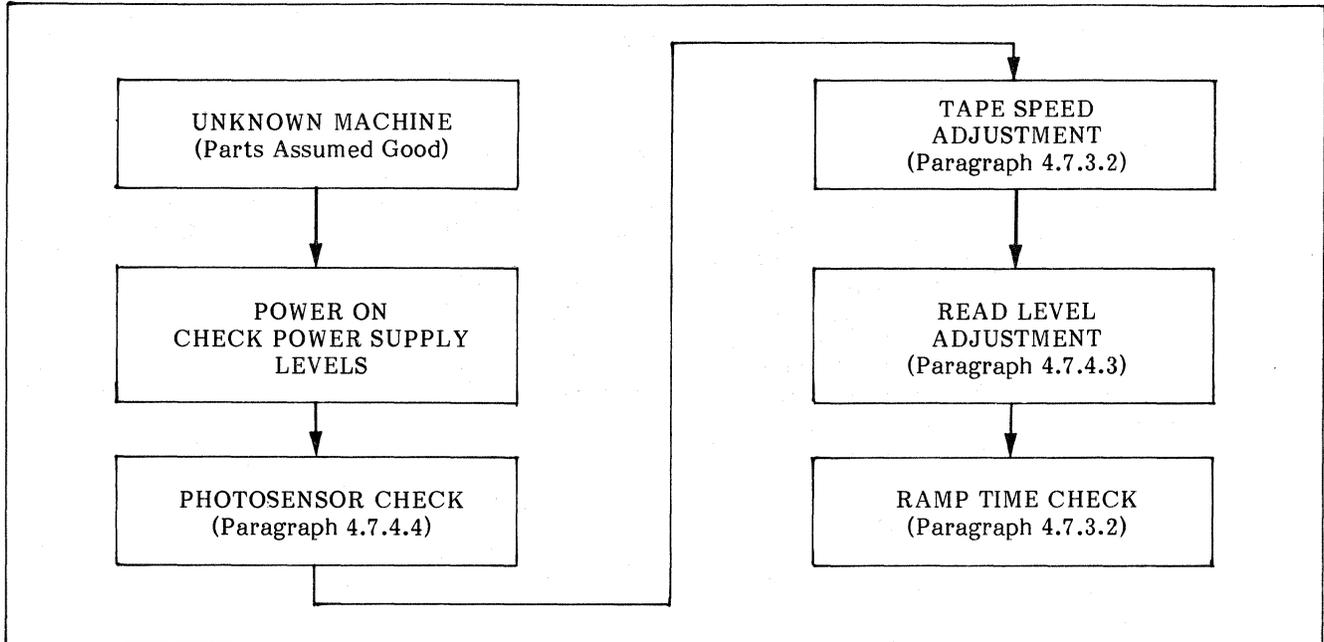
Table 4-1.
Adjustment Sequence

Tape Drive Tests

Test	Switch Setting SW 4321
Continuous Load	0000
Ramp Adjust	0001
Tape Speed Adjust	0010

System Tests

Test	Switch Setting SW 4321
Write File Mark, Continuous	0011
Read Continuous	0100
Write Continuous	0101

Formatter Tests

Test	Switch Setting SW 4321
Controller SA	0110
Read Sequencer SA	0111
Write Sequencer SA	1000
Continuous Self-Test	1001

Note: A 1 indicates that the switch should be in the ON position. Remove tape before running formatter diagnostics.

Table 4-2.
Off Line Diagnostics Switch Setting Chart

4.7.3 OFF LINE DIAGNOSTICS

4.7.3.1 General

To select the off line diagnostics, switch 7 of the eight position DIP switch located on the formatter must be set to the ON position. Ten test routines are then available, as listed in table 4-2. Prior to running these tests a kernel (sanity) test should be run on the 8035 microprocessor and the associated PROM. This test ascertains that the heart of the system is functional, and ready to execute the selected diagnostics.

1. Set switch 7 to ON position.

2. Disconnect interface cable from host to protect formatter interface drivers.

3. Check tape cartridge to guarantee that it is NOT in the SAFE position.

4. To run a different test, set switch 8 ON then OFF to reset formatter.

4.7.3.2 Tape Drive Diagnostics

Continuous Load (Switch Setting = 0000)

This routine performs up to 16 continuous LOAD sequences (without the self-test routine). It tests the basic functioning of the 6455 control electronics which allows for the measurement of the duration of the A and B hole signals.

Ramp Adjust (Switch Setting = 0001)

The tape is brought up to speed at a constant, linear acceleration. To control tape velocity, a ramp voltage is generated by the Control/Read/Write board. The voltage rises linearly to the running speed level and falls linearly to zero volt at stop. Ramp time is 25 +0/-3 msec at 30 ips, and varies inversely with speed. The ramp time (T) for different speeds (S) is given by the following formula:

$$T = 30 \times \frac{25}{S} \text{ msec}$$

The ramp adjustment procedure is greatly simplified using the ramp adjust test in conjunction with potentiometer R145, located on the Control/Read/Write board. To adjust the ramp set the diagnostic switch to 0001 and adjust potentiometer R145 until the transport shuttles the tape back and forth. When ramp setting is incorrect the transport will move the tape in the forward direction only.

Alternately the ramp time may be observed by placing an oscilloscope probe on the RAMP test point on the Control board and initiating rapid start/stop mode, long enough to allow the ramp voltage to reach a level. The ramp time is then adjusted using R145 to equal 25 msec, as shown below.
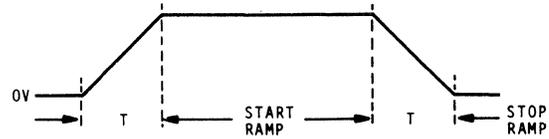
110-0103

Tape Speed Adjust (Switch Setting = 0010)

This routine initiates continuous writing of file marks to allow for the adjustment of the tape speed using the speed adjustment potentiometer R144 on the Control/Read/Write board. The tape will move in the forward direction until proper speed is achieved, at which point it will shuttle back and forth.

An alternate procedure for setting the speed is described below:

1. Connect channel 1 probe of a dual trace oscilloscope to the write data input. A convenient location would be J1-4 on the Control/Read/Write board, or IC12, pin 1 on the same board. Trigger scope on channel 1 and select 2 msec/cm time constant.

2. Connect channel 2 probe to test point TP1 on the same board and initiate the writing of short blocks on channel 1, one to ten characters long.

3. Adjust potentiometer R144 on the Control/Read/Write board so that the delay between the leading edges of the read and write data blocks is 10 msec at 30 ips. For machines operating at other tape speeds the formula for deriving the proper delay time is:

$$\frac{0.3}{S} = \text{delay in seconds}$$

where S = tape speed in inches per second.

Write File Mark Continuous (Switch Setting = 0011)

This routine will write file marks continuously on all tracks. If a bad file mark is written, a space reverse will be performed and a write FM extended.

Read Continuous (Switch Setting = 0100)

This routine will read blocks of data or file marks on all tracks continuously.

Write Continuous (Switch Setting = 0101)

This routine will write short blocks of data on all tracks continuously. If a bad block is written, a space reverse will be performed followed by a write extended routine. This will be repeated, if necessary, until a good block is written.

4.7.3.3 Formatter Diagnostics

The formatter diagnostics take advantage of the power of signature analysis (SA) to isolate faults to the component level. Certain jumpers are required to set up the SA tests. These are documented in the user's manual. An HP 5004A signature analyzer is required for these tests as well as for the kernal test for the 8035 processor. The formatter to the drive interface cable must be disconnected to perform SA tests and self-tests. The tape should be removed from the cartridge before operating the following diagnostics.

Control SA (Switch Setting = 0110)

This routine stimulates all the nodes in the controller section of the formatter so that any faults in this section can be isolated down to the component responsible.

Read Sequencer SA (Switch Setting = 0111)

This routine stimulates all the nodes in the read sequencer section of the formatter so that any faults in this section can be isolated down to the component responsible.

Write Sequencer SA (Switch Setting = 1000)

This routine stimulates all the nodes in the write sequencer section of the formatter so that any fault in this section can be isolated down to the component responsible.

Continuous Self-Test (Switch Setting = 1001)

This routine performs continuous self-test routines that allow the data separator section, including the phase lock loop, to be tested and adjusted. This is also a good verification of the functioning of the formatter as a whole.

Short and Long Loads (Switch Setting = 1xxxx)

In the ON position, this switch selects the short mode of tape loading, while in the OFF position the long, or normal mode, is selected. In the normal mode, the transport will move the tape forward in high speed to the end of tape, then rewind it to beginning of tape, optimizing tape tension for data transfer operations. In the short load mode, used in testing and diagnostics, the transport will rewind the tape directly to load point.

4.7.4 FORMATTER AND DECK ADJUSTMENT PROCEDURES

4.7.4.1 Formatter VCO Center Frequency Adjustment Procedure

Required equipment: frequency counter, adjustable DC power supply.

1. Move jumpers at SAJ6 to the test position (T) and remove jumper at JP1.

2. Measure regulated output of VCO voltage regulator RG2 (K16 pin 8) and adjust the DC power supply output to the measured value plus 4.20v. Thus, if RG2 output measures -5.1v, adjust power supply to -0.90v.

3. Connect power supply to top pin of JP1.

4. Connect frequency counter to the VCO OUT pin of SAJ6 and adjust trimmer capacitor C82 until VCO center frequency measures 3.84 MHz +/-10 KHz.

5. Replace jumper at JP1 and return SAJ6 to the normal N position.

4.7.4.2 Formatter Integrator Offset Adjustment

Required equipment: oscilloscope.

1. Set the oscilloscope to 1 usec/division, 2v/division, and add channels 1 and 2.

2. Connect oscilloscope probes to TP1 and TP2 on the Formatter board.

3. Adjust potentiometer R31 on the Formatter board until the added displayed voltage is at minimum amplitude.

4.7.4.3 Recorder Read Amplitude Adjustment Procedure

Required equipment: oscilloscope.

1. Set switches 1, 2 and 8 of the eight position diagnostic switch located on the Formatter board to the ON position then reset switch 8 OFF.

2. Set oscilloscope to 0.5v/division, invert channel 2, add channels 1 and 2.

3. Connect the oscilloscope probes to test points 1 and 2 on the Control/Read/Write PC board located on the bottom of the unit.

4. Adjust potentiometer R16 on the Control/Read/Write PC board until displayed voltage measures 3v peak to peak.

4.7.4.4 Infrared Sensor Check

The infrared sensors detect the A and B holes in the tape. The sensors are designed for maximum reliability and immunity to ambient light conditions. If the EOT or BOT are not properly detected, check the sensors as follows:

a. Disconnect the capstan motor by unplugging the molex connector.

b. Insert a tape cartridge.

c. Connect an oscilloscope probe or a voltmeter to test point A of the Control/Read/Write board.

d. Turn capstan by hand until the small A hole is opposite the A sensor. Voltage at test point A should measure approximately 4 volts.

e. Connect oscilloscope probe or voltmeter to test point B on the Control/Read/Write board.

f. Turn capstan by hand to double set of large holes. Voltage at test point B should measure approximately 4 volts.

g. Reconnect capstan motor.

4.7.4.5 Interlock Switch Check and Adjustment

If CARTRIDGE IN PLACE (CIP) signal does not go true when the cartridge is inserted:

1. Insert tape cartridge until it begins to engage with the latching mechanism. Contacts on both interlock switches should begin to open.

2. Press cartridge inward until it locks in place. Switch contacts should close completely. (This can be checked by gently pressing the switch contact toward the switch body. Any movement indicates contact is not completely closed.)

Adjustment

If contact will not close completely, loosen switch mounting screw and readjust switch position for complete contact closure.

4.8 TROUBLESHOOTING

4.8.1 GENERAL

Troubles that can arise in the Model 6455 can usually be classified as either mechanical or electrical. However, the classification may often become confusing because a basically mechanical problem can cause what appears to be an electronic malfunction and vice versa. In any case, the problem should be thoroughly analyzed before adjustments are made. Formatter troubleshooting is greatly facilitated by using signature analysis, as described below.

4.8.2 COMPATIBILITY

The Model 6455 accepts and produces tapes conforming to the standards. Occasionally, compatibility problems can arise. For example:

1. Cartridges written by and acceptable to the Model 6455 are not acceptable to another transport.

2. Foreign cartridges cannot be read by the Model 6455 but its own tapes can.

Tape speed and ramp times are important factors in tape compatibility. These should be checked as described under paragraph 4.7.3.2, Checks and Adjustments.

4.8.3 OTHER MALFUNCTIONS

Normal troubleshooting procedures should be used to locate and isolate electronic malfunctions. The first items to check are the power supply voltages on the Control/Power Supply board.

IMPORTANT

Power should be off before
removing or inserting circuit boards.

4.9 FORMATTER SIGNATURE ANALYSIS

4.9.1 GENERAL SIGNATURE ANALYSIS

Logic circuitry normally executes nonsequential program instructions. This places changing data patterns throughout the logic circuitry. The signature analysis test technique forces the microprocessor or the sequencer to continuously execute a limited test routine to place a repetitive data pattern throughout the logic circuitry.

A signature analyzer is used to probe data points within the logic circuit. The signature analyzer displays a four digit alphanumeric code (signature) which characterizes the activity measured during the test period. This manual lists the signatures taken from a properly operating 6455 formatter. If the listed signatures are the same as those obtained during the test, the related logic circuit is operating correctly. If a signature other than the one indicated is encountered the following troubleshooting steps should be taken:

1. Check test setup (SA connections, switch settings, jumper settings, etc.). Disconnect cable from formatter board to control board.

2. Check software revision level against this document. (Are the signatures given in this document valid for the prom revision used in formatter under test?)

3. Make sure the signatures being taken are valid for the test in progress. (Any signal line whose signature is not listed for a specific test has no valid signature during that test).

4.9.2 TEST SETUPS FOR SIGNATURE ANALYSIS

There are five separate test setups for troubleshooting the 6455 formatter using signature analysis. Each test setup is designed to isolate a functional block of the formatter by establishing an SA routine. THE TESTS MUST BE PERFORMED SEQUENTIALLY IN THE ORDER LISTED.

IMPORTANT: WHEN CHECKING THE SIGNATURE FOR A SIGNAL LINE, IT MUST BE CHECKED AT ALL NODES ASSOCIATED WITH THE SIGNAL LINE TO DETECT ANY OPEN TRACES.

4.9.3 SETUP FOR KERNEL ADDRESS (TEST 1)

This setup is used to collect signatures from each of the address lines of the 8035 microprocessor over its entire address range. This setup is also used to obtain signatures from the address decoding circuits that are enabled during an instruction fetch cycle.

The jumpers at SAJ1 are moved to the test position during this setup to apply an NOP instruction to the 8035. This causes the microprocessor to continuously increment its address. The signature analyzer is connected so that it turns on at address 0 and off at address 7FF hex.

This will verify that 8035 can properly address the program rom.

The nodes of interest for this test are located on page 3 of schematic diagram supplied in the 6455 operation and maintenance manual.

4.9.4 SETUP FOR KERNEL DATA (TEST 2)

This setup is used to collect signatures from each of the data lines of the program rom to verify that its contents are correct.

The jumpers at SAJ1 are moved to the test position during this setup to apply an NOP instruction to the 8035. This causes the microprocessor to continuously increment its address. The signature analyzer is connected so that it turns on at address 0 and off at address 7FF hex. The SA clock is moved to a different phase so that data can be verified. If incorrect signature(s) are detected on data lines, IC-A3 should be replaced and the test repeated.

For nodes of interest refer to page 3 of schematic diagram (IC-A3 particularly).

4.9.5 SETUP FOR CONTROLLER (TEST 3)

This setup is used to collect signatures from each of the microprocessors I/O ports and the associated device select decoders and drivers. (ICs B7, B8, J1, J2, A8, and A10.)

The jumpers at SAJ3 and SAJ5 are moved to the test position during this setup to enable the sequencer jam load latches (chip locations C1 and E1) to allow signature analysis of their outputs.

The diagnostic selector switch is set to 46 hex before power is applied. This will cause the execution of a special subprogram that will exercise all of the nodes controlled by the microprocessor.

For nodes of interest refer to pages 2, 3, 4, of the formatter schematic diagram.

4.9.6 SETUP FOR READ (TEST 4)

This setup is used to collect signatures from the read sequencer and all of its associated circuitry up to but not including the phase lock loop phase detector.

The jumpers at SAJ2 is moved to the test position during this setup to force an NOP instruction into the read sequencer.

The diagnostic selector switch is set to 47 hex before power is applied. This will cause the execution of a special subprogram that will initialize the read sequencer for signature analysis. For nodes of interest refer to pages 2, 7, 8, 9 of schematic diagram.

4.9.7 SETUP FOR WRITE (TEST 5)

This setup is used to collect signatures from the write sequencer, all of its associated circuitry, part of the read circuitry associated with the phase lock loop phase detector and loop charge pump selectors.

The jumpers at SAJ4 and SAJ6 are moved to the test position during this setup to force an NOP instruction into the write sequencer instruction bus and to apply a synchronous crystal clock continuously to the phase lock loop section.

Because of several power up states for the loop charge pump selector circuitry more than one signature is possible at some of the nodes involved. The correct listing of the multiple sets of possible signatures is shown in table m of this test.

The diagnostic selector switch is set to 48 hex before power is applied. This will cause the execution of a special subprogram that will initialize the write sequencer for signature analysis.

Note: This diagnostic must be run from a power up condition. To run this diagnostic jumper SAJ6 must be in the normal position from power up then changed to the test position after applying power. DO NOT RESET THE FORMATTER IN THE MIDDLE OF THE TEST AS THE SIGNATURES MAY BECOME INVALID IN THAT INSTANCE.

For nodes of interest refer to pages 2, 4, 5, 6, 8, 10 of schematic diagram.

4.9.8 REQUIRED TEST EQUIPMENT

1. Oscilloscope

2. HP 5004A signature analyzer and related manual.

3. VTVM (multimeter)

4.9.9 SA LISTING

The format of each part of the SA test listing is:

IC-pin signature (x), (y); cccccccc OR
mmmmmm signature (x), (y); cccccccc

where: IC-pin is the location where the signatures were taken;

mmmmmm is the mnemonic of the signal line for which the signature was taken. Cross reference listing will give the physical location of the signal line in question.

ccccc is extra instruction or comment and is always preceded by a semicolon (;).

(x) is the next section or subsection to check if the signature for that signal line was bad. If omitted and no other instruction is given proceed with the next line in that column.

(y) is the next section or subsection to check if the signature for that signal line was good. If omitted and no other instruction is given, proceed with the next line in that column.

If in both cases above there are no more lines in that column and there are no instructions, the data provided is sufficient to pinpoint a bad IC.

Capital letters instead of lower case letters when used within the brackets indicate the IC to be replaced if that condition is true. However when a specific IC is not called out, the technician must analyze the data obtained and, with the help of the schematic diagram, determine the failure with classical techniques.

After troubleshooting a section or subsection of an SA test, the test for the faulty section should be repeated to assure that it is in proper working order.

CLOCKS MUST BE CHECKED WITH AN OSCILLOSCOPE OR FREQUENCY COUNTER TO VERIFY THAT THEY ARE OPERATING AT THE CORRECT FREQUENCY.

Example on Use of the Tables

1) C14-9   A451 (d2), (J10)

Is read: "At IC-C14 pin 9 the signature should be A451; if bad go to section (d2), else replace IC-J10."

2) W.CNTR.LD/   U846 (e1), (f)

Is read: "At signal line W.CNTR.LD/ which the cross reference listing indicates as being connected to IC-E3 pin 6 and IC-E7 pin 9, should be U846. If bad go to (e1), else go to (f)."

3) K9-13   0000 ,   (K9)

Is read: "At IC-K9 pin 13 the signature should be 0000. If bad proceed with the next line, else replace IC-K9."

4) E8-17   96H4 (E8),

Is read: "At IC-E8 pin 17 the signature should be 96H4. If bad replace IC-E8, else proceed with the next line."

Troubleshooting Example

Assume the Kernel address signature analysis (Test 1) is being performed and the signature for signal line A0 is wrong (any value other than 7A33). All other signatures in (a) (Table A) are correct. In this condition, if the jumpers and the switches are set correctly the processor should be in an NOP state, that is the program counter will increment through all address states sequentially.

The first step is to go to (a1) and check signal line A5-3. If that signature is good, the other signatures in (a1) will most probably be correct so leading to section (c1). Since all other address lines were correct, ALE will also be correct (section (c1) and that will lead to the replacement of IC-A5.

Assume now that all address lines were bad. Again the next step will be to check section (a1). If bad go to (b1), else go to (c1). Section (b1) will check whether the processor is being reset in the middle of the test and it will suggest the possible source of the problem. Section (c1) will check the clock to IC-A5 and will suggest the possible source of the problem. Finally either (b1) or (c1) could lead to section (c), in which case IC-A6 should be replaced as indicated and the test repeated.

Test 1 - Kernel Address SA List

START	= ─__	SATP 9
STOP	= ─__	SATP 8
CLOCK	= ─__	SATP 3
GND	=	SATP 1

VCC SIGNATURE = 8P54

SA TEST JUMPERS USED

SAJ1

Notes:

1. The symbol (*) indicates that the signal in question is not a level. (The light on the SA probe is not steadily on or off.)

2. The symbol (**) indicates that the signal in question is at a floating level. (The light on the SA probe is on but dim, as if the probe were not inserted in the circuit.)

3. The symbol (****) indicates an unstable signature.

Diagnostic Switch Setting

	1	2	3	4	5	6	7	8
ON								
OFF	X	X	X	X	X	X	X	X

(a)

A0	7A33	(a1)
A2	0863	(a1)
A1	29PP	(a1)
A3	HH53	(a1)
A4	H1OF	(a1)
A5	3A9A	(a1)
A6	0108	(a1)
A7	F61C	(a1)
A8	528H	(a1)
A9	8C2H	(a1)
A10	0001	(a1)
OE/	8P54 *	(a1)
A3-21	0000 *	(a1),

END OF TEST

(a1)

A5-3	U467	(b1)
A5-4	53HH	(b1)
A5-7	10F6	(b1)
A5-8	CAA6	(b1)
A5-13	A218	(b1)
A5-14	7535	(b1)
A5-17	0211	(b1)
A5-18	8F37	(b1), (c1)

(b)

Check ICs A15 and A10 (page 8 and page 2 respectively) and related circuitry. (Go to controller test.)

(b1)

RESET/   8P54   (b), (c)

(c)

ICA6 might be bad. Replace it with a known good one and if problem persists check ICs B2 and B3 for proper operation.

(c1)

ALE   8P54 *   (c), (A5)

Test 2 Kernel Data SA List

START	=	SATP 9
STOP	=	SATP 8
CLOCK	=	SATP 14
GND	=	SATP 1

VCC SIGNATURE = 8P54

SA TEST JUMPERS USED

SAJ1

Notes:

1. The symbol (*) indicates that the signal in question is not a level. (The light on the SA probe is not steadily on or off.)

2. The symbol (**) indicates that the signal in question is at a floating level. (The light on the SA probe is on but dim, as if the probe were not inserted in the circuit.)

3. The symbol (****) indicates an unstable signature.

4. Signatures under listing "a" vary according to PROM version.

Diagnostic Switch Setting

	1	2	3	4	5	6	7	8
ON								
OFF	X	X	X	X	X	X	X	X

(a)

PROM C10

D0	0H09	(a1)
D1	68PP	(a1)
D2	6630	(a1)
D3	5746	(a1)
D4	5625	(a1)
D5	6583	(a1)
D6	9027	(a1)
D7	H709	(a1),

END OF TEST

(a1)

A0	7A33	(b)
A1	29PP	(b)
A2	0863	(b)
A3	HH53	(b)
A4	H10F	(b)
A5	3A9A	(b)
A6	0108	(b)
A7	F61C	(b)
A8	2946	(b)
A9	4596	(b)
A10	0000 *	(b)
A3-21	0000 *	(b), (A3)

(b)

Is the test setup correct? If yes, recheck KA SA test.

Test 3 Controller SA List

START	=	‾__	SATP 4
STOP	=	‾__	SATP 5
CLOCK	=	__/‾	SATP 12
GND	=		SATP 1

VCC SIGNATURE = U7HF

SA TEST JUMPERS USED

SAJ3 SAJ5

Notes:

1. Power up before moving SAJ3 to test. D1-19 and D2-19 should be U7HF.

2. The symbol ???? indicates an unpredictable signature.

3. The symbol (*) indicates that the signal in question is not a level. (The light on the SA probe is not steadily on or off.)

4. The symbol (**) indicates that the signal in question is at a floating level. (The light on the SA probe is on but dim, as if the probe were not inserted in the circuit.)

5. The symbol (****) indicates an unstable signature.

Diagnostic Switch Setting

	1	2	3	4	5	6	7	8
ON		X	X				X	
OFF	X			X	X	X		X

(a)

DATA/	PA69 *	(a1), (b)

(a1)

K10-2	1HC5	(a2)
C14-9	PA69	(d2), (J10)

(a2)

WRT.DATA/	0000	
J2-8	0000	(a4), (a3)

(a3)

K10-3	U7HF	(K10)
J2-9	U7HF	(J2)

(a4)

J8-14	U7HF	(e)
J8-11	0000	(a6)
J8-13	0000	(a5)

(a5)

J9-15	U7HF	
A11-6	U7HF	(e)

(a6)

H8-15	0000	
H8-14	0000	
H8-13	U7HF	
H8-9	0000	(e)
H8-2	U7HF	(a7)

(a7)

E8-1	0000	(e)
E8-19	0000	(e)

(b)

H.STRB/	A403	(b1)
H.CBSY/	A403	(b1)
H.DBSY/	U7HF	(b1)
H.FPAR/	60HH	(b1)
H.BUS0/	AP21	(b5)
H.BUS1/	HH1A	(b5)
H.BUS2/	4235	(b5)
H.BUS3/	3C33	(b5)
H.BUS4/	H8PF	(b5)
H.BUS5/	UHF1	(b5)
H.BUS6/	F324	(b5)
H.BUS7/	8FP9	(b5), (c)

(b1)

A10-13	A403	(b2)
A10-14	A403	(b2)
A10-11	60HH	(b2)
A10-12	U7HF	(b2)

(b2)

CMD.BSY	53HU	(b3)
CMD.STRB	53HU	(b3), (b4)
FMRT.PAR/	9701	(b3)
CMD.REQ/	U7HF	(b3)
FMRT.CLR/	U7HF	(b3)
DRDY/	U7HF	(b3), (b4)

(b3)

A10-5	U7HF
H.FMTR.CLR/	U7HF
H.CMD.REQ/	U7HF
H.DRDY/	U7HF
H.HPAR/	U7HF

(b4)

R.DBSY	0000	(e1)
R.STRB	0000	(e1)
W.STRB	0000	(e)
W.DBSY	0000	(e)

(b5)

DATA.BUS.0/	????	(b7)
DATA.BUS.1/	????	(b7)
DATA.BUS.2/	????	(b7)
DATA.BUS.3/	????	(b7)
DATA.BUS.4/	????	(b7)
DATA.BUS.5/	????	(b7)
DATA.BUS.6/	F324	(b7)
DATA.BUS.7/	8FP9	(b7)
DATA.BUS.IN	9684	(b6), (A8)

(b6)

A6-24	A558	(e2)
ALE	F4AU	(e2), (A2)

(b7)

R.DBSY	0000	(e1), (d)

If signatures at (d) are good J9 is possibly bad.

(c)

16X.BIAS/	U7HF	(c2)
FAST/	C62U	(c2)
FWD/	0000	(c2)
GO/	0000	(c2)
SWS/	U7HF	(c2)
THRES.B/	U7HF	(c2)
TSA/	C62U	(c2)
TSB/	41U3	(c2)
THRES.A/	0000	(c2), (d)

(c1)

J1-19	0000	
J10-13	U7HF	
A13-6	U7HF	
A14-2	0000	
A12-6	0000	
A13-8	U7HF	(e1)

(c2)

H1-2	0000	(d)
H1-5	C62U	(d)
H1-6	0000	(d)
H1-9	U7HF	(d)
H1-12	0000	(d)
H1-15	C62U	(d)
H1-16	41U3	(d)
H1-19	U7HF	(d), (c1)

(d)

CNTRL.BUS.0	5451	(d1)
CNTRL.BUS.1	????	(d1)
CNTRL.BUS.2	????	(d1)
CNTRL.BUS.3	????	(d1)
CNTRL.BUS.4	P779	(d1)
CNTRL.BUS.5	932U	(d1)
CNTRL.BUS.6	F2F1	(d1)
CNTRL.BUS.7	A0C9	(d1), END OF TEST

(d1)

RD	1960	(d2)
A12-10	4138	(d2), (d7)
J10-2	AFH0	(d2)
CHECK		(e1), (d4)

(d2)

DRV.OUT.EN/	9C55	(d3)
RD.IO.EN/	C6P4	(d3)
RD.SEQ.LD/	H686	(d3)
RD.STAT.EN/	4884	(d3)
RESET.DIAG/	FFPU	(d3)
SET.DIAG/	9F1F	(d3)
WRT.SEQ.LD/	8A38	(d3)
START.C.SA/	909C	(d3)
STOP.C.SA/	U7HF *	(d3)
DRV.INP.EN/	5C0F	(d3)

(d3)

A2-2	2P42	(e2)
A2-7	1F59	(e2)
A2-10	4A0P	(e2)
A2-15	9684	(e2)
WR	C86P	(e2)

(d4)

D2-19	U7HF	(D2)
D1-19	U7HF	(D1), (d5)

(d5)

H2-3	U7HF	(d6)
H2-4	U7HF	(d6)
H2-7	U7HF	(d6)
H2-7	U7HF	(d6)
H2-8	U7HF	(d6)
H2-13	U7HF	(d6)
H2-14	U7HF	(d6)
H2-18	****	(d6)

(d6)

J2-2	U7HF
J2-3	U7HF
J2-4	U7HF
J2-5	U7HF
J2-6	U7HF
J2-7	U7HF
J2-9	U7HF

(d7)

Check switch settings. If Correct continue with (d1).
(d1).

(e)

H3-4	0000	
H3-5	0000	
H3-6	0000	
H3-7	0000	
H3-9	0000	
H3-10	0000	
H3-11	0000	
H3-12	0000	
E4-6	0000	
E4-7	0000	
E4-8	0000	
E4-9	0000	
E4-11	0000	
E4-12	0000	
E4-13	0000	
E4-14	0000	
H3-15	U7HF	
H3-14	U7HF	
E2-6	0000	
E2-1	U7HF	
E2-2	0000	
E2-3	PU69	
E2-4	18C5	
E2-5	PU69	
E2-16	0000	
E2-17	U7HF	
E2-18	18C5	
E2-19	0000	
E6-2	U7HF	(f)

(e1)

D3-14	U7HF	
C4-6	4PU3	
C4-7	C92U	
C4-8	0000	
C4-9	C92U	
C4-11	4PU3	
C4-12	4PU3	
C4-13	0000	
C4-14	0000	
C2-6	U7HF *	
C2-7	U7HF *	
C2-8	0000	
C2-9	C92U	
C3-6	4PU3	
C6-3	4PU3	
C6-4	C92U	
C6-5	4PU3	
C6-6	C92U	
C6-8	4PU3	
C6-9	0000	
C6-10	U7HF	
C6-11	C92U	
C6-12	0000	
C6-2	U7HF	(g)

(b1)

C6-2	0000	(b2)
SYS.RST/	2395	
A14-6	0000	
A13-6	2395	
RD.SEQ.LD/	2395	(z)
RSEQ.GATE	2395	(C7)
A14-11	0000	(A14), (A13)

(b2)

Check that SAJ2 has been positioned correctly. Then check visually and/or with an ohm-meter for shorts along the trace(s) of the faulty signal lines. If no shorts, replace IC-C6.

(c)

REMIT.0	0PUH	(c1)
REMIT.1	HPC1	(c1)
REMIT.2	969F	(c1)
REMIT.3	P527	(c1)
REMIT.4	P1PC	(c1)
REMIT.5	2158	(c1)
REMIT.6	U8A6	(c1)
REMIT.7	0681	(c1), (d)

(c1)

Check visually and/or with an ohm-meter for shorts along the trace(s) of the faulty signal lines. If no shorts replace IC-C4.

(d)

REMIT.8	165P	(d1)
RAC.0	4529	(d1)
RAC.1	PC07	(d1)
RAC.2	9H17	(d1)
RTSEL.0	7824	(d1)
RTSEL.1	2F22	(d1)
RTSEL.2	CFH5	(d1)
RTSEL.3	A1PF	(d1), (e)

(d1)

Check visually and/or with an ohm-meter for shorts along the trace(s) of the faulty signal lines. If no shorts replace IC-C3.

(e)

RLATCH.EN	3C1P	(e1)
R4.LD	FH0A	(e1)
RCRC.LD	7F6U	(e1)
C2-6	3H17	(e1)
C2-7	07C8	(e1), (f)

(e1)

Check visually and/or with an ohmmeter for shorts along the trace(s) of the faulty signal lines. If no shorts replace IC-C2.

(f)

DATA.BUS.0/	0H40	(f1)
DATA.BUS.1/	0H40	(f1)
DATA.BUS.2/	0H40	(f1)
DATA.BUS.3/	0H40	(f1)
DATA.BUS.4/	2395	(f1)
DATA.BUS.5/	2395	(f1)
DATA.BUS.6/	0H40	(f1)
DATA.BUS.7/	2395	(f1), (g)

(f1)

R.DBSY	6740	(i)

Go to (g). If (g) is good, replace IC-A9.

(g)

RD0/	0HP3	(g1)
RD1/	2473	(g1)
RD2/	C85H	(g1)
RD3/	54F8	(g1)
RD4/	5H10	(g1)
RD5/	F2F/	(g1)
RD6/	74FC	(g1)
RD7/	2FA3	(g1), (h)

(g1)

B10-6	C165	(B10), (g2)

(g2)

The problem lies either in B11 or in B12.

(h)

FMTR.PAR/	6740	(h1)
RT.INP	16CU	(h2)
JAM.LD/	2395	(h3)
DATA.STRB	0000	(h5)
SEQ.IDLE/	3A19	(h6)
R.ENV/	2395	(h7)
CRC.ER	CUC5	(h4), END

If any signature in (h) above is wrong go to (i). If (i) is good come back to (h) and follow the instructions within the brackets.

(h1)

A7-6   44H5 (A7), (B10)

(h2)

D4-5   C753   (D7)
R.DATA   0000 (h8)
RDLTC/   2A5A (h9)
R.ENV.ENBL   0000 (C9), (D4)

(h3)

E13-2   725U (D13)
E13-5   0000 (E13), (E14)

(h4)

B13-4   198F (A14)
A15-8   5UUA (A15), (B13)

(h5)

DATA   0000 (z)
K12-5   0000 (K13), (K12)

(h6)

A13-8   108H (A13)
A12-6   3318 (A12), (A14)

(h7)

J14-4   2395 (J14)
F13-1   0000 (F13), (J13)

(h8)

H13-9   2395 (H13), (J13)

(h9)

D2-19   2A5A (D2), (D1)

(i)

ENV.EN   C94F (i1)
FWRT   0P0F (i1)
R.FLAG   7AAF (i1)
PLO.JAM   51FA (i1)
PLO.TRK.EN   36H5 (i1)
RD.GATE   1513 (i1)
R.DBSY   44H5 (i1)
R.DBSY/   6740 (B9)
R.STRB   38FP (i1), (h)

(i1)

D10-8   188C (D10), (D3)

(z)

Recheck controller test.

Test 5 Write SA List

START	=	⎺__ SATP 16
STOP	=	⎺__ SATP 11
CLOCK	=	__/⎺ SATP 15
GND	=	SATP 1

VCC SIGNATURE = 1165

SA TEST JUMPERS USED

SAJ4   SAJ6

Notes:

1. Power up before moving SAJ6.

2. The symbol (*) indicates that the signal in question is not a level. (The light on the SA probe is not steadily on or off.)

3. The symbol (**) indicates that the signal in question is at a floating level. (The light on the SA probe is on but dim, as if the probe were not inserted in the circuit.)

4. The symbol (****) indicates an unstable signature.

Diagnostic Switch Setting

	1	2	3	4	5	6	7	8
ON				X			X	
OFF	X	X	X		X	X		X

(a)

W64.CLK	1165*	15.36	MHz
W32.CLK	1165*	7.68	MHz
W16.CLK	1165*	3.84	MHz
VCO.CLK/	0000*	3.84	MHz
W8.CLK	1165*	1.92	MHz
WSEQ.CLK	0000*	0.96	MHz
H10-15	0000*	0.96	MHz 10% Duty Cycle
GAP.CLK	PC84	240.00	KHz

All clocks above are 50% duty cycle unless otherwise indicated. The signature will indicate the phase of each clock, but the frequency should be checked either with an oscilloscope or a frequency counter.

Only if the above clocks are correct it is allowed to proceed with the remainder of the test. If all clocks are good, start at (b).

(b)

WA0	OU23	(b1)
WA1	PC84	(b1)
WA2	627P	(b1)
WA3	CHU8	(b1)
WA4	8C36	(b1)
WA5	FA11	(b1)
WA6	41F7	(b1)
WA7	HFP7	(b1)
WA8	CC34	(b1), (c)

(b1)

E6-2	0000	(b2)
C7-4	1165	(C7)
K9-13	0000	(K9)
H7-2	1165 (y),	(H7)

(b2)

Check that SAJ4 and SAJ6 have been positioned correctly. Then check visually and/or with an ohmmeter for shorts along the trace(s) of the faulty signal lines. If no shorts, replace IC-E6.

(c)

WEMIT.0	0A84	(c1)
WEMIT.1	7A4F	(c1)
WEMIT.2	FC7P	(c1)
WEMIT.3	2472	(c1)
WEMIT.4	PP42	(c1)
WEMIT.5	U20F	(c1)
WEMIT.6	9CU4	(c1)
WEMIT.7	A525	(c1), (d)

(c1)

Check that address lines are physically connected to IC-E4, then check visually and/or with an ohmmeter for shorts along the trace(s) of the faulty signal lines. If no shorts, replace IC-E4.

(d)

W.CRC.LD	5U02	(d1)
W5.LD	009U	(d1)
W5.SHIFT.EN	44CP	(d1)
W4.SHIFT.EN	UFH6	(d1)
WLATCH.EN	3C16	(d1), (e)

(d1)

Check that address lines are physically connected to IC-E2, then check visually and/or with an ohmmeter for shorts along the trace(s) of the faulty signal lines. If no shorts, replace IC-E2.

(e)

WTSEL.0	631F	(e1)
WTSEL.1	1FU5	(e1)
WTSEL.2	4CU9	(e1)
WTSEL.3	UC8F	(e1)
WAC.0	5C0P	(e1)
WAC.1	P98P	(e1)
WAC.2	1CH5	(e1)
W.CNTR.LD/	U846	(e1), (f)

(e1)

Check that address lines are physically connected to IC-E3, then check visually and/or with an ohmmeter for shorts along the trace(s) of the faulty signal lines. If no shorts, replace IC-E3.

(f)

Check the lines in (g) below and if any of them have a bad signature check section (h) first. If the lines in (h) were good then go back to (g) and follow the directions given within the brackets.

(g)

W.CRC	949P	(g1)
WRITE DATA/	C86P	(g2)
PMP.TRK	0000	(g4)
PMP.TRK/	1165	(g4)
PMP.AQ/	1165*	(g4)
R.ENV/	67A7	(g6)
H15-5	PC84	(g8)
WT.INP	7U3C	(g3)

Check (m). If good, end of test.

(g1)

D9-1	PHC3	(D10), (D9)

(g2)

E8-17	96H4	(E8)
DN-1	8393	(H8)
DN+1	5UH1	(H8)
DN	P877	(H8)
H9-10	92U6	(H9)
H9-12	4PC4	(H9)
E9-6	A0UU	(E9)
E9-8	F9A2	(E9)
E9-12	695H	(E9)
H9-6	7838	(H9)
H9-4	C19A	(H9)
J9-9	C33A	(A11)
J9-15	A246	(J9)
J9-7	C323	(J10), (J8)

(g3)

H4-5	84C7		(D7)
DRDY/	1165		(y)
W.DLTC	1207		(E7)
FMRT.PAR/	1165	(y),	(H4)

(g4)

K12-3	0000*		(g5)
VCO.STRB/	1165*	(g7),	(K12)

(g5)

C14-5	0000		
C14-6	1165		(m)
DATA.STRB	883U		(C14)
DATA/	A90C	(y)	
K12-5	2134	(K13),	(K12)

(g6)

J13-3	883U	(g5)	
F13-12	P18H		(J13)
J14-4	995A	(J14),	(F13)

(g7)

JAM.LD/	1165		
E13-5	0000		(E14)
E13-2	1165		(g8)

;if (g8) is good, replace E13

PLO.JAM	0000	(z),	(D13)

(g8)

The signatures below could be used as a troubleshooting aid but not as a definite mean to isolate a bad IC.

RD.DATA.STRB/	UAP1	(g5)

; If (g5) is good replace K14

F14-12	0000*
D15-3	PC84
F15-5	A683
E14-8	1165*

(h)

W.DATA.STRB	1319	(h1)
W.RST	3H15	(h1)
W.RST/	2F70	(E10)
W.FLAG	3CC0	(h1)
W.PAR	U416	(h1)
W.DBSY	3U80	(h1)
W.STRB	47PH	(h1)
W4.DATA	0108	(h2), (g)

(h1)

K9-3	2A73	(K9), (H3)

(h2)

D8-1	PUFU	(D7), (h3)

(h3)

DATA.BUS.0/	1165	(y)
DATA.BUS.1/	0000	(y)
DATA.BUS.2/	1165	(y)
DATA.BUS.3/	0000	(y)
DATA.BUS.4/	0000	(y)
DATA.BUS.5/	1165	(y)
DATA.BUS.6/	0000	(y)
DATA.BUS.7/	1165	(y), (D8)

(m)

The following signatures are organized in a table. For a given signature at D15-6 the signatures for all other IC-pins are listed in the same column. If the signatures are good the circuit is operational. If they are bad they could be used as a troubleshooting aid but not as a definite mean to isolate a bad IC.

D15-6	1165*	5341	0000*	C7P6	UAP1
D14-11	0000*	0000*	0000*	0000*	0000*
D14-3	1165*	1165*	1165*	1165*	1165*
E14-6	1165*	5341	0000*	C7P6	UAP1
E14-3	1165*	1165*	1165*	1165*	1165*
E15-9	0000*	0000*	0000*	0000*	0000*
E15-7	1165*	1165*	1165*	1165*	1165*
E15-5	1165*	5341	0000*	C7P6	UAP1
E15-6	0000*	4224	1165*	A683	PC84
H15-7	PC84	C8F5	PC84*	4H07	1165*
F15-7	1165*	1165*	1165*	1165*	1165*

(y)

Recheck controller test.

(z)

Recheck read test.

4.10 PARTS REPLACEMENT

4.10.1 GENERAL

Removal and replacement of most items in the Model 6455 are obvious. Certain items such as the photosensor assembly require adjustment after installation. Adjustments and any precautions which should be exercised are described in the following removal and installation procedures.

4.10.2 EOT/BOT INFRARED SENSOR REPLACEMENT

1. Disconnect sensor molex connector.

2. Loosen the two sensor retaining screws and remove sensor.

3. Replace with new sensor assembly, connecting the sensor molex connector yet leaving the retaining screws loose enough for the sensor to be moved.

4. Insert a cartridge, disconnect capstan motor, and turn power ON.

5. Advancing tape by hand, place tape so that A hole is centered in front of sensor. Using an oscilloscope or a voltmeter attached to test point A on the Control/Read/Write board, align sensor so that maximum voltage is displayed.

6. Repeat for hole B, using test point B on the Control/Read/Write board.

7. Tighten sensor retaining screws and reconnect capstan motor.

4.10.3 CAPSTAN MOTOR REPLACEMENT

1. Disconnect motor molex connector from Control/Read/Write board, located at the bottom of the unit.

2. Using a long Allen wrench, loosen the motor retaining screw by gaining access to it from one of the side holes provided for this purpose in the frame.

3. Slide old motor out and replace with new motor.

4. Insert cartridge and align motor capstan with center of cartridge capstan.

5. Tighten motor retaining screw and reconnect molex connector.

4.10.4 MAGNETIC HEAD REPLACEMENT

1. Disconnect all 4 head connectors.

2. Remove Control/Read/Write PC board, located at the bottom of the unit.

3. From underneath the head plate loosen the head retaining screws and remove head.

4. Place new head in position, keeping the screws loose enough to allow the head to be relocated.

5. Align head so that both of its edges are equidistant from the edges of the head plate.

6. Insert tape cartridge. Tape should make even contact with read and write head surfaces, and should have equal clearance from the erase head surfaces on both sides.
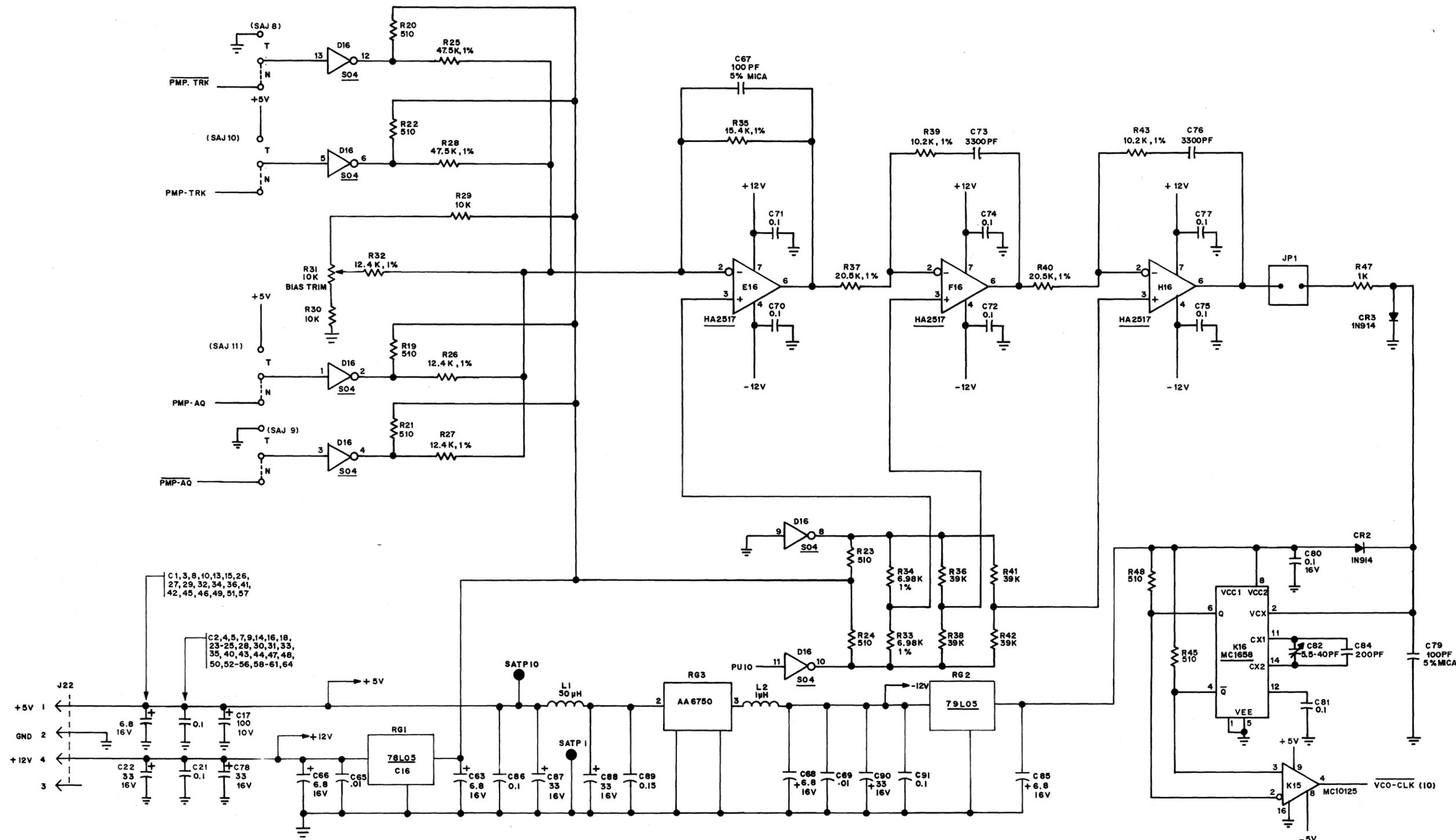
4.11 MAINTENANCE TOOLS

In addition to normal electronic tools and test gear (oscilloscope, voltohmmeter, etc.) the following items should be available for service and repair:
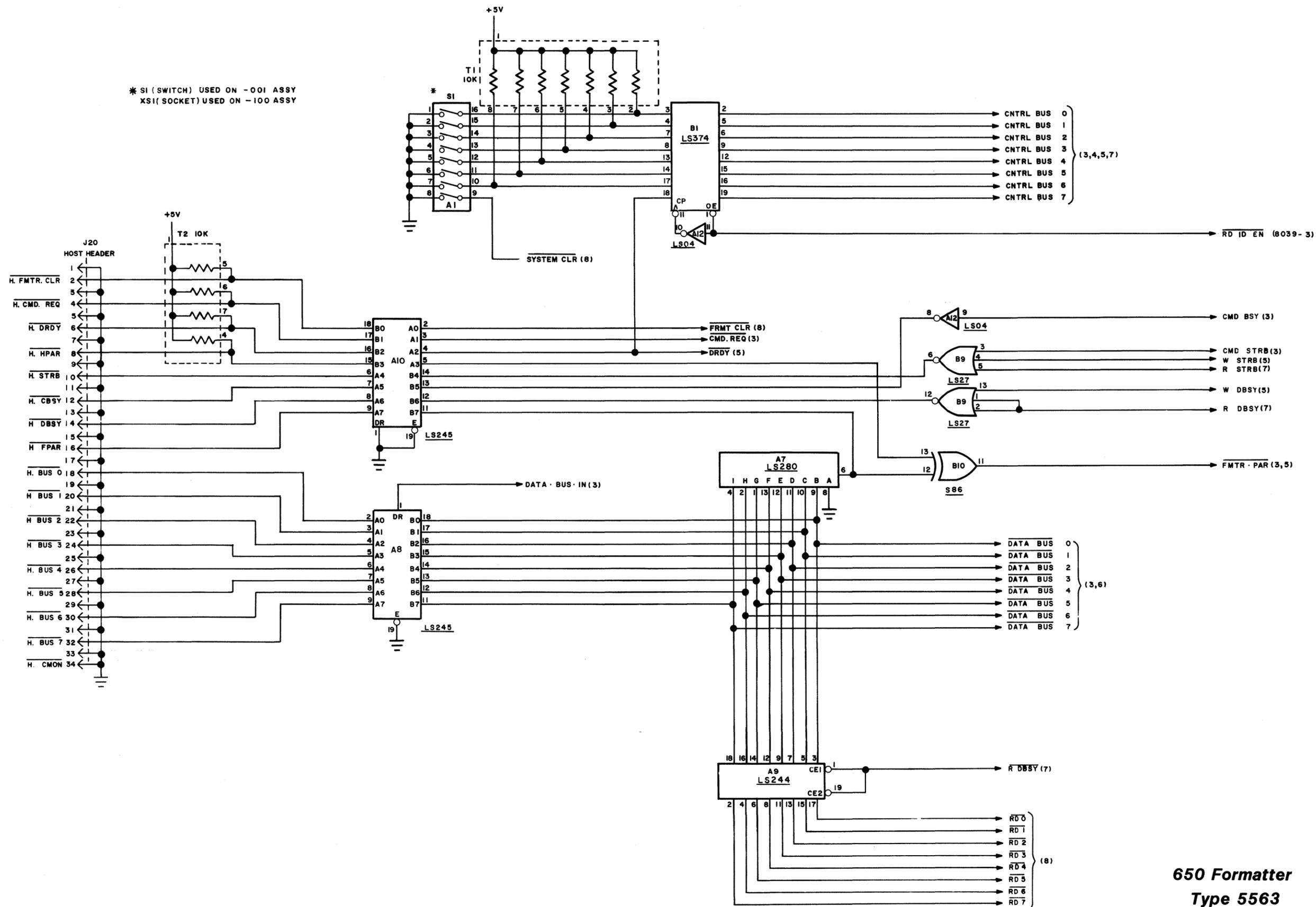
Set of nut drivers or open end wrenches
Phillips and standard slot-head screwdrivers
Maintenance Kit, Kennedy PN 190-2324-001, which contains:

Head cleaner
Hex socket keys 7/64", 5/32", 1/8", 3/32"
Reflective marker strips*
Magnasee visualizing solution
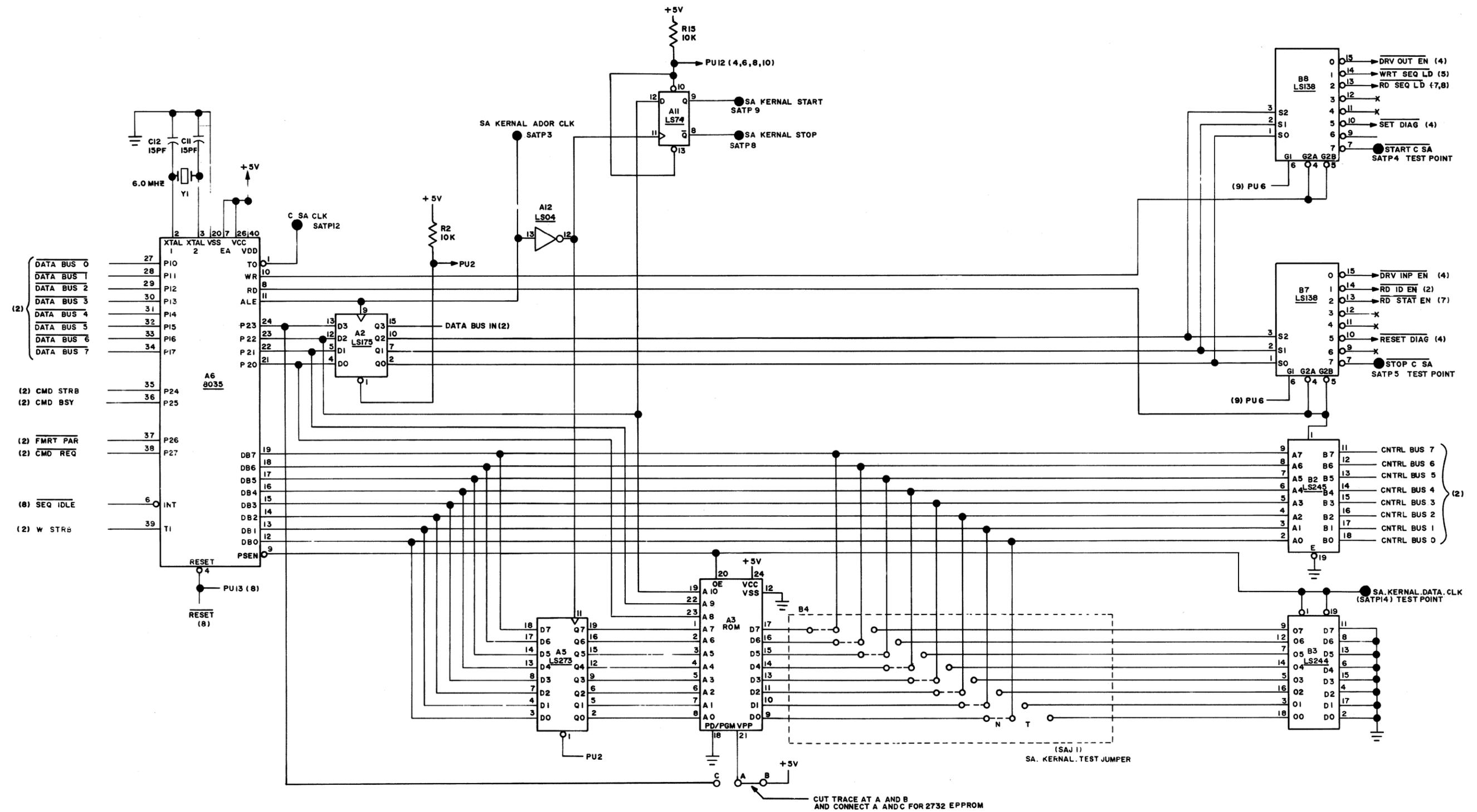Loctite, grade H
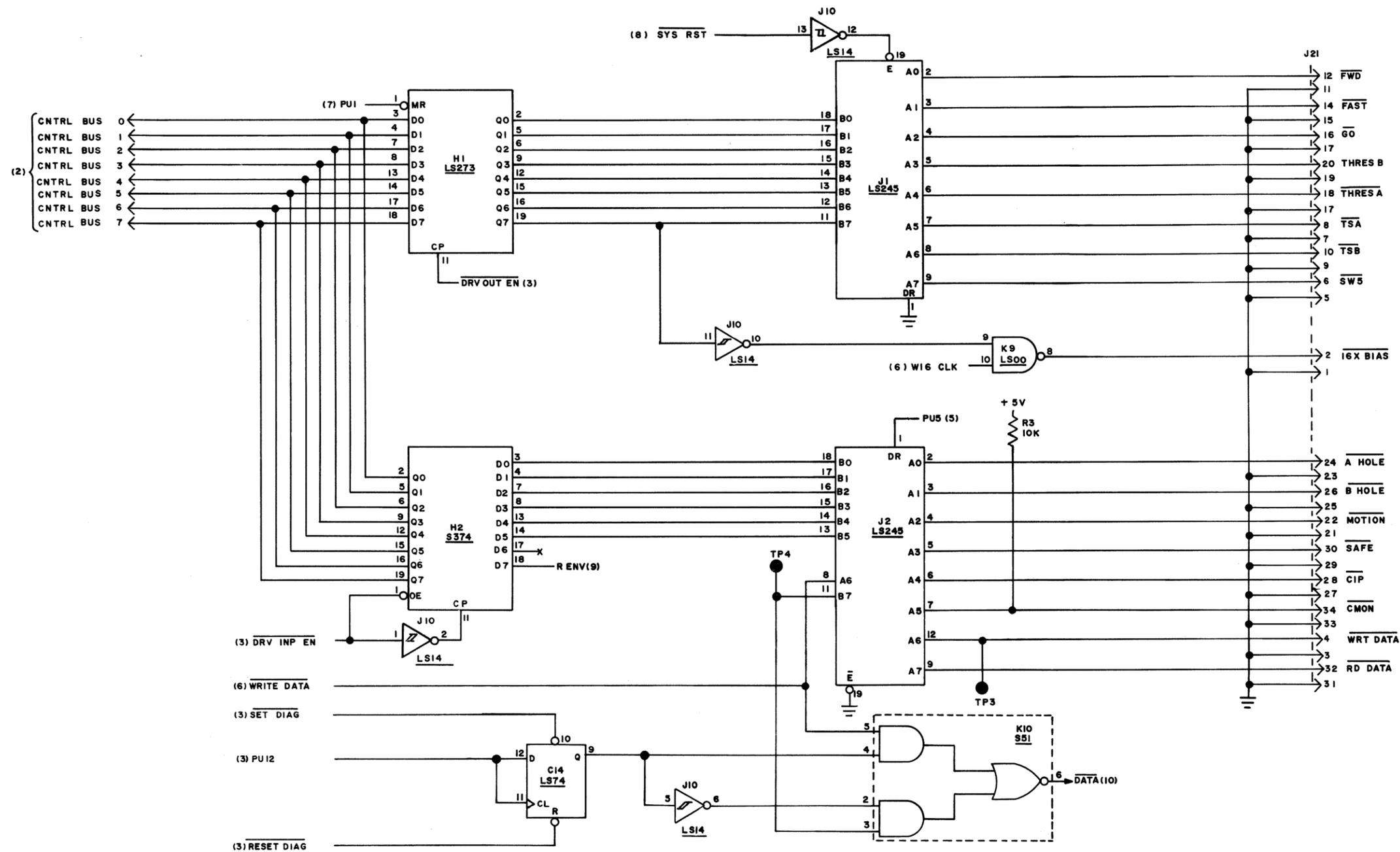Tension arm and roller gauges*
Wrench Set

*Not used on cartridge drive.

650 Formatter
Type 5563
Schematic Diagram

650 Formatter

Type 5563

Schematic Diagram

650 Formatter

Type 5563

Schematic Diagram

650 Formatter
Type 5563
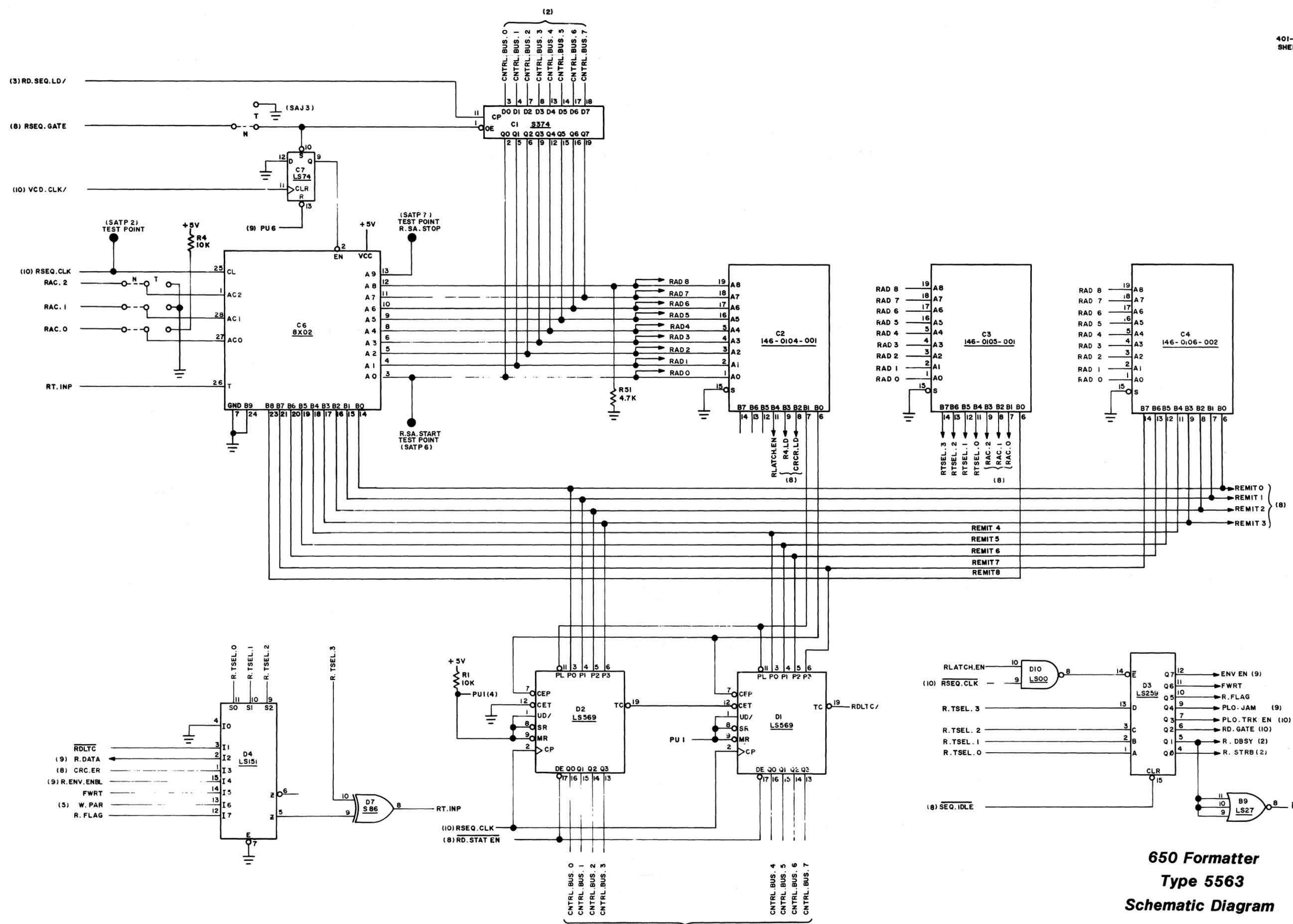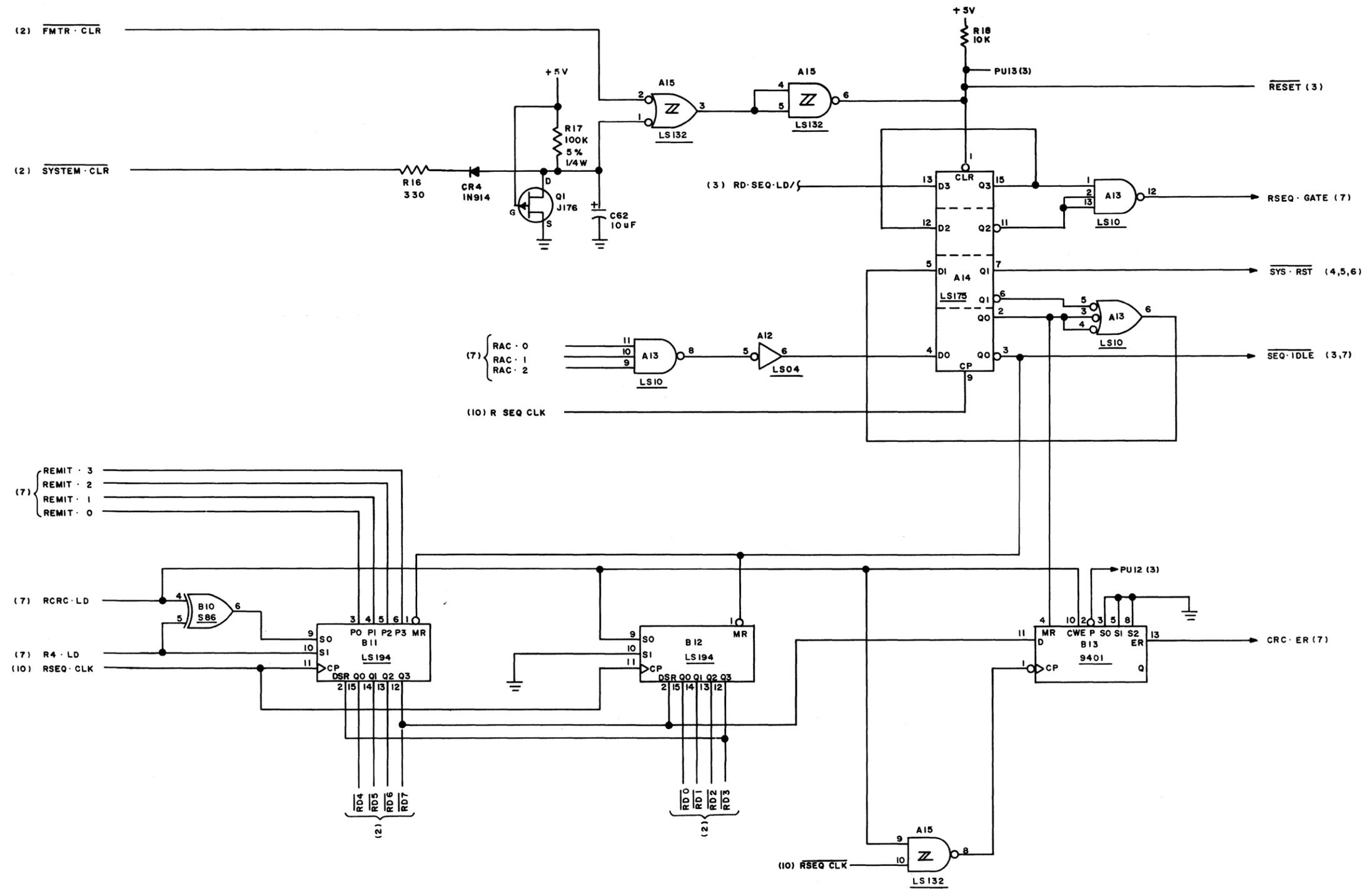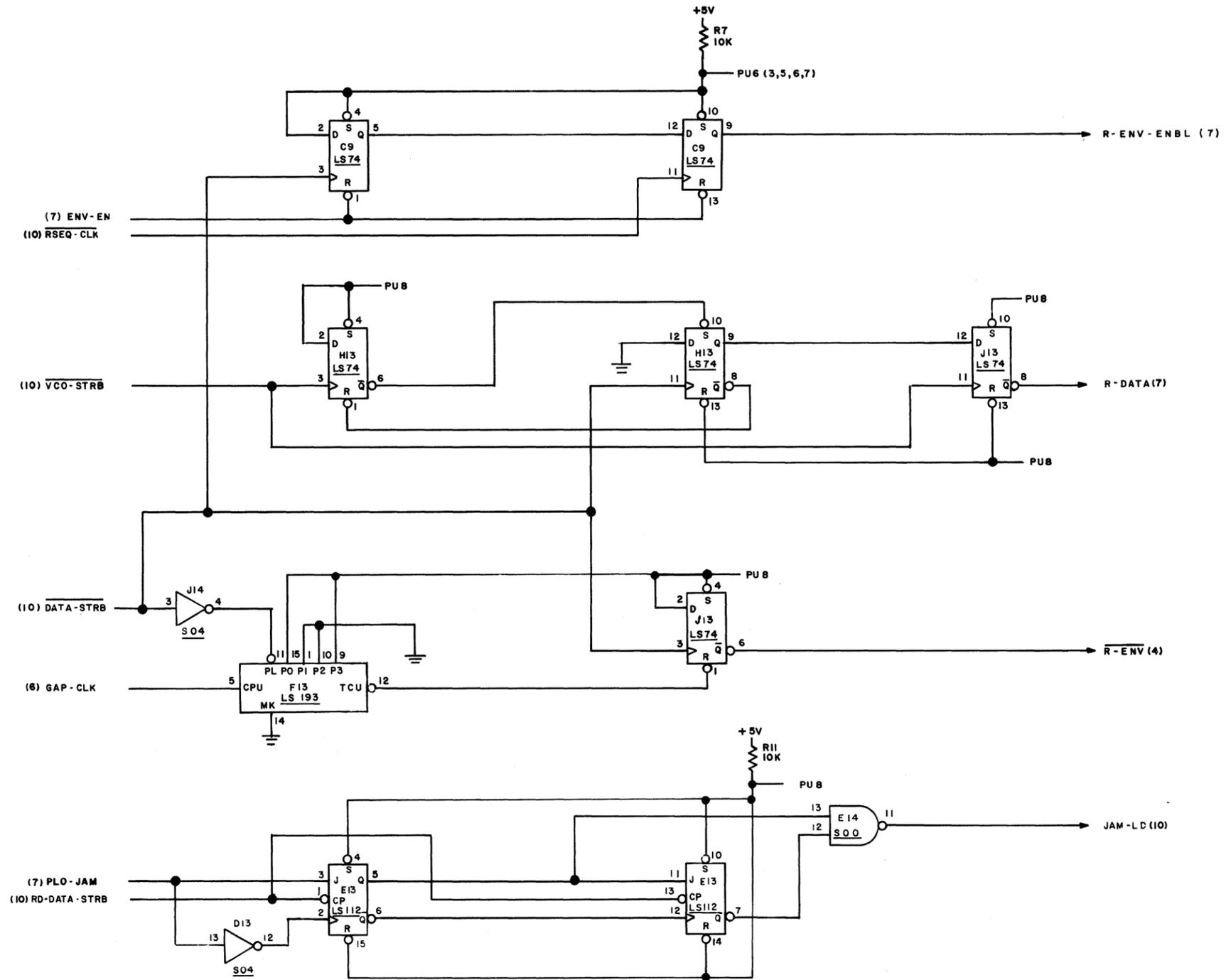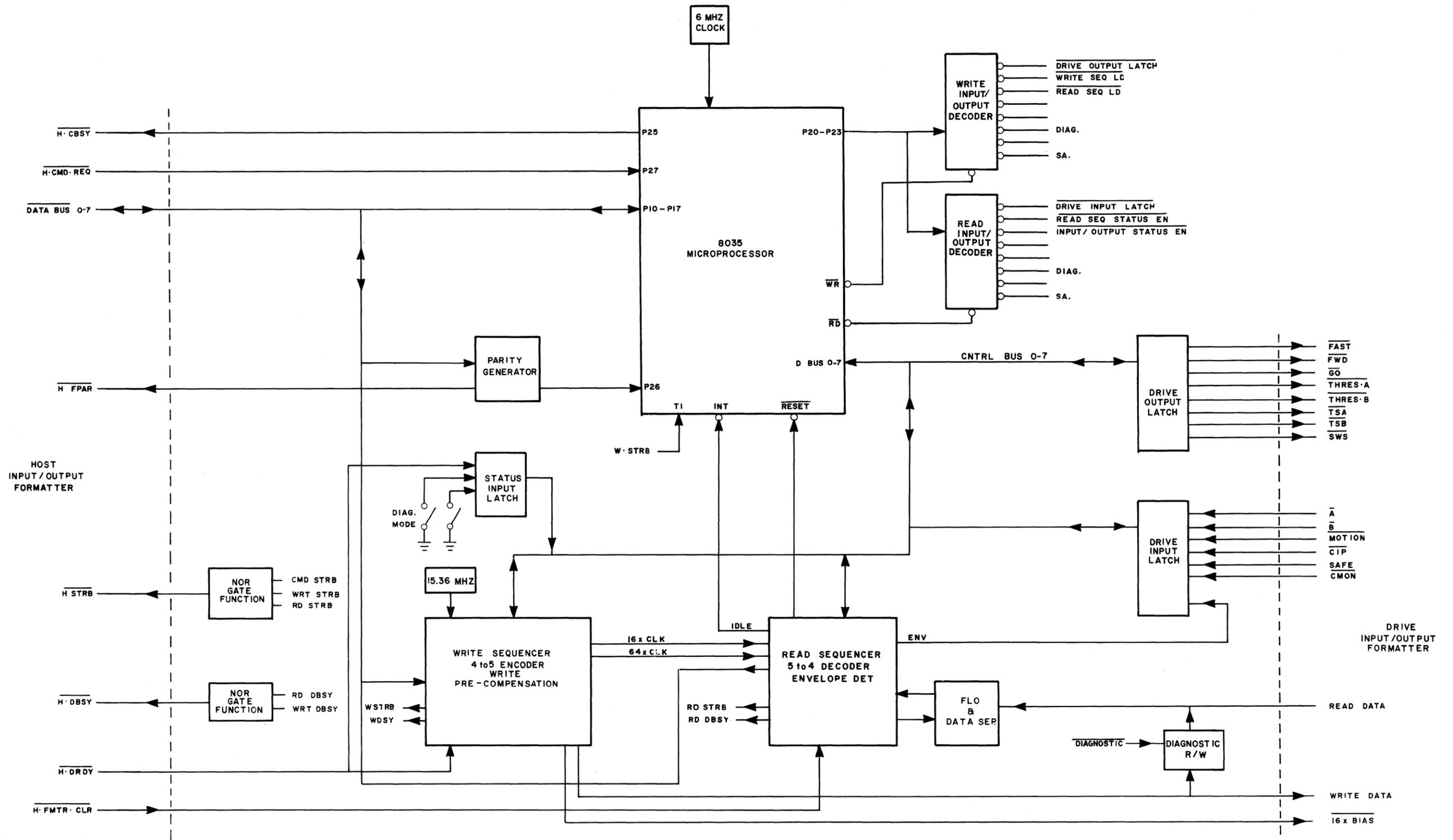Schematic Diagram

650 Formatter
Type 5563
Schematic Diagram

650 Formatter

Type 5563

Schematic Diagram

650 Formatter
Type 5563
Schematic Diagram

650 Formatter
Type 5563
Schematic Diagram

650 Formatter
Type 5563
Schematic Diagram

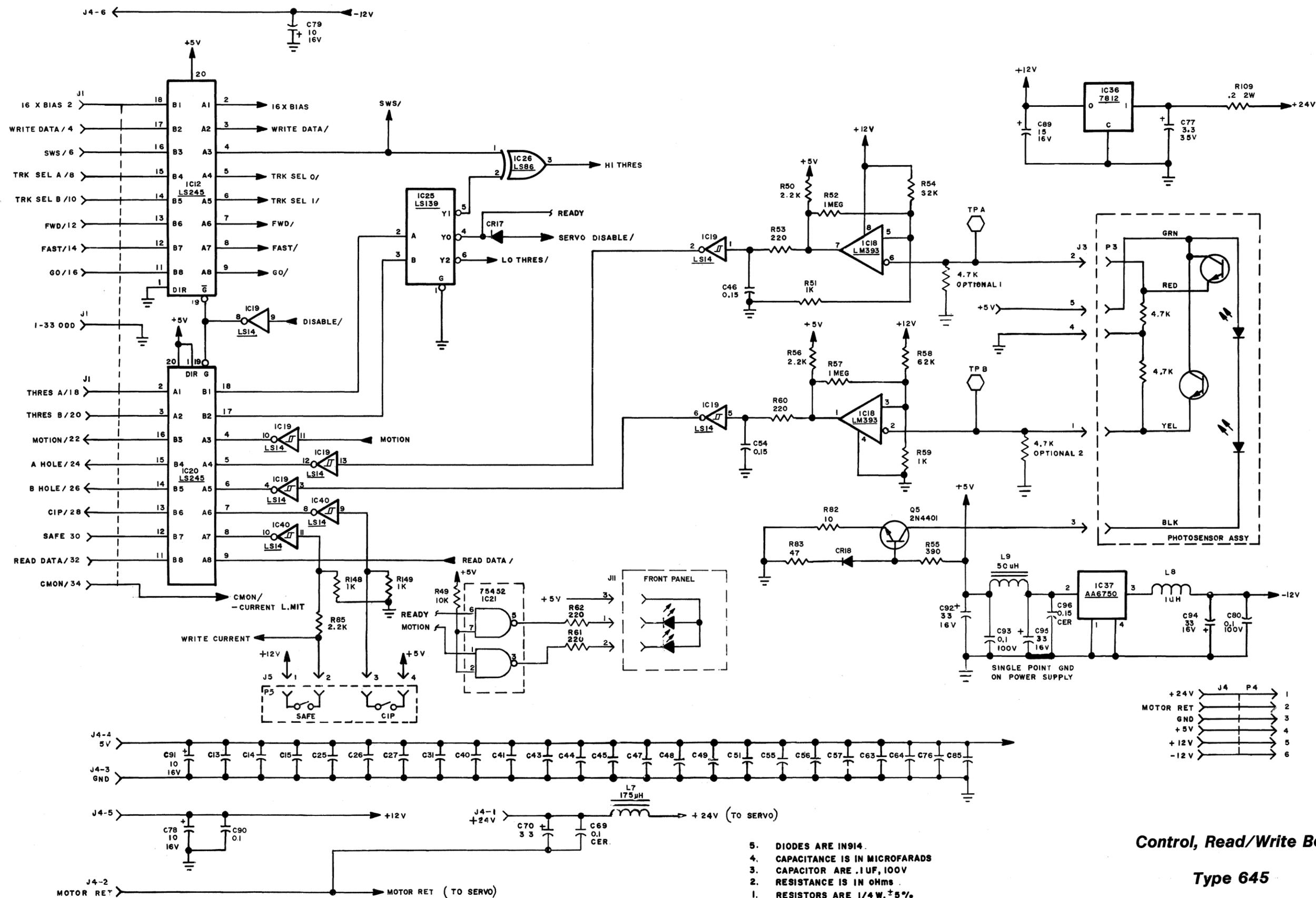650 Formatter
Type 5563
Schematic Diagram

J4-6

C79
10
16V

-12V

+5V
20

+12V

IC36
7812

R109
.2 2W

+24V

C89
15
16V

C77
3.3
35V

J1

16 X BIAS 2   18 B1   A1 2   16 X BIAS
WRITE DATA/4   17 B2   A2 3   WRITE DATA/
SWS/6   16 B3   A3 4
TRK SEL A/8   15 B4   A4 5   TRK SEL 0/
TRK SEL B/10   14 B5   A5 6   TRK SEL 1/
FWD/12   13 B6   A6 7   FWD/
FAST/14   12 B7   A7 8   FAST/
GO/16   11 B8   A8 9   GO/
                   IC12
                   LS245
               DIR G

SWS/

IC26
LS86
HI THRES

IC25
LS139
A Y1 5
   Y0 4   CR17   READY
B Y2 6   SERVO DISABLE/
G   LO THRES/

R50
2.2K
R52
1MEG
R54
32K

IC18
LM393

TP A

R53
220

C46
0.15
R51
1K

IC19
LS14

4.7K
OPTIONAL 1

+5V

J3
P3

GRN

RED

4.7K

4.7K

YEL

I-33 ODD

IC19
LS14
DISABLE/

+5V
20 1 19

DIR G
J1
THRES A/18   2 A1   B1 18
THRES B/20   3 A2   B2 17
MOTION/22   16 B3   A3 4   MOTION
A HOLE/24   15 B4   A4 5
B HOLE/26   14 B5   A5 6
CIP/28   13 B6   A6 7
SAFE 30   12 B7   A7 8
READ DATA/32 11 B8   A8 9   READ DATA /
             IC20
             LS245

IC19
LS14

IC19
LS14

IC19
LS14

IC40
LS14

IC40
LS14

R56
2.2K
R57
1MEG
R58
62K

IC18
LM393

TP B

R60
220

C54
0.15
R59
1K

4.7K
OPTIONAL 2

BLK

PHOTOSENSOR ASSY

R82
10
Q5
2N4401

R83
47
CRI8
R55
390

+5V

L9
50 uH

IC37
AA6750

L8
1uH

-12V

C92
33
16V
C93
0.1
100V
C95
33
16V
C96
0.15
CER
C94
33
16V
C80
0.1
100V

SINGLE POINT GND
ON POWER SUPPLY

CMON/34

CMON/
- CURRENT LIMIT

WRITE CURRENT

R148
1K
R149
1K

R85
2.2K

+12V   +5V

J5 1 2   3 4
P5
SAFE   CIP

+5V
R49
10K
75452
IC21

R62
220
R61
220

J11
FRONT PANEL

READY
MOTION

+5V 3

1
2

+24V   J4 P4
MOTOR RET
GND
+5V
+12V
-12V

1
2
3
4
5
6

J4-4
5V

C91 C13 C14 C15 C25 C26 C27 C31 C40 C41 C43 C44 C45 C47 C48 C49 C51 C55 C56 C57 C63 C64 C76 C85

J4-3
GND

C91
10
16V

L7
175µH

J4-5   +12V
C78
10
16V
C90
0.1

J4-1
+24V
C70
33
C69
0.1
CER
+24V (TO SERVO)

J4-2
MOTOR RET
MOTOR RET (TO SERVO)
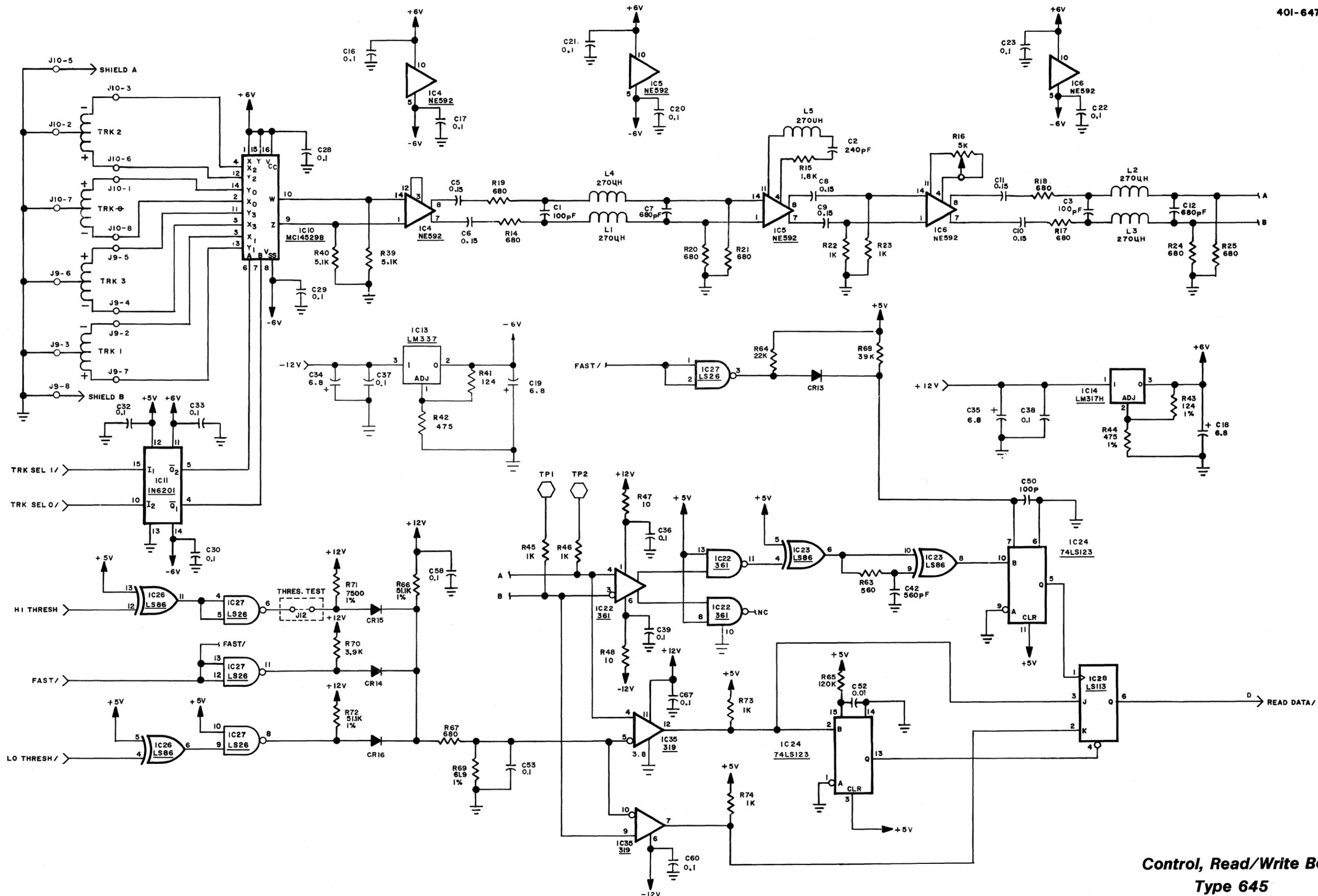
5. DIODES ARE 1N914.
4. CAPACITANCE IS IN MICROFARADS
3. CAPACITOR ARE .1UF, 100V
2. RESISTANCE IS IN oHms
1. RESISTORS ARE 1/4 W, ±5%.
NOTES: UNLESS OTHERWISE SPECIFIED.

Control, Read/Write Board

Type 645

Schematic Diagram

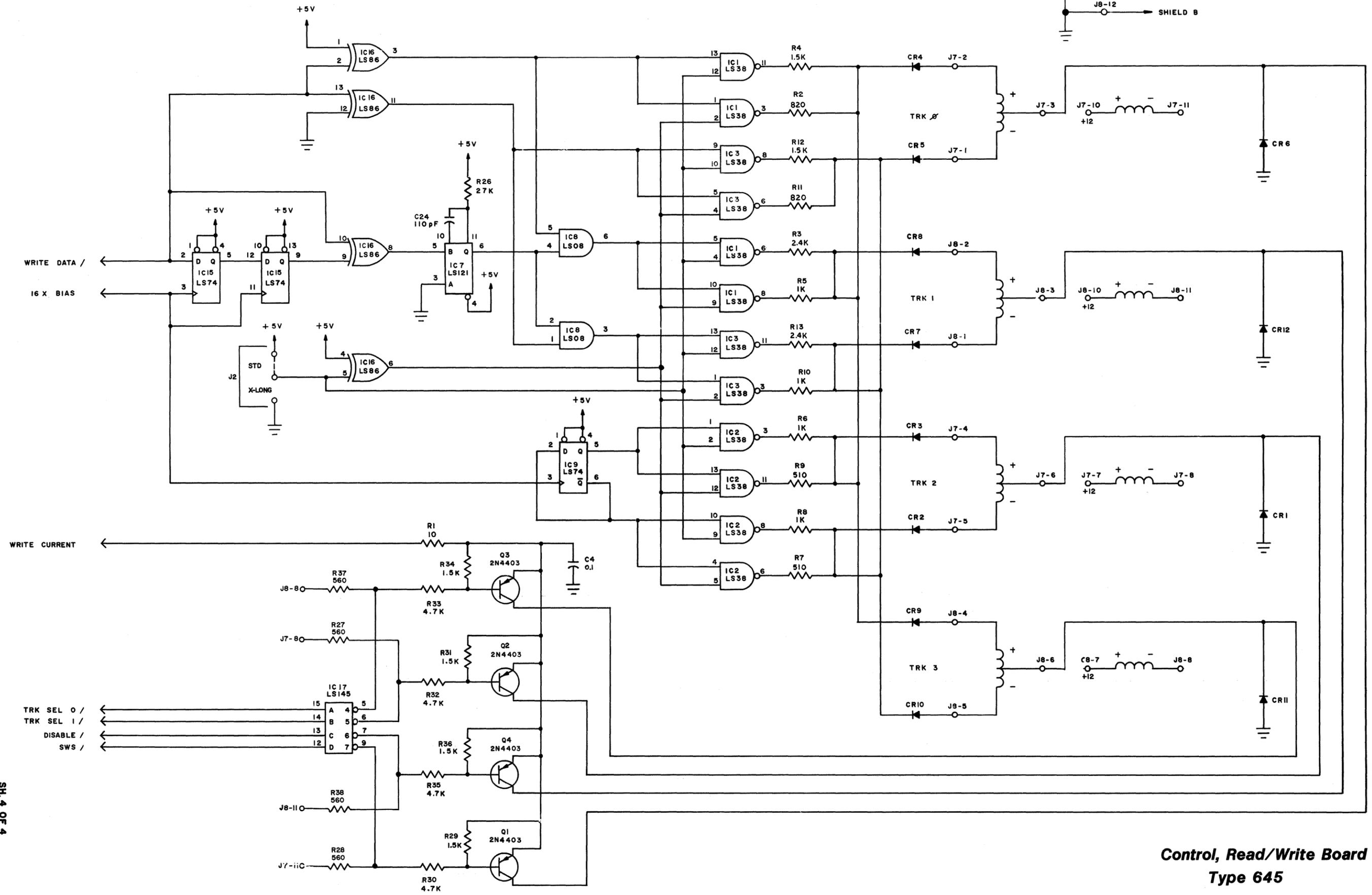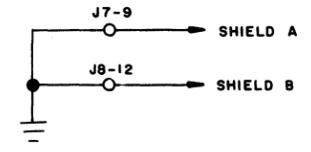401-6478-001 R

Control, Read/Write Board
Type 645
Schematic Diagram

SH. 2 OF 4
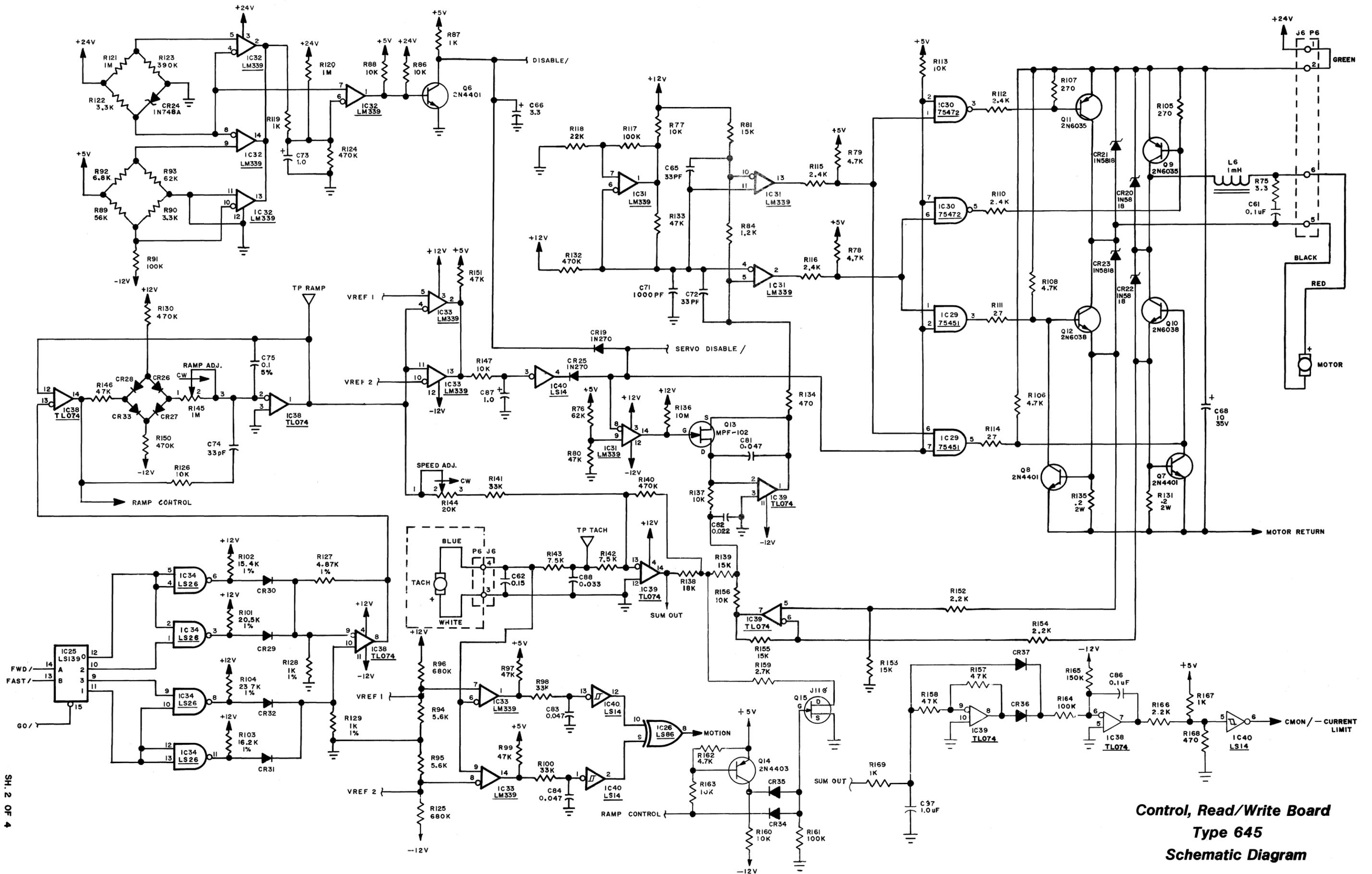
Control, Read/Write Board
Type 645
Schematic Diagram

Control, Read/Write Board
Type 645
Schematic Diagram

SH. 4 OF 4

Warranty

The Company warrants its devices against faulty workmanship or the use of defective materials (except in those cases where the materials are supplied by OEM) for a period of one year from the date of shipment to OEM, with the exception of $\frac{1}{4}$" cartridge products which are warranted for a period of ninety (90) days.

The liability of the Company under this warranty is limited to replacing, repairing, or issuing credit (at the Company's discretion) for any devices which are returned by OEM during such period provided that (a) the Company is promptly notified in writing upon discovery of such defects by OEM; (b) the defective unit is returned to the Company, transportation charges prepaid by OEM; and (c) the Company's examination of such unit shall disclose to its satisfaction that such defects have not been caused by misuse, neglect, improper installation, repair alteration or accident.

Kennedy Company is continually striving to provide improved performance, value and reliability in its products and reserves the right to make these changes without being obligated to retrofit delivered equipment.

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