MN3726MFE, MN3726MAE

6mm (1/3 inch) 512H High-Resposivity CCD Area Image Sensors

■ Overview

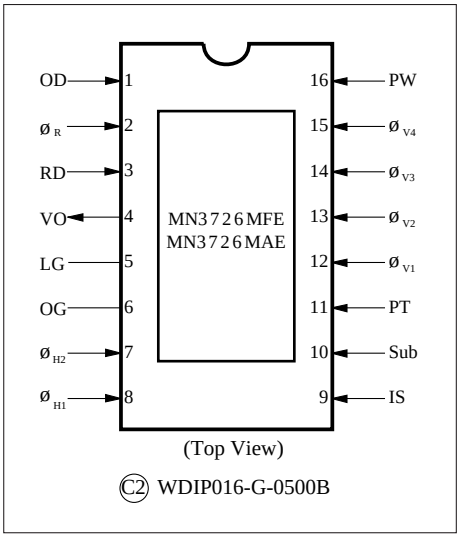
The MN3726MFE and MN3726MAE are 6mm (1/3 inch) Interline Transfer CCD (IT-CCD) solid state image sensor devices.

This device uses photodiodes in the optoelectric conversion section and CCDs for signal read out. The electronic shutter function has made possible an exposure time of 1/10000 seconds. Further, this device has the features of high sensitivity, low noise, broad dynamic range, and low smear.

This device has a total of 320K pixels (542 horizontal × 584 vertical) and provides stable and clear images with a resolution of 330 horizontal TV-lines and 420 vertical TV-lines.

Type No.	Size	System	Color or B/W
MN3726MFE	6mm (1/3 inch)	PAL	Color
MN3726MAE		CCIR	B/W

■ Pin Assignments



(Top View)

Ⓒ2 WDIP016-G-0500B

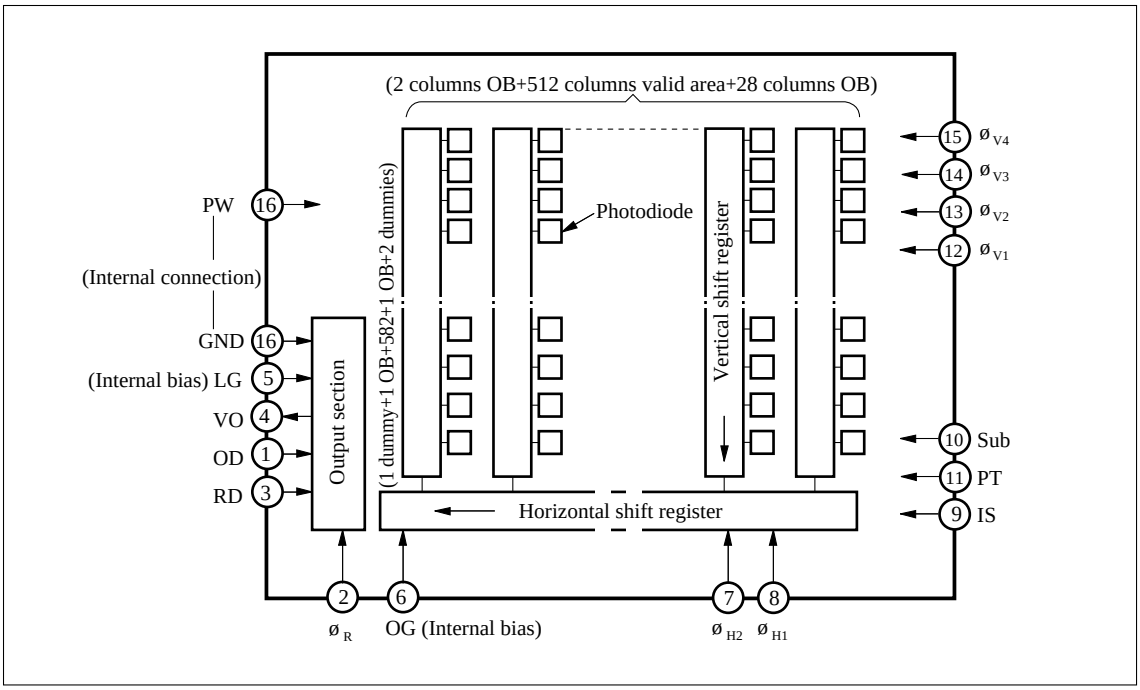
■ Features

- Total number of pixels: 542 (horizontal) × 584 (vertical)
- High sensitivity
- Low noise
- Broad dynamic range
- Low smear
- Low image lag
- Electronic shutter function present
- No image distortion
- Small size enables design of compact equipment
- High reliability
- 16 Pin DIL ceramic package (cerdip)

■ Applications

- Compact lightweight camcoders
- Communication television systems
- Door cameras
- Cameras for measurement use
- Cameras for medical use

■ Block Diagram



■ Pin Descriptions

Pin No.	Symbol	Descriptions	Pin No.	Symbol	Descriptions
1	OD	Output drain	9	IS	Input source
2	ø R	Reset pulse	10	Sub	Substrate
3	RD	Reset drain	11	PT	P-well for protection circuit
4	VO	Video output	12	ø V1	Vertical shift register clock pulse (1)
5	LG	Output load transistor gate	13	ø V2	Vertical shift register clock pulse (2)
6	OG	Output gate	14	ø V3	Vertical shift register clock pulse (3)
7	ø H2	Horizontal register clock pulse (2)	15	ø V4	Vertical shift register clock pulse (4)
8	ø H1	Horizontal register clock pulse (1)	16	PW	P-well

■ Absolute Maximum Ratings and Operating Conditions

Parameter	Symbol	Rating		Operating condition			Unit
		min	max	min	typ	max	
Reset drain voltage	V_{RD} * 1, 3	– 0.2	18	14.5	15.0	15.5	V
Output drain voltage	V_{OD} * 1, 3	– 0.2	18	14.5	15.0	15.5	V
Output load transistor gate voltage	V_{LG} * 1, 3, 6	(Supplied internally)					V
Output gate voltage	V_{OG} * 1, 3, 6	(Supplied internally)					V
Horizontal CCD input source voltage	V_{HS}	– 0.2	18	14.5	15.0	15.5	V
Protection P well voltage	V_{PT}	–10	0.2	$ø_{V(L)}$ –1.2	$ø_{V(L)}$ –1	$ø_{V(L)}$ – 0.7	V
P well voltage	V_{PW}	Reference voltage		—	0	—	V
Reset pulse voltage H-L Bias	$V_{ø R (H)}$ * 2	—	18	4.7	5	5.3	V
	$V_{ø R (L)}$ * 2	– 0.2	—	0	Adjust	5.0	V
Horizontal register clock pulse voltage 1	$V_{ø H1 (H)}$ * 2	—	18	4.5	5	5.5	V
	$V_{ø H1 (L)}$ * 2	– 0.2	—	– 0.1	0	0.1	V
Horizontal register clock pulse voltage 2	$V_{ø H2 (H)}$ * 2	—	18	4.5	5	5.5	V
	$V_{ø H2 (L)}$ * 2	– 0.2	—	– 0.1	0	0.1	V
Vertical shift register clock pulse voltage 1	$V_{ø V1 (H)}$ * 2, 5	—	18	14.5	15	15.5	V
	$V_{ø V1 (M)}$ * 2, 5	—	—	– 0.2	0	0.2	V
	$V_{ø V1 (L)}$ * 2, 5	–9	—	–7.3	–7	–6.7	V
Vertical shift register clock pulse voltage 2	$V_{ø V2 (M)}$ * 2, 5	—	15	0.8	1	1.2	V
	$V_{ø V2 (L)}$ * 2, 5	–9	—	–7.3	–7	–6.7	V
Vertical shift register clock pulse voltage 3	$V_{ø V3 (H)}$ * 2, 5	—	18	14.5	15	15.5	V
	$V_{ø V3 (M)}$ * 2, 5	—	—	– 0.2	0	0.2	V
	$V_{ø V3 (L)}$ * 2, 5	–9	—	–7.3	–7	–6.7	V
Verticaal shift register clock pulse voltage 4	$V_{ø V4 (M)}$ * 2, 5	—	15	0.8	1	1.2	V
	$V_{ø V4 (L)}$ * 2, 5	–9	—	–7.3	–7	–6.7	V
Substrate voltage	V_{Sub} *4	– 0.2	45	3	Adjust	13.8	V
Operating temperature	T_{opr}	–10	70	—	25	—	˚C
Storage tempsrature	T_{stg}	–30	80	—	—	—	˚C

Note 1) The initial setting of V_{Sub} shall be 8.0V and shall be adjusted to the minimum voltage at which no blooming is caused at a light input of 100 times the standard value. The standard light input is the one when the exposure is done at a specified aperture using a light source of 2856K and 1050nt, and placing a color temperature conversion filter LB-40 (Hoya) and an IR cutting filter CAW-500S (t=2.5mm) in the light path.

Note 2) See pulse timing diagrams on the following page.

Note 3) Absolute maximum ratings: $-0.2 < V_{Sub} - V_{PT} < +55$ (V)
$-0.2 < V_{øV} - V_{PT} < +24.5$ (V)

Note 4) V_{Sub} power supply impedance should be 100 Ohms or less.

Note 5) Output impedance of the $ø_{V1}$ to $ø_{V3}$ drivers should be 30 Ohms or more, while their power supply capacitance should be 10mA or less.

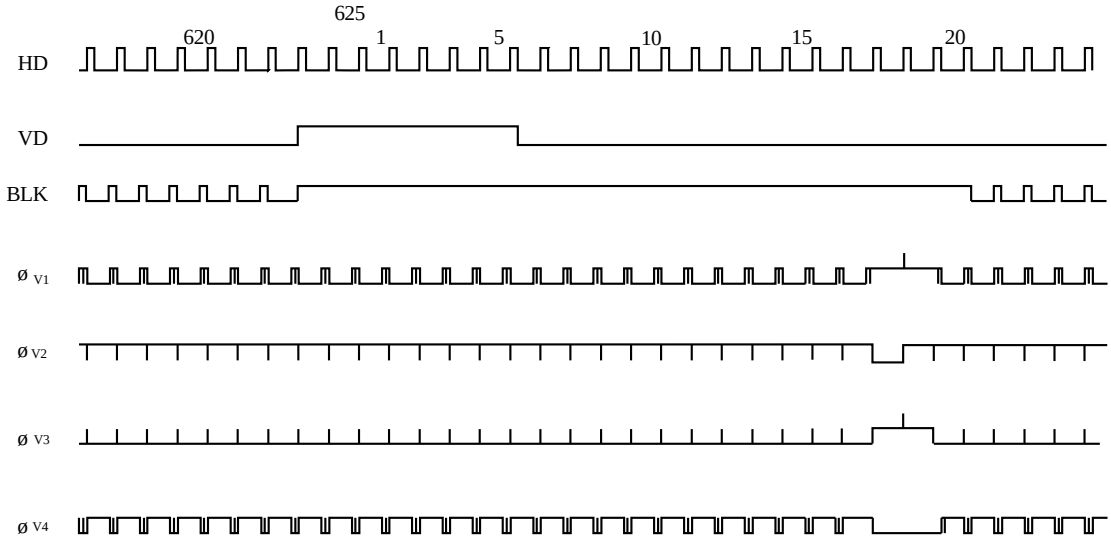
Note 6) The LG and OG pins should each be grounded via a capacitor of 0.047µF or more.

■ Optical Characteristics

Type No.	Color or B/W	Valid pixels H	Valid pixels V	S/N typ. (dB)	Saturation output typ. (mV)	Sensitivity F8 typ. (mV)	Vertical smear Sm typ. (%)	Image lag typ. (%)	Horizontal resolution typ. (TV-lines)	Vertical resolution typ. (TV-lines)
MN3726MFE	Color	512	582	60	700	300	0.002	0	330	420
MN3726MAE	B/W	512	582	60	1,000	400	0.003	0	360	420

■ Example of Recommended Driving Pulses

< Field A >



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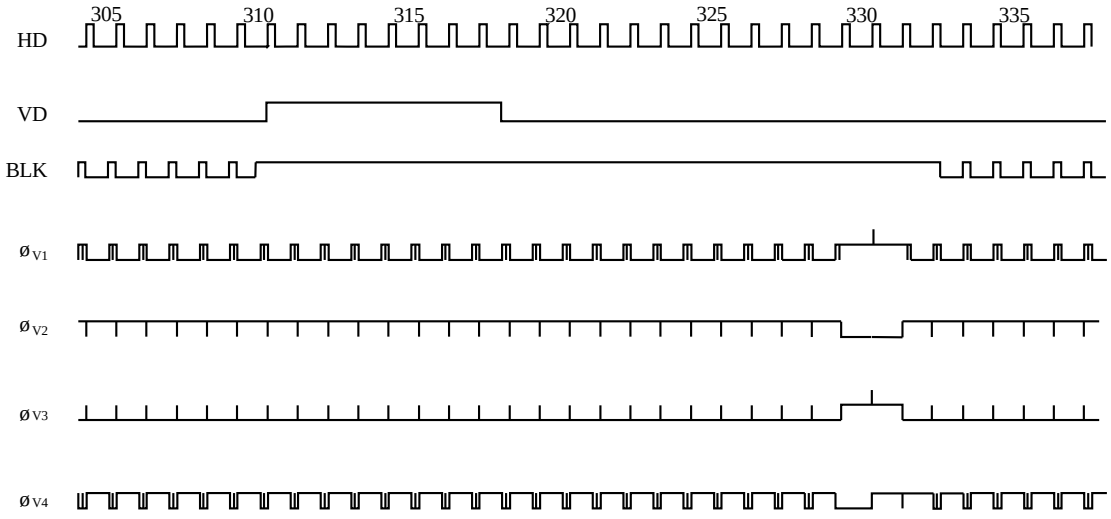

■ Example of Recommended Driving Pulses (continued)