Series 3000 Technical Reference Manual

MAD Intelligent Systems
2950 Zanker Road
San Jose, CA 95134

Notice to Users

Warning: This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

The user is warned that the shielded cables provided with this equipment MUST be used. A failure to use shielded cables may result in excessive radio-frequency emissions in violation of FCC Rules, for which the user would be responsible. If any extension cables are used they must also be shielded and the shields connected by means of metal-shell connectors so that there is a full 360 degrees of connection; pigtail connections are not good enough for radio frequencies.

Copyright

Disclaimer

MAD Intelligent Systems, Inc. does not make representations or warranties to the contents of this publication and disclaims any warranties of merchantability or fitness for a particular purpose. Additionally, MAD Intelligent Systems, Inc. reserves the right to revise and make changes to the content of this publication without obligation to inform any person of such revision.

MS-DOS is a registered trademark of Microsoft, Inc.

UNIX is a registered trademark of AT & T

Part Number 500026

Revision B of September 1988

Joyce De Mattei, Writer

About This Manual

This manual, which is written for technical maintenance personnel, system designers, and applications programmers, contains design and maintenance information for the Series 3000 Intelligent Workstation. Information about the workstation includes:

- A system overview
- The motherboard
- The Basic Input/Output System (BIOS) firmware
- The keyboard controller
- The memory board
- The Advanced Graphics Controller and optional PC Video Emulator
- The power supply
- Product specifications

Organization

This section summarizes each of the chapters in this manual.

Chapter 1. "Overview" is a description of the Series 3000 Intelligent Workstation.

Chapter 2. "Motherboard" defines the overall operation and performance of the major components on the motherboard, including the 80386 microprocessor. The optional 80287/80387 numerics coprocessor modes and functions are discussed, with a brief reference to the 82C301 bus controller and the 82C302 memory controller. The chapter also contains programming and interface information needed to develop software.

Chapter 3. "BIOS" provides the BIOS programming information on input/output control used by systems and applications programmers when developing software.

Chapter 4. "Keyboard" describes the operation of the keyboard controller, which is on the motherboard. Programming and interface information is included.

Chapter 5. "Memory" contains the specifications and instructions for the 32-bit memory board.

Chapter 6. "Advanced Graphics Controller" describes the video controller that supports video monitors. This chapter also describes the optional PC Video Emulator board which piggybacks onto the Advanced Graphics Controller for MS-DOS operation.

Chapter 7. "Power Supply" describes the power supply requirements.

Appendix A. "Product Specifications" lists the specifications for the Series 3000 Intelligent Workstation.

Related Documents

For further technical information about the Series 3000 Intelligent Workstation, refer to the following manuals:

- *Series 3000 Customer Engineer's Manual* (MAD Part Number 500027)
- *RD²S 3000 User's Guide* (MAD Part Number 500025)
- *Monochrome Monitor Manual* (MAD Part Number 500053)
- *M4 Optical Mouse Technical Reference Manual*, Mouse Systems Corporation (MAD Part Number 500434)

In addition, the following manuals contain technical information you might need:

- *YD-380B-PC*, C. Itoh Electronics, Inc. (Order Number FDL-525041 Rev. A)
- *M255XA 51/4" Mini Flexible Disk Drives Product Specifications*, Fujitsu (Order Number RS-007-062785)
- *WD-1003-WA2 Winchester Disk/Floppy Disketter Controller Preliminary OEM Manual*, Western Digital Corporation
- *Wangtec PC-36 Controller OEM Manual*, Wangtec, Inc. (Order Number 20593-001)
- *Miniscribe VI Product Manual*, Models 6032, 6053, 6074, 6085, Part Number 1011, Rev. P4, Miniscribe Corporation (Order Number 170046)
- *iAPX 386 Programmer's Reference Manual*, Intel Corporation (Order Number 230985)
- *iAPX 386 Hardware Reference Manual*, Intel Corporation (Order Number 231732)
- *iAPX 386 System Software Writer's Guide*, Intel Corporation (Order Number 231499)
- *Microsystem Component Handbook*, Intel Corporation (Order Number 230843-004)

- *iAPX 80387 Hardware Reference Manual*, Intel Corporation (Order Number 231732-001)
- *iAPX 80386 Data Sheet*, Intel Corporation (Order Number 231630)
- *CS 8230 AT/386 CHIPSet Hardware Reference Manual*, Chips and Technologies
- *82C206 Hardware Reference Manual*, Chips and Technologies
- *PC-36 Internal Tape Backup System User's Manual*, Wangtek, Inc. (Part Number 63009-001)
- *82786 Graphics Coprocessor User's Manual*, Intel Corporation (Order Number 231933-002)
- *82786 CHMOS Graphics Coprocessor*, Intel Corporation (Order Number 231676-002)
- *82786 Hardware Configuration Applications Note AP-270*, Intel Corporation (Order Number 292007-002)
- *82786 CHMOS Graphics Coprocessor Architectural Overview Applications Note AP-259*, Intel Corporation (Order Number 122711-002)
- *Bt451 RAMDAC Data Sheet*, Brooktree Corporation (Order Number DS011a-9/85)

Contents

Figures

Chapter 1. Overview

Introduction

The Series 3000 Intelligent Workstation is a multiuser, multiprocessor, and multitasking system. This chapter summarizes the main features of the Series 3000 Intelligent Workstation. The major components of the system are the following:

- the system unit
- the keyboard
- the video monitor
- the mouse

The system unit contains the hard disk drive, floppy disk drive, cartridge tape drive, motherboard, power supply, tape drive controller board, video monitor controller board, disk drive controller board, and memory board. Other hardware options can be installed. Figure 1-1 illustrates a typical system unit.

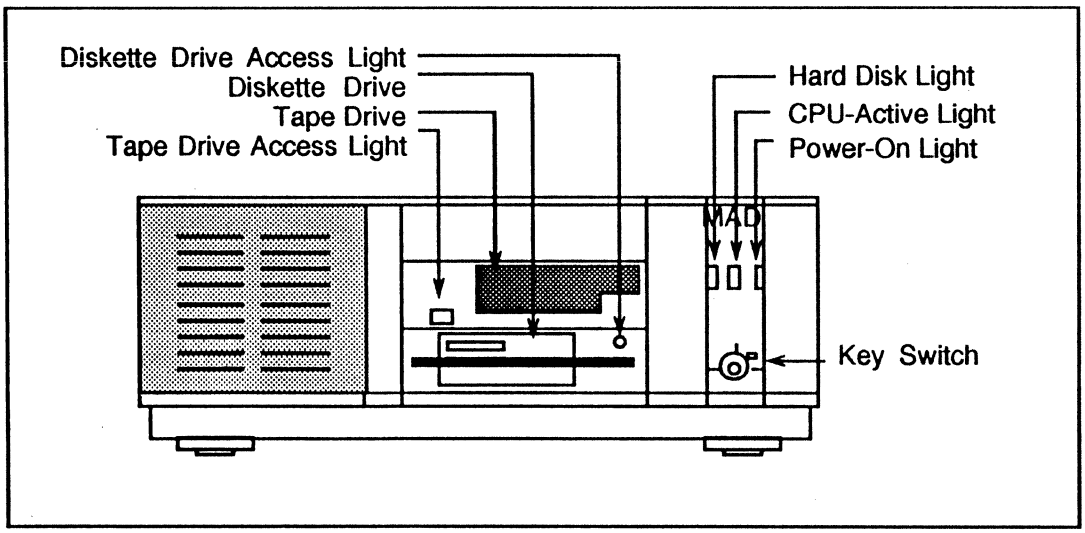

Figure 1-1. Typical System Unit

Workstation Features

The features of the Series 3000 Intelligent Workstation are as follows:

- MAD/ix operating system
- 80386 microprocessor
- 4 to 16MB of RAM memory
- 20-inch monochrome graphics monitor
- Advanced Graphics Controller
- Keylock feature with removable high-security key
- Keyboard
- Three-button optical mouse
- 1.2MB 5 1/4-inch high-density floppy disk drive
- 5 1/4-inch full height fixed disk drive
- 60MB tape drive
- Power supply
- Expansion capabilities

These features are discussed in the following sections.

MAD/ix

The Series 3000 Intelligent Workstation is shipped and tested with MAD/ix, MAD's implementation of the UNIX System V, Release 3.0 operating system.

Microprocessor

The microprocessor is the 80386, running at either 16 or 20 MHz. This microprocessor supports either the optional 80287 coprocessor or the 80387 coprocessor. The coprocessor works in parallel with the 80386 microprocessor. The coprocessor increases net processing speed by performing numerical

functions while the 80386 microprocessor attends to other concurrent tasks. See the chapter "Motherboard" for more information.

Main Memory

Main memory configurations run from 1MB to 16MB using either 256KB Single Inline Memory Module (SIMM) DRAMs or 1MB SIMM DRAMs. The minimum system configuration is 1MB for MS-DOS and 4MB for MAD/ix. For more information, see the chapter "Memory."

Monitor

The high-resolution 20-inch monochrome graphics monitor is designed for professional graphics and alphanumeric workstations. The maximum pixel format is 1280 pixels by 1024 lines. The unit includes a CRT, deflection electronics, video drive circuitry, CRT protection circuitry, an AC power supply, and a cabinet with tilt and swivel capability.

Advanced Graphics Controller

The Advanced Graphics Controller (AGC) is a high-resolution, high-performance graphics subsystem optimized for high-speed window performance. For more information, see the chapter "Advanced Graphics Controller."

Keylock Feature

The keylock feature with removable high-security key is located on the front panel. The four positions of the keylock from left to right are power off, power on (keyboard disabled), power on (keyboard enabled), and reset. For more informaton see the chapter "Hardware Description" in the *RD²S 3000 User's Guide* (MAD Part Number 500025).

Keyboard

The keyboard supported is the AT/E 101-key keyboard. No user interaction or setup is required. For more information on the keyboard, see the chapter "Keyboard" in this manual.

Mouse

One of the workstation's input devices is the three-button optical mouse. This mouse, which has an RS-232-C interface, operates on a special color-coded, 25 grid per inch pad and uses a red LED and an infrared LED to generate motion information via the grid. Power for operation is obtained from the RS-232-C signals. Pin/signal information for J9 can be found in the chapter "Motherboard." The mouse operates at 1200 baud, 8 data bits, 1 start bit, 1 stop bit, and no parity. Software to use the mouse under the X Window System is included. No MS-DOS software drivers are included. For additional information on the optical mouse, see the manual *Mouse Systems Corporation M4 Optical Mouse Technical Reference Manual* (MAD Part Number 500434).

Floppy Disk Drive

The 1.2MB 5 1/4-inch high density (96 tpi) floppy disk drive is the standard floppy disk drive on the Series 3000 Intelligent Workstation.

Disk Controller

Two disk controllers are supported. The ST506 disk controller can support up to two Winchester disk drives and two floppy disk drives. The ST506 disk controller controls one ST506 Winchester disk drive and 1 high density (96 tpi, 1.2MB) floppy disk drive. The ESDI controller controls one ESDI Winchester disk drive and one high-density (96 tpi, 1.2MB) floppy disk drive. Only one disk controller can be installed in the Series 3000 Intelligent Workstation.

Hard Disk Drive

One internal 5 1/4-inch form factor Winchester disk can be installed in the workstation. The smallest formatted capacity is 72MB. The maximum formatted capacity is 320MB. (The disk capacity is limited only by the state of 5 1/4-inch Winchester technology and will change as this technology progresses.) The interface protocol to these drives is either ST506/ST412 or ESDI, depending on the controller installed.

Cartridge Tape Drive

One cartridge tape drive and controller is part of the standard configuration. The tape drive is a DC-600A style streaming cartridge drive. The drive is a 5 1/4-inch half height form factor and has a formatted capacity of approximately

60MB. The format is QIC-24. The tape drive is used for software distribution and disk backup.

Power Supply

The power supply module provides DC power for the motherboard, the expansion boards, the disk drives, and the keyboard. The module is enclosed in a chassis near the rear of the unit. For more information on the power supply, see the chapter "Power Supply."

Expansion

The expansion features of the Series 3000 Intelligent Workstation include the following:

- Eight total slots (six 16-bit slots are AT compatible and two 8-bit slots are PC/XT compatible). One of the XT slots also has the 32-bit private memory bus connector.
- A dedicated 32-bit memory bus.
- Two half-height 5 1/4-inch peripheral bays (front access).
- One full height 5 1/4-inch peripheral bay (internal).

Options

The following options are available for the Series 3000 Intelligent Workstation:

- The Series 3000 Intelligent Workstation supports one fixed disk drive. Optional disk/controller pairs with various performance and capabilities can be chosen for the one fixed disk.
- Memory expansion to 16MB.
- An 80287/80387 math coprocessor.
- A PC Video Emulator (PVE) board for the Advanced Graphics Controller subsystem.
- An expansion board for one additional serial port and one additional parallel I/O port.

- An accessory package that allows the Series 3000 Intelligent Workstations's system unit to be mounted vertically beside a desk.
- An Ethernet expansion board.

Chapter 2. Motherboard

Introduction

The Series 3000 Intelligent Workstation's CPU hardware is contained on the motherboard — a multilayer printed circuit board that mounts flat on the bottom of the system unit. Figure 2-1 is a block diagram of the motherboard. Figure 2-2 is an illustration of the motherboard assembly.

The motherboard contains these components:

- 80386 microprocessor.
- 80287/80387 coprocessor (optional).
- 64KB of ROM.
- CHIPset Bus and Memory Controllers.
- Eight expansion slots (six 16-bit data slots and two 8-bit data slots). One of the 8-bit data slots contains the RAM memory (32-bit data, 24-bit address).
- Three programmable timers.
- 16 Interrupt Levels.
- Seven DMA Channels.
- Speaker connector.
- Keyboard controller.
- Clock/calendar with battery backup.

A group of jumpers, switches, and connectors facilitates the physical connection and electrical compatibility of the system. The power supply module in the system unit provides power for motherboard operation.

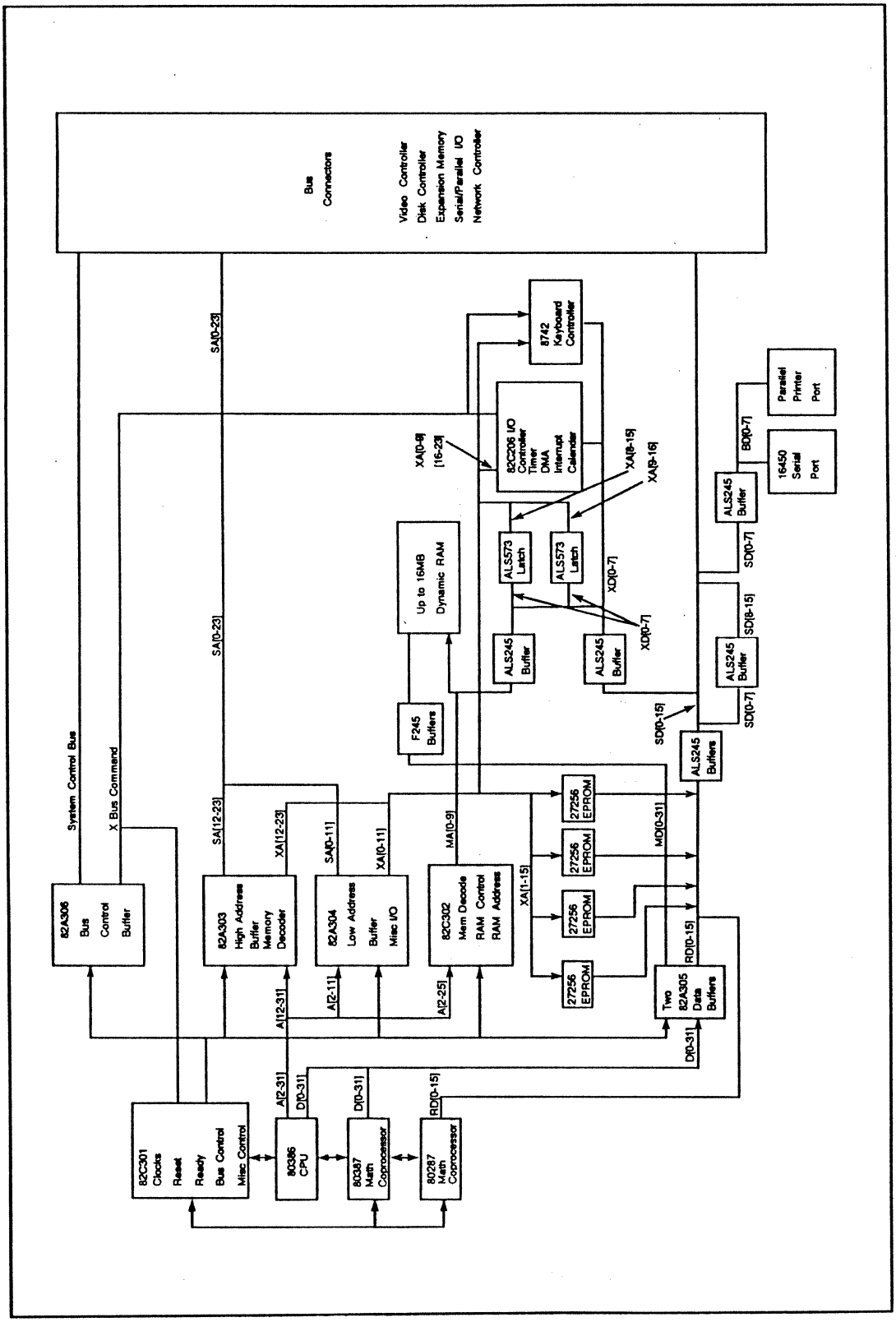

Figure 2-1. Motherboard Block Diagram

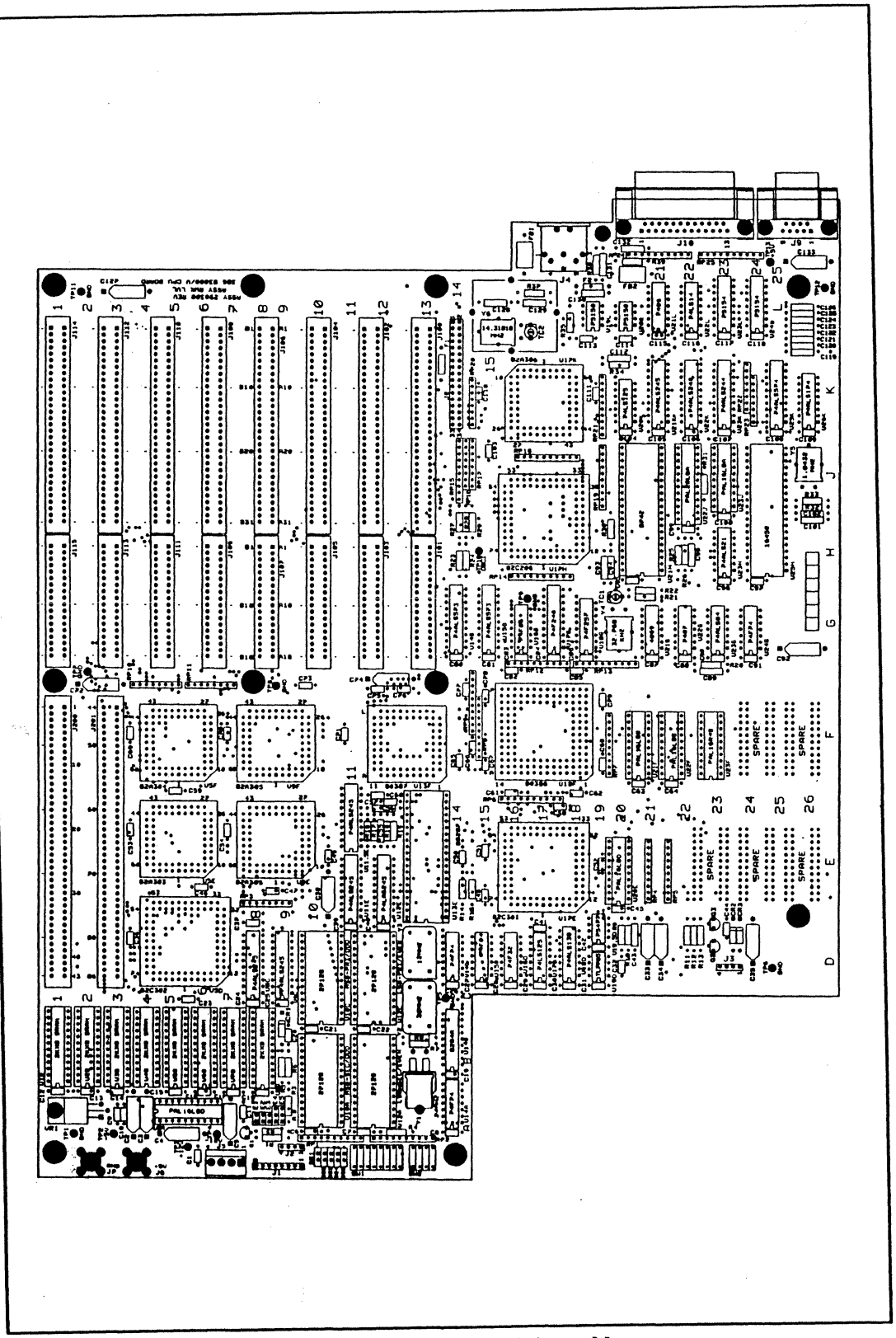

Figure 2-2. Motherboard Assembly

Microprocessor

The Series 3000 Intelligent Workstation's microprocessor operates at 16 MHz or 20 MHz.

- Technical information at 16 MHz

  The clock cycle is 62.5 nsec. A 32-bit RAM access requires two or three clock cycles (125 or 187.5 nsec). An EPROM access or off-board bus cycle requires ten clock cycles, including eight wait states or 625 nsec. Eight-bit bus operations, to 8-bit devices, take 16 clock cycles (including wait states). This results in a 1-microsecond processor cycle. Sixteen-bit bus operations to 8-bit devices take 28 clock cycles (including 26 wait states). This results in a 1.75 microsecond cycle time.

- Technical information at 20 MHz

  The clock cycle is 50 nsec. A 32-bit RAM access requires two or three clock cycles (100 or 150 nsec). An EPROM access or off-board bus cycle requires ten clock cycles including eight wait states or 500 nsec. Eight-bit bus operations to 8-bit devices take 16 clock cycles (including wait states). This results in a 800 nsec processor cycle. Sixteen-bit bus operations to 8-bit devices take 28 clock cycles (including 26 wait states). This results in a 1.4 microsecond cycle time.

Figure 2-3 lists the cycle time described above:

Item	20 MHz	16 MHz
Clock	20 MHz	16 MHz
Clock Cycle	50 nsec	62.5 nsec
Access Time	100 or 150 nsec	125 or 187.5 nsec
Bus Cycle	500 nsec	625 nsec
8-Bit Bus	800 nsec	1000 nsec
16-Bit Bus	1.400 msec	1.750 msec

Figure 2-3. Table of 80386 Cycle Times

The Series 3000 Intelligent Workstation uses the 80386 microprocessor instruction set, which is a superset of the 8086 microprocessor and 80286 microprocessor instruction sets. The Series 3000 Intelligent Workstation also

uses the instruction set for the Advanced Graphics Controller's 82786 graphics coprocessor.

There are five basic groups of instructions:

1. A Basic Instruction Set common to all Intel iAPX microprocessors. This includes instructions for logical and arithmetic operations, data movement, input/output, string manipulation, and control transfer.

2. An Extended Instruction Set that adds new instructions common to the 80186/80286, but not the 8086/8088. These instructions include block structured procedure entry and exit, parameter validation, and block I/O transfer instructions.

3. A System Control Instruction Set unique to the 80386. These instructions include control memory management and protection.

4. The optional 80287/80387 coprocessor instruction set provides fast comparison, arithmetic, and transcendental functions.

5. An instruction set of drawing and nondrawing, geometric, bit block transfer (bitblt), character block transfer (charblt), and register commands for the 82786 is included.

The 80386 microprocessor has 32-bit architecture, high-speed performance, and virtual memory support:

- There are eight 32-bit general registers for instruction operands, and addressing-mode variables.

- Physical address space can be up to 4 gigabytes.

- The Series 3000 Intelligent Workstation can support 16MB of memory. The minimum requirement is 1MB of memory (MS-DOS) or 4MB of memory (MAD/ix).

Numerics Coprocessor

The optional 80287/80387 numerics coprocessor works in parallel with the 80386 microprocessor. The optional 80287/80387 numerics coprocessor increases net processing speed by performing numeric functions while the 80386 microprocessor attends to other concurrent tasks.

The 80287/80387 numerics coprocessor recognizes three classes of numbers and seven numeric data types (See Figure 2-4).

Class	Data Type	Significant Decimal Digits	Bits Precision
Decimal Integers		18	80
Binary Integers	Word	4	16
	Short	9	32
	Long	19	64
Real Numbers	Short	6 or 7	32
	Long	15 or 16	64
	Temporary	19	80

Figure 2-4. Table of Data Types

The 80387 coprocessor adds 70 instructions to the 80386 microprocessor instruction set; the 80287 coprocessor adds 51; the 82786 graphics coprocessor on the Advanced Graphics Controller adds 40.

The eight 80-bit registers in the 80287/80387 numeric coprocessor are used to store constants and temporary results with up to 80-bit precision during calculations. These registers provide the same storage capacity as the forty 16-bit registers of the 80386 microprocessor.

The 80387 coprocessor operates at frequencies of 16 or 20 MHz. The 80287 coprocessor operates at 8 MHz. The microprocessor sends opcodes and operands to the coprocessor and receives results via I/O port addresses 0x0F8, 0x0FA, and 0x0FC. The coprocessor activates a BUSY signal when processing. Figure 2-5 lists the 80287/80387 port addresses.

Address	Direction	Function
0x000000F0	Write	Clear Busy Signal
0x000000F1	Write	Reset
0x800000F8	Write	OPCODE Write
0x800000F8	Read	CN or SW Read
0x800000FC	Read	Write Data
0x800000FC	Read	Read Data

Figure 2-5. 80287/80387 Numerics Coprocessor Port Addresses

Memory

The 80386 microprocessor's memory is divided into the following:

- Up to 4 ROM/EPROM modules
- Up to 16MB of RAM

The minimum system requirement is 1MB of memory for MS-DOS and 4MB of memory for MAD/ix.

Read Only Memory

The motherboard Read Only Memory (ROM) consists of

- Two 8-bit ROM/EPROM modules in a 16-bit arrangement
- Two expansion sockets

Odd and even addresses are stored in separate modules. ROM is assigned in duplicate at the top of the first and last 1MB of address space (0x000F0000 and 0xFFFF0000 for the standard ROM and 0x000E0000 and 0xFFFE0000 for the expansion ROM).

The ROM is not parity-checked and has an access time of 150 nsec. ROM/EPROM may also be located at the top of the first 16MB space; refer to the CS 8230 documentation for details. ROM/EPROM code can be moved into 32-bit shadow RAM for faster execution.

The system Basic Input Output System (BIOS) resides in ROM. An automatic self-test is performed by BIOS at power-up. Expansion devices are tested prior to boot-up.

BIOS supports the following I/O functions:

- Keyboard
- Floppy Disk
- Hard Disk
- Asynchronous Serial Port
- Parallel Port

- Display

For more information on BIOS, see the chapter "BIOS".

Random Access Memory

The chapter "Memory" describes the RAM memory board in detail. This section gives an overview of how RAM relates to the CPU.

Up to 16MB of RAM may be installed in the RAM memory board. This RAM starts at address 0x00000000 of the 16MB address space (see Figures 2-7 and 2-8). The memory board has a 4-bit DIP switch, which is used to enable memory (see Figure 2-6 and the chapter "Memory").

Between addresses 0x000A0000 and 0x000FFFFF, ROM code may be copied into shadow RAM. The RAM may then be write-protected and used in place of the ROM, resulting in much faster execution. Configuration registers inside the 82C302 memory controller are used to select the appropriate memory map.

Memory Board SW1 Bit				Board Status
1	2	3	4	
OFF	X	X	X	Disabled
ON	OFF	OFF	X	Enabled (Block 3)
ON	OFF	ON	X	Enabled (Block 2)
ON	ON	OFF	X	Enabled (Block 1)
ON	ON	ON	X	Enabled (Block 0)*

X = Don't Care

* = Factory Default Setting

Figure 2-6. RAM Address Spacing Enable

One refresh cycle is requested every 15 microseconds through the timer/counter (channel 1). On-board and I/O expansion RAM is initialized as follows:

- Initialize channel 1 of the timer/counter to the rate-generation mode with a period of 15 microseconds.
- Write to every memory location.

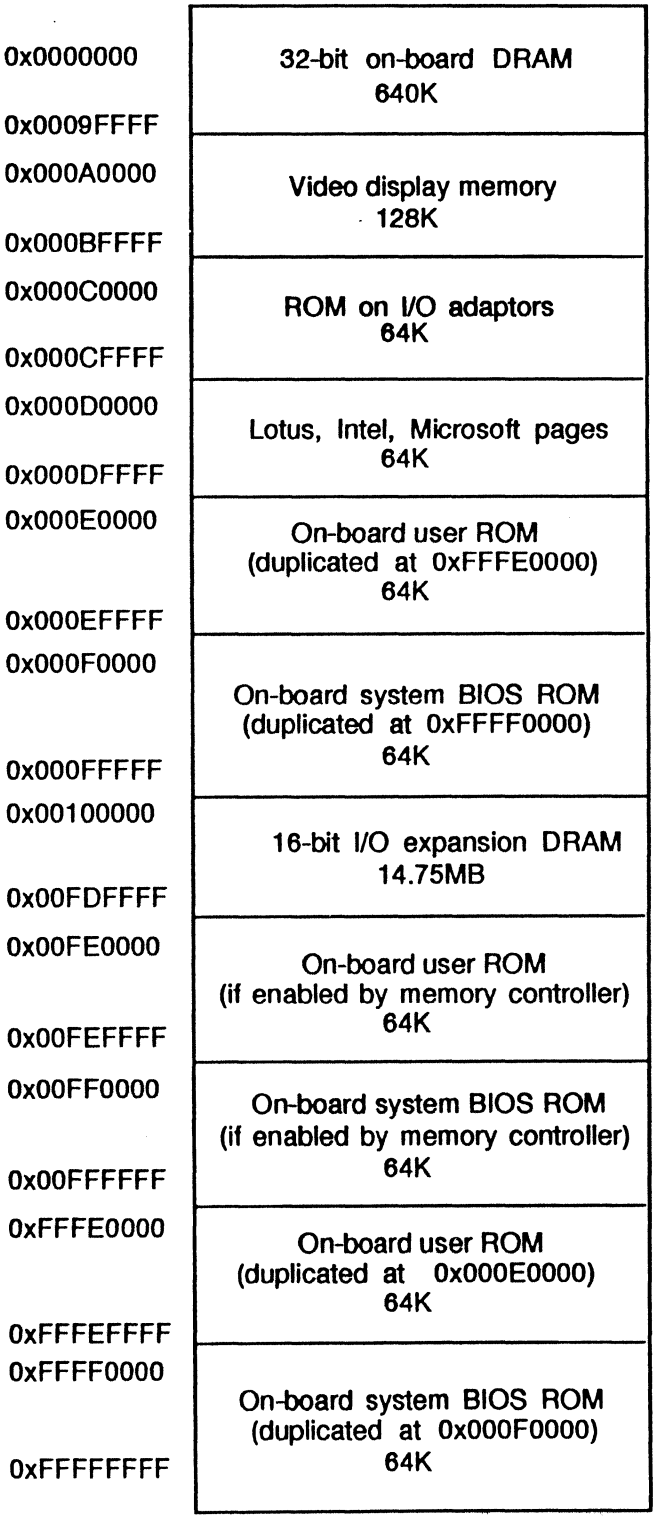

Figure 2-7. System Memory Map (1MB Systems)

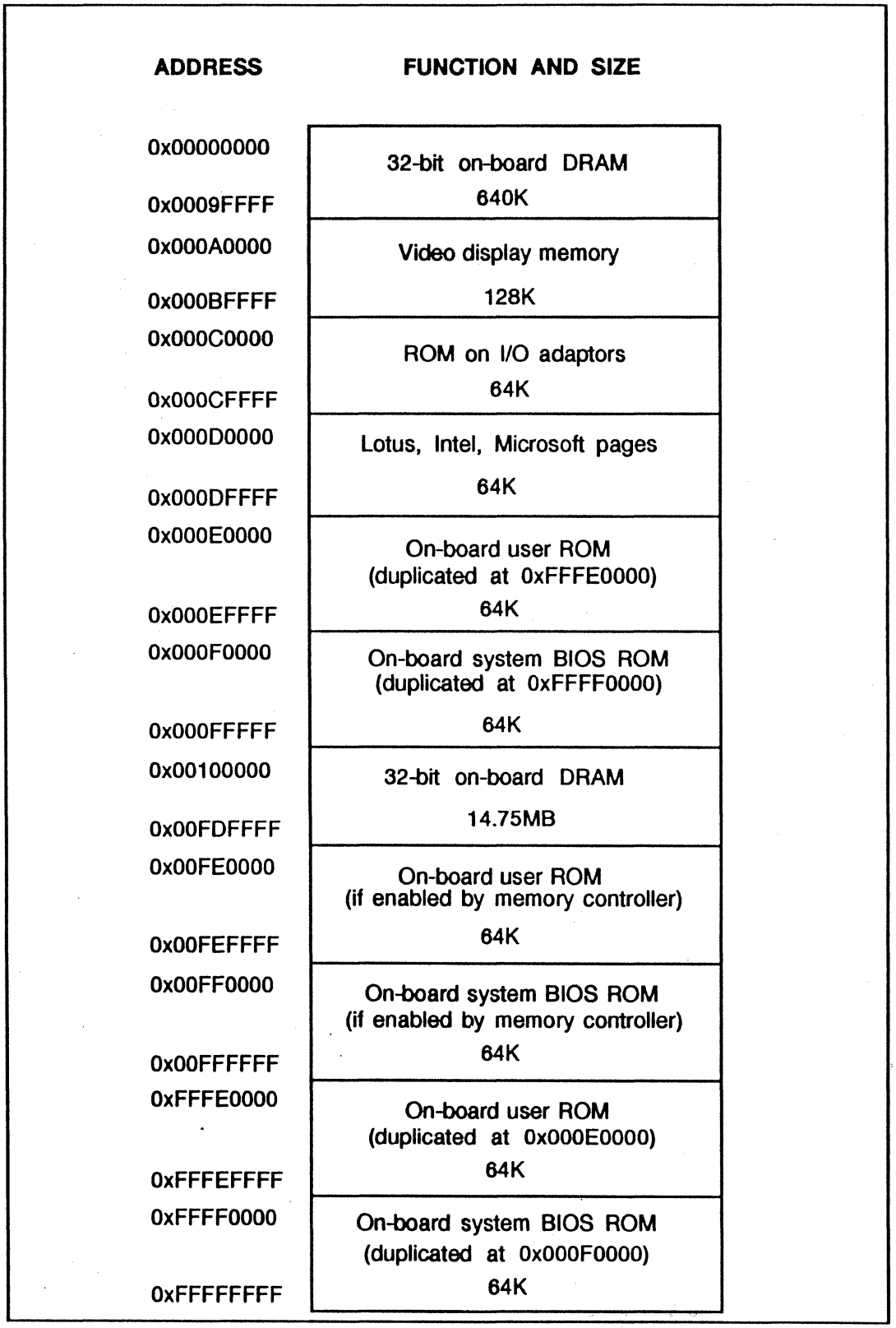

Figure 2-8. System Memory Map (16MB Systems)

CMOS RAM Configuration

The following sections describe the configuration bytes for the clock/calendar CMOS RAM. Addresses 0Eh through 33h (not including reserved addresses) are discussed.

Diagnostic Status Byte (0Eh)

Following are the bit definitions for the Diagnostic Status Byte.

Bit 7	Clock/calendar chip status power indicator 0 = Clock/calendar chip has not lost power. 1 = Clock/calendar chip has lost power.
Bit 6	Configuration-record checksum status indicator 0 = Checksum is good. 1 = Checksum is bad.
Bit 5	Configuration information status indicator 0 = Configuration information valid. 1 = Configuration information invalid.
Bit 4	Memory size miscompare 0 = Power-on check determined that memory size is same as in configuration. 1 = Memory-size miscompare.
Bit 3	Fixed disk adapter/drive initialization status 0 = Adapter and drive operating properly. System can attempt to boot-up. 1 = Adapter and/or drive failed initialization, preventing system boot-up.
Bit 2	Time status indicator (POST validity check) 0 = Time is valid. 1 = Time is invalid.
Bit 1-Bit 0	Reserved.

Shutdown Status Byte (0Fh)

Bits in this byte are defined by the power on diagnostics (POD). See the BIOS listing for details.

Floppy Disk Drive Type Byte (10h)

Following are the bit definitions for the Floppy Disk Drive Type Byte.

Bit 7-Bit 4 — Type of first floppy drive installed.
0000 = No drive present.
0001 = Double-sided disk drive (48 tpi).
0010 = High-density disk drive (96 tpi).
0011 - 1111 are reserved.

Bit 3-Bit 0 — Type of second floppy drive installed.
0000 = No drive present.
0001 = Double-sided disk drive (48 tpi).
0010 = High-density disk drive (96 tpi).
0011 - 1111 are reserved.

Address 11h

Address 11h is reserved.

Hard Disk Type 1 Through 14 (12h)

The Series 3000 Intelligent Workstation supports one internal hard disk. Disk drive types are described in Figure 2-9 or the BIOS listing at label hdtbl. In Figure 2-9 unlisted disk types are reserved. Drive types 1 through 14 are specified by a nibble located at address 12h. Drive types 16 through 63 are described by a byte located at address 19h. Following are the bit definitions for Hard Disk Type 1 through 14.

Bit 7-Bit 4 — Type (1-14) of hard disk.
0000 = No drive installed.
0001 - 1110 define types 1 through 14.
1111 = See address 19h for disk type.

Disk Type	No. of Cyl.	No. of Heads	Write Precomp	Landing Zone	MB	Sectors
1	306	4	0x128	305	10	17
2	615	4	0x300	615	20	17
3	615	6	0x300	615	30	17
4	940	8	0x512	940	62	17
5	940	6	0x512	940	46	17
6	615	4	0xFFFF	615	20	17
7	462	8	0x256	511	30	17
8	733	5	0xFFFF	733	30	17
9	900	15	0xFFFF	901	112	17
10	820	3	0xFFFF	820	20	17
11	855	5	0xFFFF	855	35	17
12	855	7	0xFFFF	855	49	17
13	306	8	0x128	319	20	17
14	733	7	0xFFFF	733	42	17
16	612	4	0x0	633	20	17
17	977	5	0x300	977	40	17
18	977	7	0xFFFF	977	56	17
19	1024	7	0x512	1023	59	17
20	733	5	0x300	732	30	17
21	733	7	0x300	732	42	17
22	733	5	0x300	733	30	17
23	306	4	0x0	336	10	17
25	615	4	0x0	615	20	17
26	1024	4	0xFFFF	1023	34	17
27	1024	5	0xFFFF	1023	42	17
28	1024	8	0xFFFF	1023	68	17
29	512	8	0x256	512	34	17
30	615	2	0x615	615	10	17
31	989	5	0x0	989	40	17
32	1020	15	0xFFFF	1024	127	17

Figure 2-9. BIOS Hard Disk Parameters (Part 1)

Disk Type	No. of Cyl.	No. of Heads	Write Precomp	Landing Zone	MB	Sectors
35	1024	9	0x1024	1024	76	17
36	1024	5	0x512	1024	42	17
37	830	10	0xFFFF	830	68	17
38	830	10	0xFFFF	830	107	34
39	1224	11	0xFFFF	1224	114	17
40	1224	15	0xFFFF	1224	312	34
41	917	15	0xFFFF	918	69	17
42	1632	8	0xFFFF	1632	333	51
43	1224	15	0xFFFF	1224	156	17
44	1216	12	0xFFFF	1216	248	34
45	1632	11	0xFFFF	1632	458	51
46	1632	15	0xFFFF	1632	624	51
47	1024	8	0xFFFF	1024	139	34

Figure 2-9. BIOS Hard Disk Parameters (Part 2)

Reserved and Equipment Byte (13h, 14h)

Following are the bit definitions for the Reserved and Equipment Byte.

Bit 7-Bit 6 — Number of floppy disk drives installed.
00 = 1 drive.
01 = 2 drives.
10 = Reserved.
11 = Reserved.

Bit 5-Bit 4 — Primary display installed.
00 = Enhanced display.
01 = Color/graphics monitor adapter (40-column).
10 = Color/graphics monitor adapter (80-column).
11 = Monochrome display and printer adapter.

Bit 3-Bit 2 — Not used.

Bit 1 — 80287/80387 coprocessor.
0 = Coprocessor not installed.
1 = Coprocessor installed.

Bit 0	Set condition indicates diskette drives installed.

Low and High Base Memory Bytes (15h,16h)

Following are the bit definitions for the Low and High Base Memory Bytes (15h and 16h).

Bit 7-Bit 0	Address 15h — Low-byte base size
Bit 7-Bit 0	Address 16h — High-byte base size Valid sizes: 0100h — 256KB motherboard RAM 0200h — 512KB motherboard RAM 0280h — 640KB (512KB motherboard RAM and 128KB memory expansion

Low and High Base Memory Bytes (17h, 18h)

Following are the bit definitions for the Low and High Base Memory Bytes (17h and 18h).

Bit 7-Bit 0	Address 17h — Low-byte expansion size
Bit 7-Bit 0	Address 18h — High-byte expansion size Valid sizes: 0200h — 512KB memory expansion 0400h — 1024KB memory expansion 0600h to 3C00h — 15360KB memory expansion

Hard Disk Type (19h)

Following are the bit definitions for the Hard Disk Type (19h).

Bit 7-Bit 0	Defines a disk type from 16 through 63. Types from 1 to 14 are defined at address 12h. Disk types are defined in Figure 2-66.

CMOS Checksum (2Eh, 2Fh)

Following are the bit definitions for the CMOS Checksum (2Eh and 2Fh). The checksum is at addresses 10h -2Dh.

Address 2Eh	High byte of checksum
Address 2Fh	Low byte of checksum.

Low and High Expansion Memory Bytes (30h, 31h)

Following are the bit definitions for the Low and High Expansion Memory Bytes (30h and 31h).

Bit 7-Bit 0	Address 30 — Low-byte expansion size
Bit 7-Bit 0	Address 31 — High-byte expansion size Valid sizes: 0200h — 512KB memory expansion 0400h — 1024KB memory expansion 0600h to 3C00h — 15360KB memory expansion

Note: This word reflects total expansion memory size as determined at power-on. Expansion memory size can be determined through interrupt 15 (refer to BIOS listing). Base memory size is determined at power-on time through system memory-size-determine interrupt.

Date Century Byte (32h)

Following are the bit definitions for the Date Century Byte (32h).

Bit 7-Bit 0	BCD value for century (BIOS interface to read and reset)

Information Flags (33h)

Following are the bit definitions for the Information Flags (33h).

Bit 7	Set if memory expansion card is installed.
Bit 6	Used by **setup** utility to output first user message after initial setup.
Bit 5-Bit 0	Reserved.

DMA Controller

The DMA controller operates at 4 MHz with a cycle time of 250 nsec. All DMA data transfer bus cycles are 1.25 microseconds. The DMA data transfer bus cycle is five clock cycles long. Cycles used to transfer bus control are not included.

DMA Channels

Seven DMA channels are supported by the 82C206. DMA channels 0, 1, 2, and 3 are used for 8-bit data transfers. Channels 5, 6, and 7 process 16-bit transfers. Channel 4 is used to cascade DMA controller 2 to DMA controller 1. Figure 2-10 shows DMA channel allocations. Figure 2-11 lists addresses for the page registers. Figure 2-12 is memory address construction for channels 3 through 0. Figure 2-13 is memory address construction for channels 7 through 5.

CTRL 1		CTRL 2	
Channel	Function	Channel	Function
0	Spare	4	Cascade
1	Spare		(CTLR 1)
2	Floppy	5	Spare
	(DSDD)	6	Spare
3	Spare	7	Spare

Figure 2-10. DMA Channel Allocations

Port Address	Direction	Function
0x080	R/W	Manufacturing Port
0x081	R/W	DMA Channel 2 Map
0x082	R/W	DMA Channel 3 Map
0x083	R/W	DMA Channel 1 Map
0x084	R/W	Unused
0x085	R/W	Unused
0x086	R/W	Unused
0x087	R/W	DMA Channel 0 Map
0x088	R/W	Unused
0x089	R/W	DMA Channel 6 Map
0x08A	R/W	DMA Channel 7 Map
0x08B	R/W	DMA Channel 5 Map
0x08C	R/W	Unused
0x08D	R/W	Unused
0x08E	R/W	Unused
0x08F	R/W	Refresh Map

Figure 2-11. DMA Page Register Port Addresses

Source	DMA Page Registers	DMA Controller 1
Address	A16h through A23h	A0h through A15h
Note: Addressing signal Byte High Enable (BHE) is generated by inverting address line A0h.		

Figure 2-12. Address Generation for DMA Channel 3 through 0

Source	DMA Page Registers	DMA Controller 2
Address	A17h through A23h	A1h through A16h
Note: Addressing signal Byte High Enable (BHE) and A0h are forced to logic 0.		

Figure 2-13. Address Generation for DMA Channel 7 through 5

DMA channel addresses cannot increase or decrease through page boundaries (64KB for channels 0 through 3 and 128KB for channels 5 through 7).

Programming the 8-Bit DMA Channels

DMA controller 1 contains channels 0 through 3. These channels support 8-bit data transfers between the 8-bit I/O adapters and the 8-bit or 16-bit memory. Each channel transfers data throughout the 16MB address space in 64KB blocks. Controller 1 is accessed by port addresses 0x000 through 0x01F. Figure 2-14 shows the controller 1 command codes.

Port Address	Direction	Function
0x000	R/W	Base and Current Address Channel 0
0x001	R/W	Base and Current Byte Channel 0
0x002	R/W	Base and Current Address Channel 1
0x003	R/W	Base and Current Byte Channel 1
0x004	R/W	Base and Current Address Channel 2
0x005	R/W	Base and Current Byte Channel 2
0x006	R/W	Base and Current Address Channel 3
0x007	R/W	Base and Current Byte Channel 3
0x008	R/W	Status Command
0x009	W	Request
0x00A	W	Single Mask Register
0x00B	W	Mode
0x00C	W	Clear Byte Pointer
0x00D	R/W	Read TEMP/MASTER Clear
0x00E	W	Clear Mask
0x00F	W	All Mask Register

Figure 2-14. DMA Controller 1 Port Addresses

Programming the 16-Bit DMA Channels

DMA controller 2 contains channels 4 through 7. Channel 4 is used to cascade to channels 0 through 3. Channels 5, 6, and 7 support 16-bit data transfers between 16-bit I/O adapters and 16-bit main memory. These DMA channels transfer data throughout the 16MB address space in 128KB blocks. Channels 5, 6, and 7 cannot transfer data on odd byte boundaries.

The 16-bit devices (I/O or memory) can only be accessed through DMA channels 5 through 7. Access to DMA controller 2 is through I/O addresses 0x0C0 through 0x0DF. Figure 2-15 lists command codes for this DMA controller.

Port Address	Direction	Function
0x0C0	R/W	Base and Current Address Channel 4
0x0C2	R/W	Base and Current Byte Channel 4
0x0C4	R/W	Base and Current Address Channel 5
0x0C6	R/W	Base and Current Byte Channel 5
0x0C8	R/W	Base and Current Address Channel 6
0x0CA	R/W	Base and Current Byte Channel 6
0x0CC	R/W	Base and Current Address Channel 7
0x0CE	R/W	Base and Current Byte Channel 7
0x0D0	R/W	Status Command
0x0D2	W	Request
0x0D4	W	Single Mask Register
0x0D6	W	Mode
0x0D8	W	Clear Byte Pointer
0x0DA	R/W	Read TEMP/MASTER Clear
0x0DC	W	Clear Mask
0x0DE	W	All Mask Register

Figure 2-15. DMA Controller 2 Port Addresses

All DMA memory transfers performed using channels 5 through 7 must occur on even byte boundaries. When the base address for these channels is programmed, the real address divided by 2 is the data written to the base address register. In addition, when the base word count for channels 5 through 7 is programmed, the count is the number of 16-bit words to be transferred. Therefore, DMA channels 5 through 7 can transfer 65,536 words (128KB maximum) for any selected page of memory.

These DMA channels divide the 16MB memory space into 128KB pages. When the DMA page registers for channels 5 through 7 are programmed, data bits D7 through D1 should contain the high-order seven-address bits (A23 through A17) of the desired memory space. Data bit D0 of the page registers for channels 5 through 7 is not used in the generation of the DMA memory address.

After power-up, all internal locations should be loaded with valid values even if some channels are unused. This is particularly true for the mode registers.

Timers/Counters

The motherboard has three timer/counter channels. The timer/counter channels are programmable and controlled by the 82C206. The three timer/counter channels are as follows:

- Channel 0
- Channel 1
- Channel 2

Figure 2-16 shows the function of the three channels. Figure 2-17 shows the 82C206 ports associated with the timer/counters.

Channel	Description
Channel 0	System Timer
GATE 0	TIED ON
CLK IN 0	1.190 MHz Oscillator
CLK OUT 0	IRQ 0 (54.9 microsecond period)
Channel 1	66.667 KHz Rate Generator
GATE 1	TIED ON
CLK IN 1	1.190 MHz Oscillator
CLK OUT 1	Request Refresh Cycle (1.5 microseconds)
Channel 2	Tone Generation for Speaker
GATE 2	Controlled by Bit 0 of Port 61
CLK IN 2	1.190 MHz Oscillator
CLK OUT 2	Used to Drive the Speaker (Programmable)

Figure 2-16. Programmable Interval Timer Channels

Port Address	Direction	Function
0x040	R/W	Counter 0 Data
0x041	R/W	Counter 1 Data
0x042	R/W	Counter 2 Data
0x043	R/W	Control Word

Figure 2-17. PIT Port Addresses

Interrupts

Sixteen levels of interrupts are provided by the microprocessor nonmaskable interrupt (NMI) and the 82C206. Although they are designated as nonmaskable, any or all interrupts can be masked. Figure 2-18 lists the interrupt level assignments in decreasing order of priority. Figures 2-19 and 2-20 list the Interrupt Controller Port addresses.

Level		Function
Micrprocessor NMI		Parity or I/O Channel Check
Interrupt Controller		
CTRL 1	**CTRL 2**	
IRQ0		Timer output 0
IRQ1		Keyboard (output buffer full)
IRQ2		Interrupt from CTLR B:
	IRQ8	Real-time clock interrupt
	IRQ9	Software redirected to INT OAH (IRQ2)
	IRQ10	Reserved
	IRQ11	Reserved
	IRQ12	Reserved
	IRQ13	Coprocessor
	IRQ14	Hard Disk Controller
	IRQ15	Reserved
IRQ3		Serial Port 2
IRQ4		Serial Port 1
IRQ5		Parallel Port 2 (Used as tape controller default on Series 3000)
IRQ6		Floppy Controller
IRQ7		Parallel Port 1

Figure 2-18. Interrupt Level Assignments

Port Address	Direction	Function
0x020	R/W	Status/Control
0x021	R/W	Status/Control

Figure 2-19. Master Interrupt Controller

Port Address	Direction	Function
0x0A0	R/W	Status/Control
0x0A1	R/W	Status/Control

Figure 2-20. Slave Interrupt Controller

VLSI Controllers

There are two VLSI Controllers:

- The 82C301 Bus Controller
- The 82C302 Memory Controller

The 82C301 Bus Controller and the 82C302 Memory Controller are discussed in the following sections. For further information on these components, refer to the Chips and Technologies CS 8230 CHIPSet documentation. The term AT Bus refers to the Series 3000 Intelligent Workstation bus that is functionally equivalent to the bus used in a PC/AT.

The 82C301 Bus Controller and 82C302 Memory Controller use internal registers for system configuration and diagnostics. These are accessed through I/O ports 22h and 23h. An indexing scheme is used to reduce the number of I/O addresses required to configure the chips. Each access (read or write) to an internal register is done by first writing its index into port 22h. This index controls the data accessible through port 23h and must be written even if the same data port is being accessed several times in a row.

Figure 2-21 illustrates the configuration register ports for the 82C301 Bus Controller and the 82C302 Memory Controller, which are discussed in the following sections.

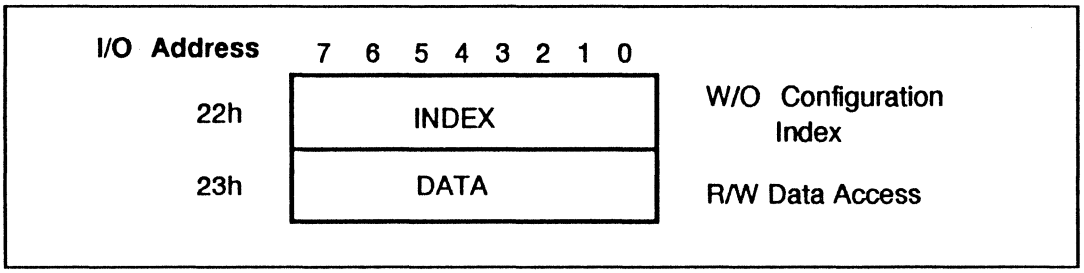

Figure 2-21. Configuration Register Access Ports

82C301 Bus Controller

The 82C301 Bus Controller provides clock generation for the AT-bus and the CPU. Controls are provided for AT-bus cycle timing and wait-state generation for I/O and memory accesses. The 82C301 Bus Controller interfaces directly with the 80386 microprocessor and implements the state machines

that control all bus accesses. The 82C301 Bus Controller also features a status register (port B).

Figure 2-22 illustrates the following 82C301 Bus Controller functions:

- Clock generation and reset control
- CPU-bus-access state machine
- AT-bus-access state machine
- Port B register and NMI logic
- Bus arbitration and refresh logic

Clock Generation and Reset Control

The 82C301 bus controller provides three major system clocks:

- The processor clock (CLK2)
- The AT-bus-access state machine clock (BCLK)
- The AT-bus clock (SYSCLK)

The BCLK (SYSCLK x 2) is internal to the 82C301 Bus Controller and is used to describe the system operation.

The clock generation circuitry uses two external clock sources:

- CLK2IN

  The frequency is 32 MHz (for 16 MHz systems) or 40 MHz (for 20 MHz systems).

- ATCLK1

  The frequency is 12 MHz (for 16 MHz systems) or 16MHz (for 20 MHz systems).

The clock-switching logic is guaranteed to provide a clean transition, with no phases shorter than the minimum or longer than the maximum values. This allows dynamic clock selection.

AT Bus Clock Selection

The 82C301 Bus Controller provides software-controlled clock selection for the AT-bus state machine. The clock can be synchronous to the CPU's CLK2 or unrelated, requiring synchronization between the AT-bus and CPU-bus state machines. While synchronization logic has been provided in all interface signals between the CPU and the AT-bus state machines, it is highly recommended that the AT-bus state machine clock (BCLK) be sourced for SCLK. An internal programmable divider has been provided, allowing BCLK frequency of CLK2/2 or CLK2/3. This eliminates the need for an additional oscillator. If the divide-by-3 option is selected, the resulting waveform will have approximately a 50% duty cycle.

The SYSCLK signal generated by the 82C301 Bus Controller is one half of the AT-bus state machine clock, BCLK. Since this clock is used to drive the AT bus, it is recommended that the divide ratio be set for a SYSCLK of about 6 or 8 MHz.

Figure 2-24 shows the combination of clock frequencies obtainable from CLK2IN with the AT Bus Clock selection scheme.

CLK2IN	SCLK	RATIO	BCLK	SYSCLK
24	12	/2	12	6
32	16	/2	16	8
40	20	/2	20	10
40	20	/3	13.3	6.7
48	24	/3	16	8

Figure 2-24. Examples of BCLK and SYSCLK

Reset Control

When RESET1 is asserted, the 82C301 bus controller asserts RESET3 and RESET4 for a system reset. For warm, non-extensive restart, RESET2 can be asserted to generate RESET3 for only the CPU and selected devices. RESET3 is also asserted when a CPU shut-down condition is detected. This feature allows register states to be maintained throughout the reset.

Processor Clock Selection

The CLK2 and SCLK signal can be selected from either of these sources (see Figure 2-23):

- External oscillator connected to CLK2IN
- AT-bus-access state machine clock BCLK

This selection is made with bit 4 of configuration register 4, which defaults to CLK2IN upon reset. If SCLK is selected as the source for BCLK, CLK2 must not be sourced from BCLK. In most cases, CLK2IN should match the rated CPU speed. BCLK can be a subdivision of CLK2IN or ATCLK1.

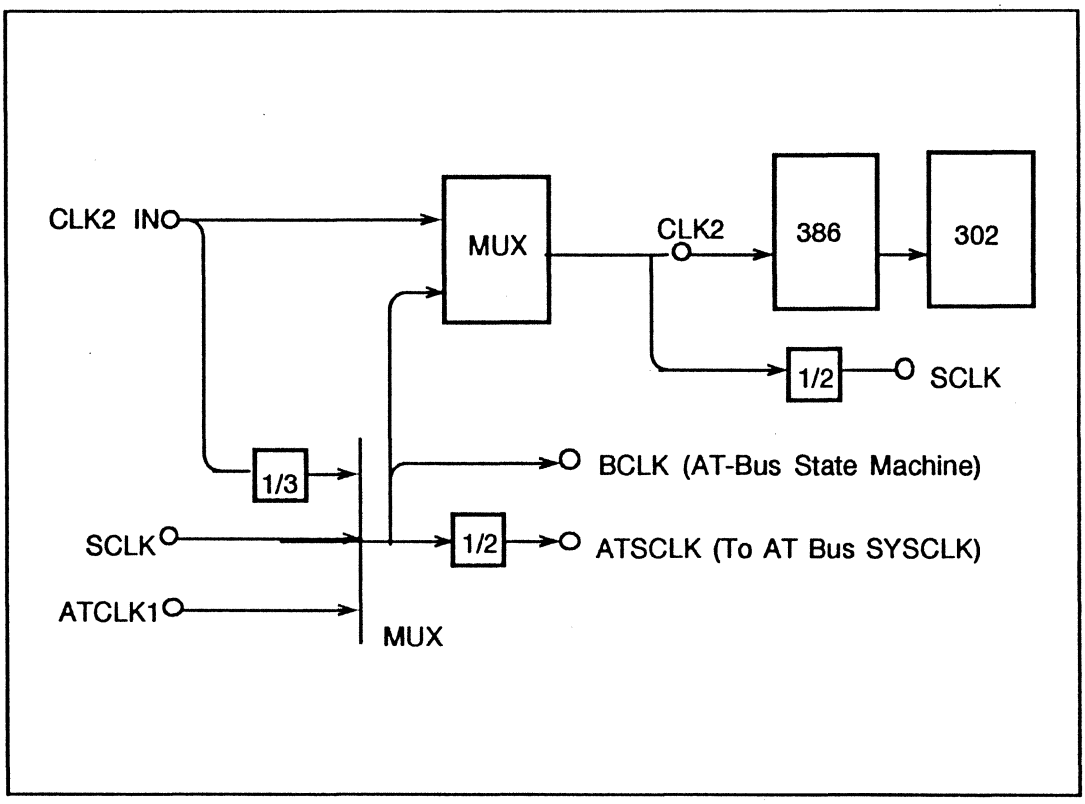

Figure 2-23. CLK2 and ATSCLK Clock Selection

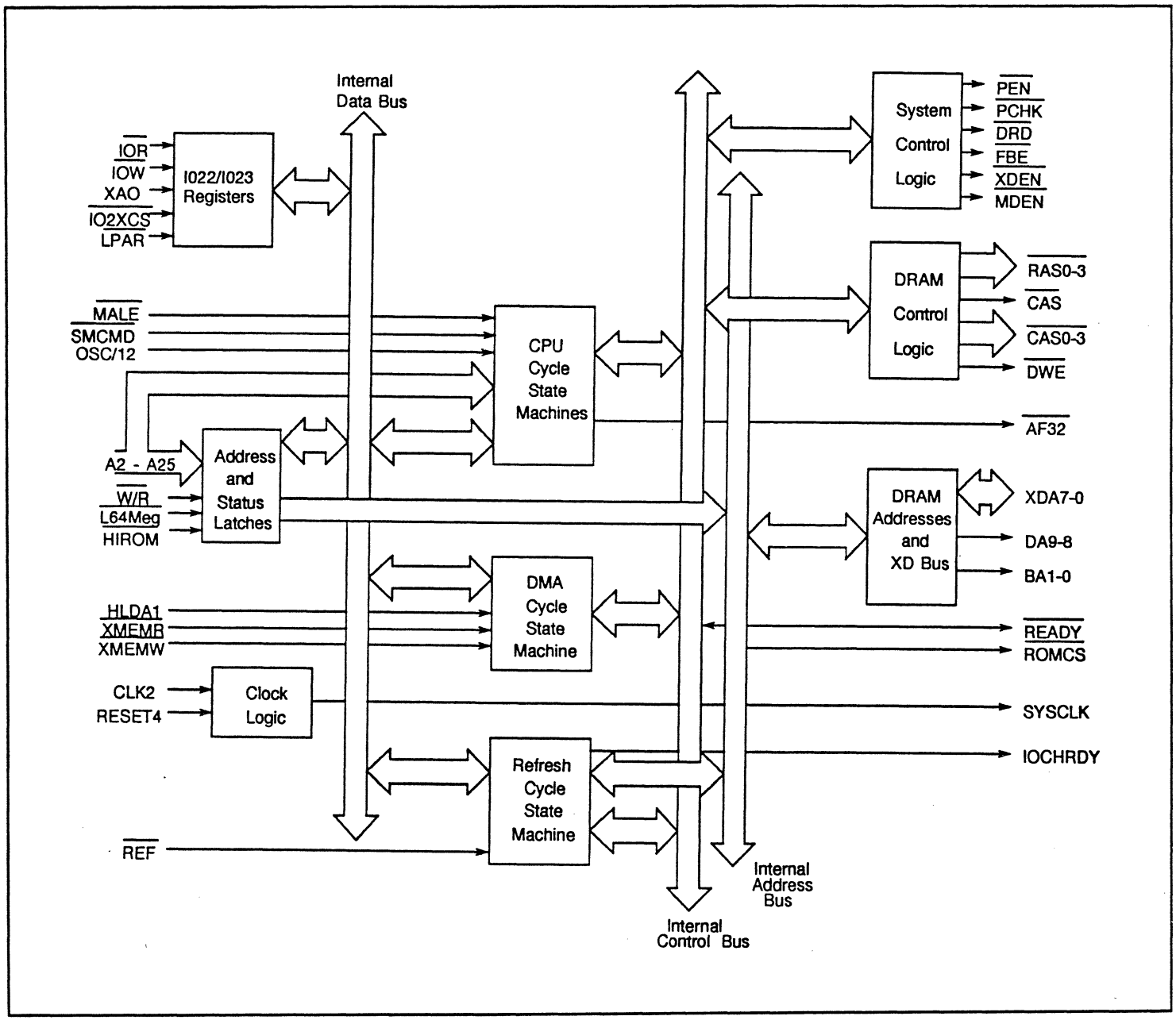

Figure 2-26. 82C302 Memory Controller Functional Block Diagram

Configuration Registers

Figure 2-25 shows the 3 bytes of configuration and diagnostic registers. The definitions for these registers are given in the section "I/O Mapping."

INDEX	7	6	5	4	3	2	1	0	
04h	VERS		—	PC	FE	TE	PF	TO	Version/Processor Clock/NMI sources
05h	M32		M16		M8		IO		Command Delay
06h	32 WS		16 WS		8 WS		B CLK		Wait State/Bus Clock

Figure 2-25. 82C301 Bus Controller Configuration Registers.

82C302 Memory Controller

The 82C302 Memory Controller performs memory control functions for page-mode access DRAM. The memory configurations can be one bank (noninterleaved) or multiple banks (2 or 4) interleaved on a 2KB-page basis.

Figure 2-26 illustrates the 82C302 Memory Controller's functions:

- DRAM memory access arbitration
- DRAM memory access cycle control
- DRAM refresh
- Memory mapping

gle-bank memory configuration upon reset and must be programmed to enable page-interleaved operation.

INDEX	7	6	5	4	3	2	1	0	
08h	0	VERS		MW	MR	HM	SM	NI	Identification
09h	R3	R2	R1	R0	D3	D2	D1	D0	ROM Configuration
0Ah	368K						256K		Memory Enable (16KB Resolution)
0Bh	496K						384K		
0Ch	624K						512K		•
0Dh	752K						640K		•
0Eh	880K						768K		•
0Fh	1008K						896K		Memory Enable (16KB Resolution)

Figure 2-27. Control and Address Space Map Registers

The register 09h controls address mapping and write protection for the low ROM area (C0000h to FFFFFh) in 64KB blocks. Registers 0Ah through 0Fh define each 16KB address range as a DRAM block in system memory, or an I/O port range.

DRAM Array Configuration and Timing

Figure 2-28 illustrates the DRAM configuration registers. Registers 10h to 13h provide the DRAM type definition and starting address for each pair of banks (0 and 1, or 2 and 3). Registers 10h (bits 6 and 7) and 12h (bits 6 and 7) define the following:

- Whether the DRAM is enabled
- If 256K DRAM is used
- If 1MB DRAM is used

These bits default to 256K DRAM upon reset.

Registers 10h (bits 0 through 5) and 12h (bits 0 through 6) define address bits (20 through 25) of the starting address of the pairs of banks. Some of these bits may not be valid because the memory banks must start at some pre-defined boundaries. For 256K DRAM, bits 20 through 25 are valid if only a

I/O Mapping

Configuration registers 08h to 0Fh define all CPU memory access as follows:

- ROM
- System DRAM
- Other local CPU bus
- I/O channel access

These provisions are made because the low 1MB is occupied by DRAM, ROM, and devices on the AT bus. For ROM accessses, it generates the ROMCS to control the PROM access; for system-memory accesses, it generates DRAM controls to the system memory under its control; for all other local CPU-bus accesses, it generates AF32 . It does not control I/O port accesses. Figure 2-27 illustrates the Control and Address space and map registers.

The 82C302 memory controller provides three 256KB areas where the ROM can be located:

- The low ROM space is located just below the 1MB address.
- The middle ROM space is located below the 16MB address.
- The high ROM space is below the 4 gigabyte address.

The low ROM is used for 8086-compatible operation; the middle ROM is used for the 80286 compatibility; the high ROM is used for the 80386 compatibility. Upon system reset, the default configuration register setting causes access to these three ROM areas to generate ROMCS. With the exception of the high ROM area (always recognized as ROM access), the other two ROM areas can be mapped to be either ROM or RAM accesses.

After reset, register 08h (bits 3 and 4) may be programmed to map the entire middle ROM area to DRAM, with write protection. Register 08h (bit 2) determines if the 82C301 Bus Controller recognizes the addresses generated beyond 16MB as local CPU-bus cycles. Register 08h (bit 1) enables registers 0Ah through 0Fh, which control the low 1MB DRAM (400000h to FFFFFh) address mapping for 256KB to 1MB addresses in 16KB blocks. Because this bit defaults upon reset, only the 0 to 256KB areas are accessible. The low 1MB DRAM can be accessed by enabling the mapping after the necessary configuration registers are programmed. Register 08h (bit 0) defaults to sin-

I/O Functions

The I/O bus accommodates the following functions:

- 100h to 3FFh address space
- 24-bit memory addresses (16MB of memory)
- 8-bit or 16-bit data access
- Direct memory access
- I/O wait state generation
- Interrupts
- Open bus structure, allowing multiple microprocessors to share system resources (including memory)
- Optional system memory refresh by I/O bus microprocessors

single-bank is enabled. This can be on any 1MB boundary. If multiple banks are enabled, they will have 2MB boundaries. For 1MB DRAM, only bits 23 through 25 are valid, forcing it on 8MB boundaries.

Register 11h (bit 7) and 13h (bit 7) define the RAS precharge time required when a page miss occurs so that DRAM of different speeds can be supported for each pair of banks. Register 11h (bit 6) and 13h (bit 6) define the wait state to be inserted to meet the DRAM speed. These parameters default to the slower timing upon reset so that the system can be powered up with minimal assumptions on the DRAM speed and the memory configuration.

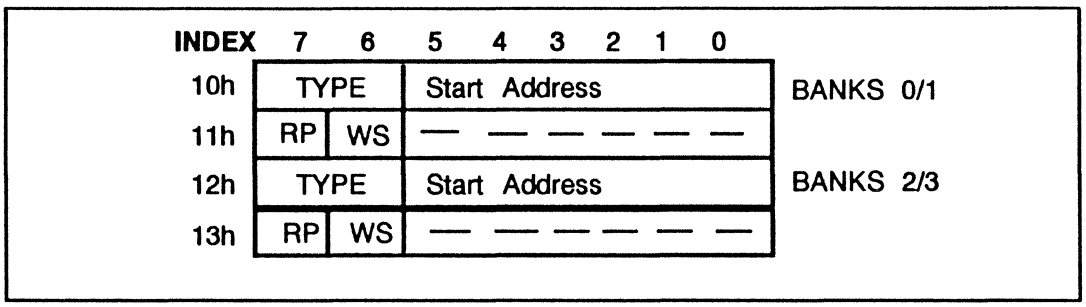

Figure 2-28. DRAM Configuration/Timing Register Summary

- SD0 through SD15 (I/O)

  SD0 through SD15 are microprocessor, memory, or I/O device data lines. D15 is the most significant bit. The 16-bit devices on the I/O bus use D0 through D15 to communicate with the microprocessor. The 8-bit devices can only use D0 through D7. A 16-bit microprocessor transfer to an 8-bit device is done by consecutive 8-bit transfers; data on D8 through D15 are gated to D0 through D7.

- BALE (O)

  Buffered Address Latch Enable (BALE) is used on the motherboard to latch valid address and memory decodes from the microprocessor. The signal, which comes from the 82A306 control bus buffer, is available to the I/O bus to indicate (along with Address Enable) a valid microprocessor or DMA address. Microprocessor addresses SA0 through SA19 are latched by the falling edge of BALE. During a DMA cycle, BALE is forced high.

- I/O CH CK* (I)

  This signal (I/O channel check) provides the motherboard with parity information about memory or devices on the I/O bus. When active (low), the signal indicates an uncorrectable error.

- SMEMR* (O) and MEMR* (I/O)

  These signals tell memory to output data to the bus. SMEMR* is active (low) only if memory decode is in the first 1MB of memory space. MEMR* is active (low) on all bus memory cycles and can be driven by any microprocesssor or DMA controller. SMEMR* is derived from MEMR* and the decode of the low 1MB of memory. If an I/O bus microprocessor wishes to drive MEMR* active, its address lines must be valid on the bus for one system clock period before doing so.

- SMEMW* (O) and MEMW* (I/O)

  These signals instruct memory to input data from the bus. The signal SMEMW* is active (low) only if memory decode is in the first 1MB of memory space. It is derived from MEMW* and the decode of the low 1MB of memory. On all bus memory cycles, MEMW* is active (low), and can be driven by any microprocessor or DMA controller. If an I/O bus

Signal Definitions

The pin functions of I/O connectors J100 through J115 are described in the sections that follow. Active low signals are indicated by an asterisk, as in SMEMR*.

- SA0 through SA19 (I/O)

  Address bits 0 through 19 are used for memory and I/O devices connected to the I/O bus. These 20 address lines, in addition to SA20 through SA23, allow access to 16MB of memory. When Buffered Address Latch Enable (BALE) is high, SA0 through SA19 are gated on the system bus and are latched on the falling edge of BALE. The addresses are generated by the microprocessor or by the DMA controller. They also can be driven by other microprocessors or DMA controllers that reside on the I/O bus.

- SA17 through SA23 (I/O)

  Address lines 17 through 23 can be driven by DMA controllers or I/O-bus-resident microprocessors. The lines are active if Buffered Address Latch Enable (BALE) is high. Because SA17 through SA23 are not latched during the microprocessor cycles, they do not stay valid for a whole cycle. Their purpose is to generate memory decodes for single-wait-state memory cycles; the decodes should be latched by I/O adapters, at the falling edge of BALE.

- SYSCLK (O)

  The system clock (see Figure 2-23), which can be programmed to one of several frequencies, should be used only for synchronization and not as a reference frequency. An external oscillator module and configuration registers inside the 82C301 bus controller are used to set the SYSCLK frequency.

- RESET DRV (O)

  Reset drive is used to reset and initialize the system at power-up (or if power returns after a failure).

- MASTER* (I)

  This active-low signal allows an I/O bus microprocessor to gain control of the system. First, an I/O bus device (DMA controller or microprocessor) issues a DRQ to a DMA channel and receives a DMA acknowledge (DACK0* to DACK7*). After receiving the DMA acknowledge, an I/O microprocessor can take control of the 3-state system bus by sending MASTER*. After MASTER* becomes active, the I/O processor must wait one system clock cycle to drive address or data lines, or two cycles to issue a Read or Write command.

- MEM CS16* (I)

  When active (low), this chip-select line tells the motherboard that the current data transfer is 16-bits, in a 1-wait-state memory cycle. The signal is derived by decoding SA17 through SA23. An open collector or three-state device that can sink up to 20 mA should be used to drive MEM CS16*.

- I/O CS16* (I)

  When active (low), this chip-select line tells the motherboard that the current data transfer is 16-bits, in a 1 wait-state I/O cycle. The signal is derived by decoding SA0 through SA9. An open collector or a 3-state device that can sink up to 20 mA should be used to drive I/OCS16* .

- OSC (O)

  This 14.31818 MHz clock has a 50% duty cycle and is not synchronous with the system clock.

- 0WS* (I)

  This Zero Wait State (active-low) signal tells the microprocessor to finish the present bus cycle without inserting any more wait cycles. To run a memory cycle to a 16-bit device (no wait states), 0WS* is derived from the address decode and a Read or Write command. To run a memory cycle to an 8-bit device (minimum two wait states), 0WS* should be driven one system clock after the Read or Write command (gated by the device's address decode) is active. Memory Read and Write commands to an 8-bit device are active at the system clock's falling edge. An open collector or a 3-state device that can sink up to 20 mA should be used to drive 0WS*

microprocessor wishes to drive MEMW* active, its address lines must be valid on the bus for one system clock period before doing so.

- DRQ0 through DRQ3, DRQ5 through DRQ7 (I)

  These signals (DMA requests) are asynchronous channel requests by peripheral devices or I/O bus microprocessors for DMA service or control of the system. The highest priority is DRQ0. The lowest priority is DRQ7. A request is generated if a DRQ line becomes active (high) and stays active until the corresponding DMA request acknowledge line (DACK) becomes active. The 8-bit DMA transfers are allowed by DRQ0 through DRQ3. Terms DRQ5 through DRQ7 allow 16-bit transfers. DRQ4 is reserved.

- DACK0* through DACK3*, DACK5* through DACK7* (O)

  These active-low signals acknowledge DMA requests DRQ0 through DRQ3 and DRQ5 through DRQ7.

- AEN (O)

  When the address enable (AEN) line is active, the DMA controller controls the address bus and the data bus Read and Write lines to memory and I/O. All other devices are isolated from the I/O bus by AEN to allow DMA transfers.

- REFRESH* (I/O)

  This active-low signal indicates a refresh cycle and can be driven by an I/O bus microprocessor.

- T/C (O)

  When the terminal count for any DMA channel is reached, T/C pulses high.

- SBHE* (I/O)

  System Bus High Enable (active-low) indicates a transfer of data on the upper byte of the data bus, SD8 through SD15. 16-bit devices use SBHE* to condition data bus buffers tied to SD8 through SD15.

Port Address (hex)	Function
0000-000F	82C206 8-bit DMA Controller 1
0020-0021	82C206 Master Interrupt Controller 1
0022-0023	CS8230 Configuration Register
0040-0043	82C206 Programmable Interval Timer
0060-0064	8742 Universal Peripheral Interface 8-bit Microcomputer
0061	TTL I/O Status and Control Port
0070	NMI ENABLE/82C206 Calendar Address Port
0071	82C206 Calendar Data Port
0080-008F	82C206 DMA Page Register Port
00A0-00A1	82C206 Slave Interrupt Controller
00C0-00DF	82C206 16-bit DMA Controller
00F0	Math Coprocessor Clear Bus
00F1	Math Coprocessor Reset
800000F8-800000FF	Math Coprocessor Opcodes and Operands
0100-03FF	Off-Board I/O
0278-027F	LPT2 Parallel Port (SW2 Selects Port)
02F8-02FF	COM2 Serial Port (SW2 Selects Port)
0378-037F	LPT1 Parallel Port (SW2 Selects Port)
03F8-03FF	COM1 Serial Port (SW2 Selects Port)

Figure 2-29. System I/O Address Map (Summary)

I/O Address Map

Figures 2-29 through 2-64 are organized numerically by port address. They describe the I/O addresses, including configuration register details for the 82C301 Bus Controller and 82C302 Memory Controller.

The term 8230 indicates both the 82C301 Bus Controller and the 82C302 Memory Controller. To access an 82C301 Bus Controller or 82C302 Memory Controller configuration register, first write its index to I/O address 0022h. After doing so, you can read from or write to the indexed register at I/O address 0023h (see Figure 2-40). The index must be written before each access.

Figures 2-42 through 2-44 describe the data byte in each 82C301 bus controller configuration register. Before writing to or reading from the register at I/O address 0023h, its index must first be written to I/O address 0022h.

Figures 2-45 through 2-58 describe the data byte in each 82C302 memory controller configuration register. Before writing to or reading from the register at I/O address 0023h, its index must first be written to I/O address 0022h.

Bit	Direction	Function
7,6	R	Version Number
5		Reserved
4	R/W	Processor Clock Select 0 = Use CLK2 Oscillator Input 1 = Use AT Bus State Machine Clock
3	R/W	0 = Power Fail NMI Disabled 1 = Power Fail NMI Enabled
2	R/W	0 = Ready Timeout NMI Disabled 1 = Ready Timeout NMI Enabled
1	R	0 = Power Fail Not Active During NMI 1 = Power Fail Active During NMI
0	R	0 = No Ready Timeout 1 = Ready Timeout

Figure 2-33. Index 04h (Version, Processor Clock, NMI Sources)

Bit	Direction	Function
7,6	R/W	AT-Bus 32-bit Memory Command Delay
5,4	R/W	AT-Bus 16-bit Memory Command Delay
3,2	R/W	AT-Bus 8-bit Memory Command Delay
1,0	R/W	AT-Bus I/O Command Delay 0 = 0 BCLK Cycle Delay 1 = 1 BCLK Cycle Delay 2 = 2 BCLK Cycle Delay 3 = 3 BCLK Cycle Delay

Figure 2-34. Index 05h (Command Delay Select)

Port Address	Direction	Function
0x000	R/W	Base and Current Address Channel 0
0x001	R/W	Base and Current Byte Channel 0
0x002	R/W	Base and Current Address Channel 1
0x003	R/W	Base and Current Byte Channel 1
0x004	R/W	Base and Current Address Channel 2
0x005	R/W	Base and Current Byte Channel 2
0x006	R/W	Base and Current Address Channel 3
0x007	R/W	Base and Current Byte Channel 3
0x008	R/W	Status Command
0x009	W	Request
0x00A	W	Single Mask Register
0x00B	W	Mode
0x00C	W	Clear Byte Pointer
0x00D	R/W	Read TEMP/MASTER Clear
0x00E	W	Clear Mask
0x00F	W	All Mask Register

Figure 2-30. 82C206 (Byte DMA 1)

Port Address	Direction	Function
0x020	R/W	Status/Control
0x021	R/W	Status/Control

Figure 2-31. 82C206 (Master Interrupt Controller 1)

Port Address	Direction	Function
0x022	W/O	Index Register
0x023	R/W	Configuration Data

Figure 2-32. CS 8230 Configuration Ports

Bit	Direction	Function
7	R	Controller Type (82C302 = Non-Cache Interleaved Controller)
6,5	R	Version
4	R/W	Middle Boot Space Write Protect 0 = Read/Write 256K RAM at FC0000h 1 = Read Only 256K RAM at 00FC0000h
3	R/W	Middle Boot RAM Disabled 0 = Boot RAM Just Below 16MB Enabled 1 = Boot RAM Just Below 16MB Disabled
2	R/W	16MB I/O Channel Memory Limit 0 = AF32 Not Asserted For Addresses >= 16MB 1 = AF32 Asserted for Addresses >= 16MB
1	R/W	Minimum Memory After Reset 0 = 256K Only Enabled 1 = Normal Configuration
0	R/W	Single Bank/Interleave Select: 0 = Disable Interleave (Single Bank) 1 = Enable Interleave

Figure 2-36. Index 08h (Identification)

Bit	Direction	Function
7,6	R/W	AT-Bus 32-bit Wait Select State 0 = 0 System Clock Cycle Wait 1 = 1 System Clock Cycle Wait 2 = 2 System Clock Cycle Wait 3 = 3 System Clock Cycle Wait
5,4	R/W	AT-Bus 16-bit Wait Select State 0 = 0 System Clock Cycle Wait 1 = 1 System Clock Cycle Wait 2 = 2 System Clock Cycle Wait 3 = 3 System Clock Cycle Wait
3,2	R/W	AT-Bus 8-bit Wait Select State 0 = 0 System Clock Cycle Wait 1 = 1 System Clock Cycle Wait 2 = 2 System Clock Cycle Wait 3 = 3 System Clock Cycle Wait
1,0	R/W	AT-BusClock Source Select 0 = Use CLK2/3 For AT-Bus Clock 1 = Use CLK2/2 For AT-Bus Clock 2 = Reserved 3 = Use ATCLK Oscillator

Figure 2-35. Index 06h (Wait State and Bus Clock Select)

Bit	Direction	Function
7	R/W	Address Map for 5C000h - 5FFFFh
6	R/W	Address Map for 58000h - 5BFFFh
5	R/W	Address Map for 54000h - 57FFFh
4	R/W	Address Map for 50000h - 53FFFh
3	R/W	Address Map for 4C000h - 4FFFFh
2	R/W	Address Map for 48000h - 4BFFFh
1	R/W	Address Map for 44000h - 47FFFh
0	R/W	Address Map for 40000h - 43FFFh
		0 = Address is in main memory 1 = Address is on the AT I/O channel

Figure 2-38. Index 0Ah (Address Map for 040000h - 05FFFFh)

Bit	Direction	Function
7	R/W	Address Map for 7C000h - 7FFFFh
6	R/W	Address Map for 78000h - 7BFFFh
5	R/W	Address Map for 74000h - 77FFFh
4	R/W	Address Map for 70000h - 73FFFh
3	R/W	Address Map for 6C000h - 6FFFFh
2	R/W	Address Map for 68000h - 6BFFFh
1	R/W	Address Map for 64000h - 67FFFh
0	R/W	Address Map for 60000h - 63FFFh
		0 = Address is in main memory 1 = Address is on the AT I/O channel

Figure 2-39. Index 0Bh (Address Map for 060000h - 07FFFFh)

Bit	Direction	Function
7	R/W	RAM Write Protect at C0000h-CFFFFh 0 = Read/Write 1 = Read Only
6	R/W	RAM Write Protect at D0000h-DFFFFh 0 = Read/Write 1 = Read Only
5	R/W	RAM Write Protect at E0000h-EFFFFh 0 = Read/Write 1 = Read Only
4	R/W	RAM Write Protect at F0000h-FFFFFh 0 = Read/Write 1 = Read Only
3	R/W	On-Board ROM Enable at C0000h-CFFFFh 0 = Main Memory or I/O Bus 1 = On-Board ROM
2	R/W	On-Board ROM Enable at D0000h-DFFFFh 0 = Main Memory or I/O Bus 1 = On-Board ROM
1	R/W	On-Board ROM Enable at E0000h-EFFFFh 0 = Main Memory or I/O Bus 1 = On-Board ROM
0	R/W	On-Board ROM Enable at F0000h-FFFFFh 0 = Main Memory or I/O Bus 1 = On-Board ROM

Figure 2-37. Index 09h (RAM/ROM Configuration in Boot Area)

Bit	Direction	Function
7	R/W	Address Map for DC000h - DFFFFh
6	R/W	Address Map for D8000h - DBFFFh
5	R/W	Address Map for D4000h - D7FFFh
4	R/W	Address Map for D0000h - D3FFFh
3	R/W	Address Map for CC000h - CFFFFh
2	R/W	Address Map for C8000h - CBFFFh
1	R/W	Address Map for C4000h - C7FFFh
0	R/W	Address Map for C0000h - C3FFFh
		0 = Address is in main memory 1 = Address is on the AT I/O channel

Figure 2-42. Index 0Eh (Address Map for 0C0000h - 0DFFFFh)

Bit	Direction	Function
7	R/W	Address Map for FC000h - FFFFFh
6	R/W	Address Map for F8000h - FBFFFh
5	R/W	Address Map for F4000h - F7FFFh
4	R/W	Address Map for F0000h - F3FFFh
3	R/W	Address Map for EC000h - EFFFFh
2	R/W	Address Map for E8000h - EBFFFh
1	R/W	Address Map for E4000h - E7FFFh
0	R/W	Address Map for E0000h - E3FFFh
		0 = Address is in main memory 1 = Address is on the AT I/O channel

Figure 2-43. Index 0Fh (Address Map for 0E0000h - 0FFFFFh)

Bit	Direction	Function
7	R/W	Address Map for 9C000h - 9FFFFh
6	R/W	Address Map for 98000h - 9BFFFh
5	R/W	Address Map for 94000h - 97FFFh
4	R/W	Address Map for 90000h - 93FFFh
3	R/W	Address Map for 8C000h - 8FFFFh
2	R/W	Address Map for 88000h - 8BFFFh
1	R/W	Address Map for 84000h - 87FFFh
0	R/W	Address Map for 80000h - 83FFFh
		0 = Address is in main memory 1 = Address is on the AT I/O channel

Figure 2-40. Index 0Ch (Address Map for 080000h - 09FFFFh)

Bit	Direction	Function
7	R/W	Address Map for BC000h - BFFFFh
6	R/W	Address Map for B8000h - BBFFFh
5	R/W	Address Map for B4000h - B7FFFh
4	R/W	Address Map for B0000h - B3FFFh
3	R/W	Address Map for AC000h - AFFFFh
2	R/W	Address Map for A8000h - ABFFFh
1	R/W	Address Map for A4000h - A7FFFh
0	R/W	Address Map for A0000h - A3FFFh
		0 = Address is in main memory 1 = Address is on the AT I/O channel

Figure 2-41. Index 0Dh (Address Map for 0A0000h - 0BFFFFh)

Bit	Direction	Function
7	R/W	DRAM RAS Precharge 0 = 3 CLK2 Times (93 nsec at 16 MHz) (75 nsec at 20 MHz) 1 = 5 CLK2 Times (155 nsec at 16 MHz) (125 nsec at 20 MHz)
6	R/W	DRAM Wait States 0 = 0 Wait State 1 = 1 Wait State
5 - 0		Reserved

Figure 2-47. Index 13h (Bank 2 and 3 Timing)

Bit	Direction	Function
7	R/W	Parity Check Disable: 0 = Parity Enabled 1 = Parity Disabled
6-2		Reserved
1-0	R	High Parity Error Address Bits 23-16

Figure 2-48. Index 28h (Parity)

Bit	Direction	Function
7-0	R	Parity Error Address Bits 23 - 16

Figure 2-49. Index 29h (Parity)

Bit	Direction	Function
7,6	R/W	DRAM Type 0 = None (Bank Disabled) 1 = 256K RAM 2 = 1MB RAM 3 = Reserved
5,0	R/W	Starting Address 25 - 20

Figure 2-44. Index 10h (Bank 0 and 1 Type and Start Address)

Bit	Direction	Function
7	R/W	DRAM RAS Precharge 0 = 3 CLK2 Times (93 nsec at 16 MHz) (75 nsec at 20 MHz) 1 = 5 CLK2 Times (155 nsec at 16 MHz) (125 nsec at 20 MHz)
6	R/W	DRAM Wait States 0 = 0 Wait State 1 = 1 Wait State
5 - 0		Reserved

Figure 2-45. Index 11h (Bank 0 and 1 Timing)

Bit	Direction	Function
7,6	R/W	DRAM Type 0 = None (Bank Disabled) 1 = 256K RAM 2 = 1MB RAM 3 = Reserved
5,0	R/W	Starting Address 25 - 20

Figure 2-46. Index 12h (Bank 2 and 3 Type and Start Address)

Bit	Direction	Function
P10		Unused
P11		Unused
P12	Input	Reserved
P13		Unused
P14		Unused
P15		Unused
P16	Input	Monochrome/Color Switch
P17	Input	Keyboard Inhibit
P20	Output	COU Reset (Reset 2)
P21	Output	A20 Gate
P22		Unused
P23		Unused
P24	Output	Keyboard Inhibit
P25		Unused
P26	Output	Keyboard Clock
P27	Output	Keyboard Data
TEST0		Keyboard Clock
TEST1		Keyboard Data

Figure 2-52. 8742 I/O Bits

Address	Direction	Function
0x0061	R/W	Bit 0 = TMR2 Gate For Speaker
	R/W	Bit 1 = SPKRDATA
	R/W	Bit 2 = PARENS (On-Board Parity Enable)
	R/W	Bit 3 = IOCKENA (Bus Error Enable)
	R	Bit 4 = Refresh Detect
	R	Bit 5 = TMROUT2 (Speaker Clock)
	R	Bit 6 = IOCHCK (Bus Error)
	R	Bit 7 = PERERR (On-Board Parity Error)

Figure 2-53. 82C301 TTL I/O Status and Control

Address	Direction	Function
0x0040	R/W	Counter 0 Data
0x0041	R/W	Counter 1 Data
0x0042	R/W	Counter 2 Data
0x0043	W	Control Word

Figure 2-50. 82C206 Programmable Interval Timer

Address	Direction	Function
0x0060	R/W	Data
0x0064	R/W	Command

Figure 2-51. 8742 8-Bit Microcomputer

Address	Description
0x00	Seconds
0x01	Seconds Alarm
0x02	Minutes
0x03	Minutes Alarm
0x04	Hours
0x05	Hours Alarm
0x06	Day Of Week
0x07	Date of Month
0x08	Month
0x09	Year
0x0A	Status Register A
0x0B	Status Register B
0x0C	Status Register C
0x0D	Status Register D
0x0E	Diagnostic Status Byte
0x0F	Shutdown Status Byte
0x10	Diskette Drive Type
0x11	Reserved
0x12	Hard Disk Drive Type 1-14
0x13	Reserved
0x14	Equipment
0x15	Low Base Memory
0x16	High Base Memory
0x17	Low Expansion Memory
0x18	High Expansion Memory
0x19	Hard Disk Types 16 Through 63
0x1A	Reserved
0x1B - 0x2D	Reserved
0x2E - 0x2F	2-byte CMOS Checksum
0x30	Low Expansion Memory
0x31	High Expansion Memory
0x32	Data Century
0x33	Information Flags Set During Power-On
0x34 - 0x3F	Reserved
0x40 - 0x7F	User RAM

Figure 2-56. Calendar RAM Locations

Address	Direction	Function
0x0071	W	Real Time Clock (RTC)

Figure 2-54. NMI Enable and Calendar Address

Address	Direction	Function
0x0070	R/W	Calendar Data

Figure 2-55. 82C206 Calendar Data Port

Address	Direction	Function
0x00C0	R/W	Base and Current Address CH 0
0x00C2	R/W	Base and Current Word CH 0
0x00C4	R/W	Base and Current Address CH 1
0x00C6	R/W	Base and Current Word CH 1
0x00CA	R/W	Base and Current Address CH 2
0x00CA	R/W	Base and Current Word CH 2
0x00CC	R/W	Base and Current Address CH 3
0x00CE	R/W	Base and Current Word CH 3
0x00D0	W	Status/Command
0x00D2	W	Request
0x00D4	W	Single Mask Register
0x00D6	W	Mode
0x00D8	R/W	Clear Byte Pointer
0x00DA	R/W	Read Tempmaster Clear
0x00DC	W	Clear Mask
0x00DE	W	All Mask Register

Figure 2-59. 82C206 Word DMA 2

Address	Direction	Function
0x00F0	W	Clear 80387/80287 Busy and Interrupt
0x00F2	W	Reset 80387/80287
0x800000F8	R/W	Opcode Port
0x800000FC	R/W	Operand Port

Figure 2-60. 80387/80287 Math Coprocessor Ports

Port Address	Direction	Function
0x080	R/W	Manufacturing Port
0x081	R/W	DMA Channel 2 Map
0x082	R/W	DMA Channel 3 Map
0x083	R/W	DMA Channel 1 Map
0x084	R/W	Unused
0x085	R/W	Unused
0x086	R/W	Unused
0x087	R/W	DMA Channel 0 Map
0x088	R/W	Unused
0x089	R/W	DMA Channel 6 Map
0x08A	R/W	DMA Channel 7 Map
0x08B	R/W	DMA Channel 5 Map
0x08C	R/W	Unused
0x08D	R/W	Unused
0x08E	R/W	Unused
0x08F	R/W	Refresh Map

Figure 2-57. 82C206 DMA Page Register

Address	Direction	Function
0x00A0	R/W	Status/Control
0x00A1	R/W	Status/Control

Figure 2-58. 82C206 Slave Interrupt Controller 2

Address	Direction	Function
0x00C0	R/W	Base and Current Address CH 0
0x00C2	R/W	Base and Current Word CH 0
0x00C4	R/W	Base and Current Address CH 1
0x00C6	R/W	Base and Current Word CH 1
0x00CA	R/W	Base and Current Address CH 2
0x00CA	R/W	Base and Current Word CH 2
0x00CC	R/W	Base and Current Address CH 3
0x00CE	R/W	Base and Current Word CH 3
0x00D0	W	Status/Command
0x00D2	W	Request
0x00D4	W	Single Mask Register
0x00D6	W	Mode
0x00D8	R/W	Clear Byte Pointer
0x00DA	R/W	Read Tempmaster Clear
0x00DC	W	Clear Mask
0x00DE	W	All Mask Register

Figure 2-59. 82C206 Word DMA 2

Address	Direction	Function
0x00F0	W	Clear 80387/80287 Busy and Interrupt
0x00F2	W	Reset 80387/80287
0x800000F8	R/W	Opcode Port
0x800000FC	R/W	Operand Port

Figure 2-60. 80387/80287 Math Coprocessor Ports

Address	Direction	Function
0x0278	R/W	Bits 0-7 = Printer Data
0x0279	R	Bit 3 = Error
	R	Bit 4 = Selected
	R	Bit 5 = Paper Empty
	R	Bit 6 = Acknowledge
	R	Bit 7 = Busy
0x027A	R/W	Bit 0 = Strobe
	R/W	Bit 1 = Autofold
	R/W	Bit 2 = Init
	R/W	Bit 3 = Select In
	R/W	Bit 4 = Interrupt Enable
		Bit 5 = Unused

Figure 2-61. LPT2 Parallel Port

Address	Direction	Function
0x02F8	R/W	Serial Data Divisor Latch LSB
0x02F9	W	Divisor Latch MSB Interrupt Enabler
0x02FA	W	Interrupt ID Register
0x02FB	W	Line Control Register
0x02FC	W	Modem Control Register
0x02FD	R	Line Status Register
0x02FE	R	Modem Status Register

Figure 2-62. COM2 Serial Port

Address	Direction	Function
0x0378	R/W	Bits 0-7 = Printer Data
0x0379	R	Bit 3 = Error
	R	Bit 4 = Selected
	R	Bit 5 = Paper Empty
	R	Bit 6 = Acknowledge
	R	Bit 7 = Busy
0x037A	R/W	Bit 0 = Strobe
	R/W	Bit 1 = Autofold
	R/W	Bit 2 = Init
	R/W	Bit 3 = Select In
	R/W	Bit 4 = Interrupt Enable
		Bit 5 = Unused

Figure 2-63. LPT1 Parallel Port

Address	Direction	Function
0x03F8	R/W	Serial Data Devisor Latch LSB
0x03F9	W	Divisor Latch MSB Interrupt Enabler
0x03FA	W	Interrupt ID Register
0x03FB	W	Line Control Register
0x03FC	W	Modem Control Register
0x03FD	R	Line Status Register
0x03FE	R	Modem Status Register

Figure 2-64. COM1 Serial Port

Speaker

The Series 3000 Intelligent Workstation's speaker can emit audio indications of error and other conditions. The speaker's volume can be halved by setting switch SW1-6 to ON. The speaker can be driven from either of the following:

- The I/O port output bit (port address 61, internal data bit 1)
- The timer/counter 2 clock output

Figure 2-65 lists the connections for the speaker connector J2.

Pin	Signal	Direction	Description
1	SPKR	Out	Speaker Control
2	Unused		Used for Connector Polarization Key
3	GND		Ground
4	+5V	Out	Speaker Power

Figure 2-65. Speaker Connector J2

Variable Capacitors

A trim capacitor, TC1, adjusts the frequency of the calendar chip oscillator to 32.768 KHz. Test point TP10 (signal OSCI) may be used to monitor the frequency.

Another trim capacitor, TC2, adjusts the frequency of the 14.31818 MHz OSC bus clock. This frequency can be tested by probing I/O bus pin B30.

Real-Time Clock

Status registers A, B, C, and D are located at port addresses 0Ah, 0Bh, 0Ch, and 0Dh, respectively. Status registers A, B, C, and D are described in the following sections:

Status Register A (0Ah)

Bit 7	Update in progress (UIP). 1 = Time update in process. 0 = current date and time available to read.
Bit 6-Bit 4	22-stage divider (DV2 thru DV0). The three divider-selection bits identify the time-based frequency used. The default is 010 = 32.768 KHz time base.
Bit 3-Bit 0	Rate selection bits (RS3 thru RS0). This is the select divider output frequency. The default is 010 = 1.024 KHz square wave output frequency and 976.562 microseconds periodic interrupt rate.

Status Register B (0Bh)

Bit 7	Set to 0 — Updates a cycle normally by advancing counts at one per second. Set to 1 — Aborts any update cycle in progress and allows the program to initialize 14 time bytes (without further updates) until another 0 is written.
Bit 6	Periodic interrupt enable (PIE). A Read/Write bit that allows an interrupt to occur at a rate specified by the rate and divider bits in Status Register A. 1 = Interrupt enabled. 0 = Interrupt disabled. Default = 0.
Bit 5	Alarm interrupt enable (AIE). 1 = Alarm interrupt enabled. 0 = Alarm interrupt disabled. Default = 0.

Bit 4	Update-ended interrupt enabled (UIE). 1 = Update-ended interrupt enabled. 0 = Update-ended interrupt disabled. Default = 0.
Bit 3	Square wave enabled (SQWE). 1 = Square-wave frequency enabled. The frequency is set by rate selection bits in Status Register A. 0 = Square-wave frequency disabled. Default = 0.
Bit 2	Date mode (DM). Date Mode indicates whether the calendar updates use binary or BCD format. 1 = Binary. 0 = BCD. Default = 0.
Bit 1	24/12. Selects 24-hour or 12-hour clock/calendar mode. 1 = 24-hour mode. 0 = 12-hour mode. Default = 1.
Bit 0	Daylight savings time enabled (DSTE) 1 = Daylight savings time enabled. 0 = Daylight savings time disabled. Default = 0.

Status Register C (0Ch)

Bit 7-Bit 4	IRQF, PF, AF, UF. The read-only flag bits are affected when AIE, PIE and UIE interrupts are enabled in Status Register B.
Bit 3-Bit 0	Reserved.

Status Register D (0Dh)

Bit 7	Valid RAM Bit (VRB). This is a read-only bit that senses loss of clock/calendar RAM battery power (see Figure 2-56). 1 = Power on clock/calendar. 0 = Loss of clock/calendar power.
Bit 6-Bit 0	Reserved.

Parallel Port Controller

The parallel port controller is located on motherboard connector J10 (back panel connector J210, a 25-pin female D connector).

The parallel port controller is configured using DIP switch SW2, bits 3 and 4 (see Figure 2-81). Line Printer Port 1 (LPT1) and Line Printer Port 2 (LPT2) occupy port addresses 0378h through 037Fh and 0278h through 027Fh, respectively. Figures 2-66 through 2-68 give the contents of the status, control and data registers.

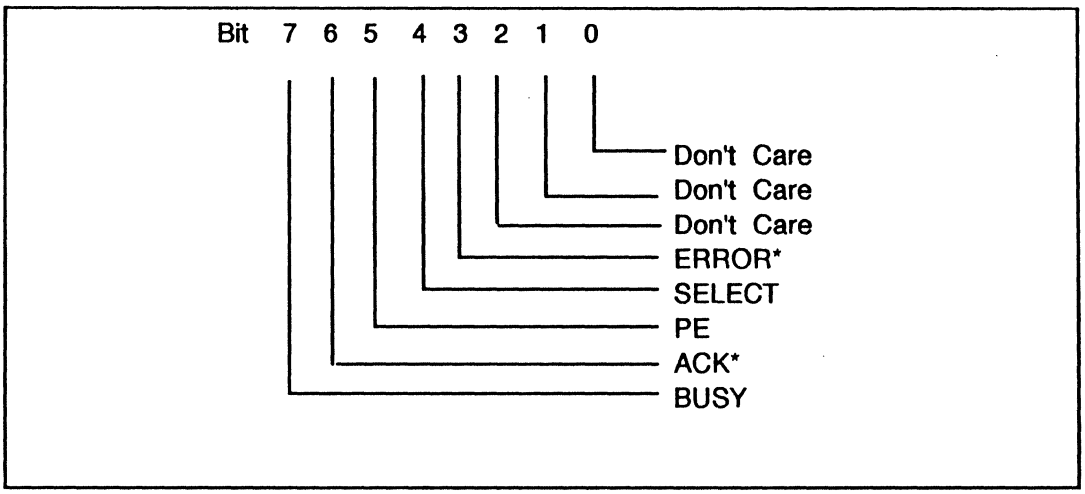

Figure 2-66. Parallel Port Status Register

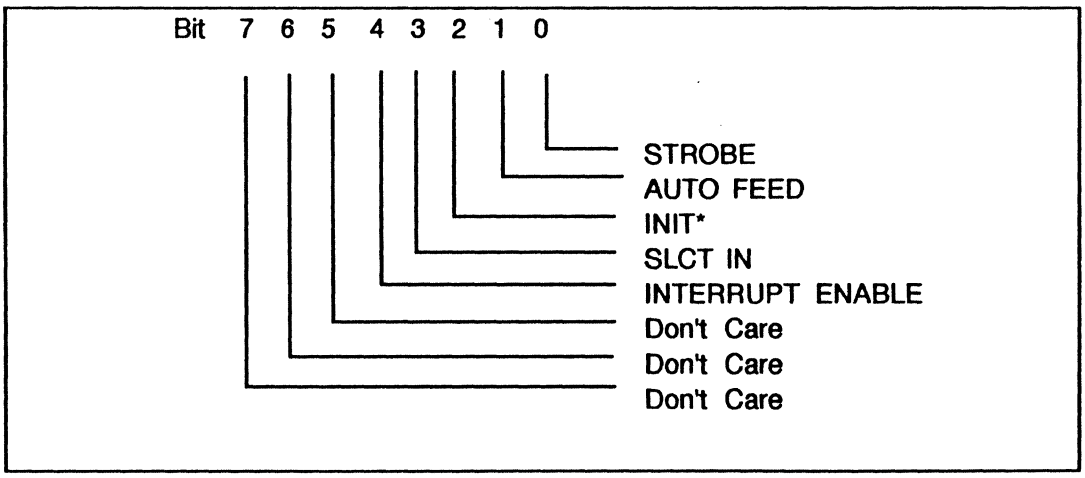

Figure 2-67. Parallel Port Control Register

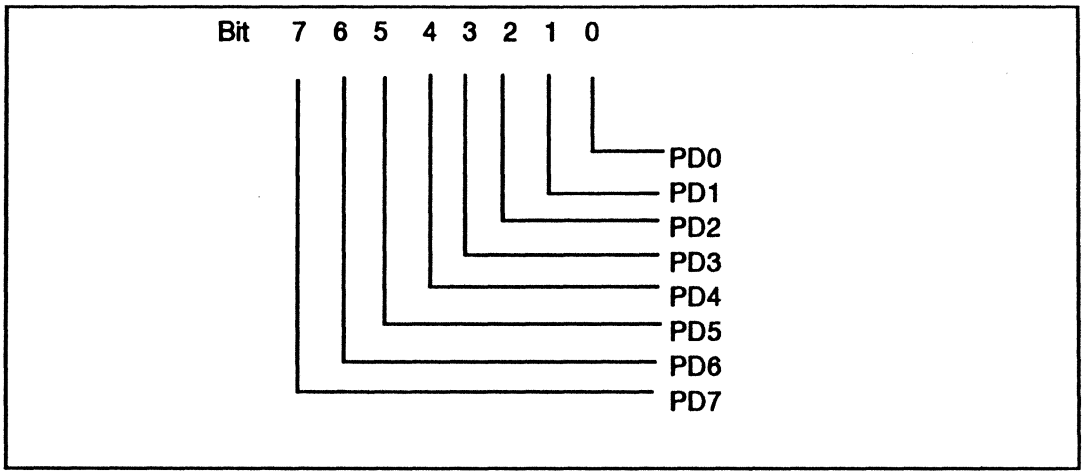

Figure 2-68. Parallel Port Data Register

Serial Port Controller

The motherboard's serial port can be designated COM1 or COM2. Motherboard connector J9 (back panel connector J209, a 9-pin male D connector) is normally used for the M4 optical mouse. See the chapter "Overview" for details.

The serial port controller is configured using DIP switch SW2, bits 1 and 2 (see Figure 2-81), and jumpers E1, E2, and E3 (see Figure 2-79). The port requires eight consecutive I/O addresses for access to the control and status registers. COM1 and COM2 occupy port addresses 03F8h through 03FFh and 02F8h through 02FFh, respectively. Figure 2-69 describes the functions of the serial port registers.

Serial communication can be programmed between 50 baud and 19,200 baud (see Figure 2-70). The programmable baud-rate generator is in the controller chip (not a separate circuit on the board). To determine the baud rate at which the serial port operates, the output of the 1.8432 MHz clock oscillator is divided by 16 and divided again by the 16-bit divisor loaded into the divisor latch registers.

Data for transmission is latched into the transmitter buffer register from the parallel data bus. The transmit data is then strobed out serially at the selected baud rate. Data is clocked into the receive buffer register serially and stored until strobed out onto the parallel data bus by the CPU. For more information, see Figure 2-71. Figures 2-72 through 2-77 describe the interrupt, modem control, line control, and status registers used during data transmission.

Function	I/O Port Address		DLAB State
	COM1	COM2	
Baud Rate Divisor LSB	0x3F8	0x2F8	1
Baud Rate Divisor MSB	0x3F9	0x2F9	1
Transmit Buffer (Write)	0x3F8	0x2F8	0
Receive Buffer (Read)	0x3F8	0x2F8	0
Interrupt Enable Register	0x3F9	0x2F9	0
Interrupt Identification Register	0x3FA	0x2FA	
Line Control Register	0x3FB	0x2FB	
Modem Control Register	0x3FC	0x2FC	
Line Status Register	0x3FD	0x2FD	
Modem Status Register	0x3FE	0x2FE	
Reserved	0x3FF	0x2FF	

Figure 2-69. Serial Port Control and Status Registers

Divisor Latch Registers (When DLAB =1, see Figure 2-70)				
Function			**Most Significant Byte**	**Least Significant Byte**
COM1 COM2			3F9h 2F9h	3F8h 2F8h
Baud	**Divisor**		**Bits**	**Bits**
Rate	**DEC**	**HEX**	**7 6 5 4 3 2 1 0**	**7 6 5 4 3 2 1 0**
50	2304	900	0 0 0 0 1 0 0 1	0 0 0 0 0 0 0 0
75	1536	600	0 0 0 0 0 1 1 0	0 0 0 0 0 0 0 0
110	1047	417	0 0 0 0 0 1 0 0	0 0 0 0 1 1 1 1
134.5	857	359	0 0 0 0 0 0 1 1	0 1 0 1 1 0 0 1
150	768	300	0 0 0 0 0 0 1 0	0 0 0 0 0 0 0 0
300	384	180	0 0 0 0 0 0 0 1	1 0 0 0 0 0 0 0
600	192	0C0	0 0 0 0 0 0 0 0	1 1 0 0 0 0 0 0
1200	96	060	0 0 0 0 0 0 0 0	0 1 1 0 0 0 0 0
1800	64	040	0 0 0 0 0 0 0 0	0 1 0 0 0 0 0 0
2000	58	03A	0 0 0 0 0 0 0 0	0 0 1 1 1 0 1 0
2400	48	030	0 0 0 0 0 0 0 0	0 0 1 1 0 0 0 0
3600	32	020	0 0 0 0 0 0 0 0	0 0 1 0 0 0 0 0
4800	24	018	0 0 0 0 0 0 0 0	0 0 0 1 1 0 0 0
7200	16	010	0 0 0 0 0 0 0 0	0 0 0 1 0 0 0 0
9600	12	00C	0 0 0 0 0 0 0 0	0 0 0 0 1 1 0 0
19200	6	006	0 0 0 0 0 0 0 0	0 0 0 0 0 1 1 0

Figure 2-70. Baud Rate Selection

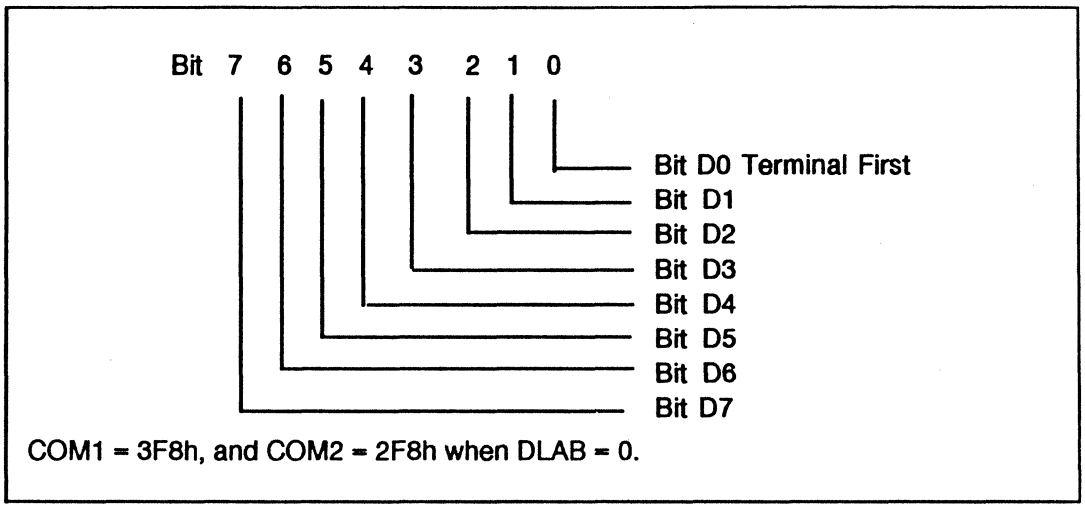

Figure 2-71. Transmit/Receive Buffer Register

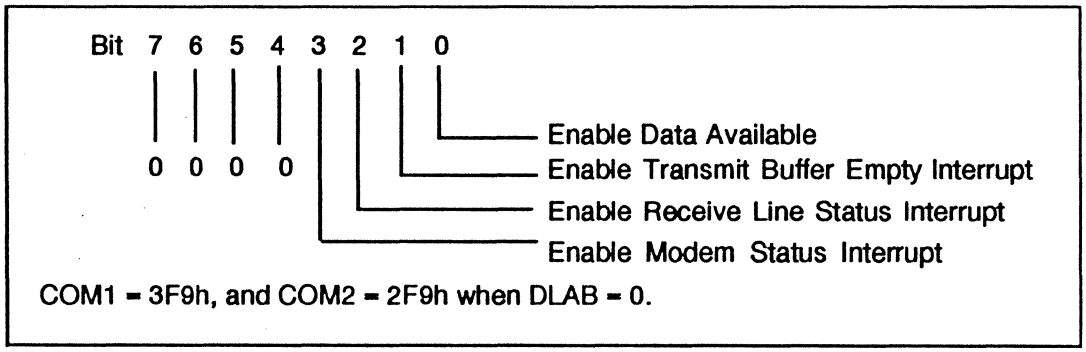

Figure 2-72. Interrupt Enable Register

7 6 5 4 3 2 1 0 | | | | | | | |	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Control
0 0 0 0 0 0 0 0		None	None	
1 1 0	1	Received Line Status	Overrun Parity, or Framing Error, or Break Interrupt	Reading the Line Status Register
1 0 0	2	Received Data Available	Received Data Available	Reading the Receive Buffer Register
0 1 0	3	Transmit Buffer Empty	Transmit Buffer Empty	Reading this Buffer (it is source of Interrupt) or writing into Transmit Buffer Register
0 0 0	4	Modem Status	CTS, DSR, RI, or RD Line Signal Detect	Reading the Modem Status Register
COM1 = 3FAh, and COM2 = 2FAh.				

Figure 2-73. Interrupt Identification Register

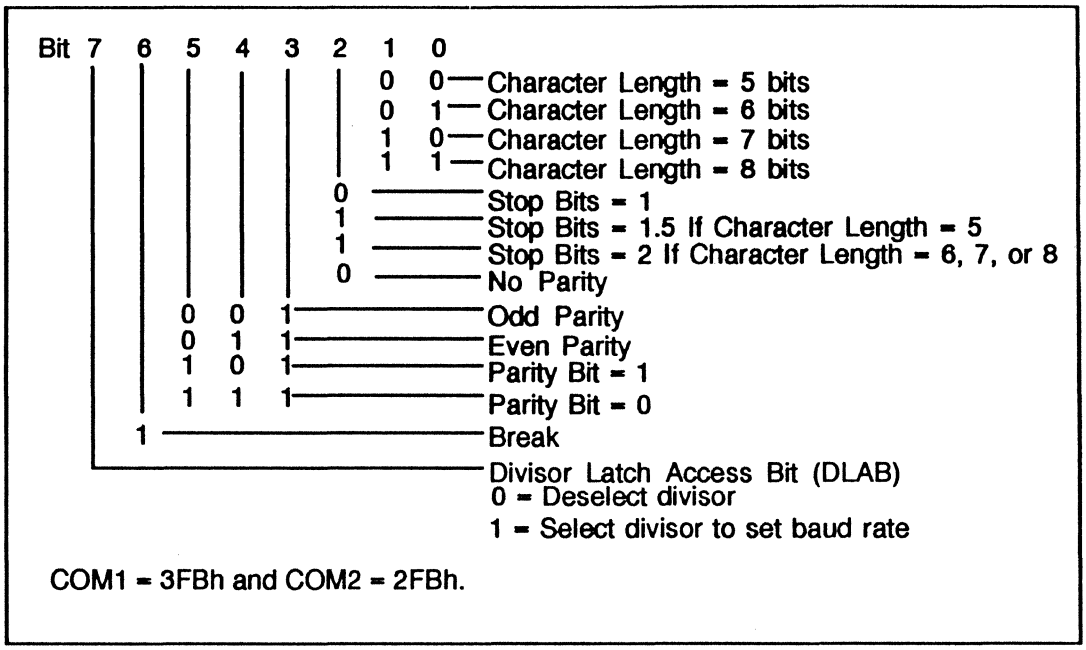

Figure 2-74. Line Control Register

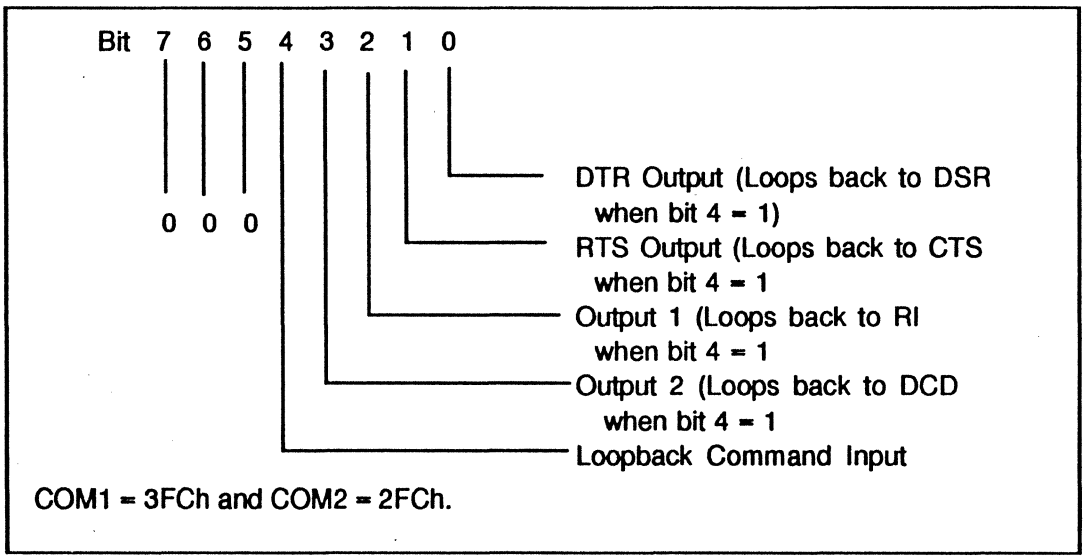

Figure 2-75. Modem Control Register

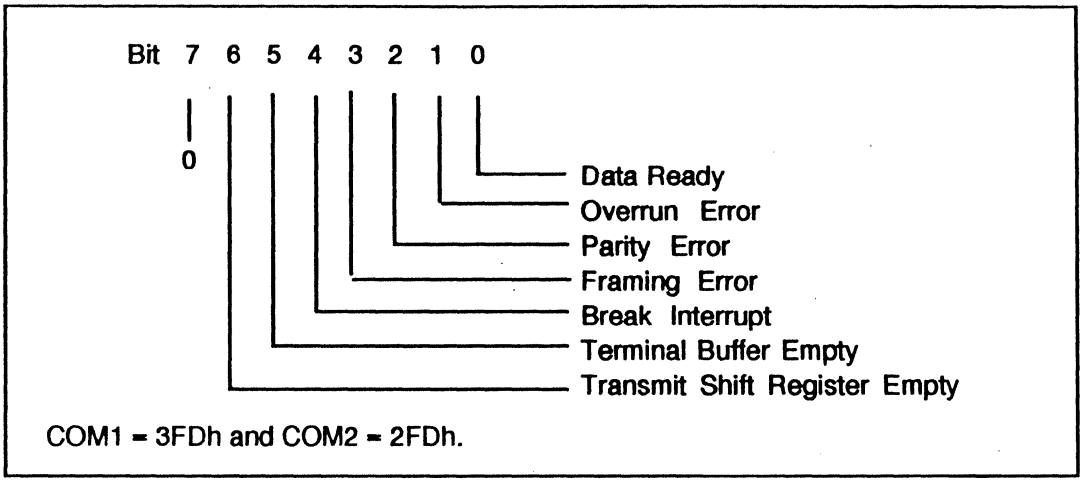

Figure 2-76. Line Status Register

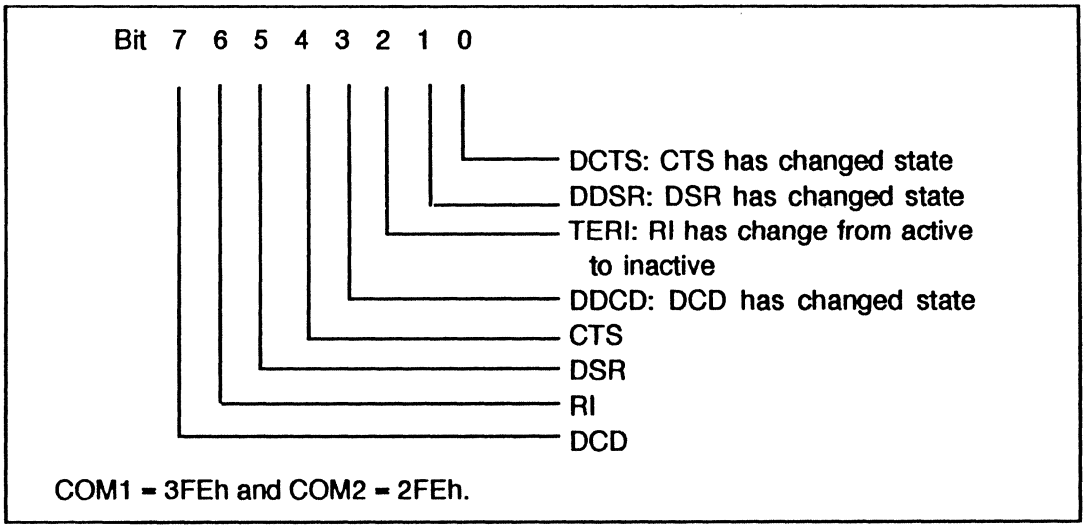

Figure 2-77. Modem Status Register

Motherboard Settings

This section provides information on jumpers (E), switches (SW), test points (TP), LED indicators, and connectors (J) on the motherboard. A plus sign (+) indicates that a bit is set at the factory. Figure 2-78 shows the location of components.

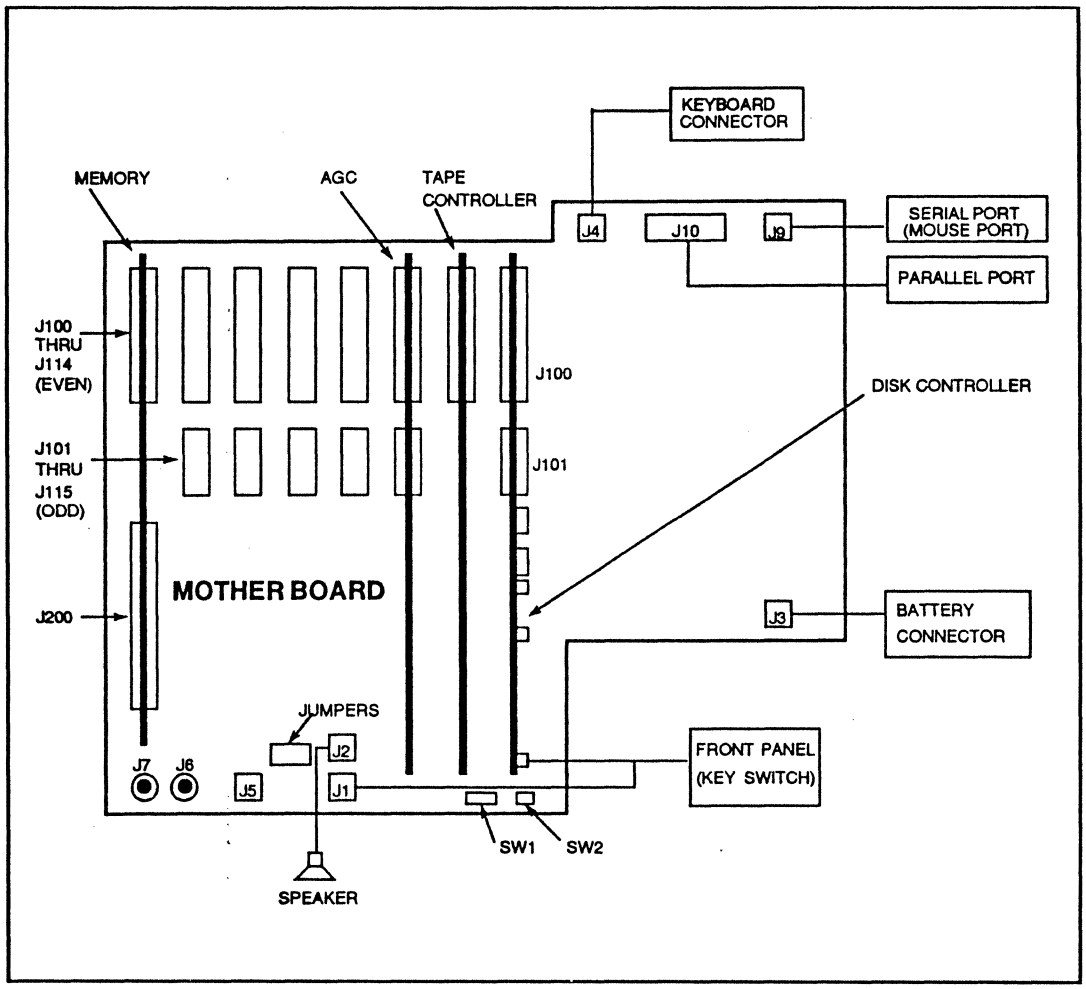

Figure 2-78. Motherboard Component Locations

Jumpers

RS-232-C Data Set Ready, Clear To Send, and Carrier Detect are controlled by jumpers on the motherboard. Figure 2-79 defines the Series 3000 jumper connections.

Jumper	Description
E1	IN = RS-232 DCD Forced True OUT = RS-232 DCD Normal (+)
E2	IN = RS-232 CTS Forced True OUT = RS-232 CTS Normal (+)
E3	IN = RS-232 DSR Forced True OUT = RS-232 DSR Normal (+)
E4	Reserved
E5	A = Normal IOCHRDY Timing (+) B = Delayed Release of IOCHRDY from bus.
(+) Factory Setting	

Figure 2-79. Series 3000 Jumpers

Switches

The two DIP switches define the following:

- The status of I/O Ports
- Video characteristics
- Other system features

Figure 2-80 displays switch settings for SW1. Figure 2-81 displays switch setttings for SW2.

Bit	Description
1	ON Color OFF Monochrome (+)
2	Reserved
3	Reserved
4	ON 27256 EPROM (+) OFF 27128 EPROM
5	ON 80386 Pipelining On (+) OFF 80386 Pipelining Off
6	ON Speaker at Half Volume OFF Speaker at Full Volume (+)
7	ON 80387 Uses Asynchronous Clock from 8284A OFF 80387 Uses Synchronous CPU Clock (+)
8	Unused
	(+) Factory Setting

Figure 2-80. Switch SW1

Bit	Description
1	ON Serial Port Enabled (+) OFF Serial Port Disabled
2	ON Serial Port is COM1 (+) OFF Serial Port is COM2
3	ON Parallel Port Enabled (+) OFF Parallel Port Disabled
4	ON Parallel Port is LPT1 (+) OFF Parallel Port is LPT2
	(+) Factory Setting

Figure 2-81. Switch SW2

Test Points and Indicators

Test points, listed in Figure 2-82, are provided on the motherboard to assist in identifying voltage levels. LED indicators, listed in Figure 2-83, are provided to determine the current operation of the Series 3000 Intelligent Workstation. Figure 2-84 lists the pin assignments for LED connector J1.

Point (TP)	Signal	Description
1	GND	
2	-5V	
3	+12V	
4	GND	
5	GND	
6	GND	
7	GND	
8	GND	
9	GND	
10	OSCI	32768 HZ Calendar Oscillator Output
11	GND	
12	GND	
13	+5V	

Figure 2-82. Test Points

LED (DS)	Description
1	On when CPU is halted (Red)
2	On when CPU is shut down (Red)
3	On when CPU is active (Green)
4	On when interrupt is pending (Yellow)
5	On when DMA is active (Yellow)

Figure 2-83. LED Indicators

Pin	Signal	Direction	Description
1	PWRLED	Out	+5V Through 150 Ohm Resistor
2	Unused		Used for Connecter Polarization Key
3	Unused		
4	CPULED	Out	CPU Bus Activity
5	Unused		
6	RESIN*	In	Reset Switch Input
7	GND		Ground
8	KBDINH*	In	Keyboard Inhibit

Figure 2-84. LED Connector J1

I/O Connectors

There are eight 62-pin and six 36-pin connectors on the motherboard. The six slots that have both 62-pin and 36-pin connectors can accommodate 16-bit devices. The two slots with just the 62-pin connector accept only 8-bit devices. Figures 2-85 and 2-86 list the pin assignments for these I/O connectors. An asterisk (*) on a signal name indicates an active low signal.

All I/O signal lines are TTL-compatible. I/O adapters should be designed with a maximum of two low-power Schottky (LS) loads per line.

Figure 2-87 illustrates DRAM board connector J200. Figures 2-88 and 2-89 show the serial port connector pins (J9) and the parallel port connector pins (J10), respectively. Figure 2-90 shows the calendar battery connector, J3. An asterisk (*) on a signal name indicates an active low signal.

Pin	Signal	Direction	Description
A1	IOCHCK*	In	I/O Bus Error Signal
A2	SD7	I/O	Data Bit 7
A3	SD6	I/O	
A4	SD5	I/O	
A5	SD4	I/O	
A6	SD3	I/O	
A7	SD2	I/O	
A8	SD1	I/O	
A9	SD0	I/O	Data Bit 0
A10	IOCHRDY	In	I/O Channel Ready
A11	AEN	Out	Address Enable (DMA Active)
A12	SA19	I/O	Address Bit 19
A13	SA18	I/O	
A14	SA17	I/O	
A15	SA16	I/O	
A16	SA15	I/O	
A17	SA14	I/O	
A18	SA13	I/O	
A19	SA12	I/O	
A20	SA11	I/O	
A21	SA10	I/O	
A22	SA9	I/O	
A23	SA8	I/O	
A24	SA7	I/O	
A25	SA6	I/O	
A26	SA5	I/O	
A27	SA4	I/O	
A28	SA3	I/O	
A29	SA2	I/O	
A30	SA1	I/O	
A31	SA0	I/O	Address Bit 0

For Expansion Connectors J100, J102, J104, J106, J108, J110, J112, and J114.

Figure 2-85. I/O Expansion Bus J100 Through J114 (Even), Part 1

Pin	Signal	Direction	Description
B1	GND		Ground
B2	RESETEDRV	Out	Master Reset
B3	+5V	Out	Power
B4	IRQ9	In	Interrupt Request 9
B5	-5V	Out	Power
B6	DREQ2 (FLOPPY)	In	DMA Request 2
B7	-12V	Out	Power
B8	OWS*	In	No Wait States
B9	+12V	Out	Power
B10	GND		Ground
B11	SMEMW*	Out	Memory Write Strobe
B12	SMEMR*	Out	Memory Read Strobe
B13	IOW*	I/O	I/O Write Strobe
B14	IOR*	I/O	I/O Read Strobe
B15	DACK3*	Out	DMA Acknowledge 3
B16	DREQ3	In	DMA Request 3
B17	DACK1*	Out	DMA Acknowledge 1
B18	DREQ1	In	DMA Request 1
B19	REFRESH	I/O	System Refresh
B20	SYSCLK	Out	Bus Clock (6 or 8 MHz)
B21	IRQ7(PRT1)	In	Interrupt Request 7
B22	IRQ6 (FLOPPY)	In	Interrupt Request 6
B23	IRQ5(PRT2)	In	Interrupt Request 5
B24	IRQ4(COM1)	In	Interrupt Request 4
B25	IRQ3(COM2)	In	Interrupt Request 3
B26	DACK2*	Out	DMA Acknowledge 2
B27	T/C	Out	DMA Terminal Count
B28	BALE	Out	Address Latch Enable
B29	+5V	Out	Power
B30	OSC	Out	14.31818 MHz Clock
B31	GND		Ground

For Expansion Connectors J100, J102, J104, J106, J108, J110, J112, and J114.

Figure 2-85. I/O Expansion Bus J100 Through J114 (Even), Part 2

Pin	Signal	Direction	Description
C1	SBHE*	I/O	Byte High Enable
C2	LA23	I/O	Address Bit 23
C3	LA22	I/O	Address Bit 22
C4	LA21	I/O	Address Bit 21
C5	LA20	I/O	Address Bit 20
C6	LA19	I/O	Address Bit 19
C7	LA18	I/O	Address Bit 18
C8	LA17	I/O	Address Bit 17
C9	MEMR*	I/O	Memory Read
C10	MEMW*	I/O	Memory Write
C11	SD8	I/O	Data Bit 8
C12	SD9	I/O	Data Bit 9
C13	SD10	I/O	Data Bit 10
C14	SD1	I/O	Data Bit 11
C15	SD12	I/O	Data Bit 12
C16	SD13	I/O	Data Bit 13
C17	SD14	I/O	Data Bit 14
C18	SD15	I/O	Data Bit 15
For PC-AT Type Expansion I/O Bus			

Figure 2-86. I/O Expansion Bus J101 Through J115 (Odd), Part 1

Pin	Signal	Direction	Description
D1	MEMCS16*	I/O	16-bit Memory Transfer
D2	IOCS16*	IN	16-bit I/O Transfer
D3	IRQ10	IN	Interrupt Request 10
D4	IRQ11	IN	Interrupt Request 11
D5	IRQ12	IN	Interrupt Request 12
D6	IRQ15	IN	Interrupt Request 15
D7	IRQ14 (HARD DISK)	IN	Interrupt Request 14
D8	DACK0*	OUT	DMA Acknowledge 0
D9	DREQ0	IN	DMA Request 0
D10	DACK5*	OUT	DMA Acknowledge 5
D11	DREQ5	IN	DMA Request 5
D12	DACK6*	OUT	DMA Acknowledge 6
D13	DREQ6	IN	DMA Request 6
D14	DACK7*	OUT	DMA Acknowledge 7
D15	DREQ7	IN	DMA Request 7
D16	+5V	OUT	Power
D17	MASTER*	IN	DMA Master
D18	GND		Ground
For PC-AT Type Expansion I/O Bus			

Figure 2-86. I/O Expansion Bus J101 Through J115 (Odd), Part 2

Pin	Signal	Direction	Description
1	GND		Logic Ground
2	MA0	Out	Memory Address Bit 0
3	MA2	Out	Memory Address Bit 2
4	MA4	Out	Memory Address Bit 4
5	MA6	Out	Memory Address Bit 6
6	+5V	Out	Logic Power
7	MA8		Memory Address Bit 8
8	MA10	Out	Memory Address Bit 10 (Unused)
9	BA1	Out	Block Address Bit 1
10	DRD*	Out	Low for reading memory
11	GND		Logic Ground
12	LBE0*	Out	Latch Byte Enable 0
13	LBE2*	Out	Latch Byte Enable 2
14	CACHE*	Out	Low When Cache Controller Installed
15	RAS0*	Out	Row Address Strobe for Bank 0
16	+5V		Logic Power
17	RAS2*	Out	Row Address Strobe for Bank 2
18	CAS*	Out	Column Address Strobe
19	CAS0*	Out	Column Address Strobe for Bank 0
20	CAS2*	Out	Column Address Strobe for Bank 2
21	GND		Logic Ground
22	MD0	I/O	Memory Data Bit 0
23	MD2	I/O	Memory Data Bit 2
24	MD4	I/O	Memory Data Bit 4
25	MD6	I/O	Memory Data Bit 6
26	+5V		Logic Power
27	MP0	I/O	Memory Parity Bit 0
28	MD9	I/O	Memory Data Bit 9
29	MD11	I/O	Memory Data Bit 11
30	MD13	I/O	Memory Data Bit 13

Figure 2-87. DRAM Board Connectors J200 and J201, Part 1

Pin	Signal	Direction	Description
31	GND		Logic Ground
32	MD15	I/O	Memory Data Bit 15
33	MD16	I/O	Memory Data Bit 16
34	MD18	I/O	Memory Data Bit 18
35	MD20	I/O	Memory Data Bit 20
36	+5V		Logic Power
37	MD22	I/O	Memory Data Bit 22
38	MP2	I/O	Memory Parity Bit 2
39	MD25	I/O	Memory Data Bit 25
40	MD27	I/O	Memory Data Bit 27
46	MA3	Out	Memory Address Bit 3
47	MA5	Out	Memory Address Bit 5
48	MA7	Out	Memory Address Bit 7
49	GND		Logic Ground
50	MA9	Out	Memory Address Bit 9
51	BA0	Out	Block Address Bit 0
52	FBK*	Out	Force All Banks Enabled for Refresh
53	DWE*	Out	DRAM Write Strobe
54	+5V		Logic Power
55	LBE1*	Out	Latched Byte Enable 1
56	LBE3*	Out	Latched Byte Enable 3
57	DBEN*	Out	Memory Data Buffer Enable
58	RAS1*	Out	Row Address Strobe for Bank 1
59	GND		Logic Ground
60	RAS3*	Out	Row Address Strobe for Bank 3
61	SPARE		
62	CAS1*	Out	Column Address Strobe for Bank 1
63	CAS3*	Out	Column Addresss Strobe for Bank 3

Figure 2-87. DRAM Board Connectors J200 and J201, Part 2

Pin	Signal	Direction	Description
64	+5V		Logic Power
65	MD1	I/O	Memory Data Bit 1
66	MD3	I/O	Memory Data Bit 3
67	MD5	I/O	Memory Data Bit 5
68	MD7	I/O	Memory Data Bit 7
69	GND		Logic Ground
70	MD8	I/O	Memory Data Bit 8
71	MD10	I/O	Memory Data Bit 10
72	MD12	I/O	Memory Data Bit 12
73	MD14	I/O	Memory Data Bit 14
74	+5V		Logic Power
75	MP1	I/O	Memory Parity Bit 1
76	MD17	I/O	Memory Data Bit 17
77	MD19	I/O	Memory Data Bit 19
78	MD21	I/O	Memory Data Bit 21
79	GND		Logic Ground
80	MD23	I/O	Memory Data Bit 23
81	MD24	I/O	Memory Data Bit 24
82	MD26	I/O	Memory Data Bit 26
83	MD28	I/O	Memory Data Bit 28
84	MD30	I/O	Memory Data Bit 30
85	MP3	I/O	Memory Parity Bit 3
86	+5V		Logic Power

Figure 2-87. DRAM Board Connectors J200 and J201, Part 3

Pin	Signal	Direction	Description
1	DCD	In	Data Carrier Detect
2	RXD	In	Receive Data
3	TXD	Out	Transmit Data
4	DTR	Out	Data Terminal Ready
5	GND		Ground
6	DSR	In	Data Set Ready
7	RTS	Out	Request To Send
8	CTS	In	Clear To Send
9	RI	In	Ring Indicator

Figure 2-88. Serial Port Connector J9

Pin	Signal	Direction	Description
1	STROBE*	OUT	Pulsed to Write Data to Printer
2	PD0	OUT	Printer Data Bit 0
3	PD1	OUT	Printer Data Bit 1
4	PD2	OUT	Printer Data Bit 2
5	PD3	OUT	Printer Data Bit 3
6	PD4	OUT	Printer Data Bit 4
7	PD5	OUT	Printer Data Bit 5
8	PD6	OUT	Printer Data Bit 6
9	PD7	OUT	Printer Data Bit 7
10	PACK*	IN	Pulsed When Data Has Been Accepted
11	PBUSY	IN	Printer Cannot Receive Data
12	PE	IN	Paper Empty
13	SLCT	IN	Printer Is Selected
14	AUTOFDXT*	OUT	Auto Line Feed
15	PERROR*	IN	Paper-End Off-line Error State
16	INIT*	OUT	Initialize
17	SLCTIN*	OUT	Printer Selected
18	GND		Ground
19	GND		Ground
20	GND		Ground
21	GND		Ground
22	GND		Ground
23	GND		Ground
24	GND		Ground
25	GND		Ground

Figure 2-89. Parallel Port Connector J10

Battery Power

Power is supplied for the date/time calendar through battery connector J3 . Figure 2-90 lists the pin assignments for the battery connector.

Pin	Signal	Description
1	+6V	Battery Output
2	Unused	Used for Connector Polarization Key
3	GND	Logic Ground
4	GND	Logic Ground

Figure 2-90. Calendar Battery Connector J3

Chapter 3. BIOS

Introduction

The Basic Input Output System (BIOS) resides in ROM on the motherboard. BIOS controls communications between internal I/O devices and those attached to the computer. Device level control for additional option boards is provided by ROM on the additional option boards. BIOS also includes these features:

- A graphics character generator
- A print screen function
- A clock/calendar.

If motherboard ROM sockets 18Fh and 22Fh are empty, additional ROM can be placed in these sockets.

BIOS controls the computer's hardware devices. It makes hardware modifications and enhancements transparent to user programs. Thus, BIOS routines permit assembly language block-level disk operations or character-level I/O operations to be programmed regardless of device characteristics or addresses. BIOS also provides time, date, memory-size determination, and other services.

During power-on diagnostics, a test is made for valid codes, starting at address 0xE0000 and ending at 0xEFFFF. BIOS performs an automatic self-test at power-up. Expansion devices are tested prior to boot-up.

BIOS supports the following input/output functions:

- Keyboard
- Floppy disk
- Hard disk
- Asynchronous serial port
- Parallel port
- Display

Using the BIOS

BIOS is accessed through CPU interrupts in the real mode. Each BIOS entry point is available through its own interrupt. For example, to determine the amount of base RAM available with the 80386 microprocessor in the real mode, INT 12H invokes the BIOS routine for determining memory size. The value is returned to the caller.

Passing Parameters

All parameters passed between BIOS routines go through CPU registers. Each BIOS function prolog indicates the registers used at call and return. For memory-size determination, no parameters are passed in. The memory size (in 1KB increments) is returned in the AX register. The AH register is used at input to indicate the desired operation.

The code to set the time of day is the following:

```
MOV AH,3              ;set real time clock
MOV CH,HOURS          ;hours in BCD
MOV CL,MINS           ;minutes in BCD
MOV DH,SECS           ;seconds in BCD
MOV DL,DAYLGT         ;1=daylight savings time
INT 1AH               ;call time of day function
```

Here is the code to read the time of day:

```
MOV AH,2              ;read real time clock
INT 1AH               ;call time of day function
```

BCD hours in CH, BCD minutes in CL, and BCD seconds in DH are returned.

BIOS routines typically save all registers except the AX and flag registers. Others are changed at return, but only when returning a value to the caller. Register use can be identified in each BIOS function prolog.

Selected Interrupt Vectors and Parameter Pointers

This section describes selected interrupt vectors and parameter pointers:

- 15h — Cassette Interface

This points to:

1. Event wait
2. Joystick support
3. Wait
4. Block move
5. Determination of memory size over 1MB
6. Virtual memory mode
7. Device busy
8. Flag interrupt complete (program termination)

Refer to the BIOS listings for more information on this vector's functions.

- 1Bh — Keyboard Break Address

This points to the code executed if the **Ctrl** and **BREAK** keys are simultaneously pressed. The vector is invoked when responding to a keyboard interrupt. Control should be returned through an IRET instruction. At power-on, the vector is initialized to point to an IRET instruction so that nothing happens when **Ctrl** and **BREAK** are pressed. The application program may set a different value.

- 1Ch — Timer Tick

This points to the code executed at each system-clock tick. It is invoked when responding to the timer interrupt. Control should be returned by an IRET instruction. The power-on routines initialize this vector to point to an IRET instruction. Thus, nothing occurs unless the application reassigns the pointer. The application must save and restore all modified registers.

- 1Dh — Video Parameters

This points to the data region containing parameters needed to initialize the video board's 6845. The 6845 is emulated when the Advanced Graphics Controller has the optional PVE board attached. There are four separate tables. All four must be reproduced to support all modes of operation. At power-on, the vector is initialized to point to the parameters contained in ROM video routines.

- 1Eh — Floppy-Disk Parameters

This points to a data region containing parameters needed for the floppy disk drive. At power-on, this vector is initialized to point to ROM floppy routine parameters. These defaults represent the requisite values for any standard drives.

- 1Fh — Graphics Character Extensions

When the read/write character controller is in the 320 x 200 or 640 x 200 graphics modes, it forms characters from an ASCII character table, using a set of dot patterns. Patterns for the first 128 characters are in ROM. If more characters are needed, change the value (0000:0) to which the vector is initialized at power-up. When established, the vector must point to a table of 1KB. Each character is represented by 8 bytes of graphic information.

- 40h — Reserved

The BIOS routines use interrupt 40h to revector the floppy disk pointer. The Series 3000 Intelligent Workstation's disk drive controller is always installed.

- 41h and 46h — Hard Disk Parameters

These point to the hard disk drive parameters:

  - 41h is for the hard drive.

  - 46h is reserved.

At power-on, if CMOS is valid, the vectors are initialized to point to appropriate parameters in the ROM disk routine. The CMOS drive type codes are used to select the parameter set pointed to.

Figure 3-1 lists the interrupt vectors and parameter pointers. Figure 3-2 lists hardware and MS-DOS reserved interrupts.

Address (hex)	Function	Interrupt or Pointer
0	Divide by Zero	
1	Single Step	
2	Non-maskable	
3	Breakpoint	
4	Overflow	
5	Print Screen	
6	Reserved	
7	Reserved	
8	Time of Day	
9	Keyboard	
A	Reserved	
B	Communications	
C	Communications	
D	Alternate Printer	
E	Floppy Disk	
F	Printer	
10	Video	
11	Equipment Check	
12	Memory	
13	Hard/Floppy Disk	
14	Communications	
15	Cassette	
16	Keyboard I/O	
17	Printer I/O	
18	ROM Monitor	
19	Bootstrap	
1A	Time of Day	
1B	Keyboard Break	
1C	TimerTick	
1D	Video Initialization	
1E	Floppy Disk Parameters	Pointer
1F	Video Graphics Characters	Pointer
40	Reserved	Pointer
41	Hard Disk Parameters	Pointer
46	Hard Disk Parameters	Pointer

Figure 3-1. Table of Interrupt Vectors and Parameter Pointers (Real Mode)

Interrupt	Function
0x20	MS-DOS Program Termination
0x21	MS-DOS Function Call
0x22	MS-DOS Terminate Address
0x23	MS-DOS CTRL Break Exit Address
0x24	MS-DOS Fatal Error Vector
0x25	MS-DOS Absolute Disk Read
0x26	MS-DOS Absolute Disk Write
0x27	MS-DOS Terminate, Fix in Storage
0x28-0x3F	Reserved For MS-DOS
0x40-0x5F	Reserved
0x60-0x67	Reserved For User Program Interrupts
0x68-0x6F	Not Used
0x70	IRQ8 Real-Time Clock Interrupt
0x71	IRQ9
0x72	IRQ10
0x73	IRQ11
0x74	IRQ12
0x75	IRQ13 BIOS Redirected to NMI
0x76	IRQ14
0x77	IRQ15
0x78-0x7F	Not Used
0x80-0x85	Reserved For BASIC
0x86-0xF0	Used by BASIC Interpreter When BASIC is Running
0xF1-0xFF	Not Used

Figure 3-2. Table of Hardware and MS-DOS Interrupts

Other Read/Write Memory Use

The BIOS routines use 256 bytes of memory from absolute 0x400 to 0x4FF (see Figure 3-3, parts 1 through 3). Locations 0x400 to 0x407 contain the base addresses of the RS-232-C serial communications boards in the computer. Locations 0x408 to 0x40F contain the base addresses of the parallel printer port controller. Locations 0x300 to 0x3FF are used as a stack area at power-on initialization and bootstrap (when control is passed to it from power-on). The application should allocate a different area to the stack where necessary.

Figure 3-4 is the BIOS memory map.

Address Mode	Function
0x400 - 0x4A1	ROM BIOS Data Area Miscellaneous Variables Addresses of RS-232 Ports Installed Configuration Manufacture Byte Memory Size (in KB) Manufacturing Scratchpad Keyboard Variables Keyboard Status Second Keyboard Status Alternate Keyboard Storage Pointer to Head of Keyboard Queue Pointer to Keyboard Queue Keyboard Queue Floppy Disk Drive Variables Drive Recalibrate Status Drive Spindle Motor Status Spindle Motor Shutoff Counter Floppy Disk Status Return Code Hard Disk Common Block Hard Disk Error Byte Status Byte From Controller Video Display Variables Current Video Display Mode Number of Columns on Display Regen Length in Bytes Regen Buffer Start Address Cursor Position For up to 8 Pages Current Cursor Mode Current Displayed (Active) Page Active Page Port Address Current Setting of 3 X 8 Register Current Palatte Setting (Color) Power-On Diagnostics Variables Optional Initialization Routine (Offset) Optional Initialization Routine (Segment) Interrupt Indicator (Flag)

Figure 3-3. Table of Reserved Memory Locations, Part 1

Address Mode	Function
0x400 - 0x4A1	Timer Variables: Timer Tick Counter 24 Hour Overflow System Variables: Bit 7 = 1 If Break Key Pressed Word = 1234H For Soft Reset Hard Disk Variables: Copy of Last Return Byte Number of Hard Disks Installed Control Retries and Extra Heads RS-232 And Printer Timeout Variables: Timeout For Parallel Printer Ports Timeout For RS-232 Serial Ports Additional Keyboard Variables: Start of Keyboard Queue End of Keyboard Queue Additional Floppy Disk Variables: Last Data Rate Selected Additional Hard Disk Variables: Copy of Hard Disk Status Register Copy of Hard Disk Error Register Hard Disk Interrupt Flag Additional Floppy Disk Variables: Drive 0 Media Status Drive 1 Media Status Drive 0 Operation Status Drive 1 Operation Status Drive 0 Present Cylinder Drive 1 Present Cylinder Reserved Keyboard LED Flag

Figure 3-3. Table of Reserved Memory Locations, Part 2

Address Mode	Function
	Real Time Clock Variables: User Event Flag Offset Pointer Event Timer (32 Bits) Event Timer Active Flag
0x4A2 - 0x4EF	Reserved
0x4F0 - 0x4FF	Reserved For Communications Between Applications
0x500 - 0x5FF	Reserved For MS-DOS
0x500	Print Screen Status Flag Store 0 = Print Screen Not Active or Successful Print Screen Operation 1 = Print Screen In Progress 255 = Error Encountered During Print Screen Operation
0x504	MS-DOS Single Drive Mode Status Byte

Figure 3-3. Table of Reserved Memory Locations, Part 3

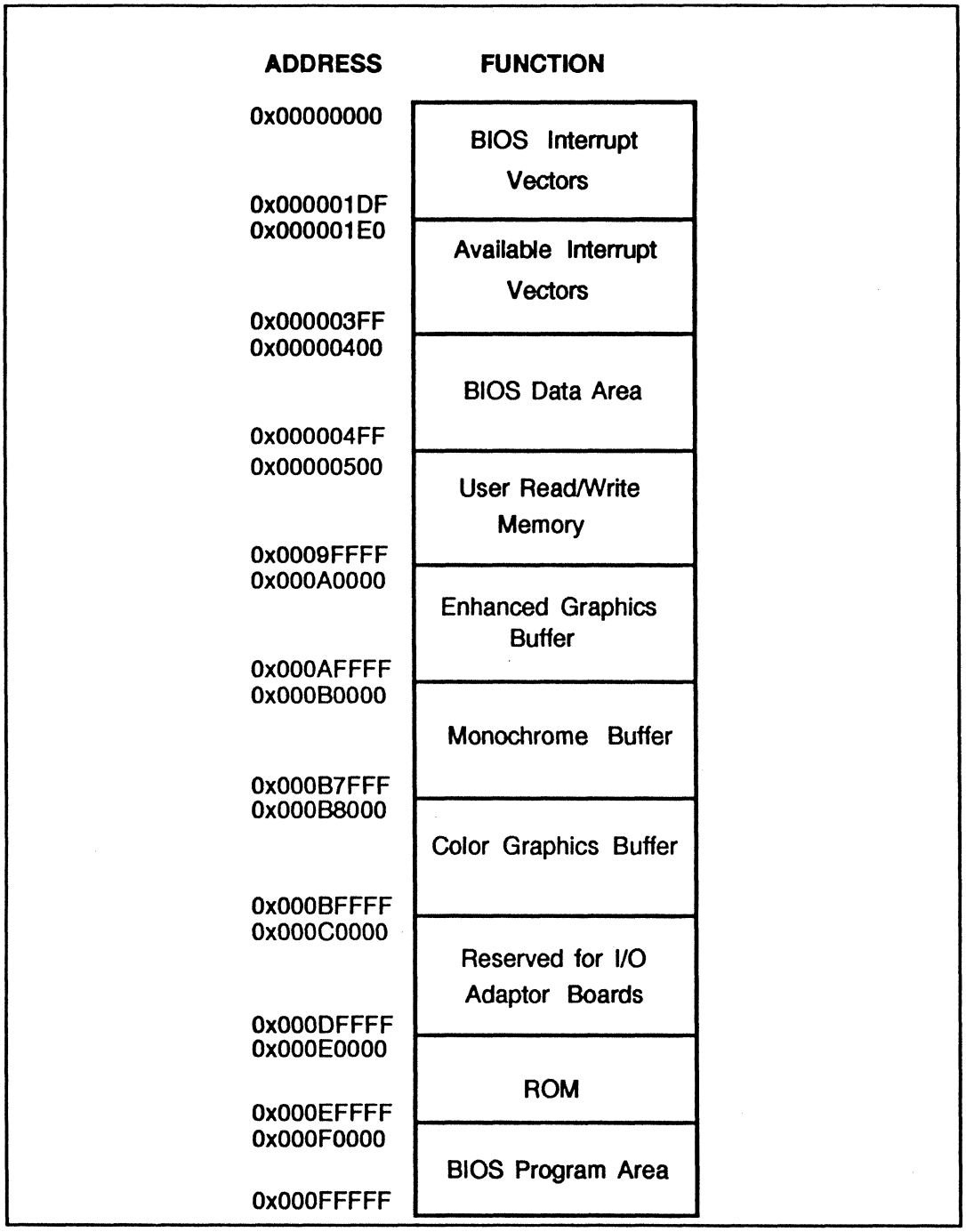

Figure 3-4. BIOS Memory Map

Keyboard Use and Encoding

This section covers the following topics:

- Encoding
- Character Codes
- Extended Functions
- Shift States
- Other Characteristics

Encoding

The Series 3000 Intelligent Workstation ROM converts keyboard scan codes into an extended version of ASCII. It includes all one-byte character codes from 0 to 255. The version also has an extended code for the following:

- Special keyboard functions
- System functions handled by the keyboard routine
- Functions handled by interrupts

Character Codes

ASCII character codes are passed to the system or application program through the BIOS keyboard routine. A "-1" means that the combination is suppressed in the keyboard routine. The codes are returned in the AL register. The chapter "Keyboard" lists keyboard codes.

Extended Functions

An extended code is used for functions not represented in standard ASCII. AL returns 000. This indicates that the program should examine a second code to verify the actual function. The second code, returned in AH, is normally the scan code of the key pressed. The chapter "Keyboard" lists these codes.

Shift States

Shift states are mainly handled by the keyboard routine. Shift states are invisible to the application or system program. The current status of active shift states is available at any time through calls to an entry point in the ROM keyboard routine.

The following keys result in altered shift states:

Shift Temporarily shifts keys 1-14, 16-28, 31- 41, 46-55, 106, and 65-74 to uppercase (lowercase if in **Caps Lock** state). **Shift** also temporarily reverses the **Num Lock** or non-**Num Lock** state of keys 91-93, 96, 98, and 101-103.

Ctrl Temporarily shifts keys 3, 7, 13, 15, 17-28, 31-39, 46-52, 106, 65-74, 42, 101, 92, 102, 91, 93, 95, 100, and 103 to the **Ctrl** state. **Ctrl** is also used with **Alt** and **Del** to cause Reset, with **Scroll Lock** to cause Break, and with **Num Lock** to cause the pause function.

Alt Temporarily changes keys 1-13, 17-26, 31-39, 46-52, and 65-74 to the **Alt** state. It can also be used with **Ctrl** and **Del** to initiate Reset.

The following **Alt** key shift state is supported on MS-DOS. It is not supported on MAD/ix or in the X Window System. The **Alt** key also permits entry of any character code (0 to 255) from the keyboard. To enter a character that may or may not be available on the keyboard, follow these steps:

1. Hold down **Alt** and type the decimal value (up to three digits) of the character desired on the numeric keypad (keys 91-93, 96-98, and 101-103).
2. Release the **Alt** key.
3. If more than three digits are typed, a modulo-256 remainder is generated. The result is interpreted as a character code and sent through the keyboard routine to the system or application program.

Break Simultaneous **Ctrl** and **Break** causes the keyboard routine to effect interrupt 1B. Also returned are extended characters AL=00 and AH=00.

Pause The following **Pause** shift state is supported on MS-DOS only. It is not supported on MAD/ix or in the X Window System. When **Ctrl** and **Num Lock** are pressed simultaneously, the keyboard interrupt routine loops and waits for any key to be pressed except **Num Lock, Shift, Caps Lock, Ctrl, Scroll Lock,** or **Alt.** Functions like list or print can thus be momentarily suspended in a system- or application-transparent way. The key used to resume operation is discarded. **Pause** is internal to the keyboard routine.

Print Screen The following **Print Screen** shift state is supported on MS-DOS only. It is not supported on MAD/ix or in the X Window System. When **Shift** and **Print Screen** are pressed simultaneously,an interrupt invokes the print screen routine. This routine works in the alphanumeric or graphics mode, with unrecognizable characters appearing as blanks.

Caps Lock Toggles keys 17-26, 31-39, and 46-52 between uppercase and lowercase modes. The keys are fixed at the selected mode when this key is pressed. Uppercase mode is indicated by the **Caps Lock** light. **Caps Lock** is internal to the keyboard routine.

Scroll Lock The following **Scroll Lock** shift state is supported on MS-DOS only. It is not supported on MAD/ix or in the X Window System. Pressing this key can be interpreted by application programs to mean that the cursor control keys should produce windows over the text and not cause cursor movement. When **Scroll Lock** is pressed again, the function is toggled. The keyboard routine simply records the current shift state of **Scroll Lock**. The application program is responsible for performing the function. When pressed, **Scroll Lock** toggles the **Scroll Lock** light.

Num Lock This key shifts the numerics keypad to uppercase. When pressed again, **Num Lock** reverses the action. If **Num Lock** and **Ctrl** are simultaneously pressed, a pause occurs. **Num Lock** is internal to the keyboard routine. When pressed, **Num Lock** toggles the **Num Lock** light.

SysRq

The following **SysRq** shift state is supported on MS-DOS only. It is not supported on MAD/ix or in the X Window System. When **SysRq** is pressed, 8500h is placed in AX and an interrupt 15 is executed. When **SysRq** is released, 8501h is placed in AX and an interrupt 15 is executed. If an application needs **SysRq**, the following rules must be observed:

- Save the previous address.
- Overlay interrupt vector 15.
- Check AH for a value of 85:
  - If yes, the process can begin.
  - If no, go to the previous address.

The application is responsible for preserving the value in all registers except AX upon return. **SysRq** is internal to the keyboard routine.

If combinations of **Alt**, **Ctrl**, and **Shift** are pressed and only one is valid. the priority is as follows:

- **Alt** has the highest priority.
- **Ctrl** is second.
- **Shift** is third.

The only valid combination of **Alt** and **Ctrl** is the **Alt-Ctrl-Del** reset function. For more information, see the section "Reset Handling."

Other Characteristics

The keyboard routine provides its own 16-character buffer. If a key is pressed when the buffer is full, it is ignored and a beep sounds. The keyboard routine also suppresses repeat action of the following:

- **Ctrl**
- **Shift**
- **Num Lock**
- **Scroll Lock**
- **Caps Lock**
- **INS**

Reset Handling

The combination of **Alt**, **Ctrl**, and **Del** results in a keyboard routine that starts a system reset (reboot). Under MAD/ix, it is recommended to shut down the system gracefully using **shutdown(1M)** or **powerdown(1M)** before rebooting the system. See the *System Administrator's Reference Manual* for more information on **shutdown(1M)** and **powerdown(1M)**. To reboot the system after shutting down the system gracefully, either turn the keyswitch to the Reset position or press **Ctrl**, **Alt**, and **Del** simultaneously. You must press **Ctrl**, **Alt**, and **Del** three times in order to reboot the system. The reset is handled by BIOS.

Chapter 4. Keyboard

Introduction

The topics discussed in this chapter are the following:

- Keyboard Communication
- CPU Interface
- Keyboard Connector

The keyboard controller circuits are located on the motherboard. These circuits function as a bidirectional serial interface, passing signals between the keyboard and the CPU (see Figure 4-1).

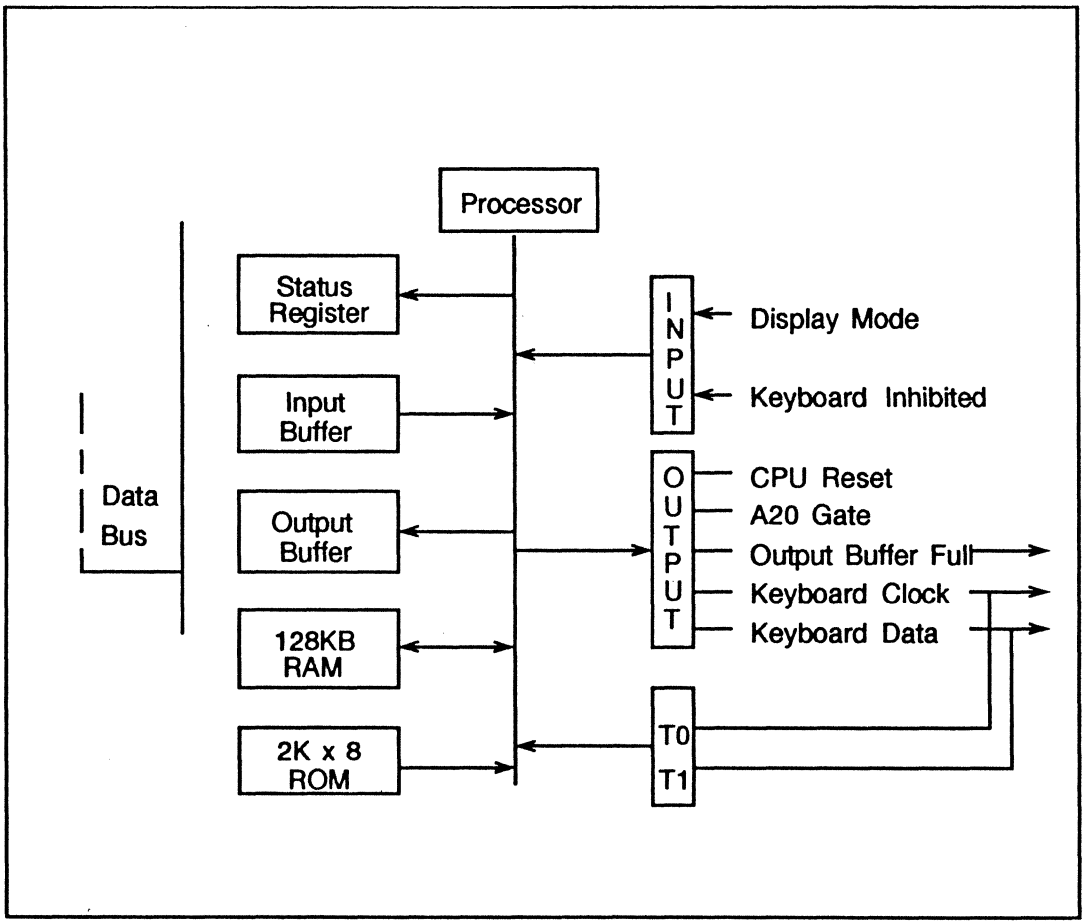

Figure 4-1. Keyboard Controller Block Diagram.

The Intel 8042 8-bit microprocessor, used for the keyboard controller, is programmed to support the enhanced AT keyboard format (see Figure 4-2).

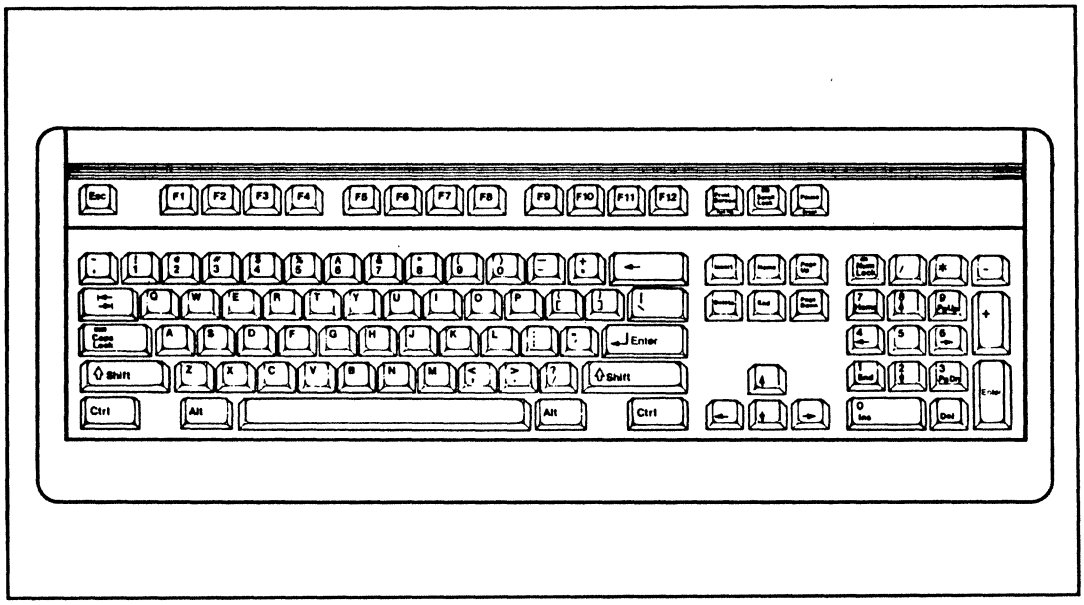

Figure 4-2. Enhanced AT-Type Keyboard Layout

Serial data from the keyboard is parity checked, scan codes are translated, and a byte of data is placed in the output buffer for transfer to the CPU. When data is in the output buffer, the controller interrupts the microprocessor to enable the transfer. The status register bits indicate if an error was detected in the received data.

Data is sent to the keyboard by writing to the keyboard controller input buffer. The byte of data is sent serially to the keyboard, with an odd parity bit automatically inserted. The keyboard must acknowledge all data transmissions. No transmission is sent to the keyboard until acknowledgment is received for the previously sent byte.

Keyboard Communication

The keyboard and its controller exchange commands and data in serial form, synchronized to a clock signal from the keyboard. An 11-bit frame is used:

- One start bit
- Eight data bits
- One odd parity bit
- One stop bit

Receiving Data From the Keyboard

Each time the keyboard sends a byte of data, the controller disables the interface until the computer accepts the byte. If the byte of data is received with a parity error, a Resend command is automatically sent to the keyboard. If the controller is unable to receive the data correctly, a 0xFF is placed in the controller output buffer and the parity bit in the status register is set to 1. The keyboard controller also times a byte of data from the keyboard. If a keyboard transmission does not end within 2 msec, a 0xFF is placed in the keyboard controller output buffer and the receive time-out bit in the status register is set. No retry is attempted on a receive time-out error.

Scan Code Translation

The scan codes received from the keyboard are translated by the keyboard controller into the computer's internal make scan codes. The scan codes are stored in the keyboard controller output buffer. Figure 4-3 lists the scan codes in the scan-code translation table. They are arranged in order of position on the keyboard. Figure 4-3 also lists reserved codes that are translated by the keyboard controller but that are not generated by the keyboard.

Character		Key Number	Make Scan Code for AT and Enhanced AT Keyboards
Shift	Unshift		
~	'		0x00
!	1	1	0xDE
@	2	2	0x16
#	3	3	0x1E
$	4	4	0x26
%	5	5	0x25
^	6	6	0x2E
&	7	7	0x36
*	8	8	0x3D
(	9	9	0x3E
)	0	10	0x46
_	-	11	0x45
+	=	12	0x4E
|	\	13	0x55
BCKSP	BCKSP	14	0x5D
TAB L	TAB R	15	0x66
Q	q	16	0x0D
W	w	17	0x15
E	e	18	0x1D
R	r	19	0x24
T	t	20	0x2D
Y	y	21	0x2C
U	u	22	0x35
I	i	23	0x3C
O	o	24	0x43
P	p	25	0x44
{	[	26	0x4D
}	]	27	0x54
CTRL	CTRL	28	0x5B
		30	0x14

Figure 4-3. Scan Codes Translation, Part 1

Character		Key Number	Make Scan Code for AT and Enhanced AT Keyboards
Shift	Unshift		
A	a	31	0x1C
S	s	32	0x1B
D	d	33	0x23
F	f	34	0x2B
G	g	35	0x34
H	h	36	0x33
J	j	37	0x3B
K	k	38	0x42
L	1	39	0x4B
:	;	40	0x4C
"	'	41	0x52
RETURN	RETURN	43	0x5A
SHIFT	SHIFT	44	0x12
Z	z	46	0x1A
X	x	47	0x22
C	c	48	0x21
V	v	49	0x2A
B	b	50	0x32
N	n	51	0x31
M	m	52	0x3A
<	,	53	0x41
>	.	54	0x49
?	/	55	0x4A
SHIFT	SHIFT	57	0x59
ALT	ALT	58	0x11
SPACE BAR	SPACE BAR	61	0x29
CAPS LOCK	CAPS LOCK	64	0x58

Figure 4-3. Scan Codes Translation, Part 2

Character		Key Number	Make Scan Code for AT and Enhanced AT Keyboards
Shift	Unshift		
F2	F2	65	0x06
F4	F4	66	0x0C
F6	F6	67	0x0B
F8	F8	68	0x0A
F10	F10	69	0x09
F1	F1	70	0x05
F3	F3	71	0x04
F5	F5	72	0x03
F7	F7	73	0x02
F9	F9	74	0x01
ESC	ESC	90	0x76
7	HOME	91	0x6C
4	[left]	92	0x6B
1	END	93	0x69
NUM LOCK	NUM LOCK	95	0x77
8	[up]	96	0x75
5		97	0x73
2	[down]	98	0x72
0	INS	99	0x70
SCROLL LOCK	SCROLL LOCK	100	0x7E
9	PGUP	101	0x7D
6	[right]	102	0x74
3	PGDN	103	0x7A
.	DEL	104	0x71
SYS PRTSC	SYS *	105	0x7F
-	-	106	0x7C
+	+	107	0x7B
		108	0x79

Figure 4-3. Scan Codes Translation, Part 3

Character		Key Number	Make Scan Code for AT and Enhanced AT Keyboards
Shift	Unshift		
		Reserved	0x60
		Reserved	0x61
		Reserved	0x78
		Reserved	0x07
		Reserved	0x0F
		Reserved	0x17
		Reserved	0x1F
		Reserved	0x27
		Reserved	0x2F
		Reserved	0x37
		Reserved	0x3F
		Reserved	0x47
		Reserved	0x4F
		Reserved	0x56
		Reserved	0x5E
		Reserved	0x08
		Reserved	0x10

Figure 4-3. Table of Scan Codes Translation, Part 4

Sending Data to the Keyboard

The keyboard is given 15 msec to start clocking data out of the keyboard controller. Once begun, the clocking function is given 2 msec for completion. If either limit is exceeded, the keyboard controller output buffer is set to 0xFE. The transmit time-out error bit is set in its status register.

The keyboard controller is programmed for a 25 msec time limit within which the keyboard must respond to all transmissions. If the limit is exceeded, the keyboard controller output buffer is set to 0xFE. In addition, the transmit and receive time-out error bits are set in the status register. No retry is made by the keyboard controller for any transmission error. If the keyboard response contains a parity error, the keyboard controller output buffer is set to 0xFE. In addition, the transmit time-out and parity error bits are set in the status register.

Keyboard Interface Inhibit

The key switch on the front panel of the Series 3000 Intelligent Workstation may be used to inhibit the keyboard interface. It has a Power On/Keyboard Off position. However, transmissions to the keyboard are allowed regardless of the state of the switch. The keyboard controller tests data received from the keyboard to determine if the byte received is a command response or a scan code. Command responses are placed in the keyboard controller's output buffer. Scan codes are ignored.

CPU Interface

The CPU and keyboard controller communicate through the following:

- A status register
- An input buffer
- An output buffer
- Input and output ports

Figure 4-4 is an overview of the interface:

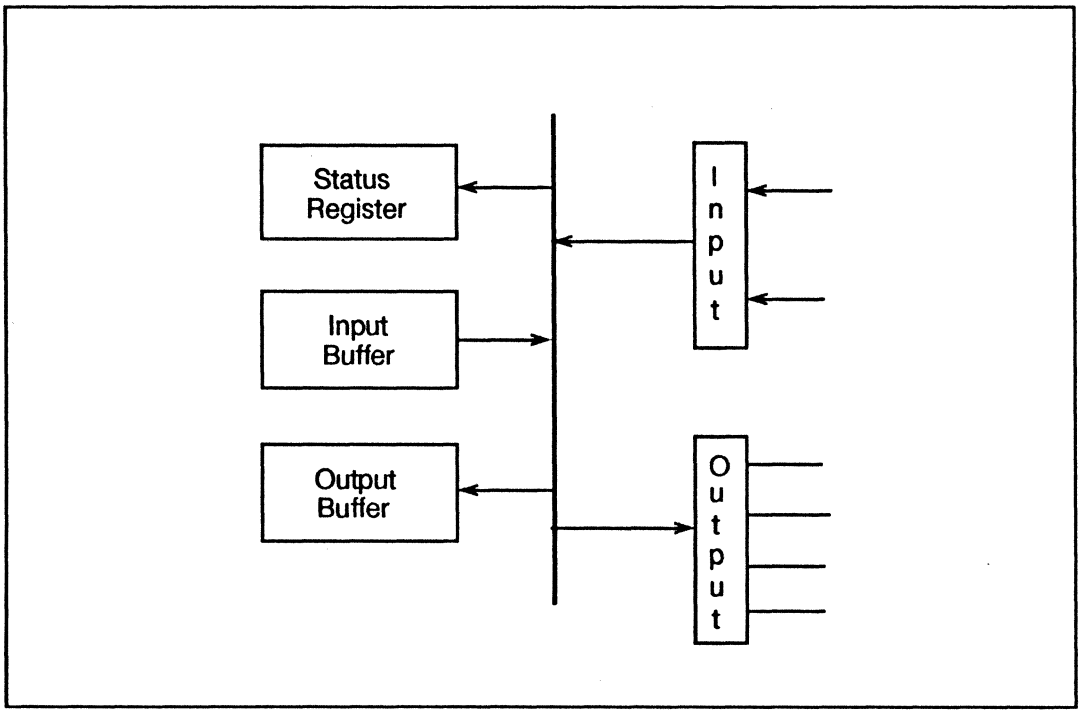

Figure 4-4. Keyboard Interface Overview.

Status Register

The status register is an 8-bit read-only register located at address 0x64 . It can be read by the system at any time. It contains information on the state of

the 8042 keyboard controller and interface. The following bit definitions describe its contents:

- Bit 0 — Output buffer
  - 0 = Output buffer empty.
  - 1 = Output buffer full. The controller has placed data into the output buffer, but the system has not yet read the data.

    This bit returns to 0 when the system reads the output buffer (I/O address 0x60).
- Bit 1 — Input buffer
  - 0 = Input buffer empty (I/O address 0x60 or 0x64).
  - 1 = Input buffer full. Data has been written into the buffer, but the controller has not read the data.

    This bit returns to 0 when the keyboard controller reads the input buffer.
- Bit 2 — System flag

  Bit 2 is set to 0 or 1 by writing to the system's flag bit in the keyboard controller's command byte. After a power-on reset, it is set to 0.
- Bit 3 — Command/Data
  - 0 = Keyboard controller data port. Writing to 0x60 sets this bit to 0.
  - 1 = Keyboard controller command port. Writing to 0x64 sets this bit to 1.

    The keyboard controller's input buffer is addressed as 0x60 or 0x64. The controller uses this bit to determine if the byte in the input buffer is a command byte (0x64) or a data byte (0x60).
- Bit 4 — Inhibit switch

  This is updated whenever data is placed in the output buffer and reflects the state of the keyboard-inhibit switch.
  - 0 = Inhibited
  - 1 = Not inhibited

- Bit 5 — Transmit time-out
  - 1 = Transmission started by the keyboard controller was properly completed.
  - An error only occurs if the transmit byte was not clocked out within the specified time limit.
  - If the transmit byte was clocked out, but a response was not received within the programmed time limit, transmit time-out and receive time-out error bits are both set.
  - If the transmit byte was clocked out but a response was received with a parity error, the transmit time-out and parity error bits are both set.
- Bit 6 — Receive time-out

  1 = Transmission was started by the keyboard but did not finish within the programmed receive time-out delay.
- Bit 7 — Parity Error
  - 0 = Last byte of data received from the keyboard had odd parity. The keyboard should send with odd parity.
  - 1 = Last byte of data received from keyboard had even parity.

Output Buffer

The keyboard controller output buffer is an 8-bit read-only register at I/O address 0x60. This buffer is used to send scan codes received from the keyboard and data bytes requested by command to the system. The output buffer should be read-only when the output buffer's full bit in the status register is 1.

Input Buffer

The keyboard controller input buffer is an 8-bit write-only register at I/O address 0x60 or 0x64. Writing to 0x60 sets a flag in the status register that indicates a data write. Writing to 0x64 sets the status register flag that indicates a command write. Data written to I/O address 0x60 is sent to the keyboard unless the keyboard controller is expecting a data byte following a controller command. Data should be written to the controller's input buffer only if bit 1 is 0 in the status register.

The following commands can be written to I/O address 0x64:

- 20h — Read keyboard controller command byte.

  The keyboard controller sends its current command byte to the output buffer.

- 60h — Write keyboard controller command byte.

  The next byte of data written to I/O address 0x60 is placed in the keyboard controller command byte. Bit definitions are as follows:

  - Bit 7 Reserved (should be a 0).

  - Bit 6 Compatibility mode.

    When this bit is set to 1, the keyboard controller converts scan codes received from keyboard to codes used by the computer. This includes converting a two-byte break sequence to a one-byte format.

  - Bit 5 Computer mode.

    Setting this bit to 1 programs the keyboard to support the computer keyboard interface. In this mode the controller does not check parity or convert scan codes.

  - Bit 4 Disable keyboard.

    Setting this bit to 1 disables the keyboard interface by driving the clock line low. Data cannot be sent or received.

  - Bit 3 Inhibit override.

    Setting this bit to 1 disables the keyboard inhibit function.

  - Bit 2 System flag.

    The value of this bit is written to the system flag bit of the status register.

  - Bit 1 Reserved (should be 0).

  - Bit 0 Enable output-buffer-full interrupt.

    When this bit is set to 1, the keyboard controller generates an interrupt when data is loaded into the output buffer.

- AAh — Self test.

  This instructs the keyboard controller to perform internal diagnostic tests. A 0x55 is loaded into the output buffer if no errors are detected.

- ABh — Internal test.

  This instructs the keyboard controller to test the keyboard clock and data lines. The test result is written to the output buffer as follows:

  - 00 No error detected.
  - 01 The keyboard clock line is stuck low.
  - 02 The keyboard clock line is stuck high.
  - 03 The keyboard data line is stuck low.
  - 04 The keyboard data line is stuck high.

- ACh — Diagnostic dump.

  Sends 16 bytes of controller RAM data, the current state of input and output ports, and the controller program status word to system. All items are sent in scan-code format.

- ADh — Disable keyboard feature.

  Sets bit 4 in the controller command byte to disable the keyboard interface by driving the clock line low. Data cannot be sent or received.

- AEh — Enable keyboard interface.

  Clears bit 4 of the keyboard controller command byte to release the keyboard interface.

- C0h — Read input port.

  This instructs the keyboard controller to read the input port and places the data in the output buffer. This should be used only if the output buffer is empty.

- D0h — Read output port.

  Causes keyboard controller to read the output port and place the data in the output buffer. This should be used only if the output buffer is empty.

- D1h — Write output port.

  This places the next byte of data written to I/O address 0x60 in the keyboard controller's output port.

> **CAUTION**
>
> Bit 0 of the keyboard controller's output port is connected to the system reset. Use extreme caution when writing to this port. This bit should never be set to zero.

- E0h — Read test inputs.

  Causes the controller to read T0 and T1 inputs. This data is placed in the output buffer. Data bit 0 represents T0 and data bit 1 represents T1.

- F0h-FFh — Pulse output port.

  Bits 0 through 3 of the keyboard controller output port can be pulsed low for about 6 msec. Bits 0 through 3 of this command indicate the bits to be pulsed. A 0 indicates that a bit should be pulsed; a 1 indicates that the bit should not be changed.

Input/Output Ports

The controller has two 8-bit output ports and two test inputs. It uses the test inputs to read levels on the keyboard's clock and data lines. One port is used for input and the other for output. Figures 4-5 through 4-7 show the bit definitions for the keyboard controller input, output port, and test input.

Bit	Definition
0	Undefined
1	Undefined
2	Reserved
3	Undefined
4	Undefined
5	Undefined
6	Display Type Switch 0 = Primary display attached to color graphics adapter 1 = Primary display attached to monochrome graphics adapter
7	Keyboard Inhibit Switch 0 = Keyboard inhibit 1 = Keyboard not inhibited

Figure 4-5. Table of Keyboard Controller Input Port Definitions

Bit	Definitions
0	CPU Reset
1	A20 Gate
2	Undefined
3	Undefined
4	Output Buffer Full
5	Undefined
6	Keyboard Clock (Output)
7	Keyboard Data (Output)

Figure 4-6. Table of Output Port Definitions

Port	Definition
T0	Keyboard Clock (Input)
T1	Keyboard Data (Input)

Figure 4-7. Table of Test Input Port Definitions

Keyboard Connector

Figure 4-9 illustrates the 5-pin DIN type shielded keyboard connector. The external keyboard cable is attached to it. The pins are used for keyboard signals. Figure 4-8 lists the pin number assignments. The Vcc pin is protected by a 7A fuse. The cable shielding is connected to two chassis ground pins within the connector.

Pin	Signal	Direction	Description
1	KBDCLK	I/O	Keyboard Clock
2	KBDDATA	I/O	Keyboard Data
3	KBDRST*	OUT	Keyboard Data
4	KBDGND		Logic Ground
5	KBD +5V	OUT	Keyboard Power
* = active low signal			

Figure 4-8. Table of Keyboard Connector J4

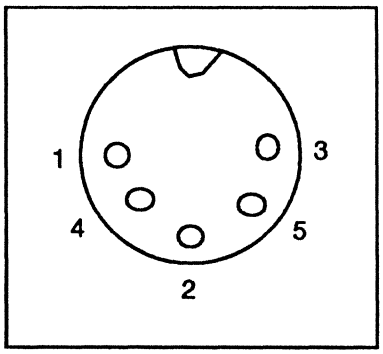

Figure 4-9. Keyboard Connector

Chapter 5. Memory

Introduction

One of the motherboard's eight slots accommodates a 32-bit-data/24-bit-address memory board. The memory board has up to four 32-bit paired banks of dynamic RAM (see Figures 5-1 and 5-2).

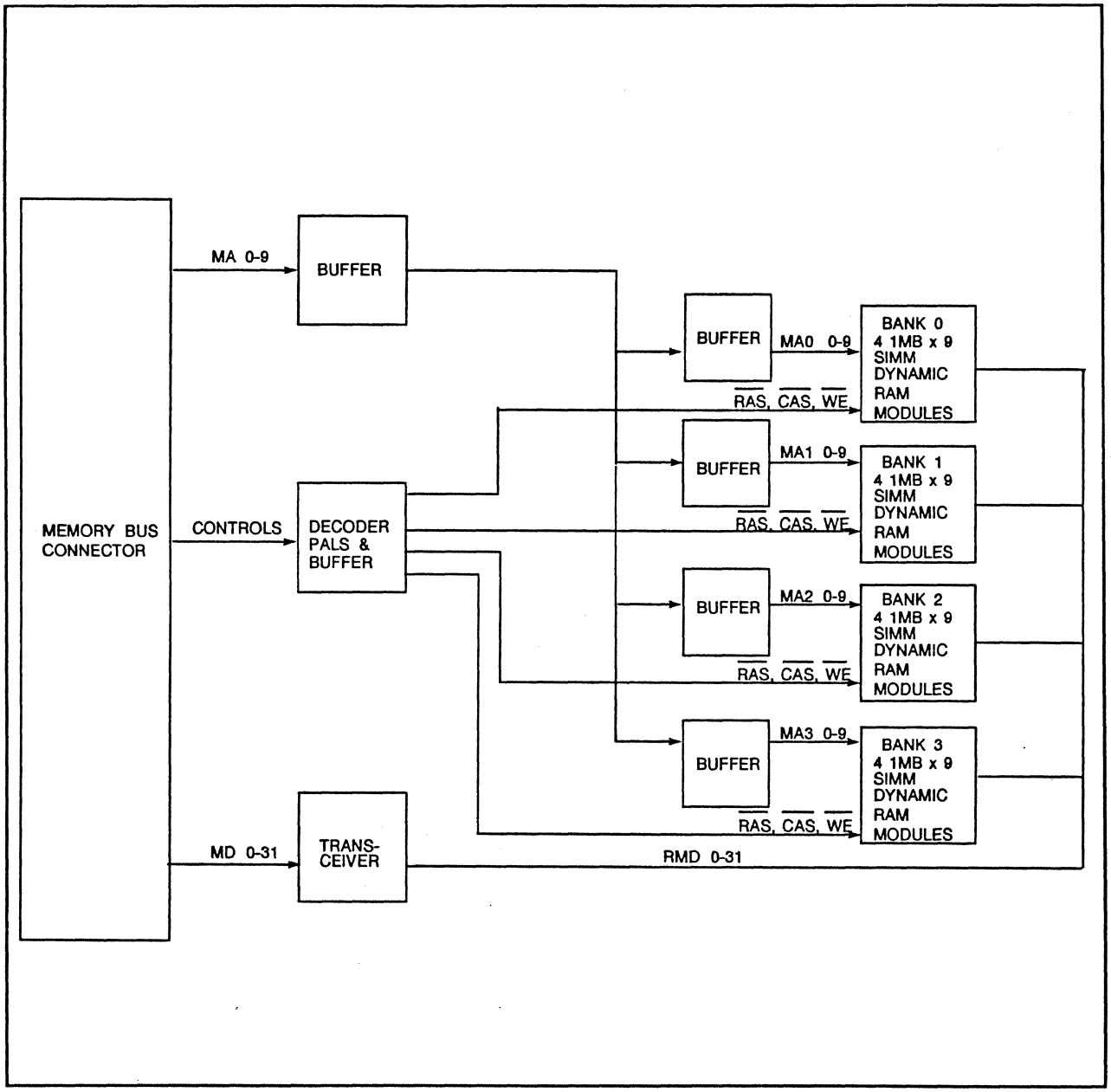

Figure 5-1. Memory Board Block Diagram

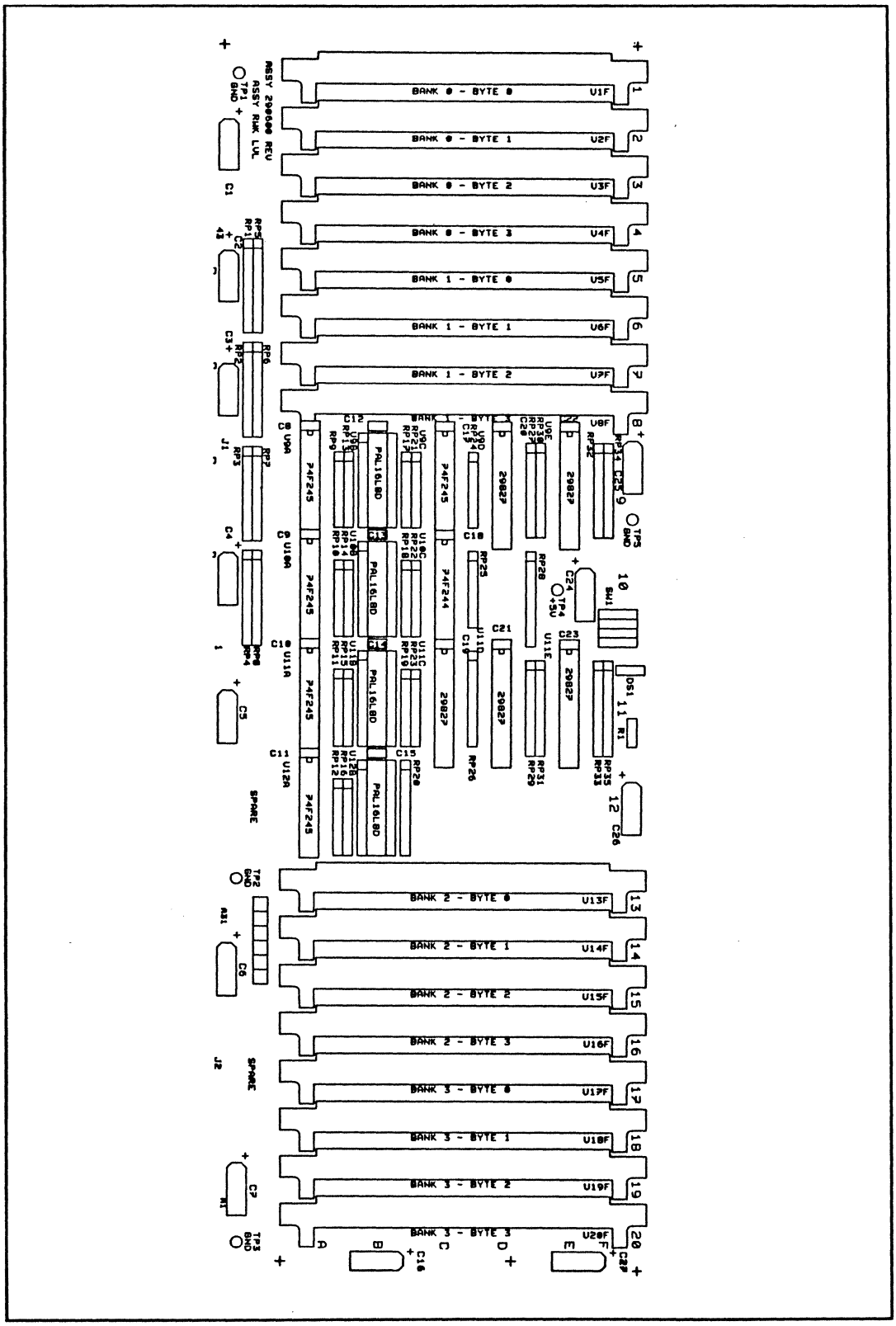

Figure 5-2. Memory Board Component Locations

One, two, or four banks can be used, as shown in Figure 5-3. Each bank contains up to 36 RAM chips (32 for data and 4 for parity) in Single Inline Memory Modules (SIMMs). Nine chips are mounted per SIMM module. Four SIMMs can carry up to 1MB using 256KB chips or up to 4MB using 1MB chips. Sixteen SIMMs can carry up to 4MB using 256KB chips or up to 16MB using 1MB chips.

Bank	1-Bank Option	2-Bank Option	4-Bank Option
0	X	X	X
1		X	X
2			X
3			X

Figure 5-3. Table of Bank-Stuffing Options

Banks must be added in pairs (0-1 and 2-3). Each pair of banks can use either 256KB x 9 or 1MB x 9 modules. A minimal system can be configured with only one bank. However, a 1-bank option results in slower performance because bank interleaving is disabled and one wait-state is automatically inserted in each memory cycle. Figure 5-4 shows the memory chip options that can be used for stuffing the board to a given memory size.

Memory interleaves within bank pairs at every 2KB of address space, as shown in Figure 5-5.

Memory Size	Bank Times Chip Type
1MB	1 X 256KB
2MB	2 X 256KB
4MB	4 X 256KB or 1 X 1MB
8MB	2 X 1MB
10MB	2 X 1MB plus 2 X 256KB
16MB	4 X 1MB

Figure 5-4. Table of Memory Chip Options

Bank	Memory Address Range
0	0K to 2K
1	2K to 4K
0	4K to 6K
1	6K to 8K
.	.
.	.
.	.

Figure 5-5. Table of Memory Interleaving

For 16 MHz no wait-state operation, the RAM must have an access time of 100 nsec. For 16 MHz one wait-state operation, 120 nsec RAMs can be used.

For 20 MHz no wait-state operation, the RAM must have an access time of 80 nsec. For 20 MHz one wait-state operation, 100 nsec RAMs can be used.

RAM refresh is requested every 15 microseconds through the motherboard's timer/counter (channel 1). On-board and I/O expansion RAM are initialized as follows:

- Initialize channel 1 of the motherboard timer/counter to the rate-generation mode with a period of 15 microseconds.
- Write to every memory location.

Switches, Connectors, LEDs and Test Points

The topics covered in this section are the following:

- Switches
- Connectors
- LEDs
- Test Points

Switches

The memory board has a 4-bit DIP switch, SW1. SW1 enables the board's address space (see Figure 5-6).

Bit				
1	2	3	4	Board Status
Off	X	X	X	Disabled
On	On	On	X	Enabled *
On	Off	On	X	Reserved
On	On	Off	X	Reserved
On	Off	Off	X	Reserved
X = Don't care				
* Factory Setting				

Figure 5-6. Table of Switch SW1

Connectors

There are two connectors on the memory board. J1 corresponds to the J200 connector on the motherboard. J2 corresponds to the J114 connector on the motherboard. Figure 5-7 (parts 1 through 3) illustrates the J1 Memory Bus Connector pin assignments and signals. Figure 5-8 illustrates the J2 I/O Expansion Bus pin assignments and signals. An asterisk (*) following a signal name indicates active low.

Pin	Signal	Direction	Description
1	GND		Logic Ground
2	MA0	IN	Memory Address Bit 0
3	MA2	IN	Memory Address Bit 2
4	MA4	IN	Memory Address Bit 4
5	MA6	IN	Memory Address Bit 6
6	+5V		Logic Power
7	MA8	IN	Memory Address Bit
8	MA10	IN	Memory Address Bit (Unused)
9	BA1	IN	Block Address Bit
10	DRD*	IN	Low for Reading Memory
11	GND		Logic Ground
12	LBE0*	IN	Latch Byte Enable 0
13	LBE2*	IN	Latch Byte Enable 2
14	Reserved		Reserved
15	RAS0*	IN	Row Address Strobe
16	+5V		Logic Power
17	RAS2*	IN	Row Address Strobe for Bank 2
18	Reserved		Reserved Cache Version
19	CAS0*	IN	Column Address Strobe Bank 0
20	CAS2*	IN	Column Address Strobe Bank 2
21	GND		Logic Ground
22	MD0	I/O	Memory Data Bit 0
23	MD2	I/O	Memory Data Bit 2
24	MD4	I/O	Memory Data Bit 4
25	MD6	I/O	Memory Data Bit 6
26	+5V		Logic Power
27	MP0	I/O	Memory Parity Bit 0
28	MD9	I/O	Memory Data Bit 9
29	MD11	I/O	Memory Data Bit 11
30	MD13	I/O	Memory Data Bit 13

Figure 5-7. Table of DRAM Bus Connector J1, Part 1

Pin	Signal	Direction	Description
31	GND		Logic Ground
32	MD15	IN	Memory Data Bit 15
33	MD16	IN	Memory Data Bit 16
34	MD18	IN	Memory Data Bit 18
35	MD20	IN	Memory Data Bit 20
36	+5V		Logic Power
37	MD22	IN	Memory Data Bit 22
38	MP2	IN	Memory Parity Bit 2
39	MD25	IN	Memory Data Bit 25
40	MD27	IN	Memory Data Bit 27
46	MA3		Memory Address Bit 3
47	MA5	IN	Memory Address Bit 5
48	MA7	IN	Memory Address Bit 7
49	GND		Logic Ground
50	MA9	IN	Memory Address Bit 9
51	BA0		Block Address Bit 0
52	FBK*	IN	Force All Banks Enable for Refresh
53	DWE*		DRAM Write Strobe
54	+5V	IN	Logic Power
55	LBE1•	IN	Latch Byte Enable 1
56	LBE3*		Latch Byte Enable 3
57	DBEN*	I/O	Memory Data Buffer Enable
58	RAS1*	I/O	Row Address Strobe for Bank 1
59	GND	I/O	Logic Ground
60	RAS3*	I/O	Row Address Strobe for Bank 3
61	Spare		
62	CAS1*	I/O	Column Address Strobe Bank 1
63	CAS3*	I/O	Column Address Strobe Bank 3
64	+5V	I/O	Logic Power
65	MD1	I/O	Memory Data Bit 1
66	MD3		Memory Data Bit 3

Figure 5-7. DRAM Bus Connector J1, Part 2

Pin	Signal	Direction	Description
67	MD5	I/O	Memory Data Bit 5
68	MD7	I/O	Memory Data Bit 7
69	GND		Logic Ground
70	MD8	I/O	Memory Data Bit 8
71	MD10	I/O	Memory Data Bit 10
72	MD12	I/O	Memory Data Bit 12
73	MD14	I/O	Memory Data Bit 14
74	+5V		Logic Power
75	MP1	I/O	Memory Parity Bit 1
76	MD17	I/O	Memory Data Bit 17
77	MD19	I/O	Memory Data Bit 19
78	MD21	I/O	Memory Data Bit 21
79	GND		Logic Ground
80	MD23	I/O	Memory Data Bit 23
81	MD24	I/O	Memory Data Bit 24
82	MD26	I/O	Memory Data Bit 26
83	MD28	I/O	Memory Data Bit 28
84	MD30	I/O	Memory Data Bit 30
85	MP3	I/O	Memory Parity Bit 3
86	+5V		Logic Power

Figure 5-7. Table of DRAM Bus Connector J1, Part 3

Pin	Signal	Direction	Description
B1	GND		Ground
B3	+5V	In	Power
B10	GND		Ground
B29	+5V	In	Power
B31	GND		Ground

Figure 5-8. Table of I/O Expansion Bus J2

LEDs

There is one LED on the memory board. It is always on as long as the board is functioning properly. Figure 5-9 illustrates the LED.

State	Description
On	Normal Operation
Off	Abnormal Operation

Figure 5-9. Table of Memory Board LED (DS1)

Test Points

Figure 5-10 lists the Series 3000 Intelligent Workstation's memory board's test points.

Point	Description
TP1	Ground
TP2	Ground
TP3	Ground
TP4	+5V
TP5	Ground

Figure 5-10. Table of Memory Board Test Points

Installation

The memory board plugs into the J200 and J114 slots on the motherboard. Figure 5-11 shows the SIMM module sockets that correspond to bank numbers.

Bank	Socket
0	U1F - U4F
2	U5F - U8F
3	U13F - U16F
4	U17F - U20F

Figure 5-11. Table of Memory Module Sockets and Banks

Chapter 7. Power Supply

Introduction

The power supply module provides DC power for the motherboard, the expansion boards, the disk drives, and the keyboard. The module is enclosed in a chassis near the rear of the unit. The power supply module can be switched between 120 VAC and 240 VAC. Its power rating is 220W (nominal) and 250W (peak). Figure 7-1 is a power supply block diagram.

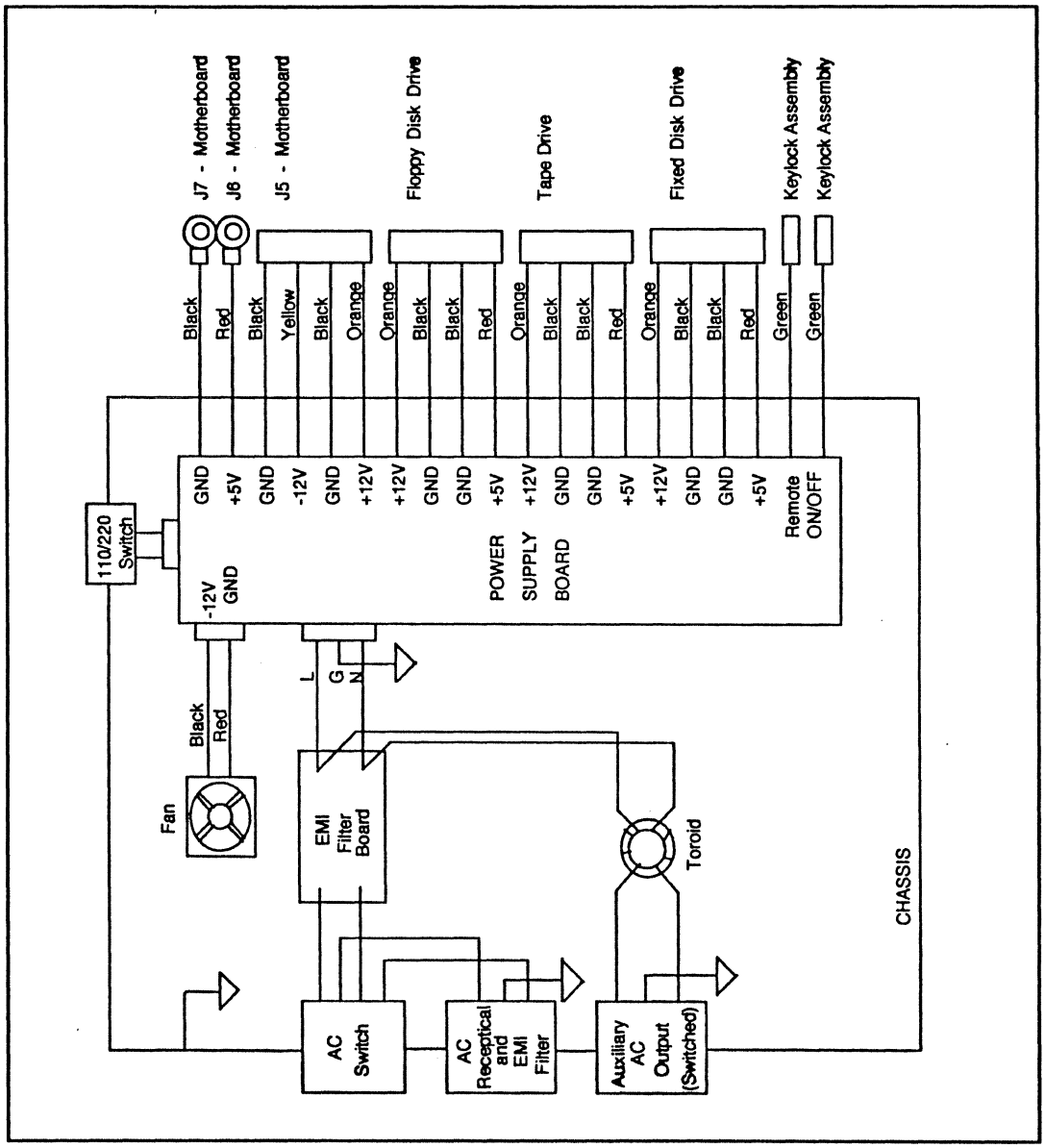

Figure 7-1. Power Supply Block Diagram

Changing the Voltage

The Series 3000 Intelligent Workstation is factory-wired for a line voltage of 120 VAC or 240 VAC. To change the voltage selection switch, follow these steps:

1. Open the system unit.
   - Turn off the power at the system unit's main power switch.
   - Disconnect the power cord.
   - Turn off the key switch and remove the key.
   - Remove the four screws on the rear panel (two on each side) that hold the cover assembly onto the chassis.
   - Slide the top cover toward the front to remove it.
2. The 120/240 voltage selection switch is located on the top of the power supply chassis near the fan. It is covered with an opaque label.
3. Change the voltage selection switch.
4. Close the system unit.

If you are using a MAD monitor, change the voltage on the monitor.

1. Locate the 120/240 switch at the far right of the monitor.
2. Using a pen point, change the setting.

The following over-voltage protections are provided:

- +5V output falls at 7V (maximum).
- +12V output falls at 13.5V (maximum).

Over-power protection is provided on all outputs.

The power supply requires a minimum load for proper operation. If primary power is applied with no load on a power supply, voltage regulation does not remain within tolerance.

Input

The Series 3000 Intelligent Workstation can operate at line frequencies between 47 Hz and 63 Hz. The maximum inrush current is 25A for 120V input or 30A for 220V input.

The Series 3000 Intelligent Workstation's input requirements are listed in Figure 7-2.

Range	Voltage VAC	Current A	Frequency Hz
120	Minimum 90	Maximum 5	Minimum 47
	Maximum 137		Maximum 63
240	Minimum 180		Minimum 47
	Maximum 259		Maximum 63

Figure 7-2. Table of Input Requirements

Output

The power supply furnishes +5 VDC, +12 VDC, and -12 VDC. Figure 7-3 lists the load current and regulation tolerance for the DC voltages.

Nominal Output	Load Current		Regulation	Ripple
	Min.	Max.		
+5 VDC	2.5A	22A	+ OR - 3%	40mV
+12 VDC	0A	9A	+ OR - 3%	40mV
-12 VDC	0A	0.3A	+ OR - 3%	80mV

Figure 7-3. Load Current and Regulation Tolerance

Initial delay time at nominal full load is 200 msec (maximum). Rise time is 70 msec (maximum). Total time to regulation is 270 msec (maximum). Holdup time is 16 msec (minimum). Transient recovery time is 1 msec (maximum) of steady state after a load change of 50% within the range of 50% to 100% of full load; transient overshoot is 4% (maximum) in the same range. The temperature effect on output is 0.2% per degree C (maximum).

Figure 7-4 shows voltages and pins for motherboard connector J5.

Pin	Signal	Direction	Description
1	GND		Ground
2	-12V	IN	Power for -5V Regulator Bus
3	GND		Ground
4	+12V	IN	Power for Bus

Figure 7-4. Motherboard Connector J5 for Power Supply

Power supply connector J6 is Vcc (+5V) logic power, and power supply connector J7 is logic ground.

Appendix A. Product Specifications

System Unit

- Motherboard with 80386 microprocessor, support circuitry, and eight expansion slots, including one memory slot
- Space for two half-height 5.25" removable-media devices
- Space for one full-height 5.25" fixed media device
- Power supply
- Key switch with power on, reset, and keyboard disable positions
- Metal housing for compliance with international emission and safety standards

Motherboard

- 80386 microprocessor
- 24-bit address bus and 16-bit data bus
- Seven DMA channels
- 16 interrupts
- Three programmable timers
- 1MB to 16MB RAM (24-bit address bus and 32-bit data bus)
- Eight expansion slots:
  - Six 16-bit slots
  - Two 8-bit slots (one with 32-bit memory board connector)

- ROM BIOS:
  - Power-on diagnostics
  - Boot loader
  - I/O support
  - Setup Utility
- Keyboard interface:
  - 5-pin DIN connector
  - PC/AT and PC/AT-E compatible
- Real-time clock/calendar chip with battery backup
- Speaker

Memory

- 8MB or 16MB DRAM using 1Mb DRAM
- 32-bit memory data bus

Hard Disk Drive

- Full-height, 5-1/4"
- Winchester type
- Storage capacities from 72MB to over 300MB

Disk Controller Board

- Supports two floppy disk drives
- Supports two hard disk drives

Floppy Disk Drives

- Half-height, 5-1/4"
- High density (1.2MB) or low density (360KB)

Streaming Tape Backup Subsystem

- 60MB (approximate) capacity using DC600A cartridge

Advanced Graphics Controller

- Native graphics mode:
  - 640 x 480 (256 colors from a 4096 palette)
  - 1280 x 1024 (4 colors from a 4096 palette)
- Native character mode with downloadable fonts:
  - 132 x 64 characters, 8 x 16 character cell, 16 colors
  - 132 x 128 characters, 8 x 8 character cell, 16 colors

Input/Output

- Serial: One RS-232-C compatible serial port. Baud rates from 110 to 19,200
- Parallel: One Centronics-compatible parallel port

Power Supply

- 220 watts
- 50 Hz or 60 Hz
- 110 VAC or 220 VAC
- AC monitor outlet
- Low-noise DC fan

Supported Operating Systems

- MAD/ix
- MS-DOS

MAD Software

- ROM BIOS with built-in setup utility
- Customer engineer diagnostics

Back Panel Connectors

- J200 — keyboard
- J201 — AC power input
- J202 — monitor power
- J209 — mouse (serial port)
- J210 — printer (parallel port)

Physical Dimensions

- 6.10 inches (15.49 cm) high
- 16.25 inches (41.30 cm) wide
- 17.00 inches (43.18 cm) deep

Operating Environment

- Temperature: 10 to 40 C (50 to 104F)
- Humidity: 20% to 80%

System Weight

- 47 lbs (21 Kg)

Options

Numeric Coprocessor

- Optional 80387 or 80287

AGC PVE Board

- Window emulation graphics mode

  A window created in a 1K x 1K display area supports the following:

  – 640 x 200 CGA graphics mode

  – 320 x 200 CGA graphics mode

- Window emulation character mode

  A window created in a 1K x 1K display area supports the following:

  – 80 x 25 x 16 color CGA character mode

  – 40 x 25 x 16 color CGA character mode

  – 80 x 25 x 2 level MDA character mode

1 Serial/1 Parallel I/O Controller

- One asynchronous RS-232-C serial port
- One Centronics-compatible parallel port
- 300 to 19,200 serial-port baud rate, software selectable
- 9-pin D male connector for serial port
- 25-pin D female connector for parallel port

Index

Numerics

A

B

C

D

N

O

P

R

S

T

V

W

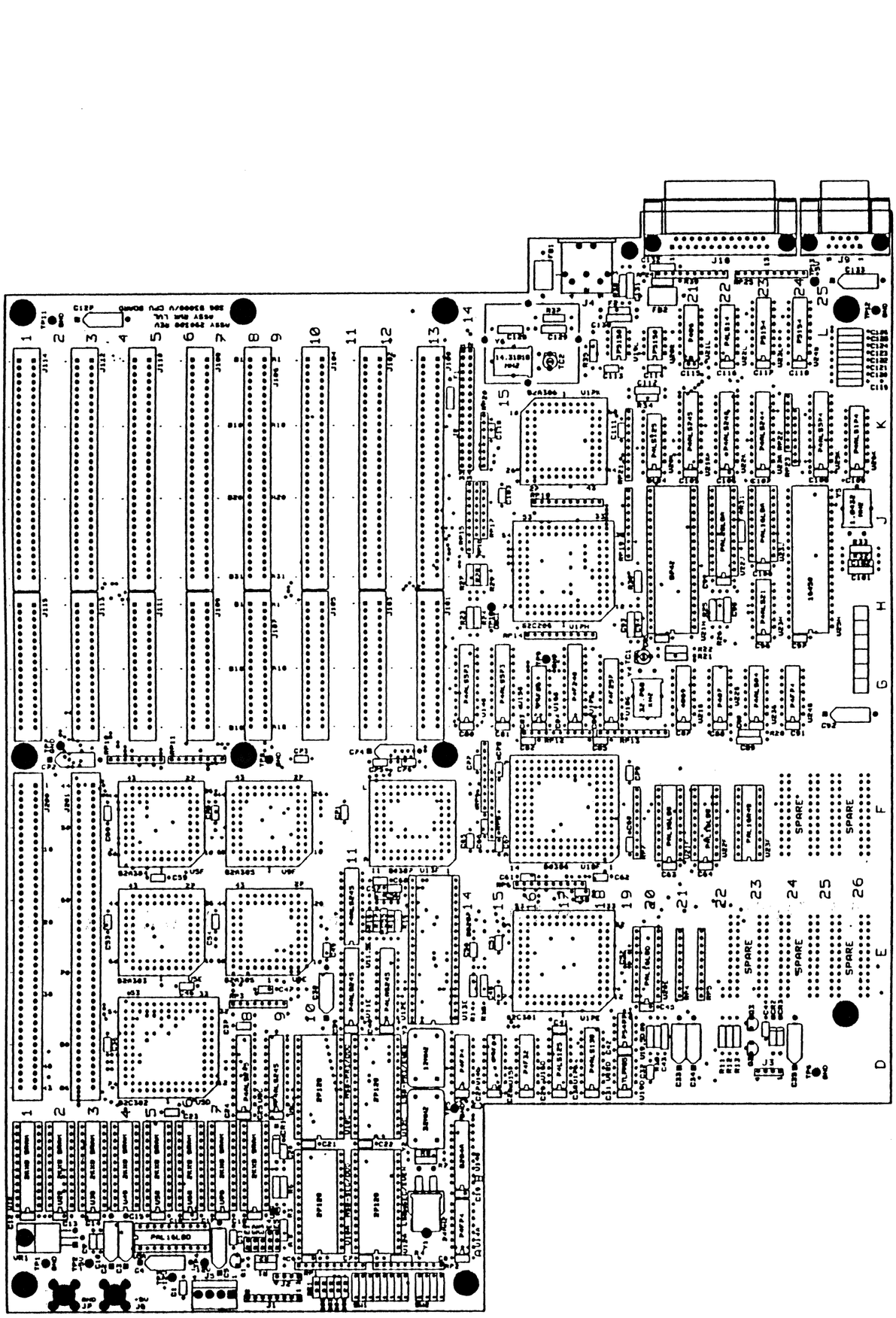

Figure 2-2. Motherboard Assembly

Figure 2-1 Motherboard Block Diagram