HARDWARE REFERENCE MANUAL

For the Ω2000-Series Graphics Controller

004-03307-00

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Revision Number	Revision History	Date
-00	First Issue. Describes the following Ω2000-Series Graphics Controllers: Ω2300s and Ω2400s with graphics preprocessor firmware version 1.0 and display processor microcode version 3.6. Ω2500s with graphics preprocessor firmware version 1.0 and display processor microcode version 2.5.	2/85

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SERVICE INFORMATION

Contact the Graphics System Service Center (GSSC) when you need any Metheus graphics system repaired, replaced, or upgraded. This includes both hardware and firmware products. Following these simple instructions when you call or write will insure the quickest possible response to your request.

(1) You must provide these three items of information when you call or write to the service center:

Model Number
Serial Number
Purchase Order Number

Model numbers and serial numbers are marked on the exterior chassis of packaged products, on the board artwork, or on the firmware. The purchase order number authorizes the service center to charge for services. The service center can also provide the latest upgrade and service contract costs.

(2) Obtain a Return Authorization (RA) number from the service center BEFORE sending any equipment. Use this number in all correspondence.

Contact the Service Center at this address:

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Preface

This manual describes the architecture, operation, and installation of the METHEUS Ω2000-Series Multiprocessor Graphics Controllers (referred to throughout this manual as graphics controllers). The information provided in this manual is intended primarily for engineers and technicians who must incorporate and maintain the Ω2000-Series products in computer graphics systems. It assumes a basic knowledge of computer science and computer graphics concepts.

SUMMARY OF CHAPTERS

Chapter 1	Introduces the architecture of the graphics controllers.
Chapter 2	Provides operating instructions and troubleshooting information.
Chapter 3	Contains installation instructions and procedures for setting configuration options.
Appendix A	Lists electrical, mechanical, environmental, and functional specifications.
Appendix B	Contains an internal interconnection diagram and lists connector pin assignments for the back panel I/O connectors.

RELATED PUBLICATIONS

The following publications contain information related to the subjects covered in this manual. Publications with an order number listed may be ordered from Metheus.

Programmer's Reference for the Ω2000-Series Multiprocessor Graphics Controller, Order number 004-03308

Ω300 and Ω400 Display Controller Reference Manual, Order number 091-02808

Ω500 Display Controller Reference Manual, Order number 091-02869

DR11-W Direct Memory Interface Module User's Guide, Digital Equipment Corporation

9111A Graphics Table User's Manual, Hewlett-Packard Corporation

Digi-Pad 5 User's Manual, GTCO Corporation

Bit Pad One User's Manual, Summagraphics Corporation

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Chapter 1
Architectural Overview

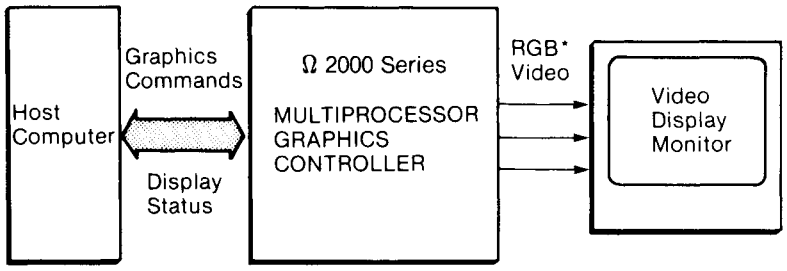
This chapter describes the Ω2000-Series Graphics Controller family. It discusses the way in which the controllers fit into a system and explains the differences between the various members of the family. It also describes the graphics controller architecture and the various options available.

PRODUCT DESCRIPTION

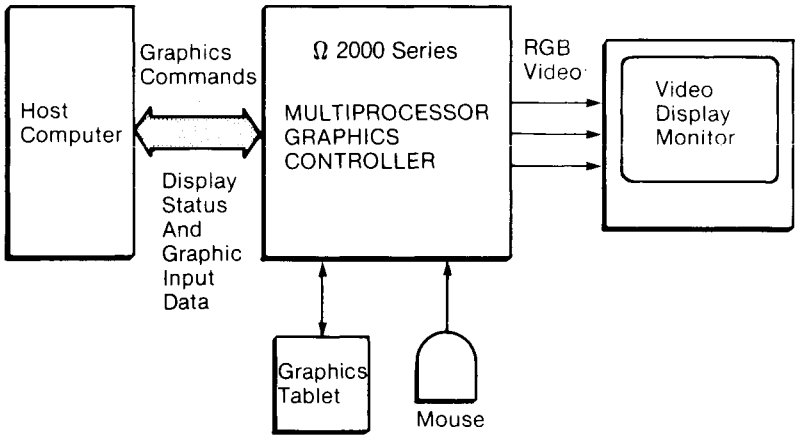
The Ω2000-Series Graphics Controllers translate graphics commands from computer systems into the video signals necessary to produce high-resolution color graphics displays. Each member of the family has a variety of display resolution options and I/O ports that permit it to be configured to different host computers and applications requirements.

Figure 1-1 shows three examples of graphics display systems using the Ω2000-Series Graphics Controllers. Shown at the top of the figure is a simple display-only system, typically with a direct 16-bit parallel connection to the host. The second system is interactive, produced by adding a graphic input device to the graphics controller. Shown at the bottom of the figure is a system in which the graphics controller is equipped with a keyboard, emulating a computer graphics display terminal.

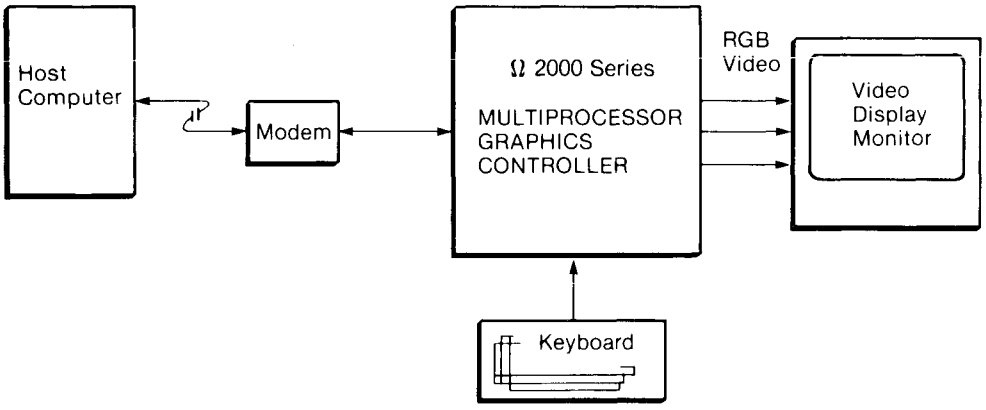
Table 1-1 lists the principal features of the various graphics controllers and explains the differences among them.



BASIC GRAPHICS DISPLAY SYSTEM



GRAPHICS DISPLAY SYSTEM WITH GRAPHICS INPUT



GRAPHICS DISPLAY SYSTEM WITH TERMINAL EMULATION

* Red Green Blue Video

F-0116

Figure 1-1. Example Ω2000-Series Systems

Table 1-1. Comparing Graphics Controller Families

Characteristic	Ω2000-Series Family		
	Ω2300	Ω2400	Ω2500
Resolution	1024x768 @ 33Hz or 736x552 @ 60 Hz or 640x480 with RS-170 or (Ω2305 only) 1024x1024 @ 30Hz	1024x768 @ 33Hz or 736x552 @ 60Hz or 640x480 with RS-170 or (Ω2445 only) 1024x1024 @ 30Hz	1280x1024 @ 60Hz (normal) or 640x512 @ 60Hz (folded)
Bit planes	4	8	8 (normal) 32 (folded)
Color Range	16 colors from a palette of 16.7 million colors	256 colors from a palette of 16.7 million colors	256 colors from a palette of 16.7 million (normal); full 16.7 million (folded)
Drawing Processor	220-nsec cycle	220-nsec cycle	167-nsec cycle
Drawing Speed			
Vectors (pixels/sec)	1.0 million	1.0 million	1.5 million
Characters (pixels/sec)	1.0 million	1.0 million	1.5 million
Polygon Fill			
Solid (pixels/sec)	1.0 million	1.0 million	1.5 million
Pattern (pixels/sec)	1.0 million	1.0 million	1.5 million
FLASH-fill (pixels/sec)	16 million	16 million	30 million
PIXBLT (pixels/sec)	0.33 million	0.33 million	1.5 million
Raster Ops	Not provided	Not provided	XOR, OR, AND, PLUS, MINUS
Pan	Pixel by pixel (except at 1X zoom: 16 pixel increments in horizontal axis)	Pixel by pixel, (except at 1X zoom: 16 pixel increments in horizontal axis)	16 pixel increments in the vertical axis, 40 pixel increments in the horizontal axis
Zoom	Integer zoom, 1X through 16X	Integer zoom, 1X through 16X	Not provided

GRAPHICS CONTROLLER ARCHITECTURE

Figure 1-2 is block diagram of the Ω2000-Series Graphics Controllers, showing the major components and their functional relationship to one another. As the diagram shows, there are two major components:

- *Display processor*, which generates and stores bit patterns that represent video displays, and generates video signals that drive the display monitor. The display processor receives its instructions from the graphics preprocessor.
- *Graphics preprocessor*, which interprets high-level instructions from the host computer, such as those defined in the Graphical Kernel System (GKS) standard, translating the high-level commands into the more primitive instruction set of the display processor.

Display Processor

As shown in Figure 1-2, the display processor's architecture is based upon the following major functional blocks:

- Drawing processor, which responds to host commands, processes data from peripherals, generates displays, and generally oversees display processor operation.
- Pixel memory, which stores pixel data for the display.
- Pixel memory controller, which controls access to pixel memory.
- Video generator, which converts data from pixel memory into analog video signals for driving a video display monitor.

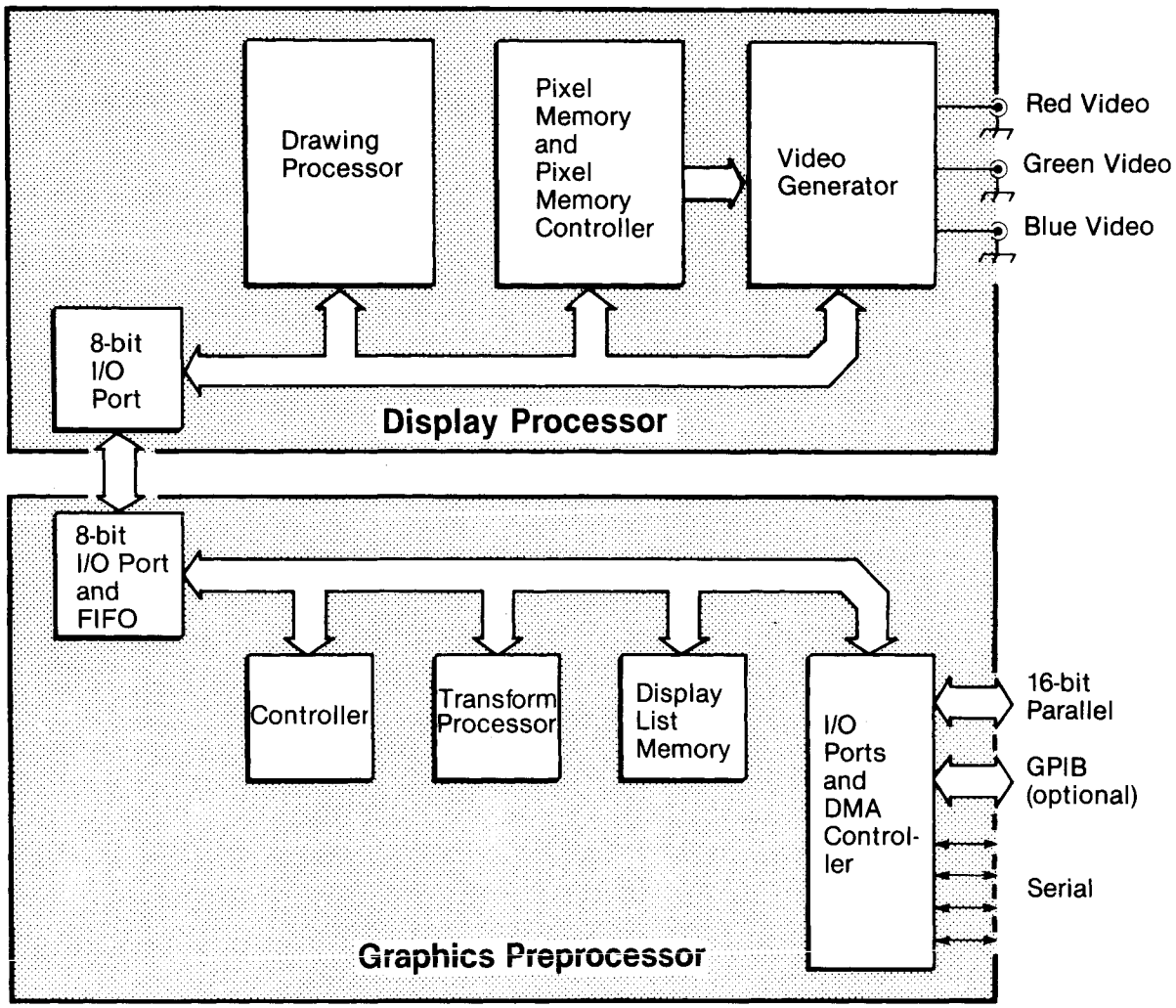


Figure 1-2. Graphics Controller Block Diagram

Drawing Processor

The drawing processor is a 12-bit, bipolar, bit-slice processor with an instruction set designed specifically for generating graphic displays. The primary function of the drawing processor is to respond to graphics commands from the host computer. In executing the graphics commands, the drawing processor creates and stores the necessary bit patterns for graphics primitives such as vectors, arcs, and polygons that form the basis of graphics displays.

As the block diagram in Figure 1-3 shows, the drawing processor consists of the following functional blocks:

- o Arithmetic/Logic unit (ALU)
- o Microprogram ROM
- o Pipeline register
- o Sequencer
- o Data bus source and destination decoder

ALU. The ALU executes arithmetic and logical operations for the drawing processor. It consists of three high-speed, bipolar, 4-bit microprocessor "bit slices" acting in parallel to process 12-bit operands. Operands pass to and from the ALU by way of the 12-bit main data bus. The sources and destinations of the operands are selected in response to condition inputs to the microprogram sequencer, which come from various parts of the Display Processor.

Microprogram ROM. The microprogram ROM is a 64-bit by 2048 word array of PROM containing sequences of microinstructions that make up the drawing processor's instruction set. In addition to controlling the operation of the ALU, many of the bits in the microinstruction word directly assert control lines to various devices throughout the display processor. This direct control over display processor operations allows the drawing processor, for example, to directly write pixel data for a vector into pixel memory at the same time as it is calculating the bit pattern necessary for that vector, thereby increasing drawing speed. A microinstruction word is divided into several fields:

- o Control field, whose bits drive various display processor control signals.
- o Conditional branching field, which directs the flow of microprogram execution.
- o Data bus source and destination field, which directs the flow of data over the data bus.
- o ALU control field, which selects operation type (add, compare, etc.), register addresses, and other ALU functions.
- o Immediate data field, which, for example, supplies constants to the ALU and initialization values to other devices on the data bus.

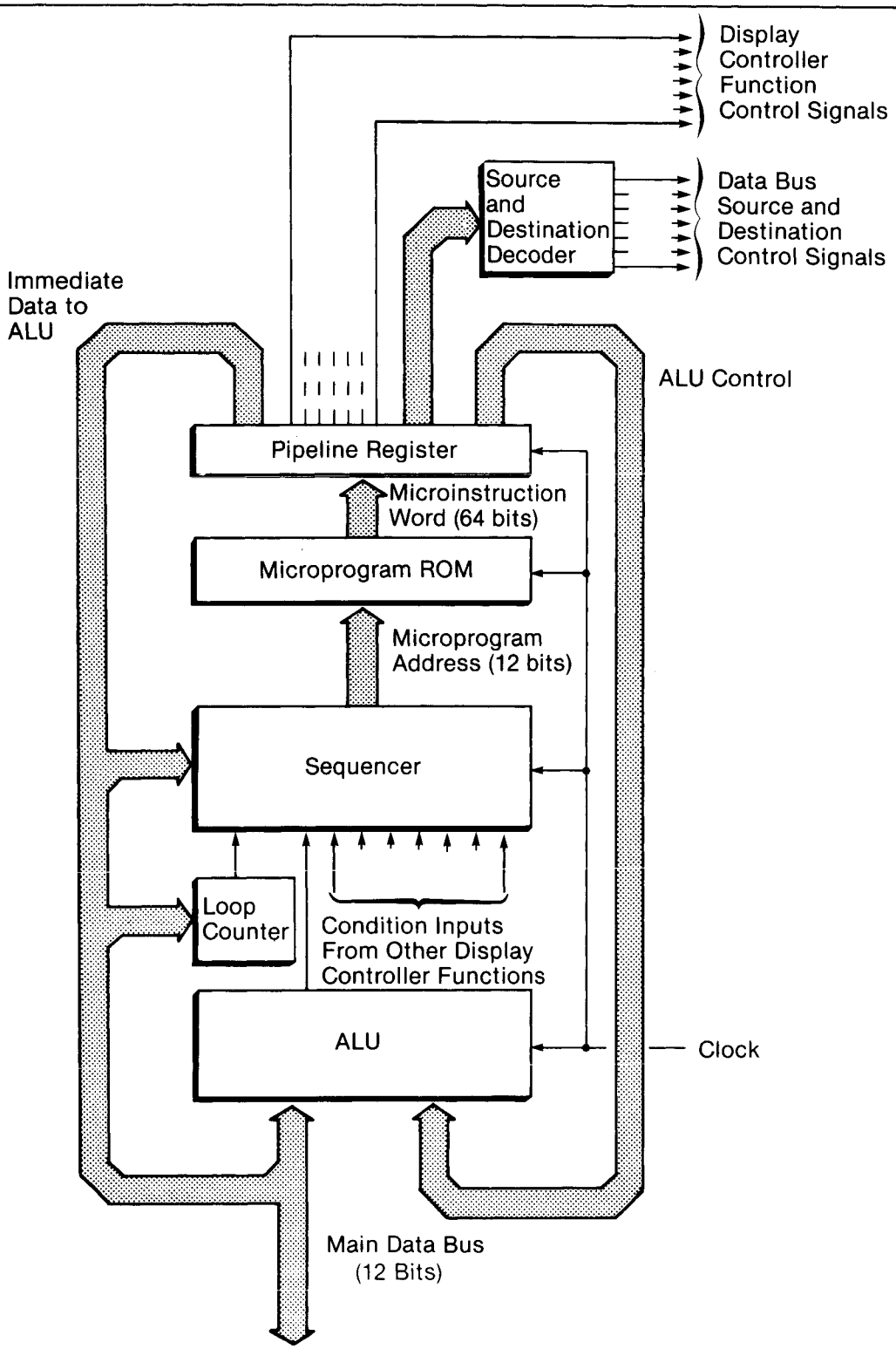


Figure 1-3. Drawing Processor Block Diagram

Pipeline Register. The purpose of the pipeline register is to allow overlapped fetching of microinstructions from the ROM. On every processor clock cycle, the pipeline register latches a new microinstruction word from the microprogram ROM. While one microinstruction is driving control lines from the pipeline register outputs, the next instruction is being fetched from ROM. This increases execution speed since it effectively eliminates ROM access time.

Sequencer. The sequencer supplies microprogram addresses to the microprogram ROM. Address generation is a dynamic process, dependent on many factors: condition inputs from different display processor functions, host instructions, and ALU operations are all factors in determining the next microprogram address in the execution sequence. The sequencer advances to the next address as the instruction selected by the previous address is being executed.

Pixel Memory

Figure 1-4 is a diagram showing the organization of the pixel memory array. As the diagram shows, the array is divided into either four (Ω2300s) or eight planes (Ω2400s and Ω2500s), each plane consisting of either sixteen (Ω2300s and Ω2400s) or twenty (Ω2500s) 64K by 1-bit dynamic RAMs (1 megabit or 1.3 megabits total per plane).

As the drawing processor receives and acts upon graphics commands from the host, it stores (via the pixel memory controller) the bit patterns required to create the specified display in pixel memory. The data in memory forms a bit map of the display; that is, each pixel of the display corresponds to a set of data bits, one bit in each plane of the memory.

To generate the video representation of the bit map on the display monitor, the pixel memory controller extracts a steady stream of pixel data from the memory array, sending it in parcels of 16 (or 20) bits at a time from each memory plane to the video generator.

From the pixel memory controller, each plane of the display memory receives the following:

- 16-bit multiplexed address
- Row and column address strobes
- One bit of input data
- Write enable signal

The address, address strobes, and data input are common to all chips on the plane; each device has a unique write enable and data output. Memory operations are described in the following section.

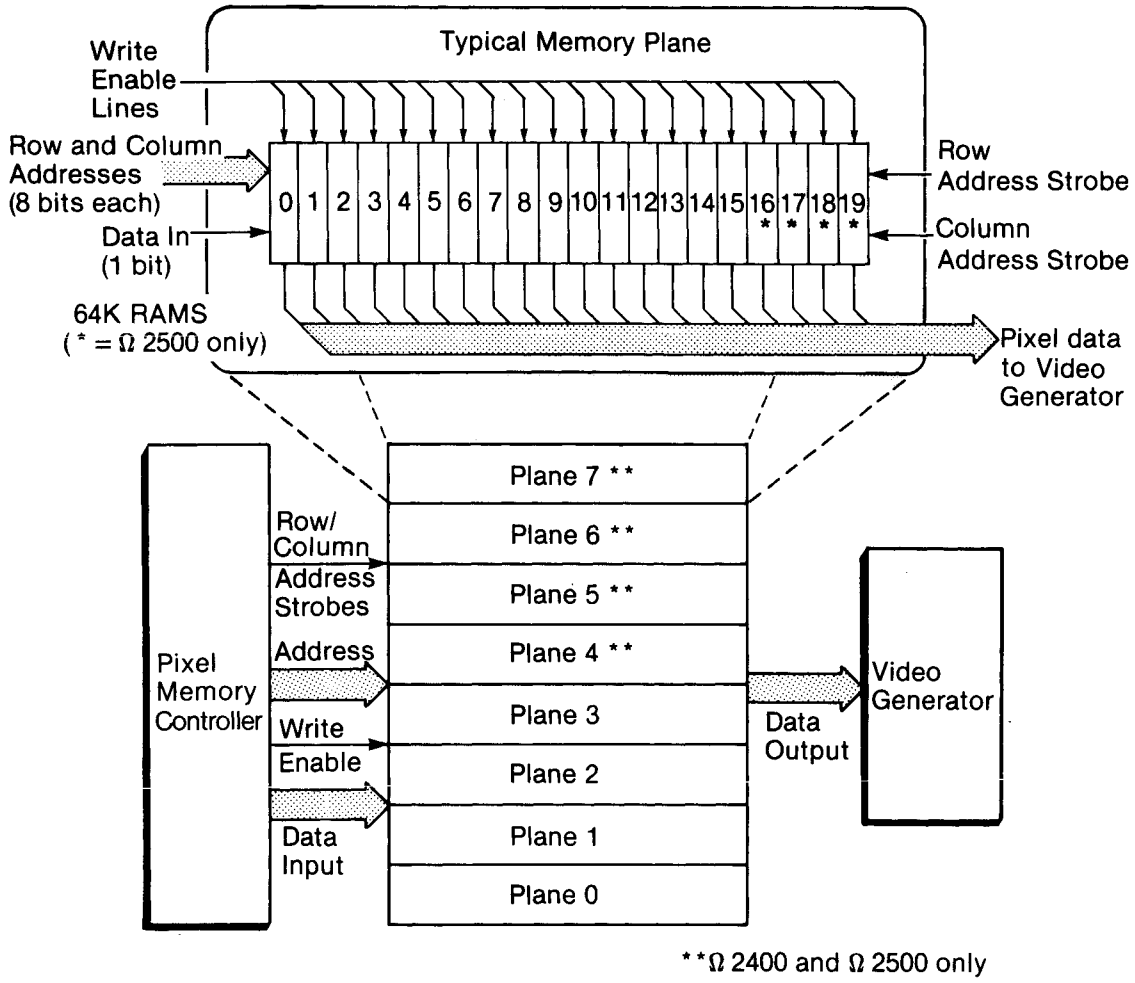


Figure 1-4. Pixel Memory Organization

Pixel Memory Controller

The pixel memory controller's most important functions are enabling the drawing processor to write, read, and modify pixel data; supplying data to the video generator to refresh the display; and refreshing the dynamic RAMs in the memory array.

Figure 1-5 is a block diagram showing the major functional blocks of the pixel memory controller. These functional blocks are as follows:

- Processor write control, which supplies address and enabling signals for drawing processor accesses to pixel memory.
- Display refresh control, which supplies addresses and enabling signals necessary for supplying the pixel data stream to the video generator.
- RAM refresh control, which supplies refresh addresses during RAM refresh cycles.
- Address selector, which sequences the multiplexed address to the memory array.
- RAS logic, which asserts the row-address strobe lines.
- Write mask and CAS logic, which asserts the column-address strobe lines and can selectively enable or disable writing into individual memory planes.
- Character and pattern generator, which generates bit patterns for alphanumeric characters and fill patterns.
- Input data path control, which selects the source of input data to the memory array.
- Readback cache, which allows the drawing processor to read the pixel memory.
- Memory cycle control, which sequences memory operations.
- Raster-op processor, which performs arithmetic and logical operations on memory input data, allowing rapid modification of display characteristics with minimal drawing processor intervention.

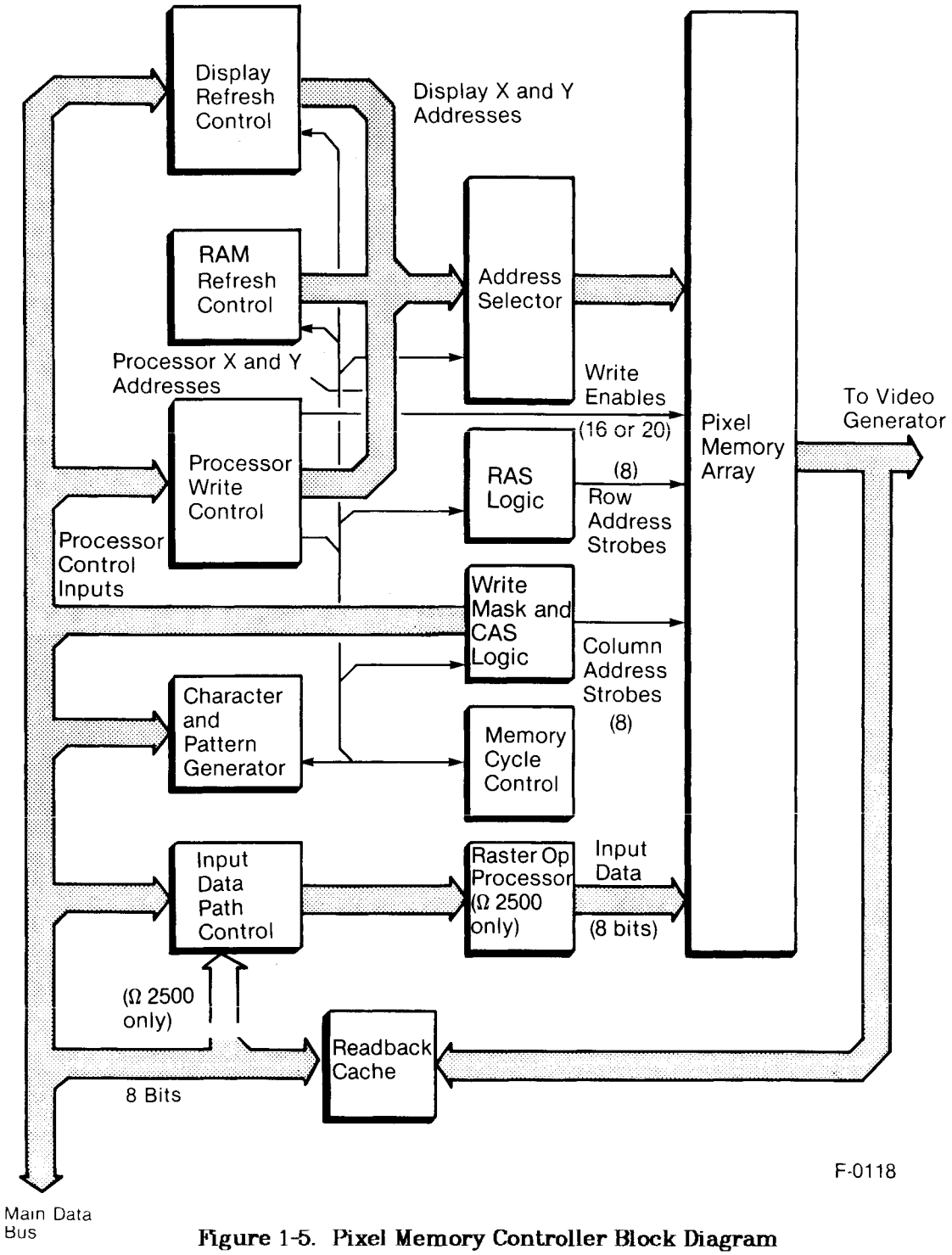


Figure 1-5. Pixel Memory Controller Block Diagram

Processor Write Operations. The drawing processor writes pixel data into memory during video display retrace periods. Because this leaves a relatively small percentage of time to create and modify the display data, the circuits involved in writing pixel data are organized to allow the drawing processor to perform the necessary vector calculations and to write data simultaneously.

Figure 1-6 is a diagram showing the functional blocks involved in processor write operations. A typical vector write sequence for the Ω2300 and Ω2400 display processors is as follows:

1. The processor loads initial addresses into the X and Y address counters within the processor write control; these counters supply the two halves of multiplexed address to the RAM array. The processor also writes data into the write mask, to control which memory planes will have data written into them. Only those planes that are write-enabled will receive a column address strobe.
2. The processor initiates a write operation through the memory cycle control, which generates control signals that sequence the write mask and CAS logic, RAS logic, and address selector.
3. If a plane is write-enabled, the CAS logic asserts a column address strobe (CAS) for that plane. Simultaneously, the selector steers the column (X) address from the X address counter in the processor write control to the pixel memory array.
4. After the column address has been latched into the memory array, the address selector steers the row address from the Y address counter to the memory array; this address is latched into the memory array by the row address strobe (RAS) from the RAS logic.

The address counters are clocked by the same clock signal as the drawing processor (220 ns for the Ω2300 and Ω2400; 167 ns for the Ω2500). The processor controls the counters through signal lines supplied directly from the pipeline register. For each write cycle, the processor allows the address counters to increment or decrement, depending on the the relative direction of the vector it is writing, until all pixels for the vector have been written.

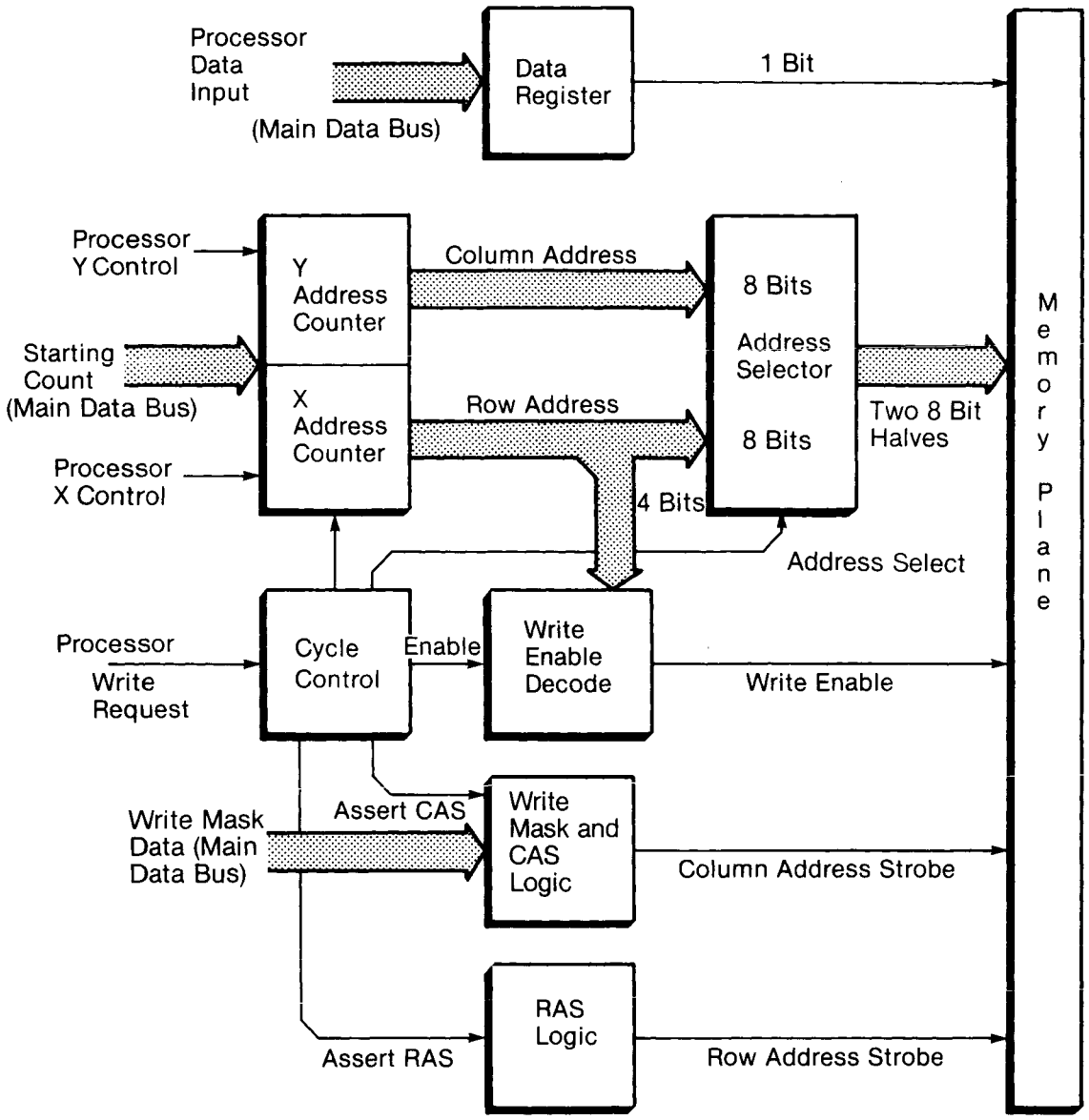


Figure 1-6. Processor Write Functions

Display Refresh. The display refresh control block of the pixel memory controller reads the display memory array, sending a continuous stream of 16-bit (Ω2300 and 2400 series) or 20-bit parcels (Ω2500 series) of pixel data from each plane of the memory array to the video shift registers within the video generator (exclusive of horizontal and vertical retrace, when the drawing processor has control of memory).

Display refresh read operations are synchronized to the video display raster by a programmable sync generator circuit, which controls the rate at which data is extracted from pixel memory. As in processor write operations, X and Y address counters within the Display Refresh circuits supply row and column addresses for the memory array.

Raster Operations. The Ω2500 display processor contains a a raster-operations (raster-op) processor. The principal component of the raster-op processor is an arithmetic/logic unit (ALU). The ALU is situated in the input data path to pixel memory, so that it can perform arithmetic and logical operations, such as Exclusive-OR or addition, on input and readback data. For example, when executing the PIXBLT command, in which a block of pixel data is transferred from one location in the display to another, the Raster Operations Processor permits the transferred data to be logically altered as it is being read back and rewritten into memory.

In addition to logical operations, the raster-op processor can also perform conditional operations. During a block transfer, for example, the raster-op processor can be set up to operate only on pixels of a certain color or range of colors.

Video Generator

The video generator converts pixel data from the pixel memory to red, green, and blue video signals that drive the display monitor.

Figure 1-7 is a block diagram of the video generator. As the diagram shows, these are the major components of the video generator:

- Video shift register and read mask, which converts data from pixel memory to a serial stream of video data, and selectively blocks data from the memory planes.
- Horizontal pan and zoom, which allows the display to be shifted and expanded. (The zoom function is not available on the Ω2500s.)
- Color map, which selects the colors that will be present on the display.
- Red, green, and blue digital-to-analog converters (DACs), which convert pixel data to video signals.

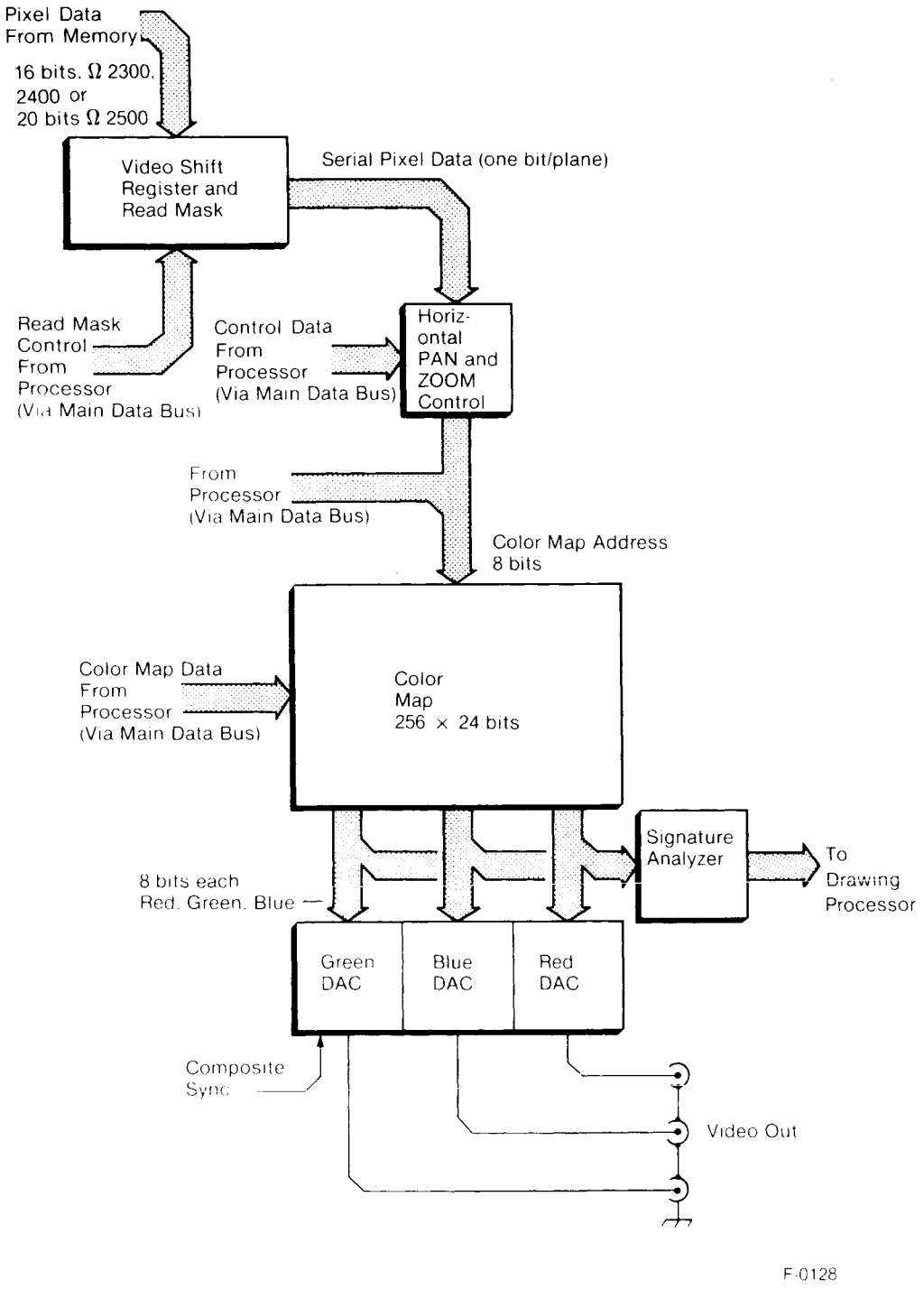


Figure 1-7. Video Generator Block Diagram

Video Shift Register. The video shift register receives parcels of 16 bits (or 20 bits in the case of the Ω2500) of data from each memory plane. These parcels of data are loaded in parallel into the registers (there is a register for each plane) and shifted out serially at the video display pixel rate (36 MHz for the Ω2300 and Ω2400 and 120 Mhz for the Ω2500). Taken together, the serialized data from the shift registers supply an 8-bit address (one bit from each plane) to the color map.

The read mask selectively blocks the data from individual planes, preventing the data from being displayed.

In the Ω2500, the video shift register block also includes a crossbar switch function, used to implement folded mode. In folded mode, each memory plane is, in effect, folded into four banks (0, 1, 2, and 3) of eight bits each. The purpose of the crossbar switch is to direct the eight bits of memory data from a particular bank to a selected (by command) color map address input. Since each bank supplies eight bits of data, the color map may receive a total 24 bits, instead of the eight bits supplied in normal mode. Note that any bank may be connected to any color map address input.

Horizontal Pan and Zoom Control. The purpose of the horizontal pan and zoom control is to allow the origin of the display to be shifted, or the size of the display to be expanded. (The Ω2500 does not have a zoom function.) Figure 1-8 is a simplified functional diagram, showing how the pan and zoom functions work. Note that parts of the pan and zoom functions lie within the pixel memory controller and other parts are in the video generator.

The zoom function uses pixel replication to expand the display; that is, each pixel is multiplied into several pixels, causing each point in the display to appear to expand. To cause pixel replication, the display refresh data stream is slowed down in relation to the display raster. This is done by slowing down the clocks to the display refresh address counters, and video shift register (using programmable prescalers), thereby slowing down the video data stream. As shown in Figure 1-8, this is controlled by a register within the display refresh control.

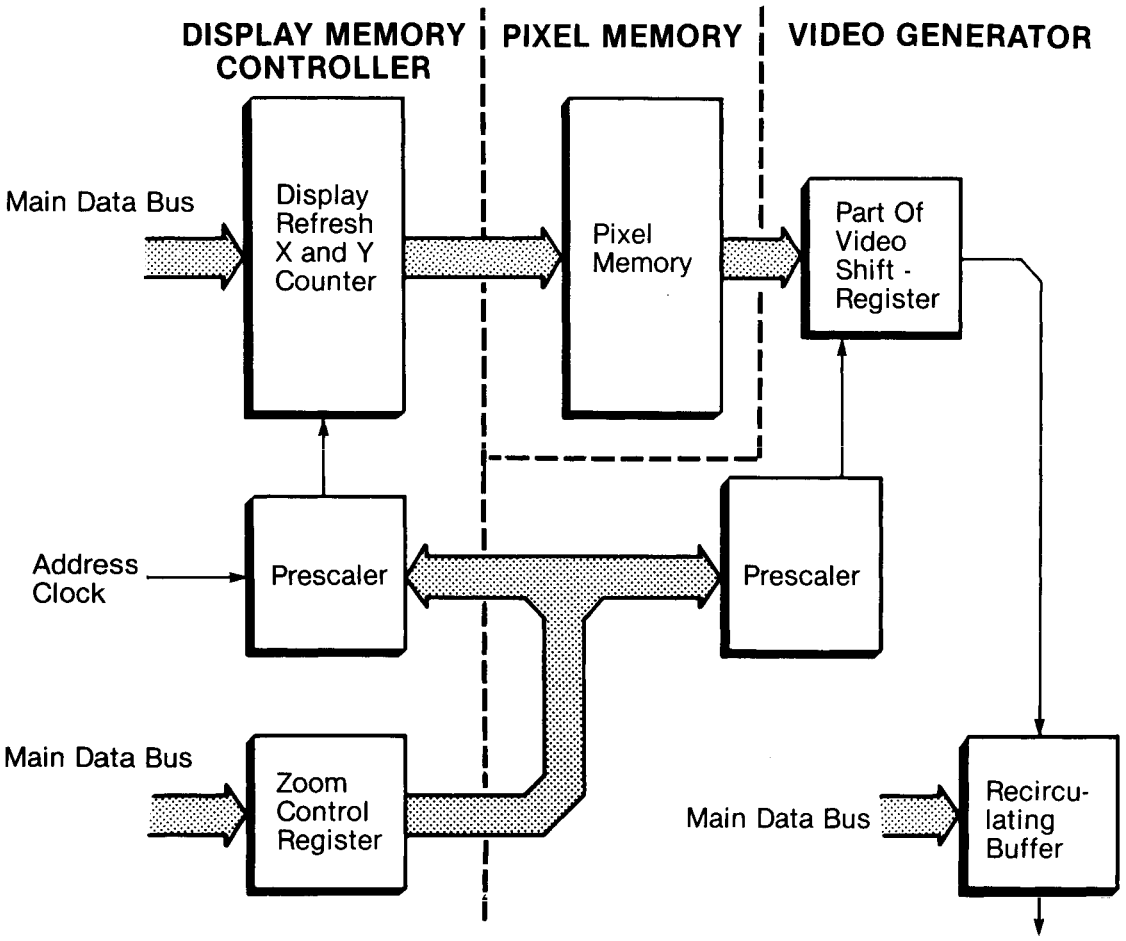


Figure 1-8. Panning and Zooming

The drawing processor pans the display by loading a starting address other than 0,0 into the display refresh address counters. This shifts the start of the display in relation to the display raster. Since the horizontal (X) display refresh address counter can address pixel memory only in increments of 16, it is necessary to have an additional fine offset control in order to achieve panning in increments of one pixel in the horizontal axis. As shown in Figure 1-8, this is accomplished by a programmable recirculating buffer at the output of the video shift register.

Color Map. The color map is a 256 by 24-bit read/write memory array that serves as a look-up table for defining the displayed color of a pixel. In the Ω2400, serialized data from the video shift register provides an 8-bit address (one bit from each

plane) to the color map. Since the Ω2300 has only 4 planes, it supplies a 4-bit address. This address selects a 24-bit value within the color map that defines the luminance values of red, green, and blue components of the pixel. The outputs of the color map drive the red, green, and blue DACs, eight bits to each DAC.

The processor can modify the data within the color map to change the current selection of colors from the palette of display colors available. The total number of colors is 16.7 million, with 16 (Ω2300) or 256 colors (the number of locations in the color map) displayable at one time. (The Ω2500 has the ability to directly select 16.7 million colors in folded mode, but they cannot all be displayed at once, since there are only 327,680 pixels on the screen.)

Digital to Analog Converters (DACs). The red, blue and green DACs convert 8-bit binary values supplied by the color map to equivalent analog voltages; these voltages drive the display monitor. Composite sync information is added to the green video output. Ω2500s also have separate HSYNC (horizontal sync) and VSYNC (vertical sync) outputs.

Diagnostic Functions

The display processor contains a signature analyzer (shown in Figure 1-8) that computes a CRC checksum of the video data from the color map. A particular display has a particular CRC signature. The drawing processor uses the signature analyzer during self-test to read the signature produced by a predefined, ROM-stored display command sequence. This way, the processor can tell whether the display generating functions are working properly. The signature analyzer may be read by the host computer as well, using the SIG READ command.

The drawing processor's microprogram ROM contains self-test routines for testing most areas of the display controller. If the processor finds an malfunction in the display controller, it can indicate the area in which the malfunction occurred by writing into a register that controls an LED status indicator. The status indicator is described in more detail in Chapter 2 of this manual.

Graphics Preprocessor

The purpose of the graphics preprocessor is to translate high level, device independent graphic instructions, such as those described in the Graphical Kernel System (GKS) and the virtual device interface (VDI) specifications, into instructions recognized by the display processor. In addition to translation, the graphics preprocessor supplies the input/output ports for host and peripheral communications. Together, the graphics preprocessor and the display processor constitute a heirarchical display-list processing system with the following capabilities:

- Segment structures

- 2D transformation and clipping
- Graphics primitives for points, circles, arcs, polygons, polylines, and polymarkers
- Graphics attributes such as color and style
- Graphics text and text attributes such as font and spacing
- Pixel operations
- Input support for locator, pick, and button-type logical devices
- Macro capability
- Keyboard and terminal display window functions

The graphics preprocessor is contained on a single 11-inch by 12-inch circuit board mounted inside the graphics controller cabinet above the display processor circuit board.

Figure 1-9 is a detailed block diagram of the graphics preprocessor. As the diagram shows, the graphics preprocessor consists of the following functional blocks:

- Preprocessor controller, which oversees graphics preprocessor operations.
- Address- and data-bus buffers, which connect the local address and data buses to the main address and data buses.
- Serial ports, four serial communications channels for host, terminal, or other serial data.
- GPIB port, an IEEE 488-1978 port for data from a host or graphic input device.
- Parallel port, a 16-bit port for host communications.
- Transform processor, which provides high-speed arithmetic data processing.
- DMA controller, which provides high-speed direct access to DRAM for the serial, parallel, GPIB, and display processor ports.
- Display list memory, a general purpose array of up to 1 megabyte of dynamic RAM for storing graphics data.
- Display processor port, through which the graphics preprocessor communicates with its display processor.
- Expansion port, which provides bus access for graphics processor expansion options

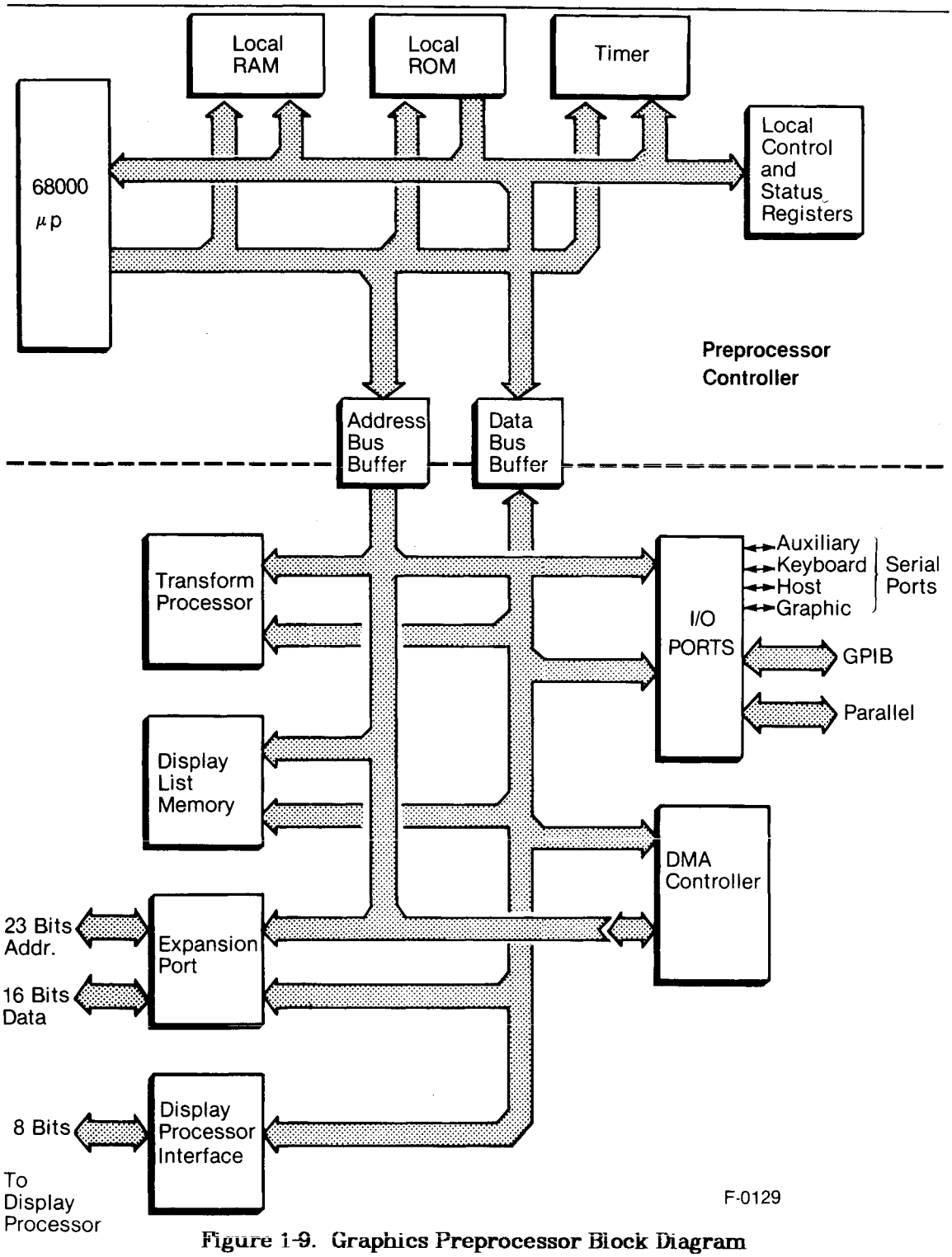


Figure 1-9. Graphics Preprocessor Block Diagram

Preprocessor Controller

The 68000 microprocessor, using the local RAM, ROM, control and status registers, and timer oversees graphics preprocessor operation. To minimize contention with the DMA controller, which makes heavy use of the main bus in transferring data to and from the graphics preprocessor, the 68000 has its own local bus (A1-A23 and D0-D15). Thus, the 68000 can execute its firmware instructions and exercise some control over the graphics preprocessor without having to contend for the main bus. The local bus is inaccessible from the main bus.

The 68000 can access up to 256 kilobytes of local ROM and up to 16 kilobytes of local RAM. The ROM contains 68000 firmware; the RAM is used for 68000 stacks, scratchpad, and other overhead functions.

The timer contains three independent programmable timer/counters. Two of the timers have designated purposes: one controls main DRAM refresh-cycle timing and one sets the bus timeout interval. The remaining section is a general-purpose timer.

The control register is a 16-bit register through which the 68000 enables interrupts from various parts of the graphics preprocessor, enables the system controller function of the GPIB interface, enables access by the display processor port to the expansion port, enables the local ROM, and selects DMA channels.

The 68000 uses eight bits of the 16-bit status register to read the state of the interrupt enable lines from the control register. The remaining eight bits of the register allow the 68000 to monitor service requests from the transform processor, and data requests from the Parallel and display processor port.

Transform Processor

The transform processor may contain up to four floating point units (FPU). Operating under control of the 68000, the FPUs speed up the arithmetic processing involved in converting high-level graphic commands from the host into low-level commands for the display processor.

Display-List Memory Array

The display-list memory array may contain 256 kilobytes or 1 megabyte (optional) of dynamic RAM. The array is accessible by the 68000, the DMA controller, and the expansion port. It serves primarily as a buffer for graphics segments and commands.

DMA Controller

The DMA controller provides two independently programmable direct memory access channels that can automatically transfer data between the main memory array and the following I/O ports:

- o Display processor port
- o GPIB port
- o Parallel port
- o Serial ports 0 and 1

16-bit Parallel Port

The 16-bit parallel port is a general-purpose, 16-bit, bidirectional I/O port. It provides separate, 16-bit, latched input and output buses and a set of handshaking signals that permit it to be configured for different host system protocols. The parallel port connects to the graphics controller's back panel circuit board, where it is configured for a specific host. The standard back panel board is configured for a DEC[1] DR11-W interface.

Serial Ports

The graphics preprocessor provides four programmable serial ports that may be configured for a variety of baud rates and communications protocols. In standard graphics preprocessor configurations, all ports are asynchronous. All of the input and output signals pass through the back panel circuit board.

Port 0 is ordinarily used for host communications. Port 1 is a "debug" port; it can supply information about command execution when connected to a terminal. Signal levels for ports 0 and 1 are set by drivers and receivers installed on the back panel board. RS-232 signal levels are standard. Ports 0 and 1 provide the following signals:

- o TxD (Transmit Data--output)
- o RxD (Receive Data--input)
- o RTS (Request to Send--output)
- o CTS (Clear to Send--input)

In addition to the signals listed above, port 0 provides DTR (Data Terminal Ready) and port 1 provides DSR (Data Set Ready), which are permanently tied high.

Port 2 is ordinarily connected to a keyboard. The inputs and outputs for this port are configured specifically for a Metheus-supplied keyboard. Port 3 connects to a mouse or graphic tablet. Both of these ports provide RS-423 signal levels.

[1]DEC is a trademark of Digital Equipment Corporation.

GPIB Port

Based on a large-scale integrated controller chip, the optional GPIB port conforms to IEEE Standard 488-1978. It can provide communications with a GPIB-compatible host or graphics tablet.

Display Processor Port

The display processor port is an 8-bit parallel port through which the graphics preprocessor communicates with its display processor.

OPTIONS

Ω 2000-Series Graphics Controller performance may be enhanced with the following options:

GPIB Interface	Allows the graphics controller to communicate with GPIB-compatible hosts and graphics input devices. This option must be specified at the time the graphics controller is ordered; it is not field-installable.
1M Display List Memory	Expands display-list memory on the graphics preprocessor from 256K to 1 megabyte. This option must be specified at the time the graphics controller is ordered; it is not field-installable.
Extended Transform Processor	Enhances display transform-processing speed. This option is field-installable.

In addition to these performance options, Ω2000-Series Graphics Controllers may be supplied with rackmounts and slides for standard rack mounting, and they may be factory-configured for 220 VAC operation. (220 volt power cords are not supplied.)

Chapter 2
Operating and Troubleshooting Instructions

This chapter contains operating and troubleshooting information for the Ω2000-Series Graphics Controllers. It includes descriptions of the controls, indicators, and I/O connectors, as well as power-up, preventive maintenance, and troubleshooting procedures.

CONTROLS, INDICATORS, AND CONNECTORS

As shown in Figure 2-1, the principal features of the graphics controller's front panel are as follows:

Power Indicator	Illuminates when the power switch is placed in the on position; it indicates that the +5 volt power supply is functioning.
Ready Indicator	Illuminates after the graphics controller has successfully completed its power-up self-test program and is ready to execute instructions.
Power Switch	Controls AC power to the graphics controller.

The back panel is also shown in Figure 2-1; its principal features are as follows:

Host Parallel Input	(J6) is the input connector for the parallel host port.
Host Parallel Output	(J5) is the output conector for the parallel host port.
Serial Host	(J7) is the connector for the serial host port.
GPIB	(J12) connects either to a GPIB host or a graphics tablet.
Serial Graphic Input	(J4) connects to a serial graphics tablet.
Serial Auxiliary	(J11) connects to a terminal to provide status information on command execution.
Serial Keyboard	(J13) connects to an RS-232 serial keyboard (not supported in initial product release).
Red, Green, Blue Video	Supply video signals to the display monitor; they are 75-ohm outputs.

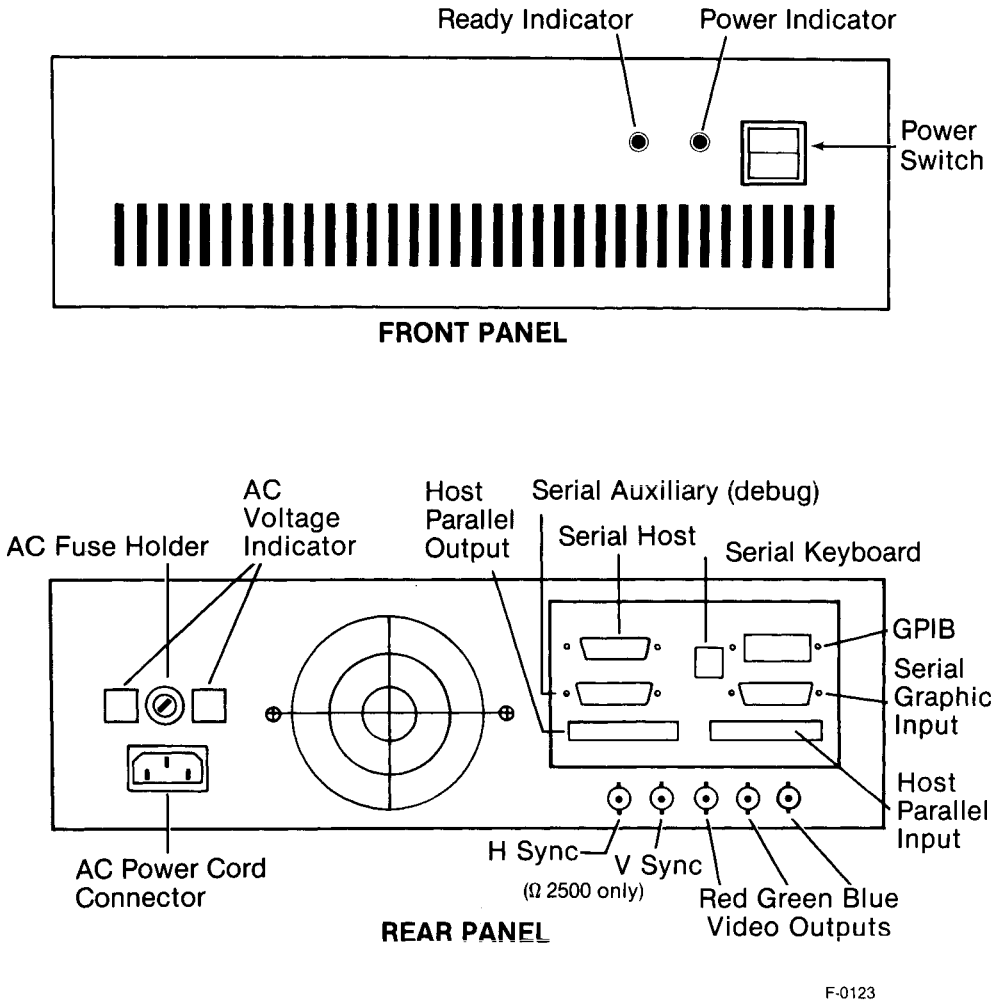


Figure 2-1. Graphics Controller Front and Rear Panels

HSync, VSync	Supply horizontal and vertical sync outputs (Ω2500s only).
AC Power Cord	Is a universal AC power cord connector; it requires a three-wire power cord with a safety ground, appropriate to the voltage range and location in which the graphics controller is to be used.
AC Fuse	Requires a 2A, 250 volt fuse for the 220 VAC range; a 4A, 250 volt fuse for the 110 VAC range. See Chapter 3 for removal and replacement procedures.
AC Voltage Indicator	Is next to the fuse, it indicates the voltage range to which the graphics controller is set.

SETTING CONFIGURATION OPTIONS

Before using the graphics controller, a number of configuration options must be set. The options are summarized in this section; Chapter 3 contains detailed procedures for setting them.

Configuration options fall into the following general categories:

- Host port configuration
- Graphic input configuration
- Auxiliary port configuration
- Display mode configuration

Host communications may be assigned to the parallel, serial, or GPIB ports. The selection is controlled configuration switches. If the serial host port is selected, the baud rate and data flow-control mode (modem, XON/OFF) must be set as well. Host communication via the GPIB port requires that a GPIB address be selected. If the GPIB port is not used for host communications, it may be assigned to a graphics tablet.

The Ω2000-Series Graphics Controllers accept two different switch-selectable serial graphics-input data formats: the Summagraphics[1] Bit Pad format and the GTCO[1] Digi-Pad high resolution format. In addition to the two data formats, four switch-selectable baud rates are available.

The auxiliary RS-232 port supplies status information about commands being processed by the graphics preprocessor. This port has four switch-selectable baud rates.

Display mode (resolution and refresh rate) for the Ω2300 and Ω2400 Graphics Controllers are set by jumpers on the Display Processor board. For Ω2500 Graphics Controllers, the display mode may be set by a command (SELRES); however, a jumper is provided on the display processor board to set the default mode at power-up.

POWER-UP AND OPERATION

Once properly connected and configured according to the instructions given in Chapter 3, graphics controller power-up and operation are simple:

1. Apply power to the display monitor and other peripherals connected to the graphics controller and allow them to warm up.

---

[1]Summagraphics is registered trademark of Summagraphics Corporation.

[2]GTCO is a trademark of GTCO Corporation.

2. Place the graphics controller's power switch in the "on" position.

The Power indicator on the front panel should come on immediately after power is applied. At this point the graphics controller begins its power-up self-test program. About 10 seconds later, the graphics controller displays a test pattern on the monitor. The Ω2500 displays two patterns: a multicolored checkerboard pattern and a "star" consisting of multicolored lines radiating from a point near the center of the screen. The Ω2300 and Ω2400 display only the star pattern. The self-test program uses the graphics controller's signature analyzer to read the signature of the test pattern; this allows it to compare a known ROM-stored signature with the actual output of the graphics controller and determine if the display circuitry is working correctly.

If the self-test program runs successfully, the Ready indicator on the front panel comes on, indicating that the graphics controller has passed self-test and is ready to execute commands from the host. (It may still be possible to execute commands even if the Ready indicator does not come on, but the graphics controller may not be completely functional.)

If a terminal is connected to the auxiliary RS-232 port, the graphics controller will also display a message giving the version number of the graphics preprocessor firmware installed.

After self-test is completed, test host communications and graphics input by executing a few commands. Refer to the *Ω2000-Series Programmer's Reference Manual* (see the preface) for further information.

If the graphics controller fails to power up and run properly, consult the troubleshooting section that follows.

WHAT TO DO IN CASE OF TROUBLE

The following list of symptoms and corrective actions is designed to help you decide whether a particular problem lies within the graphics controller or is the result of some external cause. It should also help in communicating with service personnel, if that becomes necessary. This information is not intended to allow troubleshooting to the component level. Refer to *Service Information* in the front of this manual for information on obtaining service from Metheus Corporation.

WARNING

To avoid possible personal injury and damage to the graphics controller, always turn off the power and disconnect the power cord before removing any cover or removing the fuse. Refer to Chapter 3 for procedures.

Symptom:	No power; Power and Ready indicators off, fan not running.
Corrective action:	Check that the power cord is connected to and active outlet; check the fuse.
Symptom:	Fan runs, but the Power and Ready indicators are off.
Corrective action:	Remove the top cover and check that the +5 and -5 volt supply LEDs on the graphics preprocessor board are on. If either of them is not, a power supply problem is indicted. Contact factory service.
Symptom:	Fan runs, Power indicator on, Ready light not on, no display, no communications.
Corrective action:	Remove the top cover and check the diagnostic indicators. (See "Diagnostic Indicators" later in this section.) Report the indications to factory service.
Symptom:	No display, Power and Ready indicators on, responds to "debug" terminal or host.
Corrective action:	Check monitor power, check for properly connected cables, run monitor self-test (if available).
Symptom:	Display colors missing or improper, graphics controller self-test passed.
Corrective action:	Check for shorted, open, disconnected, or reversed coaxial cables.
Symptom:	Host communications faulty, graphic input and auxiliary port normal.
Corrective action:	Make sure the cables are connected to the right connectors (on the parallel port check that the input and output cables are not reversed); check configuration (port assignment, baud rate, GPIB address, serial data-flow control).
Symptom:	No graphic input, other I/O normal.
Corrective action:	Make sure all connectors are connected properly; check power to the graphic input devices; check configuration (serial data format, baud rate, GPIB address).

Diagnostic Indicators

Figures 2-3 shows the diagnostic indicators available for troubleshooting on the Ω2300 and Ω2400; Figure 2-4 shows the indicators for the Ω2500. The graphics preprocessor in all models has the following indicators:

- Supply voltage status indicators, one each for the +5 and -5 volt supplies.
- Processor activity indicator, which indicates the microprocessor is running. It may flicker on occasionally, but is normally off.

- 7-segment indicator: F=normal operation; 1=memory error; 2=unresponsive Display Processor board.

The Ω2300 and Ω2400 display processor boards have a series of LEDs that indicate errors. All these LEDs should be on during normal operation. If D9 and D11 are off, a possible graphics preprocessor problem is indicated. If any other LEDs are off, a display processor board problem is indicated.

The Ω2500 display processor boards have a 7-segment LED to indicate errors. The indicator is visible through a viewing port in the graphics preprocessor board. (See Figure 2-3.) An F indicates normal operation, a 5 indicates a possible graphics preprocessor problem, all other characters indicate a display processor problem.

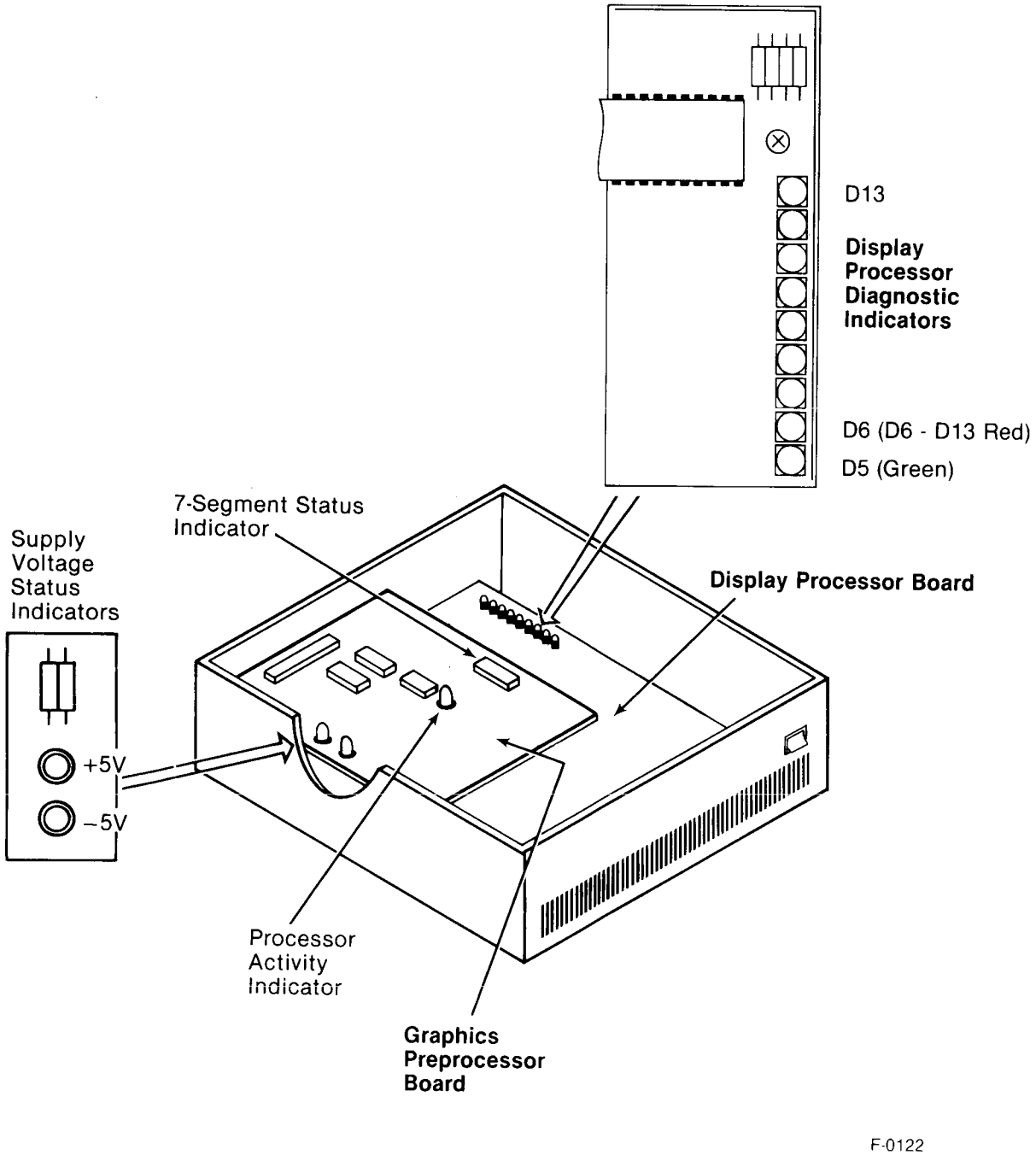


Figure 2-2. Ω2300 and Ω2400 Diagnostic Indicators

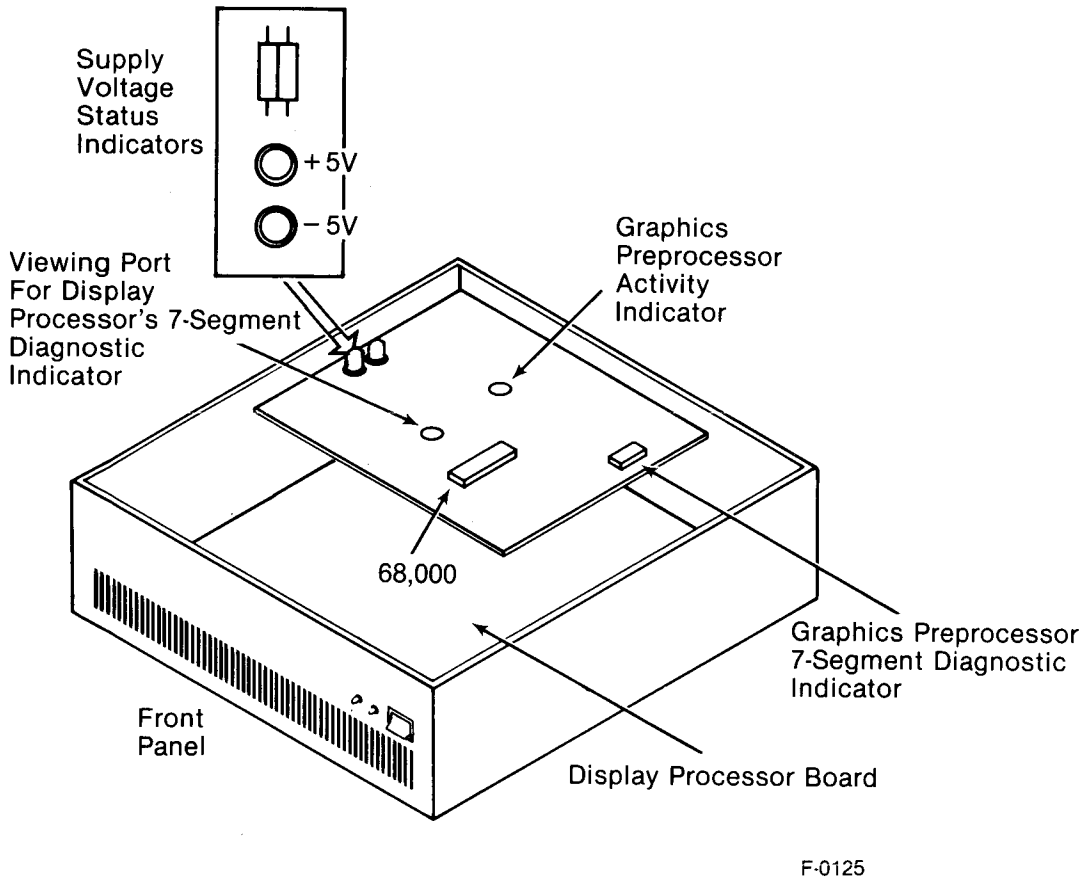


Figure 2-3. Ω2500 Diagnostic Indicators

Chapter 3
Installation and Configuration

This chapter contains installation and configuration instructions for the graphics controller. It includes guidelines for selecting an installation site, and instructions for setting line voltage and configuration switches and connecting the graphics controller to the host and graphic input devices.

WARNING

This chapter contains procedures that could expose you to hazardous voltages. These procedures should be performed only by qualified service personnel. Always turn off the power switch and disconnect the power cord before removing any cover or removing the fuse.

SELECTING AN INSTALLATION SITE

Before installation, preferably before the graphics controller arrives, you should give some consideration to the installation site, following the guidelines listed below. This will allow the installation procedure to go smoothly, and it will ensure continued reliable operation.

1. Be sure there is adequate space for the graphics controller and any peripheral equipment to be installed, such as the monitor and graphics input devices. See Appendix A for the graphics controller's dimensions.

   There should be at least 2 inches (50 mm) clearance behind the back panel of the graphics controller; especially, make sure that the fan remains clear. It is also a good idea to provide easy access for service technicians.

2. Bear in mind that limits on the lengths of the cables connecting the graphics controller to the host, monitor, and graphics input devices may affect the arrangement of the system. Using excessively long cables may degrade performance.

   When using the GPIB port to connect to the host, the total cable length must not exceed 20 meters or 2 meters multiplied by the number of devices connected to the bus, whichever is less.

   When connecting the parallel port to a DEC DR11-W host interface, the cable length should not exceed 50 feet (15.2 m) if shielded cables are used, or 10 feet (3 m) if unshielded cables are used.

The coaxial cables used to connect the video outputs of the graphics controller to the display monitor must be of equal length. Otherwise, the video components will be out of phase with one another. Use only 75-ohm cable.

3. Install the graphics controller and its peripherals on a stable surface away from vibration and shock. Be sure that the interconnecting cables cannot be pinched, chafed, pulled, stepped on, or subjected to vibration.
4. Be sure the graphics controller has adequate cooling air, especially if it is to be operated in a confined area with other heat-generating equipment (such as in an equipment rack). Ambient temperature limits are given Appendix A.
5. Be sure AC power of the proper voltage, frequency, and amperage is available for the graphics controller and its peripherals.

CHANGING THE LINE VOLTAGE RANGE

The graphics controller has two AC line voltage ranges: 110 VAC and 220 VAC. Selecting a new line voltage range is a four-part process consisting of:

- Setting jumpers on the +5 VDC and -5 VDC power supplies
- Installing a new fan
- Changing the fuse
- Installing a new power cord

To perform these procedures, a posidrive-type screwdriver and a flat-bladed screwdriver suitable for #6 screws are required. Proceed as follows:

WARNING

The following procedures could expose you to hazardous voltages. To avoid possible personal injury and damage to the graphics controller, always turn off the power switch, disconnect the power cord from the AC power outlet, and wait a minimum of 5 minutes before removing any panel from the graphics controller.

1. Turn off the graphics controller power switch, then disconnect the power cord from the AC power outlet and the receptacle on the back panel of the Graphic Controller.
2. Carefully turn the graphics controller over, resting it on its top surface.
3. Wait 5 minutes. Remove the four screws attaching the bottom cover (one in each corner) and remove the cover.
4. Figure 3-1 shows the locations of the power supplies and the line voltage jumper settings for the Ω2300 and Ω2400; Figure 3-2 shows the same information for the Ω2500. Referring to the appropriate figure, make the necessary jumper changes for the line voltage range you wish to select, as follows:

   To select 110 VAC:

On the +5 volt supply, install two straps next to the terminal block, as shown in the figure.

On the -5 volt supply, move the two AC input leads from terminals 7 and 8 on the terminal block to terminals 8 and 9. Install a jumper between terminals 7 and 8.

To select 220 VAC:

On the +5 volt supply, install one strap next to the terminal block, as shown in the figure.

On the -5 volt supply, remove the jumper between terminals 7 and 8 on the terminal block. Move the two AC input leads from terminals 8 and 9 to terminals 7 and 8.

5. Reinstall the bottom cover and turn the graphics controller upright.
6. Remove the graphics controller's top cover as described later in this section in *Top cover removal*.
7. Remove the fan from the rear panel of the graphics controller and install a new one with the correct voltage rating. The fan's power lead unplugs at the fan; the fan attaches to the rear panel with four #6 screws.

   The following replacement fans may ordered from Metheus.

110 volt range:	Metheus part #050-01992-00
220 volt range:	Metheus part #050-01998-00

   See *Service Information* at the front of this manual for information on contacting Metheus.
8. Reinstall the top cover.
9. The AC line fuse is located on the back panel of the graphics controller. Remove the fuse (using a flat-bladed screwdriver, unscrew it counterclockwise a quarter-turn) and install a new fuse of the required size (4A, 250V for the 90-132 volt range; 2A, 250V for the 186-234 volt range--use Littlefuse type 312 or equivalent).
10. The graphics controller provides a universal power cord receptacle on its back panel. Install a power cord appropriate to the AC voltage selected and the location in which the graphics controller is to be operated. Metheus supplies only North American, 120 VAC power cords.

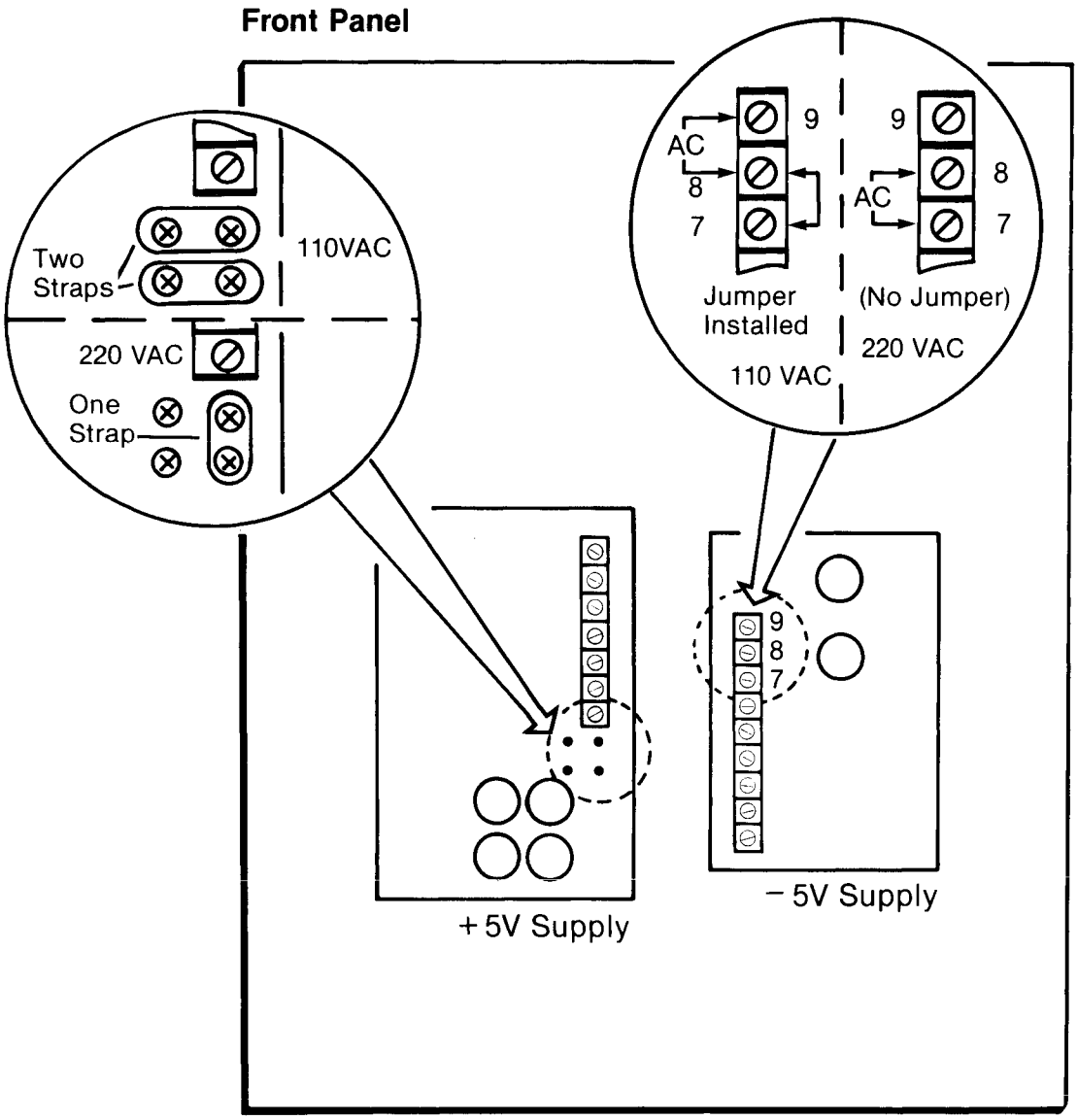


Figure 3-1. Ω2300 and Ω2400 Line Voltage Selection

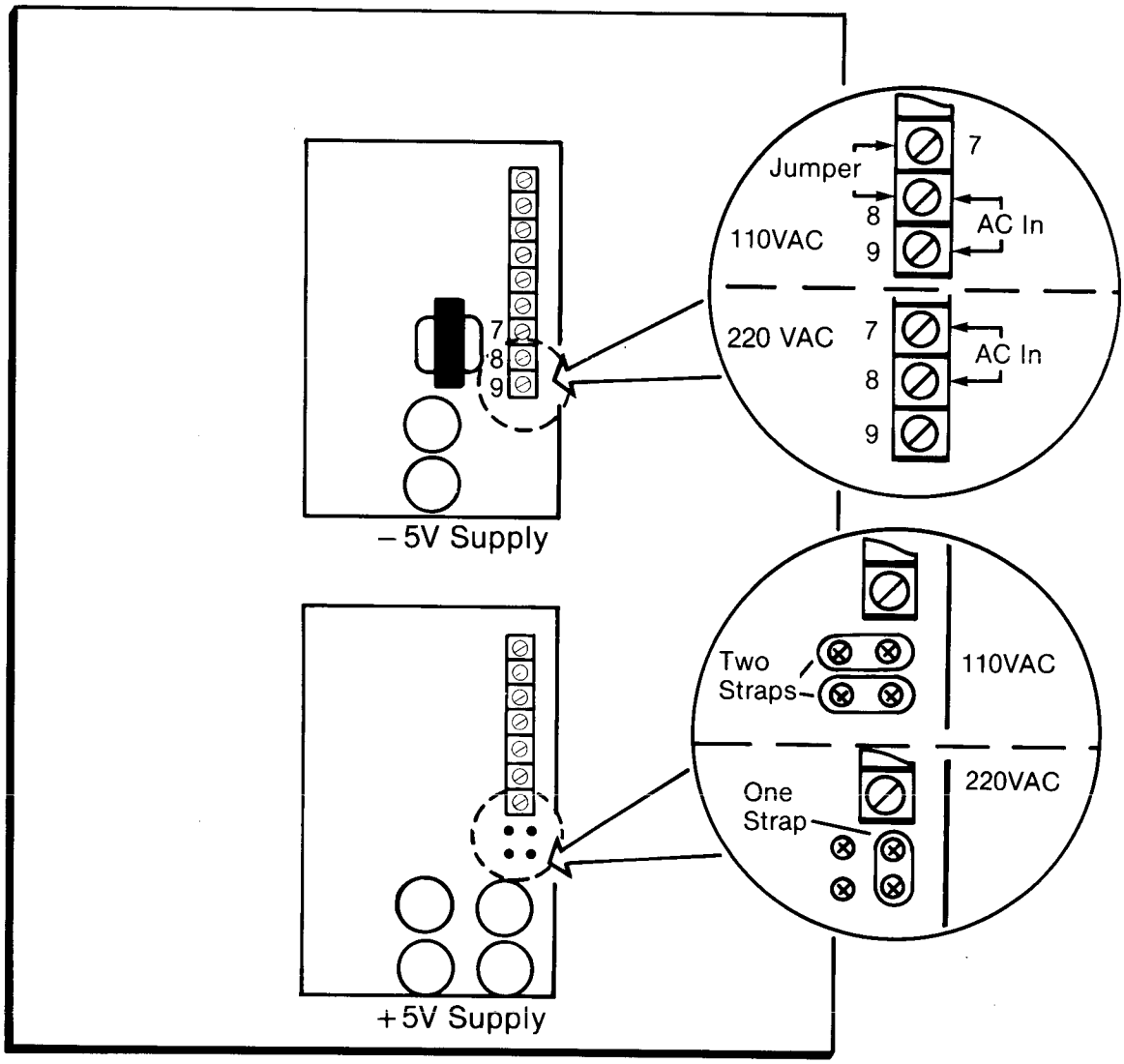


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Figure 3-2. Ω2500 Line Voltage Selection (Bottom View Shown)

GRAPHICS PREPROCESSOR CONFIGURATION

The graphics preprocessor has two banks of DIP switches for setting the following configuration options.

- Host port selection
- Host port baud rate
- Host port data flow control
- GPIB address
- Graphic input data format
- Graphic input baud rate
- Auxiliary port baud rate

To set the graphics preprocessor configuration options, proceed as follows:

WARNING

The following procedures could expose you to hazardous voltages. To avoid possible personal injury and damage to the graphics controller, always turn off the power switch, disconnect the power cord from the AC power outlet before removing the top panel.

1. Turn off the power switch and disconnect the power cord from the AC power outlet.
2. Remove the top cover, as described later in this chapter in "Removing the Top Cover."
3. Referring to Figure 3-3, locate the DIP switches on the graphics preprocessor board and make the appropriate settings. The DIP switches are divided into two banks: the low bank contains switches 0 through 7; the high bank contains switches 8 through 12. (Three switches on the high-bank are unused. Disregard the switch numbers stamped on the switches themselves.)

Switch settings are given in the following sections.

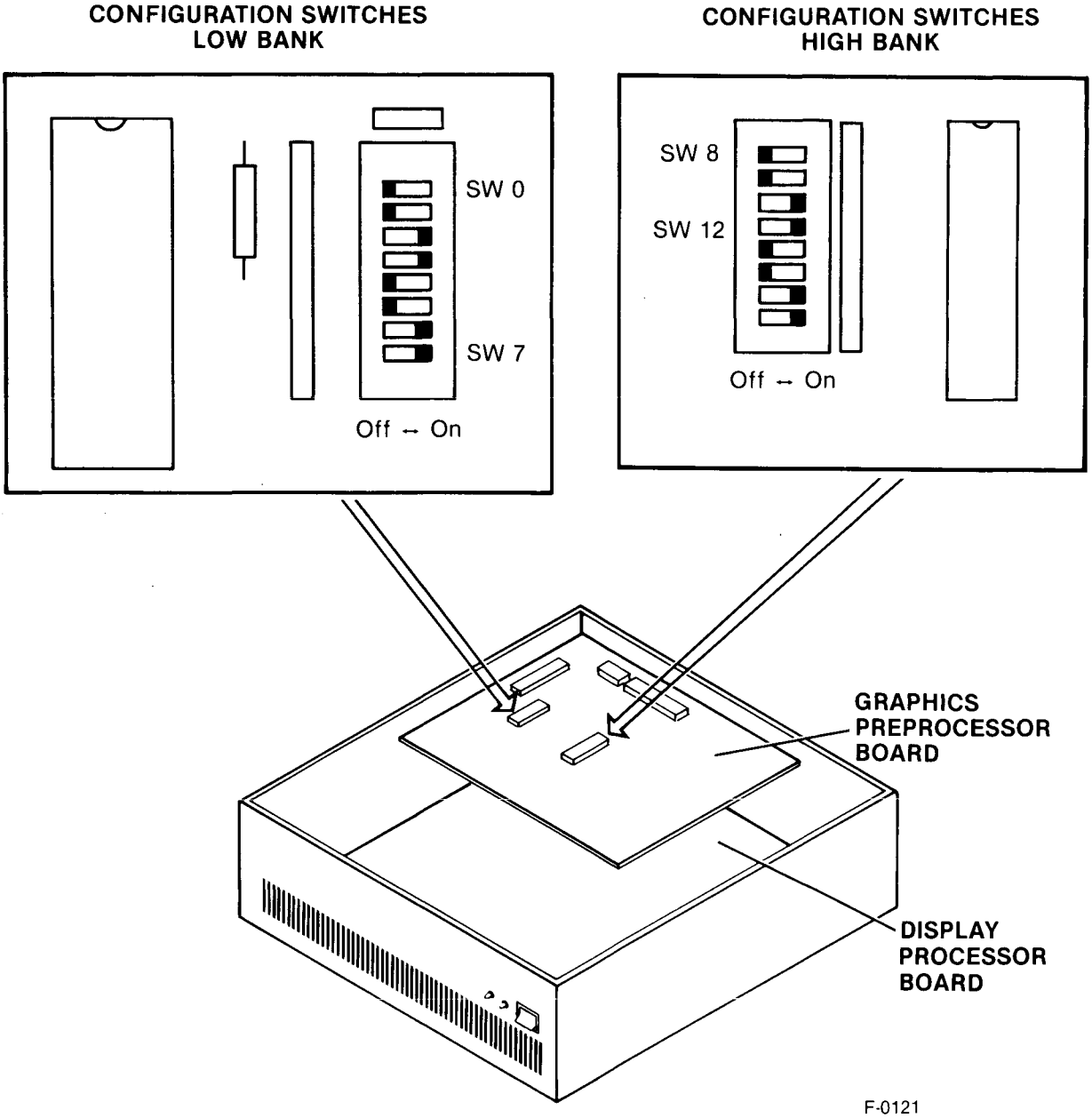

Figure 3-3. Graphics Preprocessor Configuration Switches

Host Port Selection

Configuration switches 0 and 1 (Figure 3-3) select which port is used for host communications. There are four choices:

- 16-bit parallel port.
- GPIB port. If the GPIB port is selected, the GPIB address must be set as well.
- Serial port using raw data format. In raw data format, each character received from the host is interpreted as an 8-bit binary value.
- Serial port using hexadecimal format. In hexadecimal format, each character received from the host is assumed to be one of the hexadececimal characters 0 through F; 8-bit values are assembled from two sequential characters.

Table 3-1 lists the ports and their corresponding switch settings.

Table 3-1. Host Port Selection

Port Selected	Switch 1	Switch 0
Parallel	on	off
GPIB	off	on
Serial (raw format)	on	off
Serial (hex format)	on	on

GPIB Address Selection

When the GPIB port is selected as the host port, graphics preprocessor configuration switches 2 through 6 (Figure 3-3) set the GPIB address for the port. The on/off states of the switches comprise a 5-bit binary value that selects addresses 0 through 30. Switch 6 corresponds to the most significant bit of the address; switch 2 corresponds to the least significant bit. An "on" switch is a 1; an "off" switch is a 0. To select address 8 (decimal), for example, switch 5 would be off, all others would be on.

Host Port Baud Rate

Configuration switches 4, 5, and 6 select data transfer rate for the serial host port. Table 3-2 lists the available baud rates and their corresponding switch settings.

Table 3-2. Host Port Baud Rate Settings

Baud Rate	Switch 6	Switch 5	Switch 4
300	off	off	off
1200	off	off	on
2400	off	on	off
4800	off	on	on
9600	on	off	off
19.2K	on	off	on
reserved	on	on	off
reserved	on	on	on

Host Serial Data-Flow Control

Configuration switches 2 and 3 (Figure 3-3) set the mode used for starting and stopping the flow of serial data between the host and the graphics controller. There are three choices:

Modem — When using modem flow control, the graphics controller functions as if it were a terminal connected to a modem. The graphics controller asserts the Request To Send (RTS) signal line (held permanently high) and it monitors the Clear To Send signal line to determine when it can transmit to the host. When the graphics controller is ready to receive data, it asserts the Data Terminal Ready (DTR) signal line.

XON/XOFF — When using XON/XOFF flow control, data flow between the host and the graphics controller is started and stopped using control characters. To stop the flow of data from the host, the graphics controller transmits CONTROL-S (11 hexadecimal) to the host; to resume data flow, it transmits CONTROL-Q (13 hexadecimal). Likewise, when sending data to the host, the graphics controller stops sending when it receives CONTROL-S from the host, and resumes when it receives CONTROL-Q.

CAUTION

XON/XOFF flow control cannot be used with raw data format.

None — When no data-flow control is specified, data transmission proceeds without regard to control signals or characters.

Table 3-3 lists the data flow control modes along with their corresponding switch settings.

Table 3-3. Host Port Data-Flow Control Settings

Mode	Switch 3	Switch 2
None	off	off
XON/XOFF	off	on
Modem	on	off
reserved	on	on

Graphic-Input Data Format

The graphics preprocessor accepts serial graphic input in two formats: the Summagraphics Bit Pad format, and the GTCO Digi-Pad high-resolution format. Refer to the Summagraphics and GTCO manuals listed in the preface for information on the formats.

Configuration switch 8 selects between the two formats, as follows:

ON selects the GTCO format.

OFF selects the Summagraphics Bit Pad format.

Graphic-Input Baud Rate

Configuration switches 9 and 10 (Figure 3-3) select the baud rate for the serial graphic-input device. The available baud rates and their corresponding switch settings are given in Table 3-4.

Table 3-4. Graphic-Input Baud Rate Settings

Baud Rate	Switch 10	Switch 9
300	off	off
1200	off	on
2400	on	off
9600	on	on

Auxiliary Port Baud-Rate Settings

Configuration switches 11 and 12 (Figure 3-3) select the baud rate for the auxiliary port. The available baud rates and corresponding switch settings are listed in Table 3-5.

Table 3-5. Auxiliary Port Baud-Rate Settings

Baud Rate	Switch 12	Switch 11
300	off	off
1200	off	on
2400	on	off
9600	on	on

Ω2300 AND Ω2400 DISPLAY-MODE SELECTION

The Ω2300 and Ω2400 Graphics Controllers have two display-refresh modes, 33 Hz and 60 Hz, corresponding to different display resolutions. In 60 Hz mode, the display raster is non-interlaced, with a displayed resolution of 736 pixels in the horizontal direction by 552 pixels in the vertical direction. In 33 Hz mode, the display is

interlaced, with a displayed resolution of 1024 pixels in the horizontal direction and 768 in the vertical direction. Change the display mode as follows:

NOTE

When the display mode is changed, it may be necessary to adjust or reconfigure the display monitor as well. Some monitors cannot operate at both refresh rates; in this case, it will be necessary to use a different monitor.

1. Turn off the graphics controller switch and disconnect the power cord from the AC power outlet.
2. Remove the top cover and graphics preprocessor board, as described later in this chapter in *Top Cover Removal* and *Graphics Preprocessor Removal.*
3. As shown in Figure 3-4, the display mode jumpers are installed on stake pins located near the rear edge of the display processor board. There are two two-pin jumpers, denoted in the figure by a double box enclosing two smaller boxes (which represent the stake pins). To select 33 Hz mode, install the jumpers on the right-hand pairs of pins. To select 60 Hz mode, install the jumpers on the left pairs on pins.
4. Reinstall the graphics preprocessor board and top cover.

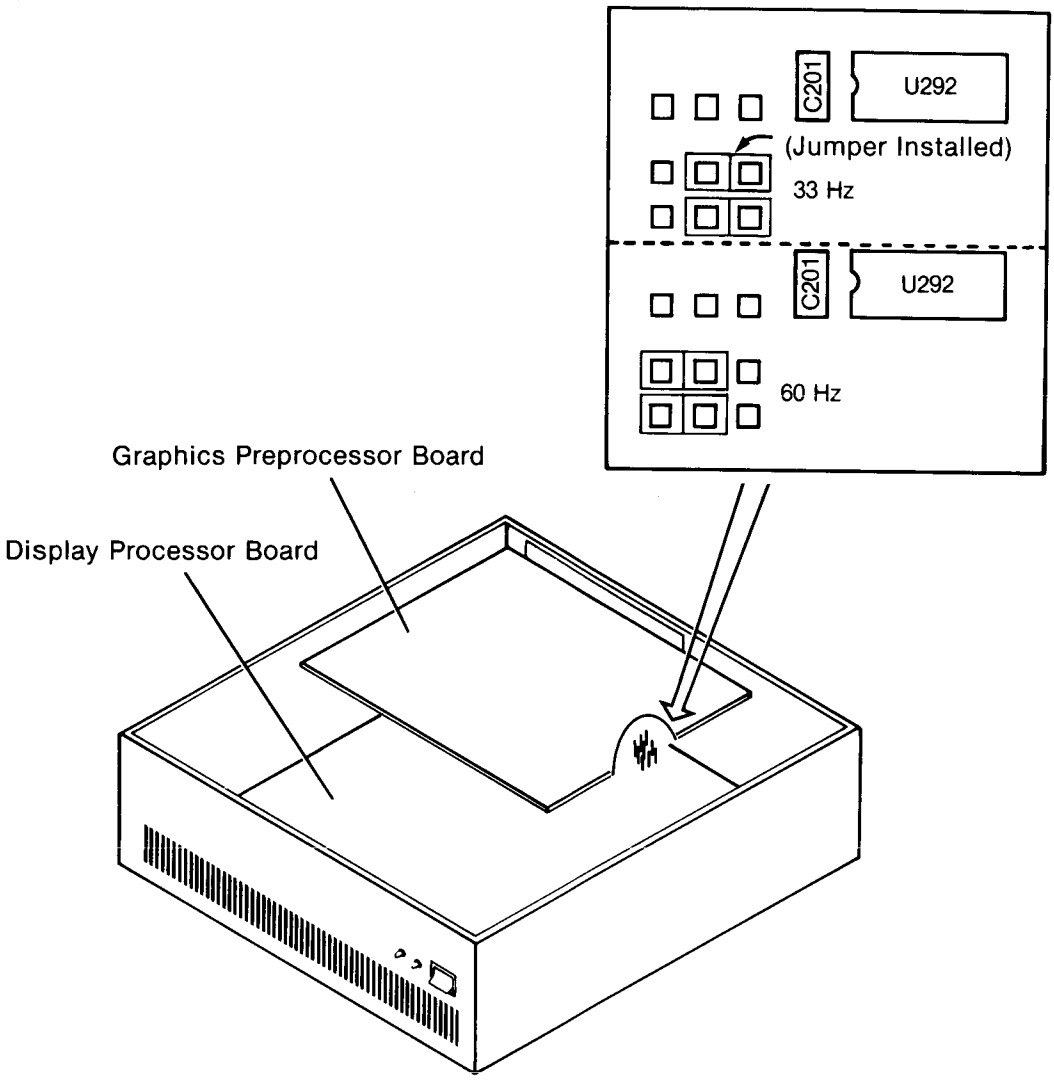

Figure 3-4. Ω2300 and Ω2400 Display-Mode Selection

Ω2500 DISPLAY-MODE SELECTION

Ω2500 Graphics Controllers have two display modes: *normal* (high resolution) mode, in which the displayed resolution is 1280 pixels horizontal by 1024 pixels vertical by 8 bits deep; and *folded* mode, in which the displayed resolution is 640 pixels horizontal by 512 pixels vertical by 32 bits deep. The two modes are selectable by software command, but the default mode at power-up is determined by a jumper on the display processsor circuit board. The location of the jumper is shown in Figure 3-5. To change the default display mode, proceed as follows:

NOTE

When the display mode is changed, it will be necessary to either reconfigure the display monitor or use a different monitor.

WARNING

The following procedures could expose you to hazardous voltages. To avoid possible personal injury and damage to the graphics controller, always turn off the power switch, disconnect the power cord from the AC power outlet before removing the top panel.

1. Turn off the graphics controller power switch and disconnect the power cord from the AC power outlet.
2. Remove the top cover as described later in this chapter in *Top Cover Removal.*
3. Referring to Figure 3-5, locate the display mode jumper and install or remove it, depending on the desired mode.
4. Reinstall the top cover and reconnect the power cord.

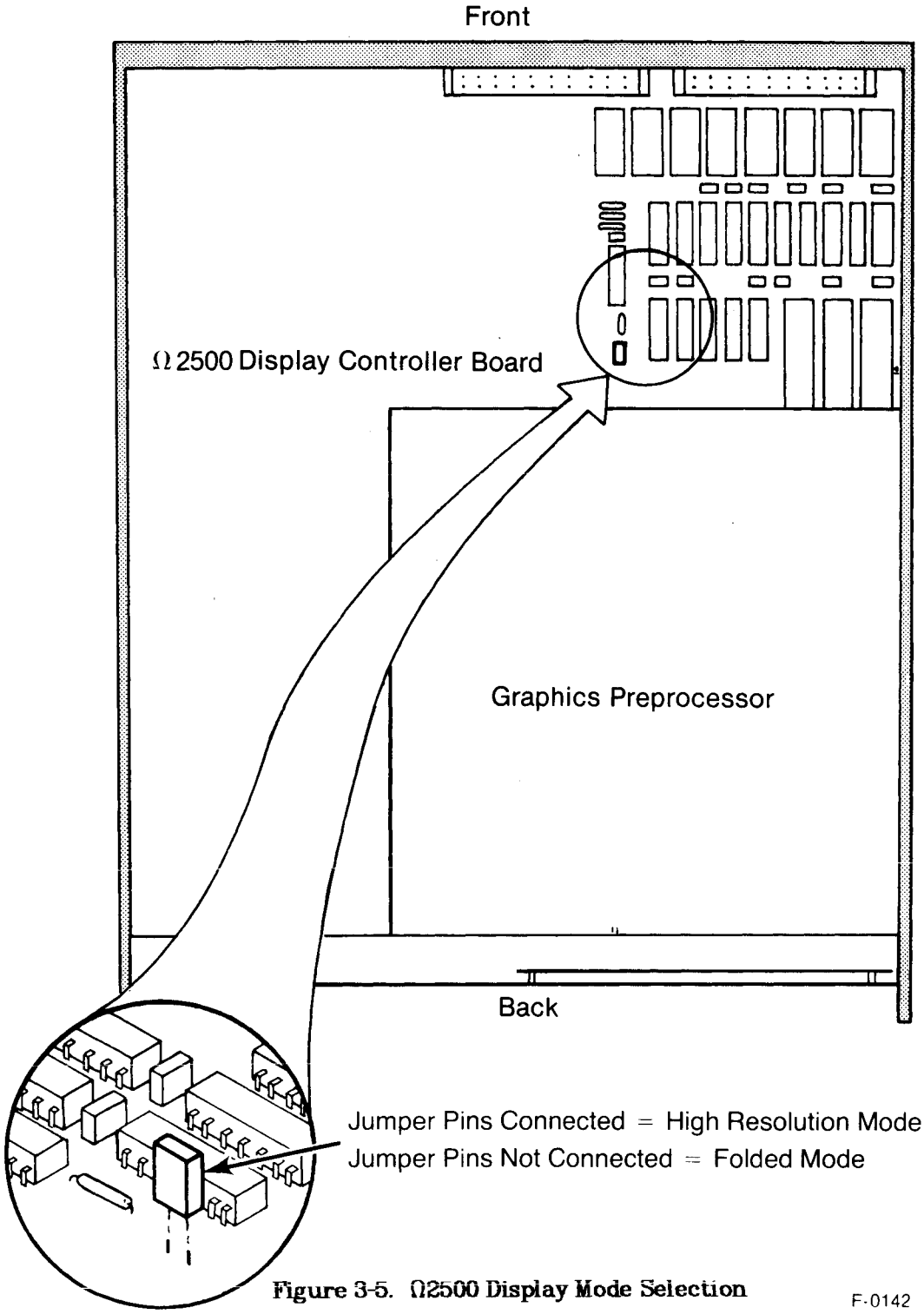

Figure 3-5. Ω2500 Display Mode Selection

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CONNECTING TO THE HOST

You have a choice of three ports to use for host computer communications: the 16-bit parallel port, the GPIB port, and the serial port. Figure 3-6 is a diagram showing the interconnecting cables for the three ports.

Parallel Port

In standard versions of the Ω2000-Series Graphics Controllers, the parallel port is configured for the DR11-W (or equivalent) interfaces used in Digital Equipment Corporation computers. Two 40-conductor ribbon cables with female connectors on each end are required for this port, one for input and one for output data. The cables are not supplied with the graphics controller.

As shown in Figure 3-6, The input-data cable (from host to graphics controller) connects to J6 (labeled HOST IN) on the rear panel of the graphics controller. At the host end, the input-data cable connects to J1 (Output) on the DR11-W interface. The output-data cable (from graphics controller to host) connects to J5 (labeled HOST OUT) on the back panel of the graphics controller. At the host end, the output-data cable connects to J2 (Input) on the DR11-W interface.

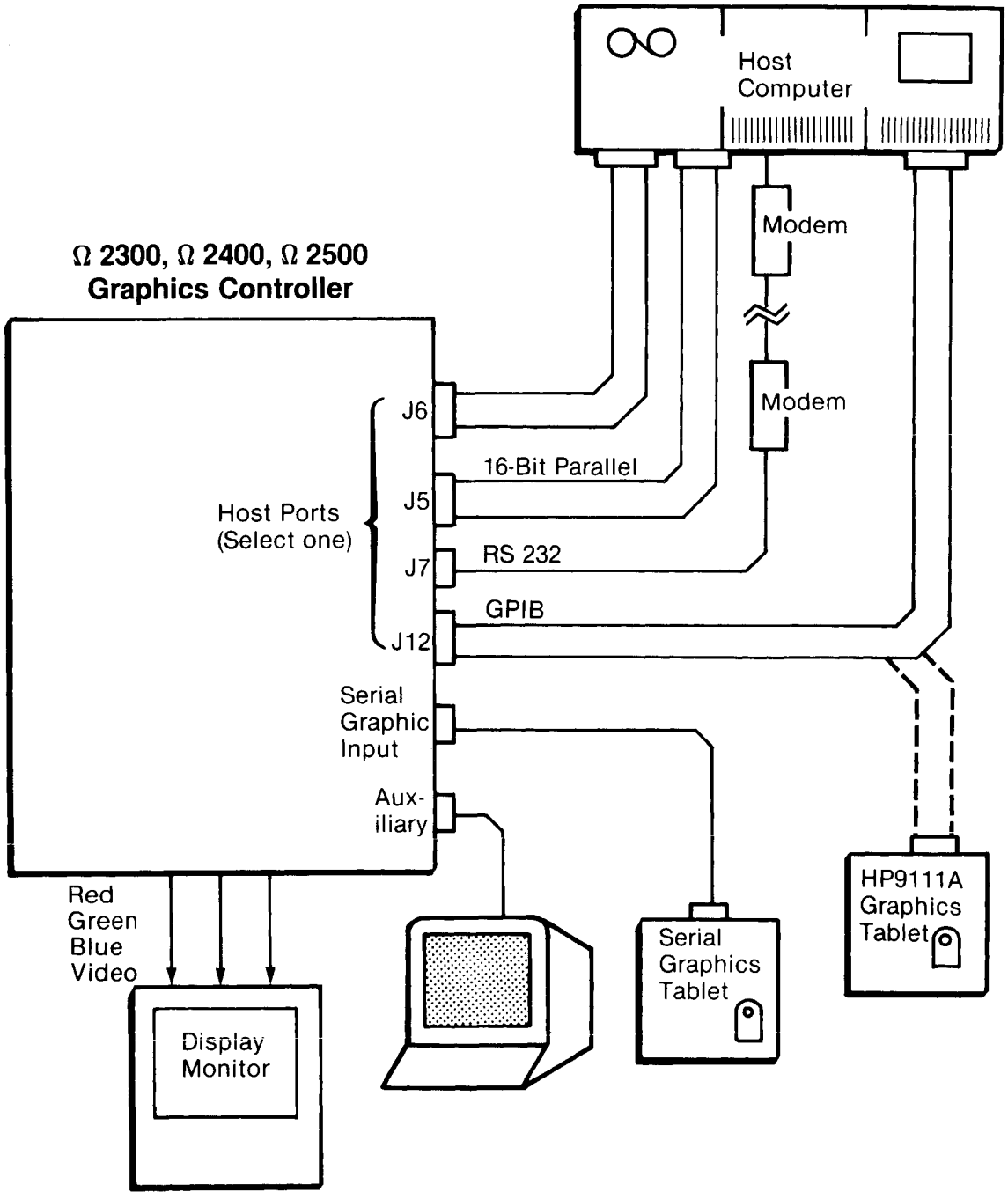


Figure 3-6. Graphics Controller Interconnections

NOTE

The maximum recommended cable lengths for the DR11-W interface are 50 feet (15.2 m) when using shielded cable, and 10 feet (3 m) when using unshielded cable.

The configuration switch settings required on the DR11-W interface board in the host are listed below. (These apply only to the DEC DR11-W interface, and not necessarily to other compatible interfaces.) Refer to the DR11-W user's guide (listed in the preface) for additional details.

- Select DR11-W link mode by setting E105 as follows:

  E105-1 to off
  E105-2 to on
  E105-3 to off
  E105-4 to on
  E105-5 to on

- Set the burst mode switch to 2-Cycle mode.
- Set the bus and vector addresses. (This depends on the particular host installation.)

GPIB Port

If the GPIB port has been selected for host communications, a standard GPIB cable is required to connect the graphics controller to the host. As shown in figure 3-6, the GPIB cable connects to J12 (labeled GPIB PROG) on the rear panel of the graphics controller.

NOTE

To comply with IEEE 488-1978, the maximum length of cable that can be used to connect together all devices in one GPIB system is 20 meters, or 2 meters multiplied by the number of devices in the system, whichever is less. Individual cable lengths greater than 4 meters should be used with caution.

Serial Port

For serial host communications, a 25-pin female RS-232 (labeled RS232 HOST) is provided on the back panel of the graphics controller. The port is set up to act as a terminal (DTE device), providing the inputs and outputs necessary to connect to a modem (DCE device). The RS-232 cable requires a male DB25P-type connector on the graphics controller end and, typically, on the modem end as well.

The signal lines provided by the port are listed in Appendix B. The number of signal lines needed in the interface cable depends on the mode of flow control selected by the configuration switches on the graphics preprocessor board. Typically, if "XON/XOFF" flow control or no flow control is selected, only the transmit and receive data lines and grounds (and in some cases DTR) will be required; however, if "modem" flow control is selected, the CTS and RTS signal will be required as well. For additional information on flow control configuration, refer to *Host Serial Data-Flow Control* earlier in this section. See also *Host Port Baud-Rate* for instructions on setting the baud rates for the port. See *Host Port Selection* for information on binary and hexadecimal serial data formats.

CONNECTING GRAPHIC-INPUT DEVICES

Graphic-input devices may be connected either to the designated RS-232 serial port or to the GPIB port. The designated RS-232 port, labeled J4 RS232 TABLET accepts input from Summagraphics Bit Pad and GTCO Digi-Pad graphics tablets (or equivalent devices). Use the RS-232 cables supplied with these devices to connect to the tablet port. Before connecting the graphic-input device, refer to to *Graphic-Input Baud Rate* and *Graphic-Input Data Format*, earlier in this chapter, which provide instructions for configuring the port.

The configuration switches on the Summagraphics Bit Pad One should be set as follows:

Switch	Setting
1-9	On
1-8	Off
1-7	On
1-6 thru 1-1	Do not change
2-6	Off
2-5	On
2-4	Off
2-3	On
2-2	Off
2-1	On
7-2	On (all other sections off)

The configuration switches on the GTCO Digi-Pad should be set as follows:

Switch	Setting	Switch	Setting	Switch	Setting
1-1	Off	2-1	On	3-1	Off
1-2	Of	2-2	Off	3-2	Off
1-3	Off	2-3	Off	3-3	Off
1-4	On	2-4	Off	3-4	On
1-5	Off	2-5	*	3-5	On
1-6	Off	2-6	Off	3-6	Off
1-7	Off	2-7	Off	3-7	On
1-8	On	2-8	Off	3-8	Off

* Off = low resolution; On = high resolution.

Refer to the Summagraphics and GTCO manuals listed in the Preface for additional configuration information on those devices.

A Hewlett-Packard[1] 9111A Graphics Tablet may be connected to te GPIB port (labeled J12 GPIB PROG), provided that the port has not been assigned to the host. A standard GPIB cable is required. No further configuration of the GPIB port is required; however, the tablet must be set up as follows:

- The GPIB address must be set to 6.
- The tablet's self-test switch must be set to the "0" position.

Refer to the user's manual for the graphics tablet (listed in the preface) for instructions on setting up the tablet.

CONNECTING A TERMINAL TO THE AUXILIARY PORT

A terminal may be connected to the auxiliary (debug) RS-232 port (labeled J11 RS-232 AUX) to query the graphics preprocessor about the status of graphics commands it has received and to display a message showing the installed firmware version number.

The auxiliary port is configured as a modem (DCE) device, providing a 25-pin female connector with the DSR (Data Set Ready) output, CTS (Clear To Send) output, and RTS (Request To Send) input signals, in addition to the Receive and Transmit data lines.

The port can be used with most TTY-type terminals providing asynchronous communications at baud rates supported by the auxiliary port. Refer to *Auxiliary Port Baud-Rate Selection* earlier in this chapter.

[1]Hewlett-Packard is a trademark of Hewlett-Packard Corporation.

CONNECTING THE DISPLAY MONITOR

The Ω2300 and Ω2400 Graphics Controllers provide three BNC-type connectors for red, green and blue video output to the display monitor. The Ω2500 family has two additional outputs, HSYNC and VSYNC, for those applications that require separate horizontal and vertical sync signals. Connect the graphics controller to the monitor using 75 Ohm coaxial cables. (Three 6-foot cables are supplied with the graphics controller.)

NOTE

Always use video cables of equal length for all video outputs. If the cables are different lengths, the video signals will be out of phase with one another.

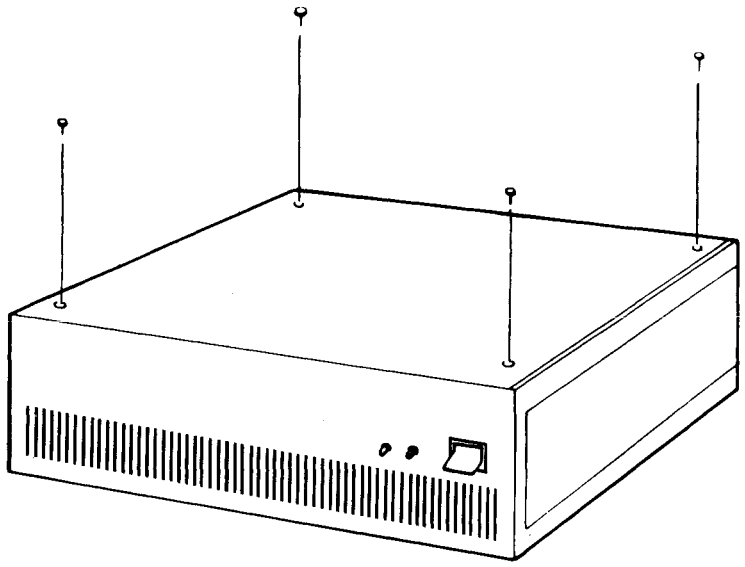
REMOVING THE TOP COVER

To remove the top cover you need a posidrive-type screwdriver.

WARNING

The following procedures could expose you to hazardous voltages. To avoid possible personal injury and damage to the graphics controller, always turn off the power switch, disconnect the power cord from the AC power outlet before removing the top panel.

1. Turn off the graphics controller's power switch and disconnect the power cord from the AC outlet.
2. Referring to Figure 3-8, remove the screws holding the top cover in place and lift off the cover. (The Ω2300 and Ω2400 each have four screws; the Ω2500 has ten.)



Remove 4 screws in Ω 2300 and Ω 2400, 10 screws in Ω 2500

F-0140

Figure 3-8. Removing the Top Cover

REMOVING THE GRAPHICS PREPROCESSOR BOARD

To remove the graphics preprocessor board, you need a posidrive-type screwdriver.

1. Remove the graphics controller's top cover as described previously.
2. Referring to Figure 3-9, disconnect the interface cables from the graphics preprocessor board.
3. Remove the nine screws attaching the graphics preprocessor to the display processor board.

4. Carefully disconnect the graphics preprocessor board from the Display Processor board. The inter-board connector is located toward the left rear of the chassis, under the graphics preprocessor.

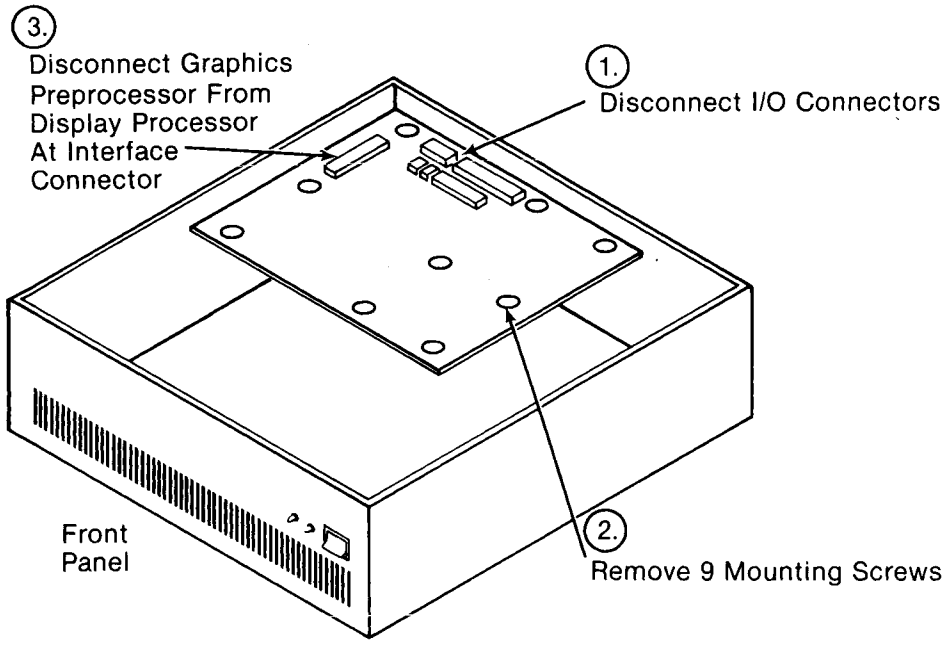


Figure 3-9. Removing the Graphics Preprocessor

REMOVING AND REPLACING THE FUSE

WARNING

To avoid possible personal injury and damage to the equipment, always turn off the power switch and disconnect the power cord before removing and replacing the fuse.

The AC line fuse is located on the back panel of the graphics controller (See Figure 2-2). To remove the fuse you need a flat-bladed screwdriver suitable for #6 screws. Unscrew the fuse counter clockwise using the screwdriver, then pull it out of its socket. Replace the fuse with one of the correct amperage, voltage, and size, as follows:

240 Volt Range:	2A, 250 volt, (Littlefuse type 312 or equivalent)
120 Volt Range:	4A, 250 volt, (Littlefuse type 312 or equivalent)

CAUTION

The power supplies contain fuses as well. Do not replace these fuses if they are blown; additional damage to the graphics controller or power supplies could result. If the main AC fuse blows more than once, call Metheus for service.

Appendix A
Specifications

Tables A-1 through A-6 list the electrical, mechanical, environmental, and functional specifications of the graphics controller.

Table A-1. Electrical Specifications

Characteristic	Specification	Supplemental Information
AC power requirements	90-132 VAC @ 4A 180-264 VAC @ 2A	47-63 Hz
Interface signals		
Serial port 0 (host)	Conforms to EIA RS-232	Signal levels set by the type of drivers installed on the back panel circuit board
Serial port 1 (aux)	Same as above	
Serial port 2 (kbd)	Conforms to EIA RS-423	
Serial port 3 (tablet)	Standard TTL	
GPIB port	Conforms to IEEE 488-1978	
parallel port	Compatible with DEC DR11-W interface	Signals configured on back panel circuit board

Table A-2. Mechanical Specifications

Characteristic	Specification
Width	17.0 inches
Height	5.25 inches
Depth	21.0 inches
Weight	30 lb

Table A-3. Environmental Specifications

Characteristic	Specification	Supplemental Information
Operating temperature	0 to 40° C (except Ω2530D: 0 to 55°)	
Humidity	0% to 90%	Noncondensing
EMI	VDE 0871 Class A FCC Class A	

Table A-4. Serial Port Functional Specifications

Characteristic	Specification	Supplemental Information
Baud rates		All ports: 8 bits/character 1 stop bit No parity
Port 0 (host)	300, 1200, 2400, 4800, 9600, 19.2 K	
Port 1 (aux)	300, 1200, 2400, 9600	
Port 2 (kbd)	not available	
Port 3 (tablet)	300, 1200, 2400, 9600	

Table A-5. GPIB Port Functional Specifications

Characteristic	Specification
IEE488-1978 compliance	Basic talker, basic listener, controller
Data transfer rate (burst)	250K bytes/sec

Table A-6. Parallel Port Functional Specifications

Characteristic	Specification	Supplemental Information
Compatibility	DEC DR11-W	Other interfaces may be supported (optional)
Data transfer rate (burst)	1M byte/sec	

Appendix B
Cabling Diagrams and Back Panel Connectors

This appendix contains an internal interconnection diagram for the graphics controller. It also correlates signal names with pin numbers for all I/O connectors on the graphics controller's back panel.

GRAPHICS CONTROLLER INTERCONNECTION DIAGRAM

Figure B-1 is a a diagram showing the interconnections between the graphics controller's components.

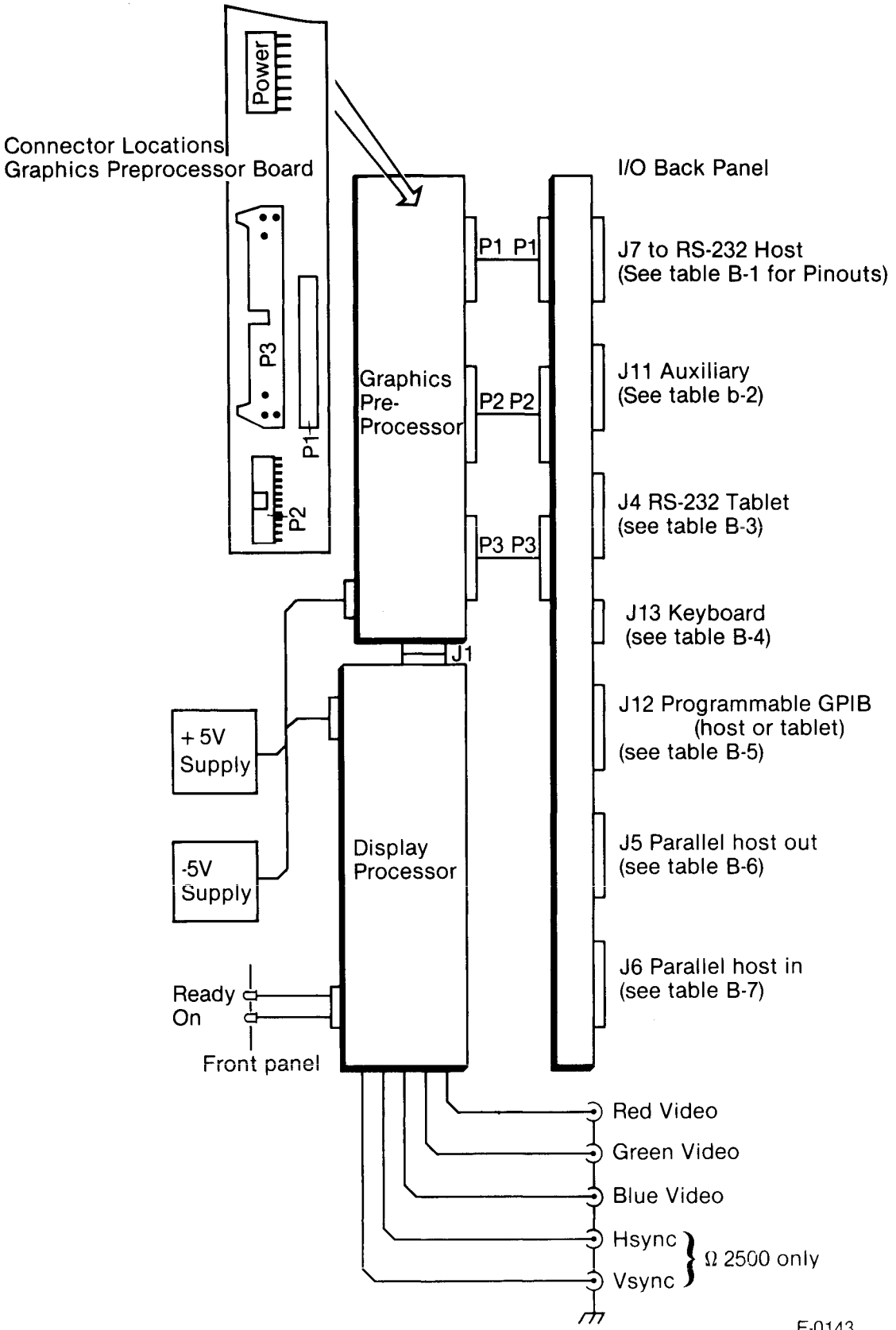


Figure B-1. Graphics Controller Interconnection Diagram

I/O CONNECTOR PIN DESCRIPTIONS

This section lists the signals carried by the graphics controller's rear panel I/O connectors, along with the pin number for each signal. The connectors are listed in several tables, as follows:

Table B-1	Host RS-232 connector.
Table B-2	Auxiliary RS-232 connector.
Table B-3	Tablet RS-232 connector.
Table B-4	Keyboard connector.
Table B-5	GPIB connector.
Table B-6	Host parallel-output connector.
Table B-7	Host parallel-input connector.

Table B-1. Host RS-232 Connector Pins

Pin Number	Signal
1	Protective ground
2	Data (to host)
3	Data (from host)
4	Request to send (RTS)
5	Clear to send (CTS)
7	Signal ground
20	Data terminal ready (DTR)

Table B-2. Auxiliary RS-232 Connector Pins

Pin Number	Signal
1	Protective ground
2	Data (from terminal)
3	Data (to terminal)
4	Request to send (RTS)
5	Clear to send (CTS)
6	Data set ready (DSR)
7	Signal ground

Table B-3. Tablet RS-232 Connector Pins

Pin Number	Signal
1	Protective ground
2	Data (from tablet)
3	Data (to tablet)
4	Request to send (RTS)
5	Clear to send (CTS)
6	Data set ready (DSR)
7	Signal ground

Table B-4. Keyboard Connector Pins

Pin Number	Signal
1	Ground
2	Data (to graphics controller)
3	Data (from graphics controller)
4	Reset
5	+5 VDC
6	Ground

Table B-5. GPIB Connector Pins

Pin Number	Signal
1	DIO1
2	DIO2
3	DIO3
4	DIO4
5	EOI
6	DAV
7	NRFD
8	NDAC
9	IFC
10	SRQ
11	ATN
12, 18-24	Ground
13	DIO5
14	DIO6
15	DIO7
16	DIO8
17	REN

Table B-6. Host Parallel Output Connector Pins

Pin Number	Signal	Pin Number	Signal
1	Ground	21	Ground
2	Cycle RQ A	22	Cycle RQ B
3	Ground	23	Ground
4	--	24	Ground
5	Ground	25	OUT7
6	READY	26	OUT8
7	Ground	27	OUT6
8	WC INC ENB	28	OUT9
9	BURST RQ	29	OUT3
10	STAT A	30	OUT10
11	Ground	31	OUT4
12	INIT	32	OUT11
13	Ground	33	OUT3
14	STAT B	34	OUT12
15	Ground	35	OUT2
16	--	36	OUT13
17	Ground	37	OUT1
18	STAT C	38	OUT14
19	Ground	39	OUT0
20	--	40	OUT15